HIGH POWER SP4T SWITCH GaAs MMIC

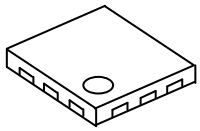
■ GENERAL DESCRIPTION

The NJG1684ME2 is a GaAs SP4T switch MMIC suitable for LTE/UMTS/CDMA/GSM applications.

The NJG1684ME2 features very low insertion loss, high isolation and excellent linearity performance down to 1.8V control voltage at high frequency up to 2.7GHz. In addition, this switch is able to handle high power signals.

The NJG1684ME2 has ESD protection devices to achieve excellent ESD performances. No DC Blocking capacitors are required for all RF ports unless DC is biased externally. And the ultra small & ultra thin EQFN12-E2 package is adopted.

■ PACKAGE OUTLINE



NJG1684ME2

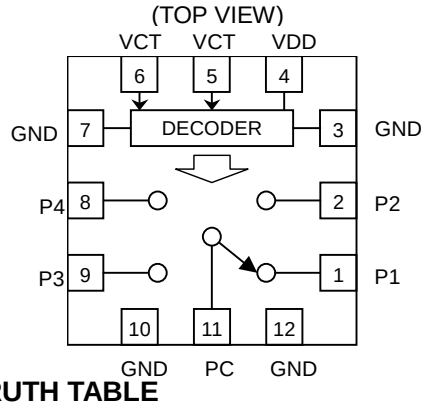
■ APPLICATIONS

LTE, UMTS, CDMA, GSM applications
Post PA Switching, Antenna Switching and Bands Switching applications
General Purpose Switching applications

■ FEATURES

● Low voltage logic control	$V_{CTL(H)}$=1.8V typ.
● Low voltage operation	V_{DD}=2.7V typ.
● Low distortion	IIP3=+70dBm typ. @f=829+849MHz, P_{IN}=24dBm
	IIP3=+69dBm typ. @f=1870+1910MHz, P_{IN}=24dBm
	2nd harmonics=-80dBc typ. @f=0.9GHz, P_{IN}=35dBm
	3rd harmonics=-77dBc typ. @f=0.9GHz, P_{IN}=35dBm
● Low insertion loss	0.25dB typ. @f=0.9GHz, P_{IN}=35dBm, V_{DD}=2.7V
	0.30dB typ. @f=1.9GHz, P_{IN}=33dBm, V_{DD}=2.7V
	0.35dB typ. @f=2.7GHz, P_{IN}=27dBm, V_{DD}=2.7V
● $P_{-0.1dB}$	36dBm min.
● Ultra small & ultra thin package	EQFN12-E2 (Package size: 1.8 x 1.8 x 0.397mm)
● RoHS compliant and Halogen Free, MSL1	

■ PIN CONFIGURATION



Pin connection

1. P1	7. GND
2. P2	8. P4
3. GND	9. P3
4. VDD	10. GND
5. VCTL2	11. PC
6. VCTL1	12. GND

Exposed PAD: GND

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

VCTL1	VCTL2	Path
L	L	PC-P1
H	L	PC-P2
L	H	PC-P3
H	H	PC-P4

NOTE: Please note that any information on this catalog will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

T_a=+25℃, Z_s=Z_l=50ohm

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	V_{DD} =2.7V, V_{CTL}=0/1.8V	37	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL1, VCTL2 terminal	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB with through-hole (101.5x114.5mm), Tj=150℃	1200	mW
Operating Temp.	T_{opr}		-40~+85	℃
Storage Temp.	T_{stg}		-55~+150	℃

■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions: T_a=+25℃, Z_s=Z_l=50ohm, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	VDD Terminal	2.375	2.7	5.0	V
Operating Current	I_{DD}	No RF input	-	180	400	μA
Control Voltage (LOW)	$V_{CTL(L)}$	VCTL1, VCTL2 Terminal	0	-	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$	VCTL1, VCTL2 Terminal	1.35	1.8	5.0	V
Control Current	I_{CTL}	$V_{CTL(H)}$=1.8V	-	4	10	μA

■ ELECTRICAL CHARACTERISTICS 2 (RF)

(General conditions: T_a=+25℃, Z_s=Z_l=50ohm, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	f=0.9GHz, P_{IN}=35dBm	-	0.25	0.40	dB
Insertion Loss 2	LOSS2	f=1.9GHz, P_{IN}=33dBm	-	0.30	0.45	dB
Insertion Loss 3	LOSS3	f=2.7GHz, P_{IN}=27dBm	-	0.35	0.50	dB
Isolation 1	ISL1	f=0.9GHz, P_{IN}=35dBm	30	37	-	dB
Isolation 2	ISL2	f=1.9GHz, P_{IN}=33dBm	25	29	-	dB
Isolation 3	ISL3	f=2.7GHz, P_{IN}=27dBm	22	25	-	dB
Input Power at 0.1dB Compression Point	$P_{-0.1dB}$	f=0.9GHz, 1.9GHz, 2.7GHz	36	-	-	dBm
2nd Harmonics 1	2fo(1)	f=0.9GHz, P_{IN}=35dBm	-	-80	-70	dBc
2nd Harmonics 2	2fo(2)	f=1.9GHz, P_{IN}=33dBm	-	-80	-70	dBc
2nd Harmonics 3	2fo(3)	f=2.7GHz, P_{IN}=27dBm	-	-90	-70	dBc
3rd Harmonics 1	3fo(1)	f=0.9GHz, P_{IN}=35dBm	-	-77	-70	dBc
3rd Harmonics 2	3fo(2)	f=1.9GHz, P_{IN}=33dBm	-	-77	-70	dBc
3rd Harmonics 3	3fo(3)	f=2.7GHz, P_{IN}=27dBm	-	-90	-70	dBc
Input 3rd order intercept point1	IIP3(1)	f=829+849MHz, P_{IN}=24dBm each *1	+65	+70	-	dBm
Input 3rd order intercept point2	IIP3(2)	f=1870+1910MHz, P_{IN}=24dBm each *1	+63	+69	-	dBm
VSWR	VSWR	On-state ports, f=2.7GHz	-	1.2	1.4	
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	1.0	5.0	μs

*1: IIP3 are defined by the following equations.
IIP3=(3 x Pout-IM3)/2+LOSS

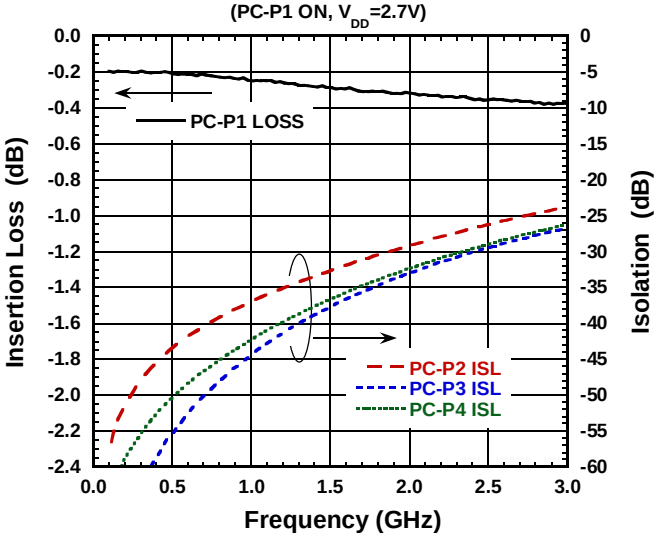
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	P1	RF transmitting/receiving port.
2	P2	RF transmitting/receiving port.
3	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
4	VDD	Positive voltage supply terminal. The positive voltage (+2.375~+5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
5	VCTL2	Control signal input terminal. This terminal is set to High-Level (+1.35~+5.0V) or Low-Level (0~+0.45V).
6	VCTL1	Control signal input terminal. This terminal is set to High-Level (+1.35~+5.0V) or Low-Level (0~+0.45V).
7	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
8	P4	RF transmitting/receiving port.
9	P3	RF transmitting/receiving port.
10	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
11	PC	RF transmitting/receiving port. Please connect an inductor with GND terminal for ESD protection.
12	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
Exposed Pad	GND	Ground terminal.

■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

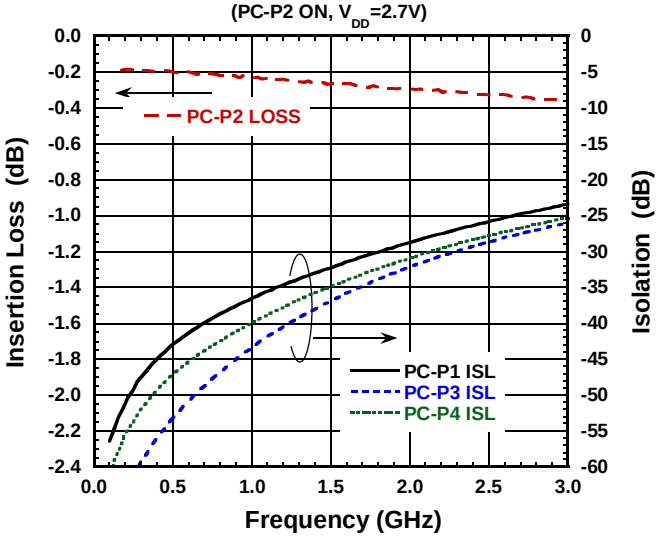
Loss, ISL vs Frequency

(PC-P1 ON, V_{DD}=2.7V)



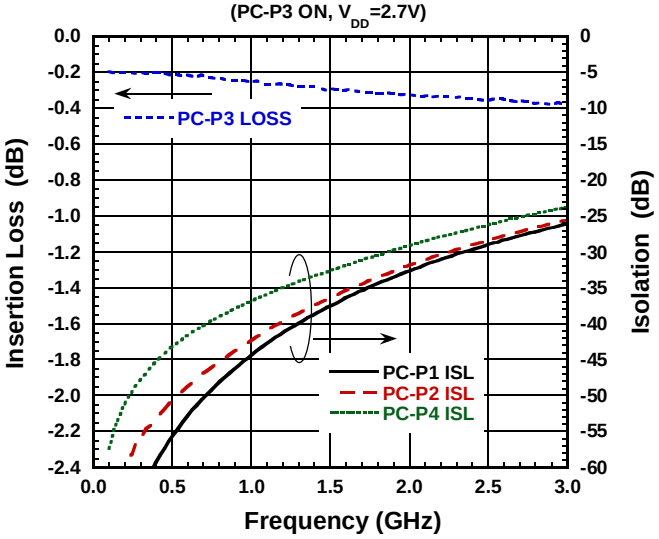
Loss, ISL vs Frequency

(PC-P2 ON, V_{DD}=2.7V)



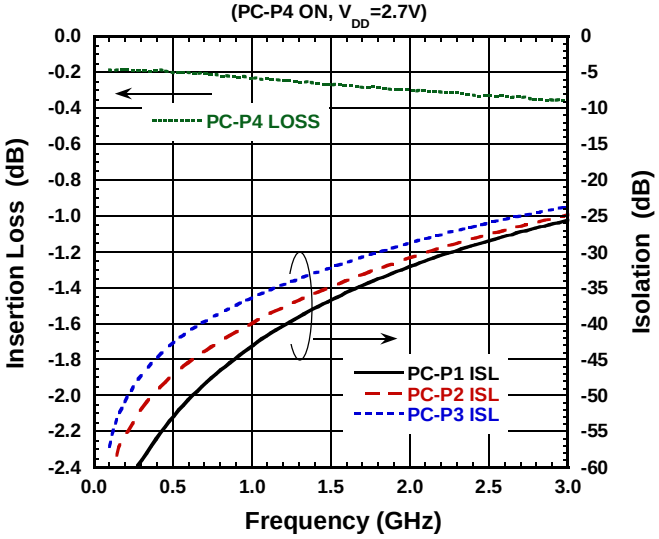
Loss, ISL vs Frequency

(PC-P3 ON, V_{DD}=2.7V)



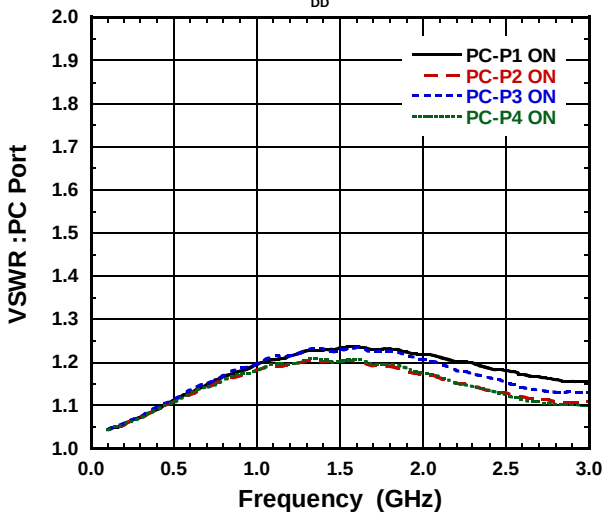
Loss, ISL vs Frequency

(PC-P4 ON, V_{DD}=2.7V)



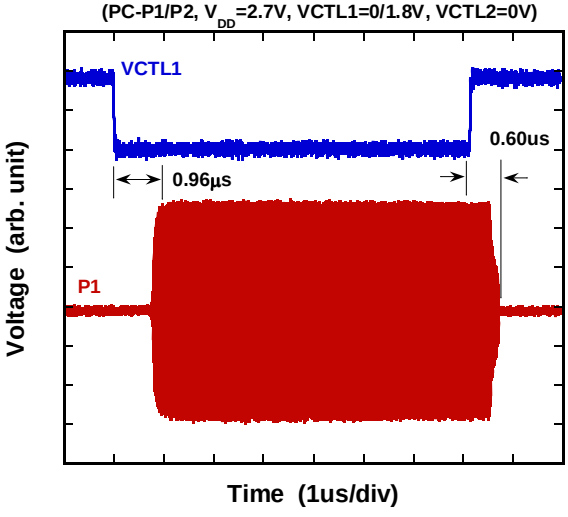
VSWR vs Frequency

(V_{DD}=2.7V)



Switching Time

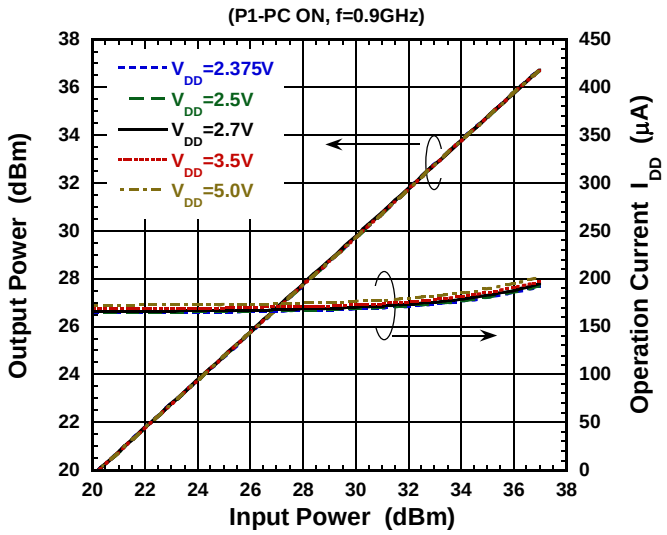
(PC-P1/P2, V_{DD}=2.7V, VCTL1=0/1.8V, VCTL2=0V)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

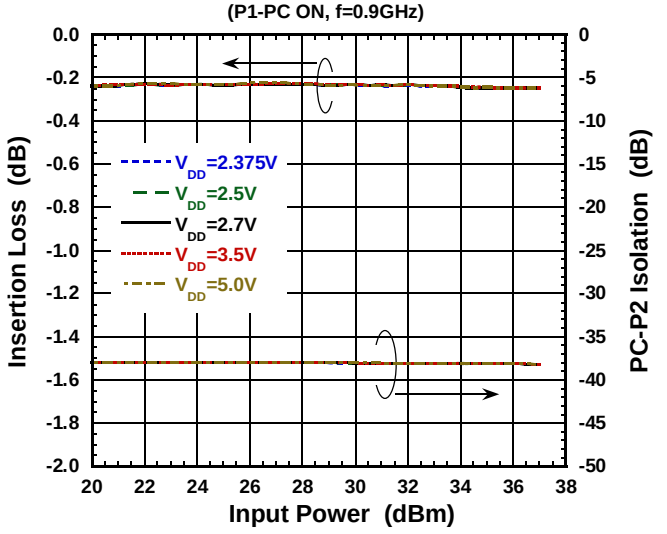
Output Power, I_{DD} vs Input Power

(P1-PC ON, f=0.9GHz)



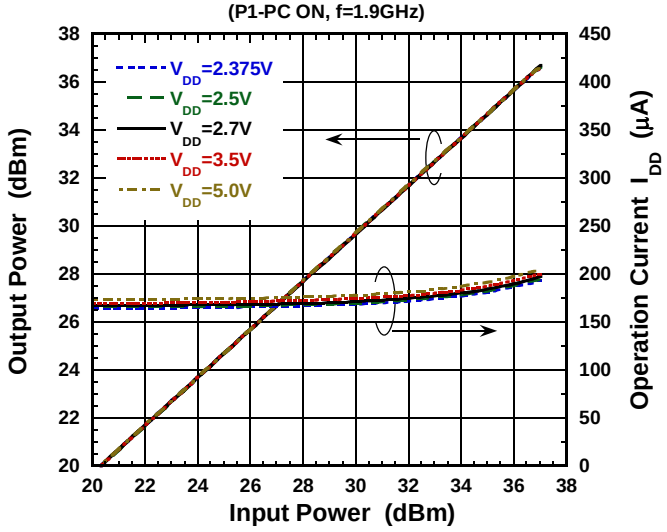
Loss, ISL vs Input Power

(P1-PC ON, f=0.9GHz)



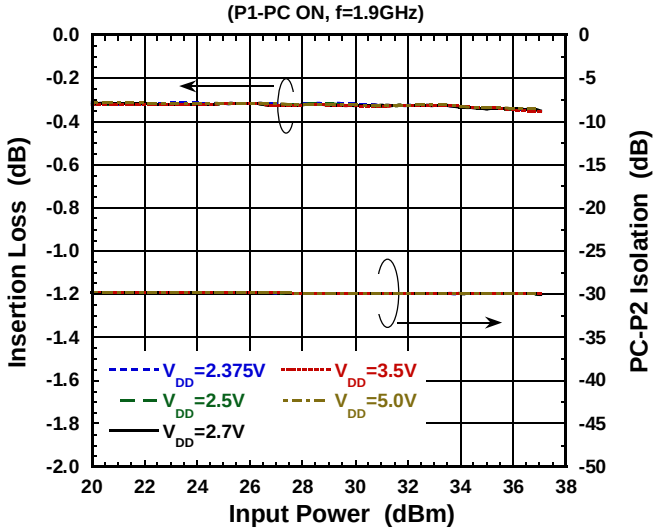
Output Power, I_{DD} vs Input Power

(P1-PC ON, f=1.9GHz)



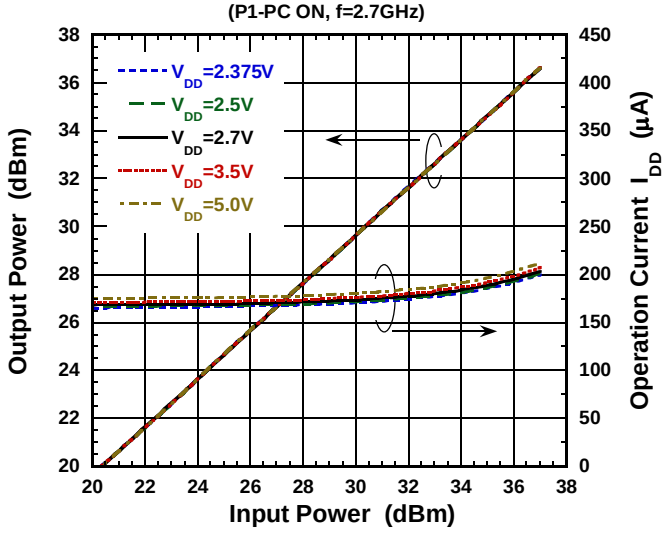
Loss, ISL vs Input Power

(P1-PC ON, f=1.9GHz)



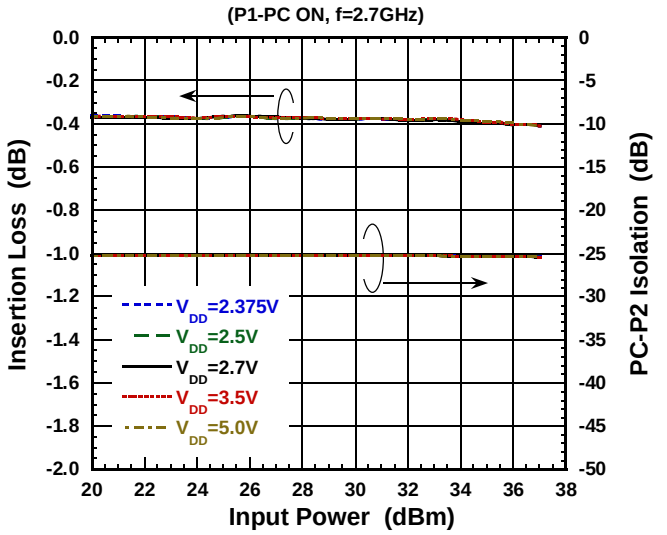
Output Power, I_{DD} vs Input Power

(P1-PC ON, f=2.7GHz)



Loss, ISL vs Input Power

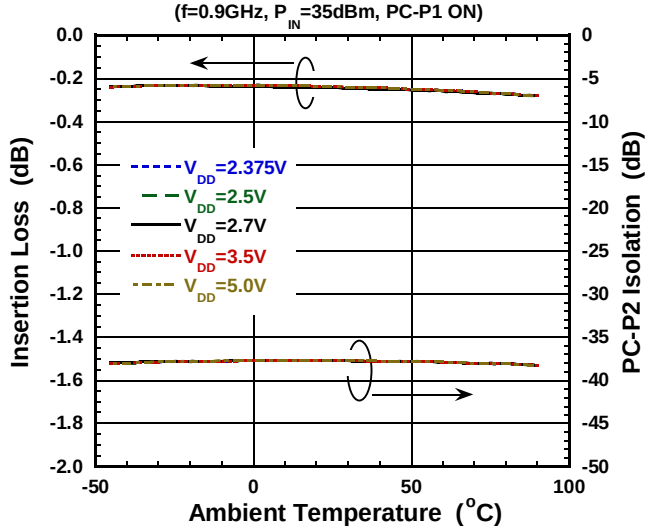
(P1-PC ON, f=2.7GHz)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

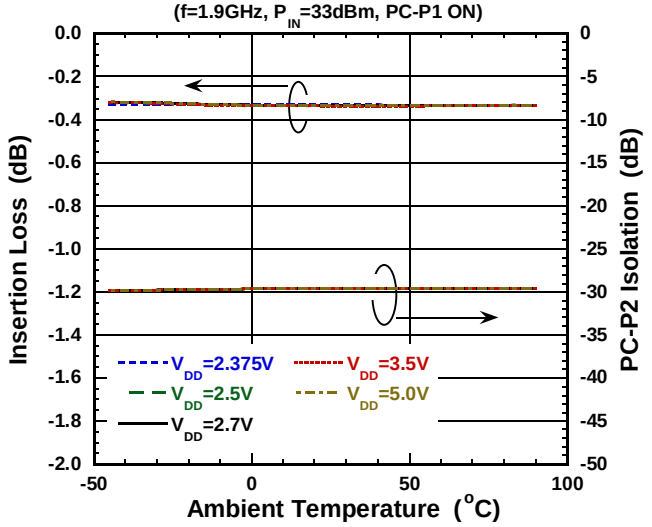
Loss, ISL vs Temperature

(f=0.9GHz, P_{IN}=35dBm, PC-P1 ON)



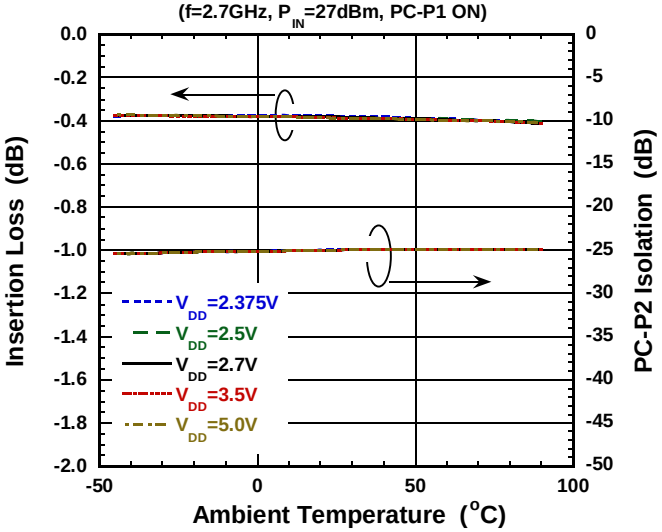
Loss, ISL vs Temperature

(f=1.9GHz, P_{IN}=33dBm, PC-P1 ON)



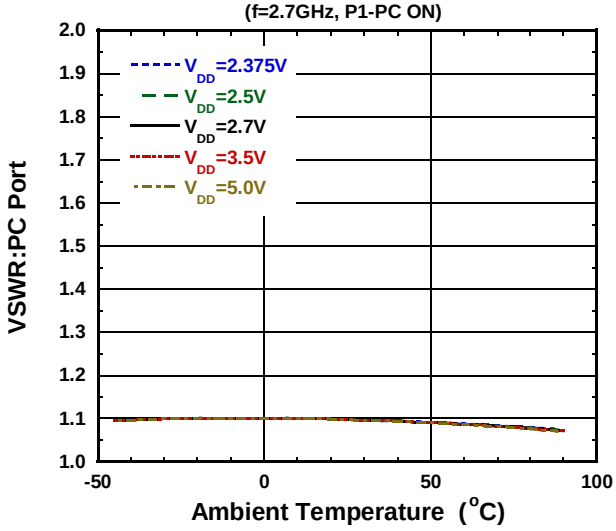
Loss, ISL vs Temperature

(f=2.7GHz, P_{IN}=27dBm, PC-P1 ON)



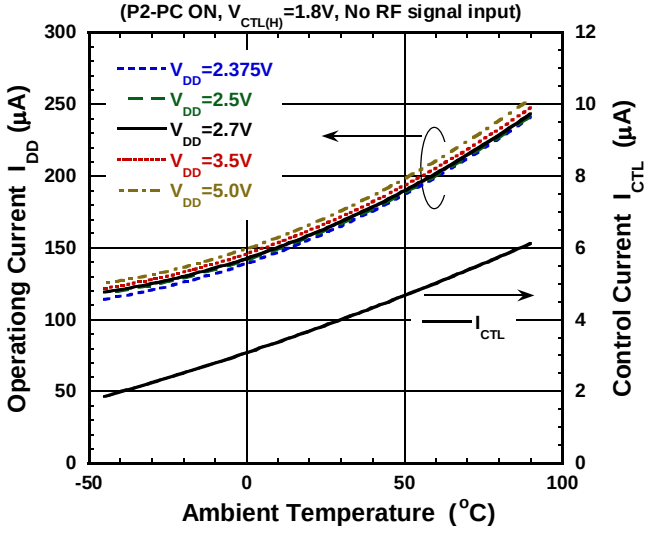
VSWR vs Temperature

(f=2.7GHz, P1-PC ON)



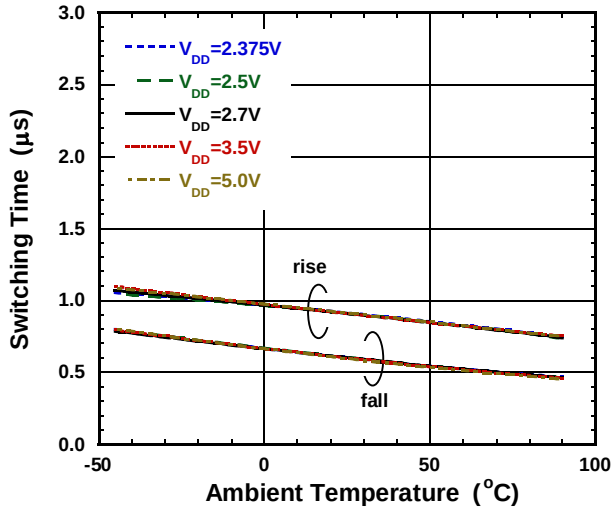
I_{DD}, I_{CTL} vs Temperature

(P2-PC ON, $V_{CTL(H)}$=1.8V, No RF signal input)



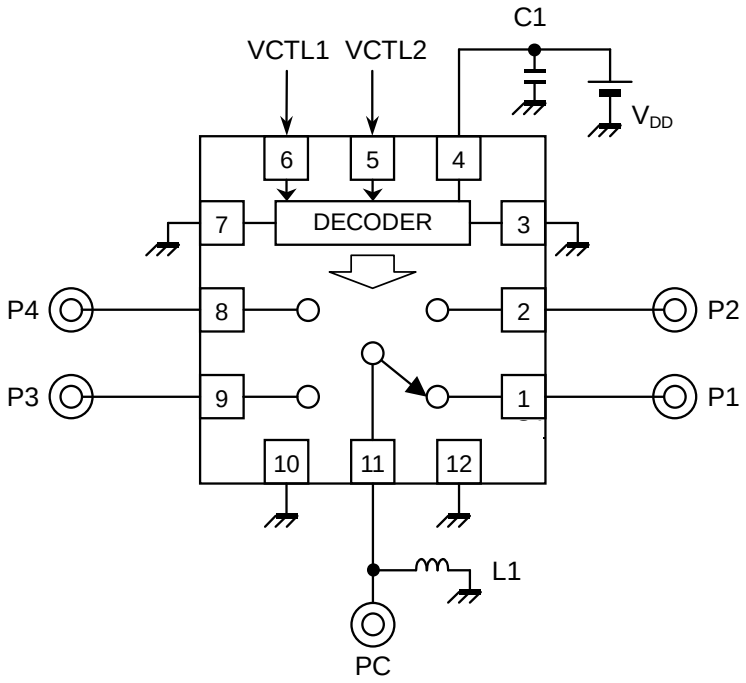
Switching Time vs Temperature

(PC-P1, VCTL1=H/L, VCTL2=L)



■ APPLICATION CIRCUIT

(TOP VIEW)



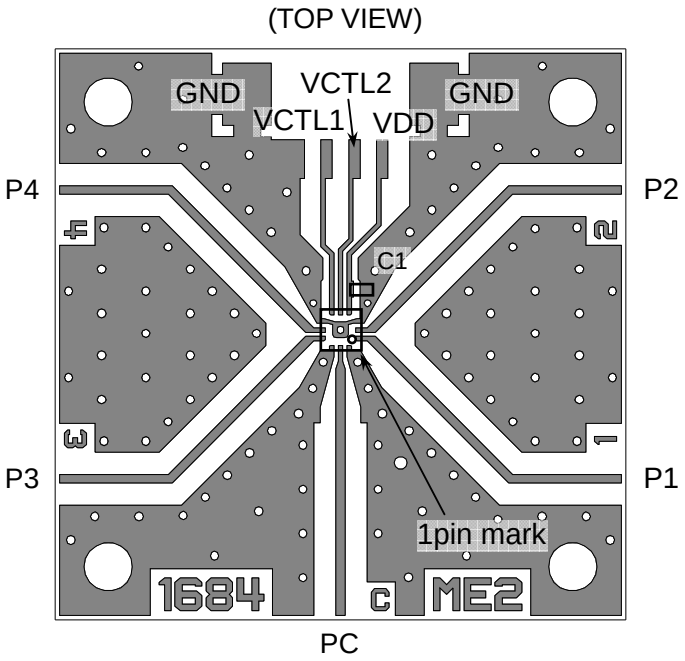
PRECAUTIONS

[1] The Inductor L1 is required for enhancing ESD protection level.
[2] All RF terminals are biased DC GND level.
[3] No DC block capacitors are required for RF ports unless DC is biased externally.

■ PARTS LIST

No.	Parameters	Note
C1	1000pF	MURATA (GRM15)
L1	68nH	TAIYO-YUDEN (HK1005)

■ PCB LAYOUT

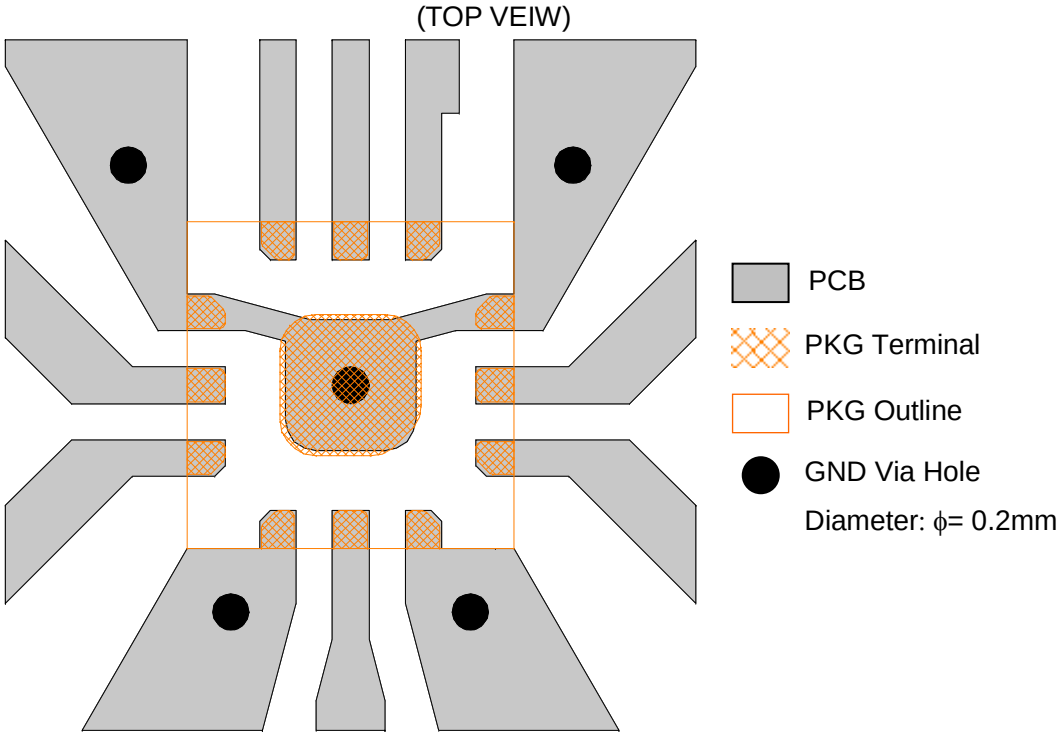


PCB:	FR-4, t=0.2mm
Capacitor Size:	1005
Strip Line Width:	0.4mm
PCB Size:	26 x 26mm

Losses of PCB and connectors, Ta=+25℃

Frequency (GHz)	Loss (dB)
0.9	0.27
1.9	0.50
2.7	0.61

<PCB LAYOUT GUIDELINE>



■ PRECAUTIONS

[1] No DC block capacitors are required for RF ports unless DC is biased externally. When the other device is biased at certain voltage and connected to the NJG1684ME2, a DC block capacitor is required between the device and the switch IC. This is because the each RF port of NJG1684ME2 is biased at 0 V (GND).

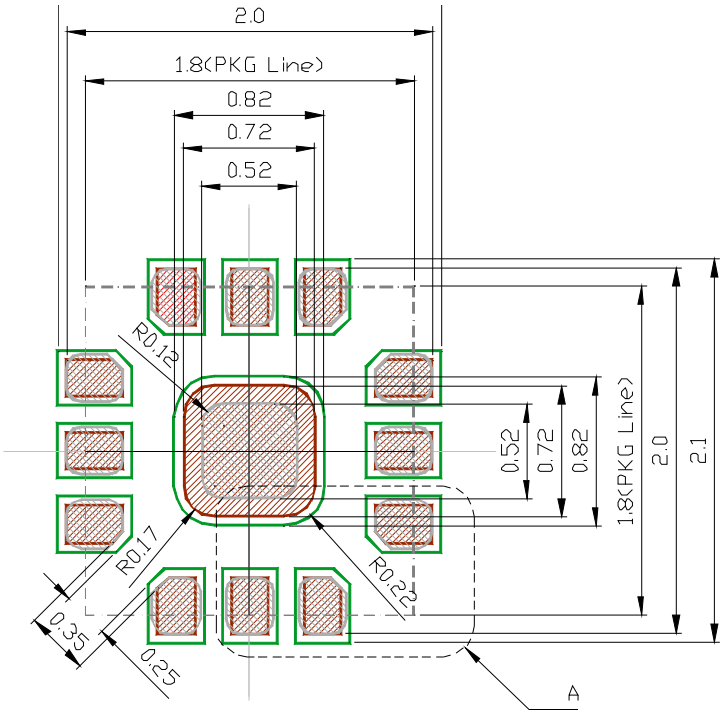
[2] For good RF performance, all GND terminals must be connected to PCB ground plane of substrate, and via-holes for GND should be placed near the IC.

[3] For good RF performance, through-holes for GND should be placed close to the GND pin 6 and pin 13. One of the ways to do this is to place a via-hole at the TAB pad under this IC.

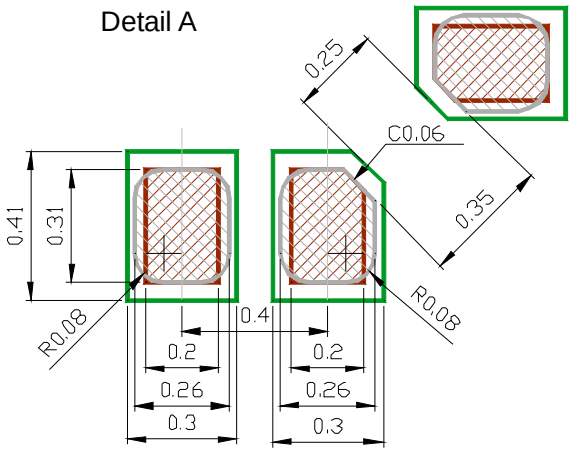
■ RECOMMENDED FOOTPRINT PATTERN (EQFN12-E2 PACKAGE Reference)

: Land
: Mask (Open area) *Metal mask thickness : 100um
: Resist(Open area)

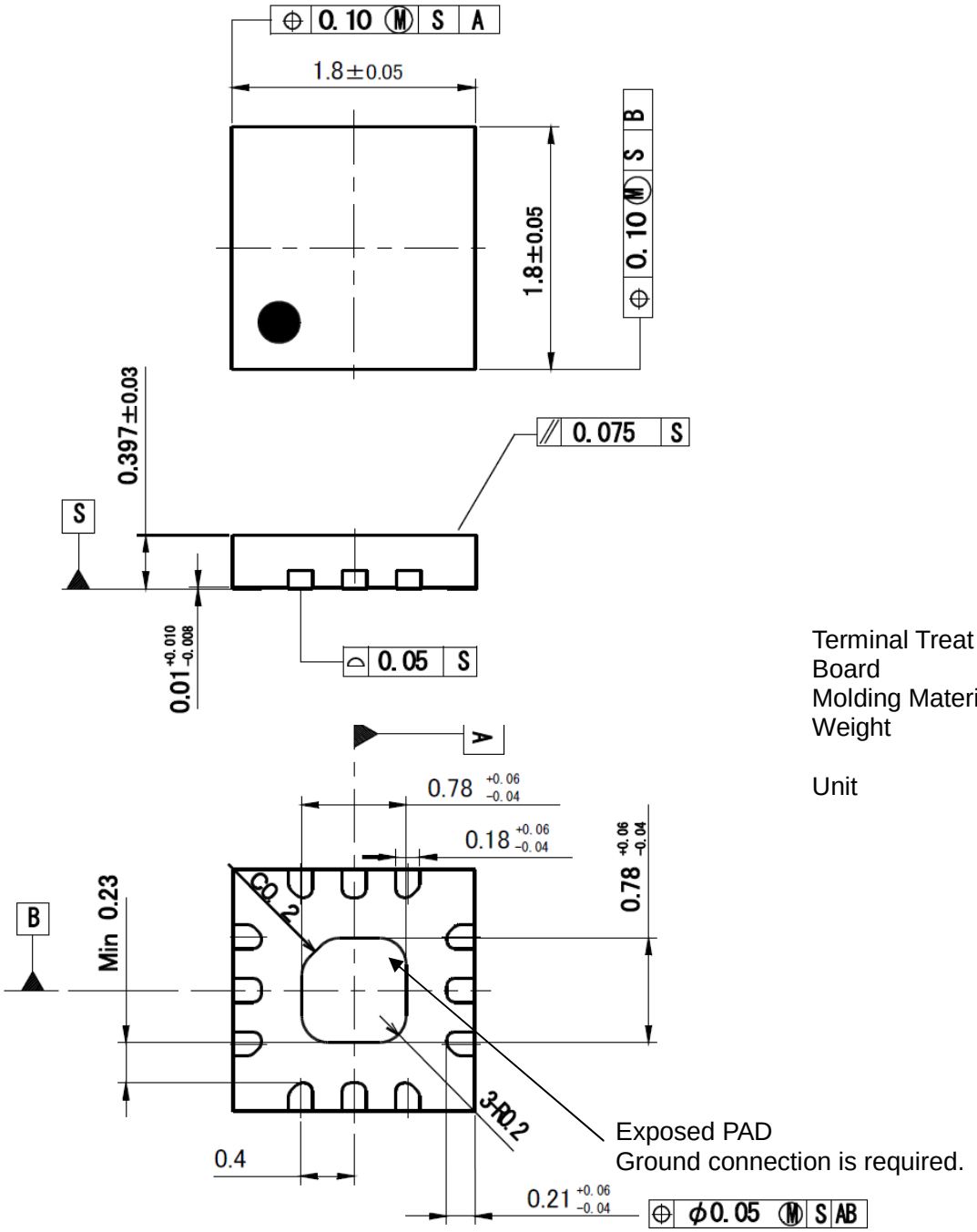
PKG : 1.8mm x 1.8mm
Pin pitch : 0.4mm



Detail A



■ PACKAGE OUTLINE (EQFN12-E2)



Terminal Treat	: SnBi
Board	: Copper
Molding Material	: Epoxy resin
Weight	: 3.7mg
Unit	: mm

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

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