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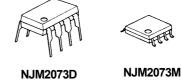


DUAL LOW VOLTAGE POWER AMPLIFIER

■ GENERAL DESCRIPTION

■ PACKAGE OUTLINE

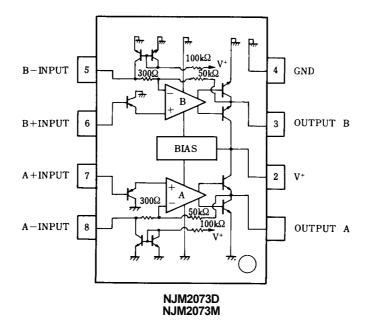
The NJM2073 is a monolithic integrated circuit in 8 lead dual-in-line package, which is designed for dual audio power amplifier in portable radio and handy cassette player.



■ FEATURES

- Operating Voltage (V⁺=1.8V~15V)
- Low Crossover Distortion
- Low Operating Current
- Bridge or Stereo Configuration
- No Turn-on Noise
- Package Outline
 DIP8,DMP8
- Bipolar Technology

■ PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	15	V
Output Peak Current	I _{OP}	1	Α
Power Dissipation	P _D	(DIP8) 700 (DMP8) 300	mW
Input Voltage Range	V _{IN}	± 0.4	V
Operating Temperature Range	T _{opr}	-40~+85	°C
Storage Temperature Range	T _{stg}	-40~+125	°C

■ ELECTRICAL CHARACTERISTICS D-Type

(1) BTL Configuration (Test Circuit Fig.1)

(V⁺=6V,Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
	V ⁺	TEST SONDITION		1111.		V
Operating Voltage	1	_	1.8	-	15	1
Operating Current	Icc	R _L =∞	-	6	9	mA
Output Offset Voltage	ΔV_{O}	$R_L=8\Omega$		10	50	mV
(Between the Outputs)						
Input Bias Current	lΒ		-	100	-	nA
Output Power	_	THD=10%,f=1kHz				
•	Po	$V^{\dagger}=9V,R_{L}=16\Omega$ (Note)	-	2.0	-	W
	Po	$V^{+}=6V,R_{L}=8\Omega$ (Note)	0.9	1.2	-	W
	Po	$V^{+}=4.5V,R_{L}=8\Omega$	-	0.6	-	W
	Po	$V^{\dagger}=4.5V,R_{L}=4\Omega$ (Note)	-	0.8	-	W
	Po	$V^{\dagger}=3V_{1}R_{L}=4\Omega$	200	300	-	mW
	Po	$V^{\dagger}=2V,R_{L}=4\Omega$		80	-	mW
		THD=1%.f=40Hz~15kHz				
	Po	$V^{\dagger}=6V,R_{L}=8\Omega$	_	1.0	-	W
	Po	$V^{+}=4.5V_{1}R_{1}=4\Omega$	-	0.6	-	W
Total Harmonic Distortion	THD	$P_0=0.5W$, $R_L=8\Omega$, $f=1kHz$	-	0.2	-	%
Close Loop Voltage Gain	A_{V}	f=1kHz	41	44	47	dB
Input Impedance	Z_{IN}	f=1kHz	100	-	-	kΩ
Equivalent Input Noise Voltage	V _{NI1}	R _S =10kΩ,A Curve	_	2	-	μV
4	V _{NI2}	R _S =10kΩ,B=22Hz~22kHz	_	2.5	_	μV
Ripple Rejection	RR	f=100Hz	_	40	_	dB
Cutoff Frequency	f _H	A_V =-3dB from f=1kHz,R _L =8 Ω ,P _O =1W	-	130	-	kHz

(Note) At on PC Board

(2) Stereo Configuration (Test Circuit Fig.2)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		1.8	-	15	V
Output Voltage	Vo		-	2.7	-	V
Operating Current	Icc	R _L =∞	-	6	9	mA
Input Bias Current	I _B		-	100	-	nA
Output Power (Each Channel)		THD=10%,f=1kHz				
	Po	V^{\dagger} =6V,R _L =4 Ω (Note)	0.5	0.65	-	W
	Po	$V^{+}=4.5V,R_{L}=4\Omega$	-	0.32	-	W
	Po	$V^{\dagger}=3V,R_{L}=4\Omega$	-	120	-	mW
	Po	$V^{\dagger}=2V,R_{L}=4\Omega$	-	30	-	mW
		THD=1%,f=1kHz				
	Po	$V^{\dagger}=6V,R_{L}=4\Omega$	-	500	-	mW
	Po	$V^{+}=4.5V,R_{L}=4\Omega$	-	250	-	mW
Total Harmonic Distortion	THD	P_O =0.4W, R_L =4 Ω , f =1kHz	-	0.25	-	%
Voltage Gain	A _V	f=1kHz	41	44	47	dB
Channel Balance	ΔA_{V}		-	-	± 1	dB
Input Impedance	Z_{IN}	f=1kHz	100	-	-	kΩ
Equivalent Input Noise Voltage	V _{NI1}	R _S =10kΩ,A Curve	-	2.5	-	μV
_	V_{Nl2}	R_S =10k Ω ,B=22Hz~22kHz	-	3	-	μV
Ripple Rejection	RR	f=100Hz,C _X =100µF	24	30	-	dB
Cutoff Frequency	f _H	A_V =-3dB from f=1kHz, R_L =8 Ω , P_O =250mW	-	200	ı	kHz

(Note) At on PC Board

■ ELECTRICAL CHARACTERISTICS M-Type

(1) BTL Configuration (Test Circuit Fig.1)

(V⁺=6V,Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		1.8	-	15	V
Operating Current	Icc	R _L =∞	-	6	9	mA
Output Offset Voltage	ΔV_{O}	$R_L=8\Omega$	-	10	50	mV
(Between the Outputs)						
Input Bias Current	I_{B}		-	100	-	nA
Output Power		THD=10%,f=1kHz				
	Po	V^{\dagger} =6V,R _L =16 Ω (Note)	-	8.0	-	W
	Po	$V^{\dagger}=4V,R_L=8\Omega$ (Note)	350	460	-	mW
	Po	V^{\dagger} =3V,R _L =4 Ω (Note)	200	300	-	mW
	Po	$V^{\dagger}=2V,R_{L}=4\Omega$	-	80	-	mW
		THD=1%,f=40Hz~15kHz				
	Po	$V^{\dagger}=4V,R_{L}=8\Omega$	-	380	-	mW
Total Harmonic Distortion	THD	V^{\dagger} =4V,R _L =8 Ω ,P _O =200mW,f=1kHz	-	0.2	-	%
Close Loop Voltage Gain	A_V	f=1kHz	41	44	47	dB
Input Impedance	Z_{IN}	f=1kHz	100	-	-	kΩ
Equivalent Input Noise Voltage	V_{NI1}	R _S =10kΩ,A Curve	-	2	-	μV
•	V_{NI2}	R_S =10k Ω ,B=22Hz~22kHz	-	2.5	-	μV
Ripple Rejection	RR	f=100Hz	-	40	-	dB
Cutoff Frequency	f⊢	A_V =-3dB from f=1kHz, R_L =16 Ω , P_O =0.5W	-	130	-	kHz

(Note) At on PC Board

(2) Stereo Configuration (Test Circuit Fig.2)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		1.8	-	15	V
Output Voltage	Vo		-	2.7	-	V
Operating Current	Icc	R _L =∞	-	6	9	mA
Input Bias Current	I_{B}		-	100		nA
Output Power (Each Channel)		THD=10%,f=1kHz				
	Po	$V^{+}=6V,R_{L}=16\Omega$	-	240	-	mW
	Po	$V^{+}=5V,R_{L}=8\Omega$ (Note)	-	270	-	mW
	Po	$V^{+}=4V,R_{L}=4\Omega$ (Note)	180	250	-	mW
	Po	$V^{+}=3V,R_{L}=4\Omega$	-	120	-	mW
	Po	$V^{+}=2V,R_{L}=4\Omega$	-	30	-	mW
		THD=1%,f=1kHz				
	Po	$V^{+}=4V,R_{L}=4\Omega$	-	180	-	mW
Total Harmonic Distortion	THD	$V^{+}=4V,R_{L}=4\Omega,P_{O}=150$ mW,f=1kHz	-	0.25	-	%
Voltage Gain	A_{V}	f=1kHz	41	44	47	dB
Channel Balance	ΔA_{V}		-	-	±1	dB
Input Impedance	Z_{IN}	f=1kHz	100	-	-	kΩ
Equivalent Input Noise Voltage	V_{NI1}	R _S =10kΩ,A Curve	-	2.5	-	μV
	V_{Ni2}	R_S =10k Ω ,B=22Hz~22kHz	-	3		μV
Ripple Rejection	RR	f=100Hz,C _X =100µF	24	30	-	dB
Cutoff Frequency	f_H	A_V =-3dB from f=1kHz, R_L =16 Ω , P_O =125mW	-	200	-	kHz

(Note) At on PC Board

■ TYPICAL APPLICATION & TEST CIRCUIT

Fig.1 BTL Configuration

Fig.2 Stereo Configuration

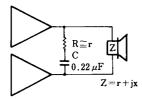
INPUT $2 \frac{1}{0.1\mu}$ 0.1μ $1 \frac{1}{2}$ 0.1μ $1 \frac{1}{2}$ 0.1μ $1 \frac{1}{2}$ 0.22μ $1 \frac{1}{2}$ $1 \frac{1}{2}$ 1

note:pin No.to D,M-Type

■ PARASTIC OSCILLATION PREVEMTING CIRCUIT

Put 1Ω+0.22μF on parallel to load,if the load is speaker.Recommend putting 0.1μF and more than 100μF capacitors with good high frequency characteristics in to near ground and supply voltage pins.

In BTL operation of less than 2V supply voltage, parastic oscillation may be occurred with R=1Ω. And so recommended R to be the same value of pure resistance(r) when it is lower than 3V.

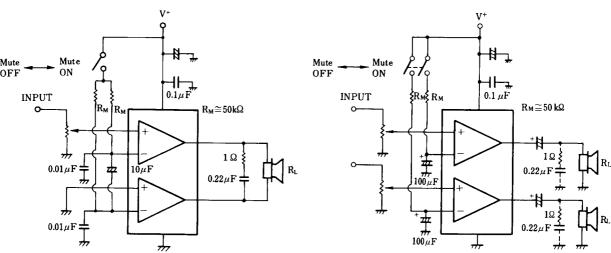


■ MUTING CIRCUIT

When Mute ON.OUTPUT level saturates to GND side.

Fig.3 BTL Configuration

Fig.4 Stereo Configuration



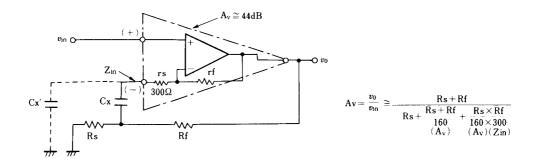
■ VOLTAGE GAIN REDUCTION APPLICATION EXAMPLE

(1) Outline of way to further Reduction

NJM2073 by taking in assamption, as one of OP-AMP (Gain 44dB, minus input impedance about 300Ω), to feedback from output to minus input helps to get reduction of stabilized Voltage Gain. Fig. 5 indicates the model example.

Here is the point to be noticed that, in order to get the appropriate output Bias Voltage, it is important to keep the minus input floating as DC condition, (inserting Cx), and also that when extended too much reduction of Gain might cause Oscillation due to high band phase margin. The reduction of voltage gain is limited at around 26dB (20 times), and when oscillation, it in necessary to attach the oscillation stopper. Please examine the C_X value accordingly to the application requirement.

Fig.5 Model of Voltage Gain Reduction



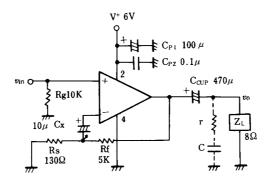
(2) The Application Example of Voltage Gain Reduction. (STEREO)

Fig.6 indicates the application example and Table1 indicates the recommendable value of parts to be attached externally.

Table1, Applicating purpose and Recommended Value of Externally parts to be attached.

EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENDED VALUE	REMARKS
R_g	Plus input to be grounded by fixed DC	Under about 100kΩ	Catch the noise when much higher.
R _s	AV shall be decided with R _f	-	
R_{f}	AV shall be decided with R _s	About 5kΩ	The co-temperature of AV becomes higher in case when $R_{\rm S}$ is higher resistance. The current from output pin to GND becomes higher, in case when $R_{\rm S}$ is lower resistance. (The current sinks in vain.)
C _X	Minus input to be grounded by fixed DC	-	Low-band Cut off frequency (fL) is to be decided. The rise time becomes longer in case that C _X is big.
C _{CUP}	Output DC Decoupling	When $R_L=8\Omega$, More than $220\mu F$	fL shall be decided by C_{CUP} and Z_{L} .
C _{P1}	Stabilization of V ⁺	More than about C _{CUP}	Inserting near around V ⁺ pin and GND pin.
C _{P2}	Prevention of Oscillation	More than 0.1µF	
r	Prevention of Oscillation	About R _L	Inserting near around V ⁺ pin and GND pin.
С	Prevention of Oscillation	0.22µF	To be examined by about the resistor volume of the speaker load.

Fig.6 STEREO Application Example.



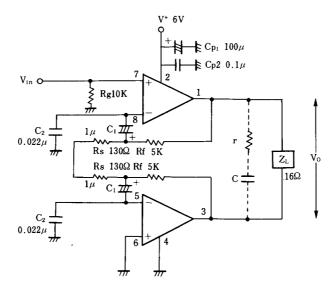
• Application for Voltage Gain Reduction (BTL)

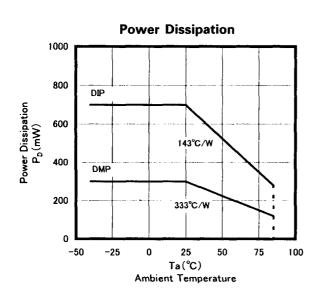
Fig.7 indicates the application example, Table2 shows recommended value of externally attaching parts.

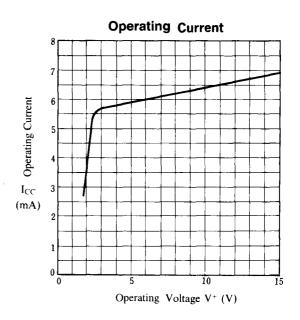
Table2 Applicating purpose and Recommended Value of External Part

EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENDED VALUE	REMARKS
R_{g}	DC condition ground of plus input	Below about 10kΩ	Making noise when higher.
Rs	AV shall be decided with R _f	•	
Rf	AV shall be decided with R _s	About 5kΩ	Temperature feature to be increased accordingly as in higher AV value. When lower,to be trended of Oscillation.
C ₁	Releasing minus input in to DC condition	-	Setting up low band Cut-off frequency (fL). More higher,the rise time become longer.
C ₂	Preventing Oscillation	About 0.02μF	The more higher in value, the high band THD, due to phase slipping to be deteriorated. When lower, to be trended of oscillation.
C _{P1}	Stability of V ⁺ Preventing Oscillation	More than about 100µF	Inserting near around at V^{\dagger} and the GND pin.
C_{P2}	Preventing Oscillation	More than 0.1µF	Inserting near around at V^{\dagger} and the GND pin.
r	Preventing Oscillation	About R _L	To be examined at around pure resister Value of speaker load.
С	Preventing Oscillation	0.22µF	

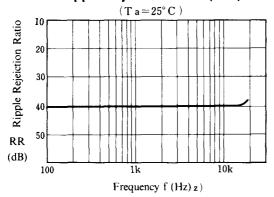
Fig.7 BTL Application

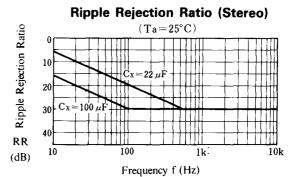




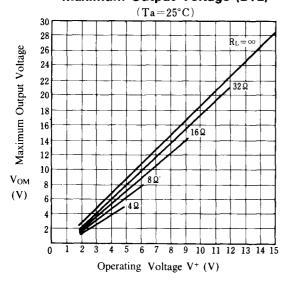


Ripple Rejection Ratio (BTL)

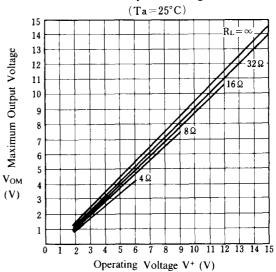




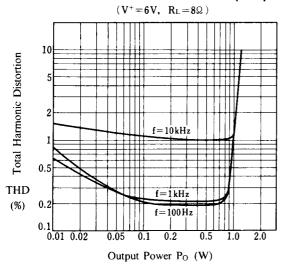
Maximum Output Voltage (BTL)



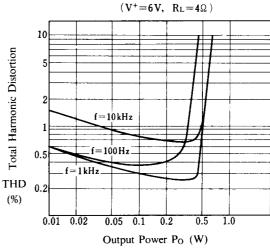
Maximum Output Voltage (Stereo)



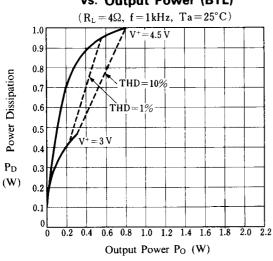
Total Harmonic Distortion (BTL)



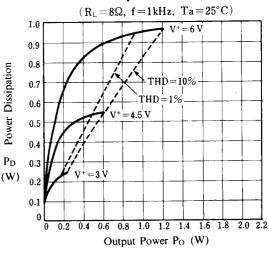
Total Harmonic Distortion (Stereo)



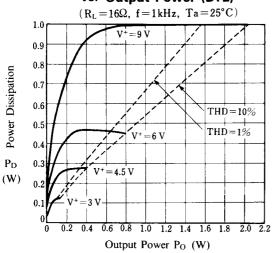
Power Dissipation vs. Output Power (BTL)



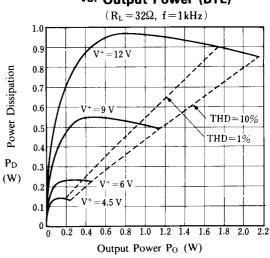
Power Dissipation vs. Output Power (BTL)



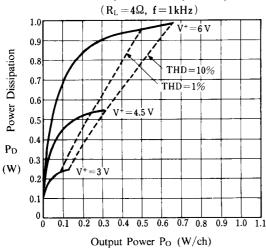
Power Dissipation vs. Output Power (BTL)



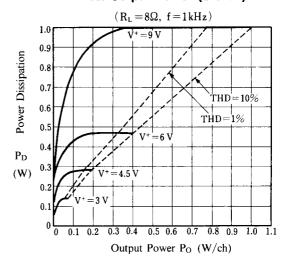
Power Dissipation vs. Output Power (BTL)



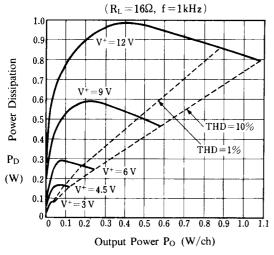
Power Dissipation vs. Output Power (Stereo)



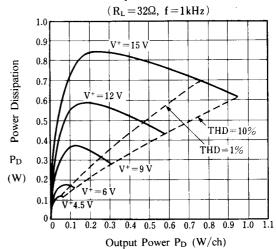
Power Dissipation vs. Output Power (Stereo)



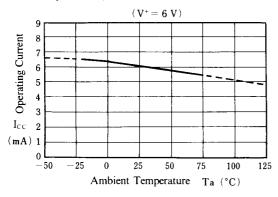
Power Dissipation vs. Output Power (Stereo)



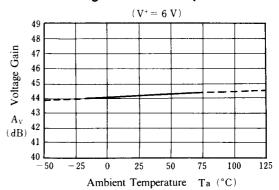
Power Dissipation vs. Output Power (Stereo)



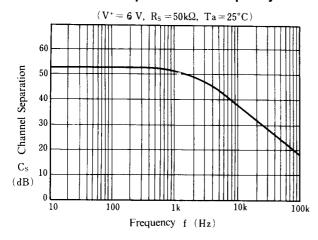
Operating Current vs. Temperature



Voltage Gain vs. Temperature



Channel Separation vs. Frequency



[CAUTION]

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