

## LOW-NOISE DUAL OPERATIONAL AMPLIFIER

### ■ GENERAL DESCRIPTION

The NJM5532C is a high performance dual low noise operational amplifier. This features low noise performance ( $5\text{nV}/\sqrt{\text{Hz}}$ ), and considerably higher Gain Band Width (10MHz), low distortion (0.0003%). This makes the device especially suitable for application in high quality and professional audio.

### ■ PACKAGE OUTLINE

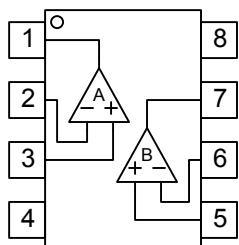


NJM5532CG  
(SOP8)

### ■ FEATURES

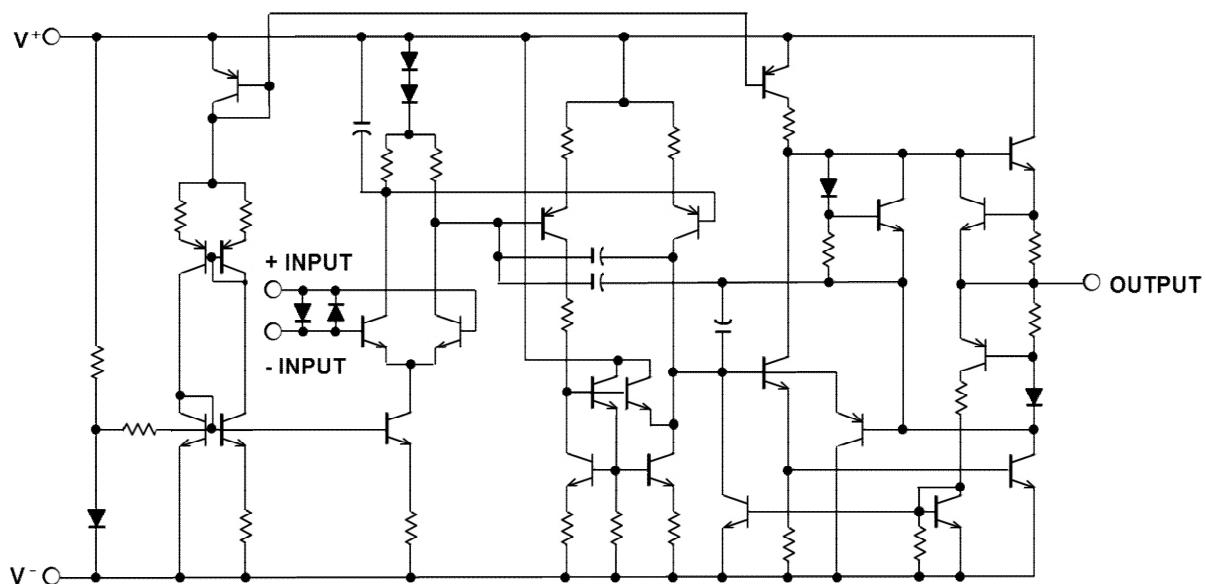
|                                  |  |
|----------------------------------|--|
| • Equivalent Input Noise Voltage | : $5\text{nV}/\sqrt{\text{Hz}}$ typ. at 1kHz |
| • Gain bandwidth product         | : 10MHz typ.                                 |
| • Common-Mode Rejection Ratio    | : 100dB typ.                                 |
| • High DC Voltage Gain           | : 94dB typ.                                  |
| • High Slew Rate                 | : 9V/us typ.                                 |
| • Wide power supply range        | : $\pm 3\text{V}$ to $\pm 22\text{V}$        |
| • Internal ESD protection        |  |
| Human body model (HBM)           | : $\pm 2000\text{V}$ typ.                    |

### ■ PIN CONFIGURATION



| PIN FUNCTION      |
|-------------------|
| 1. A OUTPUT       |
| 2. A -INPUT       |
| 3. A +INPUT       |
| 4. V              |
| 5. B +INPUT       |
| 6. B -INPUT       |
| 7. B OUTPUT       |
| 8. V <sup>+</sup> |

### ■ EQUIVALENT CIRCUIT (Each Amplifier)



# NJM5532C

## ■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

| PARAMETER                                    | SYMBOL                         | RATINGS                                   | UNIT |
|--|--------------------------------|---|------|
| Supply voltage                               | V <sup>+</sup> /V <sup>-</sup> | ±22                                       | V    |
| Input voltage <sup>(1)</sup>                 | V <sub>IN</sub>                | V-0.3 to V+44                             | V    |
| Output terminal input voltage                | V <sub>O</sub>                 | V-0.3 to V <sup>+</sup> +0.3              | V    |
| Differential input voltage <sup>(2)</sup>    | V <sub>ID</sub>                | ±0.5                                      | V    |
| Input current <sup>(3)</sup>                 | I <sub>IN</sub>                | ±10                                       | mA   |
| Output short-circuit duration <sup>(4)</sup> |                                | Infinite                                  | -    |
| Power Dissipation                            | P <sub>D</sub>                 | 690 <sup>(5)</sup><br>1000 <sup>(6)</sup> | mW   |
| Operating free-air temperature range         | T <sub>opr</sub>               | -40 to 85                                 | °C   |
| Storage temperature range                    | T <sub>sg</sub>                | -65 to +150                               | °C   |

(1) Input voltage is the voltage should be allowed to apply to the input terminal independent of the magnitude of V<sup>+</sup>.

The normal operation will establish when any input is within the Common Mode Input Voltage Range of electrical characteristics.

(2) Differential voltage is the voltage difference between +INPUT and -INPUT.

(3) Excessive input current will flow if a differential input voltage in excess of approximately 0.5 V is applied between the inputs, unless some limiting resistance is used.

(4) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

(5) EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 2layers, FR-4) mounting

(6) EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 4layers, FR-4) mounting

## ■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER      | SYMBOL                         | CONDITION            | MIN. | TYP. | MAX. | UNIT |
|----------------|--------------------------------|----------------------|------|------|------|------|
| Supply Voltage | V <sup>+</sup> /V <sup>-</sup> | T <sub>a</sub> =25°C | ±3   | -    | ±22  | V    |

## ■ ELECTRICAL CHARACTERISTICS

V<sup>+</sup>/V<sup>-</sup>=±15V, T<sub>a</sub>=25°C (unless otherwise noted)

| PARAMETER                                   | SYMBOL           | CONDITION   | MIN.       | TYP.     | MAX.        | UNIT |
|---|------------------|---|------------|----------|-------------|------|
| Input Offset Voltage                        | V <sub>IO</sub>  | R <sub>S</sub> =50Ω<br>T <sub>a</sub> =25°C<br>0°C<T <sub>a</sub> <70°C <sup>(7)</sup>                        | -<br>-     | 0.5<br>- | 4<br>5      | mV   |
| Input Offset Current                        | I <sub>IO</sub>  | T <sub>a</sub> =25°C<br>0°C<T <sub>a</sub> <70°C <sup>(7)</sup>   | -          | 10       | 150<br>200  | nA   |
| Input Bias Current                          | I <sub>B</sub>   | T <sub>a</sub> =25°C<br>0°C<T <sub>a</sub> <70°C <sup>(7)</sup>   | -<br>-     | 200      | 800<br>1000 | nA   |
| Open Loop Gain 1                            | A <sub>v1</sub>  | R <sub>L</sub> ≥600Ω, V <sub>O</sub> =±10V<br>T <sub>a</sub> =25°C<br>0°C<T <sub>a</sub> <70°C <sup>(7)</sup> | 83.5<br>80 | 94<br>-  | -<br>-      | dB   |
| Open Loop Gain 2                            | A <sub>v2</sub>  | R <sub>L</sub> ≥2kΩ, V <sub>O</sub> =±10V<br>T <sub>a</sub> =25°C<br>0°C<T <sub>a</sub> <70°C <sup>(7)</sup>  | 88<br>83.5 | 100<br>- | -<br>-      | dB   |
| Supply Voltage Rejection Ratio              | SVR              | R <sub>S</sub> ≤10kΩ, V <sup>+</sup> /V <sup>-</sup> =±9V to ±15V   | 80         | 100      | -           | dB   |
| Supply Current, all amp                     | I <sub>CC</sub>  | no load   | -          | 8        | 16          | mA   |
| Common mode Input Voltage Range             | V <sub>ICM</sub> |   | ±12        | ±13      | -           | V    |
| Common Mode Rejection Ratio                 | CMR              | R <sub>S</sub> ≤10kΩ  | 70         | 100      | -           | dB   |
| Short-circuit Output Current <sup>(8)</sup> | I <sub>SC</sub>  |   | 20         | 50       | 75          | mA   |

| PARAMETER                       | SYMBOL   | CONDITION   | MIN.                 | TYP.                 | MAX. | UNIT                       |
|---------------------------------|----------|---|----------------------|----------------------|------|----------------------------|
| Maximum Output Voltage          | $V_{OM}$ | $R_L \geq 600\Omega$<br>$R_L \geq 600\Omega, V^+/V^- = \pm 18V$                         | $\pm 12$<br>$\pm 15$ | $\pm 13$<br>$\pm 16$ | -    | V                          |
| Input Resistance                | $R_{IN}$ |   | 30                   | 150                  | -    | k $\Omega$                 |
| Output Resistance               | $R_o$    |   | -                    | 0.3                  | -    | $\Omega$                   |
| Small-signal Voltage Gain       | $A_v$    | $f=10\text{kHz}$  | -                    | 67                   | -    | dB                         |
| Gain Band Width Product         | GBP      | $R_L = 600\Omega, C_L = 100\text{pF}$   | -                    | 10                   | -    | MHz                        |
| Powerband Width                 | $W_{PG}$ | $R_L = 600\Omega, V_o = \pm 10V$<br>$R_L = 600\Omega, V_o = \pm 14V, V^+/V^- = \pm 18V$ | -                    | 140<br>100           | -    | kHz                        |
| Equivalent Input Noise Voltage1 | $e_n$    | $f=30\text{Hz}$<br>$f=1\text{kHz}$  | -                    | 8<br>5               | -    | nV/ $\sqrt{\text{Hz}}$     |
| Equivalent Input noise Current  | $I_n$    | $f=30\text{Hz}$<br>$f=1\text{kHz}$  | -                    | 2.7<br>0.7           | -    | pA/ $\sqrt{\text{Hz}}$     |
| Equivalent Input Noise Voltage2 | $V_{NI}$ | $f=20$ to $20\text{kHz}$  | -                    | 0.6                  | 0.8  | $\mu\text{V}_{\text{rms}}$ |
| Slew Rate                       | SR       |   | -                    | 9                    | -    | V/ $\mu\text{s}$           |
| Overshoot factor                | $K_{OV}$ | $G_V=1, V_{IN}=100\text{mV}_{\text{PP}}, C_L=100\text{pF}, R_L=600\Omega$               | -                    | 10                   | -    | %                          |
| Channel Separation              | CS       | $f=1\text{kHz}$   | -                    | 110                  | -    | dB                         |

(7) This parameter is not 100% test.

(8) Temperature and /or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

## ■ APPLICATION INFORMATION

### • Back-to-back Diode Protection

The input terminals of the NJM5532C are protected from excessive differential voltage by back-to-back diodes.

However, When used in voltage follower circuit, the back-to-back diode may break at power on.

Therefore, put a current-limiting resistance to input terminal as shown Fig.1.

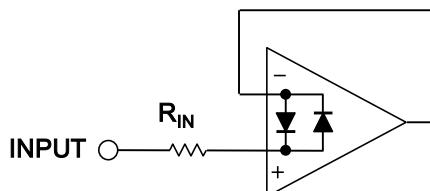


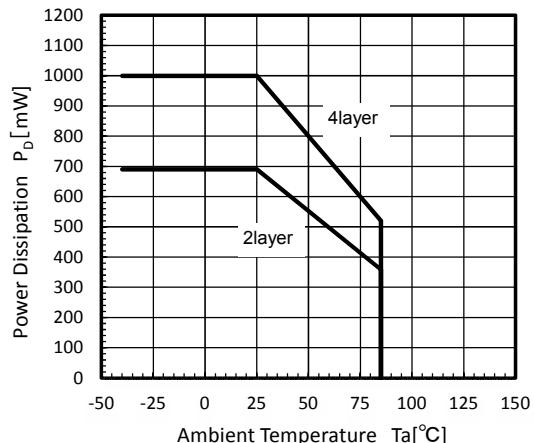
Fig.1

### • Caution to Thermal Design

If the NJM5532C junction temperature ( $T_j$ ) exceeds guaranteed value (150 degree) and the package power dissipation ( $P_D$ ), there is possibility of the NJM5532C deterioration or breakdown.

The NJM5532C supply current is higher ( $I_{CCMAX}=16\text{mA}$  at  $V^+/V^- = \pm 15V, Ta=+25^\circ\text{C}$ ) and has positive temperature coefficient (Refer to Supply Current vs. Temperature characteristic).

Therefore, you should carefully design with due attention to the supply voltage, the internal power dissipation and the ambient temperature.



# NJM5532C

## •Countermeasure to Excess Current by Parasitic Circuit

When the NJM5532C V+ is open (Fig.2), the NJM5532C may be burnt flowing the excess current by internal parasitic circuit(Fig.3).The excess current generating condition is following:

- / Between input terminal and V- voltage difference is higher.
- / Between input terminal and GND impedance is small.
- / V+ terminal is connected with low impedance. (letc is higher)

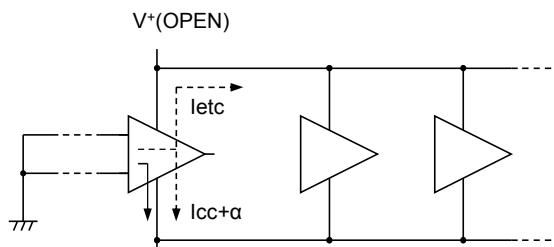


Fig.2

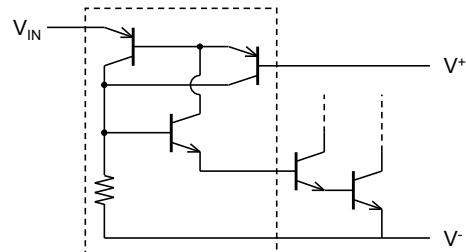


Fig.3

For countermeasure to excess current by parasitic circuit, NJRC recommends the following method.

- / prevent operating of a parasitic circuit by inserting a diode (Fig.4-1/4-2).
- / limiting a parasitic circuit operation by inserting a resistance (1kΩ or more) (Fig.5).

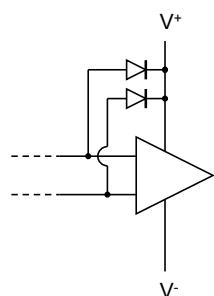


Fig.4-1

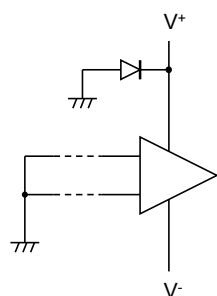


Fig.4-2

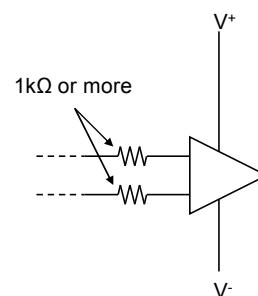
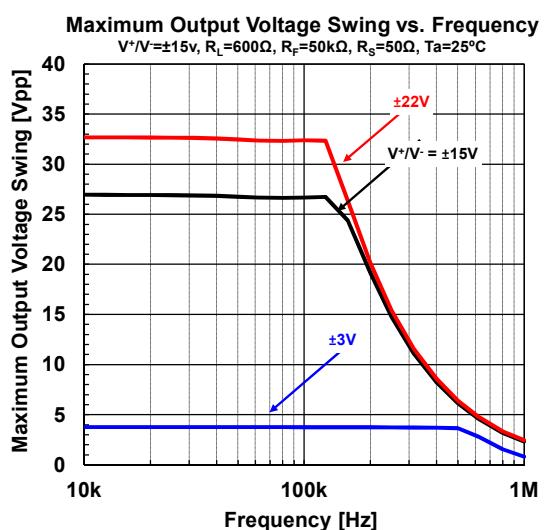
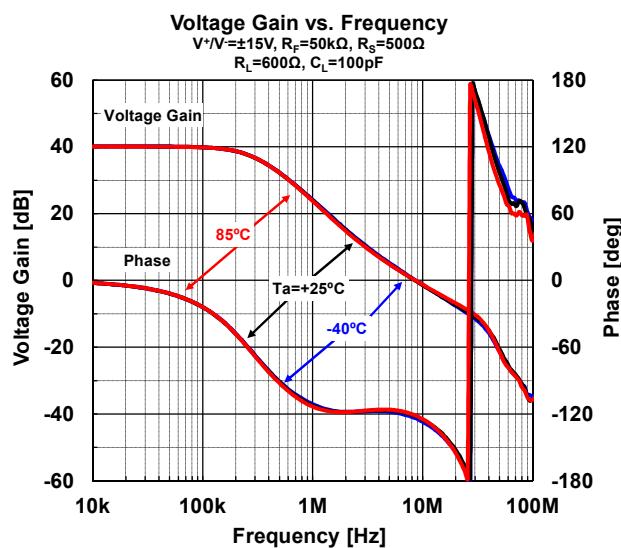
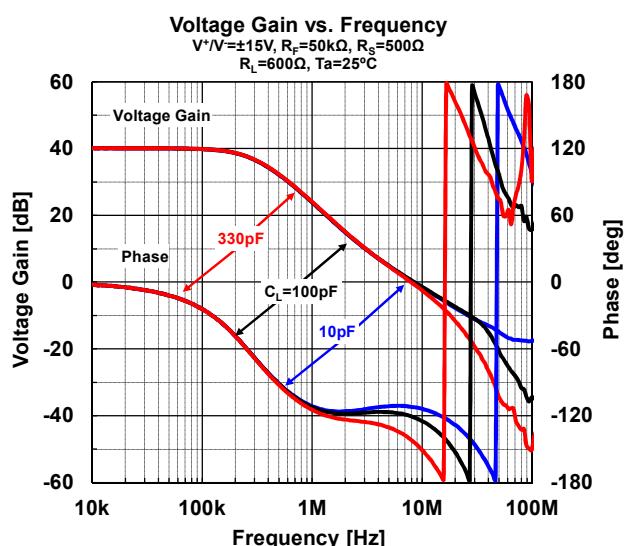
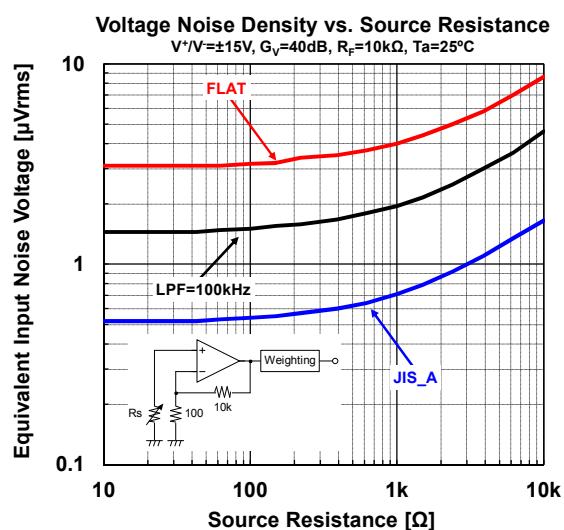
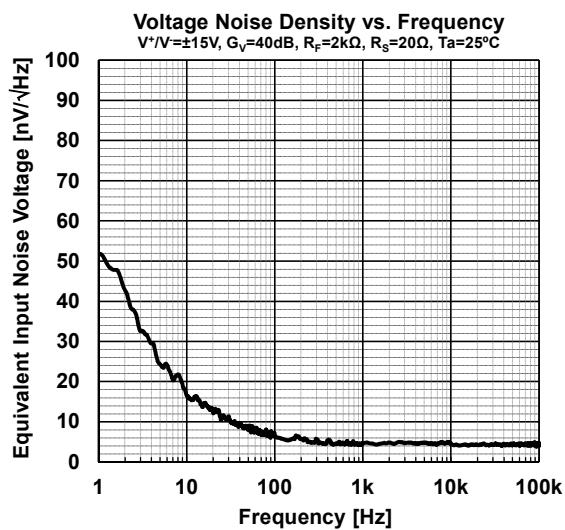
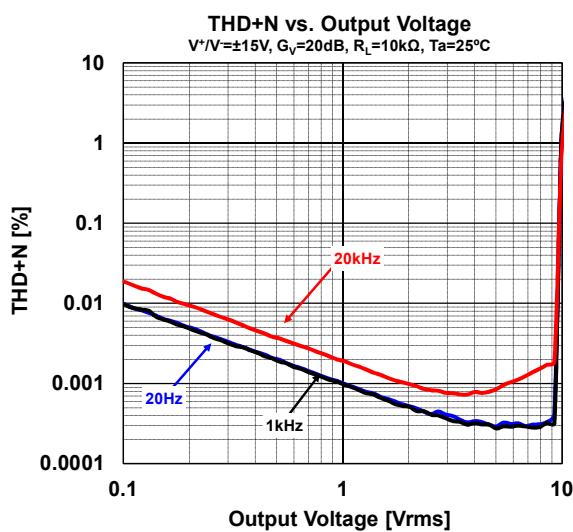


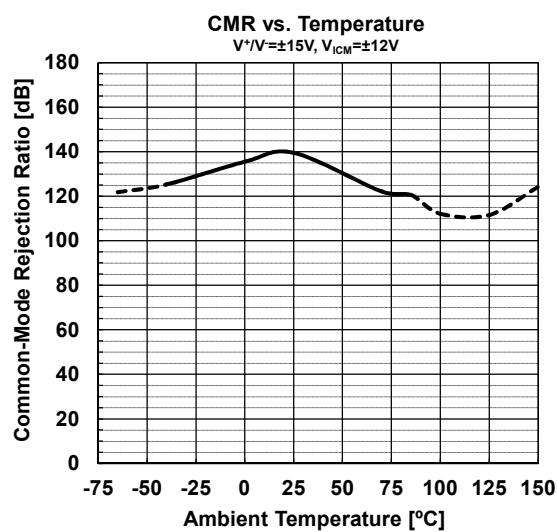
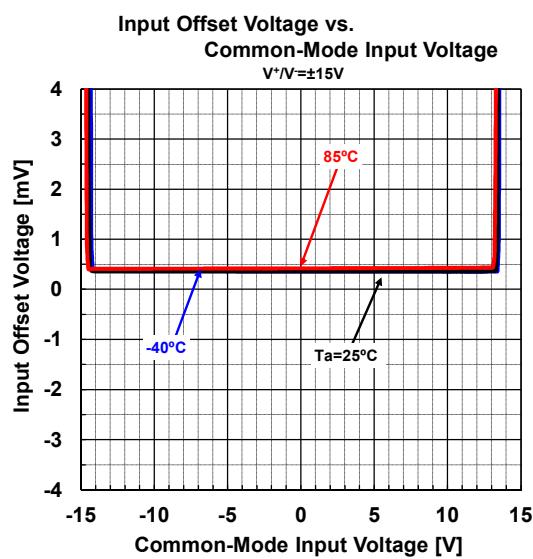
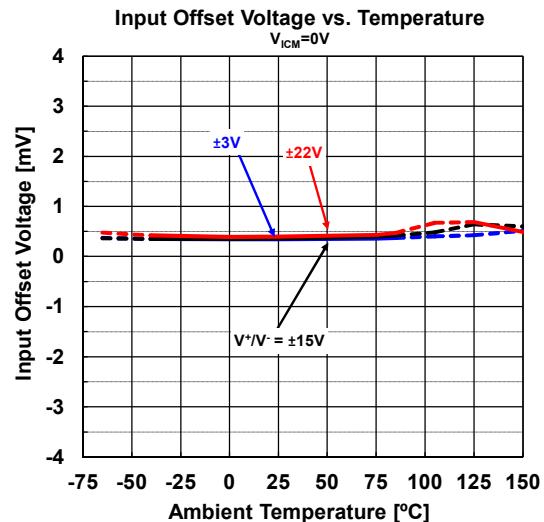
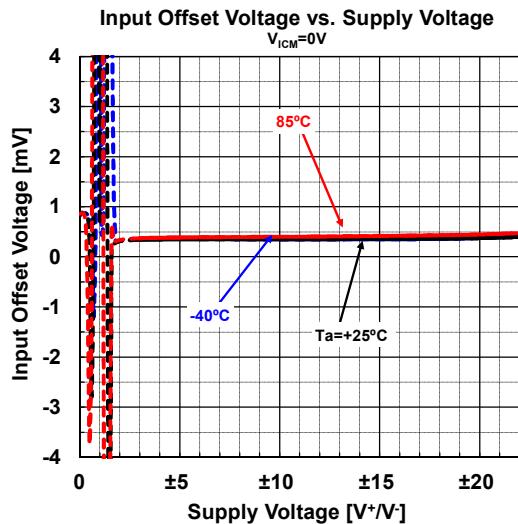
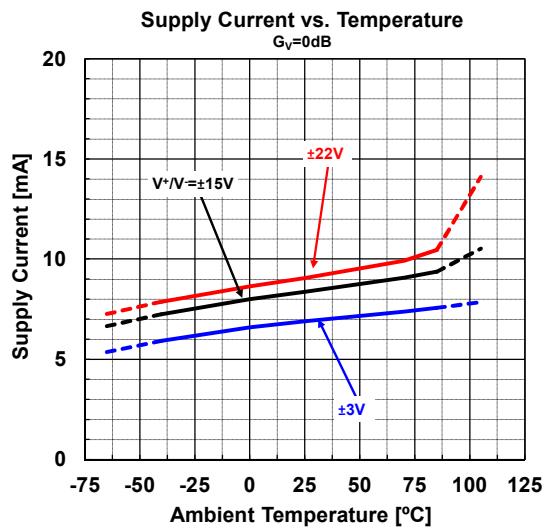
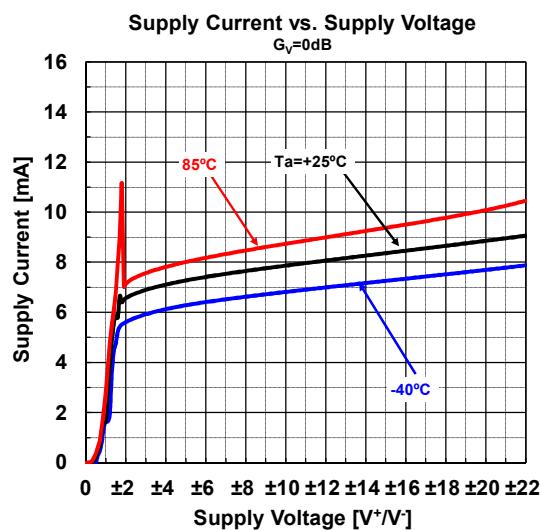
Fig.5

## ■ TYPICAL CHARACTERISTICS

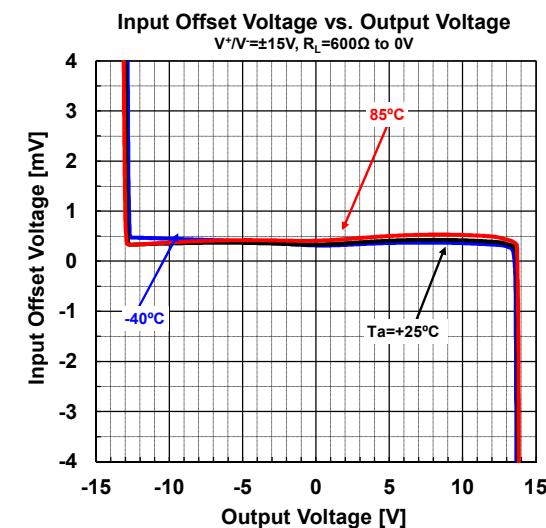
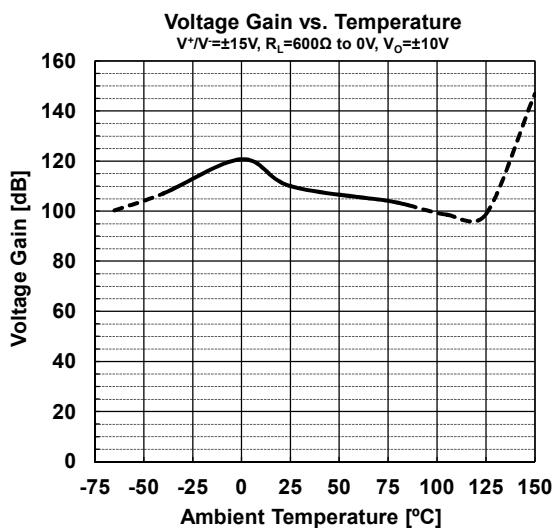
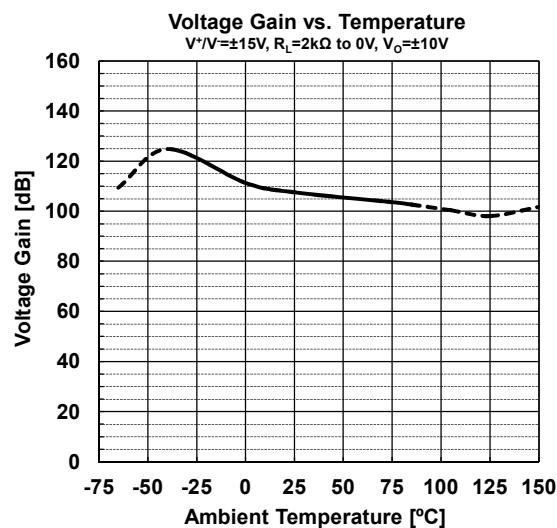
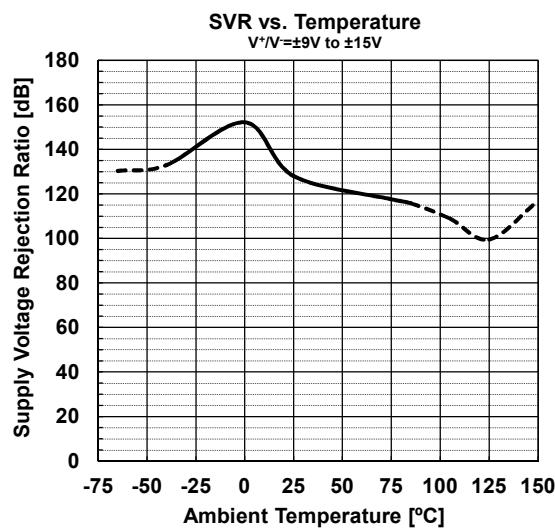
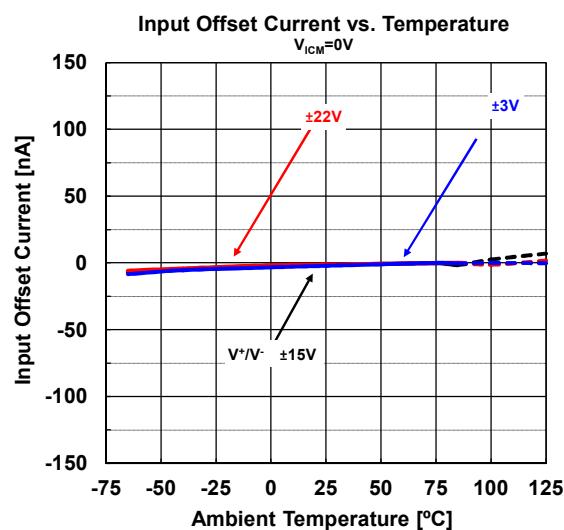
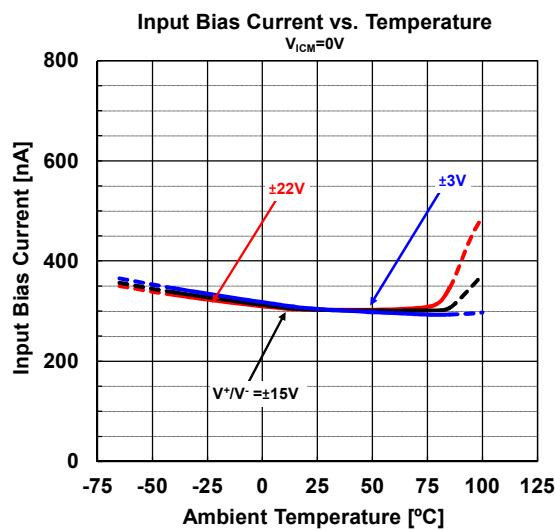


# NJM5532C

## ■ TYPICAL CHARACTERISTICS

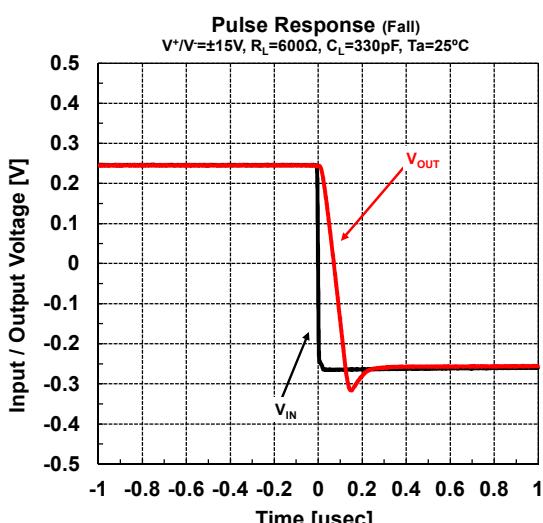
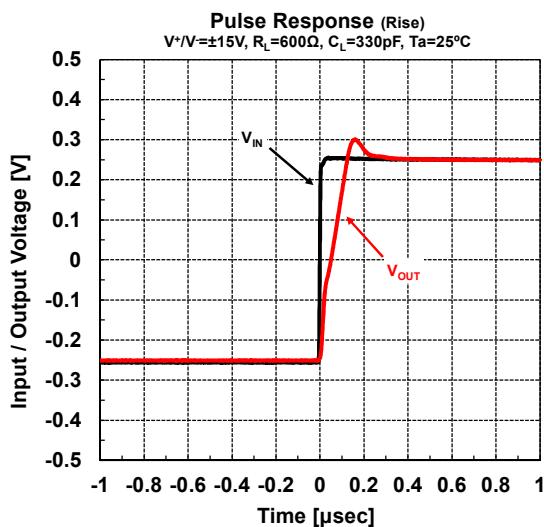
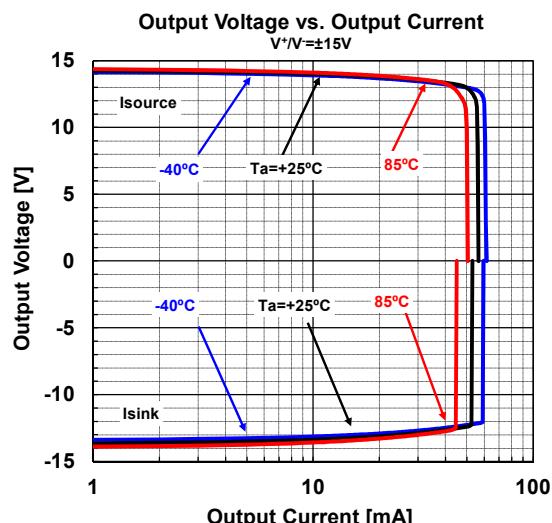
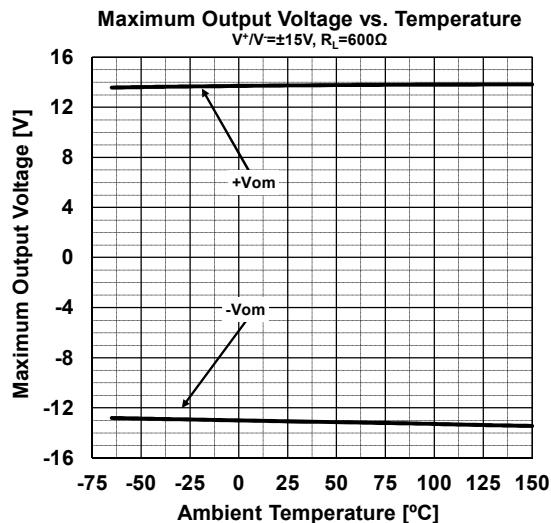
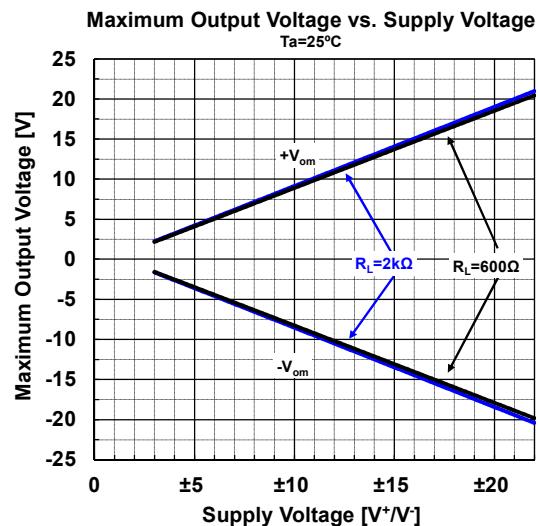
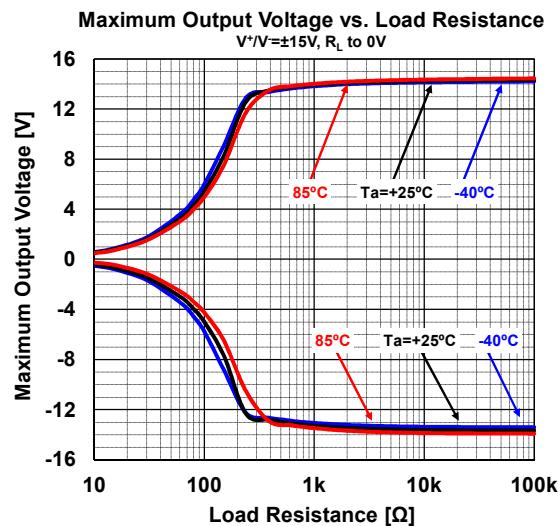


## ■ TYPICAL CHARACTERISTICS

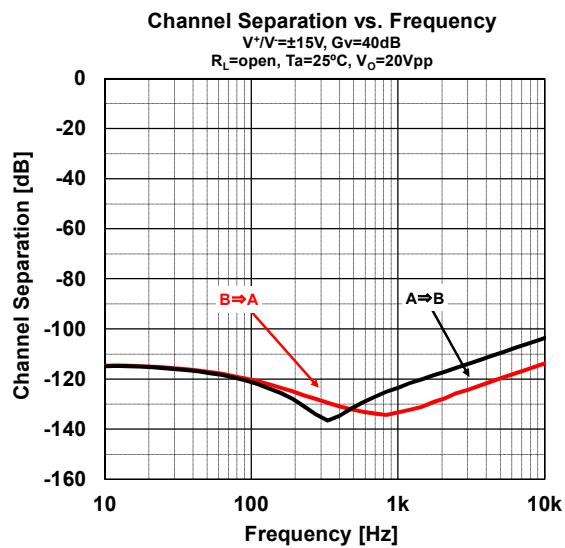
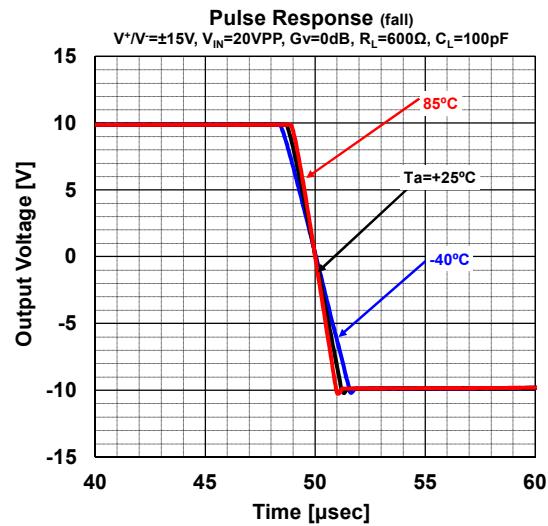
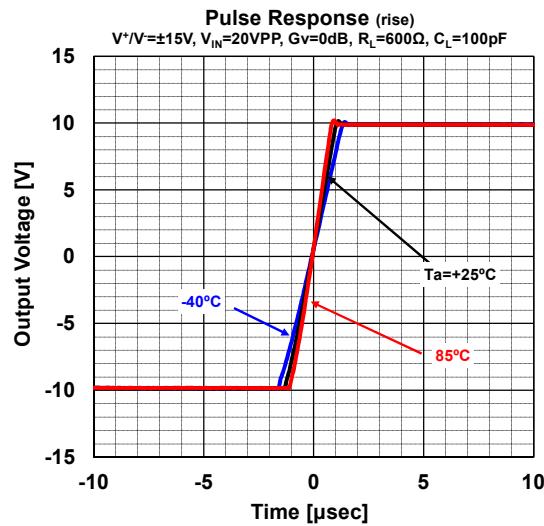


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## ■ TYPICAL CHARACTERISTICS



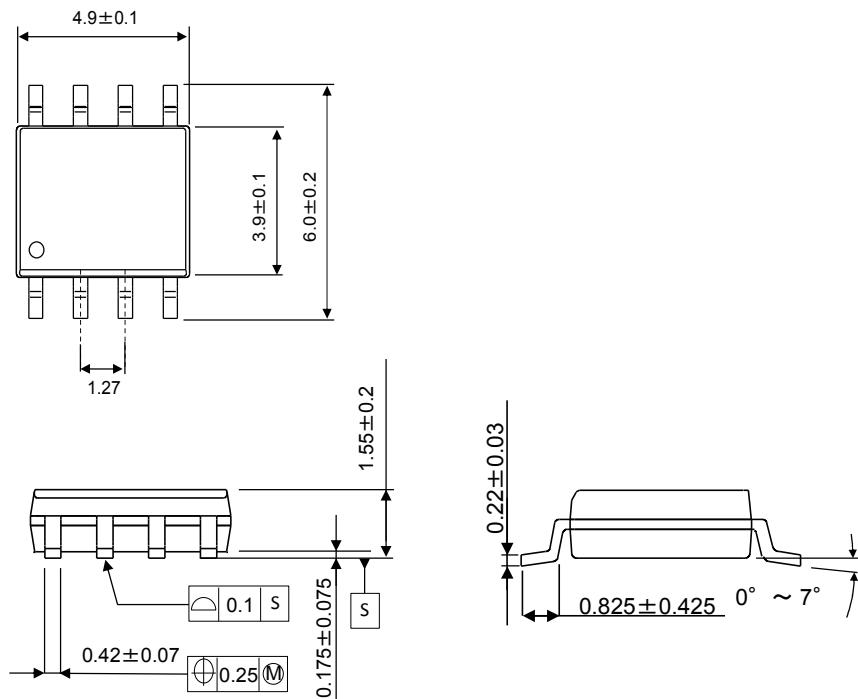
## ■ TYPICAL CHARACTERISTICS



# NJM5532C

## ■PACKAGE OUTLINE UNIT : mm

SOP8



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