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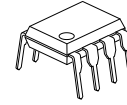
LOW OFFSET VOLTAGE, LOW DRIFT OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

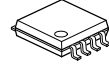
The NJM OP-07 is ultra-low input offset voltage and bias current, low drift and high gain operational amplifier with internal frequency compensation.

The NJM OP-07 is suitable for a precision instrumental amplifier.

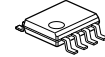
■ PACKAGE OUTLINE



NJMOP-07D



NJMOP-07M

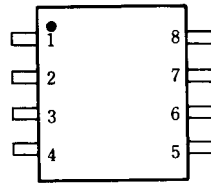


NJMOP-07E

■ FEATURES

- Low V_{IO} (60 μ V typ.)
- Low I_B (1.8nA typ.)
- Low Drift (unnull 0.5 μ V/ $^{\circ}$ C typ.)
(null 0.4 μ V/ $^{\circ}$ C typ.)
(0.4 μ V/ M_o typ.)
- Wide Operating Voltage (\pm 3V \sim \pm 22V)
- Package Outline DIP8, DMP8, SOP8 JEDEC 150mil
- Bipolar Technology

■ PIN CONFIGURATION



NJMOP-07D

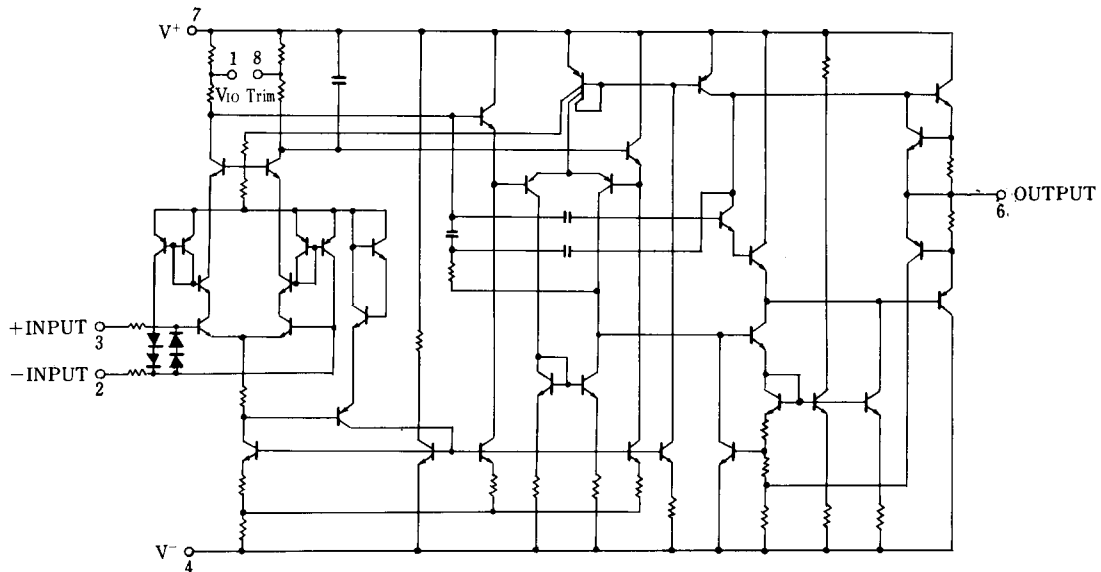
NJMOP-07M

NJMOP-07E

PIN FUNCTION

1. V_{IO} Trim
2. -INPUT
3. +INPUT
4. V^-
5. NC
6. OUTPUT
7. V^+
8. V_{IO} Trim

■ EQUIVALENT CIRCUIT



NJMOP-07

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+ / V^-	± 22	V
Input Voltage	V_1	± 22 (note1)	V
Differential Input Voltage	V_{ID}	± 30	V
Power Dissipation	P_D	(DIP8) 500(note2) (DMP8) 300(note2) / 430(note3) (SOP8) 300 (note2) / 640(note3)	mW
Storage Temperature Range	T_{stg}	-40~+125	°C
Operating Temperature Range	T_{opr}	-40~+85	°C
Output Current		continuous	

(note1) For supply voltage less than $\pm 22V$, the absolute maximum input voltage is equal to the supply voltage.

(note2) Device itself.

(note3) Mounted on the EIA/JEDEC standard board (76.2×114.3×1.6mm, two layer, FR-4).

■ ELECTRICAL CHARACTERISTICS

(Ta=+25°C, $V^+ / V^- = \pm 15V$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}		-	60	150	μV
Long Term Stability		(note4,5)	-	0.4	2	$\mu V / M_0$
Input Offset Current	I_{IO}		-	0.8	6	nA
Input Bias Current	I_B		-	± 1.8	± 7	nA
Open Loop Output Resistance	R_O	$V_O=0, I_O=0$	-	60	-	Ω
Input Resistance	R_{ID}	(Differential Mode)	8	33	-	M Ω
Input Resistance	R_{IC}	(Common Mode)	-	120	-	G Ω
Input Common Mode Voltage Range	V_{ICM}		± 13	± 14	-	V
Common Mode Rejection Ratio	CMR	$V_{CM} = \pm 13V$	100	120	-	dB
Supply Voltage Rejection Ratio	SVR	$V^+ / V^- = \pm 3V \sim \pm 18V$	90	104	-	dB
Large Signal Voltage Gain 1	AV_1	$R_L \geq 2k\Omega, V_O = \pm 10V$	101.5	112.0	-	dB
Large Signal Voltage Gain 2	AV_2	$R_L = 500\Omega, V_O = \pm 0.5V, V^+ / V^- = \pm 3V$	100.0	112.0	-	dB
Maximum Output Voltage 1	V_{OM1}	$R_L \geq 10k\Omega$	± 12	± 13	-	V
Maximum Output Voltage 2	V_{OM2}	$R_L > 2k\Omega$	± 11.5	± 12.8	-	V
Maximum Output Voltage 3	V_{OM3}	$R_L > 1k\Omega$	-	± 12	-	V
Slew Rate	SR	$R_L \geq 2k\Omega$	-	0.17	-	V/ μS
Unity Gain Bandwidth	f_T	$A_{VCL} = 1$	-	0.5	-	MHz
Operating Current 1	I_{CC1}	$V^+ / V^- = \pm 15V$	-	2.7	5.0	mA
Operating Current 2	I_{CC2}	$V^+ / V^- = \pm 3V$	-	0.67	1.3	mA
Offset Adjustment Range		$R_P = 20k\Omega$	-	± 4	-	mV
Equivalent Input Noise Voltage	V_{NI}	0.1Hz~10Hz (note5)	-	0.38	0.65	μV_{P-P}
Equivalent Input Noise Voltage 1	e_{n1}	$f_0 = 10Hz$ (note5)	-	10.5	20	nV/ \sqrt{Hz}
Equivalent Input Noise Voltage 2	e_{n2}	$f_0 = 100Hz$ (note5)	-	10.2	13.5	nV/ \sqrt{Hz}
Equivalent Input Noise Voltage 3	e_{n3}	$f_0 = 1kHz$ (note5)	-	9.8	11.5	nV/ \sqrt{Hz}
Equivalent Input Noise Current	I_{NI}	0.1Hz~10Hz (note5)	-	15	35	pA \sqrt{Hz}
Equivalent Input Noise Current 1	i_{n1}	$f_0 = 10Hz$ (note5)	-	0.35	0.9	pA/ \sqrt{Hz}
Equivalent Input Noise Current 2	i_{n2}	$f_0 = 100Hz$ (note5)	-	0.15	0.27	pA/ \sqrt{Hz}
Equivalent Input Noise Current 3	i_{n3}	$f_0 = 1kHz$ (note5)	-	0.13	0.18	pA/ \sqrt{Hz}

■ ELECTRICAL CHARACTERISTICS

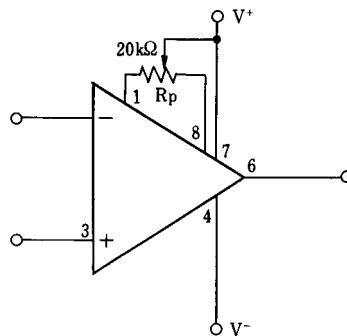
($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}, V^+ / V^- = \pm 15\text{V}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}		-	85	250	μV
Average V_{IO} Drift (unnull)		(note5)	-	0.5	1.8	$\mu\text{V}/^{\circ}\text{C}$
Average V_{IO} Drift (null)		$R_p = 20\text{k}\Omega$, (note5)	-	0.4	1.6	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current	I_{IO}		-	1.6	8	nA
Average I_{IO} Drift		(note5)	-	12	50	$\text{pA}/^{\circ}\text{C}$
Input Bias Current	I_{IB}		-	± 2.2	± 9	nA
Average I_{IB} Drift		(note5)	-	18	50	$\text{pA}/^{\circ}\text{C}$
Input Common Mode Voltage Range	V_{ICM}		± 13	± 13.5	-	V
Common Mode Rejection Ratio	CMR	$V_{CM} = \pm 13\text{V}$	97	120	-	dB
Supply Voltage Rejection Ratio	SVR	$V^+ / V^- = \pm 3\text{V} \sim \pm 18\text{V}$	86	120	-	dB
Voltage Gain	A_V	$R_L \geq 2\text{k}\Omega, V_O = \pm 10\text{V}$	100	400	-	V/mV
Maximum Output Voltage	V_{OM}	$R_L \geq 2\text{k}\Omega$	± 11	± 12.6	-	V

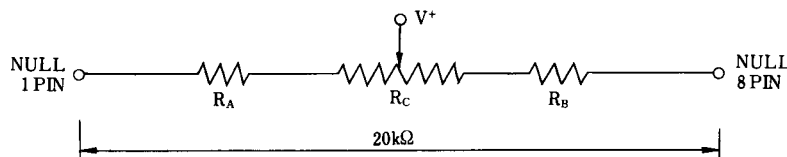
(note 4) Long Term Stability refers to the average trend line of V_{IO} vs. time over extended periods after the first 30 days of operation.

(note 5) According to the evaluation by NJRC, more than 90% of all these products can be guaranteed.

■ OFFSET ADJUSTMENT METHOD



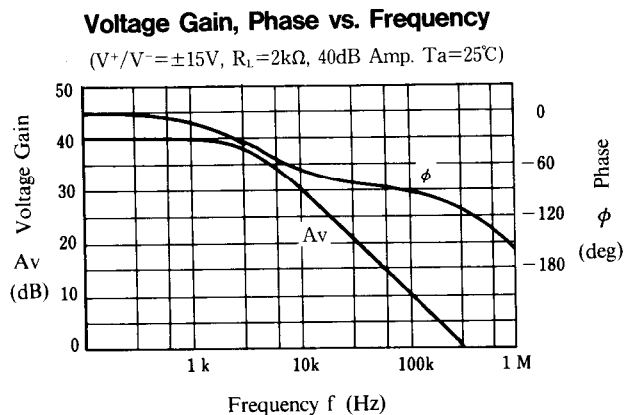
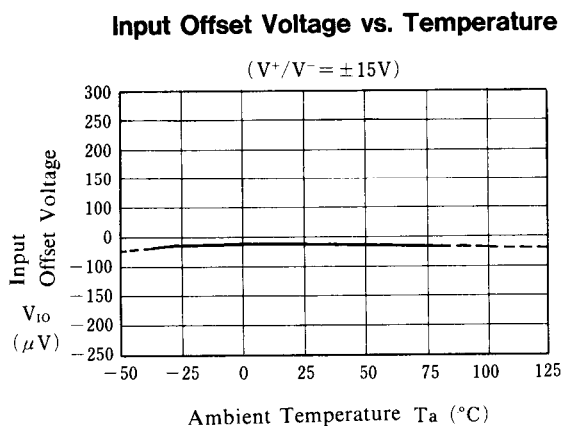
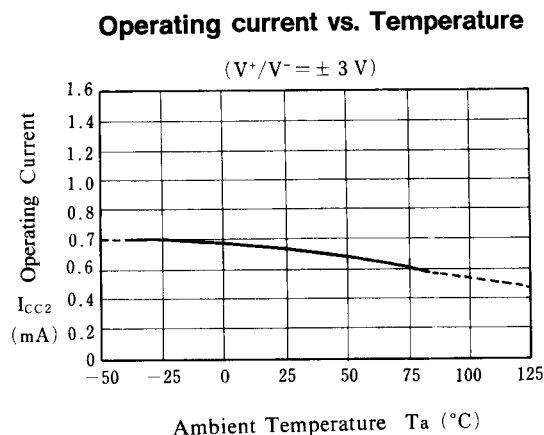
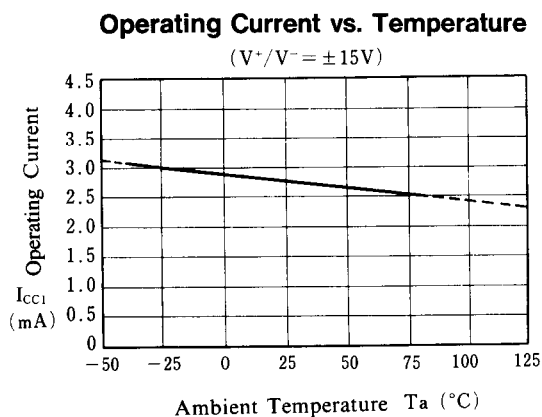
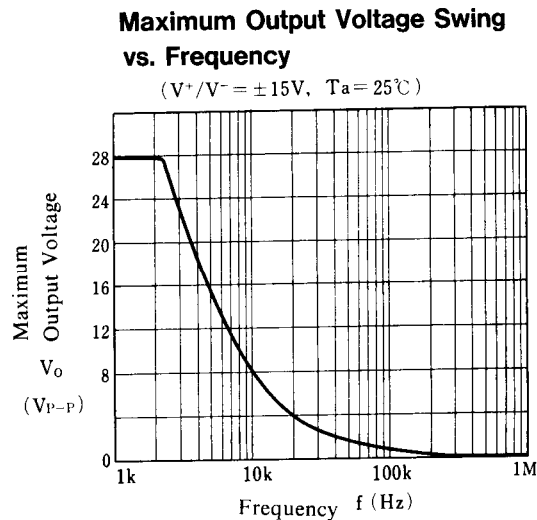
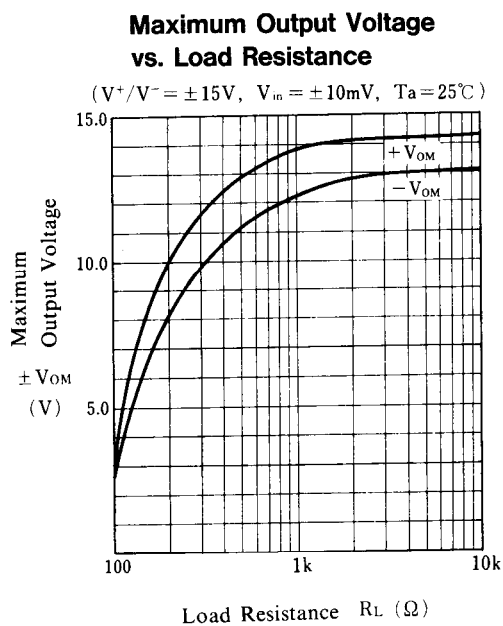
For making low sensitivity of change in the input offset voltage against resistance regulation of potentiometer
(Easy case of offset adjustment)



* R_A, R_B Fixed $7.5\text{k}\Omega$, R_C adjustable $5.0\text{k}\Omega$

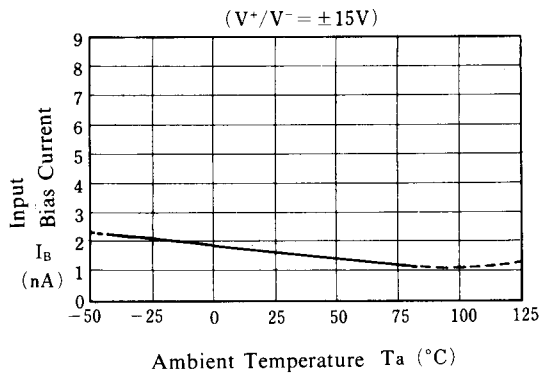
* R_A, R_B, R_C are metalfilm resistors, R_C is more than 10 times winding.

■ TYPICAL CHARACTERISTICS

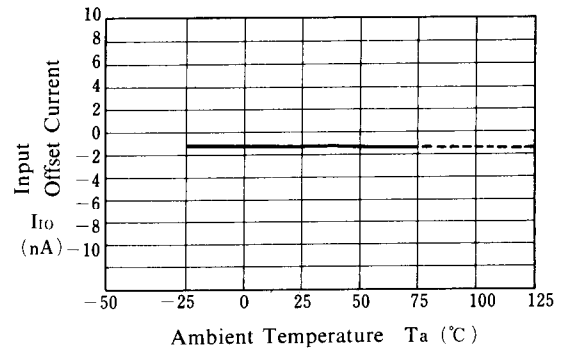


■ TYPICAL CHARACTERISTICS

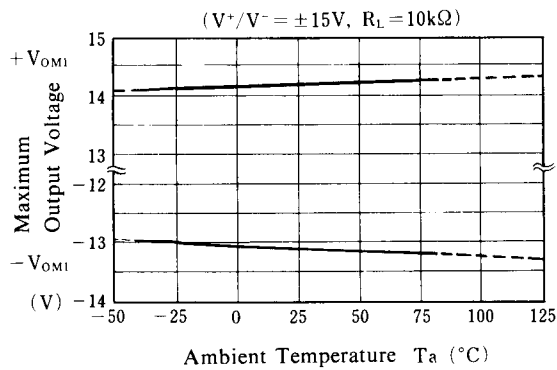
Input Bias Current vs. Temperature



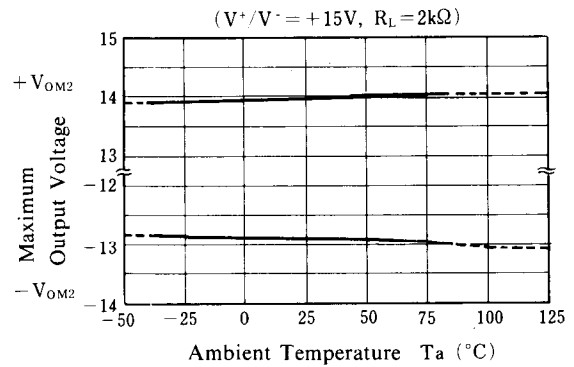
Input Offset Current vs. Temperature



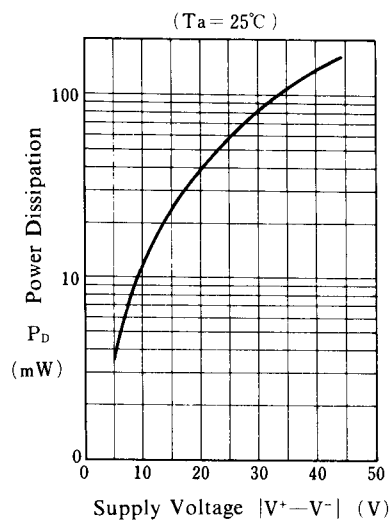
Maximum Output Voltage vs. Temperature



Maximum Output Voltage vs. Temperature



Power Dissipation vs. Supply Voltage



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