HIGH VOLTAGE I_O = 500 mA LDO REGULATOR

■ FEATURES

- Fast transient response
- Wide operating voltage — 4.0 V to 40 V
- Wide operating temperature — T_a = −40°C to 125°C
- High-accuracy output voltage — V_O ±1.0% (T_a = 25°C)
- Output current — 500 mA (min)
- ON/OFF control
- Ceramic capacitor compatible
- Undervoltage lockout
- Thermal shutdown
- Overcurrent protection
- Package — TO-252-5-L5

■ APPLICATIONS

- Car infotainment
- Industrial equipment
- Consumer appliances

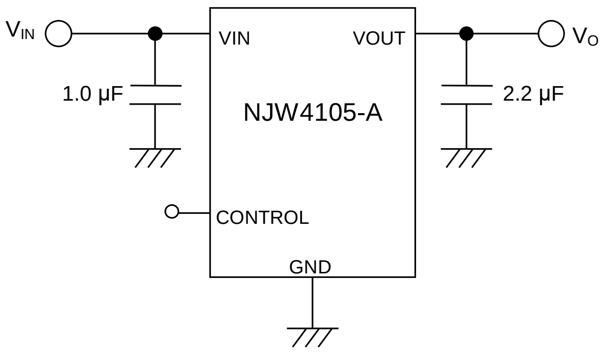
■ DESCRIPTION

The NJW4105 is a 45 V, I_O = 500 mA fast transient response low dropout regulator. This device achieves fast transient response and offers stable output voltage even at line or load fluctuations.

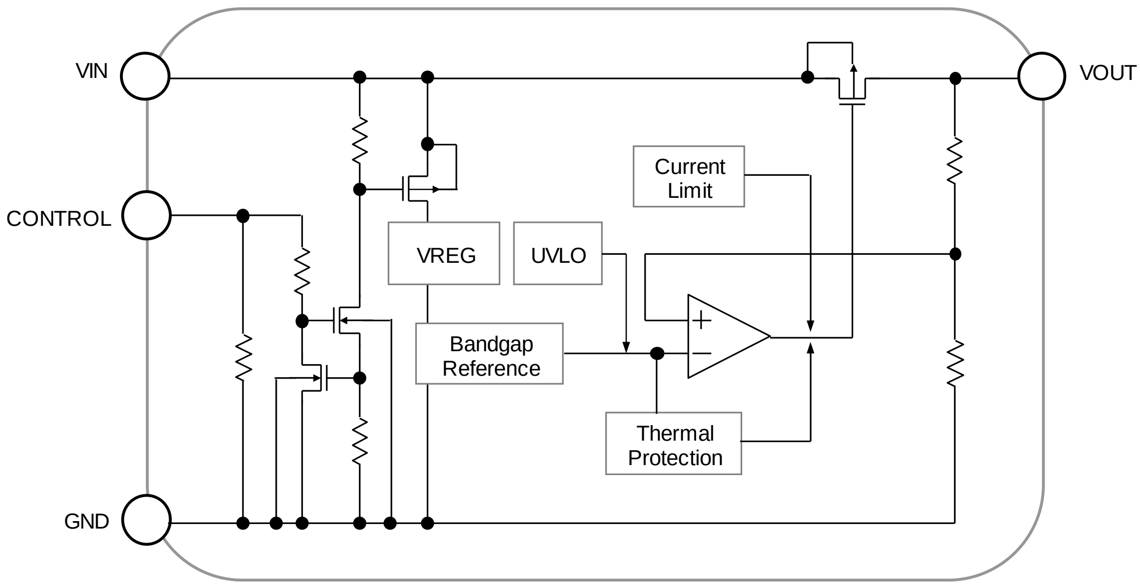
The NJW4105 provides outstanding high output voltage accuracy that guaranteed ±1.0% under the conditions of V_{IN} = V_O + 1 V to 40 V, I_O = 0 mA to 500 mA.

Moreover, wide operating voltage and wide operating temperature make the NJW4105 ideal for automotive accessories or applications that require high reliability.

■ TYPICAL APPLICATION



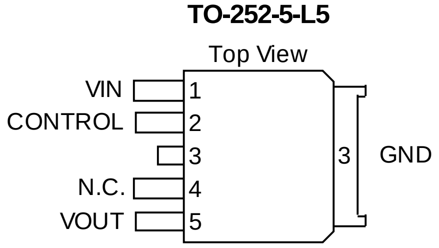
■ BLOCK DIAGRAM



■ OUTPUT VOLTAGE RANK

PRODUCT NAME	OUTPUT VOLTAGE
NJW4105DL5-33A	3.3 V
NJW4105DL5-05A	5.0 V
NJW4105DL5-08A	8.0 V

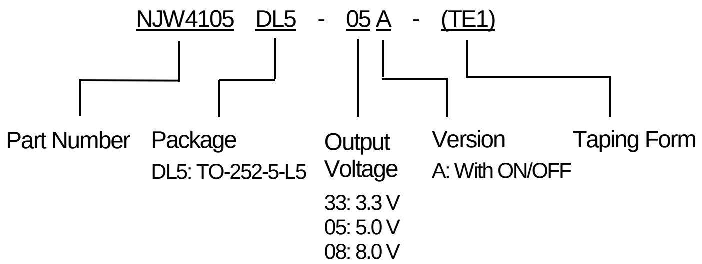
■ PIN CONFIGURATION



PIN NO.	NAME	FUNCTION
1	VIN	Input pin
2	CONTROL	ON/OFF control pin
3	GND	Ground pin
4	N.C.	Not internally connected*
5	VOUT	Output pin

*This pin is not internally connected. Connect to ground or leave floating (open). Connect to ground to improve thermal dissipation.

■ PRODUCT NAME INFORMATION



■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4105DL5-33A (TE1)	TO-252-5-L5	Yes	Yes	Sn-2Bi	105A33	301	3000
NJW4105DL5-05A (TE1)	TO-252-5-L5	Yes	Yes	Sn-2Bi	105A05	301	3000
NJW4105DL5-08A (TE1)	TO-252-5-L5	Yes	Yes	Sn-2Bi	105A08	301	3000

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Input Voltage	V_{IN}	−0.3 to 45	V
Control Voltage	V_{CONT}	−0.3 to 45	V
Output Voltage	V_O	−0.3 to V_{IN} ≤ +17 (1)	V
Power Dissipation (T_a = 25°C) TO-252-5-L5	P_D	2-Layer / 4-Layer / High Power 4-Layer 870 (2) / 3000 (3) / 4700 (4)	mW
Junction Temperature	T_j	−40 to 150	°C
Storage Temperature	T_{stg}	−50 to 150	°C

(1) When the input voltage is less than 17 V, the absolute maximum output voltage is equal to the input voltage. If the input voltage is below 17 V, the maximum output voltage is 17 V.
(2) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
(3) 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4).
(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)
(4) High Power 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm, 4-layer FR-4).
(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)
*For the specifications of each board, see the Board Specifications of THERMAL CHARACTERISTICS.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Operating Voltage	V_{IN}	4.0 to 40	V
Control Voltage	V_{CONT}	0 to 40	V
Output Current	I_O	0 to 500	mA
Operating Temperature	T_{opr}	−40 to 125	°C

■ ELECTRICAL CHARACTERISTICS

$V_{IN} = V_O + 1$ V, $C_{IN} = 1.0$ μF, $C_O = 2.2$ μF, $T_a = 25$°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Voltage	V_O	$V_{IN} = V_O + 1$ V to 40 V, $I_O = 0$ mA to 500 mA		−1.0%	-	+1.0%	V
Quiescent Current	I_Q	$I_O = 0$ mA, except I_{CONT}		-	65	105	μA
Quiescent Current at Control OFF	$I_{Q(OFF)}$	$V_{CONT} = 0$ V		-	-	1	μA
Output Current	I_O	$V_O \times 0.9$		500	-	-	mA
Line Regulation	$\Delta V_O/\Delta V_{IN}$	$V_{IN} = V_O + 1$ V to 40 V, $I_O = 30$ mA	$V_O = 3.3$ V	-	-	23.5	mV
			$V_O = 5.0$ V	-	-	34.0	
			$V_O = 8.0$ V	-	-	52.5	
Load Regulation	$\Delta V_O/\Delta I_O$	$I_O = 0$ mA to 500 mA	$V_O = 3.3$ V	-	-	18.5	mV
			$V_O = 5.0$ V	-	-	22.5	
			$V_O = 8.0$ V	-	-	36.0	
Ripple Rejection	RR	$V_{IN} = V_O + 1$ V, ein = 200 mVrms, f = 1 kHz, $I_O = 10$ mA	$V_O = 3.3$ V	-	56	-	dB
			$V_O = 5.0$ V	-	53	-	
			$V_O = 8.0$ V	-	50	-	
Dropout Voltage 1 (5)	ΔV_{IO1}	$I_O = 300$ mA		-	0.24	0.42	V
Dropout Voltage 2 (5)	ΔV_{IO2}	$I_O = 500$ mA		-	0.40	0.70	V
Control Current	I_{CONT}	$V_{CONT} = 1.6$ V		-	0.5	2.0	μA
Control Voltage for ON-State	$V_{CONT(ON)}$			1.6	-	-	V
Control Voltage for OFF-State	$V_{CONT(OFF)}$			-	-	0.6	V
UVLO Release Voltage	V_{UVLO}	V_{IN} = low to high		2.3	2.7	3.1	V
UVLO Hysteresis Voltage	V_{HYS}	V_{IN} = high to low		200	500	-	mV
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T_a$	$T_a = -40$°C to 125°C, $I_O = 30$ mA		-	±50	-	ppm/°C

(5) Output voltages below 3.8 V are excluded.

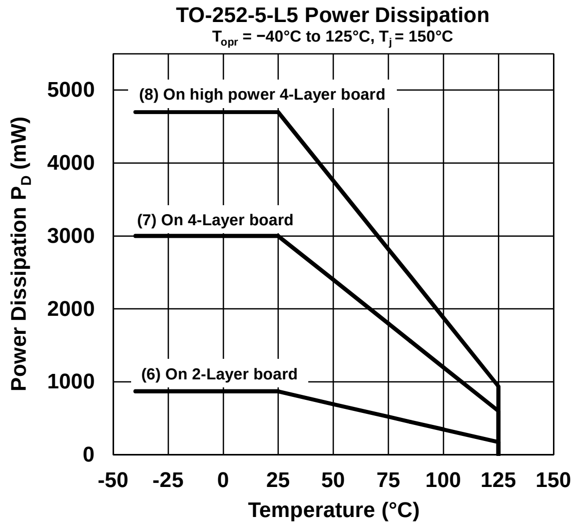
■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-To-Ambient Thermal Resistance TO-252-5-L5	θ_{ja}	2-Layer / 4-Layer / High Power 4-Layer 143 (6) / 41 (7) / 26 (8)	°C/W
Junction-To-Top of Package Characterization Parameter TO-252-5-L5	ψ_{jt}	2-Layer / 4-Layer / High Power 4-Layer 30 (6) / 15 (7) / 11 (8)	°C/W

■ BOARD SPECIFICATIONS

BOARD		JEDEC 2-LAYER BOARD	JEDEC 4-LAYER BOARD	HIGH POWER 4-LAYER BOARD
Dimension		76.2 mm × 114.3 mm, t = 1.6 mm		
Material		FR-4		
Cu Area	Surface Layer (Thickness: 70 µm)	NJR recommended land pattern + Measurement wiring	NJR recommended land pattern + Measurement wiring	NJR recommended land pattern + Heat dissipation pattern (50 mm × 50 mm) + Measurement wiring
	2nd Layer (Thickness: 35 µm)	-	74.2 mm × 74.2 mm	74.2 mm × 74.2 mm
	3rd Layer (Thickness: 35 µm)	-	74.2 mm × 74.2 mm	74.2 mm × 74.2 mm
	Back Layer (Thickness: 70 µm)	-	-	74.2 mm × 74.2 mm
Thermal Vias		-	Connected from surface layer to 2nd layer	All layers are connected

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



(6) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
(7) 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4).
(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)
(8) High Power 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm, 4-layer FR-4).
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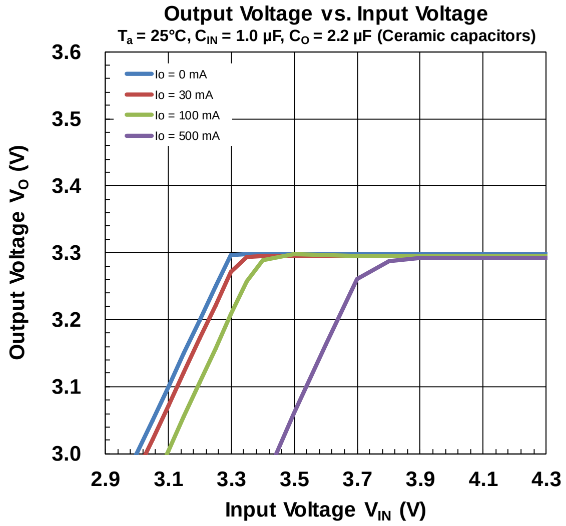
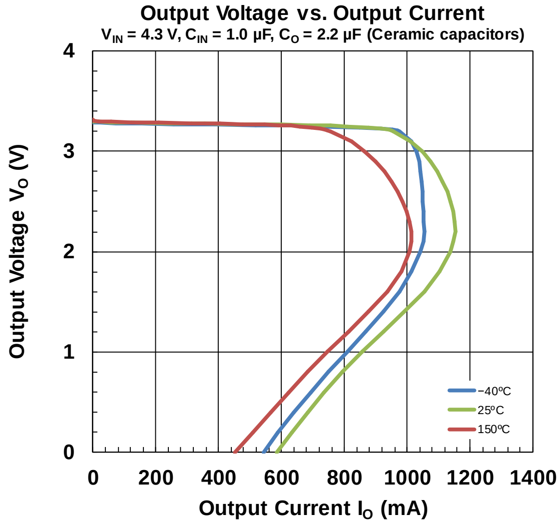
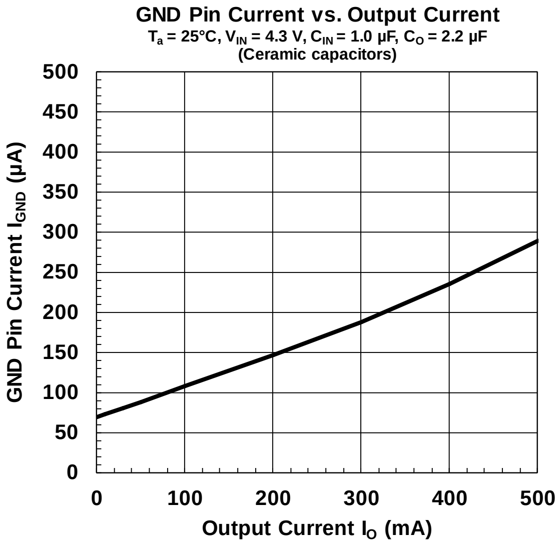
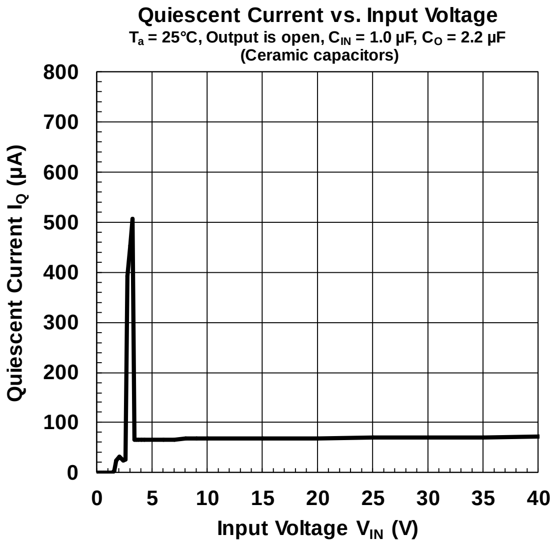
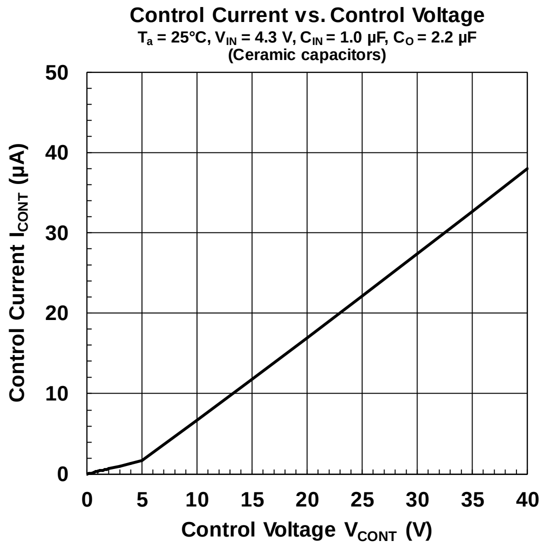
■ TYPICAL CHARACTERISTICS (V_O = 3.3 V)

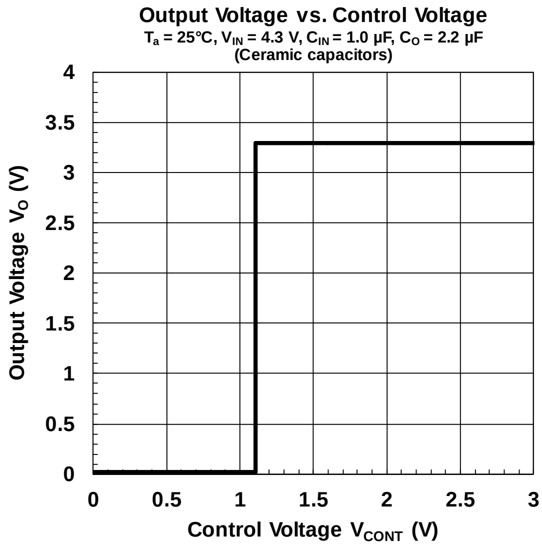




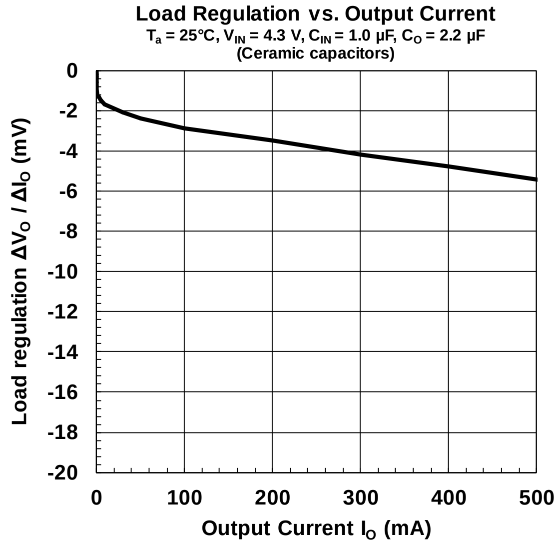


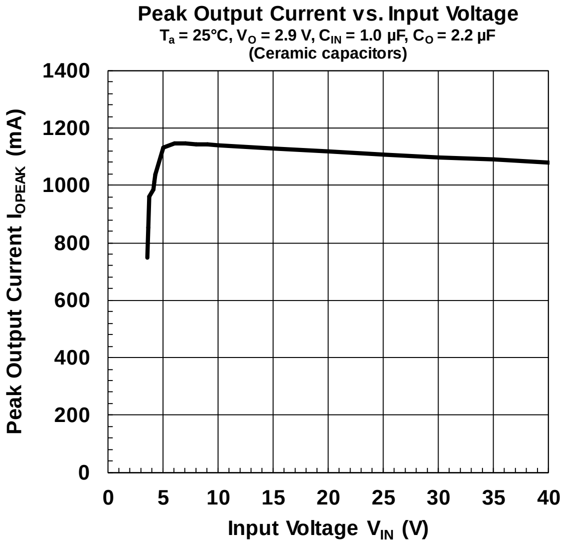


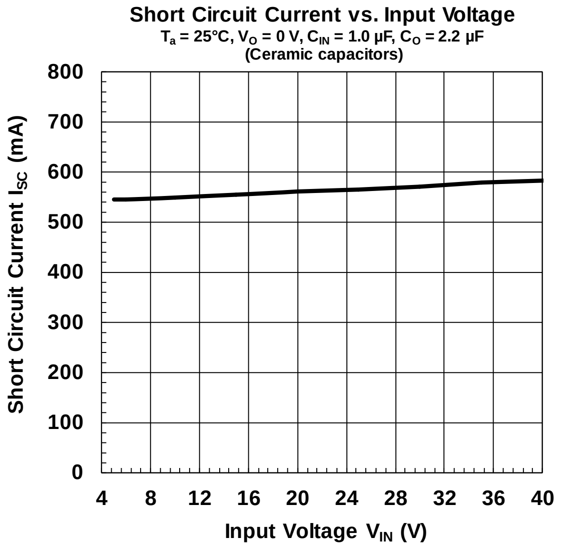


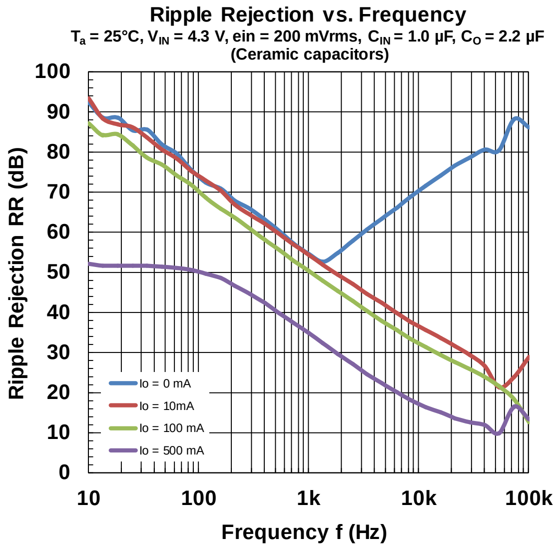


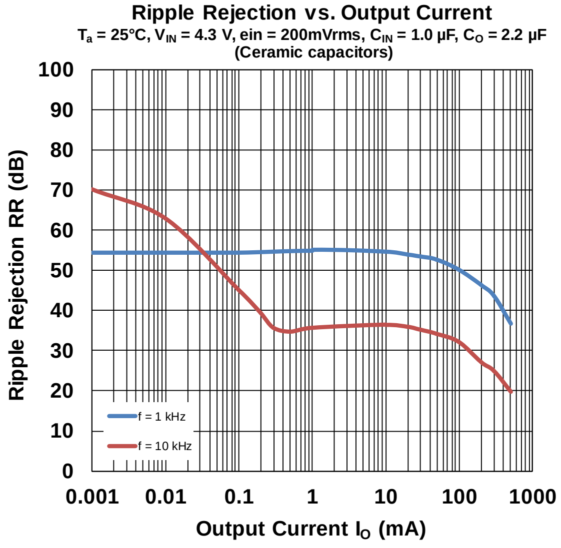
■ TYPICAL CHARACTERISTICS (V_O = 3.3 V)

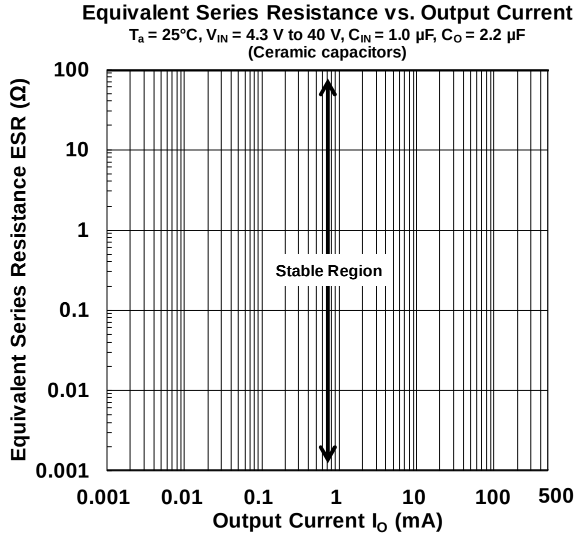












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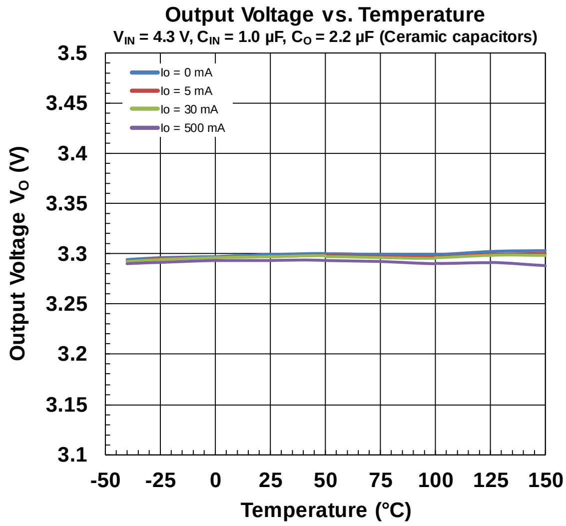

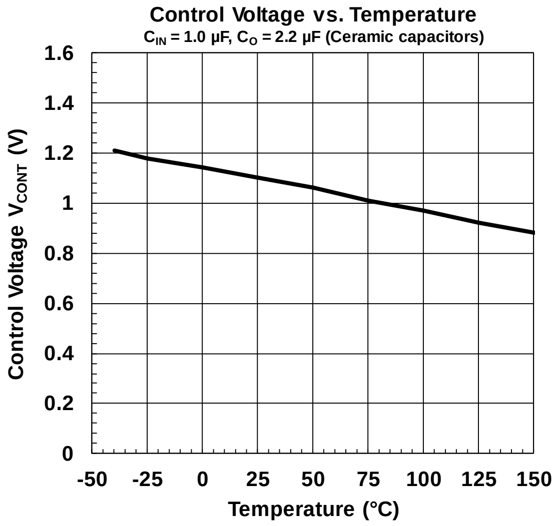

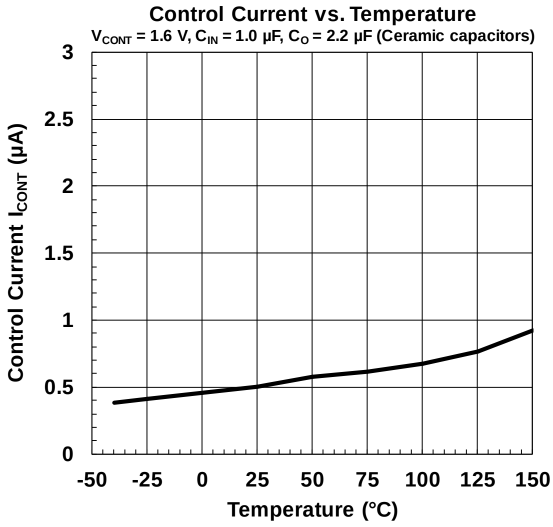

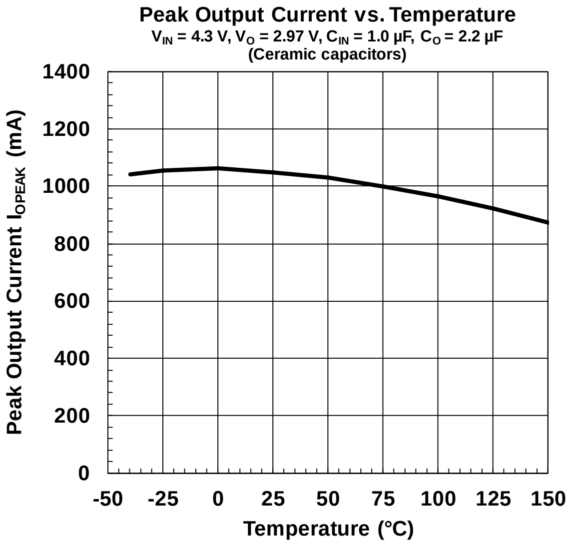

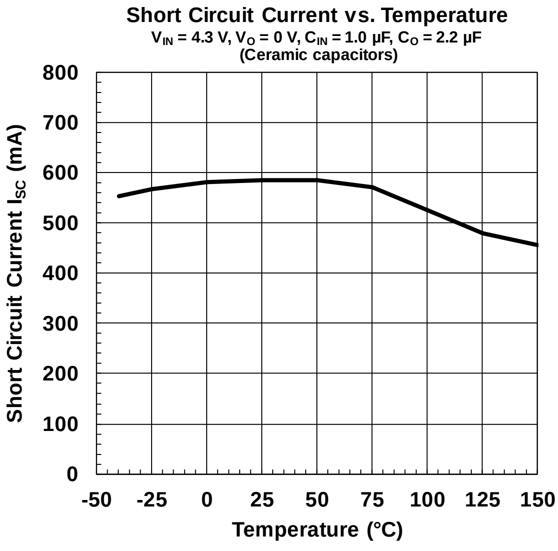

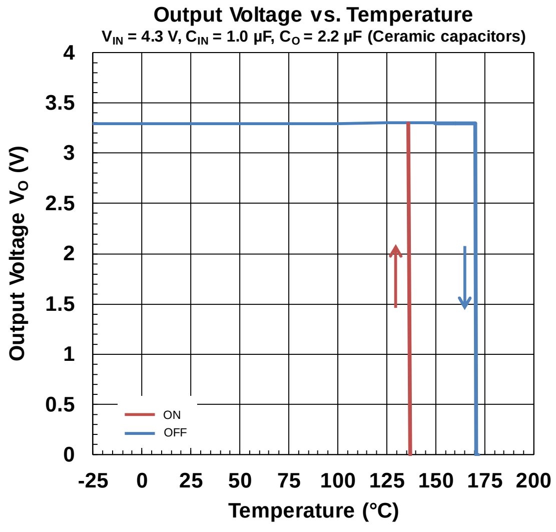

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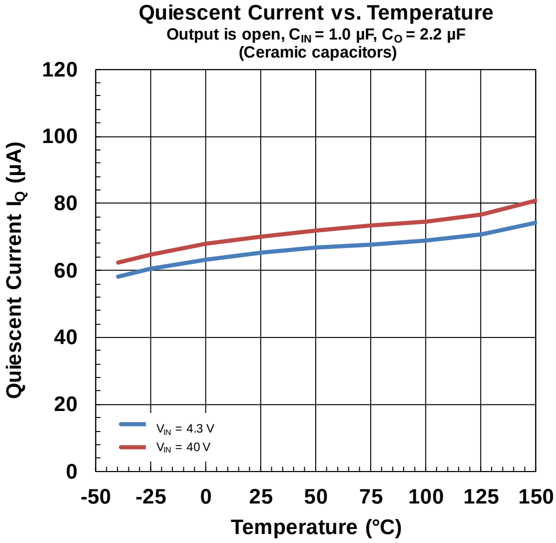
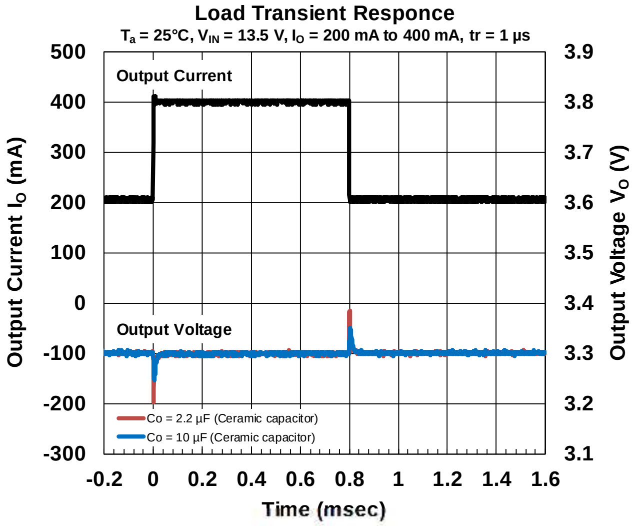
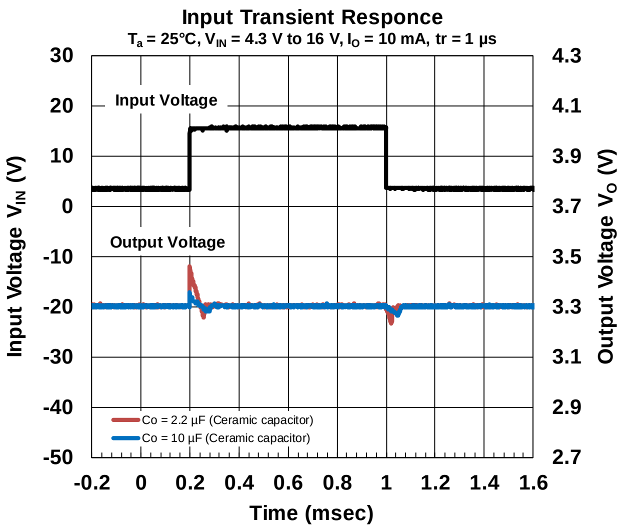
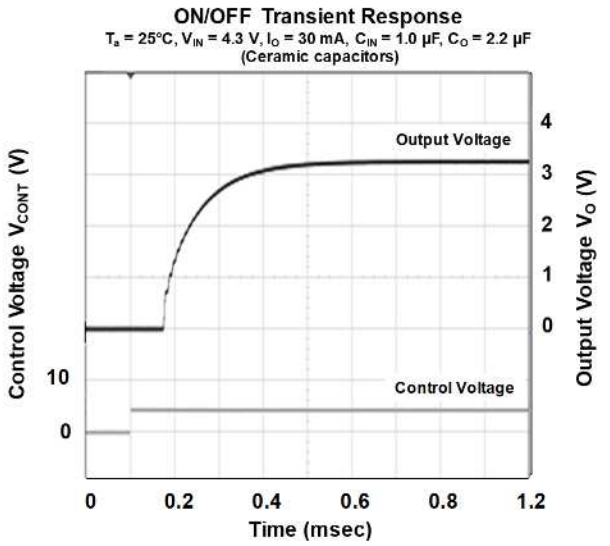
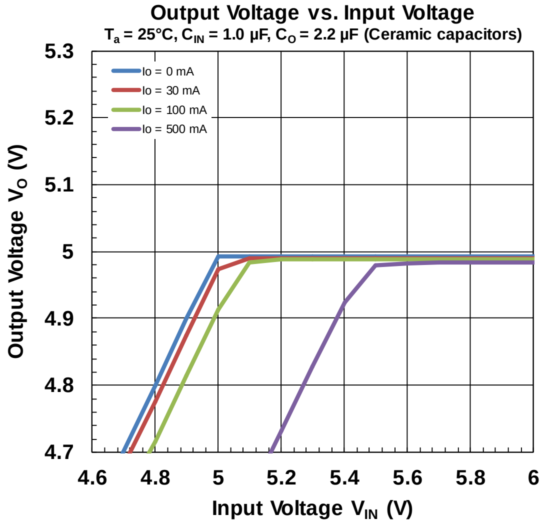


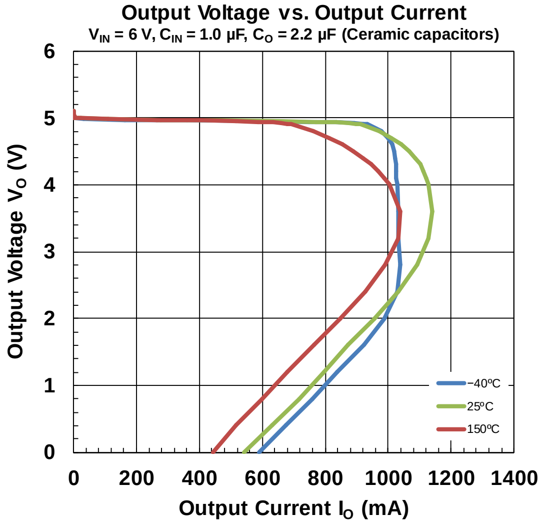


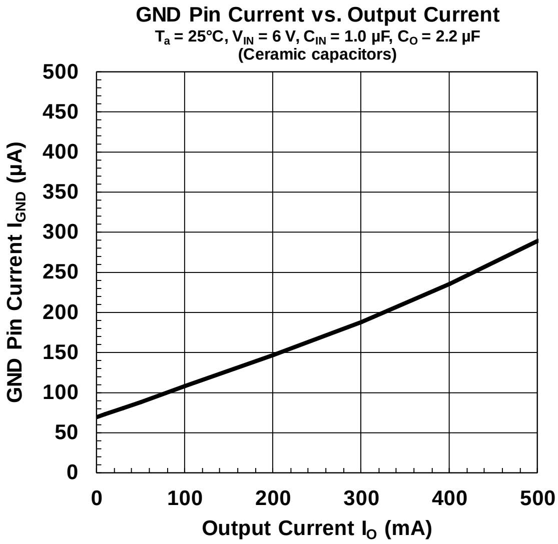


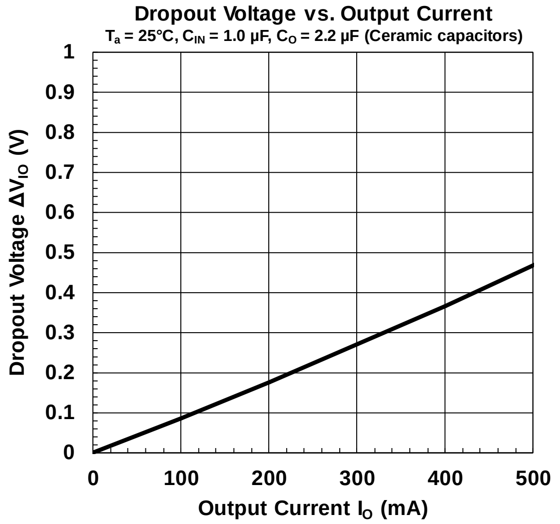


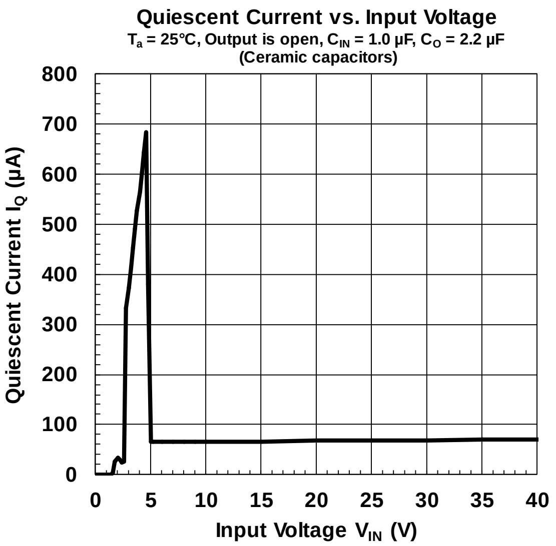
■ TYPICAL CHARACTERISTICS (V_O = 5 V)

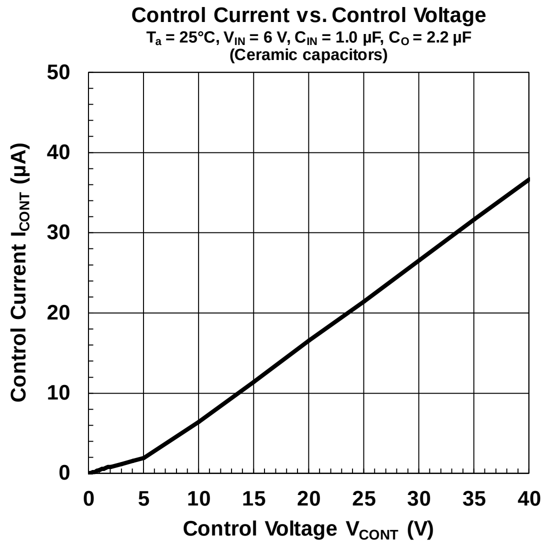




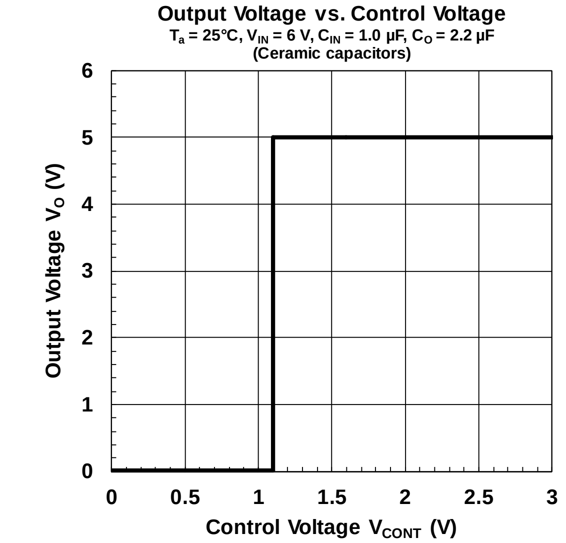


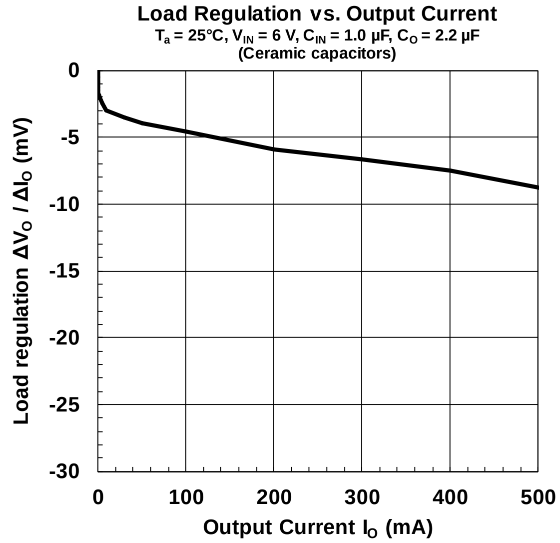


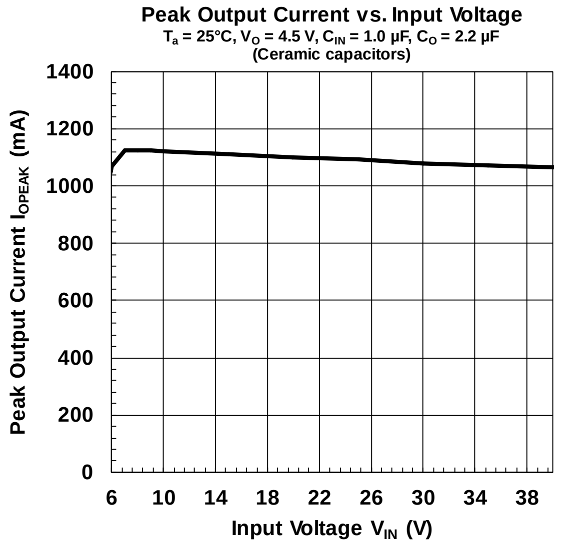


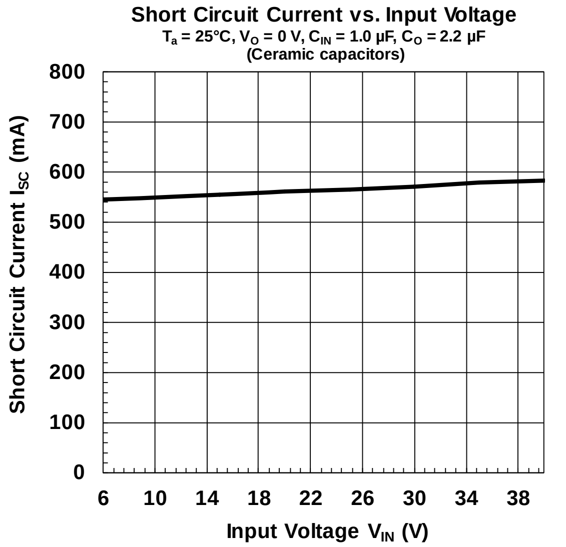


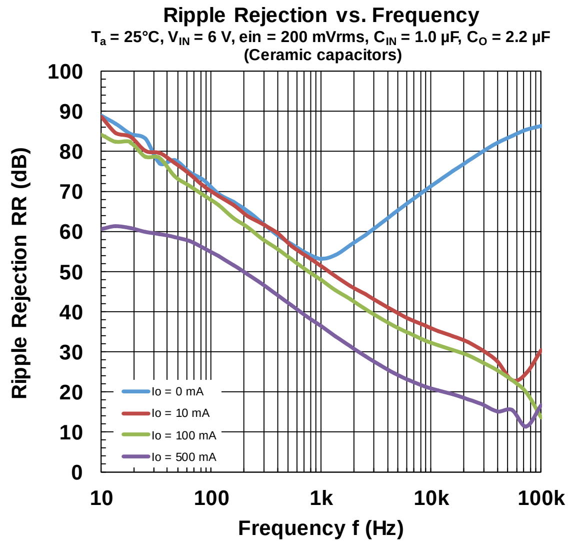
■ TYPICAL CHARACTERISTICS (V_O = 5 V)

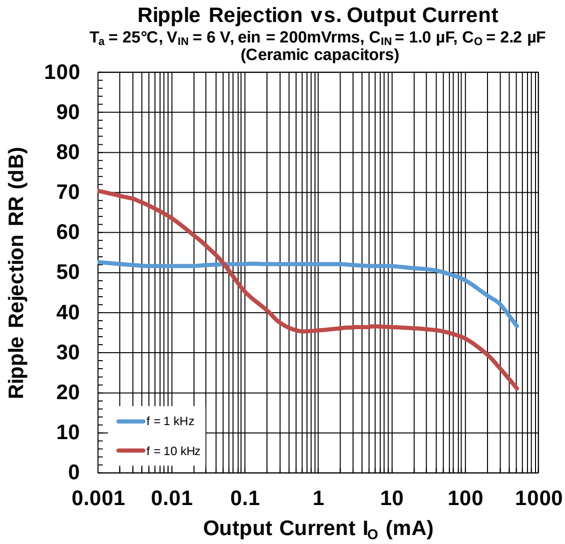






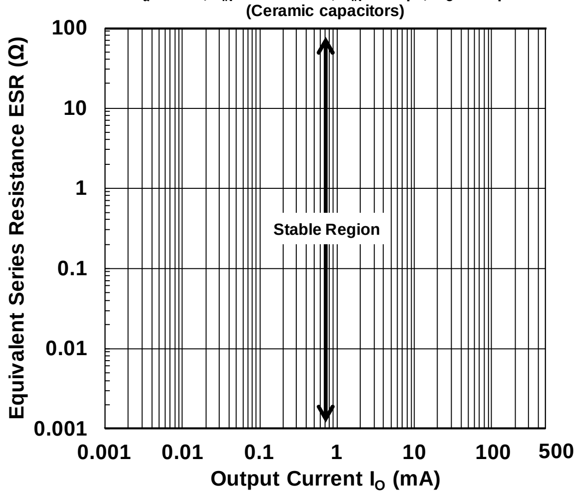




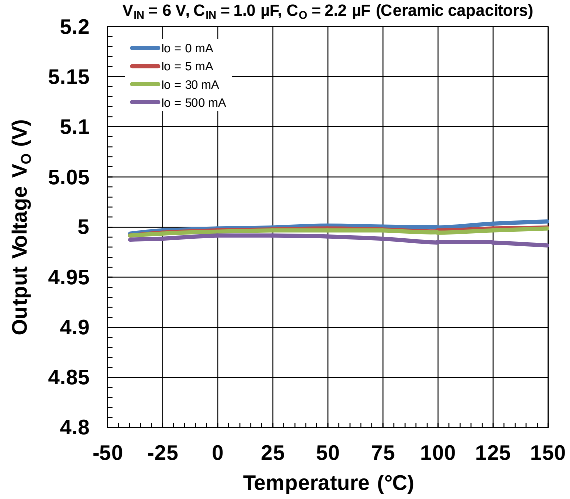


■ TYPICAL CHARACTERISTICS (V_O = 5 V)

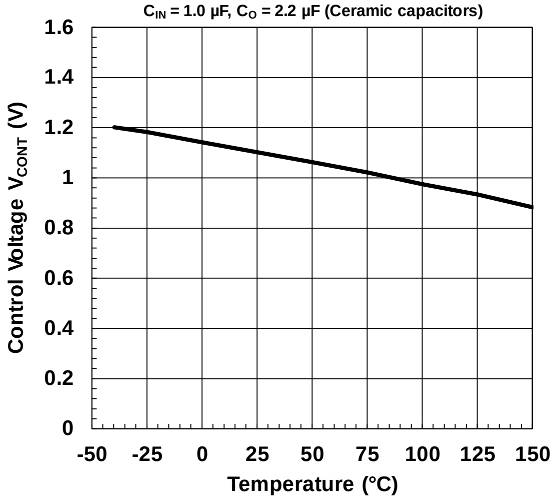
Equivalent Series Resistance vs. Output Current
T_a = 25°C, V_{IN} = 6 V to 40 V, C_{IN} = 1.0 µF, C_O = 2.2 µF
(Ceramic capacitors)



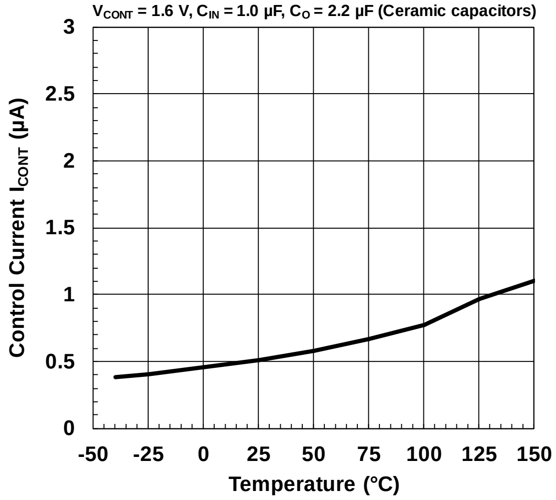
Output Voltage vs. Temperature
V_{IN} = 6 V, C_{IN} = 1.0 µF, C_O = 2.2 µF (Ceramic capacitors)



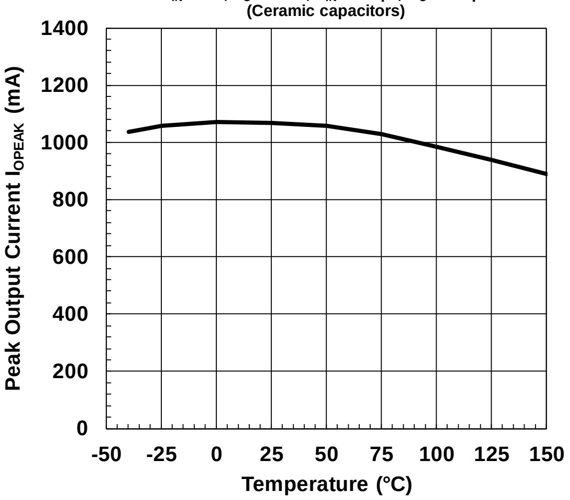
Control Voltage vs. Temperature
C_{IN} = 1.0 µF, C_O = 2.2 µF (Ceramic capacitors)



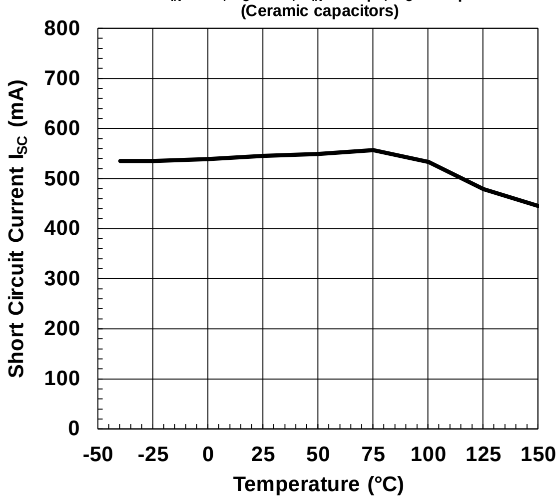
Control Current vs. Temperature
V_{CONT} = 1.6 V, C_{IN} = 1.0 µF, C_O = 2.2 µF (Ceramic capacitors)



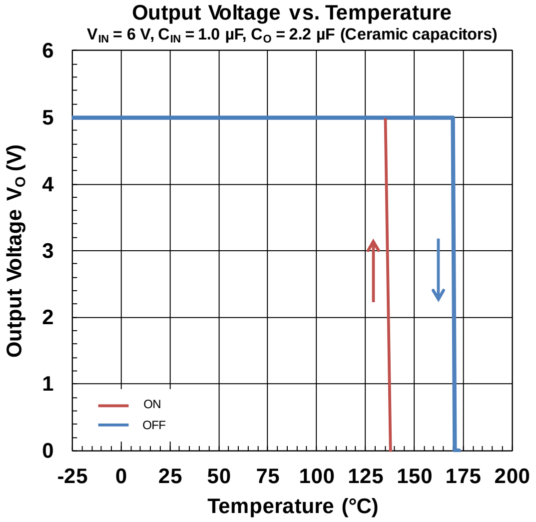
Peak Output Current vs. Temperature
V_{IN} = 6 V, V_O = 4.5 V, C_{IN} = 1.0 µF, C_O = 2.2 µF
(Ceramic capacitors)

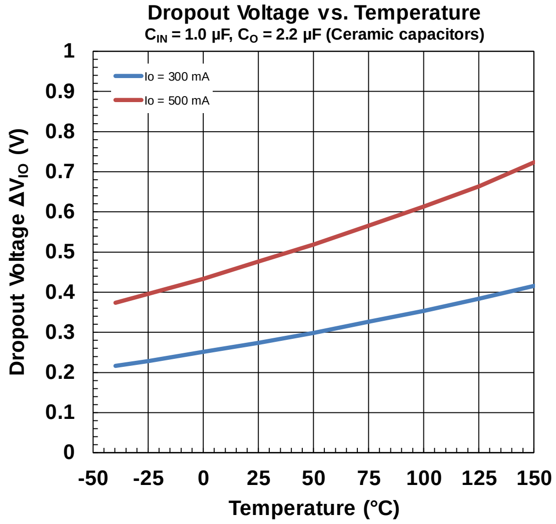


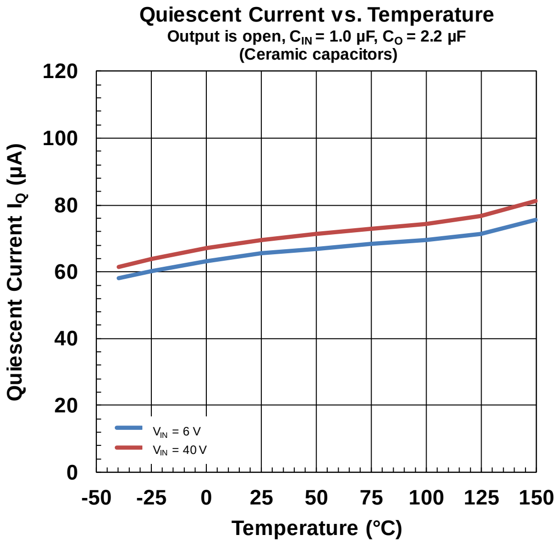
Short Circuit Current vs. Temperature
V_{IN} = 6 V, V_O = 0 V, C_{IN} = 1.0 µF, C_O = 2.2 µF
(Ceramic capacitors)

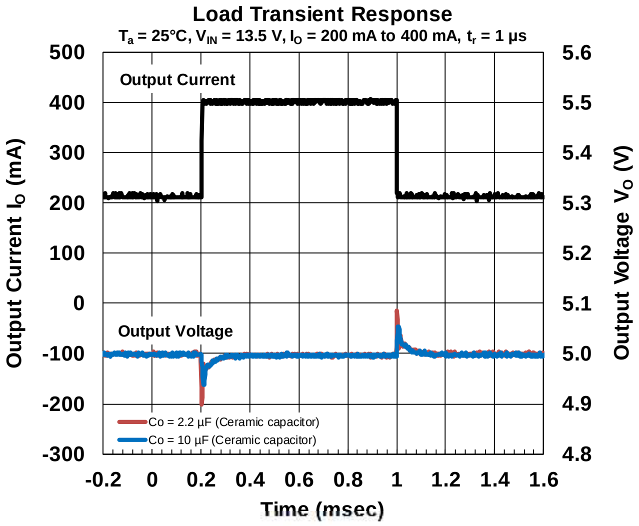


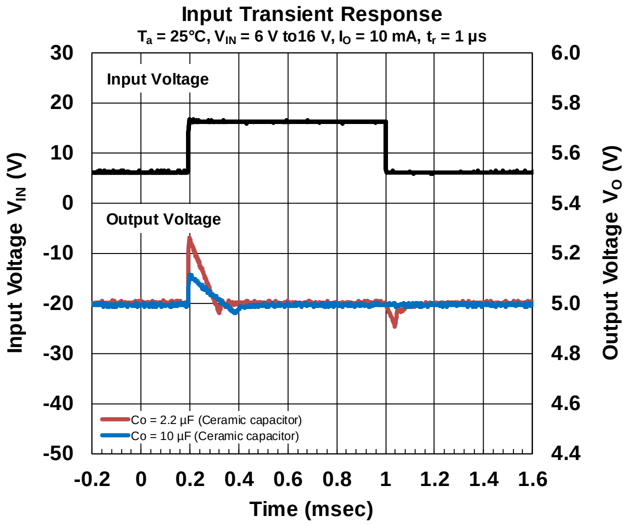
■ TYPICAL CHARACTERISTICS (V_O = 5 V)

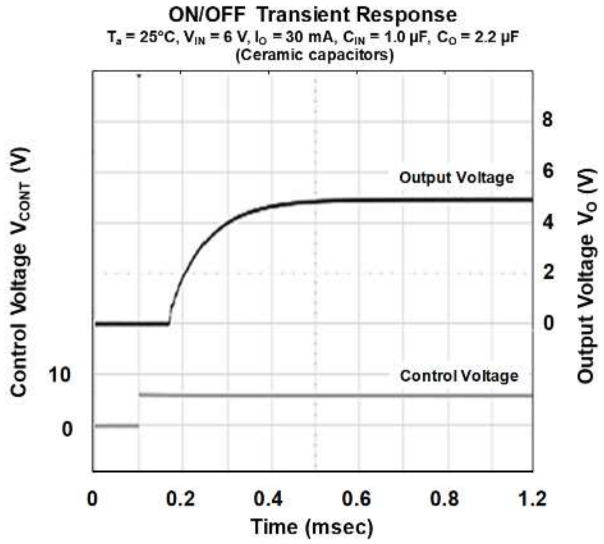




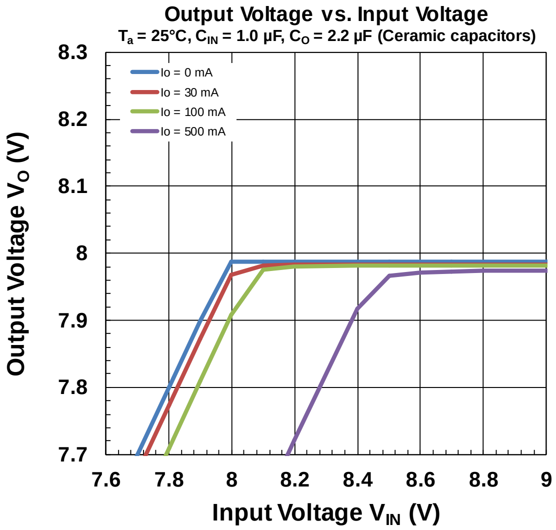


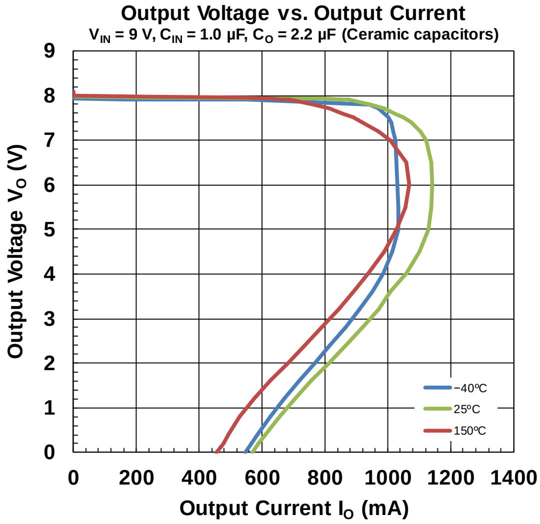


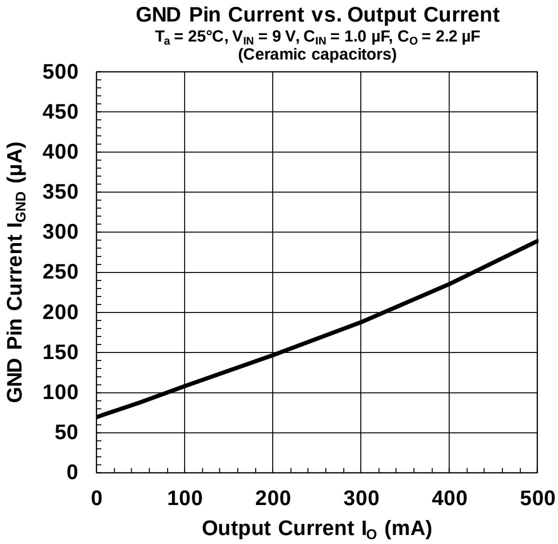


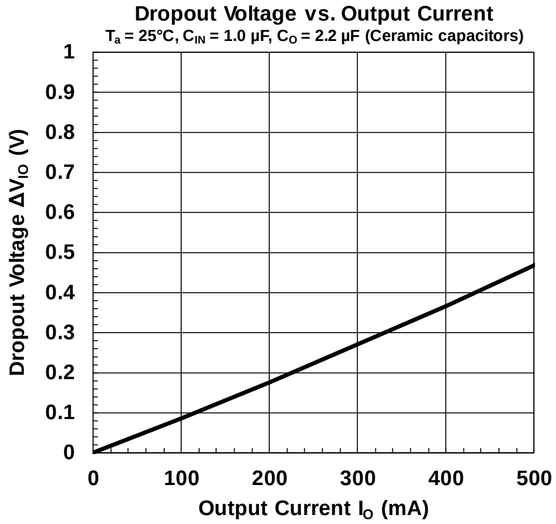


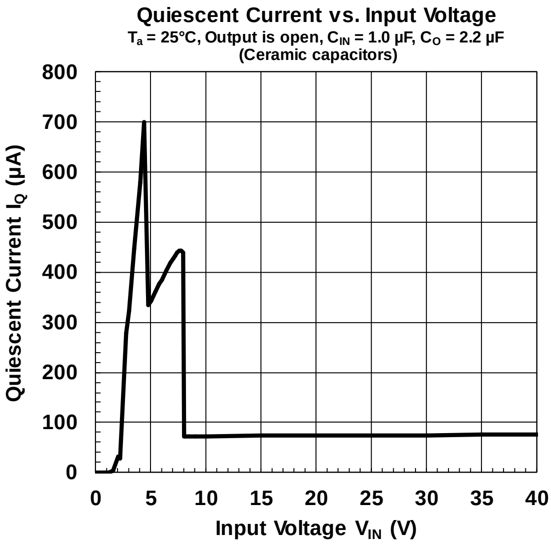
■ TYPICAL CHARACTERISTICS (V_O = 8 V)

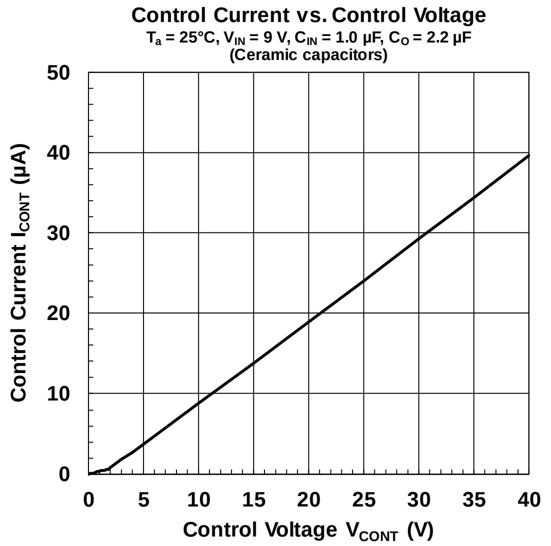






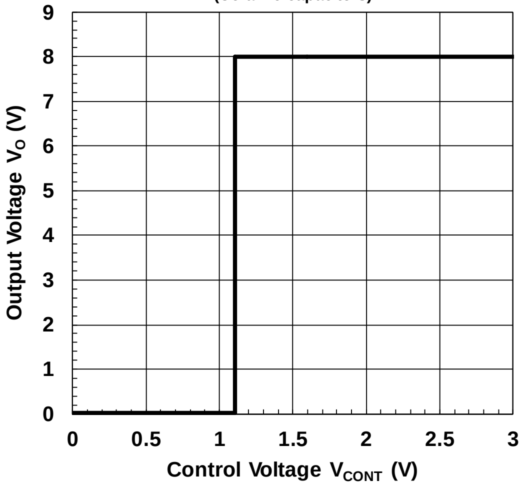




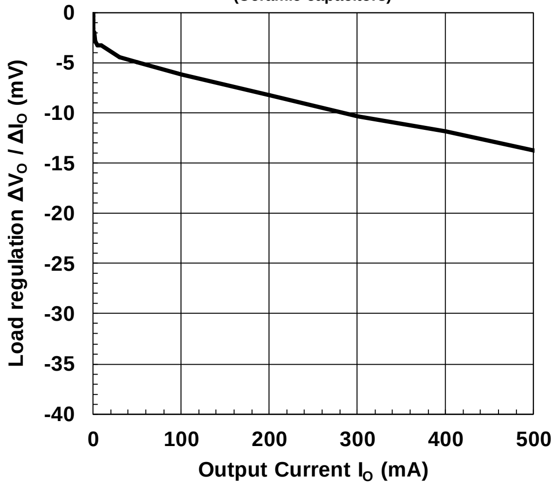


■ TYPICAL CHARACTERISTICS (V_O = 8 V)

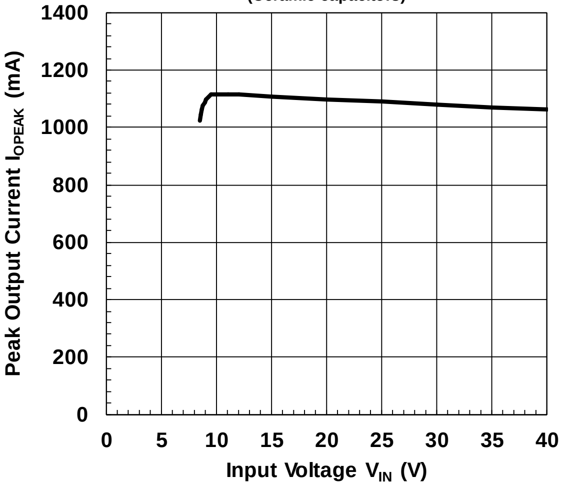
Output Voltage vs. Control Voltage
T_a = 25°C, V_{IN} = 9 V, C_{IN} = 1.0 µF, C_O = 2.2 µF
(Ceramic capacitors)



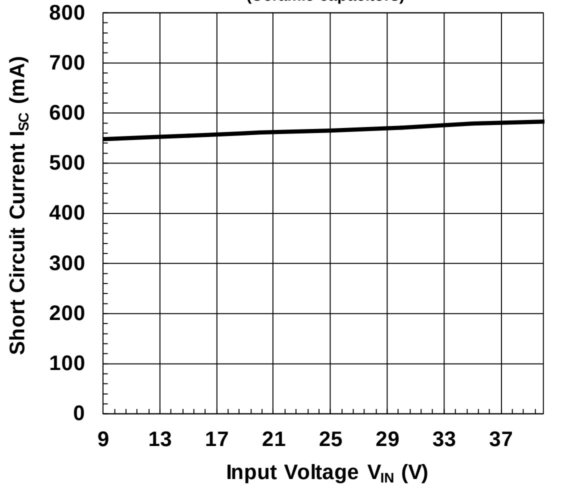
Load Regulation vs. Output Current
T_a = 25°C, V_{IN} = 9 V, C_{IN} = 1.0 µF, C_O = 2.2 µF
(Ceramic capacitors)



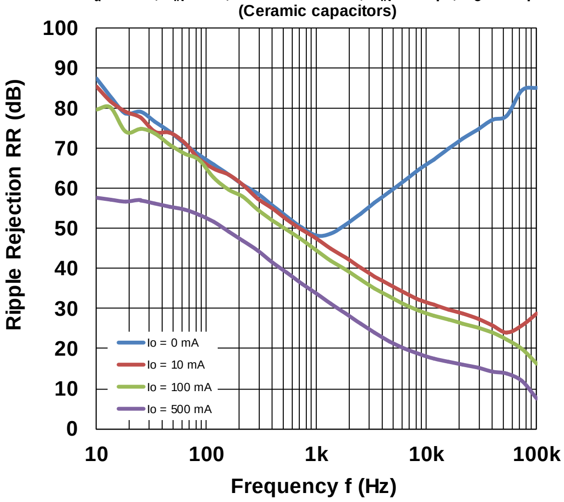
Peak Output Current vs. Input Voltage
T_a = 25°C, V_O = 7.2 V, C_{IN} = 1.0 µF, C_O = 2.2 µF
(Ceramic capacitors)



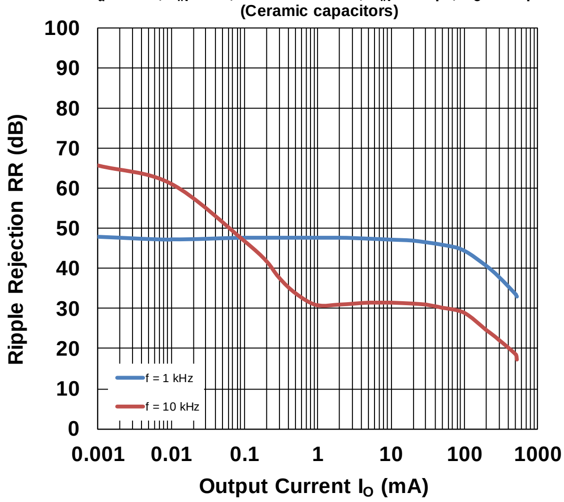
Short Circuit Current vs. Input Voltage
T_a = 25°C, V_O = 0 V, C_{IN} = 1.0 µF, C_O = 2.2 µF
(Ceramic capacitors)



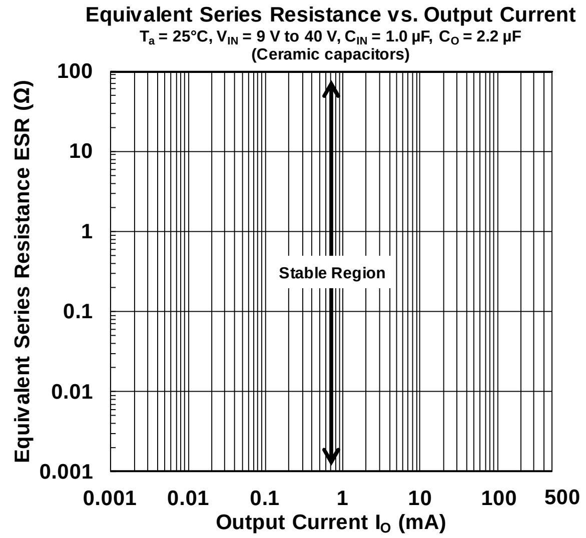
Ripple Rejection vs. Frequency
T_a = 25°C, V_{IN} = 9 V, ein = 200 mVrms, C_{IN} = 1.0 µF, C_O = 2.2 µF
(Ceramic capacitors)

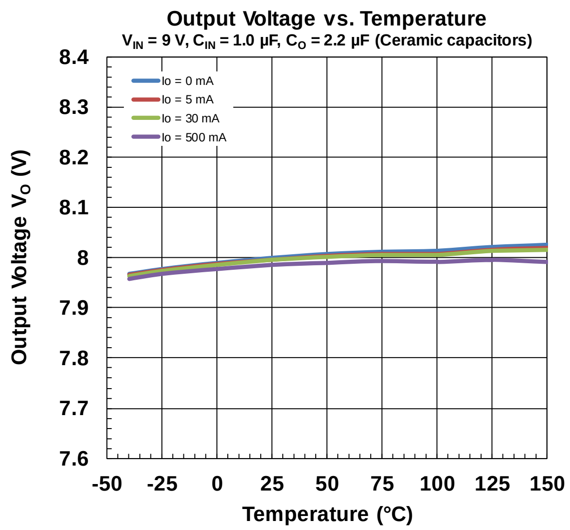


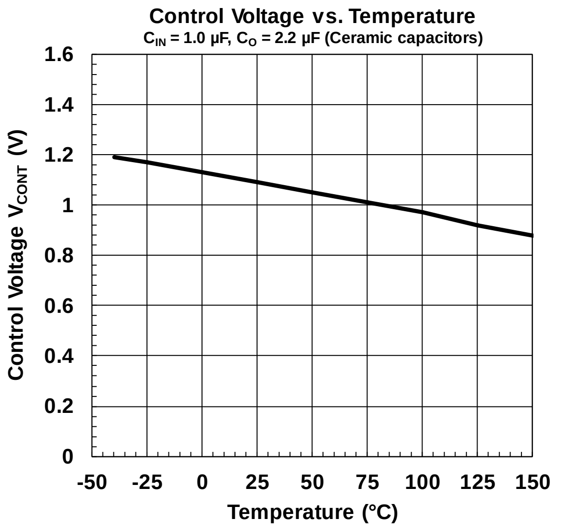
Ripple Rejection vs. Output Current
T_a = 25°C, V_{IN} = 9 V, ein = 200mVrms, C_{IN} = 1.0 µF, C_O = 2.2 µF
(Ceramic capacitors)

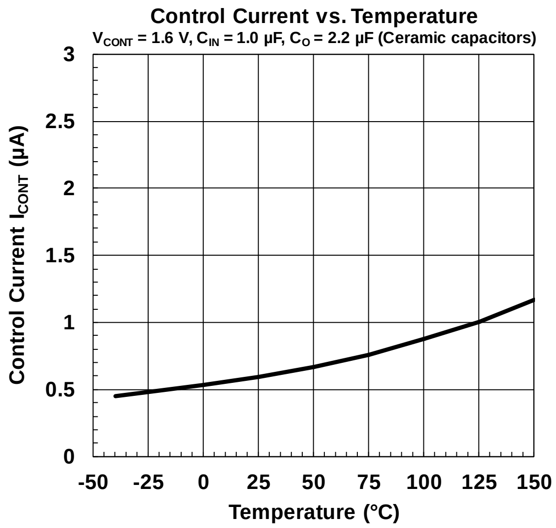


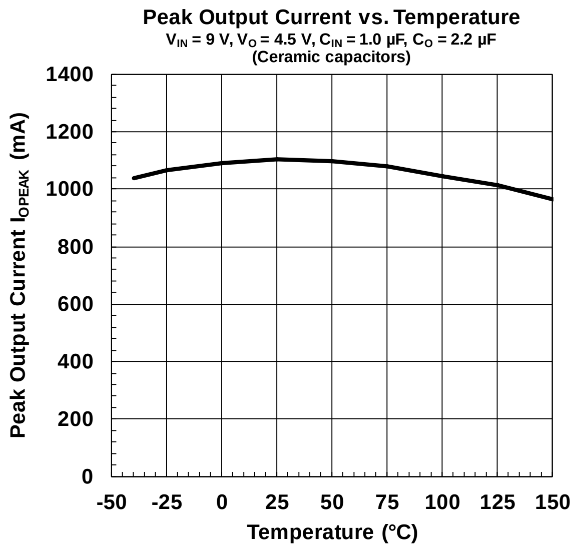
■ TYPICAL CHARACTERISTICS (V_O = 8 V)

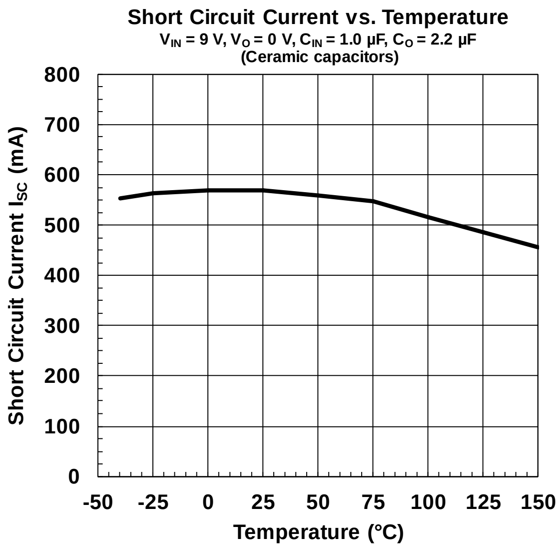




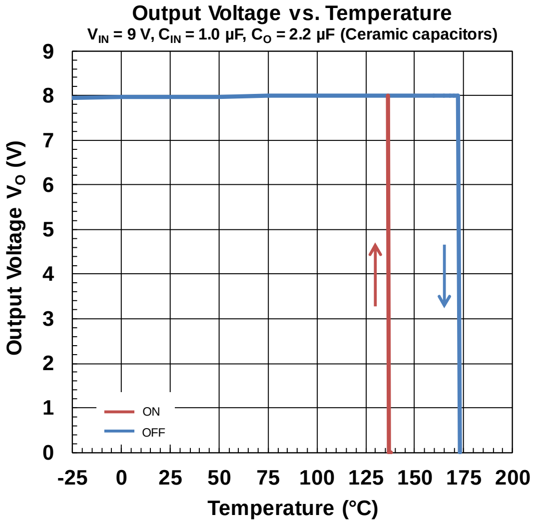


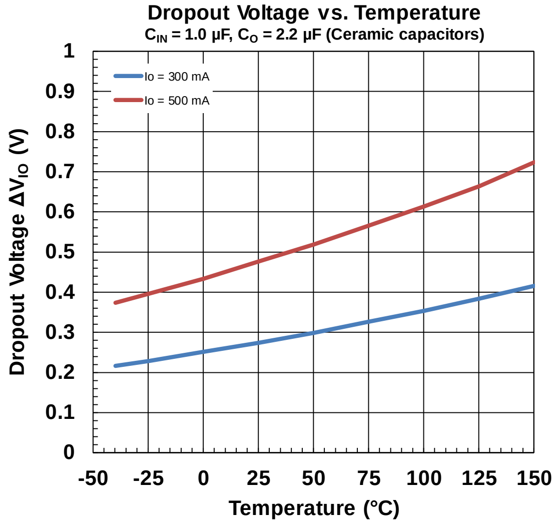


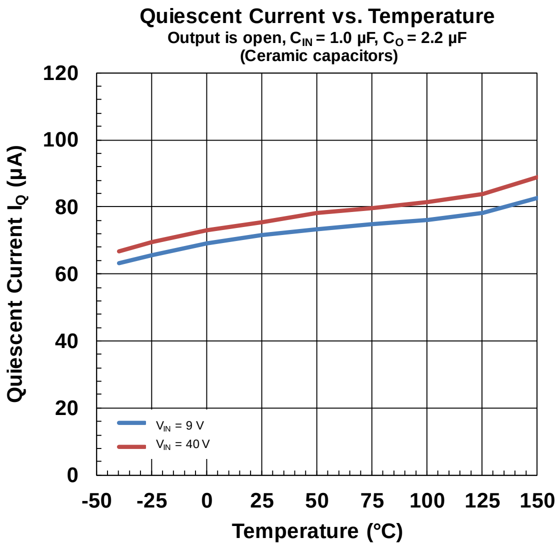


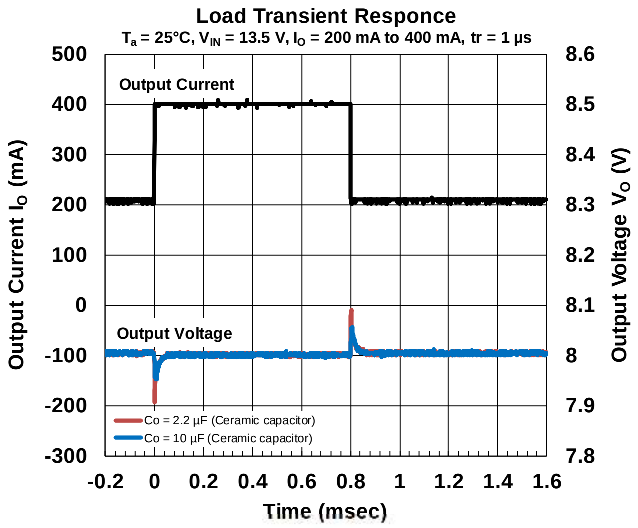


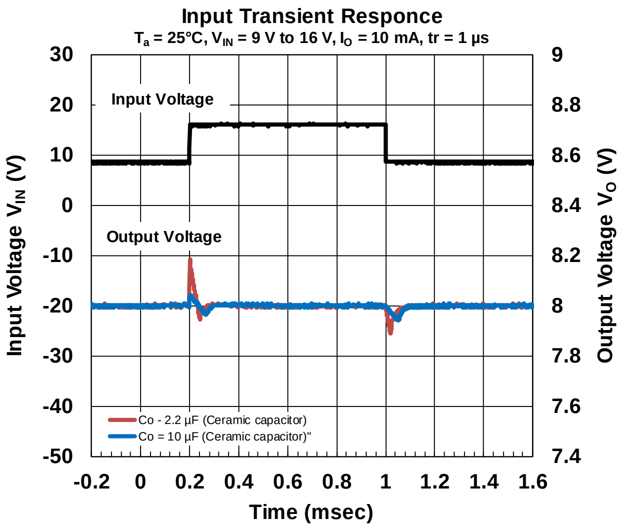
■ TYPICAL CHARACTERISTICS (V_O = 8 V)

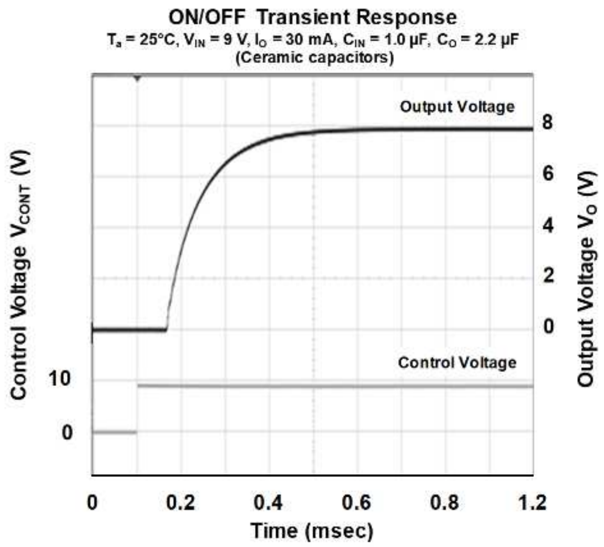






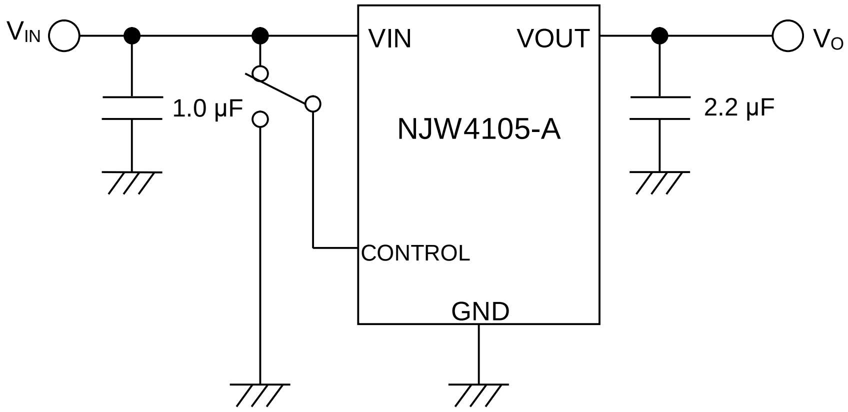






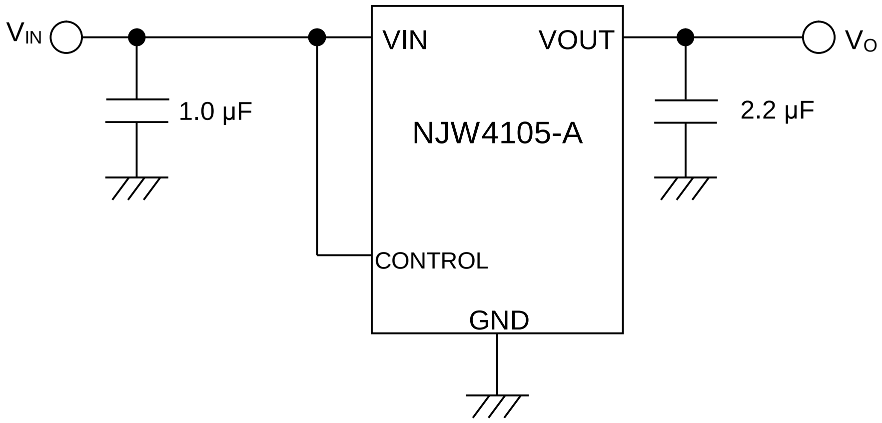
■ **TYPICAL APPLICATION**

1. When ON/OFF control is used.



The CONTROL pin is turned on at high level and turned off at open or GND level.

2. When ON/OFF control is not used.



Connect the CONTROL pin to the V_{IN}.

■ APPLICATION NOTE

Input Capacitor (C_{IN})

The C_{IN} prevents oscillations and reduce power supply ripple of applications when the power supply impedance is high or power supply line is long. Connecting a 1.0 µF or larger C_{IN} between VIN and GND pins as short path as possible.

Output Capacitor (C_O)

C_O is necessary for phase compensation of the internal error amplifier in the regulator, and the capacitance value and ESR affect the stability of the circuit. If a capacitor less than 2.2 µF is used, output noise and/or regulator oscillation may occur due to lack of the phase compensation. For stable operation, connect a 2.2 µF or larger C_O within the stable operation region (0.001 Ω ≤ ESR ≤ 100 Ω) between the VOUT and GND pins as short path as possible. The recommended capacitance value varies depending on the output voltage, and a low output voltage may require a large capacitance value; therefore, confirm the recommended capacitance of the required output voltage. As the capacitance value of C_O increases, output noise and ripple decrease, and the response to output load fluctuations also improves.

Select the output capacitor considering various characteristics such as frequency characteristics, temperature characteristics, and DC bias characteristics. For the C_O, a capacitor with excellent temperature characteristics and sufficient margin for output voltage is recommended.

Undervoltage Lockout (UVLO)

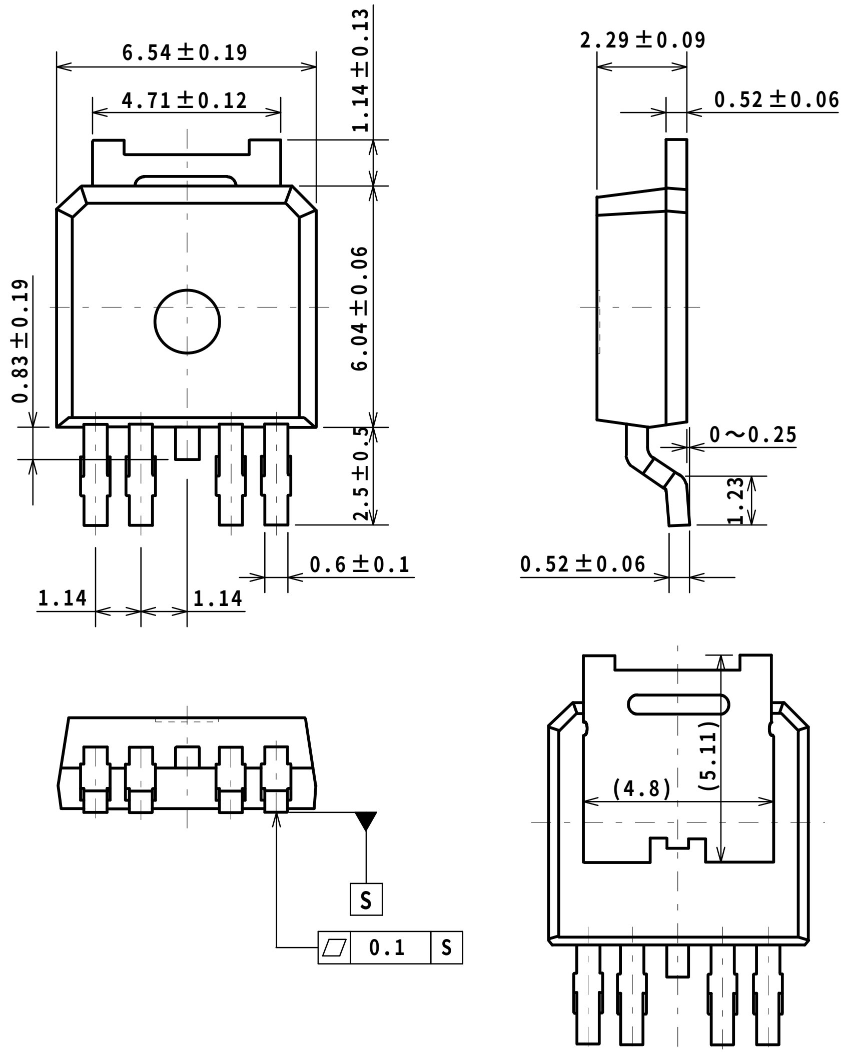
This circuit prevents malfunction by locking out the output when V_{IN} is below the UVLO detection voltage. The output voltage rises when the input voltage rises and exceeds the UVLO release voltage (2.7 V, typ). When the input voltage drops below the UVLO detection voltage (2.2 V, typ)*, the output voltage falls.

*UVLO detection voltage (2.2 V, typ) = UVLO release voltage (2.7 V, typ) − UVLO hysteresis voltage (500 mV, typ)

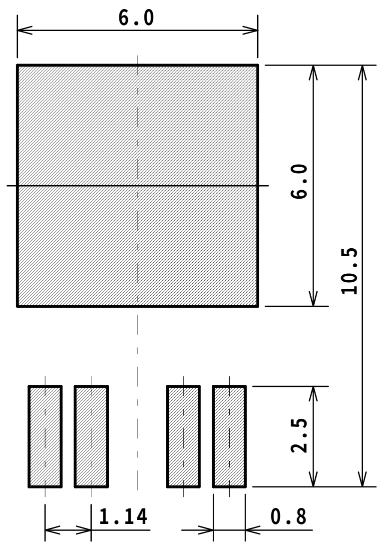
TO-252-5-L5

Unit: mm

■ PACKAGE DIMENSIONS



■ EXAMPLE OF SOLDER PADS DIMENSIONS

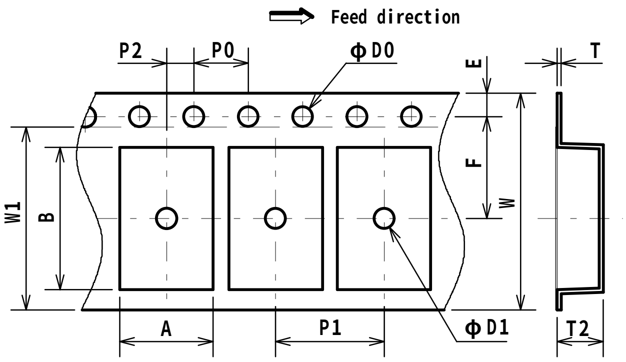


TO-252-5-L5

Unit: mm

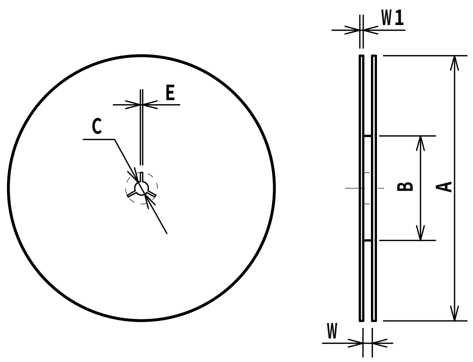
■ PACKING SPEC

TAPING DIMENSIONS



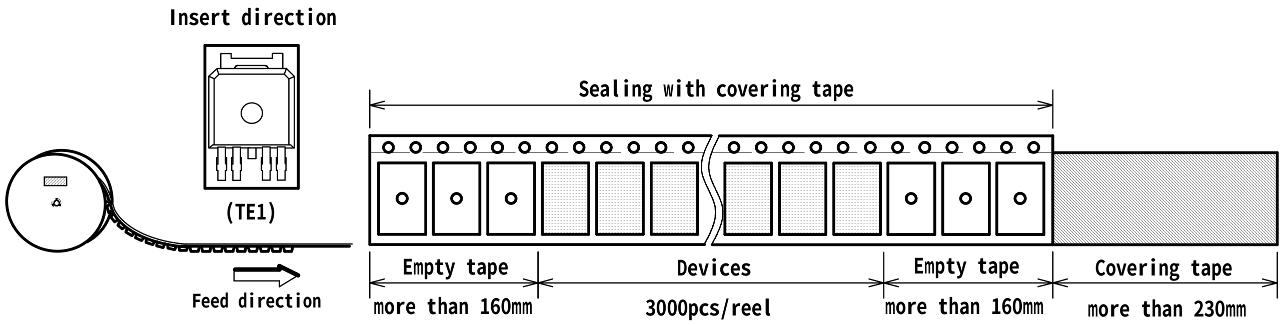
SYMBOL	DIMENSION	REMARKS
A	6.9±0.1	BOTTOM DIMENSION
B	10.5±0.1	BOTTOM DIMENSION
D0	1.5 $^{+0.1}_{0}$	
D1	1.5 $^{+0.1}_{0}$	
E	1.75±0.1	
F	7.5±0.1	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.1	
T	0.3±0.1	
T2	3.4 max	
W	16.0±0.3	
W1	13.5	THICKNESS 0.1max

REEL DIMENSIONS

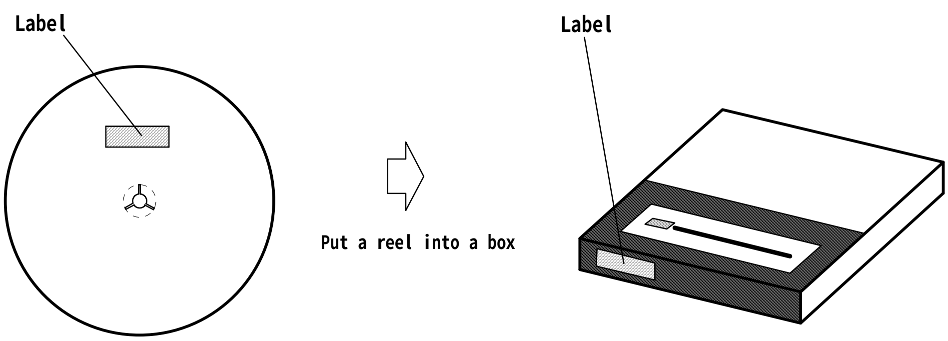


SYMBOL	DIMENSION
A	φ330±2
B	φ 80±1
C	φ 13±0.5
E	2
W	17.5±0.5
W1	2±0.5

TAPING STATE

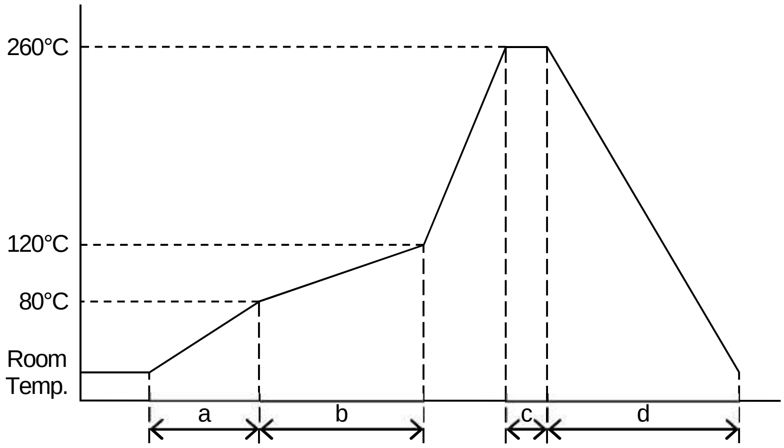


PACKING STATE



■ RECOMMENDED MOUNTING METHOD

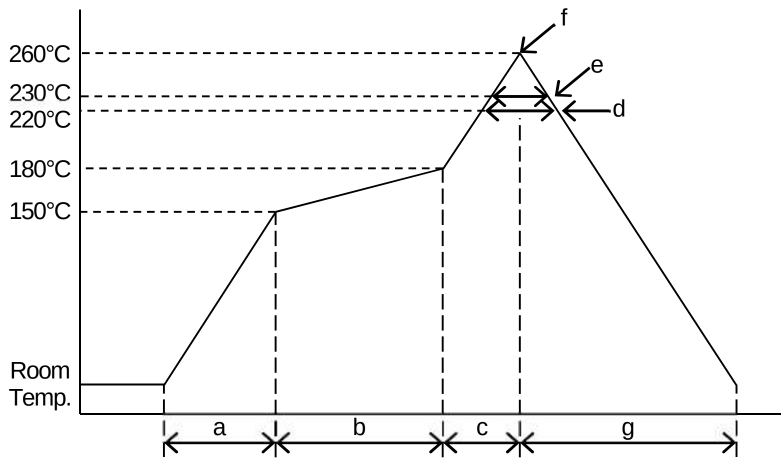
FLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 7°C/s
b	Pre-heating temperature Pre-heating time	80 to 120°C 60 to 120s
c	Peak temperature Peak time	lower than 260°C shorter than 10s
d	Temperature ramping rate	1 to 7°C/s

The temperature indicates at the surface of mold package.

INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature Pre-heating time	150 to 180°C 60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

■ REVISION HISTORY

DATE	REVISION	CHANGES
October 19, 2020	Ver.1.0	Initial release
January 14, 2021	Ver.1.1	Revised lower limit of ESR

[CAUTION]

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6. The products listed in this datasheet may not be appropriate for use in certain equipment where reliability is critical or where the products may be subjected to extreme conditions. You should consult our sales office before using the products in any of the following types of equipment.

   - Aerospace Equipment
   - Equipment Used in the Deep Sea
   - Power Generator Control Equipment (Nuclear, steam, hydraulic, etc.)
   - Life Maintenance Medical Equipment
   - Fire Alarms / Intruder Detectors
   - Vehicle Control Equipment (Airplane, railroad, ship, etc.)
   - Various Safety Devices

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9. The product specifications and descriptions listed in this datasheet are subject to change at any time, without notice.