2.4MHz, 2.5A MOSFET Switching Regulator IC for Buck Converter

■FEATURES

●High Oscillating Frequency	100kHz to 2.4MHz
●High Efficiency at Light Loads	A ver.
●Low Iq at Sleep Mode	Iq=120μA typ. A ver.
●Current Mode Control	
●External Clock Synchronization	
●Wide Operating Voltage Range	3.4V to 40V
●Switching Current	3.6A min.
●PWM Control	
●Maximum Duty Cycle 100%	
●External Compensation Circuit	
●Correspond to Ceramic Capacitor (MLCC)	
●Soft Start Function	2ms typ.
●UVLO (Under Voltage Lockout)	
●Over Current Protection (Hiccup type)	
●Thermal Shutdown Protection	
●Power Good Function	
●Standby Function	
●Package Outline	HSOP8-M1

■APPLICATION

●Consumer Electronics
●Industrial Equipment
●High voltage to logic and microprocessor power supplies

■GENERAL DESCRIPTION

The NJW4171 is a high speed oscillating frequency buck converter with 40V/2.5A MOSFET. It has two lineup: the A version has PWM/PFM mode to ensure high efficiency at light load, the B version is forced PWM mode.

Operating voltage range is wide input range from 3.4V to 40V, it can correspond to supply voltage drop such as cold crank. Moreover, 100% maximum duty cycle contribute to maintain stable output voltage even if supply voltage drops.

The NJW4171 has wide switching oscillating frequency range, 100kHz to 2.4MHz and internal external clock synchronization function. Therefore the NJW4171 can avoid interference with the AM radio frequency.

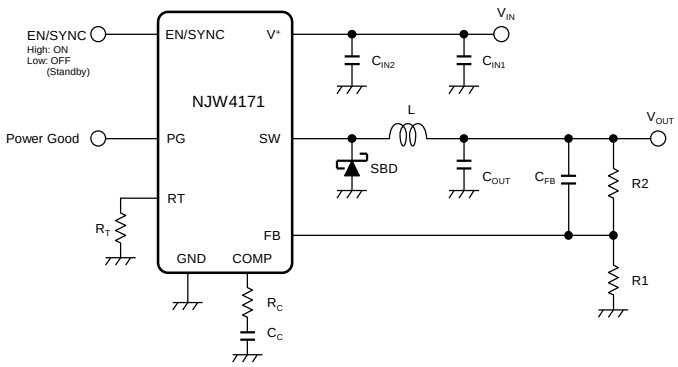
Internal protection functions: UVLO, an over current protection and a thermal shutdown circuit can protect circuit when abnormal condition.

The NJW4171 has wide coverage in consumer electronics and industrial application, because of features that are wide input range, wide switching oscillating frequency range and 100% maximum duty cycle.

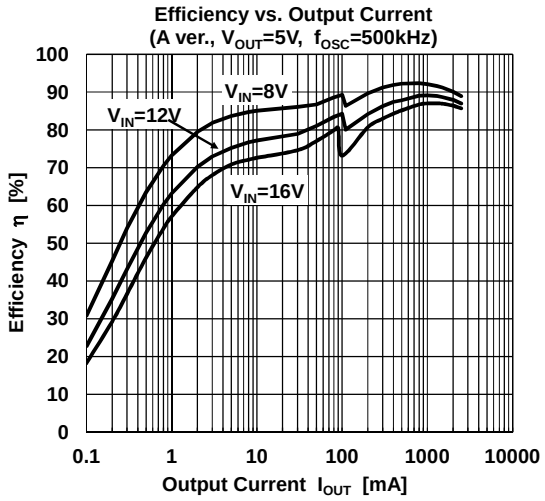
■PRODUCT CLASSOFOCATION

NAME	Ver.	FUNCTION
NJW4171GM1-A	A	With light load mode
NJW4171GM1-B	B	Without light load mode

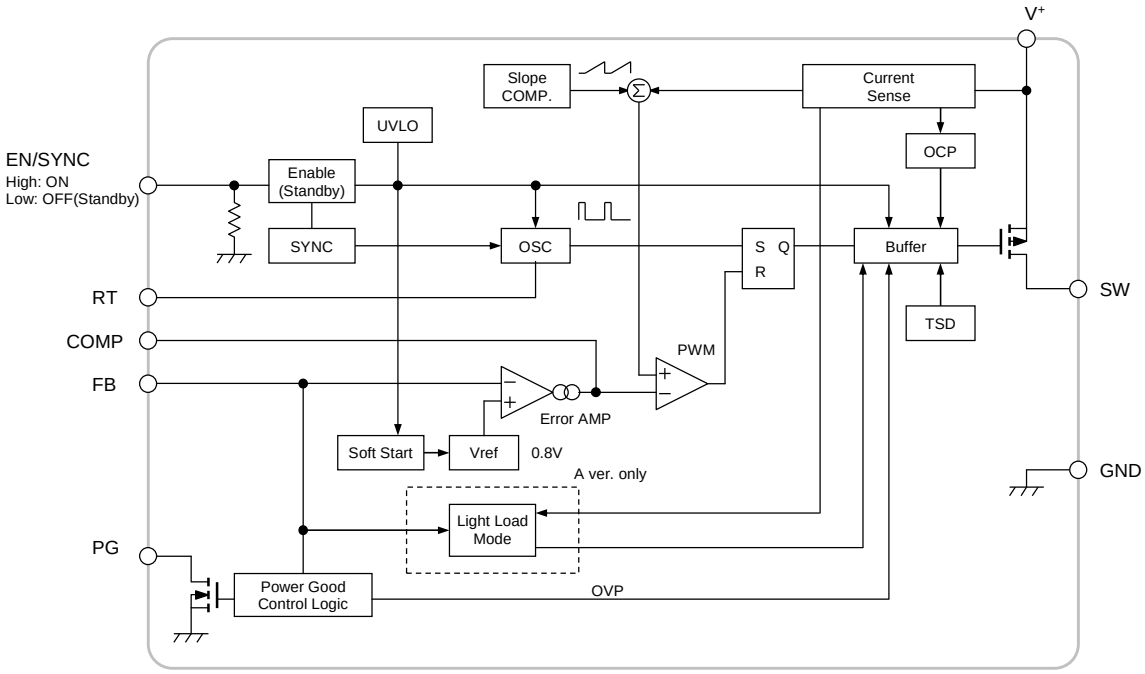
■TYPICAL APPLICATION



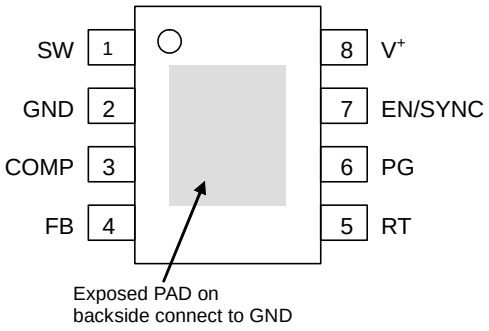
■APPLICATION CHARACTERISTICS



■BLOCK DIAGRAM



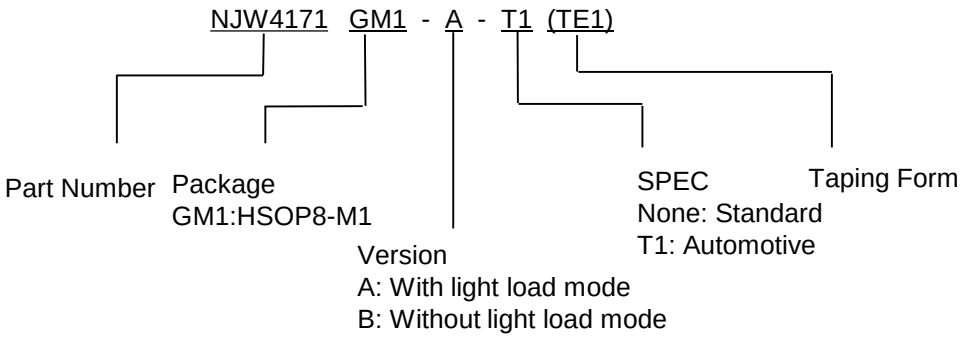
■PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION
1	SW	Switch output
2	GND	Ground
3	COMP	Error Amplifier output
4	FB	Feedback input
5	RT	Oscillating frequency setting
6	PG	Power Good output
7	EN/SYNC	Enable control and external clock synchronization
8	V+	Power supply

Note) Exposed Pad on backside should be connected to ground and soldered to PCB.

■PRODUCT NAME INFORMATION



■ORDERING INFORMATION

PRODUCT NAME	PACKAGE OUTLINE	LIGHT LOAD MODE	AUTO MOTIVE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4171GM1-A (TE1)	HSOP8-M1	yes		yes	yes	Sn100%	4171A	81	3000
NJW4171GM1-A-T1 (TE1)	HSOP8-M1	yes	yes	yes	yes	Sn100%	71AT1	81	3000
NJW4171GM1-B (TE1)	HSOP8-M1			yes	yes	Sn100%	4171B	81	3000
NJW4171GM1-B-T1 (TE1)	HSOP8-M1		yes	yes	yes	Sn100%	71BT1	81	3000

This data sheet are applied to "NJW4171GM1-A" and "NJW4171GM1-B".
Please refer to each data sheet for other versions.

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	-0.3 to +45	V
V^+- SW pin Voltage	V_{V-SW}	+45	V
EN/SYNC pin Voltage	$V_{EN/SYNC}$	-0.3 to +45	V
FB pin Voltage	V_{FB}	-0.3 to +7	V
PG pin Voltage	V_{PG}	-0.3 to +7	V
Power Dissipation(Ta=25°C) HSOP8-M1	P_D	(2-layer / 4-layer) 860(1)/ 2,900(2)	mW
Junction Temperature	T_j	-40 to +150	°C
Operating Temperature	T_{opr}	-40 to +125	°C
Storage Temperature	T_{stg}	-50 to +150	°C

(1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 2Layers)

(2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V^+	3.4 to 40	V
PG pin Voltage	V_{PG}	0 to 5.5	V
Timing Resistor	R_T	2.15 to 78.7	kΩ
Oscillating Frequency	f_{OSC}	100 to 2,400	kHz
External Clock Input	f_{SYNC}	f_{OSC}×0.9 to f_{OSC}×1.7 Maximum 2,800kHz	kHz

■ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V^+=V_{EN./SYNC}$=12V, R_T=6.8kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lockout Block						
ON Threshold Voltage	V_{T_ON}	V^+= L → H	3.1	3.25	3.4	V
OFF Threshold Voltage	V_{T_OFF}	V^+= H → L	3.0	3.15	3.3	V
Hysteresis Voltage	V_{HYS}		70	100	–	mV
Soft Start Block						
Soft Start Time	t_{SS}	V_B=0.75V	1	2	4	ms
Oscillator Block						
Oscillating Frequency 1	f_{OSC1}	R_T=27kΩ	255	300	345	kHz
Oscillating Frequency 2	f_{OSC2}	R_T=6.8kΩ	850	1,000	1,150	kHz
Oscillating Frequency 3	f_{OSC3}	R_T=2.87kΩ	1,860	2,000	2,140	kHz
Error Amplifier Block						
Reference Voltage	V_B		-1.0%	0.8	+1.0%	V
Input Bias Current	I_B		-0.1	–	0.1	μA
Error Amplifire Transconductance	gm		–	450	–	μA/V
Error Amplifire Gain	Av		–	1,000	–	–
Output Source Current	I_{OM+}		52	64	76	μA
Output Sink Current	I_{OM-}		52	64	76	μA
PWM Comparate Block						
Maximum Duty Cycle	$MAXDUTY$	A version V_{FB}=0.3V, B version V_{FB}=0.6V	100	–	–	%
Minimum OFF Time	$t_{OFF-min}$		–	65	105	ns
Minimum ON Time	t_{ON-min}		–	100	140	ns
OCP Block						
COOL DOWN Time	t_{COOL}		–	110	–	ms
Output Block						
Output ON Resistance	R_{ON}	I_{SW}=2.5A	–	0.15	0.3	Ω
Switching Current Limit	I_{LIM}		3.6	4.6	5.5	A
SW Leak Current	I_{LEAK}	$V_{EN/SYNC}$=0V, V^+=40V, V_{SW}=0V	–	–	4	μA

■ELECTRICAL CHARACTERISTICS (CONTINUED)

(Unless otherwise noted, $V^+=V_{EN./SYNC}$=12V, R_T=6.8kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Enable Control / Sync Block						
EN/SYNC pin High Threshold Voltage	$V_{THH\_EN/SYNC}$	$V_{EN/SYNC}$= L → H	1.6	–	V^+	V
EN/SYNC pin Low Threshold Voltage	$V_{THL\_EN/SYNC}$	$V_{EN/SYNC}$= H → L	0	–	0.5	V
EN/SYNC pin Input Bias Current	$I_{EN/SYNC}$	$V_{EN/SYNC}$=12V	–	0.8	1.8	μA
Power Good Block						
High Level Detection Voltage	V_{THH_PG}	Measured at FB pin, Rising	0.848	0.864	0.880	V
Low Level Detection Voltage	V_{THL_PG}	Measured at FB pin, Rising	0.744	0.760	0.776	V
Hysterisis Region	V_{HYS_PG}		–	16	–	mV
Power Good ON Resistance	R_{ON_PG}	I_{PG}=10mA	–	100	150	Ω
Leak Current at OFF State	I_{LEAK_PG}	V_{PG}=5.5V	–	–	0.1	μA
General Characteristics						
Quiescent Current	I_{DD}	A version, R_L=No load, Not Switching	–	120	150	μA
		B version, R_L=No load, Not Switching	–	2.2	2.7	mA
Standby Current	I_{DD_STB}	$V_{EN/SYNC}$=0V	–	–	3	μA

■THERMAL CHARACTERISTICS

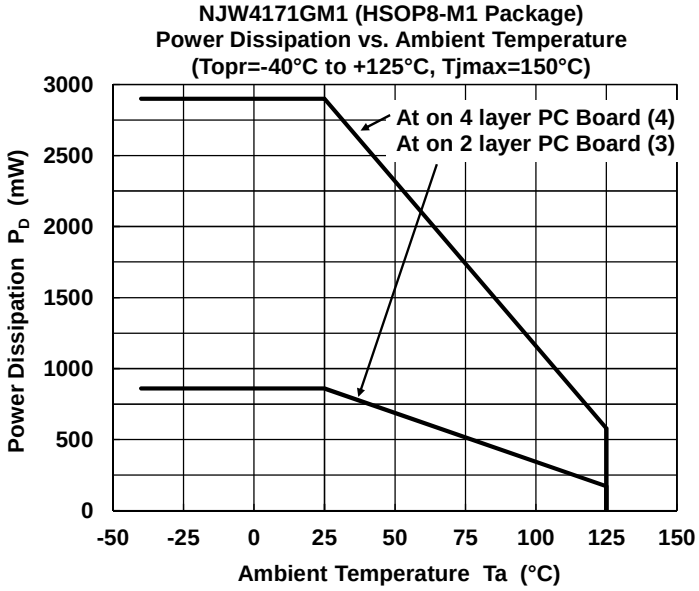
PARAMETER	SYMBOL	VALUE		UNIT
Junction-to-ambient thermal resistance	θja	HSOP8-M1	145(3) 43(4)	°C/W
Junction-to-Top of package characterization parameter	ψjt	HSOP8-M1	22(3) 6.3(4)	°C/W

(3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 2Layers)

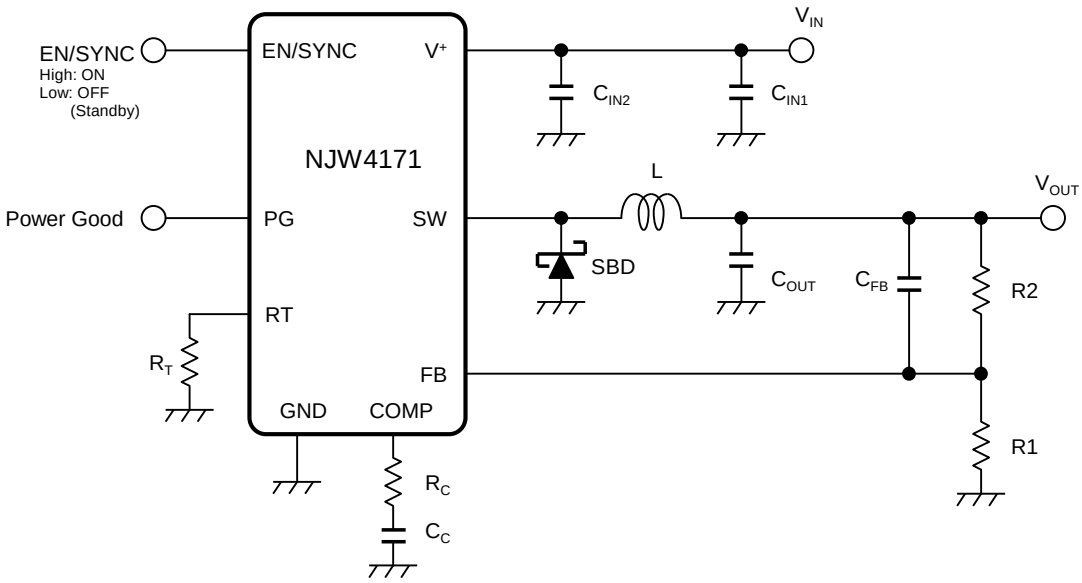
(4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JEDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■POWER DISSIPATION vs. AMBIENT TEMPERATURE

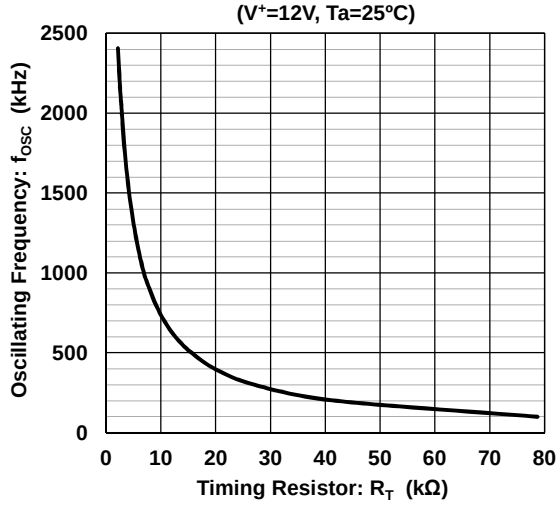


■TYPICAL APPLICATION

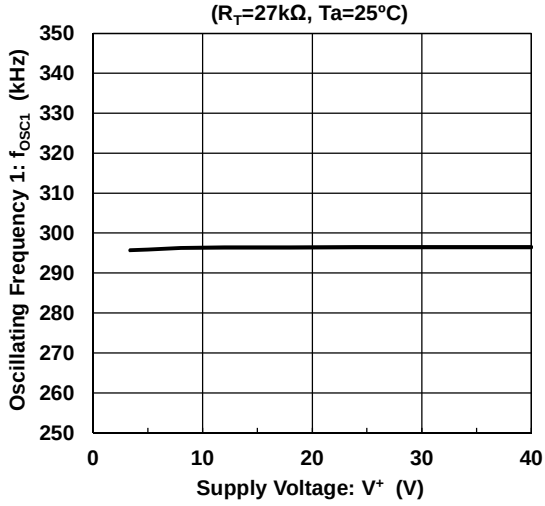


■TYPICAL CHARACTERISTICS

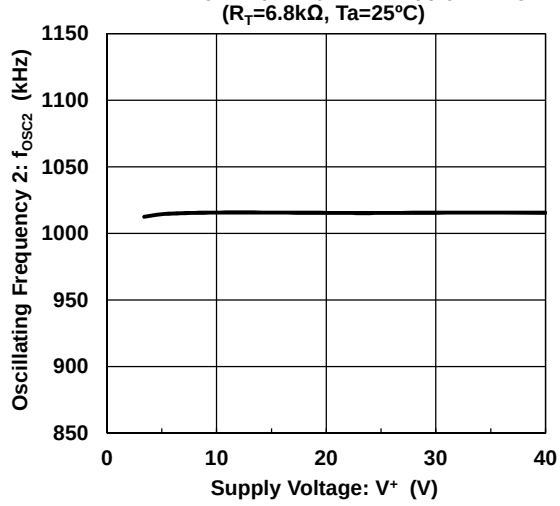
Timing Resistor vs. Oscillating Frequency
(V^+=12V, Ta=25°C)



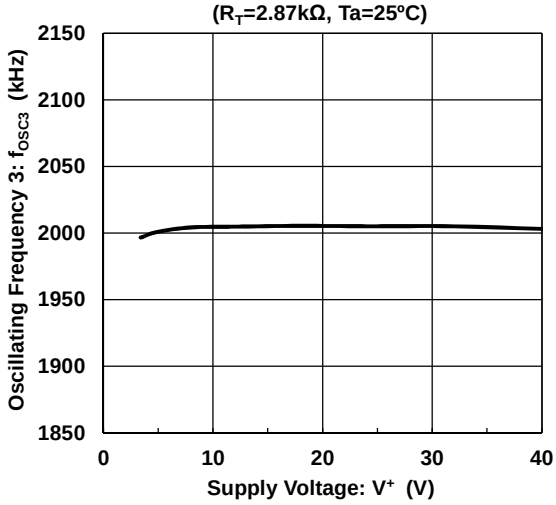
Oscillating Frequency 1 vs. Supply Voltage
(R_T=27kΩ, Ta=25°C)



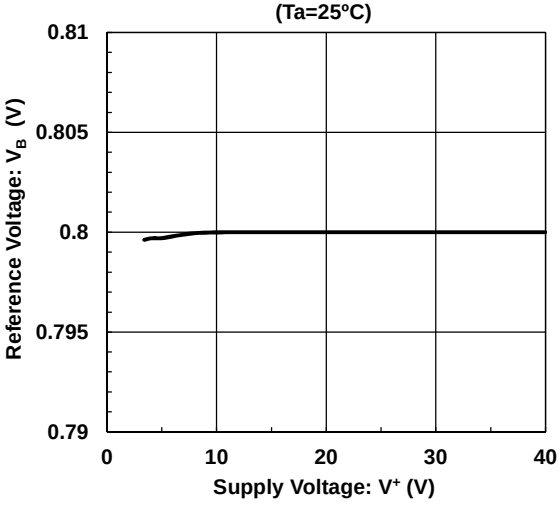
Oscillating Frequency 2 vs. Supply Voltage
(R_T=6.8kΩ, Ta=25°C)



Oscillating Frequency 3 vs. Supply Voltage
(R_T=2.87kΩ, Ta=25°C)

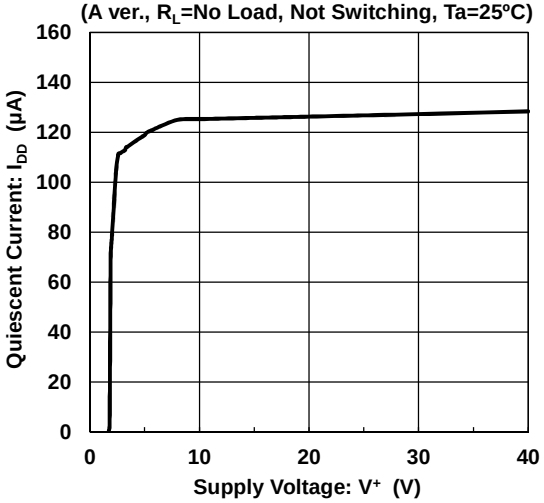


Reference Voltage vs. Supply Voltage
(Ta=25°C)

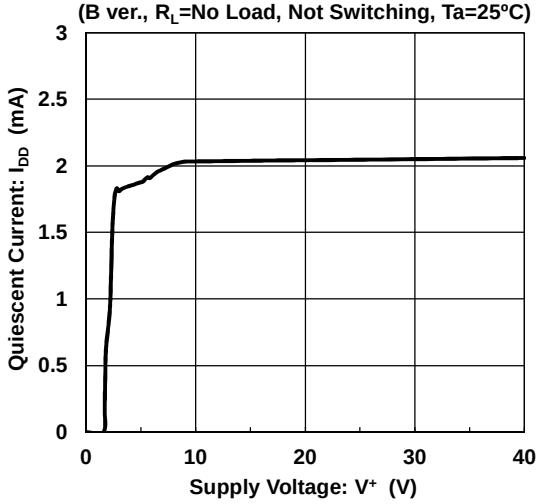


■ TYPICAL CHARACTERISTICS

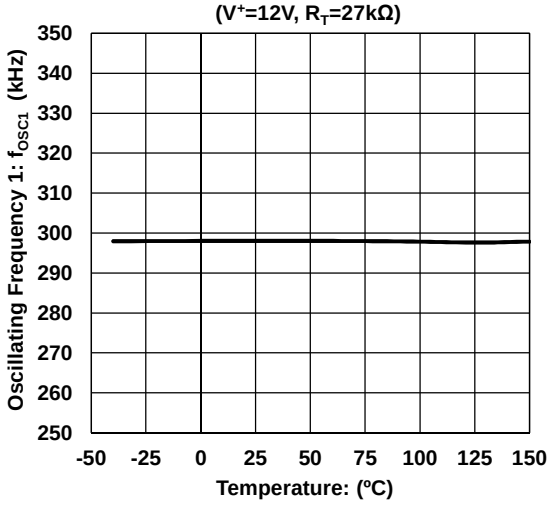
Quiescent Current vs. Supply Voltage
(A ver., R_L=No Load, Not Switching, Ta=25ºC)



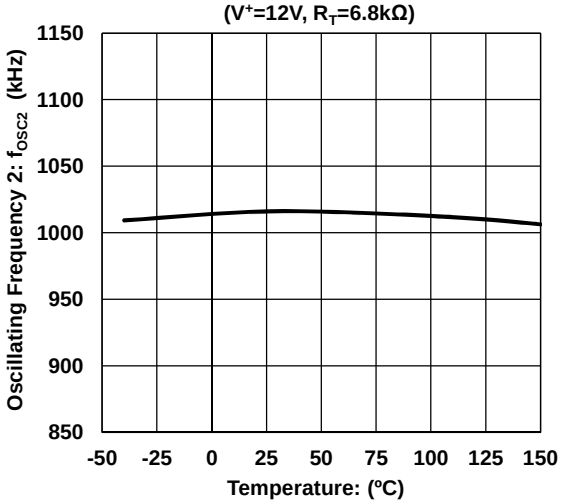
Quiescent Current vs. Supply Voltage
(B ver., R_L=No Load, Not Switching, Ta=25ºC)



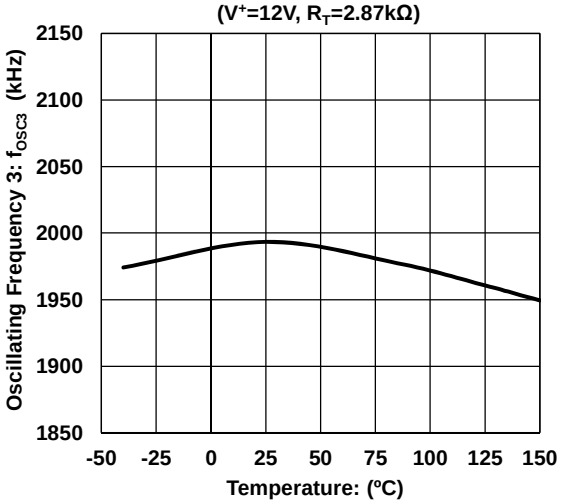
Oscillating Frequency 1 vs Temperature
(V^+=12V, R_T=27kΩ)



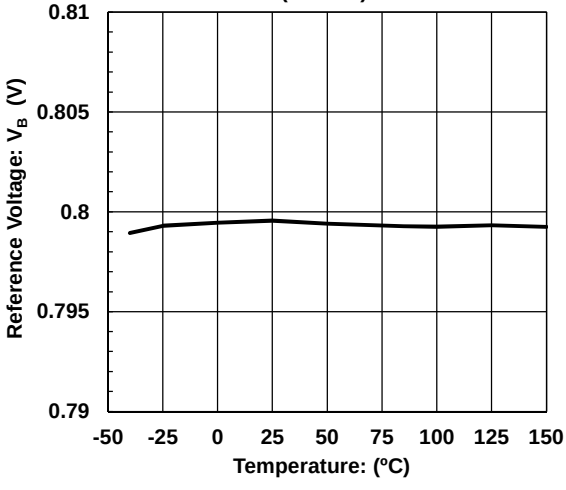
Oscillating Frequency 2 vs Temperature
(V^+=12V, R_T=6.8kΩ)



Oscillating Frequency 3 vs Temperature
(V^+=12V, R_T=2.87kΩ)

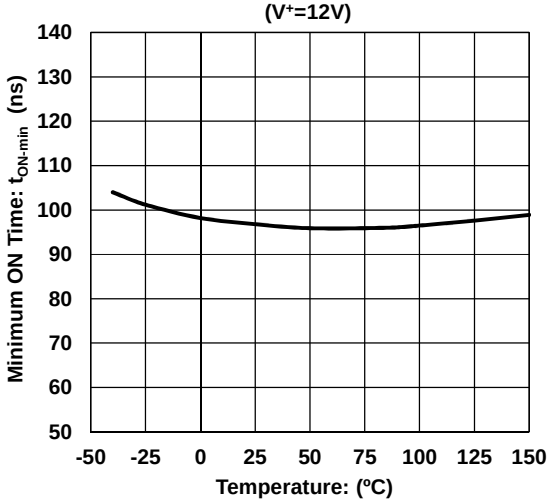


Reference Voltage vs. Temperature
(V^+=12V)

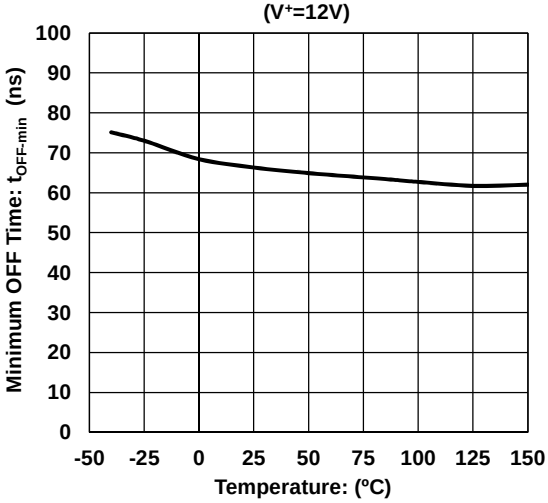


■ TYPICAL CHARACTERISTICS

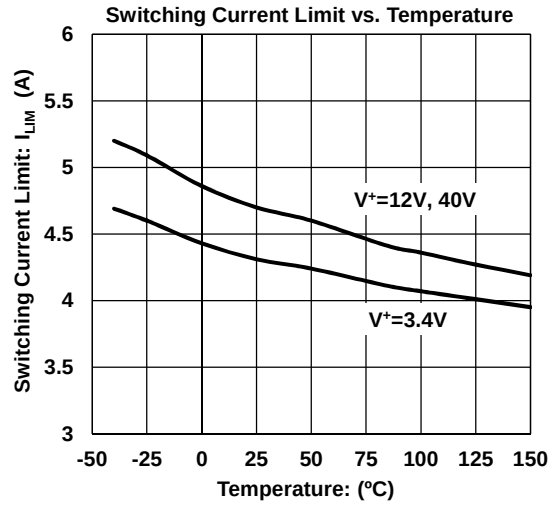
Minimum ON Time vs. Temperature
(V^+=12V)



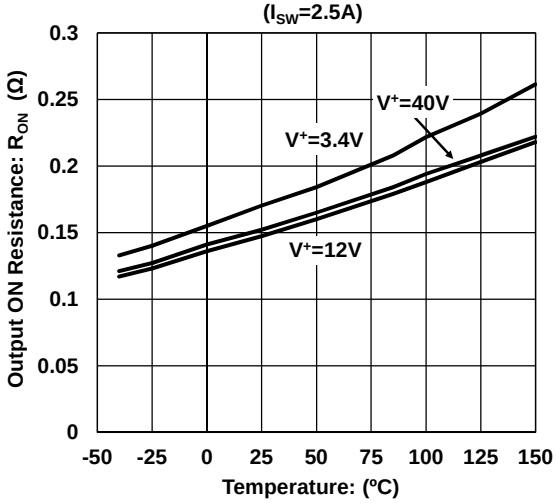
Minimum OFF Time vs. Temperature
(V^+=12V)



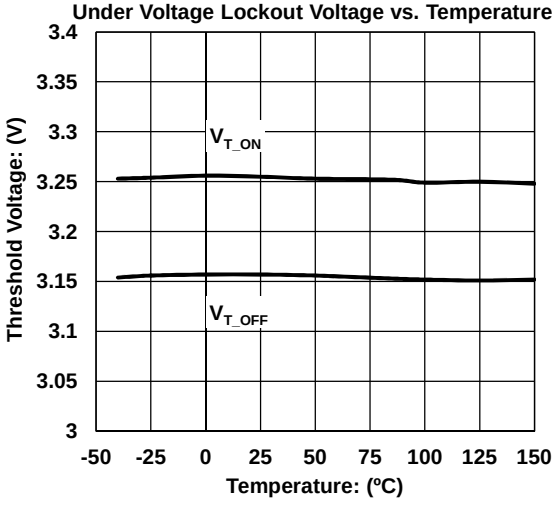
Switching Current Limit vs. Temperature



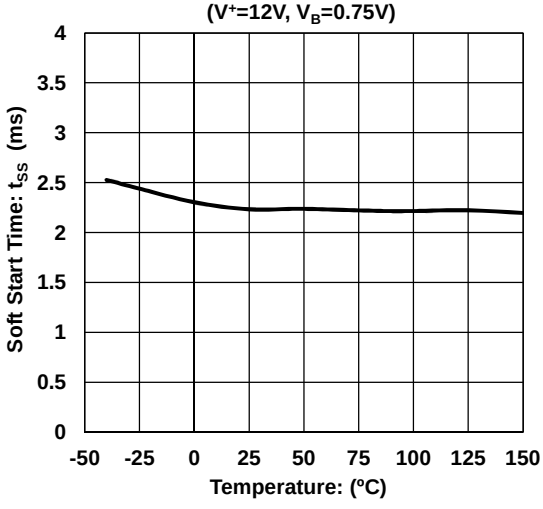
Output ON Resistance vs. Temperature
(I_{SW}=2.5A)



Under Voltage Lockout Voltage vs. Temperature

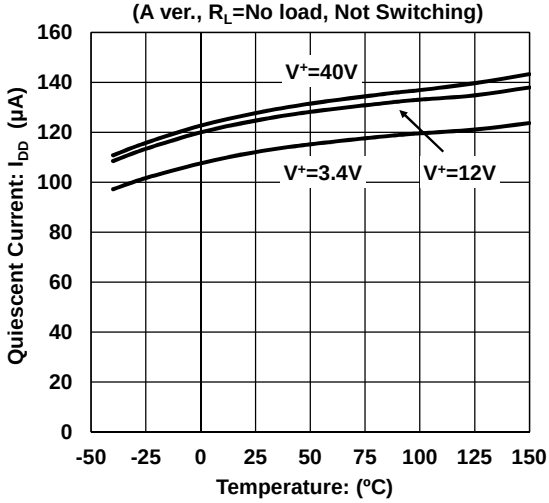


Soft Start Time vs. Temperature
(V^+=12V, V_B=0.75V)

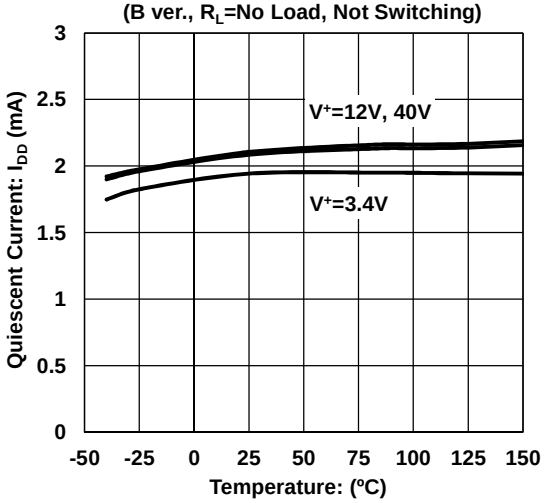


■ TYPICAL CHARACTERISTICS

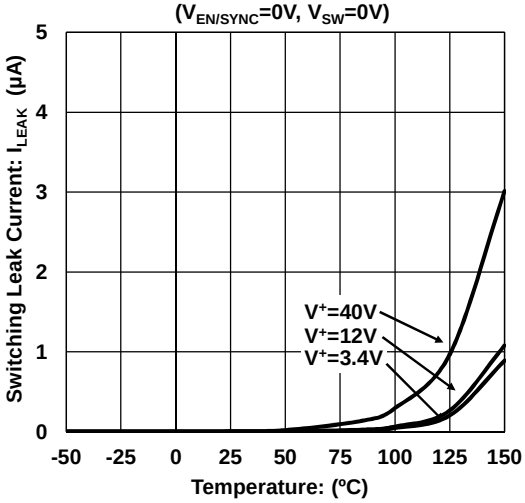
Quiescent Current vs. Temperature
(A ver., R_L=No load, Not Switching)



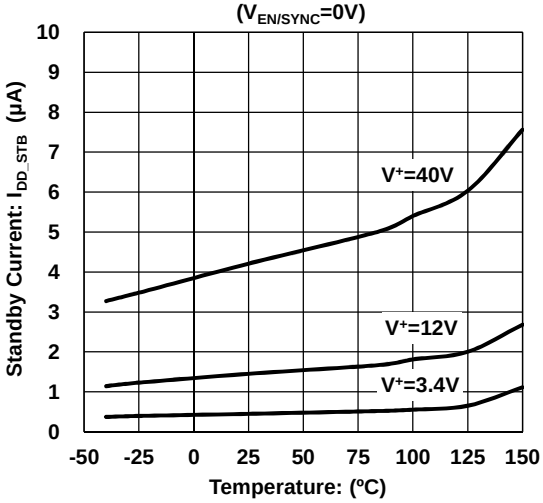
Quiescent Current vs. Temperature
(B ver., R_L=No Load, Not Switching)



Switching Leak Current vs. Temperature
($V_{EN/SYNC}$=0V, V_{SW}=0V)



Standby Current vs. Temperature
($V_{EN/SYNC}$=0V)



■ **PIN DESCRIPTIONS**

PIN NAME	PIN NUMBER	FUNCTION
SW	1	Switch Output pin of Power MOSFET
GND	2	GND pin
COMP	3	Output pin of the Error Amplifier. A resistor and capacitors for compensation are connected between the COMP pin and the GND.
FB	4	Output Voltage Detecting pin Connects output voltage through the resistor divider tap to this pin in order to voltage of the FB pin become 0.8V.
RT	5	Oscillating Frequency Setting pin by Timing Resistor. Oscillating Frequency should set between 100kHz and 2.4MHz.
PG	6	Power Good pin. An open drain output that goes high impedance when the FB pin voltage is stable around +8% to -5%.
EN/SYNC	7	Standby Control pin The EN/SYNC pin internally pulls down resistor. Normal Operation at the time of High Level. Standby Mode at the time of Low Level or OPEN. Moreover, it operates by inputting clock signal at the oscillatory frequency that synchronized with the input signal.
V^+	8	Power Supply pin for Power Line Insert a bypass capacitor close to the V^+ pin – the GND pin connection in order to lower high frequency impedance.
Exposed PAD	–	Exposed PAD on backside should be connected to ground and soldered to PCB.

■ Description of Block Features

1. Description of Light Load Mode

NJW4171 A version have a light load mode to give efficiency in the light load. When a output current decreases, NJW4171 switches over from PWM mode to PFM mode automatically. The IC becomes the sleep state then, and the quiescent current of the IC decreases to 120μA typ.. Therefore NJW4171 can minimize an input current of the application.

If the peaks of the switch current become less than about 200mA typ., NJW4171 is switched by a light load mode.

In the light load mode, the ripple voltage becomes slightly larger than in the normal operation because the oscillating frequency becomes lower due to the PFM operation. Fig. 1. shows operation waveform of the light load mode.

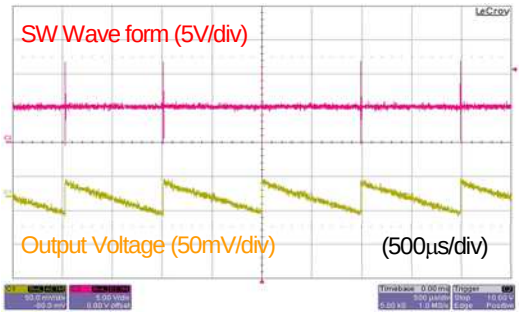
Increasing the inductor L-value improves the efficiency at light load because the switching shut down time is extended.

It optimizes efficiency at light load to minimizing the leak current of the output voltage setting resistor and the leak current of the catch diode.

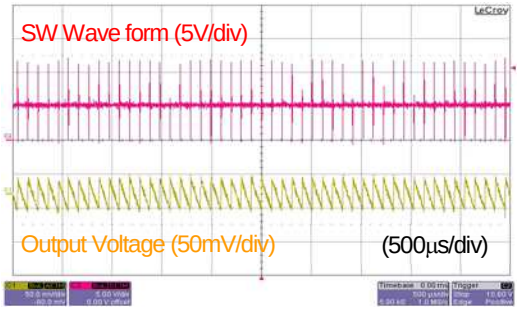
Light load mode of NJW4171 can be used by setting the EN/SYNC pin to high level.

During external synchronous operation, the light load mode is disabled and operates at the input clock frequency.

When the CLK signal is input to the EN/SYNC pin at operate in light load mode, it switches from light load mode to normal operation mode.



a) Waveform of I_{OUT}=1mA



b) Waveform of I_{OUT}=10mA

Fig. 1.
Operation waveform of the Light Load Mode

The NJW 4171 B version is not in light load mode.
Changes in the switching frequency at light load operation will affect the ripple frequency. You should use the B version for load sensitive to ripple noise.

■ **Description of Block Features (Continued)**

2. Basic Functions / Features

● Error Amplifier Section (Error AMP)

0.8V±1% precise reference voltage is connected to the non-inverted input of this section.

To set the output voltage, connects converter's output to inverted input of this section (FB pin). If requires output voltage over 0.8V, inserts resistor divider.

This AMP section has high gain and external compensation pin (COMP pin). It is easy to insert a resistor and a capacitor between the COMP pin and the GND, making possible to set optimum loop compensation for each type of application.

● PWM Comparator Section (PWM), Oscillating Circuit Section (OSC)

Oscillating frequency can be set by inserting resistor between the RT pin and GND. Table. 1. shows example of oscillating frequency and timing resistor. The resistance supports a series of E24 and a series of E96.

Referring to the sample characteristics in "Timing Resistor and Oscillating Frequency", set oscillation between 100kHz and 2.4MHz.

Table 1. NJW4171 oscillating frequency and timing resistor

Oscillating Frequency (MHz)	Timing Resistor (kΩ)	Oscillating Frequency (MHz)	Timing Resistor (kΩ)
0.1	78.7	1.2	5.6
0.2	41.2	1.4	4.53
0.3	27	1.6	3.83
0.4	20	1.8	3.3
0.5	15.4	2.0	2.87
0.6	12.7	2.1	2.67
0.7	10.7	2.2	2.49
0.8	9.1	2.3	2.32
0.9	7.87	2.4	2.15
1.0	6.8		

The PWM signal is output by feedback of output voltage and slope compensation switching current at the PWM comparator block. The NJW4171 can operate with low saturation so that maximum duty is 100%.

NJW4171 is limited in minimum ON time $t_{ON\text{-}min}$=100ns typ. and minimum OFF time t_{OFF}-min=65ns typ.

When you design the application, please refer to "Application information - Setting of the oscillating frequency".

● Power MOSFET (SW Output Section)

The power is stored in the inductor by the switch operation of built-in power MOSFET. The output current is limited to 3.6A(min.) the overcurrent protection function. In case of step-down converter, the forward direction bias voltage is generated with inductance current that flows into the external regenerative diode when MOSFET is turned off.

The SW pin allows voltage between the V^+ pin and the SW pin up to +45V. However, you should use an Schottky diode that has low saturation voltage.

● Power Supply, GND pin (V^+ and GND)

In line with switching element drive, current flows into the IC according to frequency. If the power supply impedance provided to the power supply circuit is high, it will not be possible to take advantage of IC performance due to input voltage fluctuation. Therefore insert a bypass capacitor close to the V^+ pin – the GND pin connection in order to lower high frequency impedance.

■ **Description of Block Features (Continued)**

3. Additional and Protection Functions / Features

● Under Voltage Lockout (UVLO)

The UVLO circuit operating is released above V^+=3.25V(typ.) and IC operation starts. When power supply voltage is low, IC does not operate because the UVLO circuit operates. There is 100mV(typ.) width hysteresis voltage at rise and decay of power supply voltage. Hysteresis prevents the malfunction at the time of UVLO operating and releasing.

● Soft Start Function (Soft Start)

The output voltage of the converter gradually rises to a set value by the soft start function. The soft start time is 2ms (typ.). It is defined with the time of the error amplifier reference voltage becoming from 0V to 0.75V. The soft start circuit operates after the release UVLO and/or recovery from thermal shutdown.

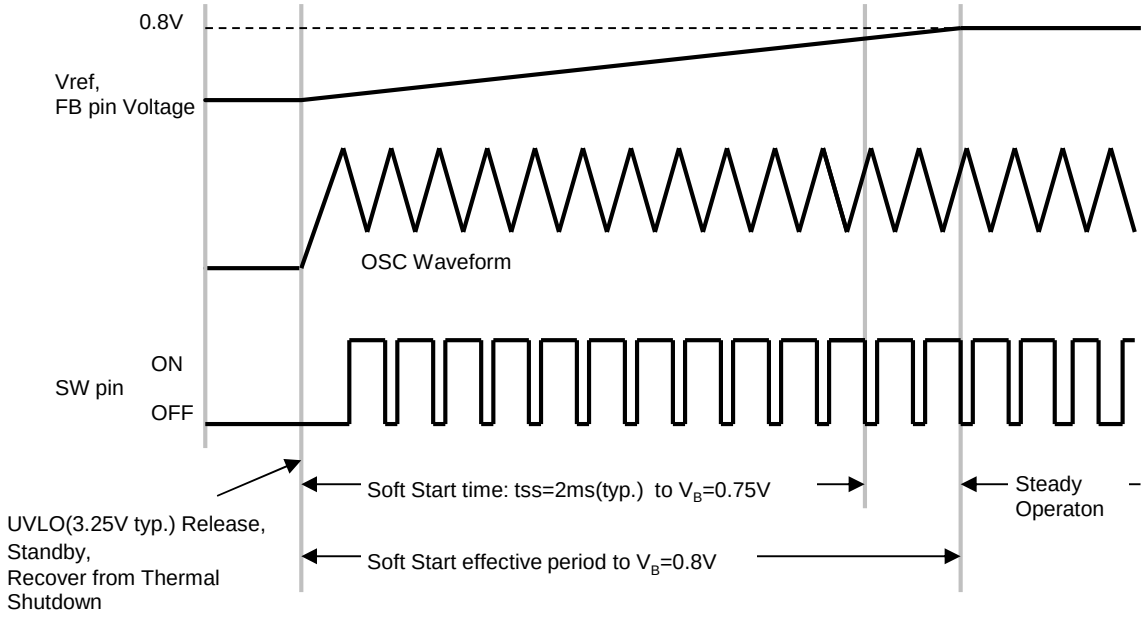


Fig. 2. Startup Timing Chart

■ **Description of Block Features (Continued)**

● Over Current Protection Circuit (OCP)

NJW4171 contains overcurrent protection circuit of hiccup architecture. The overcurrent protection circuit of hiccup architecture is able to decrease heat generation at the overload.

The NJW4171 output returns automatically along with release from the over current condition.
At when the switching current becomes I_{LIM} or more, the overcurrent protection circuit is stopped the MOSFET output. The switching output holds low level down to next pulse output at OCP operating.

When FB pin voltage becomes 0.5V or less, the switching operation stops after the overcurrent detection continued 128 pulses.

After NJW4171 switching operation was stopped, it restarts by soft start function after the cool down time of approx 110ms (typ.).

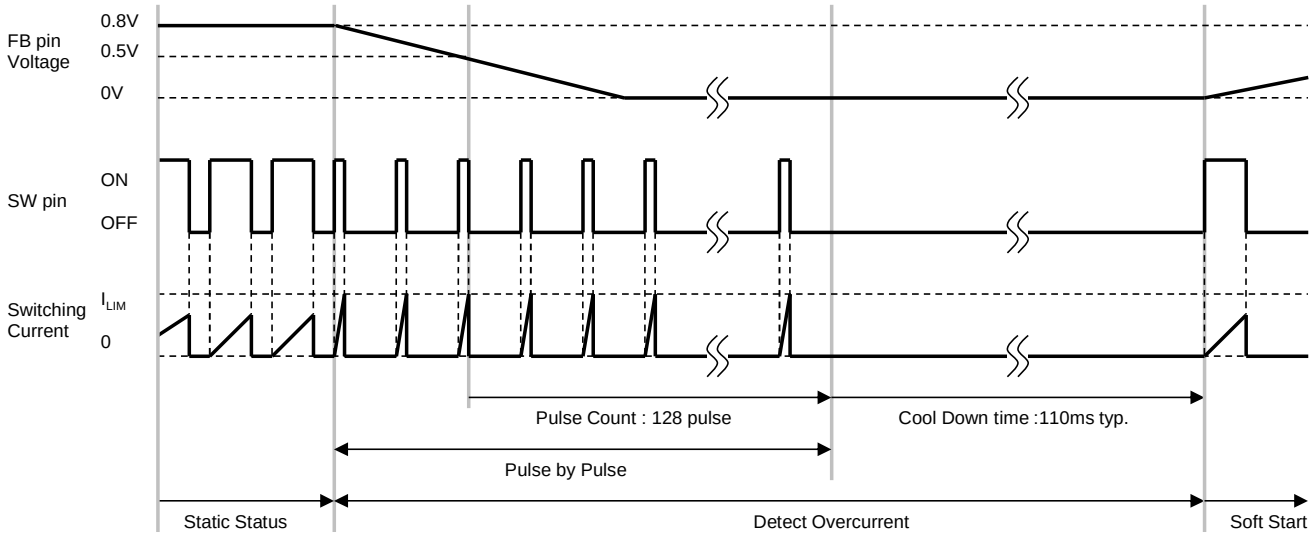


Fig. 2. Timing Chart at Over Current Detection

● Thermal Shutdown Function (TSD)

When Junction temperature of the NJW4171 exceeds the 165°C*, internal thermal shutdown circuit function stops SW function. When junction temperature decreases to 145°C* or less, SW operation returns with soft start operation.

The purpose of this function is to prevent malfunctioning of IC at the high junction temperature. Therefore it is not something that urges positive use. You should make sure to operate within the junction temperature range rated (150°C). (* Design value)

● Standby Function

The NJW4171 stops the operating and becomes standby status when the EN/SYNC pin becomes less than 0.5V.

The EN/SYNC pin internally pulls down resistor, therefore the NJW4171 becomes standby mode when the EN/SYNC pin is OPEN. You should connect this pin to V^+ when you do not use standby function.

■ **Description of Block Features (Continued)**

● External Clock Synchronization

By inputting a square wave to EN/SYNC pin, can be synchronized to an external frequency.
You should fulfill the following specification about a square wave. (Table 2.)

Table 2. The input square wave to an EN/SYNC pin.

	Condition
Input Frequency	f_{OSC}×0.9 to f_{OSC}×1.7 2,800kHz Maximum
Duty Cycle	40% to 60%
Voltage magnitude	1.6V or more at High level 0.5V or less at Low level

The trigger of the switching operating at the external synchronized mode is detected to the rising edge of the input signal. At the time of switching operation from standby or asynchronous to synchronous operation, it has set a delay time approx 20μs to 30μs in order to prevent malfunctions. (Fig. 4.)

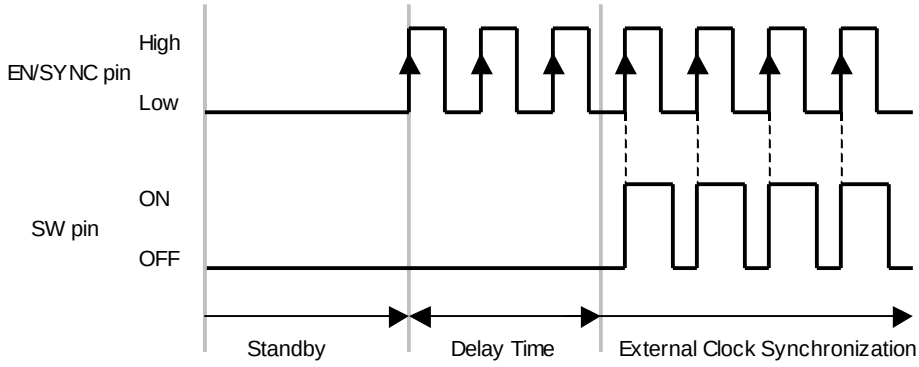


Fig. 4. Switching Operation by External Synchronized Clock

● Power Good Function, Over Voltage Protection

It monitors the output status and outputs a signal from PG pin that internally connected to open drain MOSFET.
The Power Good pin goes high impedance when the FB pin voltage is stable around 0.760V to 0.864V(typ.).
A low on the pin indicates that the FB pin voltage is out of the setting voltage.
To prevent malfunction of the Power Good output, it has hysterisis 16mV(typ.) and the delay time approx 20μs to 30μs against the FB pin voltage changes.

The High level detection of Power Good includes an overvoltage protection.
When FB pin voltages exceed the high level detection voltage by abnormality of the application, NJW4171 turns off power MOSFET by priority.

■ Application Information

● Oscillating Frequency Setting

When the switching regulator high oscillating frequency, the application can use a small inductor and capacitor. If oscillating frequency is high, consider that you are subject to efficiency reduction of the application and a limit of the minimum ON time.

NJW4171 is set in $t_{ON\text{-}min}$ 100ns typ. at the minimum ON time. As for the ON time for buck converter application, set oscillating frequency to become more than 100ns typ.

The buck converter of ON time is decided the following formula.

$$ton = \frac{V_{OUT}}{V_{IN} \times f_{OSC}} [s]$$

V_{IN} shows input voltage and V_{OUT} shows output voltage.

When the ON time becomes below in 100ns typ., in order to maintain output voltage at a stable state, change of duty or pulse skip operation may be performed.

● Inductors

Because a large current flows to the inductor, you should select the inductor with the large current capacity not to saturate. Design the inductor ripple current ΔI_L in approx. 20% to 40% of the output current.

Reducing L decreases the value of the inductor. However a peak current increases and adversely affects the efficiency. (Fig. 5.)

Moreover, you should be aware that the output current is limited because it becomes easy to operating to the overcurrent limit.

The peak current is decided the following formula.

$$\Delta I_L = 0.2 \text{ to } 0.4 \times I_{OUT} [A]$$

$$L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f_{OSC}} [H]$$

$$Ipk = I_{OUT} + \frac{\Delta I_L}{2} [A]$$

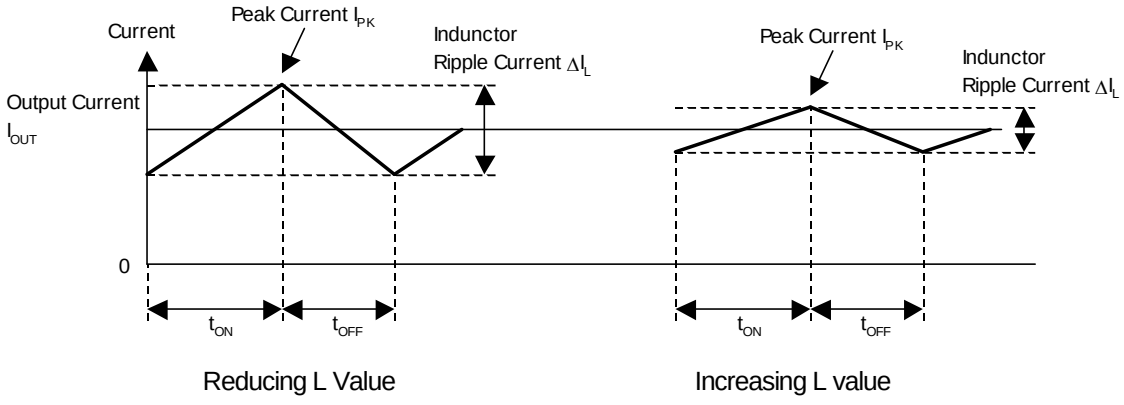


Fig. 5. Inductor Current State Transition (Continuous Conduction Mode)

■ **Application Information(Continued)**

In most case, a suitable inductor L-value is fixed by oscillating frequency. The Inductor setting example is shown in Table 3.

Table 3. Inductor Setting Example

Oscillating Frequency [MHz]	Inductor L [μH]	Part Number
0.1	47 (22 to 100)	CLF12577NIT (TDK)
0.3	15 (6.8 to 33)	CLF10060NIT (TDK)
0.5	10 (4.7 to 22)	CLF7045NIT (TDK)
1	4.7 (2.2 to 10)	CLF6045NIT (TDK)
1.5	3.3 (1.8 to 6.8)	CLF6045NIT (TDK)
2.1	2.2 (1 to 4.7)	CLF5030NIT (TDK)
2.4	1.5 (0.8 to 3.3)	CLF5030NIT (TDK)

Inductor L-value is a theoretical value. The optimum value varies according such factors as application specifications and components. Fine-tuning should be done on the actual device.

● Input Capacitor

Transient current flows into the input section of a switching regulator responsive to frequency. If the power supply impedance provided to the power supply circuit is large, it will not be possible to take advantage of the NJW4171 performance due to input voltage fluctuation. Therefore insert an input capacitor as close to the MOSFET as possible. A ceramic capacitor is the optimal for input capacitor.

The effective input current can be expressed by the following formula.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} [A]$$

In the above formula, the maximum current is obtained when $V_{IN} = 2 \times V_{OUT}$, and the result in this case is $I_{RMS} = I_{OUT\,(MAX)} \div 2$.

When selecting the input capacitor, carry out an evaluation based on the application, and use a capacitor that has adequate margin.

■ **Application Information(Continued)**

● Output Capacitor

An output capacitor stores power from the inductor, and stabilizes voltage provided to the output. Because NJW4171 corresponds to the output capacitor of low ESR, the ceramic capacitor is the optimal for compensation.

In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

The output capacitor is decided in reference to follows.

$$C_{OUT} = \frac{100}{V_{OUT} \times f_{OSC}} \times 10^6 \ [\mu F]$$

Therefore when selecting a capacitors, you should confirm the characteristics with supplier datasheets.

When selecting an output capacitor, you must consider Equivalent Series Resistance (ESR) characteristics, ripple current, and breakdown voltage.

The output ripple noise can be expressed by the following formula.

$$V_{ripple(p-p)} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}} \right) [V]$$

The effective ripple current that flows in a capacitor (I_{rms}) is obtained by the following equation.

$$I_{rms} = \frac{\Delta I_L}{2\sqrt{3}} \ [Arms]$$

● Catch Diode

When the switch element is in OFF cycle, power stored in the inductor flows via the catch diode to the output capacitor. Therefore during each cycle current flows to the diode in response to load current. Because diode's forward saturation voltage and current accumulation cause power loss, a Schottky Barrier Diode (SBD), which has a low forward saturation voltage, is ideal.

When select the SBD, the reverse current at the high temperature is important, too.

The characteristic of SBD has a high reverse current than a general diode. If the reverse current is large, it leads to the loss of the diode, so check the specification of the SBD.

● Setting Output Voltage, Compensation Capacitor

The output voltage V_{OUT} is determined by the relative resistances of R1, R2.

Because leak current increase if a resistor value is low, the efficiency in the light load is affected.

When use the A version of the light load function, you should increase resistance to improve a loss with the light load.

$$V_{OUT} = \left(\frac{R2}{R1} + 1 \right) \times V_B \ [V]$$

■ **Application Information (Continued)**

● Compensation design example

A switching regulator requires a feedback circuit for acquiring a stable output. Because the frequency characteristics of the application change according to the inductance, output capacitor, and so on, the compensation constant should ideally be determined in such a way that the maximum band is acquired while the necessary phase for stable operation is maintained.

These compensation constants play an important role in the adjustment of the NJW4171 when mounted in an actual unit. Finally, select the constants while performing measurement, in consideration of the application specifications.

Feedback and Stability

Basically, the feedback loop should be designed in such a way that the open loop phase shift at the point where the loop gain is 0 dB is less than -180°. It is also important that the loop characteristics have margin in consideration of ringing and immunity to oscillation during load fluctuations. With the NJW4171, the feedback circuit can be freely designed, enabling the arrangement of the poles and zeros which is important for loop compensation, to be optimized.

The characteristics of the poles and zeros are shown in Fig. 6.

Poles: The gain has a slope of -20 dB/dec, and the phase shifts -90°.

Zeros: The gain has a slope of +20 dB/dec, and the phase shift +90°.

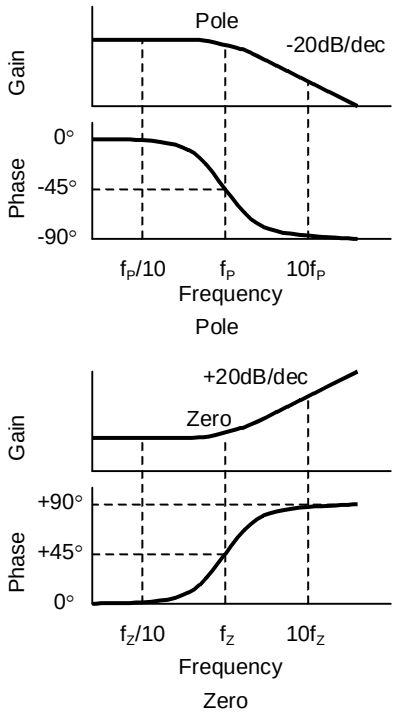


Fig. 6.
Characteristics of Pole and Zero

If the number of factors constituting poles is defined as “n”, the change in the gain and phase will be “n”-fold. This also applies to zeros as well. The poles and zeros are in a reciprocal relationship, so if there is one factor for each pole and zero, they will cancel each other.

Pole and Zero Settings

The position of the poles and zeros are decided by the setting of an application and the error amplifier.

Fig. 9. shows compensation circuit. Table 4. shows setting of poles and zeros.

■ **Application Information (Continued)**

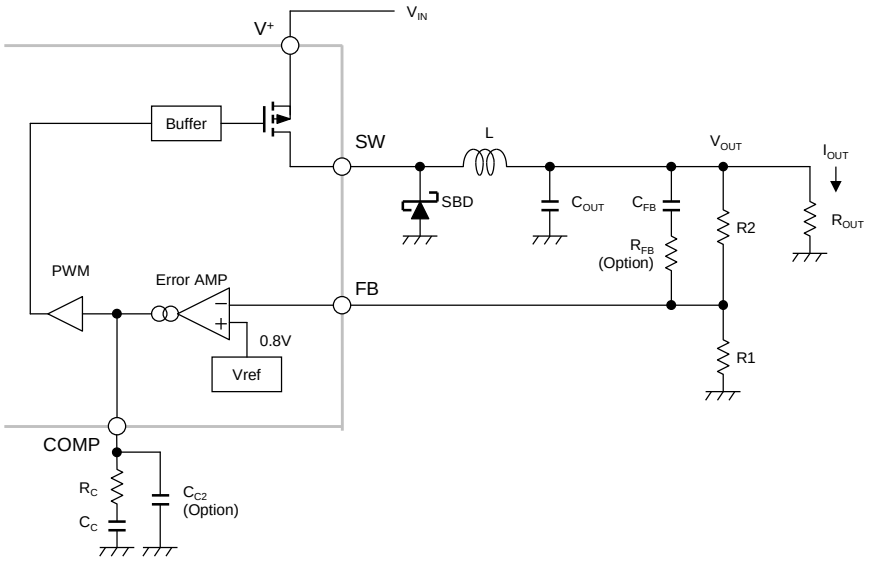


Fig. 7. Compensation Circuit Configuration

Table 4. Setting of Poles and Zeros

Symbol	Calculating formula	Setting example	Description
f_{P1}	$f_{P1} = \frac{1}{2 \times \pi \times \frac{A_V}{gm} \times C_C}$ (ex. 71.7Hz)	$\frac{f_{OSC}}{20000} < f_{P1} < \frac{f_{OSC}}{5000}$	A position of 1st pole f_{P1} is fixed by C_C connected to the output of the error amplifier.
f_{POUT}	$f_{POUT} = \frac{1}{2 \times \pi \times \frac{V_{OUT}}{I_{OUT}} \times C_{OUT}}$ (ex. 2.4kHz)	$3.5 < \frac{f_{Z1}}{f_{POUT}} < 12$ (ex. 8.8)	The pole f_{POUT} is caused by capacitor and load resistance connected to the output. In this case, the load resistance assumes a maximum load current and calculates. When it uses a ceramic capacitor for C_{OUT}, it is realistic to calculate at effective capacitance in consideration of DC bias.
f_{Z1}	$f_{Z1} = \frac{1}{2 \times \pi \times R_C \times C_C}$ (ex. 21.2kHz)		A position of zero f_{Z1} is fixed by R_C and C_C connected to the output of the error amplifier.
f_{Z2}	$f_{Z2} = \frac{1}{2 \times \pi \times R2 \times C_{FB}}$	20kHz to 80kHz (ex. 38.8kHz)	The Zero f_{Z2} is caused by R2 and C_{FB}. The f_{Z2} compensates it for a phase shift of f_{P2}.
f_{P2}	–	About 50kHz	The 2nd pole of the error amplifier is set to about 50kHz.

Note) The specifications example is based on application circuit P.27.

Above several 100 kHz, various poles are generated, so the upper limit of the frequency range where the loop gain is 0 dB is set to fifth (1/5) to tenth (1/10) of oscillating frequency.

When high oscillating frequency, control a loop gain to about 100kHz to get enough phase margins.

In addition, please tuning R_{FB} and C_{C2} when circuit is unstable in the high frequency area of the loop gain.

■ **Application Information (Continued)**

● Board Layout

In the switching regulator application, because the current flow corresponds to the oscillating frequency, the substrate (PCB) layout becomes an important.

You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible. Fig.8. shows a current loop at step-down converter. Especially, should lay out high priority the loop of C_{IN}-SW-SBD that occurs rapid current change in the switching. It is effective in reducing noise spikes caused by parasitic inductance.

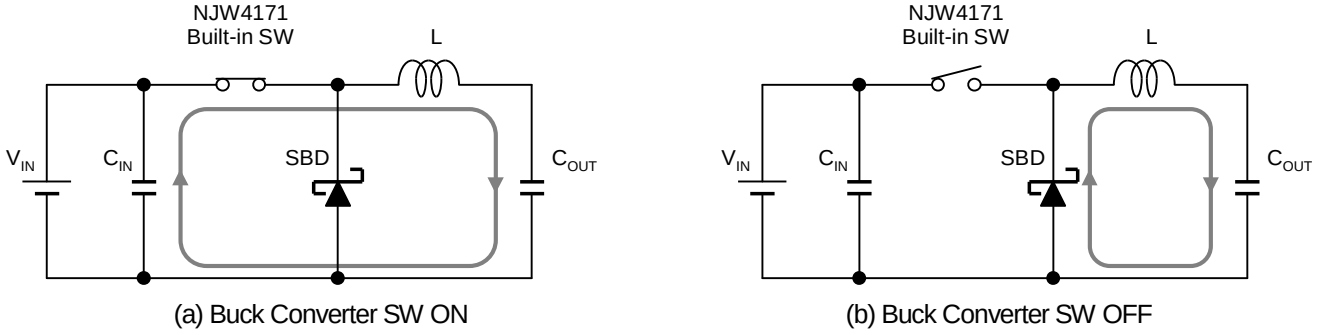


Fig. 8. Current Loop at Buck Converter

Concerning the GND line, it is preferred to separate the power system and the signal system, and use single ground point.

The voltage sensing feedback line should be as far away as possible from the inductance. Because this line has high impedance, it is laid out to avoid the influence noise caused by flux leaked from the inductance.

Fig. 9. shows example of wiring at buck converter. Fig. 10. shows the PCB layout example.

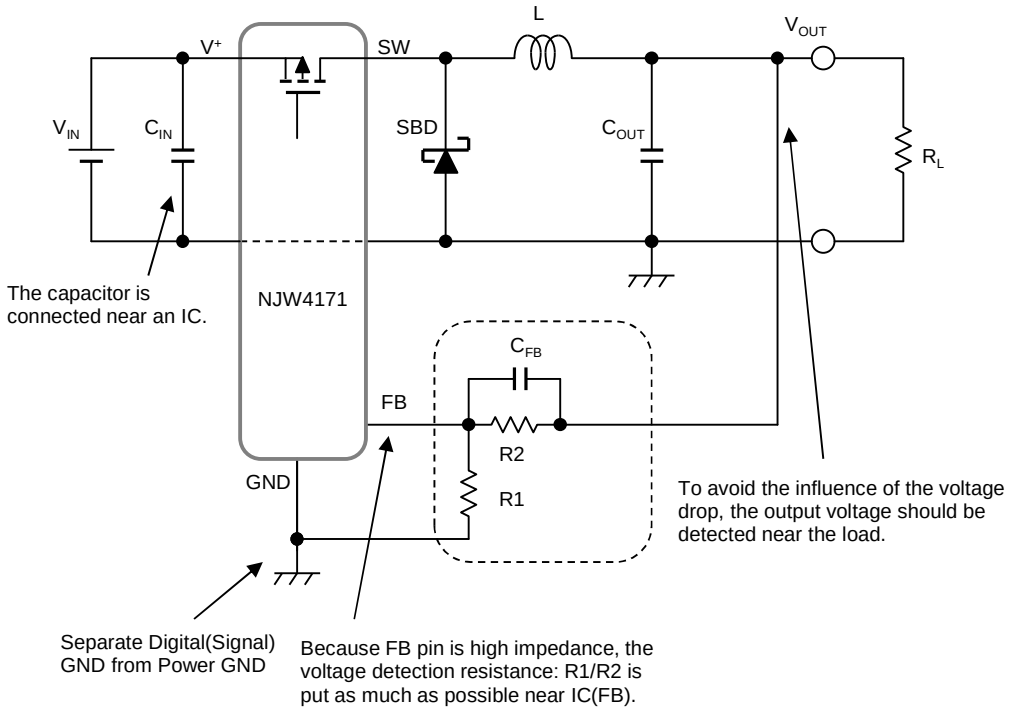
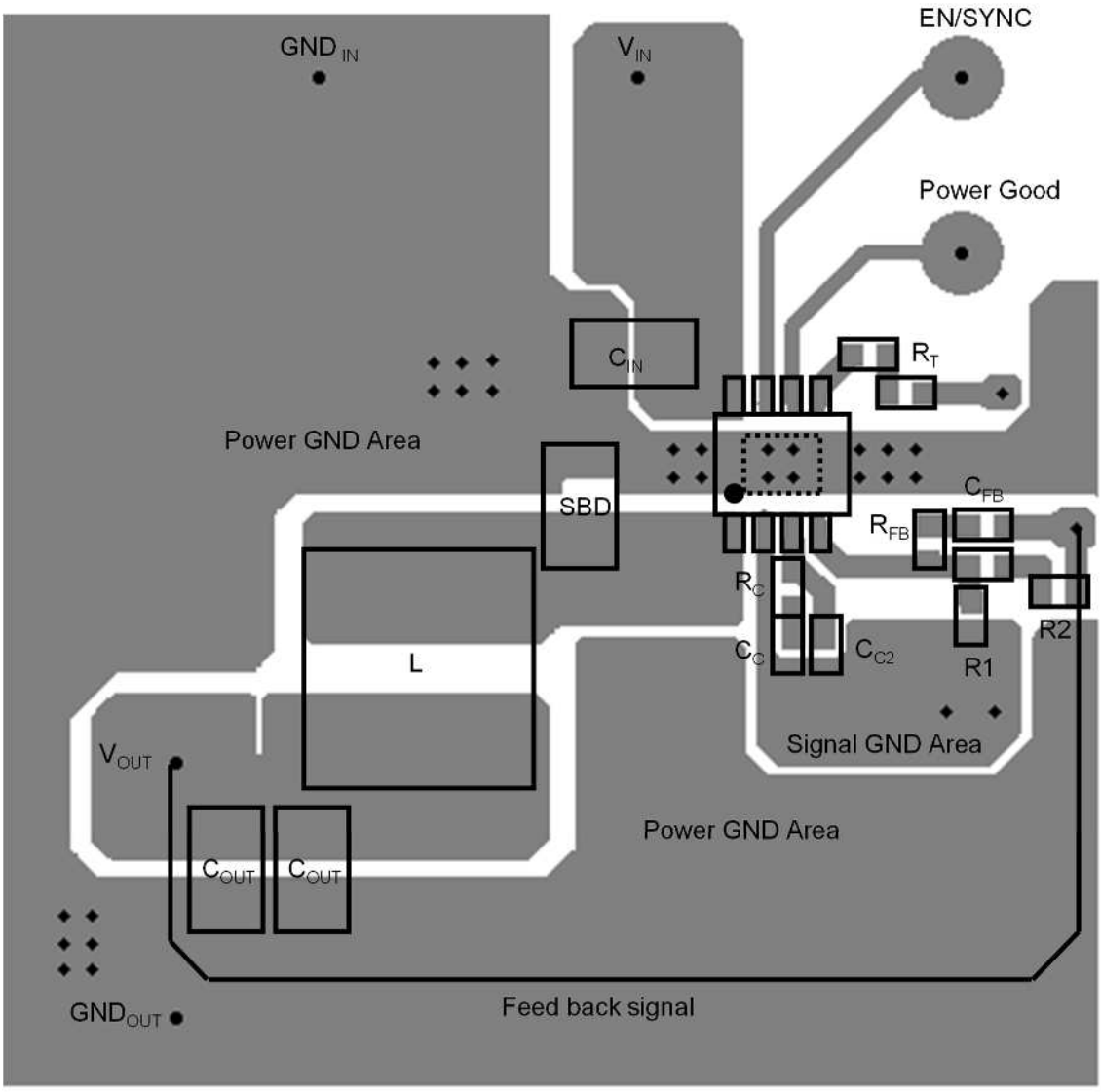


Fig. 9. Board Layout at Buck Converter

■ **Application Information (Continued)**



Connect Signal GND line and Power GND line on backside pattern

Fig. 10. Layout Example (upper view)

■ **Calculation of Package Power**

A lot of the power consumption of buck converter occurs from the internal switching element (Power MOSFET). Power consumption of NJW4171 is roughly estimated as follows.

Input Power:	$P_{IN} = V_{IN} \times I_{IN}$ [W]
Output Power:	$P_{OUT} = V_{OUT} \times I_{OUT}$ [W]
Diode Loss:	$P_{DIODE} = V_F \times I_{L(avg)} \times$ OFF duty [W]
NJW4171 Power Consumption:	$P_{LOSS} = P_{IN} - P_{OUT} - P_{DIODE}$ [W]

Where:

V_{IN}	: Input Voltage for Converter	I_{IN}	: Input Current for Converter
V_{OUT}	: Output Voltage of Converter	I_{OUT}	: Output Current of Converter
V_F	: Diode's Forward Saturation Voltage	$I_{L(avg)}$	: Inductor Average Current
OFF duty	: Switch OFF Duty cycle		

Efficiency (η) is calculated as follows.

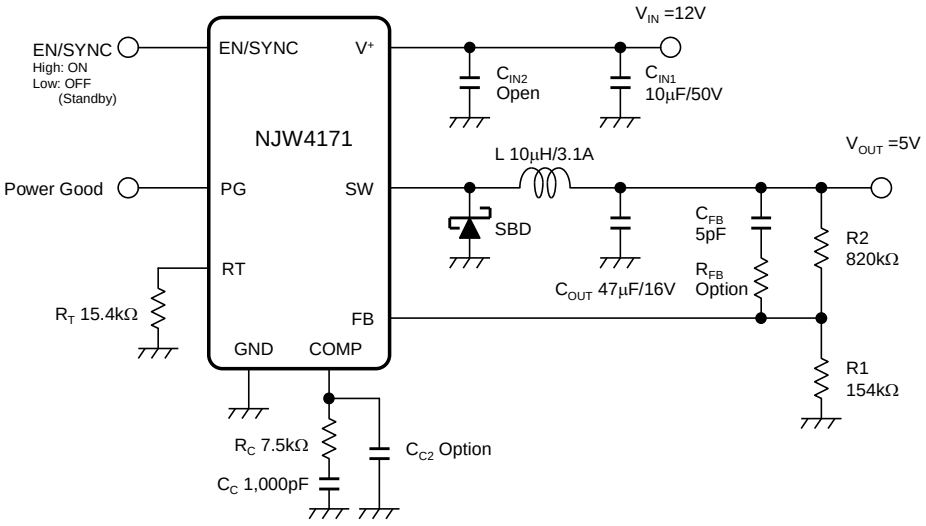
$\eta = (P_{OUT} \div P_{IN}) \times 100$ [%]

You should consider temperature derating to the calculated power consumption: P_D.

You should design power consumption in rated range referring to the power dissipation vs. ambient temperature characteristics.

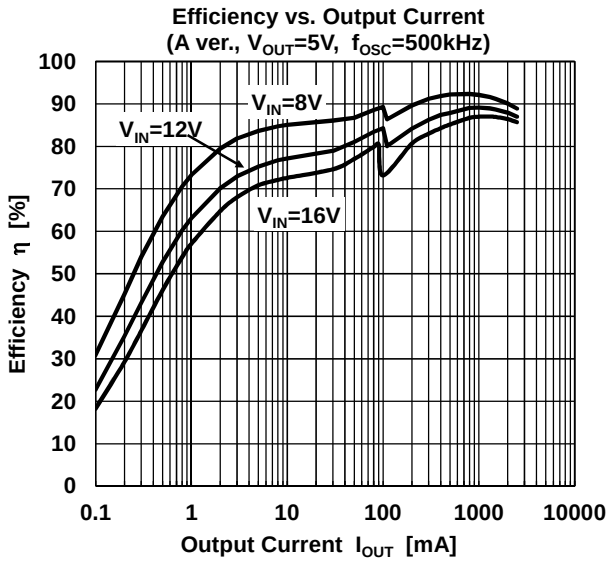
■ Application Design Examples

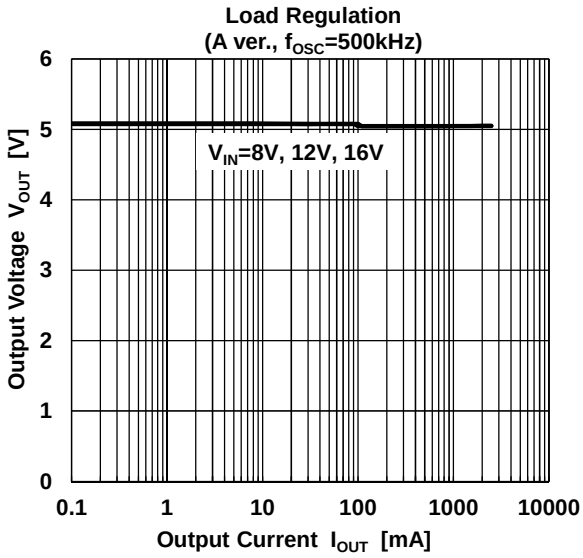
IC : NJW4171GM1-A
Input Voltage : V_{IN}=12V
Output Voltage : V_{OUT}=5V
Output Current : I_{OUT}=2.5A
Oscillating frequency : f_{OSC}=500kHz

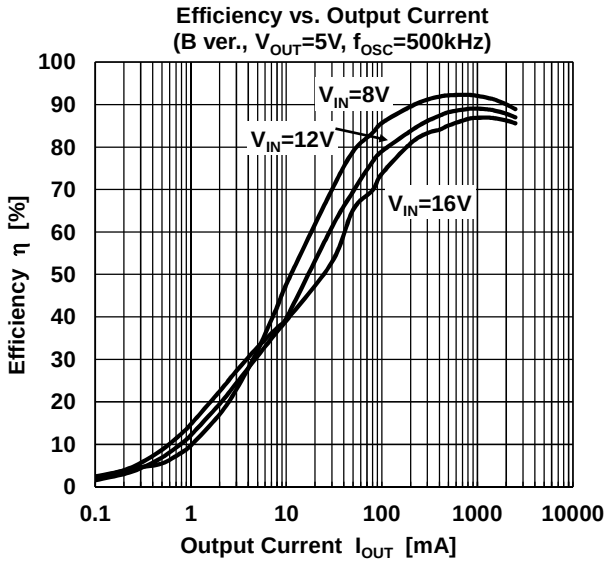


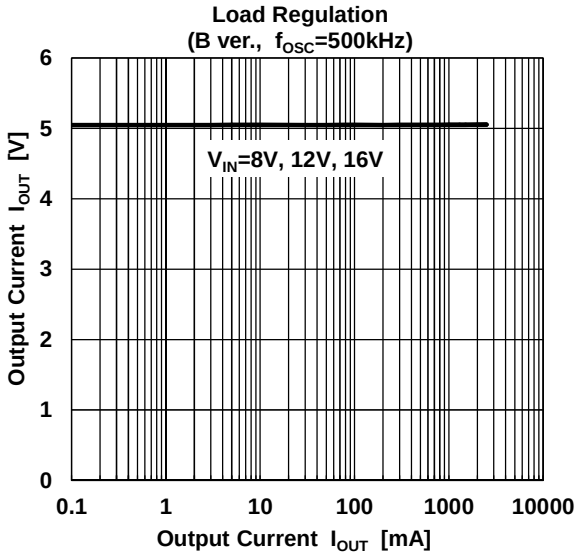
Reference	Qty.	Part Number	Description	Manufacturer
IC	1	NJW4171GM1-A	Internal 2.5A MOSFET SW.REG. IC	New JRC
L	1	CLF7045NIT-100M	Inductor 10µH, 3.1A	TDK
SBD	1	D1FT4A	Schottky Diode 40V, 3A	Shindengen
C_{IN1}	1	UMK325BJ106MM	Ceramic Capacitor 3225 10µF, 50V, X5R	Taiyo Yuden
C_{OUT}	1	GRM32EB31C476KE15	Ceramic Capacitor 3225 47µF, 16V, B	Murata
C_{FB}	1	5pF	Ceramic Capacitor 1608 5pF, 50V, CH	Std.
C_C	1	1,000pF	Ceramic Capacitor 1608 1,000pF, 50V, CH	Std.
R_C	1	7.5kΩ	Resistor 1608 7.5kΩ, ±1%, 0.1W	Std.
R1	1	154kΩ	Resistor 1608 154kΩ, ±1%, 0.1W	Std.
R2	1	820kΩ	Resistor 1608 820kΩ, ±1%, 0.1W	Std.
R_T	1	15.4 kΩ	Resistor 1608 15.4kΩ, ±1%, 0.1W	Std.

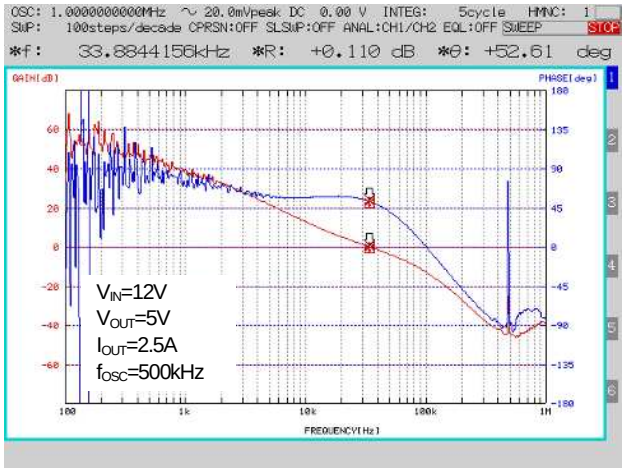
■ Application Characteristics







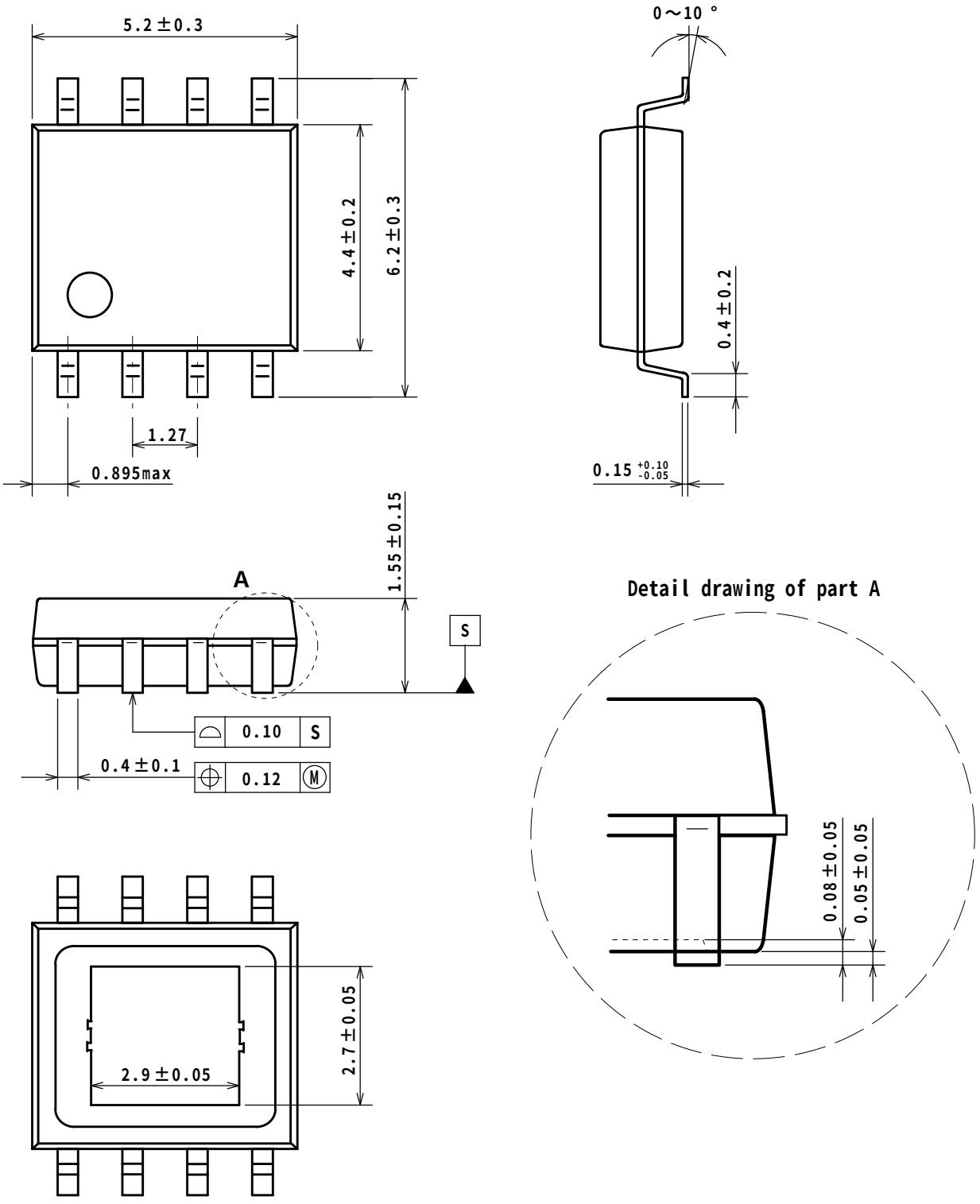




HSOP8

Unit: mm

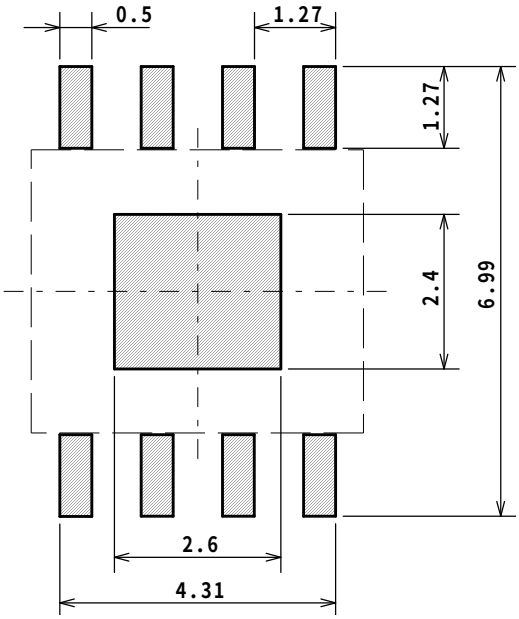
■PACKAGE DIMENSIONS



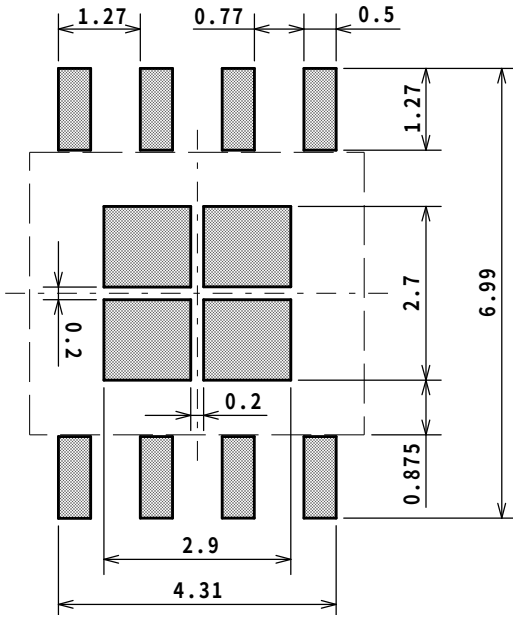
HSOP8

Unit: mm

■EXAMPLE OF SOLDER PADS DIMENSIONS



<Solder pattern>



<Metal mask>

<Instructions for mounting>

Please note the following points when you mount HSOP-8 package IC because there is a standoff on the backside electrode.

(1) Temperature profile of lead and backside electrode.

It is necessary that both re-flow temperature profile of lead and backside electrode are higher than preset temperature.
When solder wet temperature is lower than lead/backside electrode temperature, there is possibility of defect mounting.

(2) Design of foot pattern / metal mask

Metal mask thickness of solder pattern print is more than 0.13mm.

(3) Solder paste

The mounting was evaluated with following solder paste, foot pattern and metal mask.
Because mounting might be greatly different according to the manufacturer and the product number even if the solder composition is the same.
We will strongly recommend to evaluate mounting previously with using foot pattern, metal mask and solder paste.

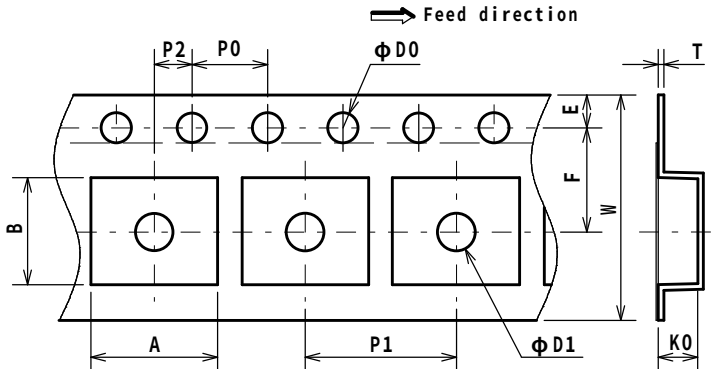
Solder paste composition	Sn37Pb (Senju Metal Industry Co., Ltd：OZ7053-340F-C)
	Sn3Ag0.5Cu (Senju Metal Industry Co., Ltd：M705-GRN350-32-11)

HSOP8

■ PACKING SPEC

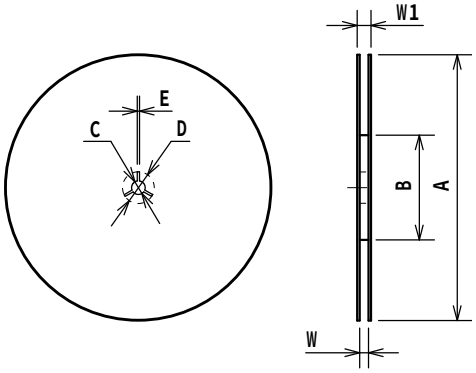
Unit: mm

TAPING DIMENSIONS



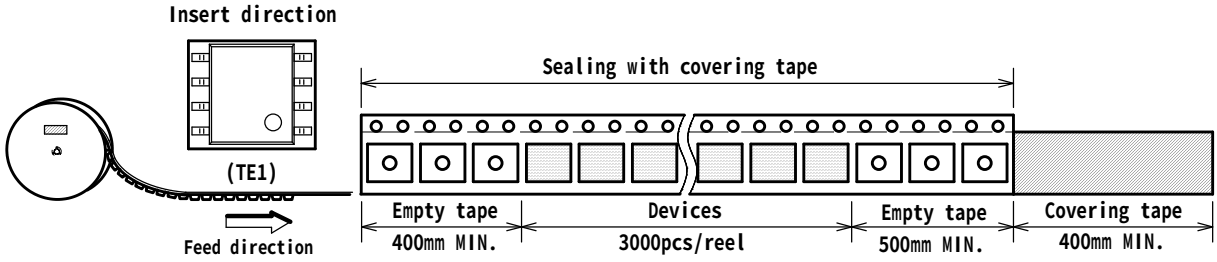
SYMBOL	DIMENSION	REMARKS
A	6.7±0.1	
B	5.55±0.1	
D0	1.55±0.05	
D1	2.05±0.05	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.3±0.05	
T2	2.47	
K0	2.1±0.1	
W	12.0±0.2	

REEL DIMENSIONS

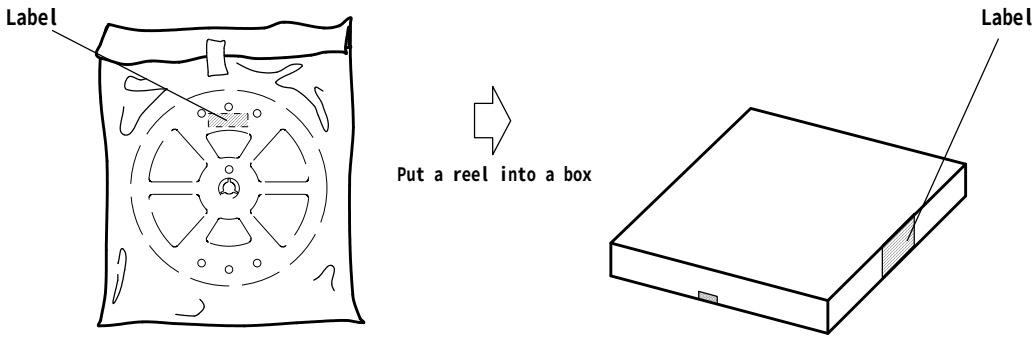


SYMBOL	DIMENSION
A	Φ330±2
B	Φ 80±1
C	Φ 13±0.2
D	Φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	17.5±1

TAPING STATE



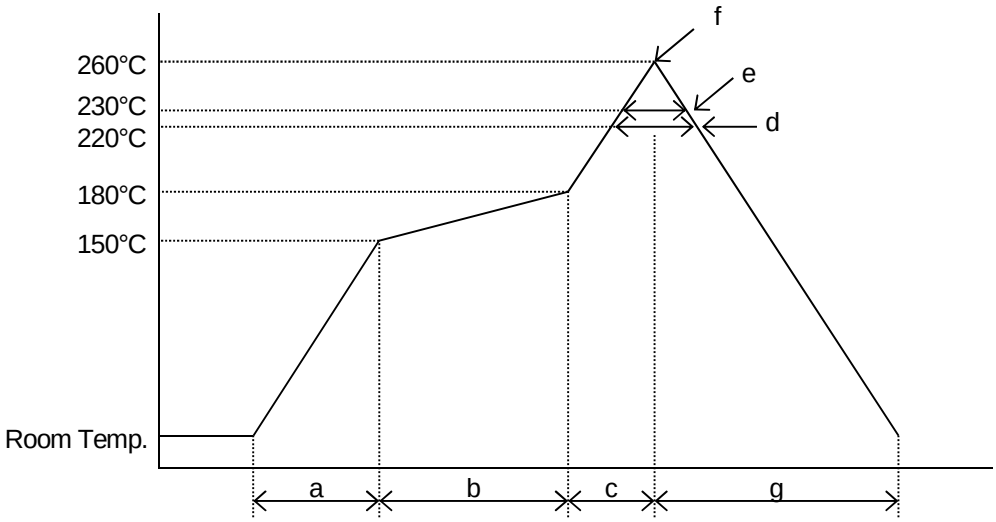
PACKING STATE



■ MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD

Recommended reflow soldering procedure



a:Temperature ramping rate	: 1 to 4°C /s
b:Pre-heating temperature	: 150 to 180°C
time	: 60 to 120s
c:Temperature ramp rate	: 1 to 4°C /s
d:220°C or higher time	: Shorter than 60s
e:230°C or higher time	: Shorter than 40s
f:Peak temperature	: Lower than 260°C
g:Temperature ramping rate	: 1 to 6°C /s

The temperature indicates at the surface of mold package.

■**REVISION HISTORY**

DATE	REVISION	CHANGES
27.Mar.2017	Ver.1.0	New Release
13.Apr.2017	Ver.1.1	Corrected of FEATURES. Addition of PACKAGE DIMENSIONS, EXAMPLE OF SOLDER PADS DIMENSIONS, PACKING SPEC and MOUNTING METHOD.
01.Aug.2017	Ver.1.2	Corrected of Application Data.
17.Jun.2019	Ver.1.3	Status change of A ver., Correct the formula of P.23
29.Oct.2019	Ver.1.4	Correct the formula of P.19
5.Feb.2021	Ver.1.5	Add the *PRODUCT CLASSIFICATION*
23.Aug.2021	Ver.1.6	Corrected of Application.

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