RICOH

R1271x Series

30 V, 1 A Synchronous PWM Step-down DC/DC Converter

No. EA-517-201127

OVERVIEW

The R1271x is a synchronous step-down DC/DC converter with a maximum input voltage rating of 42V. This device is suitable for small inductors with the switching frequency of 2 MHz. The external components are only an inductor and several capacitors and a resistance. The tiny DFN package option makes the power circuit compact .

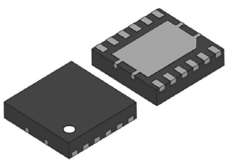
KEY BENEFITS

- High efficiency 85% is realized with switching frequency of 2 MHz
- The output voltage is maintained at cranking by reducing a switching frequency to minimum 1/4 of normal frequency.
- EMI noise reduction by using a spread spectrum clock generator. (Diffusion Rate: +10%).

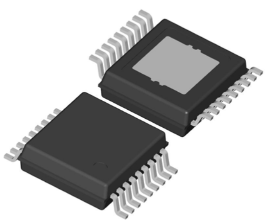
KEY SPECIFICATIONS

- Input Voltage Range (Maximum Ratings): 3.6 V to 30 V (42 V)
- Start-up Voltage: 4.5 V
- Standby Current: Typ. 4 µA
- Operating Temperature Range: -40°C to 105°C
- Output Voltage Accuracy: ±1.0% (Ta = 25°C)
- Oscillator Frequency: Typ.2 MHz (Fixed inside the IC)
- Spread Spectrum Clock Generator (SSCG): Diffusion Rate: Typ. +10%
- Minimum On-Time: Typ. 70 ns
- Minimum Off-Time: Typ. 120 ns
- Duty-over: Oscillation Frequency x 1 ~ 1/4
- Soft start function
- Thermal Shutdown: Typ. Tj = 160°C
- Undervoltage Lockout (UVLO): VCC = 3.3 V (Typ.)
- Overvoltage Lockout (OVLO): VIN = 35 V (Typ.)
- Overvoltage Detection (OVD): Output Voltage (VOUT) +10%
- LX Current Limit: Typ. 1.8 A (LIMIT Pin Open)
- High-side MOS FET On Resistance: Typ. 0.4 Ω
- Low-side MOS FET On Resistance: Typ. 0.2 Ω

PACKAGES

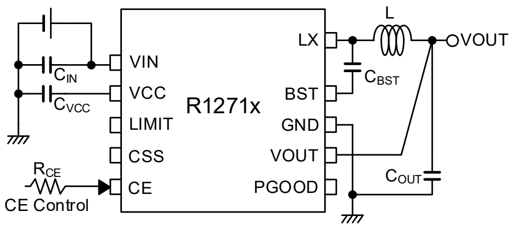


*Wettable Flanks
DFN3030-12B
3.0 x 3.0 x 0.8 (mm)

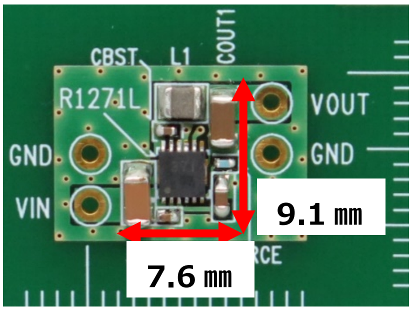


HSOP-18
5.2 x 6.2 x 1.45 (mm)

TYPICAL APPLICATION



PCB EXAMPLE



EV Board (DFN3030-12B)

OPTIONAL FUNCTIONS

Product Name	Set Output Voltage (V_{SET})
R1271x331∗	3.3 V
R1271x501∗	5.0 V

Product Name	Overcurrent Protection	SSCG
R1271xxx1A	Hiccup-type	Disable
R1271xxx1B	Latch-type	Disable
R1271xxx1C	Hiccup-type	Enable
R1271xxx1D	Latch-type	Enable

APPLICATIONS

- Digital Electronics: Digital TVs, DVD Players
- Portable Communication Equipment, Cameras, Video Cameras

SELECTION GUIDE

The set Output Voltage, the Optional functions and Quality class can be designated by user's request.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1271Lxx1*-TR	DFN3030-12B	3,000 pcs	Yes	Yes
R1271Sxx1*-E2-FE	HSOP-18	1,000 pcs	Yes	Yes

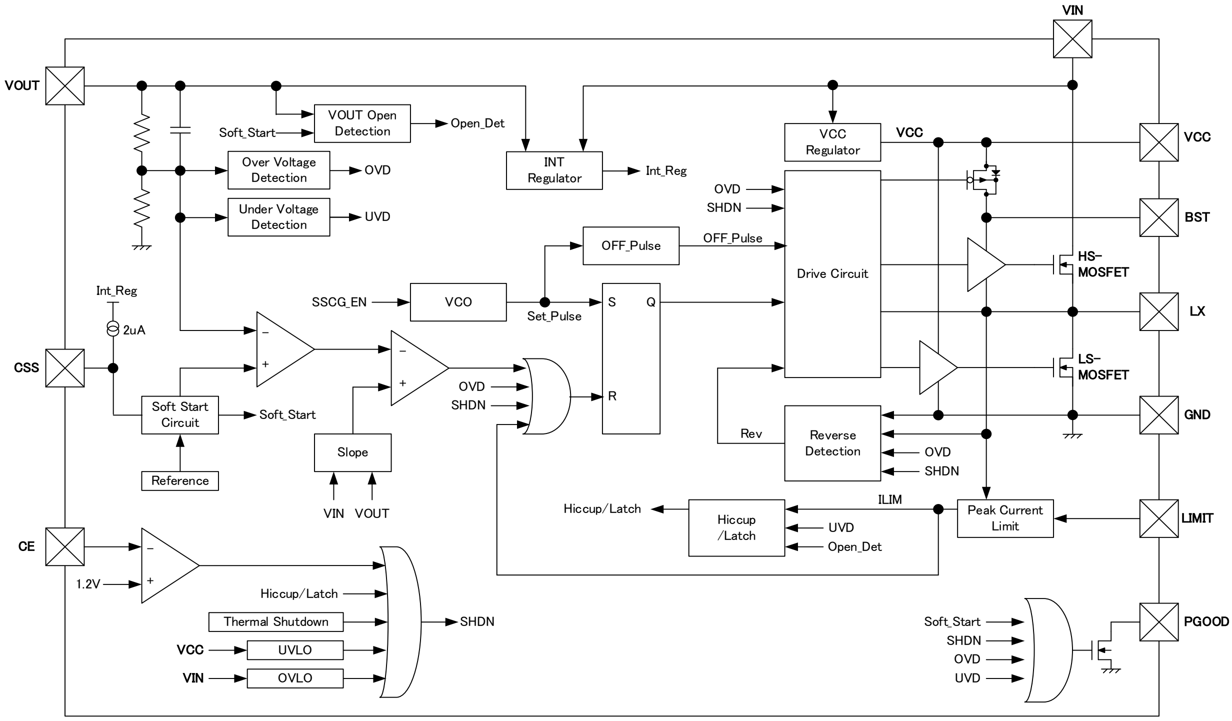
xx : Select the Set Output Voltage (V_{SET}).

xx	Set Output Voltage (V_{SET})
33	3.3 V
50	5.0 V

∗ : Select the optional functions.

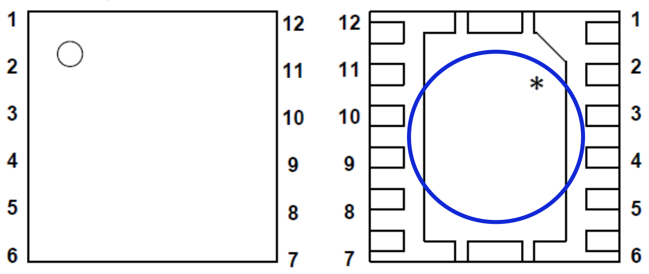
∗	Overcurrent Protection	SSCG
A	Hiccup-type	Disable
B	Latch-type	Disable
C	Hiccup-type	Enable
D	Latch-type	Enable

BLOCK DIAGRAM



R1271x Block Diagram

PIN DESCRIPTIONS



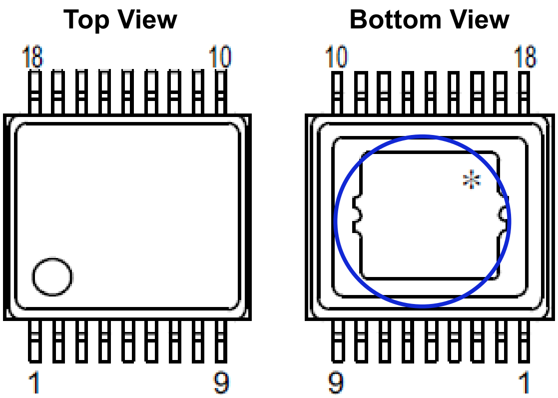
R1271L (DFN3030-12B) Pin Configuration

∗ The tab on the bottom of the package is substrate level (GND). The tab must be connected to the ground plane on the board.

R1271L (DFN3030-12B) Pin Description

Pin No.	Pin Name	Description
1	VIN	Power Supply Pin
2	NC[1]	No Connection
3	VCC	VCC Output Pin
4	LIMIT	Current Limit Adjustment Pin
5	CSS	Soft-start Adjustment Pin
6	CE	Chip Enable Pin, Active-high
7	PGOOD	Power Good Pin
8	VOUT	Output Voltage Feedback Input Pin
9	NC[1]	No Connection
10	GND	GND Pin
11	BST	Bootstrap Pin
12	LX	Switching Pin

(1) It is recommended to set the NC pin left open to prevent failure caused by adjacent pins' short circuit.



R1271S (HSOP-18) Pin Configuration

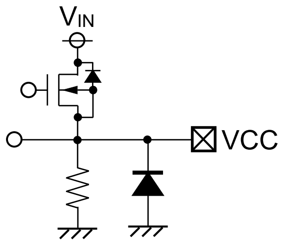
* The tab on the bottom of the package is substrate level (GND). The tab must be connected to the ground plane on the board.

R1271S (HSOP-18) Pin Description

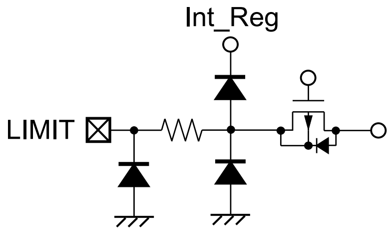
Pin No.	Pin Name	Description
1, 2	VIN[1]	Power Supply Pin
3, 4	NC[2]	No Connection
5	VCC	VCC Output Pin
6	LIMIT	Current Limit Adjustment Pin
7	CSS	Soft-start Adjustment Pin
8	NC[2]	No Connection
9	CE	Chip Enable Pin, Active-high
10	PGOOD	Power Good Pin
11	VOUT	Output Voltage Feedback Input Pin
12	NC[2]	No Connection
13, 14, 15	GND[1]	GND Pin
16	BST	Bootstrap Pin
17, 18	LX[1]	Switching Pin

(1) The pins with the same name should be tied together except NC pins.
(2) It is recommended to set the NC pin left open to prevent failure caused by adjacent pins' short circuit.

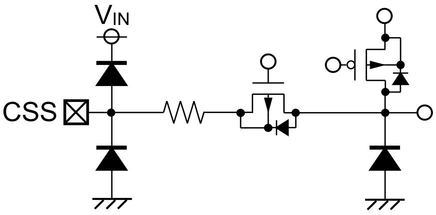
● Equivalent Circuits for the Individual Terminals



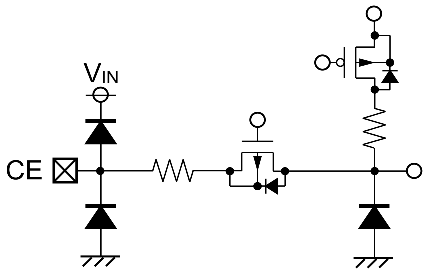
Equivalent Circuit for VCC Pin



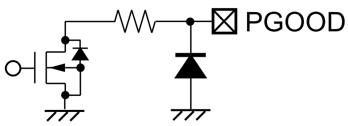
Equivalent Circuit for LIMIT Pin



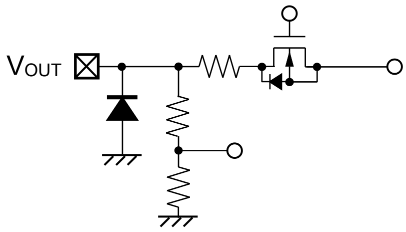
Equivalent Circuit for CSS Pin



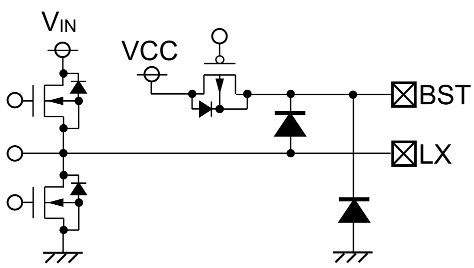
Equivalent Circuit for CE Pin



Equivalent Circuit for PGOOD Pin



Equivalent Circuit for V_{OUT} Pin



Equivalent Circuit for BST-LX Pin

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ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Pin Input Voltage	−0.3 to 42	V
V_{CE}	CE Pin Voltage	−0.3 to V_{IN}+0.3 ≤ 42	V
V_{CSS}	CSS Pin Voltage	−0.3 ~ 3	V
V_{OUT}	VOUT Pin Voltage	−0.3 to 30	V
V_{CC}	VCC Pin Voltage	−0.3 to 6	V
	VCC Pin Output Current	Internally Limited	mA
V_{BST}	BST Pin Voltage	LX−0.3 to LX+6	V
V_{LX}	LX Pin Voltage	−0.3 to V_{IN} +0.3 ≤ 36	V
V_{PGOOD}	PGOOD Pin Voltage	−0.3 to 16	V
V_{LIMIT}	LIMIT Pin Voltage	−0.3 to 6	V
P_D	Power Dissipation	Refer to Appendix *"POWER DISSIPATION"*	
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	Operating Input Voltage	3.6 to 30	V
Ta	Operating Temperature Range	−40 to 105	°C
V_{UP}	PGOOD Pin Pull-up Voltage	0 to 5.5	V

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

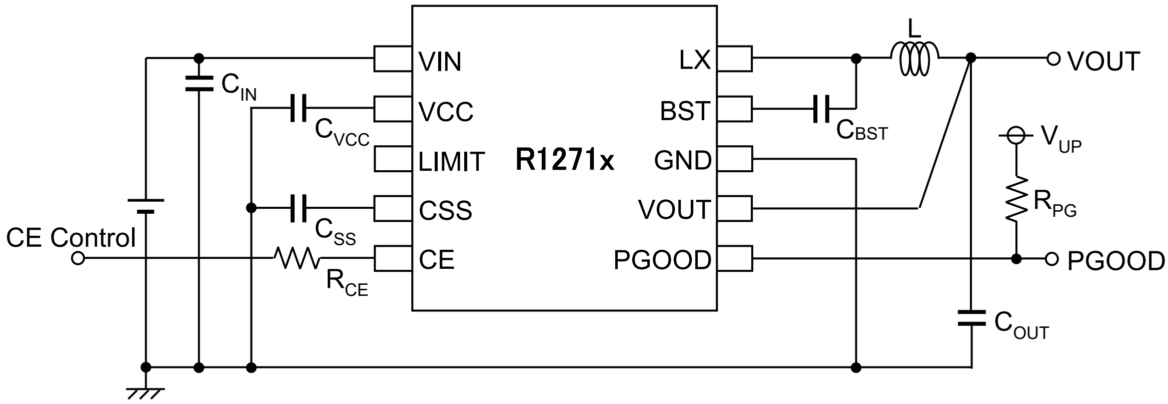
V_{IN} = 12 V, V_{CE} = V_{IN}, unless otherwise specified.
The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

R1271x Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{START}	Start-up Voltage				[4.5]	V
V_{CC}	VCC Pin Voltage (VCC-GND)	V_{OUT} = V_{SET} x 1.05	[4.75]	5	[5.25]	V
$I_{STANDBY}$	Standby Current	V_{CE} = 0 V		4		μA
		V_{IN} = 30 V, V_{CE} = 0 V			[30]	
I_{VIN1}	VIN Consumption Current 1 at PWM switching stop	V_{OUT} = V_{SET} x 1.05		1.0	[1.35]	mA
V_{UVLOF}	Undervoltage Lockout (UVLO) Threshold Voltage	V_{CC} Falling	[3.10]	3.3	[3.50]	V
V_{UVLOR}		V_{CC} Rising	[4.10]	4.3	[4.49]	V
V_{OVLOR}	Overvoltage Lockout (OVLO) Threshold Voltage	V_{IN} Rising	[33.6]	35	[36.75]	V
V_{OVLOF}		V_{IN} Falling	[32.0]	34	[36.2]	V
V_{OUT}	Output Voltage (R1271x331x)	Ta = 25°C	3.267	3.3	3.333	V
		−40°C ≤ Ta ≤ 105°C	[3.234]		[3.366]	
	Output Voltage (R1271x501x)	Ta = 25°C	4.950	5.0	5.050	
		−40°C ≤ Ta ≤ 105°C	[4.900]		[5.100]	
f_{OSC0}	Oscillator Frequency 0	8 V ≤ V_{IN} ≤ 16 V, I_{OUT} = 0 A	[1800]	2000	[2200]	kHz
t_{SS1}	Soft-start Time 1	CSS = OPEN	[0.36]	0.5	[0.75]	ms
t_{SS2}	Soft-start Time 2	CSS = 4.7 nF	[1.4]		[2.0]	ms
I_{TSS}	Soft-start Pin Charging Current	V_{CSS} = 0 V	[1.8]	2	[2.2]	μA
V_{SSEND}	CSS Pin Voltage at soft-start stop		[0.635]	0.64	[0.705]	V
R_{DIS_CSS}	CSS Pin Discharge Resistance	V_{IN} = 4.5 V, V_{CE} = 0 V, V_{CSS} = 3 V	[1.8]	3	[5]	kΩ
$I_{LXLIMIT}$	LX Current Limit (High-side MOS FET)	DC Current, LIMIT = OPEN	[1.5]	1.8	[2.3]	A
		DC Current, LIMIT = 0V	[0.75]	1.0	[1.25]	
V_{CEH}	CE ”High” Input Voltage		[1.25]			V
V_{CEL}	CE ”Low” Input Voltage				[1.1]	V
I_{CEH}	CE ”High” Input Current	V_{IN} = V_{CE} = 30 V		1.2	[2.45]	μA
I_{CEL}	CE ”Low” Input Current	V_{IN} = 30V, V_{CE} = 0 V	[-0.1]	0	[0.1]	μA
I_{VOUTH}	VOUT ”High” Pin Current		[130]		[390]	μA
$V_{PGOODOFF}$	PGOOD “Low” Output Voltage	V_{IN} = 3.6 V, I_{PGOOD} = 1 mA			[0.35]	V
$I_{PGOODOFF}$	PGOOD Pin Leakage Current	V_{IN} = 30V, V_{PGOOD} = 6 V	[-0.1]	0	[0.1]	μA
V_{OVDR}	Overvoltage Detection (OVD) Threshold Voltage	V_{OUT} Rising	V_{SET} [x1.06]	V_{SET} x1.10	V_{SET} [x1.14]	V
V_{OVDF}	Overvoltage Release (OVD) Threshold Voltage	V_{OUT} Falling	V_{SET} [x1.02]	V_{SET} x1.07	V_{SET} [x1.12]	V
V_{UVDF}	Undervoltage Detection (UVD) Threshold Voltage	V_{OUT} Falling	V_{SET} [x0.86]	V_{SET} x0.90	V_{SET} [x0.94]	V
V_{UVDR}	Undervoltage Release (UVD) Threshold Voltage	V_{OUT} Rising	V_{SET} [x0.88]	V_{SET} x0.93	V_{SET} [x0.98]	V

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

• TYPICAL APPRICATION CIRCUIT



R1271x Typical Application Circuit

Recommended Ceramic Capacitors

Symbol	Capacitance	Tolerance	Voltage resistance	Temperature characteristics
C_{IN}	10 µF	±10%	50 V	X7R
C_{OUT}	10 µF	±10%	50 V	X7S
C_{BST}	0.1 µF	±10%	25 V	X7R
C_{VCC}	1.0 µF	±20%	16 V	X7R

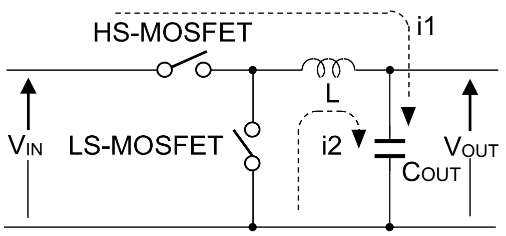
Symbol	Inductance	Tolerance	Rated current
L	2.2 µH	±20%	3.3A

It is recommended to set 1 kΩ or higher for R_{CE} and 10 kΩ or higher for R_{PG}

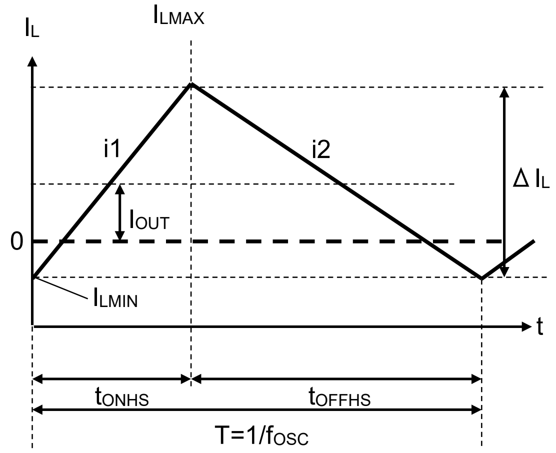
THEORY OF OPERATION

Operation of Step-down DC/DC Converter

The basic operation of the step-down DC/DC converter is shown in the following figures.



Basic Circuit



Current Through Inductor

Step1. When the high-side MOSFET turns on, current I_L (= i1) flows through the Inductor(L) to charge C_{OUT} and provide I_{OUT}. At this moment, I_L increases from I_{LMIN} to reach I_{LMAX} in proportion to the on-time period (t_{ON}) of the high-side MOSFET.

Step2. When the high-side MOSFET turns off, the low-side MOSFET turns on to flow current I_L (= i2).

Step3. The low-side MOSFET turns on until going to the next cycle. When I_{OUT} is small, the low-side MOS FET must keep “on” to meet $I_L = I_{LMIN} < 0$.

In the PWM mode, the output voltage is maintained constant by controlling t_{ONHS} with the constant switching frequency (f_{OSC}).

Calculation of Inductor Current

The peak inductor current I_{LMAX} can be estimated by the following equation.

$I_{LMAX} = I_{OUT} + 1 / 2 \times (V_{IN} – V_{OUT}) / L \times V_{OUT} / V_{IN} / f_{OSC}$

Example: I_{LMAX} = 1A + 1/2 × (12V – 5V) / 2.2μH × 5V / 12V / 2MHz
= 1.331 A

The above can be calculated from the equation with the inductor current in continuous mode of a general step-down DC/DC converter. The P-P value of the inductor ripple current is "ΔI_L".

The ΔI_L is calculated by Equation 1 when the high side MOS FET is ON.

$\Delta I_L = (V_{IN} – V_{OUT}) / L \times t_{ONHS}$ ······ Equation 1

The ΔI_L is calculated by Equation 2 when the high side MOS FET is OFF.

$\Delta I_L = V_{OUT} / L \times t_{OFFHS}$ ······ Equation 2

Using Equation 2 to Equation 1, the ON duty of the high side MOS FET $t_{ONHS} / (t_{ONHS} + t_{OFFHS}) = D_{ON}$ is solved by Equation 3.

$D_{ON} = V_{OUT} / V_{IN}$ ······ Equation 3

And then, the ripple current ΔI_L is calculated by substituting t_{ONHS} = Don / f_{OSC} into Equation 1.

$\Delta I_L = (V_{IN} - V_{OUT}) / L \times D_{ON} / fosc$ ······ Equation 4

At this time, I_{LMAX} flowing in the inductor and high side MOS FET is calculated by Equation 5.

$I_{LMAX} = I_{OUT} + \Delta I_L / 2$ ······ Equation 5

Therefor I_{LMIN} is calculated by Equation 6.

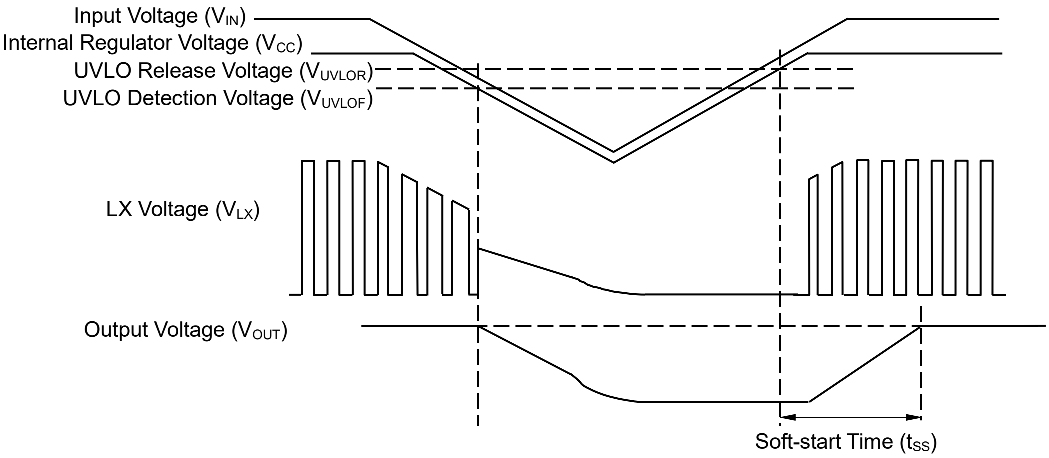
$I_{LMIN} = I_{OUT} - \Delta I_L / 2$ ······ Equation 6

Note that the input-output conditions and peripheral components should be determined in consideration of I_{LMAX} and I_{LMIN}.

The above calculations are based on the ideal operation in continuous mode.

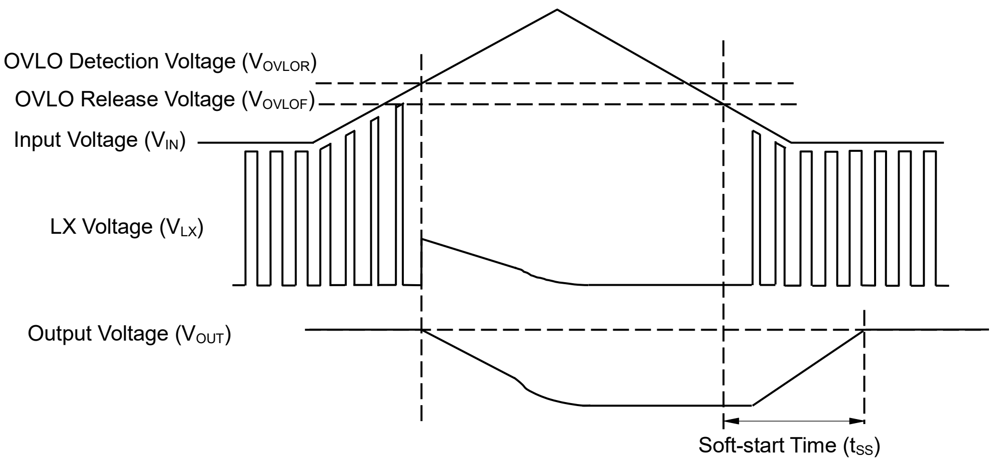
UVLO (Undervoltage Lockout)

When the VCC pin voltage decreases below the UVLO detection threshold voltage due to the input voltage decrease, the R1271x turns the switching off to prevent the malfunction of the device. Due to the switching stop, the output voltage decreases according to the load and C_{OUT}. If the VCC pin voltage increases above the UVLO release threshold voltage, the device restarts the operation with soft-start.



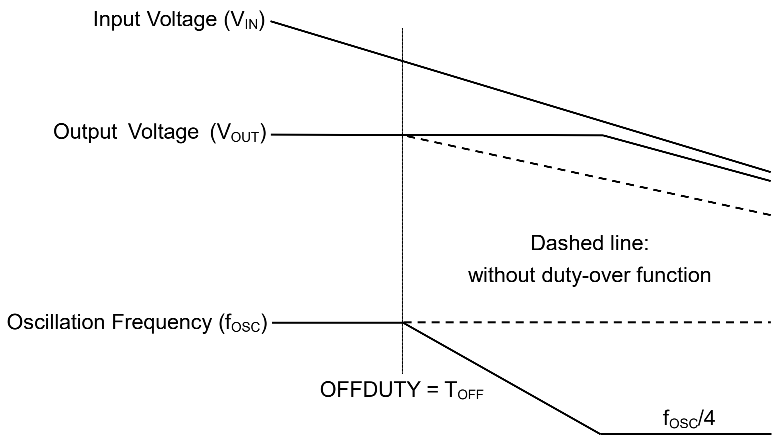
OVLO (Overvoltage Lockout)

When the input voltage rises above the OVLO detection threshold of voltage, the R1271x turns the switching off to prevent malfunctions of the device or damage on the high side MOS FET and low side MOS FET due to overvoltage. Due to the switching stop, the output voltage decreases according to the load and C_{OUT}. If the input voltage decreases below the OVLO release threshold voltage, the device restarts the operation with soft start. Note that this function does not guarantee the operation exceeding the absolute maximum ratings.



Duty-over Function

When the input voltage is dropped at when the input voltage drops, the R1271x linearly changes the operating frequency to 1/4 of the set oscillator frequency in order to maintain the output voltage. This increases the on duty and reduce the voltage difference between input and output. The duty-over starts operating when it detects the minimum off-time.



Frequency modulation by duty over

Minimum Off-Time

The minimum off time indicates the minimum time that the high side MOS FET can be turned off within the oscillation period. The minimum off time (Typ. 120 ns) of R1271x is determined by the internal circuit, using a NMOS of high side MOS FET by adopting bootstrap method. Charging a voltage to drive the high side MOS FET is needed, and the minimum off time is determined by the time required for charging.
When the input voltage is low or sudden load transient occurs, the high-side MOS FET is turned off at least every 4 cycles by the duty over function substantially. The input / output voltage difference is decreased by increasing the maximum duty ratio.

Minimum On-Time

The minimum on-time indicates the minimum time duration that the R1271x can turn the high-side MOS FET on during the oscillation period. The minimum on-time (Typ. 70 ns) of the device is determined by the internal circuit. The device cannot generate a pulse width that is less than the pulse width of minimum on-time. If the minimum step-down ratio/ the oscillator frequency: [V_{OUT} / V_{IN} x (1 / f_{OSC})].is less than the minimum on-time, the pulse skipping occurs, which stabilizes the output voltage but increases the ripple of current and voltage.

Standby Function

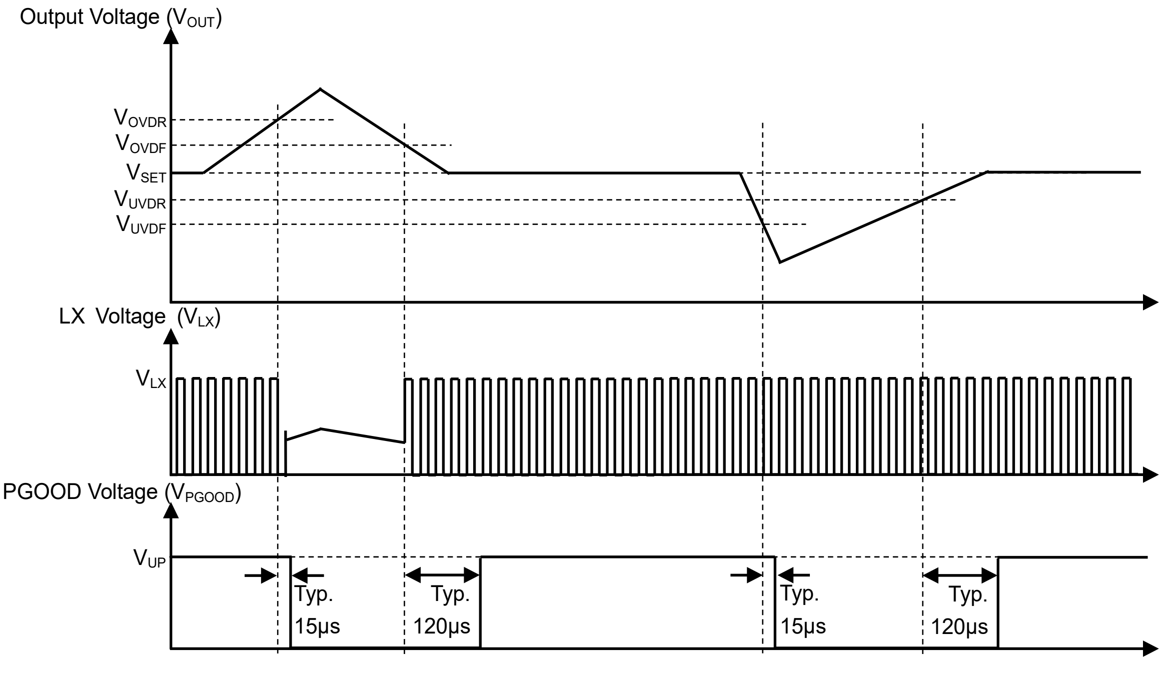
When the CE pin voltage drops below 1.1V (“Low” threshold voltage), switching is turned off. If the CE pin voltage rises above the 1.25 V (“High” threshold voltage), the R1271x will restart with a soft start.
In order for the VIN current to be the standby current ($I_{STANDBY}$), the CE pin voltage must be 0.4V or less.

Overvoltage Detection (OVD)

The OVD function monitors the output voltage. Switching stops even if the internal circuit is active state, when detecting the overvoltage. The OVD detection voltage is Typ.110% of VSET, and the PGOOD pin outputs "Low" when VOUT is over the OVD detection threshold voltage for Typ.15 μs or more. When V_{OUT} is under 107% (Typ.) of V_{SET}, the PGOOD pin outputs “High” after delay time (Typ.120 μs). Then, switching is controlled by normal operation.

Under Voltage Detection (UVD)

The UVD function monitors the output voltage. The UVD detection voltage is Typ.90% of VSET, and the PGOOD pin outputs "Low" when VOUT is less than the UVD detection threshold voltage for Typ.15 μs or more. When V_{OUT} is over 93% (Typ.) of V_{SET}, the PGOOD pin outputs “High” after delay time (Typ.120 μs.). Then, the overcurrent protection works when detecting a current limit during the UVD detection.



Overvoltage detection / undervoltage detection sequence

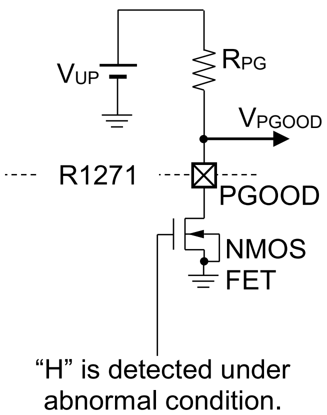
PGOOD (Power Good) Function

The power good function with using a Nch open drain output pin can detect the following states of the R1271x. The NMOS FET turns on and the PGOOD pin becomes "Low" when detecting them.

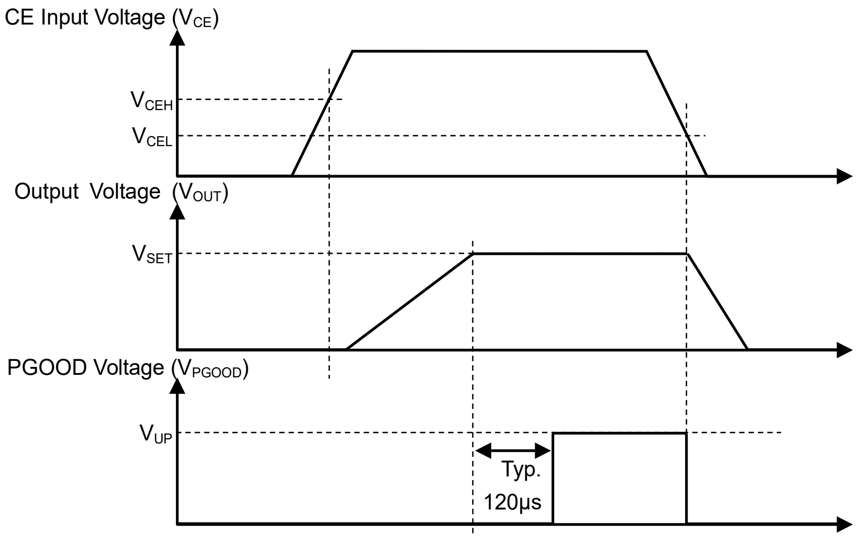
- V_{CE}<V_{CEL}
- UVLO
- OVLO
- Thermal Shutdown
- Soft-start
- UVD
- OVD
- Hiccup-type Protection
- Latch-type protection

After the device returns to their original state, the NMOS FET turns off and the PGOOD pin outputs "High" (PGOOD Input Voltage: V_{UP}).

The PGOOD pin is designed to become 0.35 V or less in "Low" level when the current floating to the PGOOD pin is 1 mA. The use of the PGOOD input voltage (V_{UP}) of 5.5 V or less and the pull-up resistor (R_{PG}) of 10 kΩ to 100 kΩ are recommended. If not using the PGOOD pin, connect it to "Open" or "GND".



Power good schematic



Power good circuit rise / fall sequence

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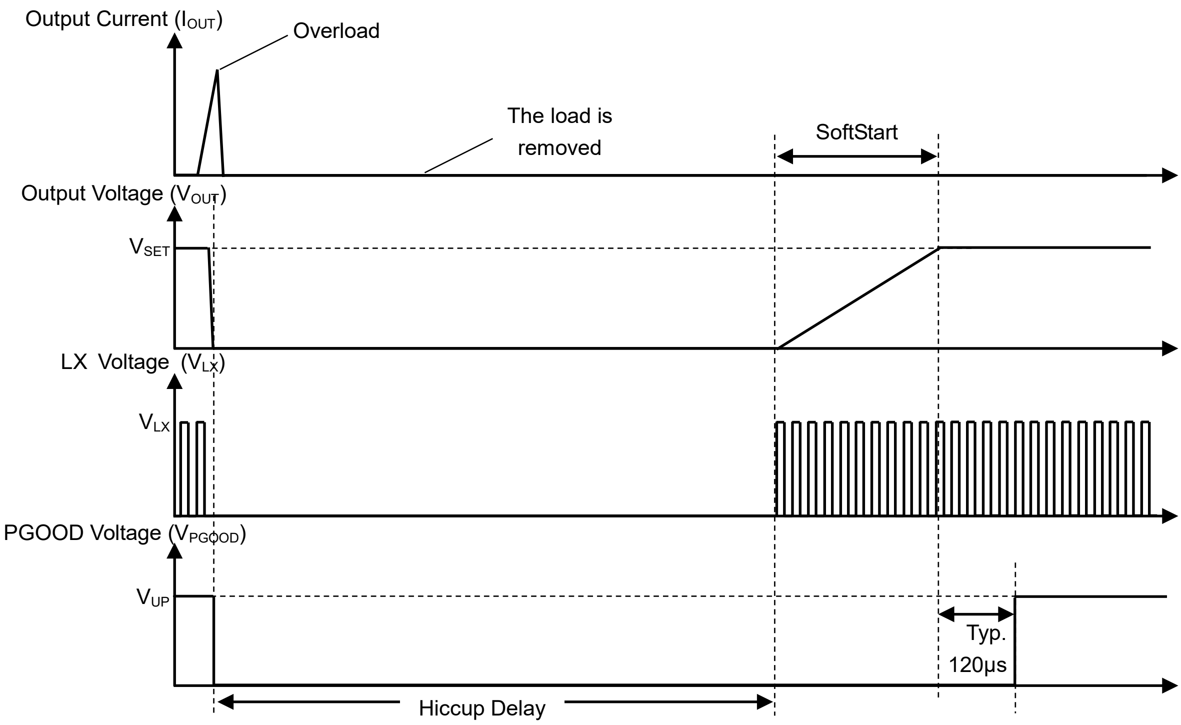
Hiccup-type / Latch-type Overcurrent Protection

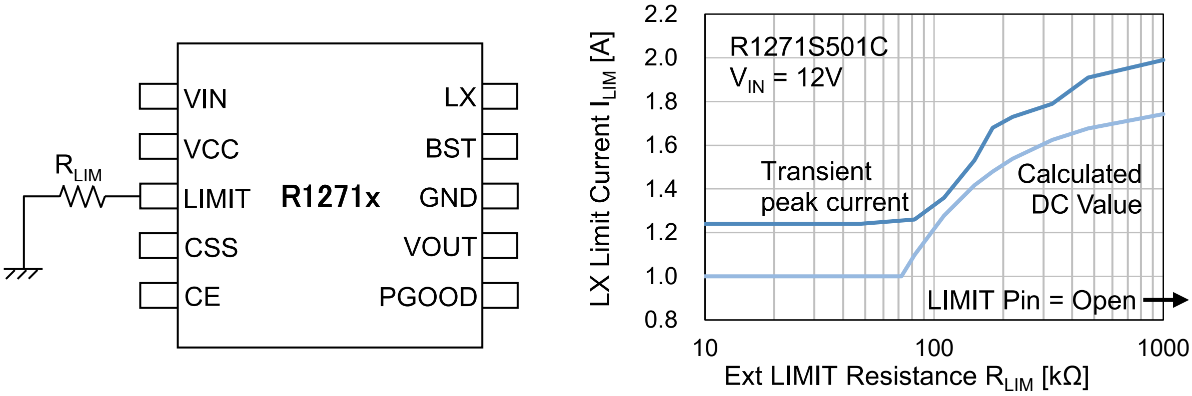
There are two types of overcurrent protection, the hiccup type and Latch type, and it works only if the VOUT open protection function or UVD works during current limit detection. The latch type holds the switching stopped after the overcurrent protection is activated. In order to release the latch state, it is necessary to restart the IC by setting the CE pin to "Low" or setting the VIN to the UVLO detection voltage or lower. After the overcurrent protection is activated, the hiccup type latches once to stop switching. Then, after a hiccup delay (Typ.7ms), a soft start is started. Since the Hi-Cup type automatically recovers after the overcurrent protection is activated, there is no need to switch the CE pin to "Low" / "High". In addition, there is no worry of destruction due to heat generation because a switching stop period of Typ.7ms is provided before restarting. After the overcurrent protection is activated, the hiccup type repeats restarting and latching until the cause of the overcurrent is eliminated. If the output is shorted to GND, it will be turned on and off repeatedly until the cause of the short circuit is eliminated.



Hiccup type overcurrent protection timing chart

Current Limit

The output current of the R1271x is limited by a peak current method. The current limit value is set to Typ. 1.8A (DC value) when the LIMIT pin is open. It can be adjusted to a minimum of Typ. 1.0A (DC value) with an external resistor. Current limit circuit operates by monitoring the drain - source voltage of a high-side MOSFET. The transient current limit of the inductor current is set to be higher than the DC value. Also, the larger the input / output voltage difference, the larger the difference between the transient current limit value of the inductor current and the DC current limit value. The current limit of the device starts operating after the minimum on-time, so it has to be careful especially when the device is used close to the minimum on-time because the current limit will increase.



Current limit adjustment by LIMIT pin resistor

Set R_{LIM} as follows.

R_{LIM} [kΩ] = -32 / (LIMSET / 1.8 - 1)

LIMSET : The setting limit current [A]

However, no matter how small the R_{LIM} is, it cannot be set to a LIMSET of 1 A or less.
The power consumption of R_{LIM} is 1mW or less.

Precautions for Current Limit of Function Under Operating in Low Input Voltage

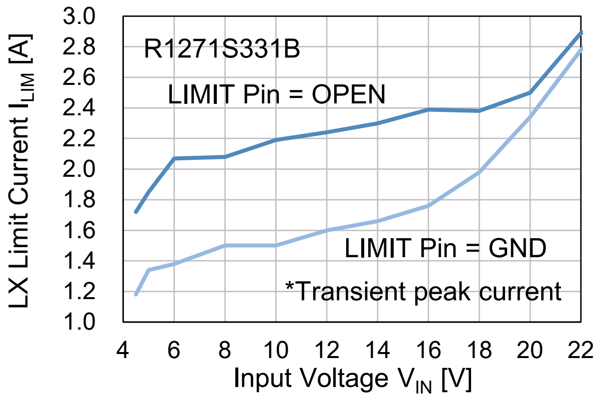
When using the R1271x with V_{IN} = 5 V or less, the load current may be limited in following two cases.

First Case: The device designed to reach current limit by monitoring the voltage difference between VIN and LX. During the low input voltage operation, the driving capability of high-side MOS FET decreases, so the voltage difference between VIN and LX becomes larger with smaller output current. Therefore, the load current may be limited during the low input voltage operation.

Second Case: During the low input voltage operation, the duty-over function decreases the oscillator frequency. While the oscillator frequency is 1/4 of the set frequency, drawing the load current can cause a voltage difference between the input and output. These make the device to exit from duty-over condition, and as a result, the output voltage drops.

Both cases show that the current limit is depending on the input voltage and load current. Careful consideration is required when applying a heavy load while the input voltage is low. The following graph shows the relation between input voltage and load current.

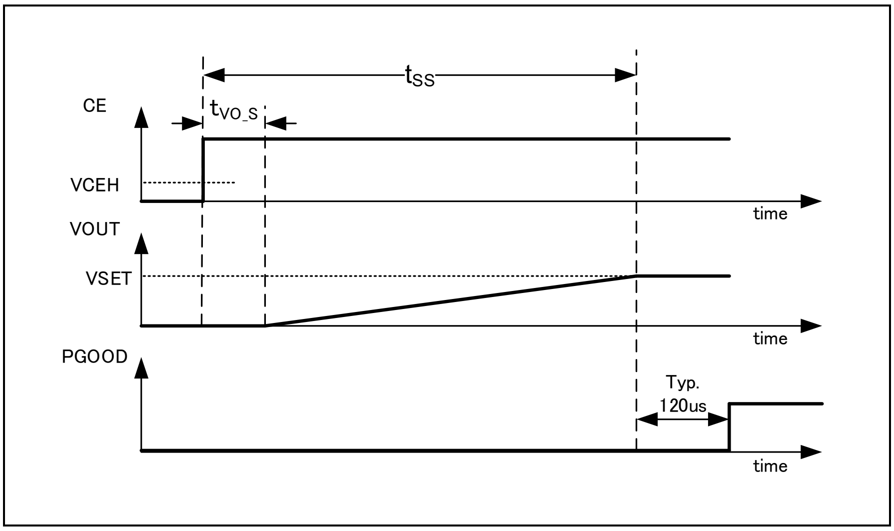
If the BST voltage between BST and LX drops extremely, the device forcibly turns off the switching to charge the BST voltage to prevent a malfunction of internal logic. This function may operate when V_{IN} = 4.5 V or less and it affects the output voltage ripple. Also, under the condition that V_{IN} = 4.5 V or less and the undervoltage is detected as the output voltage decreases, the hiccup or latch type protection may work by the protection function in the IC.



R1271x Current Limit vs. Input Voltage (VOUT = 3.3 V)

Soft-start Adjustment

The soft-start time is a time between a rising edge (“High” level) of the CE pin and the timing when the output voltage reaches the set output voltage.



Soft start sequence

Connecting a capacitor (C_{SS}) to the CSS pin can adjust the soft-start time (t_{SS}) – provided the internal soft-start time of Typ.500 µs as a lower limit. The adjustable soft-start time (t_{SS2}) is Typ.1.6 ms when connecting an external capacitor of 4.7 nF with the charging current of Typ.2.0 µA and Typ.0.64 V.

Soft-start time

(T_{SS})[ms] = Css[nF] / 2 × 0.64 + 0.16

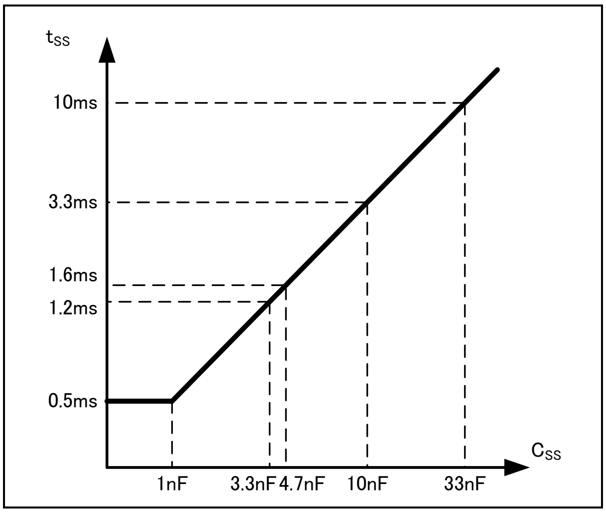
When C_{SS} = 4.7 nF

T_{SS} = 4.7 / 2 × 0.64 + 0.16 = 1.6 [ms]

If not required to adjust the soft-start time, set the CSS pin to “Open” to enable the internal soft-start time (t_{SS1}) of Typ.500 µs.

When a large-capacitance output capacitor is connected, the overcurrent or LX ground fault protection may work due to an inflow of large current at startup. Thus, set a longer soft start time to reduce the amount of current and prevent from operating the protections due to the rapid startup.

Soft-start time of t_{ss1} when CSS pin is "Open, and t_{ss2} when C_{SS} = 4.7 nF are guaranteed under the conditions described in the chapter of “Electrical Characteristics”



C_{SS} [nF] = (t_{SS} – t_{VO_S}) / 0.64 × 2.0

t_{SS}: Soft-start time (ms)

t_{VO_S}: Time period from CE = "High" to VOUT's rising (Typ. 0.160 ms)

Soft-start Time Adjustment Capacitor vs Soft-start Time

VOUT Open Protection

When V_{OUT} is lower than Typ.0.6 V or less at soft start completion, VOUT pin is recognized "OPEN" and the hiccup-type or Latch-type protection is activated.

Reverse Current Limit

The reverse current limit start operating when the reverse current flowing through the low-side MOSFET exceeds the set reverse current threshold. It turns off the low-side MOSFET to control the reverse current. The reverse current limit is Typ. 1A. This function operates when the output voltage is pulled-up to more than the set output voltage due to the short circuit.

Thermal Shutdown Function

When the junction temperature exceeds the thermal shutdown detection threshold (Typ. 160°C), R1271x cuts off the output from DC/DC and suppresses the self-heating. When the junction temperature falls below the thermal shutdown release threshold (Typ. 140°C), the IC will restart with the soft start operation.

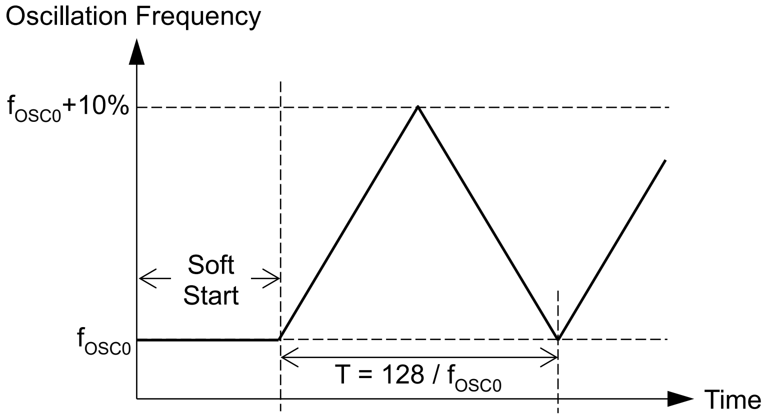
SSCG (Spread Spectrum Clock Generator)

In order to reduce the interference of conductive / radioactive noise, R1271x has prepared a version in which the SSCG (Spread Spectrum Clock Generator) function is enabled during PWM operation.

SSCG suppresses noise peaks and average noise at specific frequencies by spreading the oscillation frequency over a wide band.

In this version, the oscillation frequency (f_{OSC0}) changes in a triangular wave shape in the range of Typ. + 10% of the set frequency from the set frequency. The modulation period is f_{OSC0} / 128.Triangular wave modulation cannot be maintained during duty over and pulse skip operations, which are functions for maintaining the output voltage.

Also, at soft start, the oscillation frequency is not modulated and operates at the set frequency.



SSCG frequency fluctuation diagram

Precautions for Selecting External Components

Inductor

Select a product that has a small DC resistance, a sufficient rated current, and is resistant to magnetic saturation. DC resistance affects efficiency. In case that the inductance value of an inductor is extremely small, the peak current of LX may increase along with the load current. As a result, the current limit circuit may unexpectedly work.

Capacitor

- Select a capacitor that has a sufficient margin to the drive voltage ratings with consideration of the DC bias characteristics and the temperature characteristics.
- Ceramic capacitors are recommended for the input capacitor (C_{IN}) and the output capacitor (C_{OUT}). The combined use of a ceramic capacitor and an electrolyte capacitor is also available. When using an electrolyte capacitor, select it with the lowest possible ESR in consideration of the allowable ripple current rating (I_{RMS}). I_{RMS} can be calculated by the following equation.

$$I_{RMS} \fallingdotseq I_{OUT} / V_{IN} \times \sqrt{\{ V_{OUT} \times (V_{IN} - V_{OUT}) \}}$$

The electrolyte capacitor has a characteristic of increasing ESR when it is at a low temperature, so careful consideration is required to make enough phase compensation in case of using an electrolyte capacitor for C_{OUT}.

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TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

- External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.
- Place a capacitor (C_{BST}) as close as possible to the LX pin and the BST pin.
- The tab on the bottom of the package must be connected to GND when mounted on the board. To improve thermal dissipation on the multilayer board, surface, secure the GND layer as large as possible and set via to release the heat to the other layer in the connecting part of the tab on the bottom.
- It is recommended that NC pin left open to prevent failure caused by adjacent pins' short circuit.
- If V_{OUT} is forced negative voltage before start-up, the IC may not be able to ramp up.
- Make the wiring between the LX pin and the inductor as short as possible to reduce the parasitic capacitance.
- Place the input capacitor (C_{IN}) on the same side of the IC. If it is placed on the different side of the IC by using via, the parasitic inductance of the via may increase the noise.
- Feedback the output voltage from the closest point of C_{OUT}.
- Thermal shutdown function is designed for preventing risk of smoke and fire. The function does not have the effect under the input over voltage or damaged by beyond the absolute maximum rating condition.
- Do not design with depending on the thermal shutdown function as the system protection. The thermal shutdown function is designed for the IC.

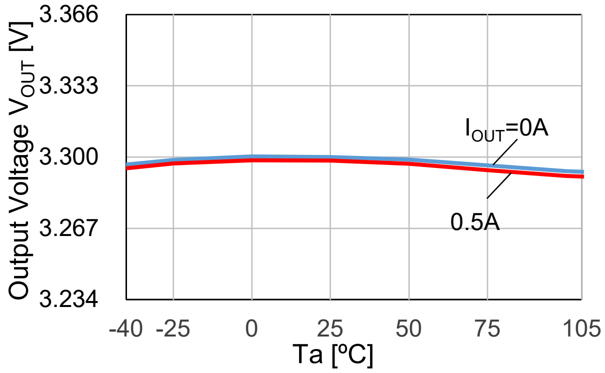
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

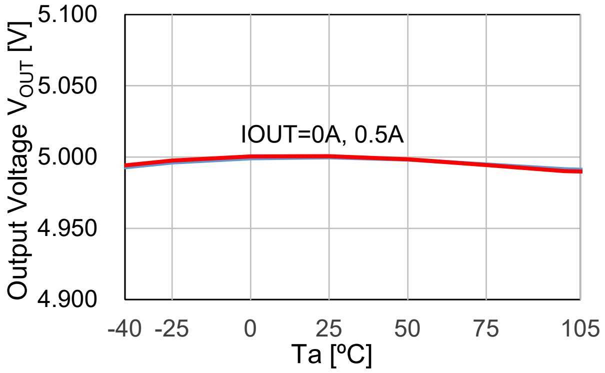
1) Output Voltage vs Temperature

V_{IN} = 12 V

V_{SET} = 3.3 V



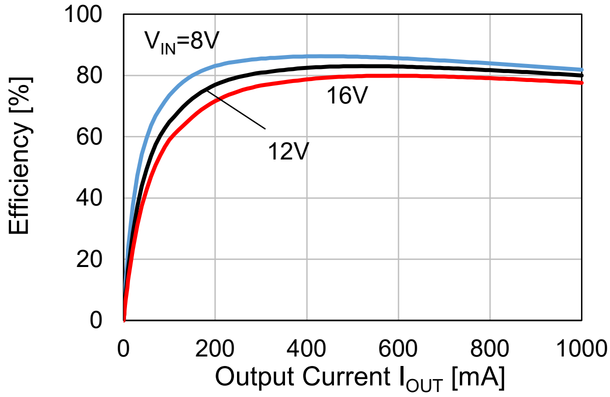
V_{SET} = 5.0 V



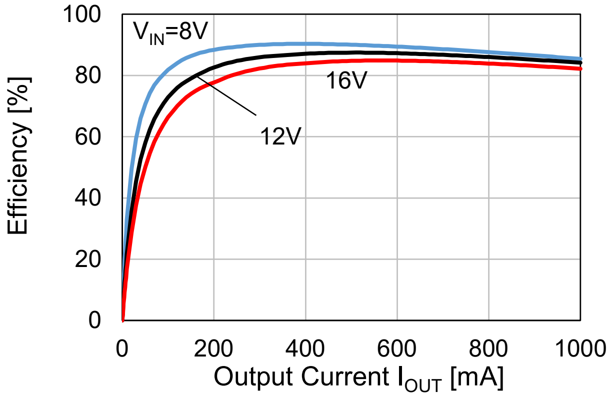
2) Efficiency

Ta = 25 ºC

V_{SET} = 3.3 V



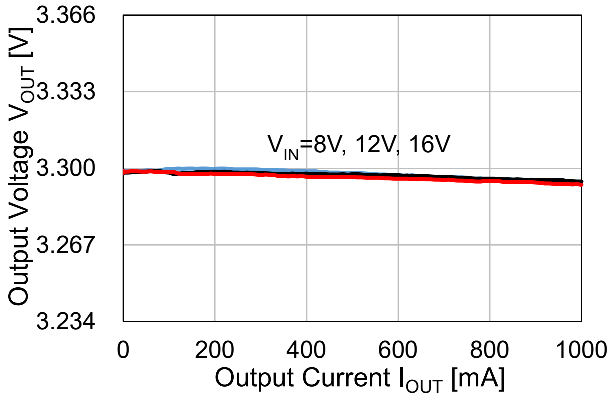
V_{SET} = 5.0 V



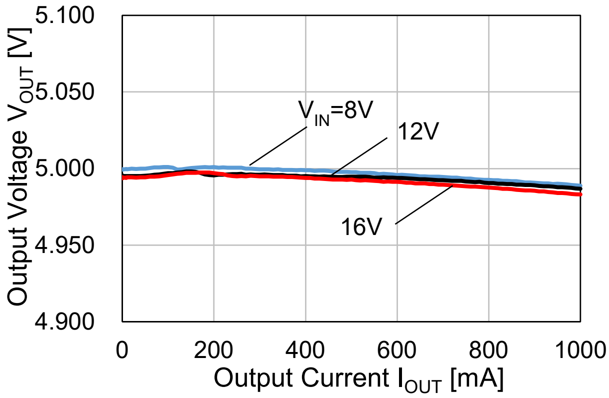
3) Load Regulation

Ta = 25 ºC

V_{SET} = 3.3 V



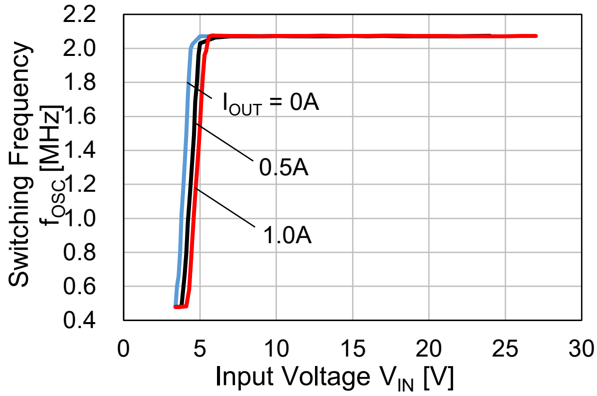
V_{SET} = 5.0 V



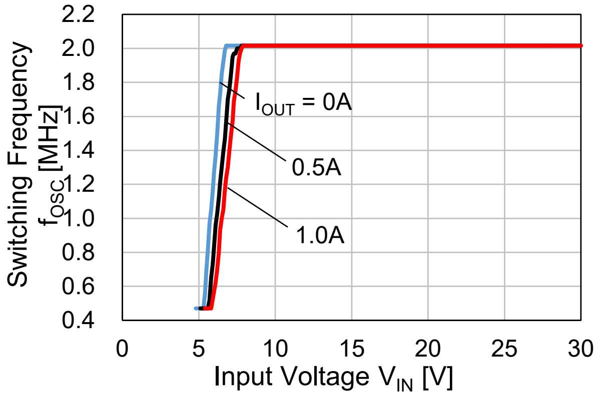
4) Switching Frequency vs Input Voltage

Ta = 25 °C

V_{SET} = 3.3 V



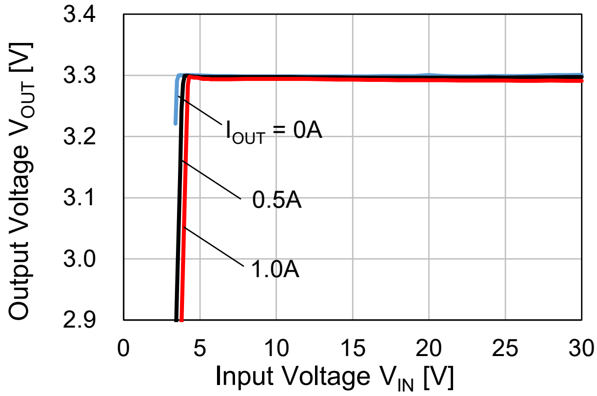
V_{SET} = 5.0 V



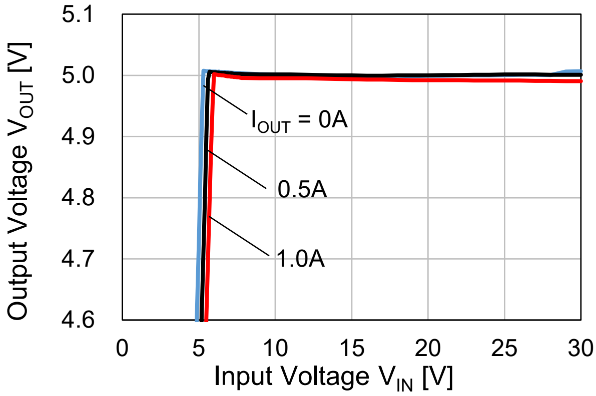
5) Output Voltage vs Input Voltage

Ta = 25 °C

V_{SET} = 3.3 V



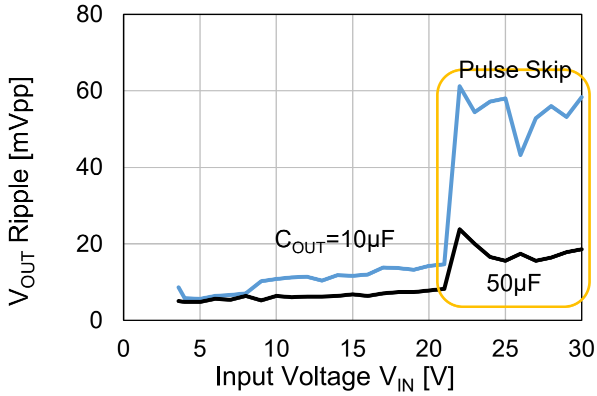
V_{SET} = 5.0 V



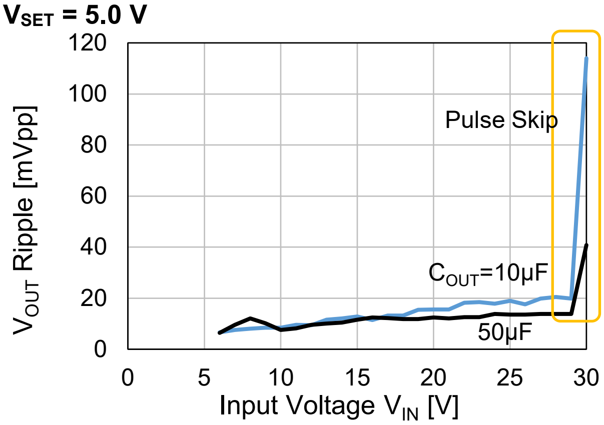
6) V_{OUT} Ripple vs Input Voltage

I_{OUT} = 0 A, Ta = 25 °C

V_{SET} = 3.3 V



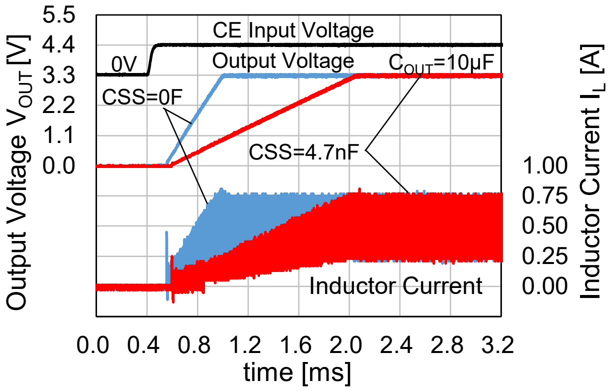
V_{SET} = 5.0 V



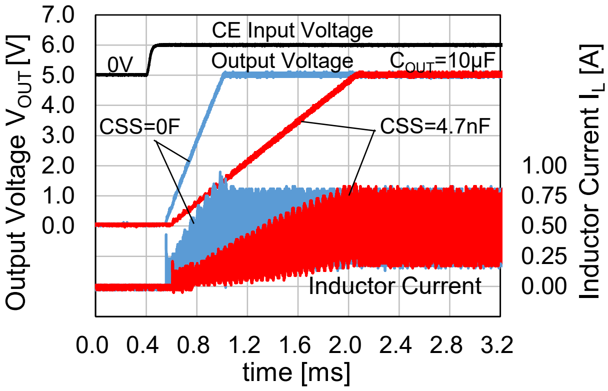
7) Start up by CE

V_{IN} = 12 V, I_{OUT} = 0.5 A, Ta = 25 °C

V_{SET} = 3.3 V



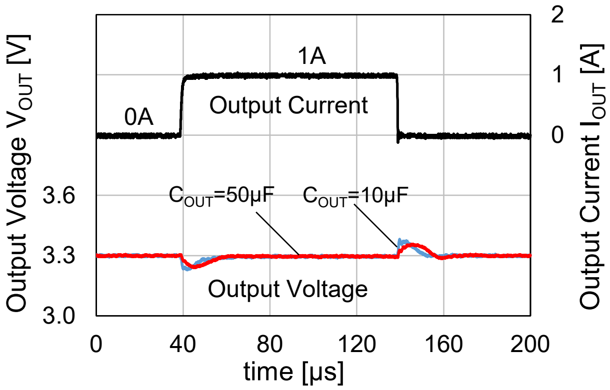
V_{SET} = 5.0 V



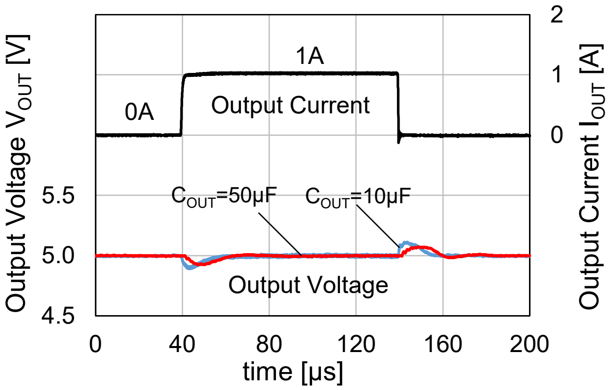
8) Load Transient Response

V_{IN} = 12 V, Ta = 25 °C

V_{SET} = 3.3 V



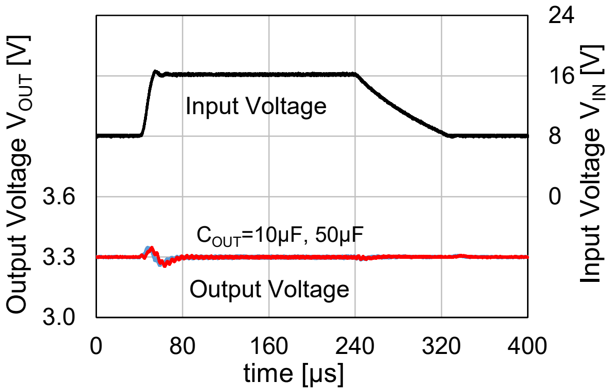
V_{SET} = 5.0 V



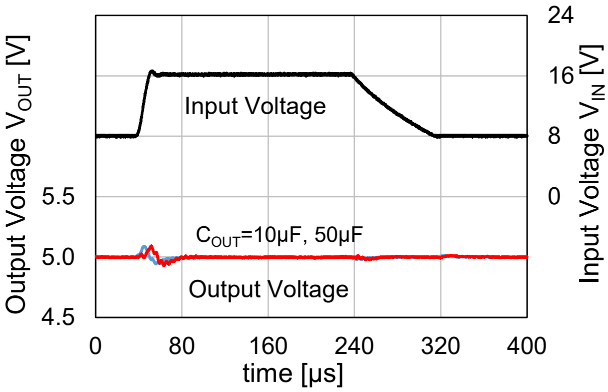
9) Line Transient Response

I_{OUT} = 0.5 A, Ta = 25 °C

V_{SET} = 3.3 V



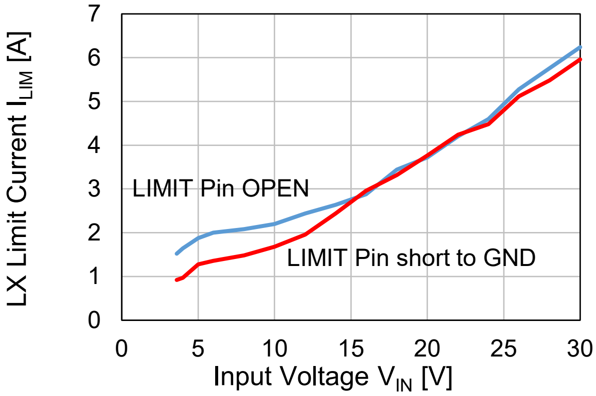
V_{SET} = 5.0 V



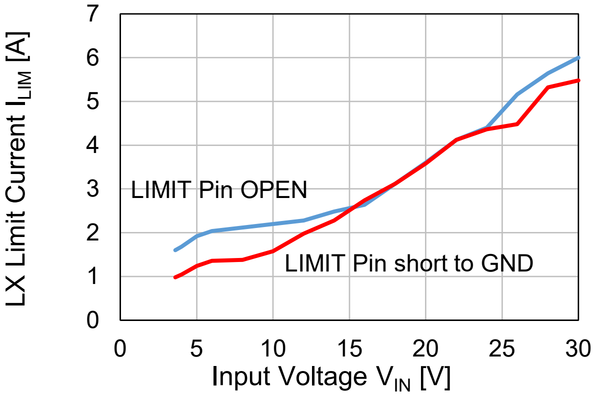
10) Limit Current vs Input Voltage

Ta = 25 ºC

V_{SET} = 3.3 V



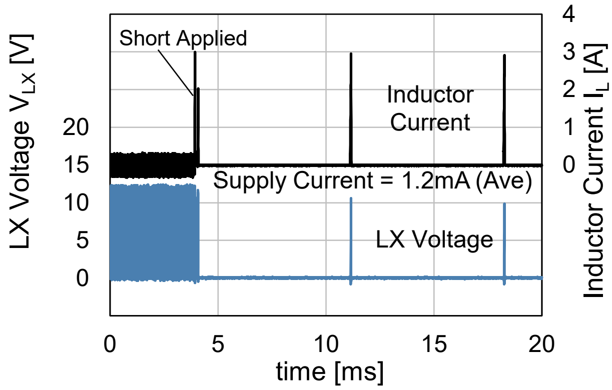
V_{SET} = 5.0 V



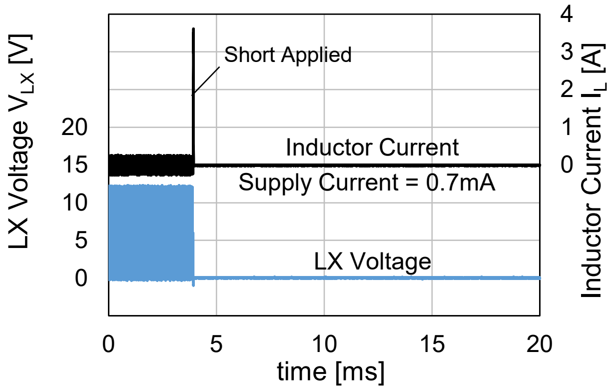
11) Short Circuit Transient

V_{IN} = 12 V, Ta = 25 ºC

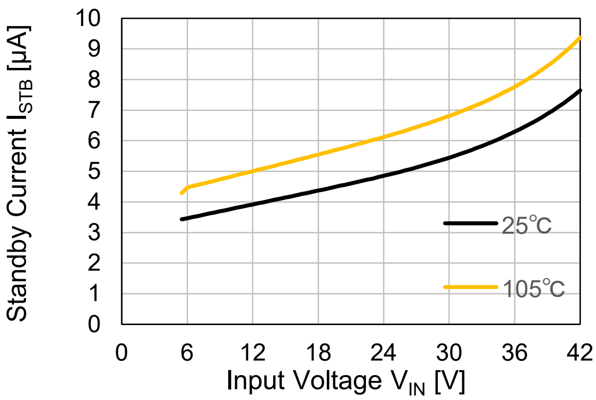
R1271S501C (HICCUP)



R1271S331B (LATCH)

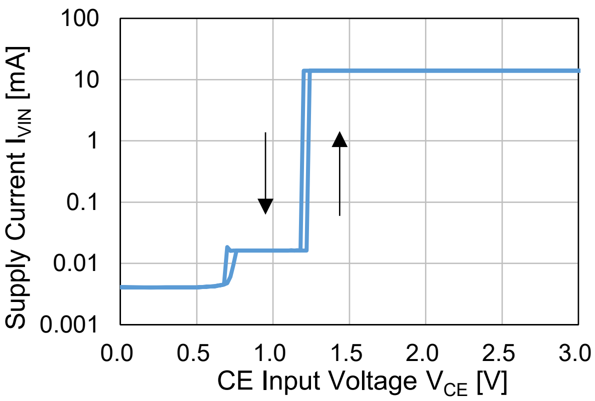


12) Standby Current vs Input Voltage



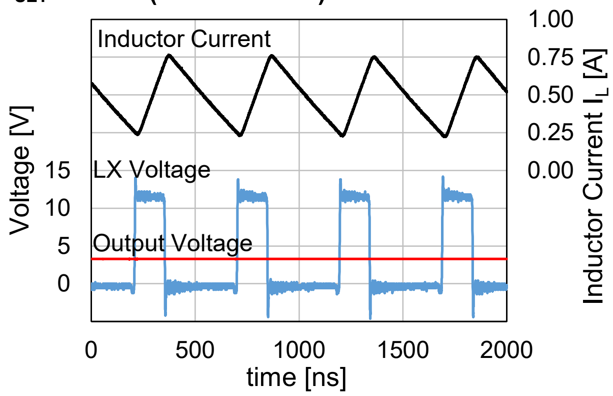
13) Supply Current vs CE

V_{IN} = 12 V, Ta = 25 ºC

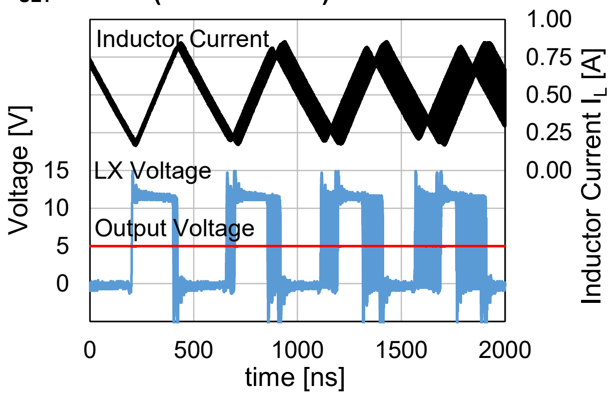


14) Typical Switching
V_{IN} = 12 V, I_{OUT} = 0.5 A, Ta = 25 °C

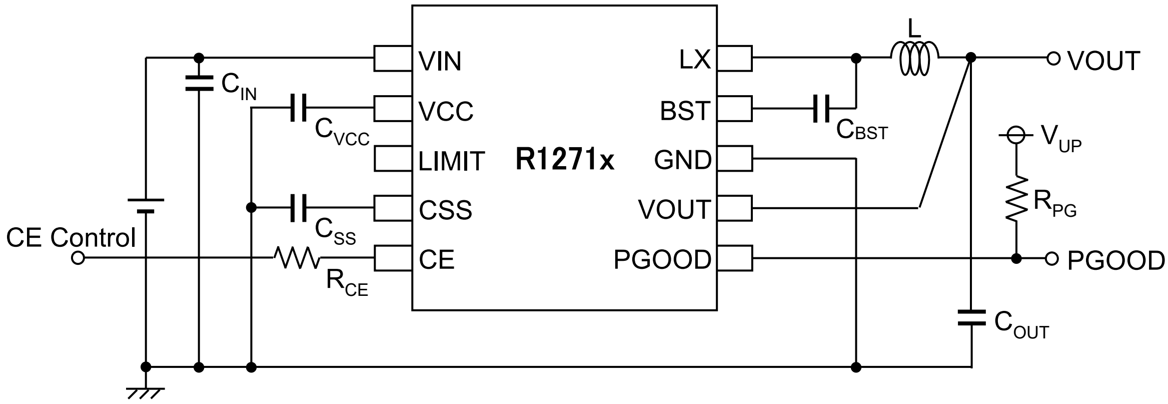
V_{SET} = 3.3 V (R1271S331B)



V_{SET} = 5.0 V (R1271S501C) SSCG Enable



Test Circuit



R1271x Test Circuit for Typical Characteristics

Measurement Components for Typical Characteristics

Symbol	Capacitance	Parts number	Maker
C_{IN}	10 μF	CGA5L1X7R1H106K	TDK
C_{OUT}	10 μF	CGA5L1X7R1H106K	TDK
C_{BST}	0.1 μF	CGA2B1X7R1C104K	TDK
C_{VCC}	1.0 μF	CGA3E1X7R1V105K	TDK

Symbol	Inductance	Parts number	Maker
L	2.2 μH	TFM252012ALVA2R2MTAA	TDK

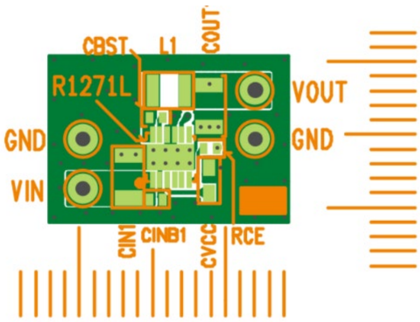
We recommend 1 kΩ or more for R_{CE} and 10 kΩ or more for R_{PG}.

APPLICATION INFORMATION

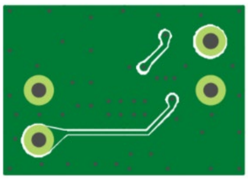
PCB LAYOUT

R1271L (Package:：DFN3030-12) PCB Layout

Top Layer

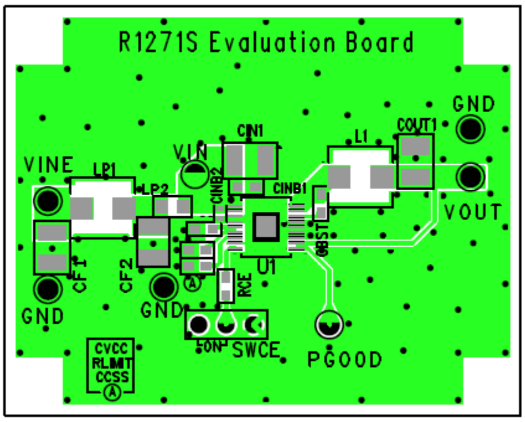


Bottom Layer

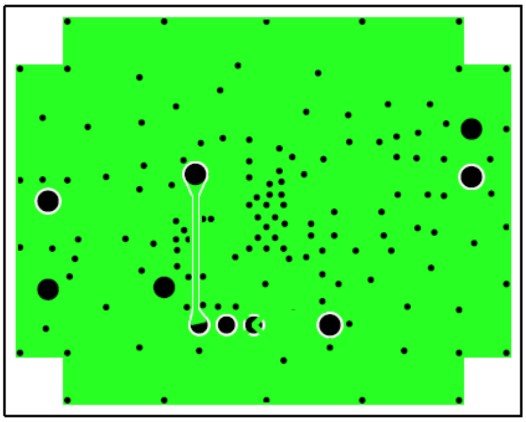


R1271S (Package：HSOP-18) PCB Layout

Top Layer



Bottom Layer



PD-DFN3030-12B-(105125)-JE-A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

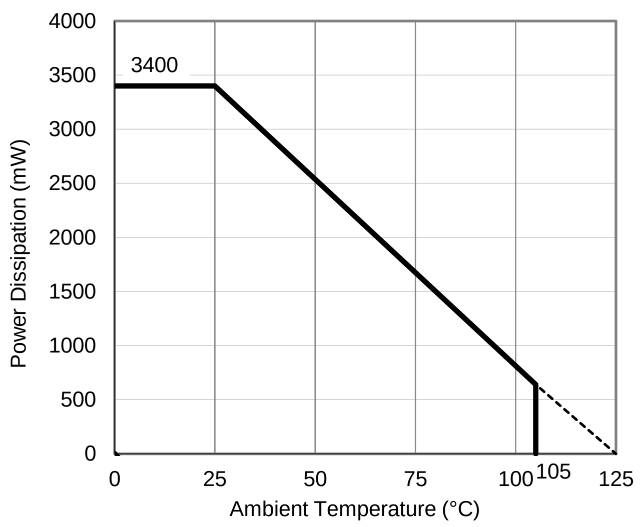
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 32 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

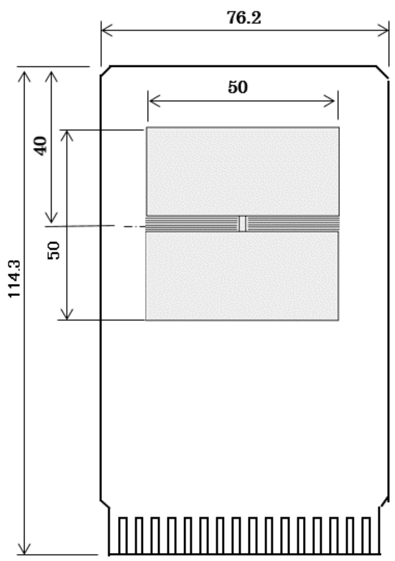
Item	Measurement Result
Power Dissipation	3400 mW
Thermal Resistance (θja)	θja = 29°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 3.1°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

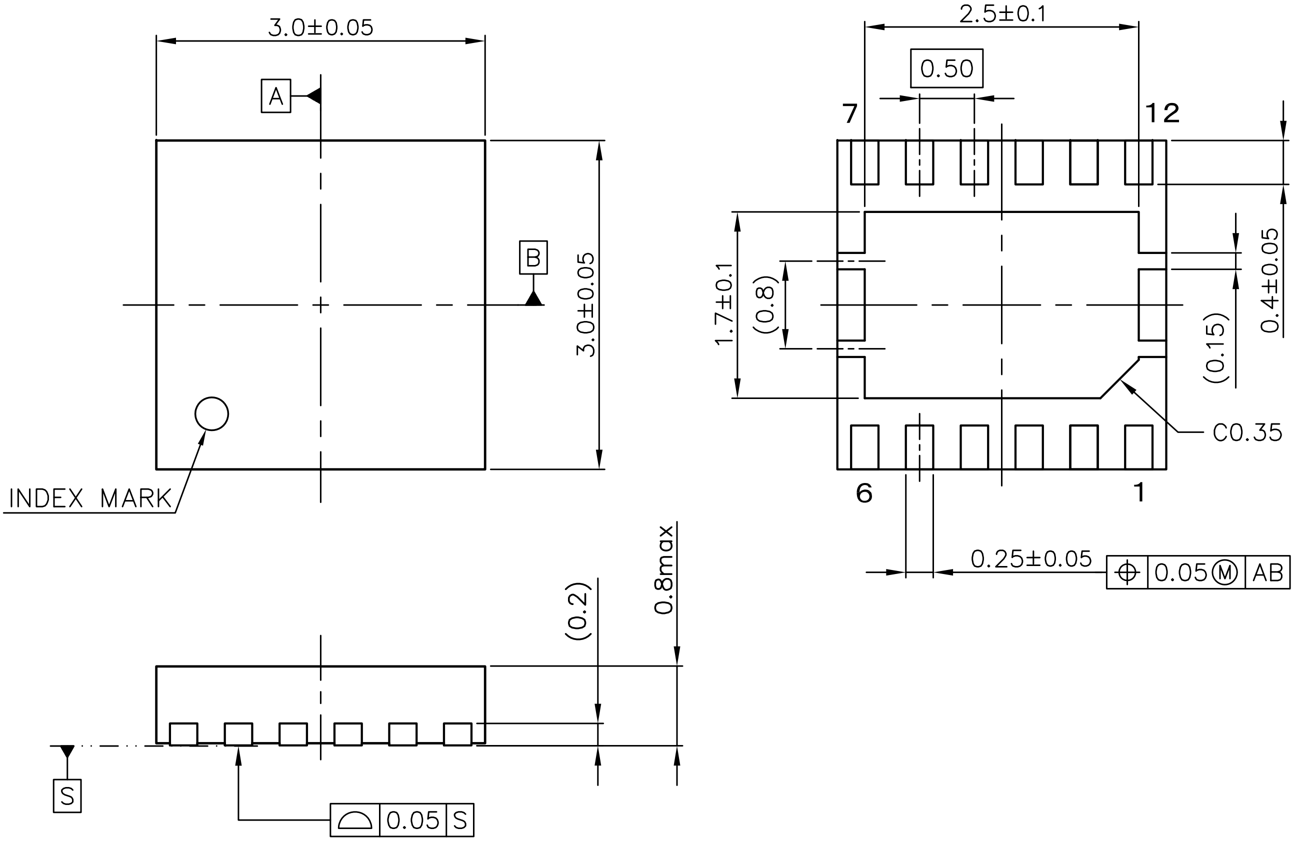


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH



DFN3030-12B Package Dimensions (Unit: mm)

PD-HSOP-18-(105125)-JE-C

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

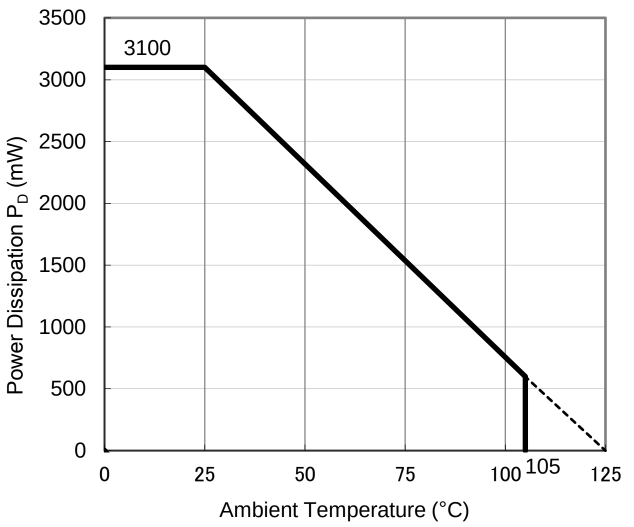
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

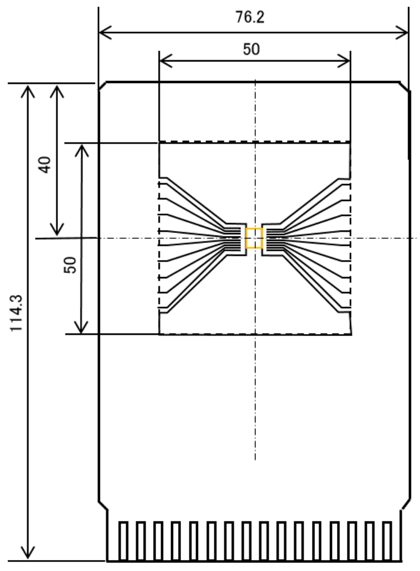
Item	Measurement Result
Power Dissipation	3100 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

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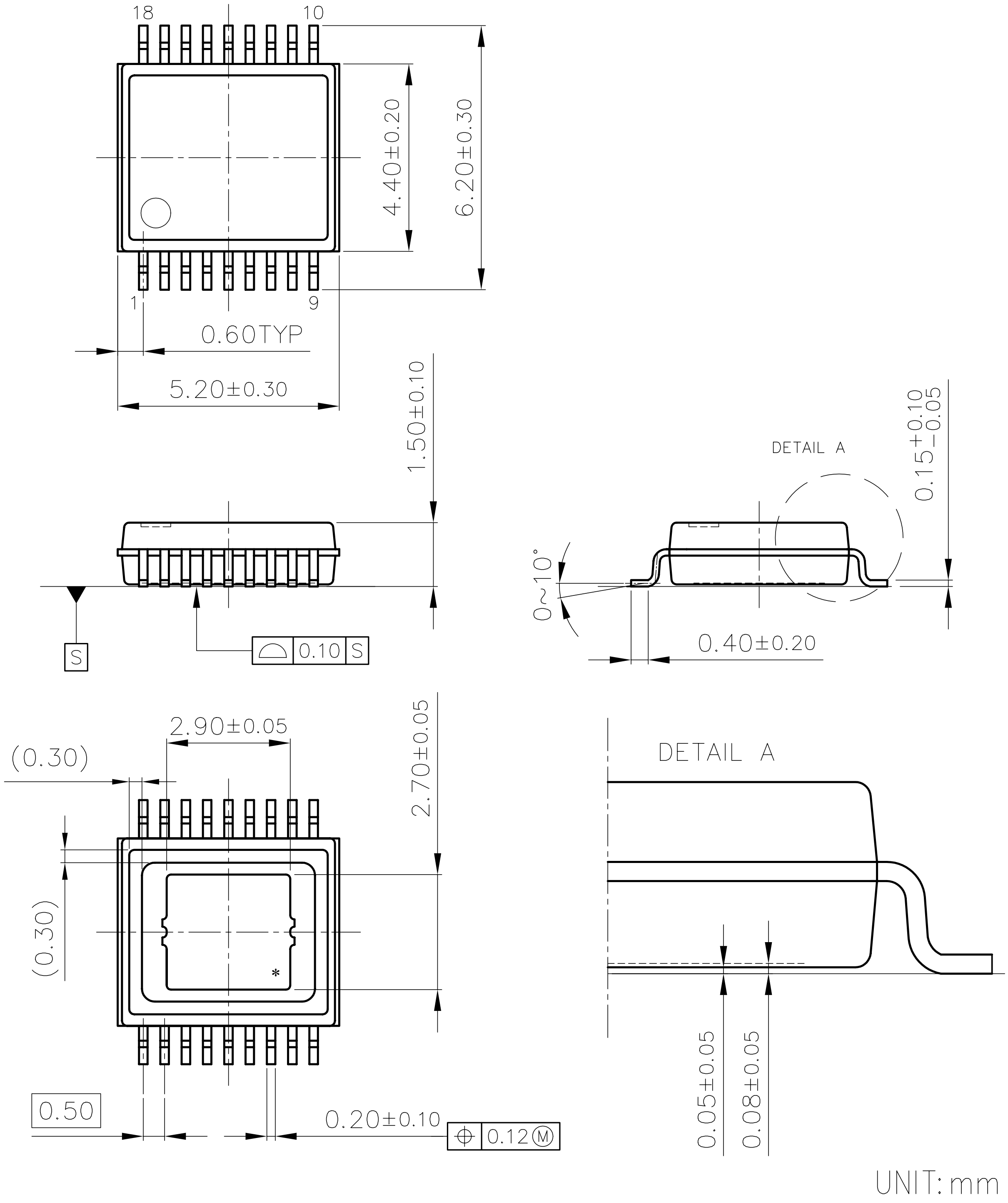
DM-HSOP-18-JE-B



HSOP-18 Package Dimensions

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