30 V, 3 A Synchronous Step-down DC/DC Converter

No. EA-404-201112

OVERVIEW

The R1276S is a 36-V rated synchronous step-down DC/DC converter with built-in transistor. Under cranking condition, the switching frequency is automatically reduced to keep output voltage level constant.

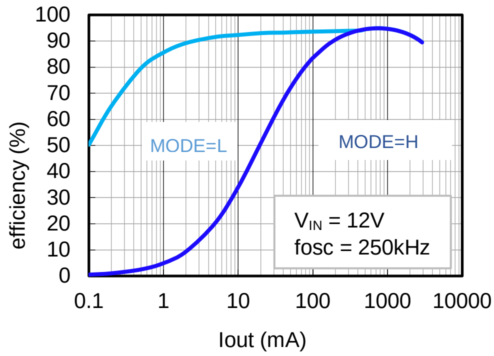
KEY BENEFITS

- High efficiency of 95%
- Maintains the output voltage constant at cranking by reducing a switching frequency to the minimum 1/4.
- Achieves the EMI noise reduction by using a spread spectrum clock generator. (Diffusion Rate: +10%).

KEY SPECIFICATIONS

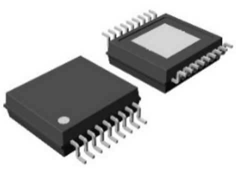
- Input Voltage Range (Maximum Ratings): 3.6 V to 30 V (36 V)
- Start-up Voltage: 4.5 V
- Standby Current: Typ. 4 µA
- Output Voltage Range: 0.7 V to 6.5 V
- Feedback Voltage: 0.64 V ±1.0%
- Consumption Current at No Load (at VFM mode): Typ. 12 µA
- Adjustable Oscillator Frequency Using External Resistors: 250 kHz to 1 MHz(1)
- External Synchronous Clock Frequency: 250 kHz to 1 MHz
- Spread Spectrum Clock Generator (SSCG): Diffusion Rate Typ. +10%
- Minimum ON-Time: Typ. 70 ns
- Minimum OFF-Time: Typ. 120 ns
- Duty-over: Min. 1/4
- Soft-start
- Thermal Shutdown: Tj = 160°C
- Undervoltage Lockout (UVLO): V_{CC} = 3.3 V (Typ.)
- Overvoltage Lockout (OVLO): V_{IN} = 35 V (Typ.)
- Overvoltage Detection (OVD): FB Pin Voltage (V_{FB}) +10%
- LX Current Limiting: Typ. 4.2 A
- Over-current Protection: Hiccup-type
- High-side Transistor ON Resistance: Typ.0.145 Ω
- Low-side Transistor ON Resistance: Typ. 0.095 Ω

TYPICAL CHARACTERISTICS



Efficiency (V_{OUT} = 5 V)

PACKAGE



HSOP-18

5.2 x 6.2 x 1.45 (mm)

OPTIONAL FUNCTIONS

Select the optional functions from below.

Product Name	Output voltage range
R1276S001*	3.15 V < V_{OUT} ≤ 6.0 V
R1276S002*	6.0 V < V_{OUT} ≤ 6.5 V
R1276S004*	0.7 V ≤ V_{OUT} ≤ 3.15 V

Product Name	Over-current Protection	SSCG
R1276SxxxA	Hiccup-type	Disable
R1276SxxxC	Hiccup-type	Enable

APPLICATIONS

- Digital Electronics: Digital TVs, DVD Players
- OA Equipment: Printers, Facsimiles
- Portable Communication Equipment, Cameras, Video Cameras
- Battery-powered Equipment

(1) The adjustable oscillation frequency range becomes 250 kHz ≤ f_{OSC} ≤ 600 kHz when 0.7 V ≤ V_{OUT} < 3.3 V.

SELECTION GUIDE

The Output voltage range, the Optional functions and Quality class are user-selectable.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1276Sxxx*-E2-FE	HSOP-18	1,000 pcs	Yes	Yes

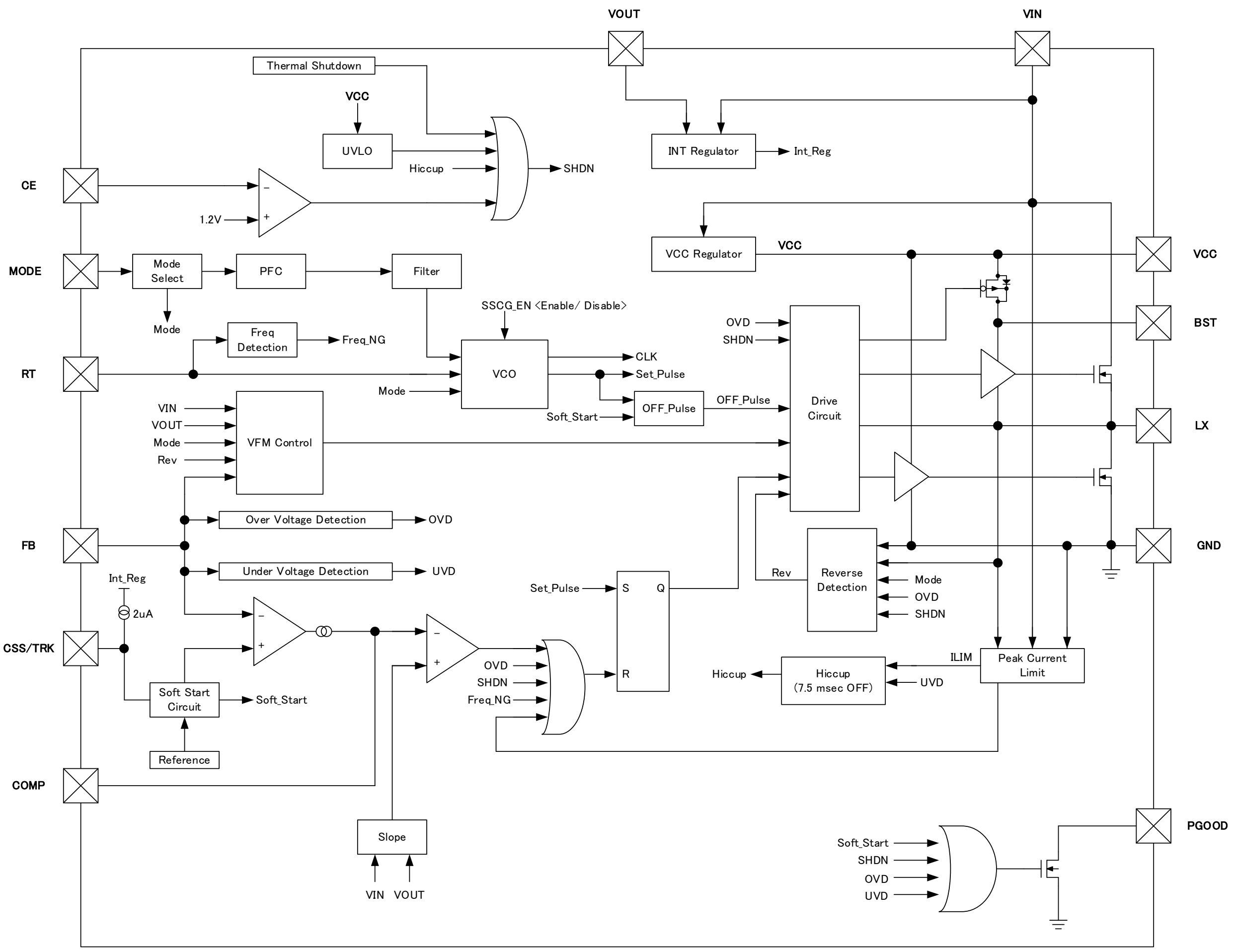
xxx : Select an output voltage range from below.

xxx	Output voltage range
001	3.15 V < V_{OUT} ≤ 6.0 V
002	6.0 V < V_{OUT} ≤ 6.5 V
004	0.7 V ≤ V_{OUT} ≤ 3.15 V

* : Select an optional function from below.

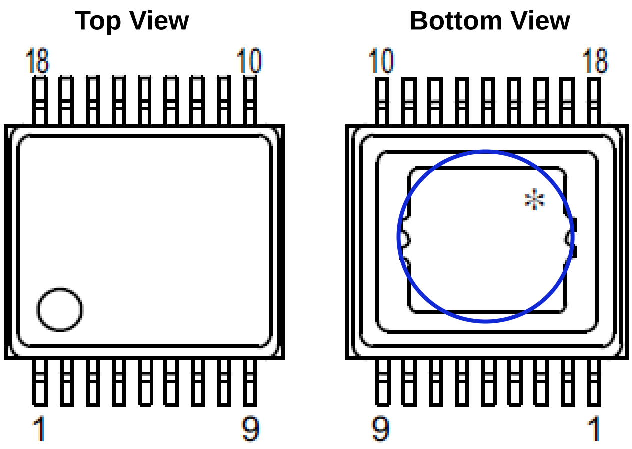
*	Over-current Protection	SSCG
A	Hiccup-type	Disable
C	Hiccup-type	Enable

BLOCK DIAGRAM



R1276S Block Diagram

PIN DESCRIPTIONS



R1276S (HSOP-18) Pin Configuration

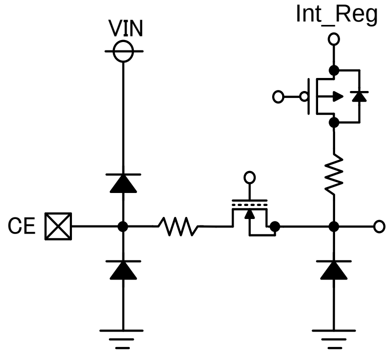
∗ The tab on the bottom of the package is substrate level (GND). It must be connected to the ground plane on the board.

R1276S Pin Descriptions

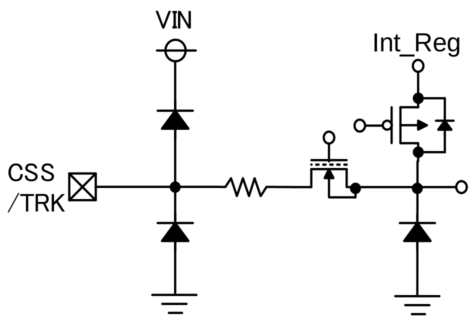
Pin No.	Pin Name	Description
1, 2	VIN[1]	Power Supply Pin
3	NC	Not Connected
4	CE	Chip Enable Pin, Active-high
5	CSS/TRK	Soft-start Adjustment Pin
6	COMP	Capacitor Connecting Pin for Error Amplifier's Phase Compensation
7	FB	Feedback Input Pin for Error Amplifier
8	PGOOD	Power Good Output Pin
9	VOUT	Output Voltage Feedback Input Pin
10	MODE	Mode Setting Input Pin
11	RT	Oscillator Frequency Adjustment Pin
12	VCC	VCC Output Pin
13	BST	Bootstrap Pin
14, 15, 16	GND[1]	GND Pin
17	NC	Not Connected
18	LX	Switching Pin

(1) The pins with the same name should be connected together.

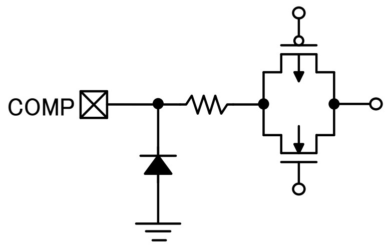
Equivalent Circuits for the Individual Terminals



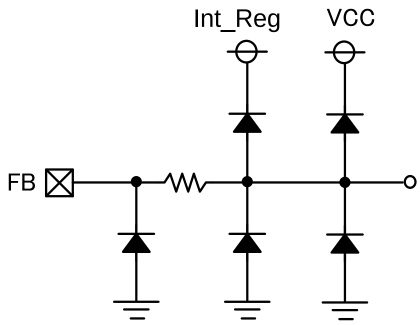
Equivalent Circuit for CE Pin



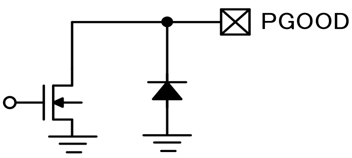
Equivalent Circuit for CSS/TRK Pin



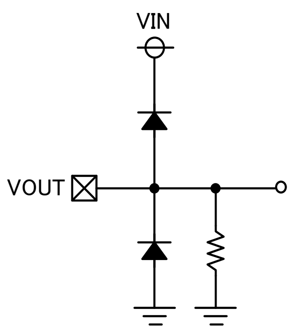
Equivalent Circuit for COMP Pin



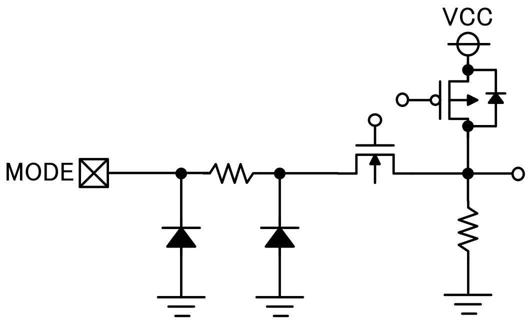
Equivalent Circuit for FB Pin



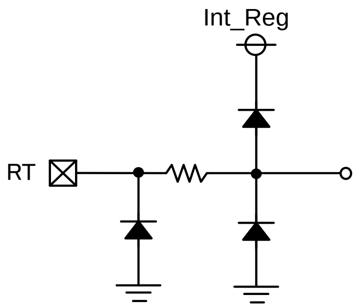
Equivalent Circuit for PGOOD Pin



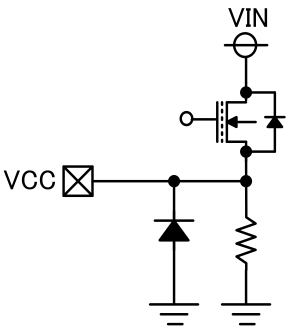
Equivalent Circuit for VOUT Pin



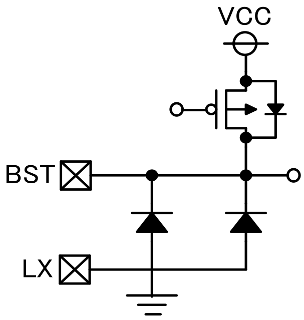
Equivalent Circuit for MODE Pin



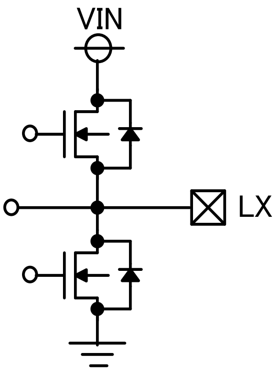
Equivalent Circuit for RT Pin



Equivalent Circuit for VCC Pin



Equivalent Circuit for BST Pin



Equivalent Circuit for LX Pin

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Pin Input Voltage	−0.3 to 36	V
V_{CE}	CE Pin Voltage(1)	−0.3 to V_{IN}+0.3 ≤ 36	V
$V_{CSS/TRK}$	CSS/TRK Pin Voltage	−0.3 to 3	V
V_{OUT}	VOUT Pin Voltage	−0.3 to 16	V
V_{RT}	RT Pin Voltage	−0.3 to 3	V
V_{COMP}	COMP Pin Voltage(2)	−0.3 to 6	V
V_{FB}	FB Pin Voltage	−0.3 to 3	V
V_{CC}	VCC Pin Voltage	−0.3 to 6	V
	VCC Pin Output Current	Internally Limited	mA
V_{BST}	BST Pin Voltage	LX−0.3 to LX+6	V
V_{LX}	LX Pin Voltage(1)	−0.3 to V_{IN} +0.3 ≤ 36	V
V_{MODE}	MODE Pin Voltage	−0.3 to 6	V
V_{PGOOD}	PGOOD Pin Voltage	−0.3 to 6	V
P_D	Power Dissipation	Refer to Appendix *"POWER DISSIPATION"*	
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	Operating Input Voltage	3.6 to 30	V
Ta	Operating Temperature Range	−40 to 105	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) It should not exceed V_{IN} + 0.3 V.
(2) It should not exceed V_{CC} + 0.3 V.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, V_{CE} = V_{IN}, unless otherwise specified.

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

R1276S Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
V_{START}	Start-up Voltage					4.5	V
V_{CC}	VCC Pin Voltage (VCC-GND)		V_{FB} = 0.672 V, V_{MODE} = 5 V	4.75	5	5.25	V
$I_{STANDBY}$	Standby Current		V_{IN} = 30 V, V_{CE} = 0 V		4	30	µA
I_{VIN1}	VIN Consumption Current 1 at PWM switching stop	R1276S001x R1276S002x	V_{FB} = 0.672 V, V_{MODE} = 5 V, V_{OUT} = V_{LX} = 5 V		1.0	1.35	mA
		R1276S004x	V_{FB} = 0.672 V, V_{MODE} = 5 V, V_{OUT} = V_{LX} = 1.5 V		1.6	1.95	
I_{VIN2}	VIN Consumption Current 2 at VFM switching stop	R1276S001x R1276S002x	V_{FB} = 0.672 V, V_{MODE} = 0 V, V_{OUT} = V_{LX} = 5 V		12	60	µA
		R1276S004x	V_{FB} = 0.672 V, V_{MODE} = 0 V, V_{OUT} = V_{LX} = 1.5 V		42	92	
V_{UVLO1}	Undervoltage Lockout (UVLO) Threshold		V_{CC}, Falling	3.1	3.3		V
V_{UVLO2}			V_{CC}, Rising		4.3	4.5	V
V_{OVLO1}	Overvoltage Lockout (OVLO) Threshold		V_{IN}, Rising	33.6	35	36	V
V_{OVLO2}			V_{IN}, Falling	32	34		V
V_{FB}	FB Voltage Accuracy		Ta = 25°C	0.6336	0.64	0.6464	V
			−40°C ≤ Ta ≤ 105°C	0.6272		0.6528	
$f_{OSC}0$	Oscillator Frequency 0		R_{RT} = 121 kΩ	225	250	275	kHz
$f_{OSC}1$	Oscillator Frequency 1		R_{RT} = 29 kΩ	900	1000	1100	kHz
f_{SYNC}	Synchronizing Frequency		f_{OSC} reference when 250kHz ≤ f_{SYNC} ≤ 1MHz	f_{OSC}x0.5		f_{OSC}x1.5	kHz
t_{SS1}	Soft-start Time 1		$V_{CSS/TRK}$ = “OPEN”	0.36		0.75	ms
t_{SS2}	Soft-start Time 2		$V_{CSS/TRK}$ = 4.7 nF	1.4		2	ms
I_{TSS}	Soft-start Pin Charging Current		$V_{CSS/TRK}$ = “GND”	1.8	2	2.2	µA
V_{SSEND}	CSS/TRK Pin Voltage at soft-start stop			V_{FB}	V_{FB} +0.03	V_{FB}+0.06	V
R_{DIS_CSS}	CSS/TRK Pin Discharge Resistance		V_{IN} = 4.5 V, V_{CE} = 0 V, $V_{CSS/TRK}$ = 3 V		2	5	kΩ
$I_{LXLIMIT}$	LX Current Limiting		High-side Transistor, DC current, V_{MODE} = 5V	3.36	4.2	5.58	A
$I_{REVLIMIT}$	Reverse Current Limiting		Low-side Transistor, DC current, V_{MODE} = 5V		1.7	3.5	A
V_{CEH}	CE Input Voltage, “High”			1.25			V
V_{CEL}	CE Input Voltage, “Low”					1.1	V
I_{CEH}	CE Input Current, “High”		V_{IN} = V_{CE} = 30 V		1.2	2.45	µA
I_{CEL}	CE Input Current, “Low”				0	0.1	µA

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

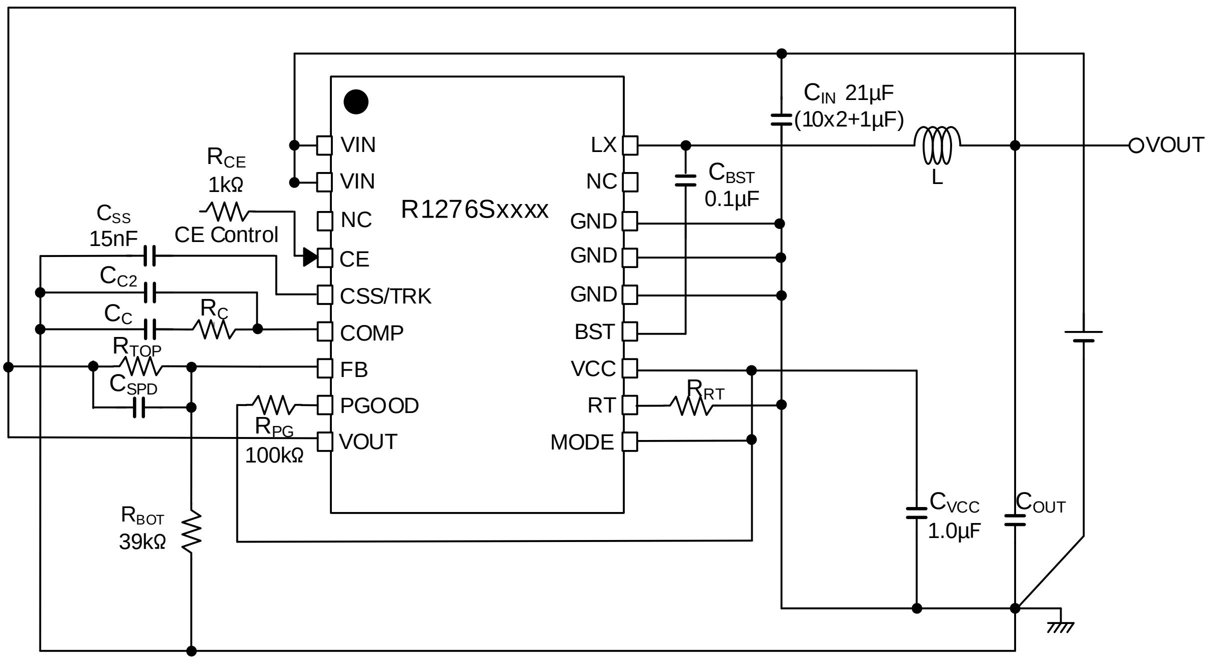
V_{IN} = 12 V, V_{CE} = V_{IN}, unless otherwise specified.
The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

R1276S Electrical Characteristics (Continued) **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{FBH}	FB Input Current, “High”	V_{FB} = 0.672 V	−0.1	0	0.1	μA
I_{FBL}	FB Input Current, “Low”	V_{FB} = 0 V	−0.1	0	0.1	μA
V_{MODEH}	MODE Input Voltage, “High”		1.40			V
V_{MODEL}	MODE Input Voltage, “Low”				0.74	V
I_{MODEH}	MODE Input Current, “High”	V_{MODE} = 5 V		6.25	14.0	μA
I_{MODEL}	MODE Input Current, “Low”	V_{MODE} = 0 V	−0.1	0	0.1	μA
T_{TSD}	Thermal Shutdown Temperature Threshold	Rising	150	160		°C
T_{TSR}		Falling	125	140		°C
$V_{PGOODOFF}$	PGOOD “Low” Output Voltage	V_{IN} = 3.6 V, I_{PGOOD} = 1 mA			0.25	V
$I_{PGOODOFF}$	PGOOD Pin Leakage Current	V_{IN} = 30 V, V_{PGOOD} = 6 V			100	nA
V_{FBOVD1}	FB Pin Overvoltage Detection (OVD) Threshold	V_{FB}, Rising	V_{FB} x1.060	V_{FB} x1.10	V_{FB} x1.140	V
V_{FBOVD2}		V_{FB}, Falling	V_{FB} x1.024	V_{FB} x 1.07	V_{FB} x1.111	V
V_{FBUVD1}	FB Pin Undervoltage Detection (UVD) Threshold	V_{FB}, Falling	V_{FB} x0.860	V_{FB} x 0.90	V_{FB} x0.946	V
V_{FBUVD2}		V_{FB}, Rising	V_{FB} x0.895	V_{FB} x 0.93	V_{FB} x0.974	V

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

TYPICAL APPLICATION CIRCUIT



R1276S Typical Application Circuit

R1276SxxxA/C Constant Table

Code (xxx)	F_{OSC} [kHz]	V_{OUT} [V]	L [μH]	C_{OUT} [μF]	C_{SPD} [pF]	R_{TOP} [kΩ]	R_{RT} [kΩ]	R_C [kΩ]	C_C [nF]	C_{C2} [pF]
001	250	3.3	15	200 (100×2)	100	162 (150+12)	121 (220ǁ270)	22	10	100
		5.0	22	200 (100×2)	100	267 (240+27)	121 (220ǁ270)	27	10	100
	500	3.3	10	66 (22×3)	22	162 (150+12)	56	22	3.3	33
		5.0	10	100	22	267 (240+27)	56	22	4.7	33
	1000	3.3	4.7	48.7 (22×2+4.7)	22	162 (150+12)	28.7 (220ǁ33)	12	3.3	15
		5.0	4.7	48.7 (22×2+4.7)	22	267 (240+27)	28.7 (220ǁ33)	12	3.3	15
002	500	6.5	15	147 (100+47)	22	357 (330+27)	56	22	4.7	33
004	250	0.7	3.3	430 (100+330)	1500	3.7 (2.2+1.5)	121 (220ǁ270)	5.1	47	150

ǁ: Parallel connection

Selection of External Components

External components and its value required for R1276S are described. Each value is reference value at initial. Since inductor's variations and output capacitor's effective value may lead a drift of phase characteristics, adjustment to a unity-gain and phase characteristics may be required by evaluation on the actual unit.

1. Determination of Requirements

Determine the frequency, the output capacitor, the current and the input voltage required. For reference values, parameters listed in the following table will be used to explain each equation

Parameter	Value
Output Voltage (V_{OUT})	3.3 V
Output Current (I_{OUT})	3 A
Input Voltage (V_{IN})	12 V
Input Voltage Range	8 V to 16 V
Frequency (f_{OSC})	1000 kHz
ESR of Output Capacitor (R_{COUT_ESR})	3 mΩ

2. Selection of Unity-gain Frequency (f_{UNITY})

The unity-gain frequency (f_{UNITY}) is determined by the frequency that the loop gain becomes "1" (zero dB). It is recommended to select within the range of one-sixth to one-twentieth of the oscillator frequency (f_{OSC}). Since the f_{UNITY} determines the transient response, the higher the f_{UNITY}, the faster response is achieved, but the phase margin will be tight. Therefore, it is required that the f_{UNITY} can secure the adequate stability. As for the reference, the f_{UNITY} is set to 100 kHz.

3. Selection of Inductor

After the input and the output voltages are determined, a ripple current (ΔI_L) for the inductor current is determined by an inductance (L) and an oscillator frequency (f_{OSC}). The ripple current (ΔI_L) can be calculated by Equation 1.

$\Delta I_L = (V_{OUT} / L / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX})$ ··········Equation 1
V_{IN_MAX} : Maximum input voltage

The core loss in the inductor and the ripple current of the output voltage become small when the ripple current (ΔI_L) is small. But, a large inductance is required as shown by Equation 1. The inductance can be calculated by Equation 2 when a reference value of ΔI_L assumes 0.6 A is appropriate value.

$L = (V_{OUT} / \Delta I_L / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX})$ ··········Equation 2
$= (V_{OUT} / 0.6 / f_{OSC}) \times (1 - V_{OUT} / V_{IN\_MAX})$

The inductance can be calculated by substituting each parameter to Equation 2.

$L = (3.3\ V / 0.6\ A / 1000\ kHz) \times (1 - 3.3\ V / 16V)$
$= 4.37\ \mu H$

When selecting the inductor of 4.7 µH as an approximate value of the above calculated value, ΔI_L can be shown as below.

$\Delta I_L = (3.3\ V / 4.7\ \mu H / 1000\ kHz) \times (1 - 3.3\ V / 16\ V)$
$= 0.557\ A$

4. Setting of Output Capacitance

The output capacitance (C_{OUT}) must be set to meet the following conditions.

■ Calculation based on phase margin

To secure the adequate stability, it is recommended that the pole frequency (f_{P_OUT}) is set to become equal or below one-fourteenth of the unity-gain frequency. The pole frequency (f_{P_OUT}) can be calculated by Equation 3.

$f_{P\_OUT} = 1/(2 \times \pi \times C_{OUT\_EFF} \times ((R_{OUT\_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT\_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT\_ESR}))$
··········Equation 3

C_{OUT_EFF} : Output capacitance (effective value)
R_{OUT_MIN} : Output resistance at maximum output current
$R_{OUT\_MIN} = V_{OUT} / I_{OUT}$
$= 3.3\ V / 3\ A$
$= 1.1\ \Omega$

Equation (4) can be expressed by substituting $f_{P\_OUT} = f_{UNITY} / 14$ to Equation 3.

$$C_{OUT\_EFF} = 14 / (2 \times \pi \times f_{UNITY} \times ((R_{OUT\_MIN} \times 2 \times \pi \times f_{OSC} \times L) / (R_{OUT\_MIN} + 2 \times \pi \times f_{OSC} \times L) + R_{COUT\_ESR}))$$

……………Equation 4

Then, the output capacitance (effective value) can be calculated by substituting each parameter to Equation 4.

$$C_{OUT\_EFF} = 14/(2 \times \pi \times 100\text{kHz} \times ((1.1\Omega \times 2 \times \pi \times 1000\text{ kHz} \times 4.7\ \mu\text{H})/(1.1\Omega + 2 \times \pi \times 1000\text{kHz} \times 4.7\mu\text{H}) + 3\text{m}\Omega))$$
$$= 21.01\ \mu\text{F}$$

■ Calculation based on ripple at PWM mode

With using the calculated value of C_{OUT}, the amount of ripple at the PWM mode can be shown as Equation 5 and Equation 6.

$$I_{L\_PWM} = ((V_{IN\_MAX} - V_{OUT}) / L) \times V_{OUT} / V_{IN\_MAX} / f_{OSC}$$ …… Equation 5

$$V_{OUT\_PWM} = R_{COUT\_ESR} \times (I_{L\_PWM}) + (I_{L\_PWM} / 2) / f_{OSC} / C_{OUT\_EFF}$$ …… Equation 6

I_{L_PWM} : Maximum current of inductor
V_{OUT_PWM} : Maximum output ripple

Ripple at the PWM mode must be set to become 10 mV to 15 mV or less. If it is over the target value, the output capacitance must be calculated by Equation 7.

$$C_{OUT\_EFF} = (I_{L\_PWM} / 2) / f_{OSC} / (V_{OUT\_PWM} - R_{COUT\_ESR} \times (I_{L\_PWM}))$$ …… Equation 7

Then, the output capacitance (effective value) can be calculated by substituting each parameter to Equation 7.

$$C_{OUT\_EFF} = 0.557\text{ A} / 2 / 1000\text{ kHz} / (10\text{ mV} – 3\text{m}\Omega \times 0.557\text{ A})$$
$$= 33.46\text{ uF}$$

It is recommended that the output capacitance is set to become equal or over the effective value calculated by Equation 4 and Equation7.

The output capacitance (effective value), which is derated depending on the DC voltage applied, can be calculated by Equation 8. Refer to "*Capacitor Manufacture's Datasheet*" for details about derating.

$$C_{OUT\_EFF} = C_{OUT\_SET} \times (V_{CO\_AB} - V_{OUT}) / V_{CO\_AB}$$ ……Equation 8

C_{OUT_SET} : Output capacitor's spec
V_{CO_AB} : Capacitor's voltage rating

With using Equation 8, the effective value is calculated to become 33.46 µF or more. The output voltage (C_{OUT}) can be shown as below when V_{CO_AB} is 16 V.

$C_{OUT\_SET} > C_{OUT\_EFF} / ((V_{CO\_AB} - V_{OUT}) / V_{CO\_AB})$
$C_{OUT\_SET} > 33.46\ \mu F / ((16 - 3.3) / 16)$
$C_{OUT} > 42.15\ \mu F$

As the calculated result, C_{OUT} selects a capacitor of 44 µF (22 µF × 2) (the effective value is 34.9 µF).

■ Calculation based on ripple at VFM mode

With using the calculated value of C_{OUT}, the amount of ripple at the VFM mode can be shown as Equation 9 and Equation 10.

$I_{L\_VFM} = ((V_{IN\_MAX} - V_{OUT}) / L) \times C_{OEF\_TON\_VFM} \times V_{OUT} / V_{IN\_MAX} / f_{OSC}$ ………………………………… Equation 9
$V_{OUT\_VFM} = R_{COUT\_ESR} \times (I_{L\_VFM}) + C_{OEF\_TON\_VFM} \times (I_{L\_VFM} / 2) / f_{OSC} / C_{OUT\_EFF}$ ………………… Equation 10

I_{L_VFM} : Maximum current of inductor
$C_{OEF\_TON\_VFM}$: ON-time scaling (multiples of PWM_ON time)
V_{OUT_VFM} : Maximum output ripple

$C_{OEF\_TON\_VFM}$ can be calculated by 1.75 times (Typ.) as the design value. The ripple value can be calculated by substituting each parameter to Equation 9 and Equation 10.

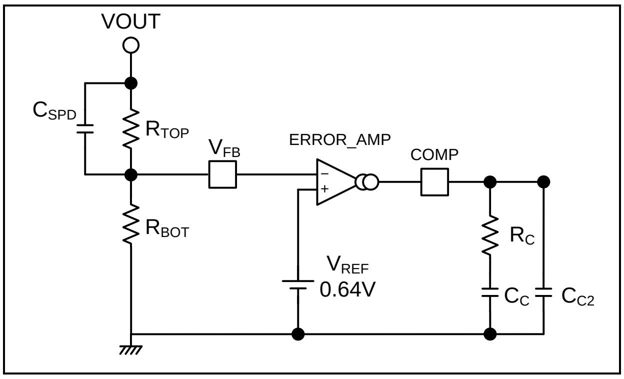
$I_{L\_VFM} = ((16\ V - 3.3\ V) / 4.7\ \mu H) \times 1.75 \times 3.3\ V / 16\ V / 1000\ kHz$
$= 0.975\ A$
$V_{OUT\_VFM} = 3\ m\Omega \times 0.975\ A + 1.75 \times (0.975\ A / 2) / 1000\ kHz / 34.9\ \mu F$
$= 27.36\ mV$

V_{OUT_VFM} must be set to become the target ripple value or less. If V_{OUT_VFM} is over the target value, the output capacitance must be calculated by Equation 11.

$C_{OUT\_EFF} = 1.75 \times (I_{L\_VFM} / 2) / f_{OSC} / (V_{OUT\_VFM} - R_{COUT\_ESR} \times (I_{L\_VFM}))$ …………………………… Equation 11

5. Designation of Phase Compensation

Since the current amplifier for the voltage feedback is output via the COMP pin, the phase compensation is achieved with using external components. The phase compensation is able to secure stable operation with using a ceramic output capacitor and the phase compensation circuit.



Connection Example for External Phase Compensation Circuit

■ Calculation of R_C

The phase compensation resistance (R_C) to set the calculated unity-gain frequency can be calculated by Equation 12.

$R_C = 2 \times \pi \times \mathbf{f_{UNITY}} \times V_{OUT} \times C_{OUT\_EFF} / (g_{m\_ea} \times V_{REF} \times g_{m\_pwr})$ ·········· Equation 12

g_{m_ea} : Error amplifier of g_m
V_{REF} : Reference voltage (0.64 V)
g_{m_pwr} : power level of g_m

$g_{m\_pwr} \times \Delta V_S = \Delta I_L$

$g_{m\_ea} / \Delta V_S = 0.05 \times 10$ ^ (-6) $\times f_{OSC} / V_{OUT}$

$g_{m\_ea} \times g_{m\_pwr} = 0.05 \times 10$ ^ (-6) $\times \Delta I_L \times f_{OSC} / V_{OUT}$ ·········· Equation 13

ΔV_S : Output amplitude of the slope circuit

R_C can be calculated by substituting Equation 13 to Equation 12.

$R_C = 2 \times \pi \times \mathbf{f_{UNITY}} \times V_{OUT} \times C_{OUT\_EFF} / (V_{REF} \times 0.05 \times 10$ ^ (-6) $\times \Delta I_L \times f_{OSC} / V_{OUT})$
$= 2 \times \pi \times 100$ kHz $\times 3.3$ V $\times 34.9$ µF / (0.64 × 0.05 × 10 ^ (-6) × 0.557A × 1000 kHz / 3.3 V)
$=13.4 \fallingdotseq 12$ kΩ

■ Calculation of C_C

C_C must be calculated by Equation 14 so that the zero frequency of the error amplifier meets the highest pole frequency (f_{P_OUT}). Then, f_{P_OUT} = 4.28 kHz is determined by calculation of Equation 3.

$C_C = 1 / (2 \times \pi \times R_C \times f_{P\_OUT})$ ··········· Equation 14
$= 1/ (2 \times 3.14 \times 12\ k\Omega \times 4.28\ kHz)$
$= 2.772 \fallingdotseq 3.3\ nF$

■ Calculation of C_{C2}

C_{C2} can be calculated by two different calculation methods to vary from the zero frequency (f_{Z_ESR}) depending on the ESR of a capacitor. f_{Z_ESR} can be calculated by Equation 15.

$f_{Z\_ESR} = 1 / (2 \times \pi \times R_{COUT\_ESR} \times C_{OUT\_EFF})$ ··········· Equation 15
$= 1519\ kHz$

[When the zero frequency is lower than f_{OSC} / 2]

C_{C2} sets the pole to f_{Z_ESR}.

$C_{C2} = R_{COUT\_ESR} \times C_{OUT\_EFF} / R_C$ ··········· Equation 16

[When the zero frequency is higher than f_{OSC} / 2]

C_{C2} sets the pole to f_{OSC} / 2 so as to be a noise filter for the COMP pin.

$f_{OSC} / 2 = 1 / (2 \times \pi \times R_C \times C_{C2})$
$C_{C2} = 2 / (2 \times \pi \times R_C \times f_{OSC})$ ··········· Equation 17

In the reference example, C_{C2} is used as the noise filter for the COMP pin because of being higher than $f_{OSC}/2$.

$C_{C2} = 26.53 \fallingdotseq 22\ pF$

■ Calculation of C_{SPD}

C_{SPD} is set to the zero frequency to meet the unity-gain frequency.

$R_{TOP} = R_{BOT} \times (V_{OUT} / V_{REF} - 1)$
$C_{SPD} = 1 / (2 \times \pi \times \mathbf{f_{UNITY}} \times R_{TOP})$ ··········· Equation 18

When $R_{BOT} = 39\ k\Omega$,
$R_{TOP} = 39\ k\Omega \times (3.3\ V / 0.64\ V - 1)$
$= 162.1\ k\Omega$

$C_{SPD} = 1 / (2 \times \pi \times 100\ kHz \times 162.1\ k\Omega)$
$= 9.82 \fallingdotseq 10\ pF$

Cautions in Selecting External Components

Inductor

- Choose an inductor that has small DC resistance, sufficient allowable current and is hard to cause magnetic saturation. DC resistance affects efficiency. If the allowable current is insufficient and magnetic saturation occurs, the current cannot be superimposed and the inductor may be destroyed. If the inductance value is small, the peak current of LX may increase along with the load current. As a result, the current limit circuit may start to operate when the peak current of LX reaches to “LX limit current”.

Capacitor

- Choose a capacitor that has a sufficient margin to the drive voltage ratings with consideration of the DC bias characteristics and the temperature characteristics.
- The use of ceramic capacitors for C_{IN} and C_{OUT} is recommended although an electrolytic capacitor can be used. If using the electrolyte capacitor, select it with the lowest possible ESR with consideration of the allowable ripple current rating (I_{RMS}). I_{RMS} can be calculated by the following equation.

$$I_{RMS} \fallingdotseq I_{OUT} / V_{IN} \times \sqrt{\{ V_{OUT} \times (V_{IN} - V_{OUT}) \}}$$

Electrolytic capacitors may have characteristics that ESR increases at low temperatures, use it with caution to the phase compensation, especially when using as a C_{OUT}.

THEORY OF OPERATION

MODE Pin Function

The R1276S operating mode is switched between the forced PWM mode and PLL_PWM mode, by a voltage or a pulse applied to MODE pin. The forced PWM mode is selected when the voltage of the MODE pin is 1.4 V or more, and the PWM works regardless of a load current. The PWM/VFM auto-switching mode is selected when it is 0.74 V or less, and control is switched between a PWM mode and a VFM mode depending on the load current. See "*Forced PWM mode and VFM mode*" for details. And see "*Frequency Synchronization Function*" for the operation on connecting an external clock.

Frequency Synchronization Function

The R1276S can synchronize to the external clock being inputted via the MODE pin, with using a PLL (Phase-locked loop). The forced PWM mode is selected during synchronization. The external clock with a pulse-width of 100 ns or more is recommended. The allowable range of oscillation frequency is 0.5 to 1.5 times of the set frequency, and the operating guaranteed frequency is in the 250 kHz to 1 MHz range(1). When starting up the device while the external clock is sent to the MODE pin, the device synchronizes to the external clock while starting up with soft-start. Be aware that if the voltage difference between input and output is reduced and the device goes into the maxduty or duty-over condition, the device starts operating at 1 to1/4 of the synchronous frequency and goes into the asynchronous condition with the MODE pin.

Duty-over

When the input voltage is reduced at cranking, the operating frequency is reduced until one-fourth of the set frequency with being linearly proportional to time in order to maintain the output voltage. Exploiting the ON duty to exceed the maxduty value at normal operation can make the differential between input and output voltages small. The duty over function operates when the minimum OFF time is detected at the set frequency and external synchronization frequency

UVLO (Undervoltage Lockout)

If the VCC pin voltage drops below the UVLO detection threshold of 3.3 V (Typ.) due to the input voltage drop, the R1276S turns the switching off to prevent the malfunction of the device. Due to the switching stop, the output voltage drops according to the load and C_{OUT}. If the VCC pin voltage rises above the UVLO threshold of 4.3 V (Typ.), the device restarts the operation with soft-start. For the R1276S, 4.5 V, the maximum UVLO release voltage, is a start-up voltage.

OVLO (Overvoltage Lockout)

If the input voltage rises above the OVLO detection threshold of 35 V (Typ.), the R1276S turns the switching off to prevent malfunctions of the device or damage on the transistor due to overvoltage. Due to the switching stop, the output voltage drops according to the load and C_{OUT} values. If the input voltage drops below the OVLO release threshold of 34 V (Typ.), the device restarts the operation with soft-start. Note that this function does not guarantee the operation above the absolute maximum ratings.

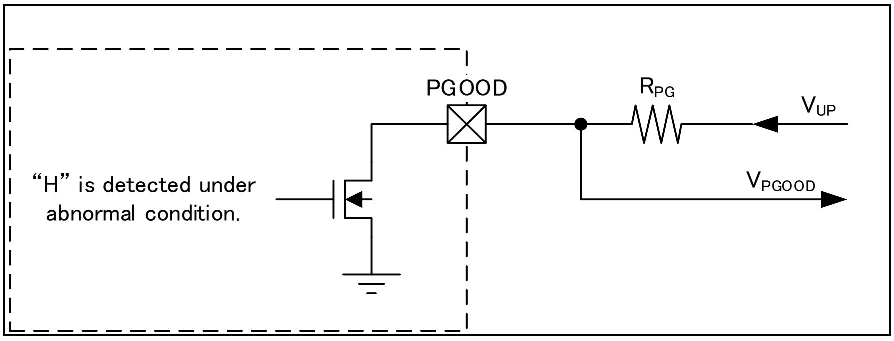
(1) The adjustable oscillation frequency range becomes 250 kHz ≤ f_{OSC} ≤ 600 kHz when 0.7 V ≤ V_{OUT} < 3.3 V.

PGOOD (Power Good) Output

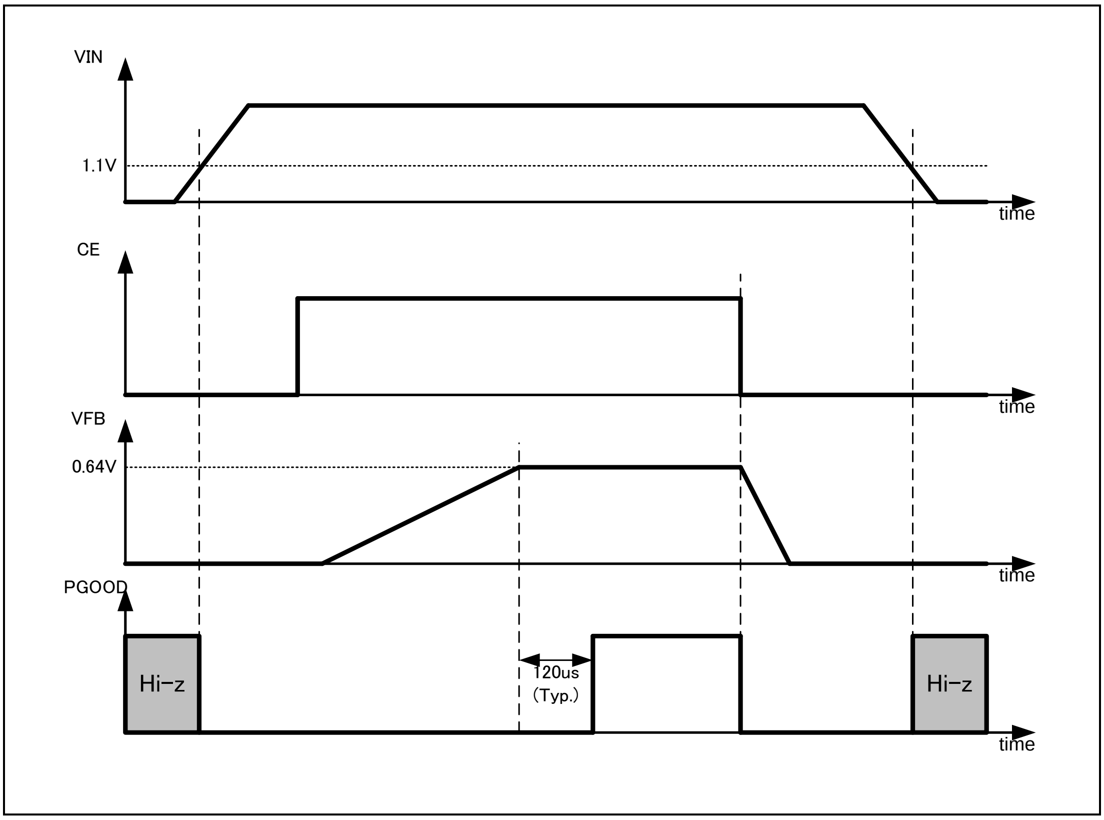
The power good function with using a NMOS open drain output pin can detect the following states of the R1276S. The NMOS turns on and the PGOOD pin becomes “Low” when detecting them. After the device returns to their original state, the NMOS turns off and the PGOOD pin outputs “High” (PGOOD Input Voltage: V_{UP}).

- CE = “Low” (Shut down)
- UVLO
- OVLO
- Thermal Shutdown
- Soft-start
- UVD
- OVD
- Hiccup-type Protection

The PGOOD pin is designed to become 0.25 V or less in “Low” level when the current floating to the PGOOD pin is 1 mA. The use of the PGOOD input voltage (V_{UP}) of 5.5 V or less and the pull-up resistor (R_{PG}) of 10 kΩ to 100 kΩ are recommended. If not using the PGOOD pin, connect it to “Open” or “GND”.



Power Good Circuit



Rising / Falling Sequence of Power Good Circuit

Under Voltage Detection (UVD)

The UVD function indirectly monitors the output voltage with using the FB pin. The PGOOD pin outputs “Low” when the UVD detector threshold is 90% (Typ.) of V_{FB} and V_{FB} is less than the UVD detector threshold for more than 15 µs (Typ.). When V_{FB} is over 93% (Typ.) of 0.64 V, the PGOOD pin outputs “High” after delay time (Typ.120 µs.). And, the hiccup-type overcurrent protection works when detecting a current limiting during the UVD detection.

Overvoltage Detection (OVD)

The OVD function indirectly monitors the output voltage with using the FB pin. Switching stops even if the internal circuit is active state, when detecting the overvoltage of V_{FB}. The PGOOD pin outputs “Low” when the OVD detector threshold is 110% (Typ.) of V_{FB} and V_{FB} is over the OVD detector threshold for more than 15 µs (Typ.). When V_{FB} is under 107% (Typ.) of 0.64 V, the PGOOD pin outputs “High” after delay time (Typ.120 µs.). Then, switching is controlled by normal operation.

Hiccup-type Overcurrent Protection

The hiccup-type overcurrent protection can work under the operating conditions that is the UVD can function during the current limiting. The hiccup type protection stops switching and releases the circuit after the protection delay time (Typ. 7.5 ms). Since this protection is auto-release, the CE pin switching of “Low”/“High” is unnecessary. When the output is shorted to GND, switching of “ON” / “OFF” is repeated until the shorting is released.

Minimum ON-Time

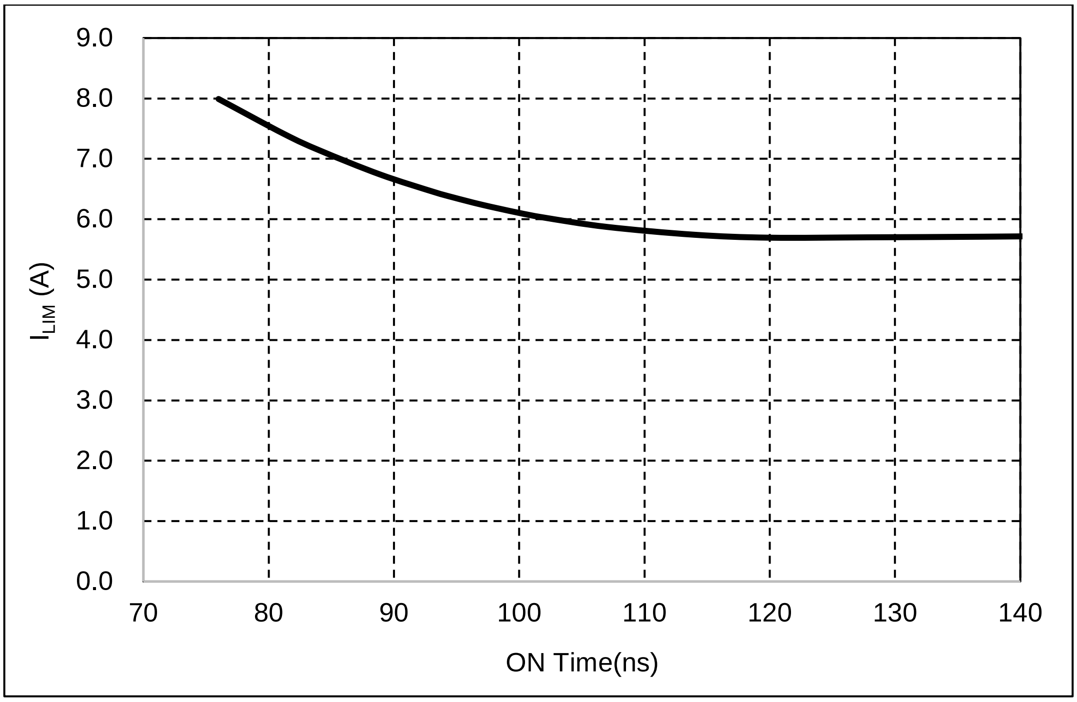
The minimum ON-time means the minimum time duration that the R1276S can turn the high-side transistor on during the oscillation period. The minimum on-time of the device (Typ. 70 ns) is determined by the internal circuit. The device cannot generate a pulse width that is less than the pulse width of minimum on-time. Therefore, when setting the output voltage and the oscillator frequency, be careful that the minimum step-down ratio [V_{OUT} / V_{IN} x (1 / f_{OSC})] is not less than the minimum on-time. If they are set to less than the minimum step-down ratio, the pulse skipping occurs, which outputs the V_{OUT} but increases the ripple current and the output voltage ripple.

Minimum OFF-Time

The minimum OFF-time means the minimum time duration that the R1276S can turn the high-side transistor off during the oscillation period. By the adoption of bootstrap method, the high-side transistor, which is used as the R1276S internal circuit for the minimum off-time, is used a NMOS. The voltage sufficient to drive the high-side transistor must be charged. Therefore, the minimum off-time is determined from the required time to charge the voltage. By the adoption of the frequency’s reduction method by one-quarter of a set value (Min.), if the input-output difference voltage becomes small or load transients are caused, the OFF period can be caused once in four-cycle period of normal cycle. As a result, the minimum off-time becomes 120 ns (Typ.) substantially, and the maximum duty cycle can be improved.

Current Limit

The output current of the R1276S is limited by the current limit using a peak current method. The current limit is set to 4.2 A (Typ. DC value) and it is fixed inside the IC. The current limit circuit limits the current by monitoring the drain to source voltage of a high-side transistor. The transitional current limit of the inductor current is set to be higher than the DC value. The current limit of the device starts operating after the minimum on-time, so it has to be careful especially when the device is used close to the minimum on-time because the current limit will increase. The following diagram shows the relation between current limit and on-time using our evaluation board. The longer the on-time is, the more the current approaches the current limit value of 4.2 A (Typ. DC value).



R1276S Current Limit vs LX On-Time

Precautions for Operating in Low Input Voltage

When using the R1276S with V_{IN} = 5 V or less, the load current may be limited in following two cases.

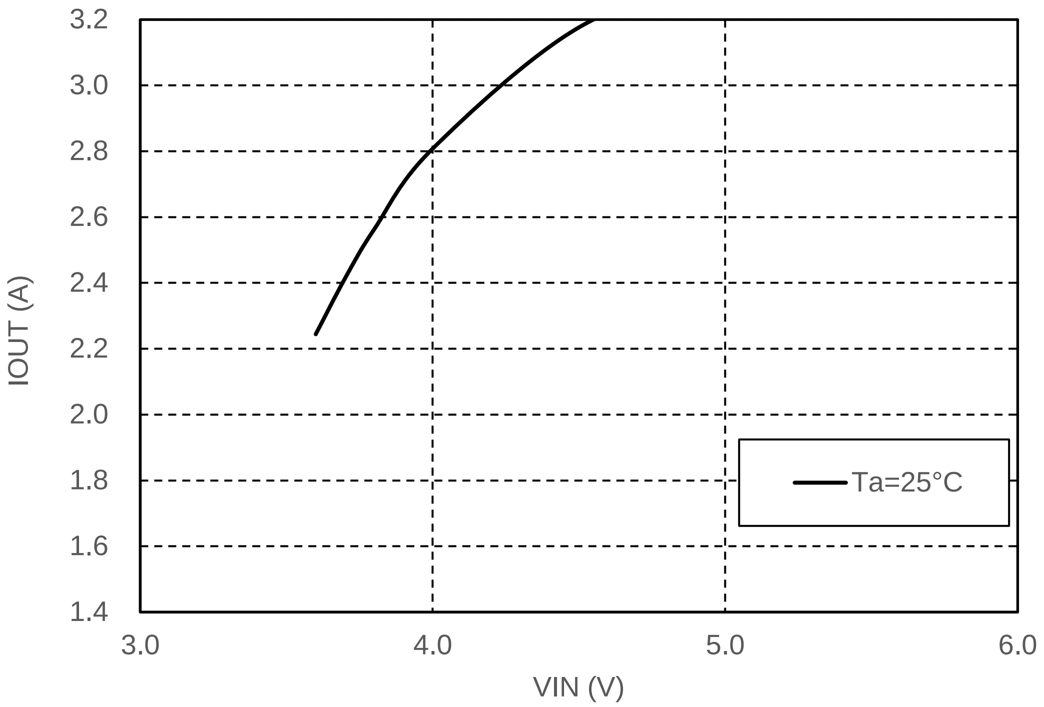
First Case: The device designed to reach current limit by monitoring the voltage difference between VIN and LX. During the low input voltage operation, the driving capability of high-side transistor decreases, so the voltage difference between VIN and LX becomes larger with smaller output current. Therefore, the load current may be limited during the low input voltage operation.

Second Case: During the low input voltage operation, the duty-over function decreases the oscillator frequency. While the oscillator frequency is 1/4 of the set frequency, drawing the load current can cause a voltage difference between the input and output. These make the device to exit from duty-over condition, and as a result, the output voltage drops.

Both cases show that the current limit is depending on the input voltage and load current. Careful consideration is required when applying a heavy load while the input voltage is low. The following graph shows the relation between input voltage and load current.

If the BST voltage between BST and LX drops extremely, the device forcibly turns off the switching to charge the BST voltage to prevent malfunction of the logic circuit.

This may occur when V_{IN} is 4.5 V or less and it may affect the output voltage ripple. Also, if V_{IN} is less than 4.5 V and UVD is detected as the output voltage decreases, the hiccup-type overcurrent protection may work due to the protection function inside the IC.



V_{OUT} = 3.3 V / f_{OSC} = 1MHz Setting

R1276S Output Current vs Input Voltage

Output Voltage Setting

The output voltage (V_{OUT}) can be set by adjustable values of R_{TOP} and R_{BOT}. The value of V_{OUT} can be calculated by Equation 1:

$V_{OUT} = V_{FB} \times (R_{TOP} + R_{BOT}) / R_{BOT}$ ·· Equation 1

For example, when setting V_{OUT} = 3.3 V and setting R_{BOT} = 39 kΩ, R_{TOP} can be calculated by substituting them to Equation 1. As a result of the Equation 2, R_{TOP} can be set to 162 kΩ.

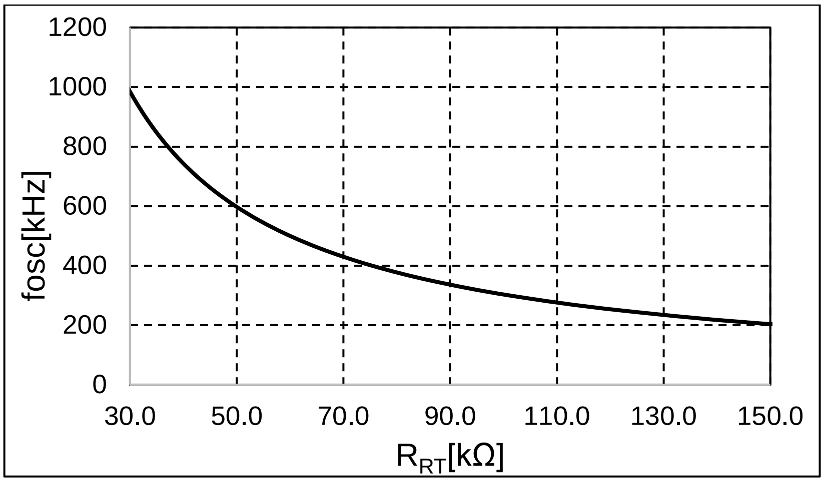
To make 162 kΩ with using the E24 type resistors, the connecting use of 160 kΩ and 2 kΩ resistors in series is required. If the tolerance level of the set output voltage is wide, using a resistor of 160 kΩ to R_{TOP} can reduce the number of components. Rbot is recommended to be 39kΩ or less.

R_{TOP} = (3.3 V / 0.64 V - 1) × 39 kΩ
= 162 kΩ·· Equation 2

R1276S is designed assuming R_{TOP} and R_{BOT} resistance variation of ± 1%

Oscillation Frequency Setting

Connecting the oscillation frequency setting resistor (R_{RT}) between the RT pin and GND can control the oscillation frequency in the range of 250 kHz to 1 MHz(1). For example, using the resistor of 60 kΩ can set the frequency of about 500 kHz.
The Electrical Characteristics guarantees the oscillation frequency under the conditions stated below for f_{OSC0} at R_{RT} = 121 kΩ and f_{OSC1} at R_{RT} = 29 kΩ.
For the SSCG type (xxxC), an up-spreading modulation is used (Typ. +10%).



R_{RT} [kΩ] = 34610 × f_{OSC} [kHz] ^ (-1.023)

R1276S Oscillation Frequency vs. Oscillation Frequency Setting Resistor

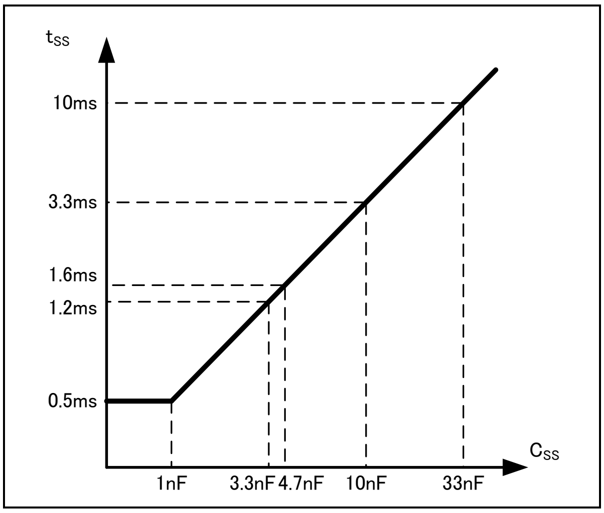
(1) The adjustable oscillation frequency range becomes 250 kHz ≤ f_{OSC} ≤ 600 kHz when 0.7 V ≤ V_{OUT} < 3.3 V.

Soft-start Adjustment

The soft-start time is a time between a rising edge (“High” level) of the CE pin and the timing when the output voltage reaches the set output voltage. Connecting a capacitor (C_{SS}) to the CSS/TRK pin can adjust the soft-start time (t_{SS}) – provided the internal soft-start time of 500 µs (Typ.) as a lower limit. The adjustable soft-start time (t_{SS2}) is 1.6 ms (Typ.) when connecting an external capacitor of 4.7 nF with the charging current of 2.0 µA (Typ.) and 0.64 V (Typ.). If not required to adjust the soft-start time, set the CSS/TRK pin to “Open” to enable the internal soft-start time (t_{SS1}) of 500 µs (Typ.). When a large-capacitance output capacitor is connected, the overcurrent protection may work due to an inflow of large current at startup. Thus, set a longer soft start time to reduce the amount of current and prevent from operating the protections due to the rapid startup.

R1276 may repeatedly restart by detecting an overcurrent at startup depending on conditions, set t_{SS} to 4 ms or more.

Each of soft-start time (tss1/ tss2) when CSS/TRK pin is set to “Open” is guaranteed under the conditions described in the chapter of “Electrical Characteristics”.

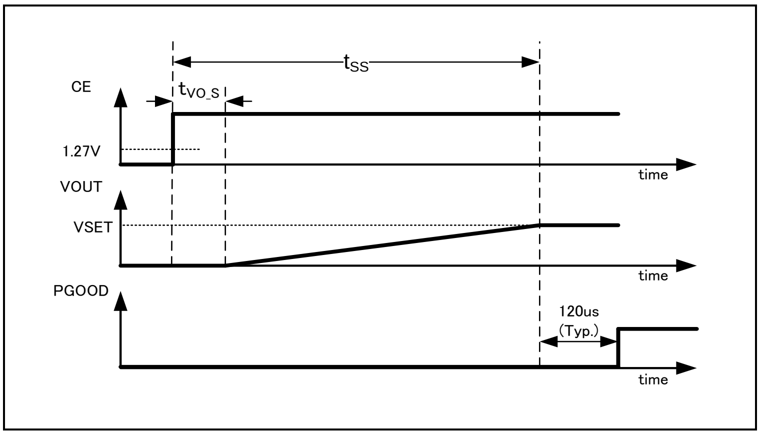


C_{SS} [nF] = (t_{SS} – t_{VO_S}) / 0.64 × 2.0

t_{SS}: Soft-start time (ms)

t_{VO_S}: Time period from CE = “High” to VOUT’s rising (Typ. 0.160 ms)

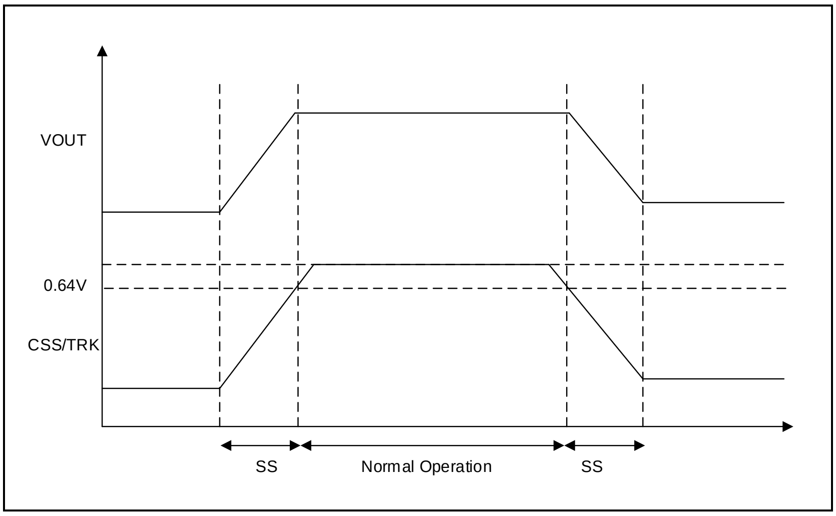
Soft-start Time Adjustment Capacitor vs Soft-start Time



Soft-start Sequence

Tracking Function

Applying an external tracking voltage to the CSS/TRK pin can control the soft-start sequence – provided that the lowest internal soft-start time is limited to 500 µs (Typ.). Since V_{FB} becomes nearly equal to $V_{CSS/TRK}$ at tracking, the complex start timing and soft-start can be easily designed. The available voltage at tracking is between 0 V and 0.64 V. If the tracking voltage is over 0.64 V, the internal reference voltage of 0.64 V is enabled. Also, an arbitrary falling waveform can be generated by reducing $V_{CSS/TRK}$ to 0.64 V (Typ.) or less, because the R1276S supports both of up- and down- tracking.



Tracking Sequence

Reverse Current Limit

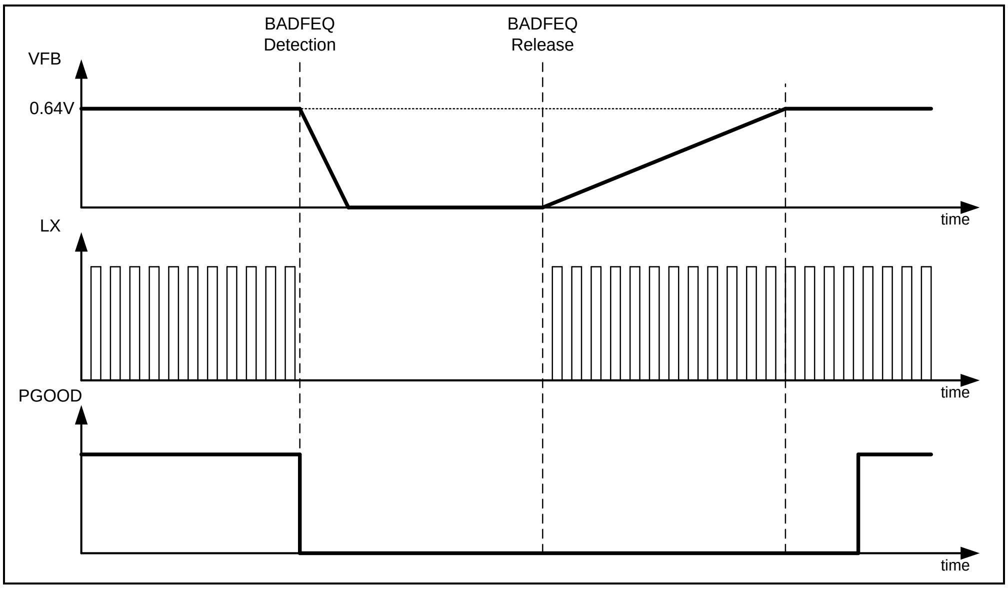
The reverse current limit starts operating when the reverse current flowing through the low-side transistor exceeds the set reverse current threshold. It turns off the low-side transistor to control the reverse current. The reverse current limit is 1.7 A (Typ.). This function operates when the output voltage is pulled up more than the set output voltage due to short-circuiting.

SSCG (Spread Spectrum Clock Generator)

The SSCG function works for EMI reduction at the PWM mode. The function makes EMI waveforms decrease in amplitude to generate a triangle waveform within approximately +10.0% (Typ.) of the oscillator frequency (f_{OSC}). The modulation cycle is f_{OSC} / 128. SSCG is enabled only when MODE = High. SSCG is not effective when a clock is externally applied. The oscillator frequencies are not modulated during the soft-start and operates at the set frequency or external sync frequency.

Bad Frequency Protection (BADFREQ)

If a current equivalent to 4 MHz (Typ.) or more or 125 kHz (Typ.) or less is applied to the RT pin when the oscillator frequency setting resistor (R_{RT}) of the RT pin is in open / short, the R1276S will stop switching to protect the IC and will cause the internal state to transition to its state before the soft-start. The R1276S will restart under the normal control from the state of soft-start when recover after the abnormal condition.

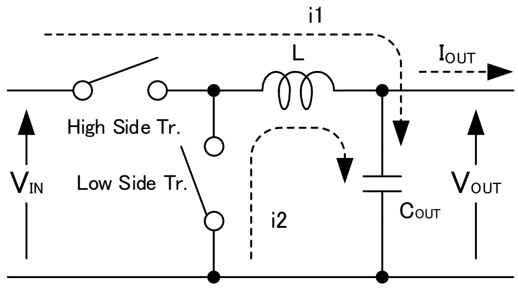


BADFREQ Detection/ Release Sequence

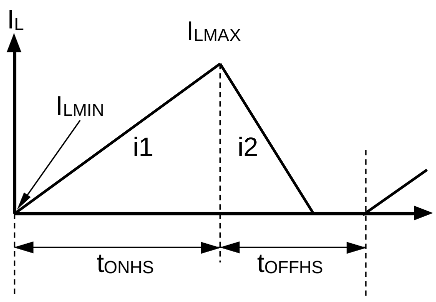
Operation of Step-down DC/DC Converter

The basic operation of the step-down DC/DC converter is shown in the following figures.

This step-down DC/DC converter charges energy in the inductor while the high-side transistor turns on, and discharges the energy from the inductor when the high-side transistor turns off. This inductor reduces the energy loss to provide the lower output voltage (V_{OUT}) than the input voltage (V_{IN}).



Basic Circuit



Current Through Inductor

Step1. When the high-side transistor turns on, current I_L (= i1) flows through the L to charge C_{OUT} and provide I_{OUT}. At this moment, I_L = i1 increases from I_{LMIN} of 0 to reach I_{LMAX} in proportion to the on-time period (t_{ONHS}) of the high-side transistor.

Step2. When the high-side transistor turns off, the low-side transistor turns on in order to maintain I_L at I_{LMAX}, and current I_L (= i2) flows.

Step3. **When MODE = L (VFM/PWM Auto-switching mode)**,
I_L (= i2) decreases gradually and reaches $I_L = I_{LMIN} = 0$, the low-side transistor turns off. This case is called as discontinuous mode. The VFM mode is switched when R1276S goes to the discontinuous mode. If the output current is increased, a time period of t_{OFFHS} runs out prior to reach of $I_L = I_{LMIN} = 0$. The result is that the high-side transistor turns on and the low-side transistor turns off in the next cycle. This case is called continuous mode.
When MODE = H (Forced PWM mode), MODE = External Clock (PLL_PWM mode),
Since the continuous mode works at all time, the low-side transistor turns on until going to the next cycle. That is, the low-side transistor must keep “On” to meet $I_L = I_{LMIN} < 0$, when reaches $I_L = I_{LMIN} = 0$.

In the PWM mode, the output voltage is maintained constant by controlling t_{ONHS} with the constant switching frequency (f_{OSC}).

Forced PWM Mode and VFM Mode

The output voltage control methods are selectable between the PWM / VFM Auto-switching mode and the forced PWM mode by using the MODE pin.

Forced PWM Mode

The R1276S goes into the forced PWM mode by setting the MODE pin “High”. The forced PWM mode operates at fixed switching frequency even during the light load in order to reduce noise. Therefore, when the output current (I_{OUT}) is ΔI_L / 2 or less, I_{LMIN} becomes "0” or less.

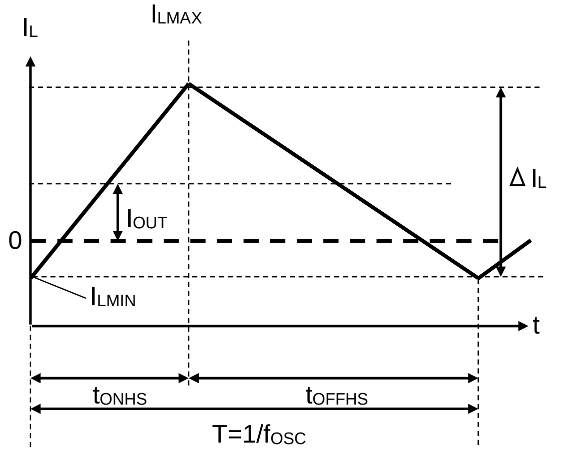
That is, the electric charge, which is charged to C_{OUT}, is discharged via transistor for the durations – when I_L reaches “0” from I_{LMIN} during the t_{ONHS} periods and when I_L reaches I_{LMIN} from “0” during t_{OFFHS} periods.

But, pulses are skipped to prevent the overvoltage when high-side transistor is set to ON under the condition that the output voltage being more than the set output voltage.

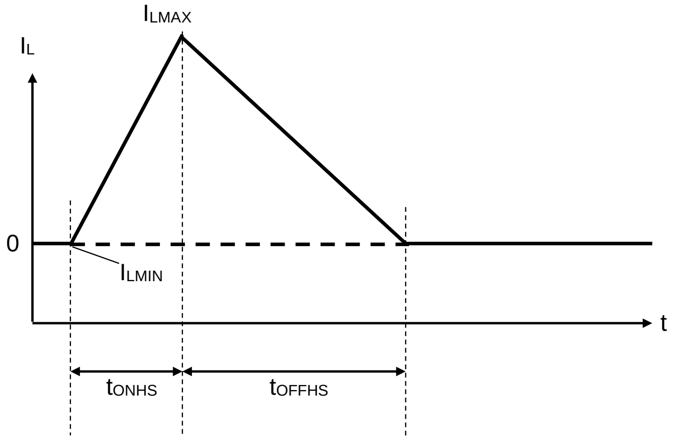
VFM Mode

PWM / VFM Auto-switching mode is selected when setting the MODE pin to “Low”. This mode can automatically switch from PWM to VFM to achieve a high-efficiency during light load conditions. By the VFM mode architecture, the high-side transistor is turned on for t_{ONHS} × 1.75 (typ.) at the PWM mode under the same condition as the VFM mode when the FB pin voltage drops below the internal reference voltage (Typ.0.64 V). After the On-time, the high-side transistor is turned off and the low-side transistor is turned on. When the inductor current of 0 A is detected, the low-side transistor is turned off and the switching operation is stopped (Both of hi- and low-side transistors are OFF). The switching operation restarts when the FB pin voltage becomes less than 0.64 V.

The On-time at the PWM mode is determined by a resistance, input and output voltages, which are connected to the RT pin. Refer to “*Calculation of VFM Ripple”* for detailed description on the On-time at the VFM mode.



Forced PWM Mode



VFM Mode

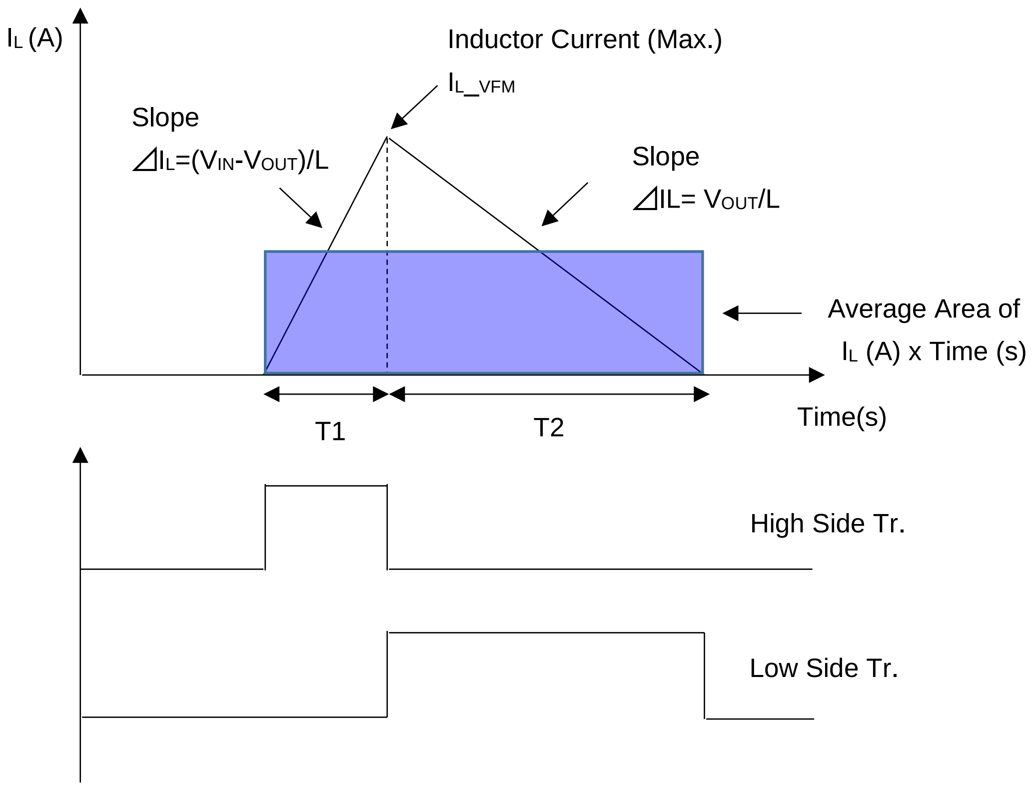
Calculation of VFM Ripple

Calculation example of output ripple voltage (V_{OUT_VFM}) is described. V_{OUT_VFM} can be calculated by Equation 1. And, the maximum value of inductor current (I_{L_VFM}) can be calculated by Equation 2.

$V_{OUT\_VFM} = R_{COUT\_ESR} \times (I_{L\_VFM}) + C_{OEF\_TON\_VFM} \times (I_{L\_VFM} / 2) / f_{OSC} / C_{OUT\_EFF}$ ············ Equation 1

$I_{L\_VFM} = ((V_{IN} - V_{OUT}) / L) \times C_{OEF\_TON\_VFM} \times V_{OUT} / V_{IN} / f_{OSC}$ ············ Equation 2

V_{OUT_VFM} : Output ripple
R_{COUT_ESR} : ESR of output capacitor
I_{L_VFM} : Maximum current of inductor
$C_{OEF\_TON\_VFM}$: Scaling factor of On-time - Typ.1.75 times (Design value)
$(V_{IN}-V_{OUT}) / L$: Slope of inductor current
$C_{OEF\_TON\_VFM} \times V_{OUT} / V_{IN} / f_{OSC}$: On-time



Inductor Current Waveform at VFM Mode

Output voltage can be calculated by the following simple equation.

$V_{OUT} = I \times T/C$

I : Current, C : Capacitance, T : Time

Since I is represented by *1/2 x* I_{L_VFM} as the average current, the time of current passing at the VFM mode can be expressed by the following equation.

$T = C_{OEF\_TON\_VFM} / f_{OSC}$

And, the output ripple voltage (V_{OUT_VFM}) is superimposed a voltage for ESR × I, and Equation 1 is determined. But, ESR is so small that it may be ignored if ceramic capacitors are connected in parallel.

The amount of charge to the output capacitor can be calculated by Equation 3.

(High-side transistor On-time (T1) + Low-side transistor On-time (T2)) × Average amount of current
………… Equation 3

Then, T1 and T2 can be calculated by the following equations, and the time of current passing can be determined.

$T1 = C_{OEF\_TON\_VFM} / f_{OSC} \times V_{OUT} / V_{IN}$ ····· (On-time at VFM)
$T2 = (V_{IN}/V_{OUT}-1) \times T1$ $(0 = I_{L\_VFM} - V_{OUT}/L \times T2)$

$T = T1 + T2$
$= V_{IN} / V_{OUT} \times T1$
$= C_{OEF\_TON\_VFM} / f_{OSC}$

And then, the amount of charge can be determined as Equation 4.

$T \times I_{L\_VFM} / 2 = C_{OEF\_TON\_VFM} / f_{OSC} \times I_{L\_VFM} / 2$ ·· Equation 4

With using above equations, the output ripple voltage (V_{OUT_VFM}) can be calculated by Equation 5.

$V = IT/C = C_{OEF\_TON\_VFM} / f_{OSC} \times I_{L\_VFM} / 2 / C_{OUT\_EFF}$ ·· Equation 5

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points. Refer to *PCB Layout* below.

- External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.

- Place a capacitor (C_{BST}) as close as possible to the LX pin and the BST pin. If controlling slew rate for EMI, a resistor (R_{BST}) should be in series between the BST pin and the capacitor (C_{BST}).

- The tab on the bottom of the HSOP-18 package must be connected to GND when mounted on the board. To improve thermal dissipation on the multilayer board, secure the GND layer as large as possible and set via to release the heat to the other layer in the connecting part of the tab on the bottom.

- The NC pin must be set to “Open”.

- The MODE pin requires the high voltages with the high stability when the forced PWM mode (MODE = “High”) is enabled. If the voltage with the high stability cannot be applied, connection to the VCC pin as “High” level is recommended. Avoid the use of the MODE pin being “Open”.

- If V_{OUT} is a minus potential, the setup cannot occur.

- Shorten the wiring between the Lx pin and the inductor so that the parasitic capacitance is not provided.

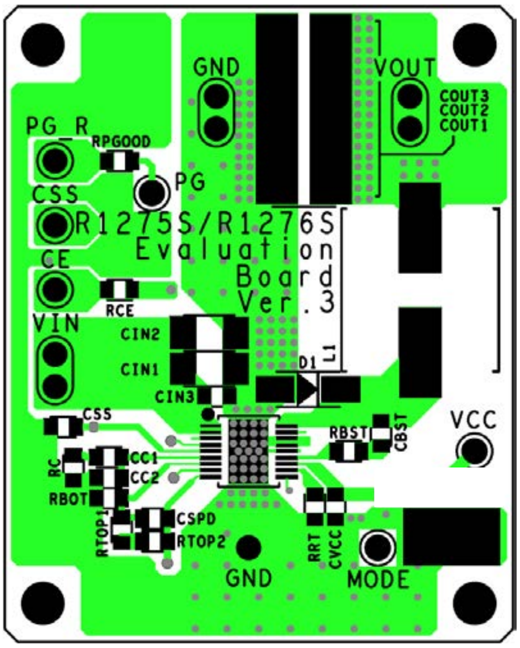
- It is recommended to place the input capacitor (C_{IN}) on the same side as the IC. If it is placed on the different side as the IC by using via, the noise may be increased due to the parasitic inductance component of via.

- Feedback the output voltage near the C_{OUT}.

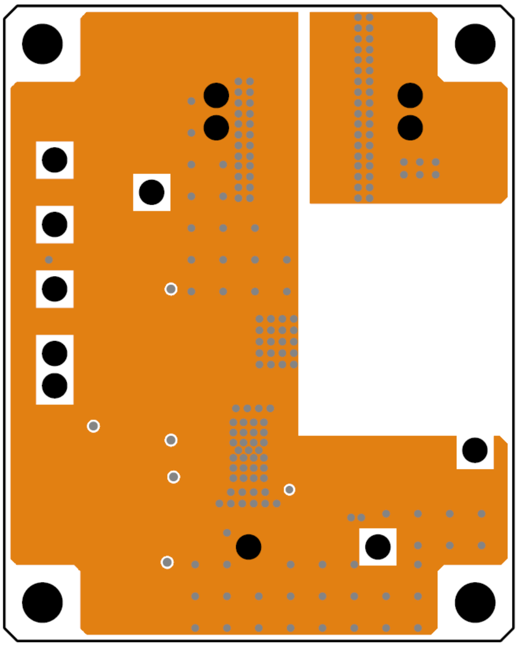
- Place R_{TOP}, R_{BOT}, and C_{SPD} near FB pin and mount them at a position apart from the inductor, Lx pin, and BST pin to prevent the effect of noise.

PCB Layout

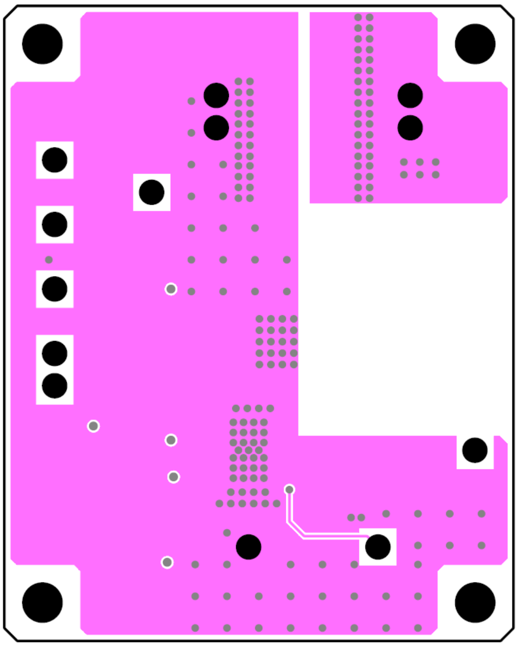
R1276S



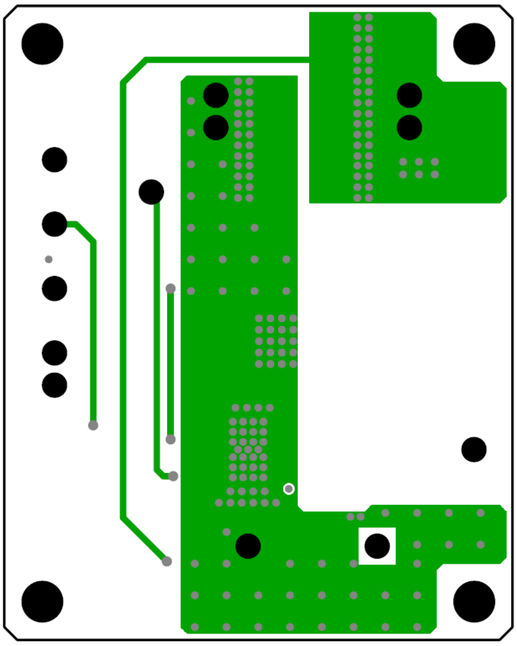
Layer 1 (Top)



Layer 2



Layer 3

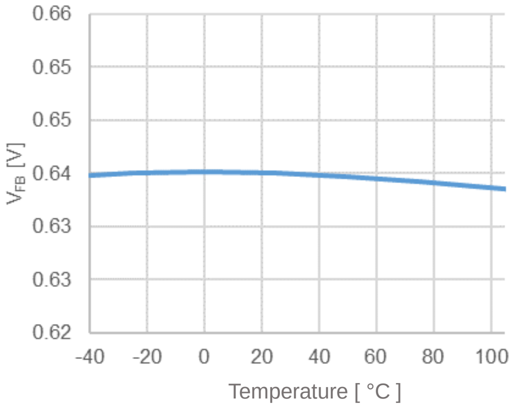


Layer 4 (Bottom)

TYPICAL CHARACTERISTICS

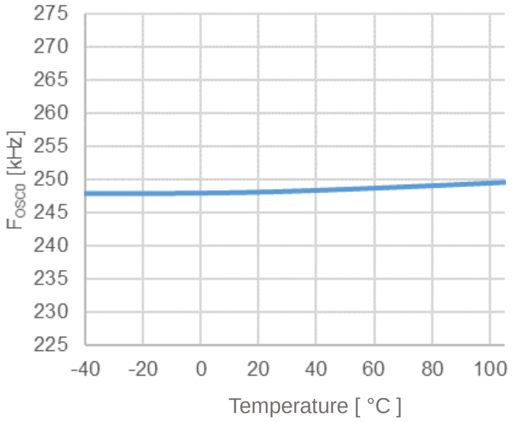
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) FB Voltage

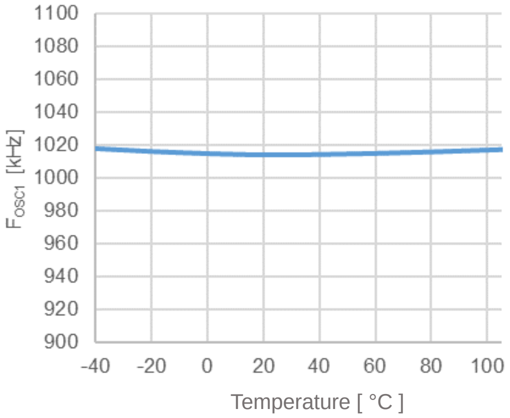


2) Oscillator Frequency

250 kHz (RT = 121 kΩ)

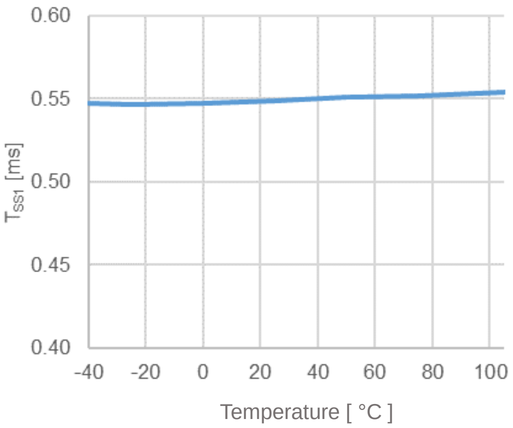


1000 kHz (RT = 28.7 kΩ)

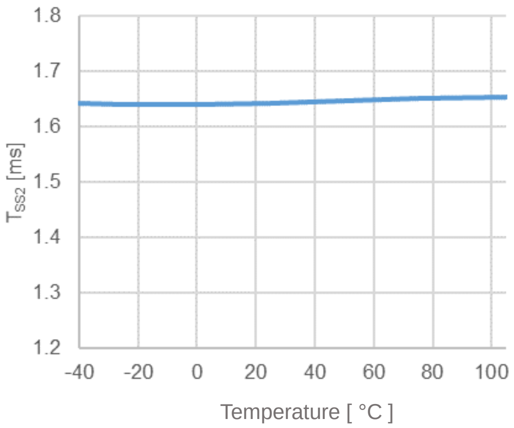


3) Soft-start Time

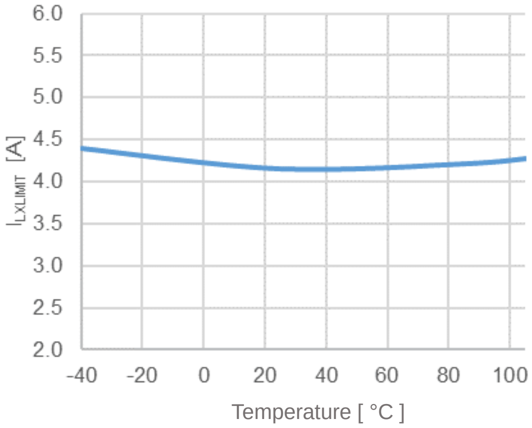
Internally Fixed Soft-start Time (C_{SS} = Open)



Externally Adjustable Soft-start Time (C_{SS} = 4.7 nF)

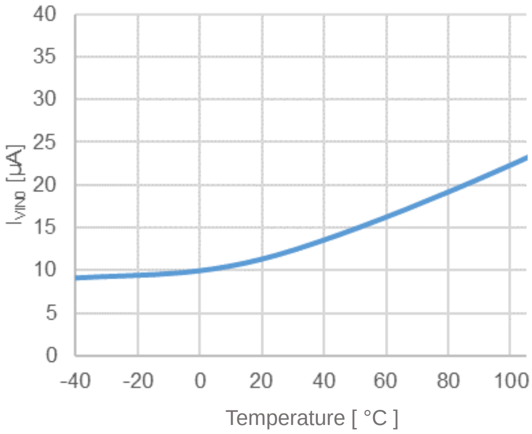


4) LX Limit Current

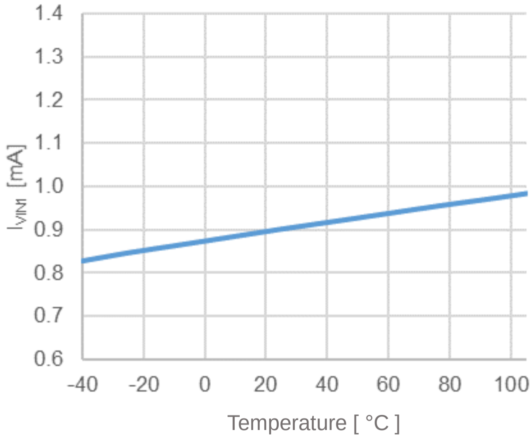


5) V_{IN} Supply Current 1

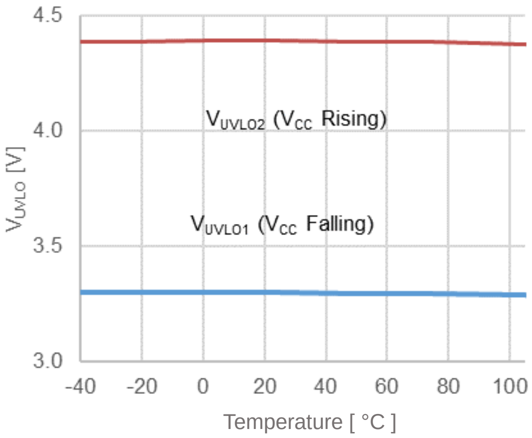
V_{IN} = 12 V, Mode = L



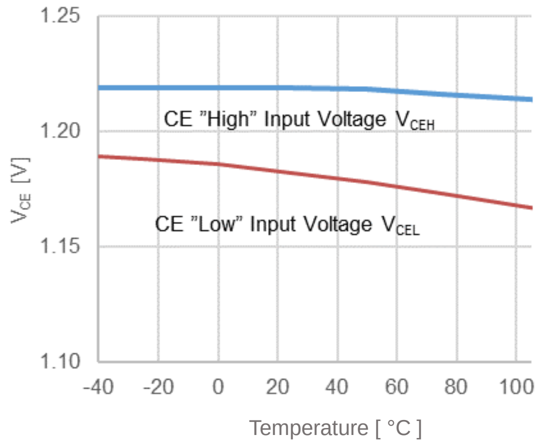
V_{IN} = 12 V, Mode = H



6) UVLO

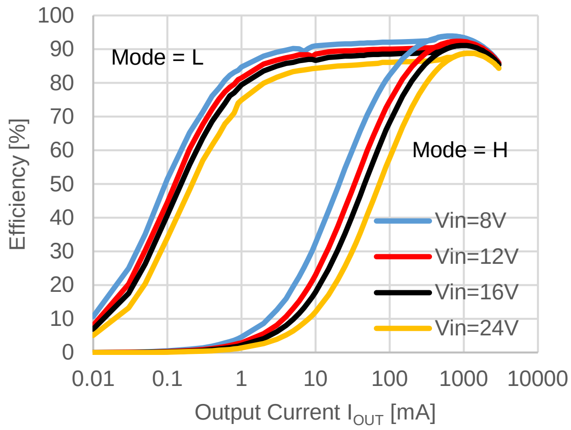


7) CE Input Voltage

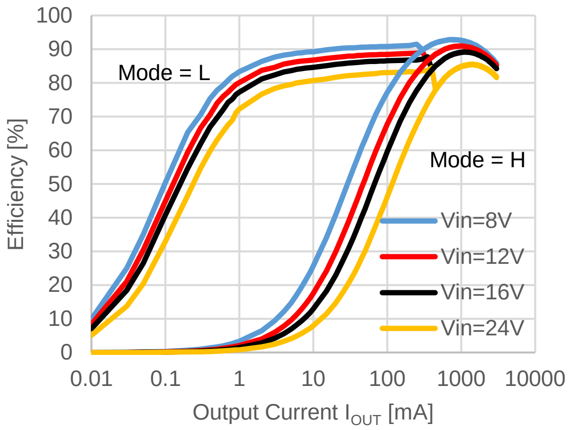


8) Efficiency

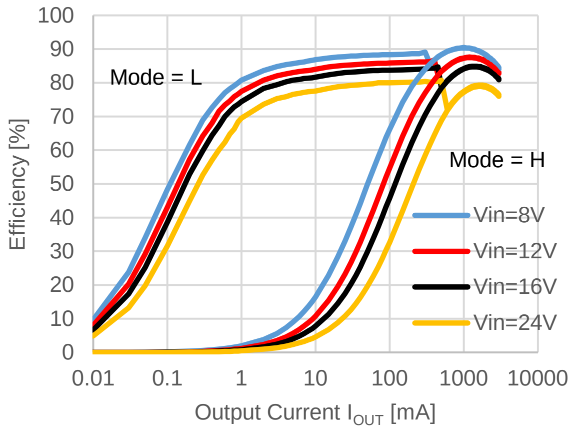
V_{OUT} = 3.3 V, f_{OSC} = 250 kHz



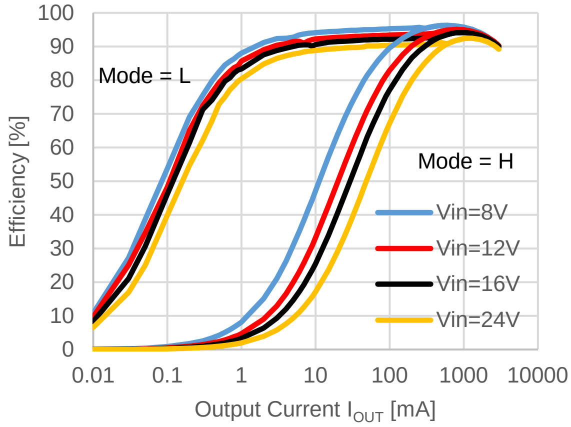
V_{OUT} = 3.3 V, f_{OSC} = 500 kHz



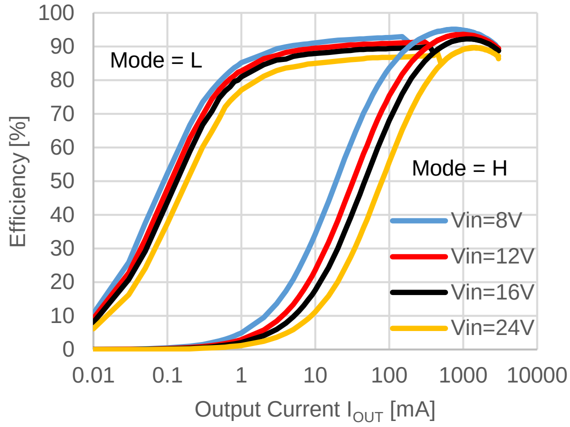
V_{OUT} = 3.3 V, f_{OSC} = 1000 kHz



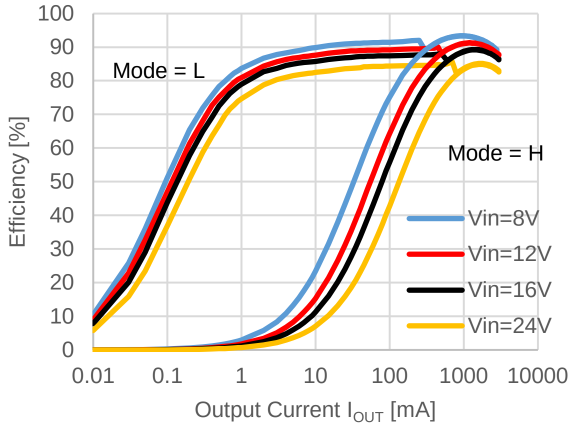
V_{OUT} = 5.0 V, f_{OSC} = 250 kHz



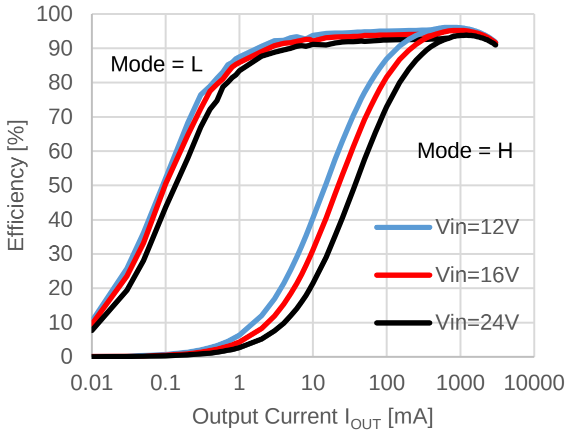
V_{OUT} = 5.0 V, f_{OSC} = 500 kHz



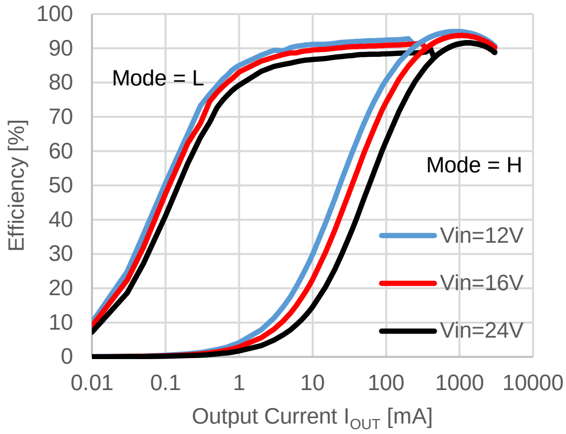
V_{OUT} = 5.0 V, f_{OSC} = 1000 kHz



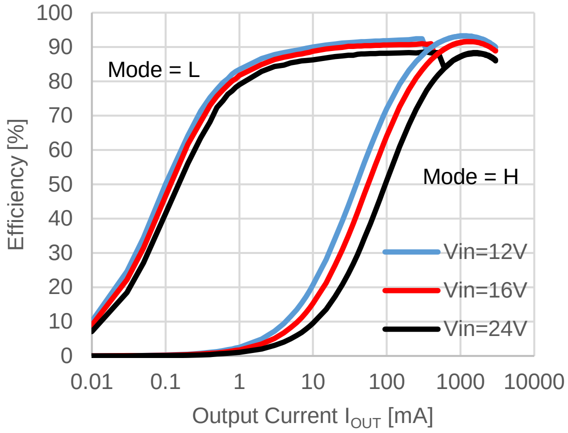
V_{OUT} = 6.5 V, f_{OSC} = 250 kHz



V_{OUT} = 6.5 V, f_{OSC} = 500 kHz

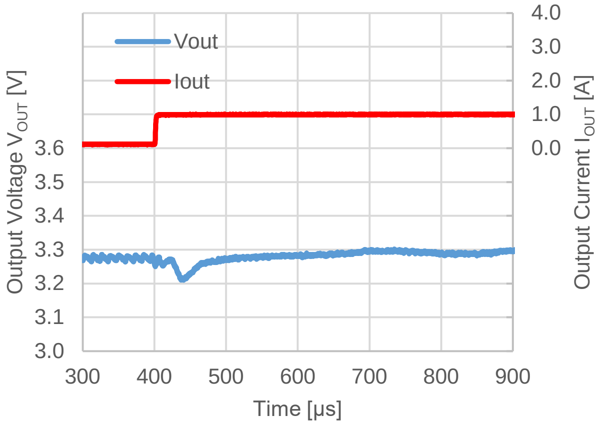


V_{OUT} = 6.5 V, f_{OSC} = 1000 kHz

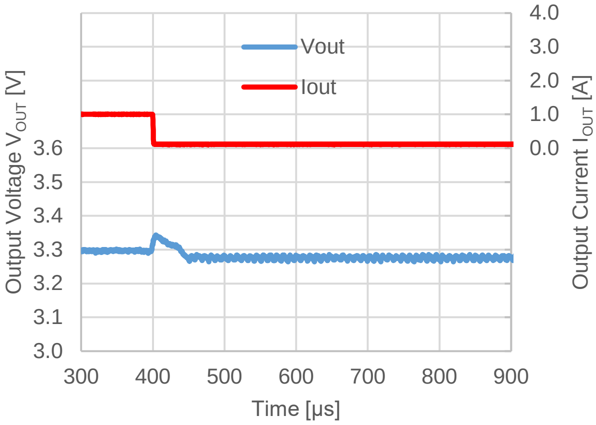


9) Load Transient Response

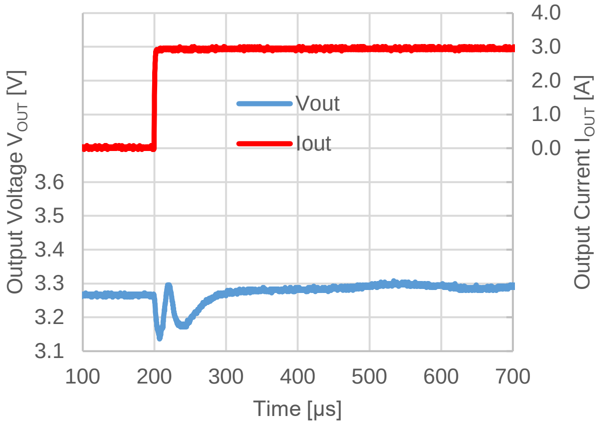
V_{OUT} = 3.3 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0.1 A → 1 A, Mode = L, Tr = 1 A/μs



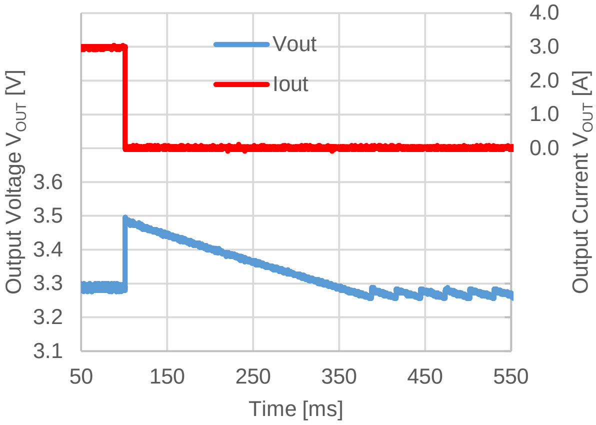
V_{OUT} = 3.3 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 1 A → 0.1 A, Mode = L, Tf = 1 A/μs



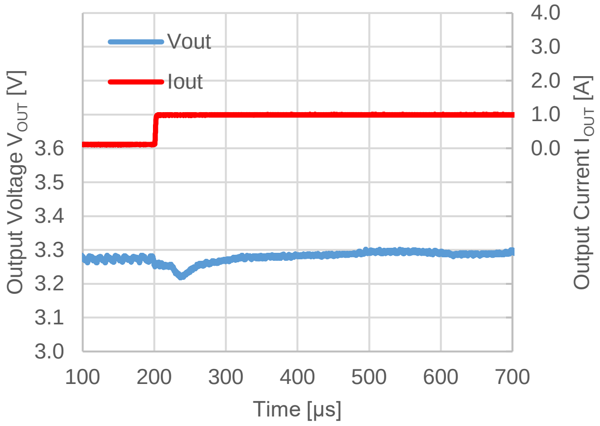
V_{OUT} = 3.3 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0 A → 3 A, Mode = L, Tr = 1 A/μs



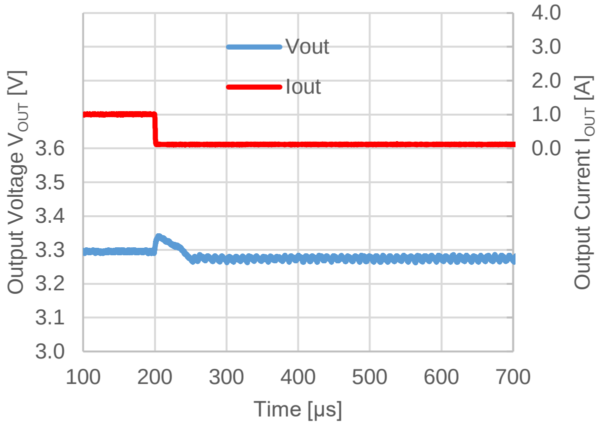
V_{OUT} = 3.3V, V_{IN} = 12V, f_{OSC} = 500kHz
I_{OUT} = 3 A → 0 A, Mode = L, Tf = 1 A/μs



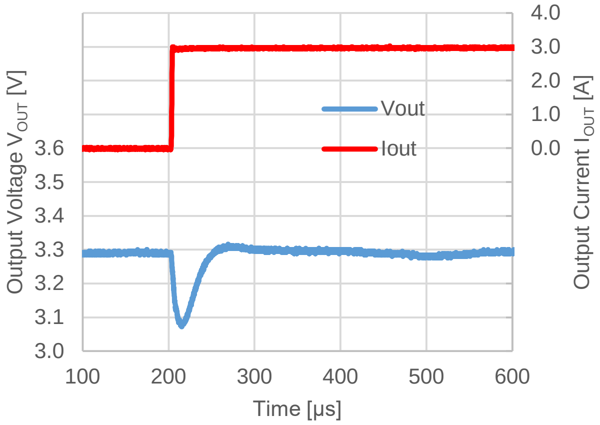
V_{OUT} = 3.3 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0.1 A → 1 A, Mode = L, Tr = 1 A/μs



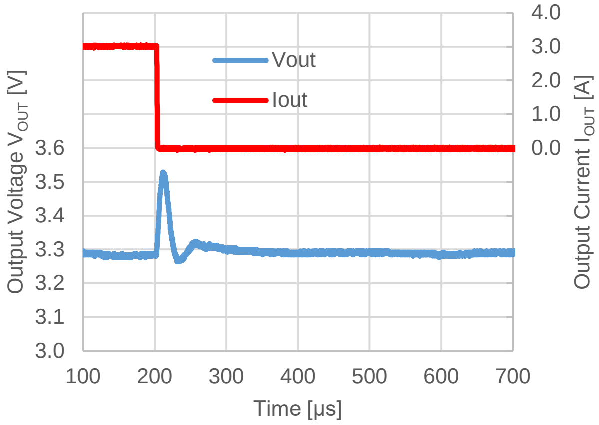
V_{OUT} = 3.3 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 1 A → 0.1 A, Mode = H, Tf = 1 A/μs



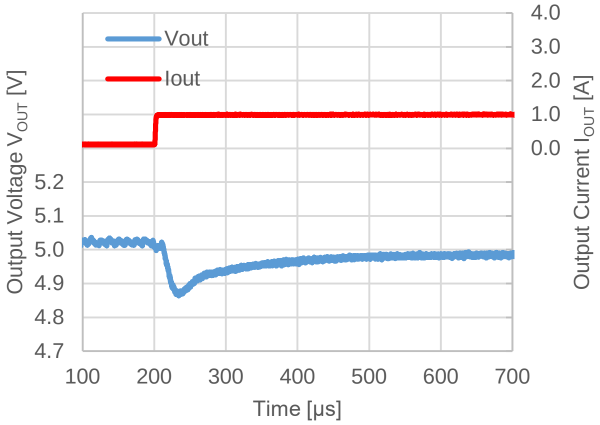
V_{OUT} = 3.3 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0 A → 3 A, Mode = H, Tr = 1 A/μs



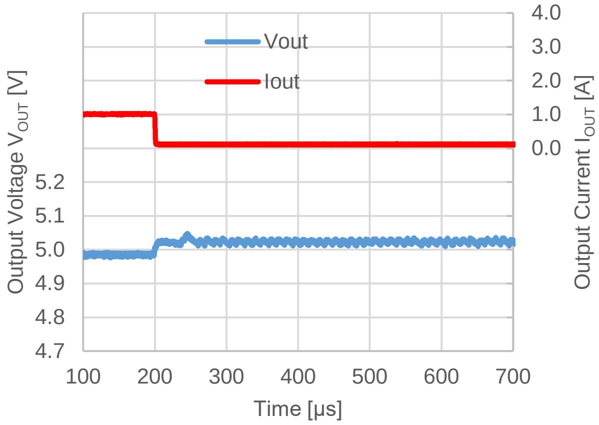
V_{OUT} = 3.3 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 3 A → 0 A, Mode = H, Tf = 1 A/μs



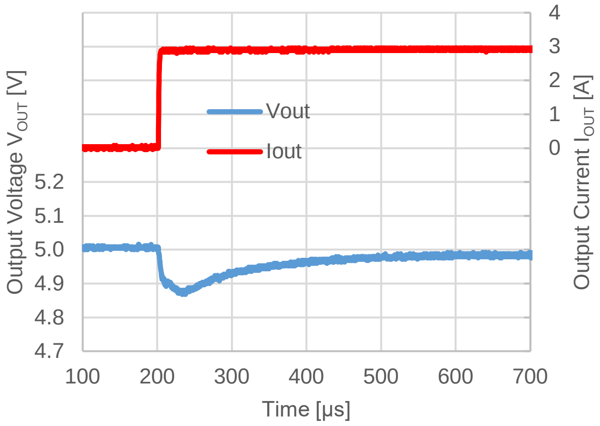
V_{OUT} = 5.0 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0.1 A → 1 A, Mode = L, Tr = 1 A/μs



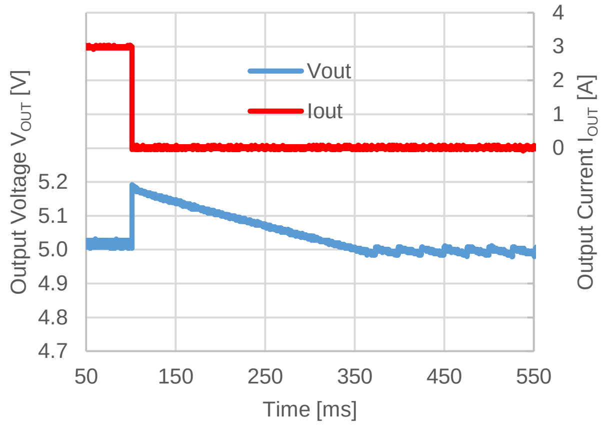
V_{OUT} = 5.0 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 1 A → 0.1 A, Mode = L, Tf = 1 A/μs



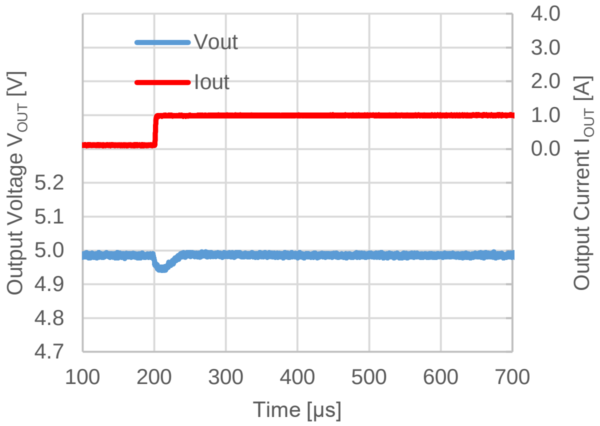
V_{OUT} = 5.0 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0 A → 3 A, Mode = L, Tr = 1 A/μs



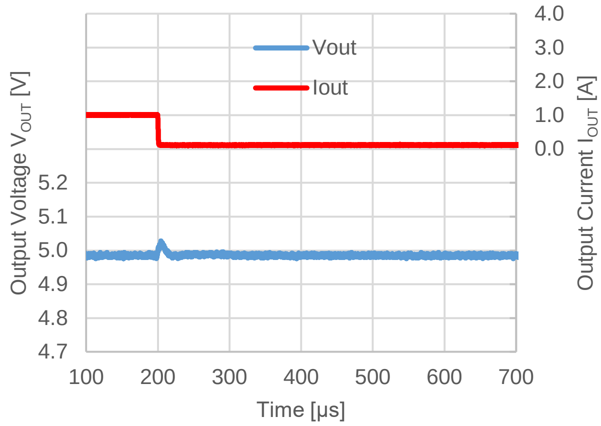
V_{OUT} = 5.0 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 3 A → 0 A, Mode = L, Tf = 1 A/μs



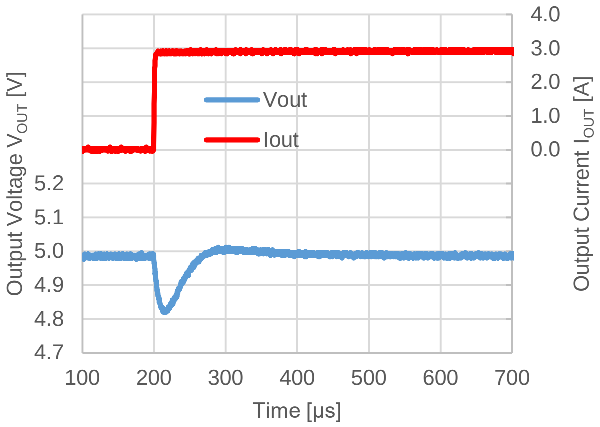
V_{OUT} = 5.0 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0.1 A → 1 A, Mode = H, Tr = 1 A/μs



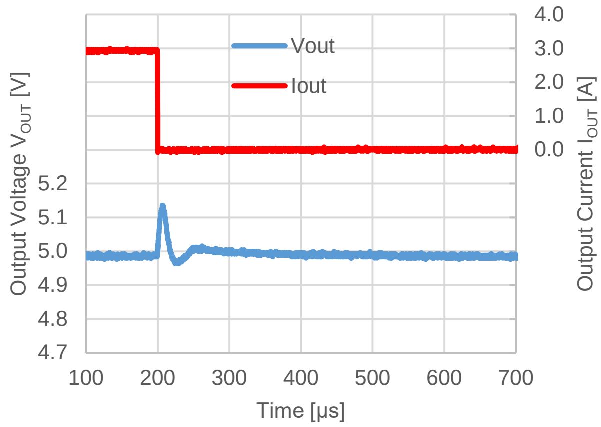
V_{OUT} = 5.0 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 1 A → 0.1 A, Mode = H, Tf = 1 A/μs



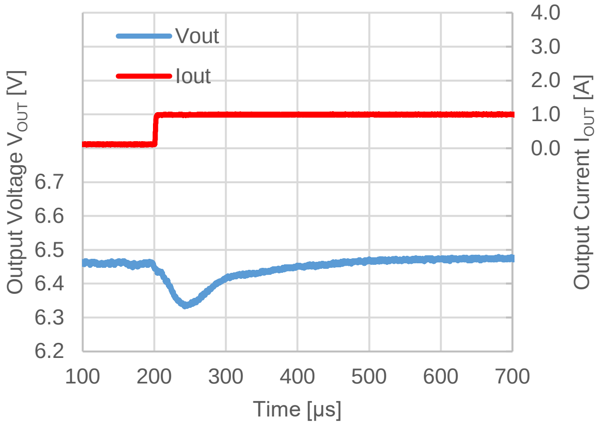
V_{OUT} = 5.0 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0 A → 3 A, Mode = H, Tr = 1 A/μs



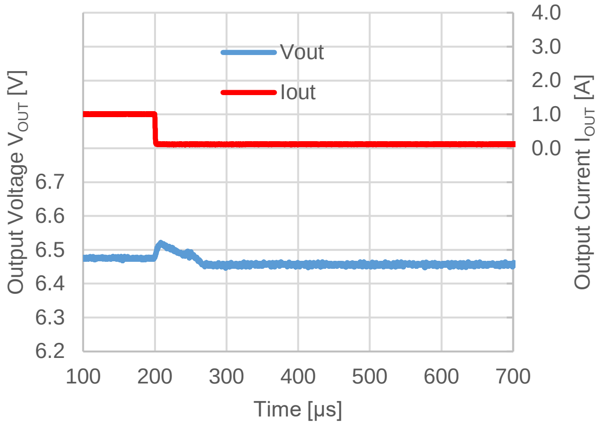
V_{OUT} = 5.0 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 3 A → 0 A, Mode = H, Tf = 1 A/μs



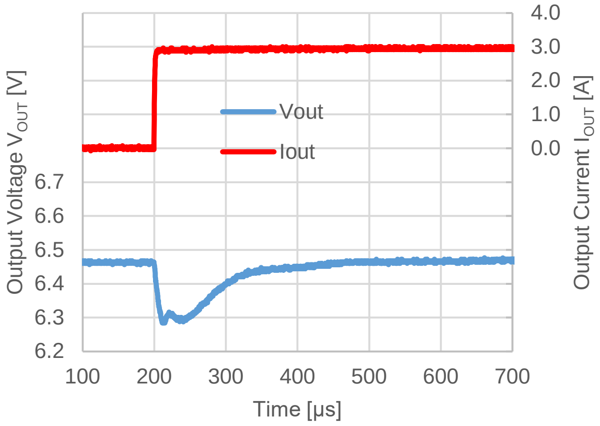
V_{OUT} = 6.5 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0.1 A → 1 A, Mode = L, Tr = 1 A/μs



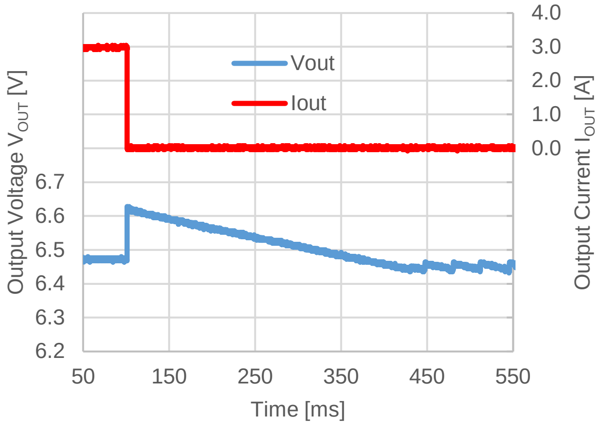
V_{OUT} = 6.5 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 1 A → 0.1 A, Mode = L, Tf = 1 A/μs



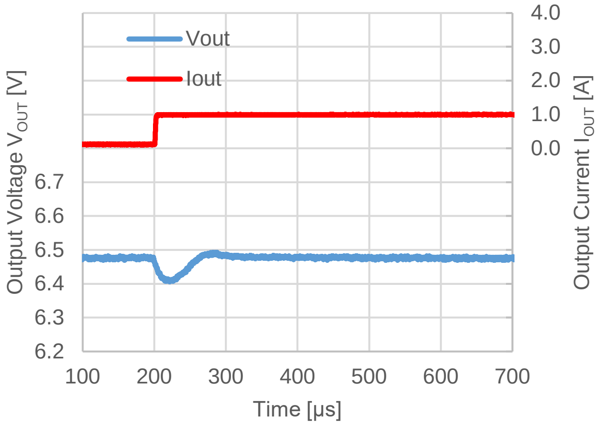
V_{OUT} = 6.5 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0 A → 3 A, Mode = L, Tr = 1 A/μs



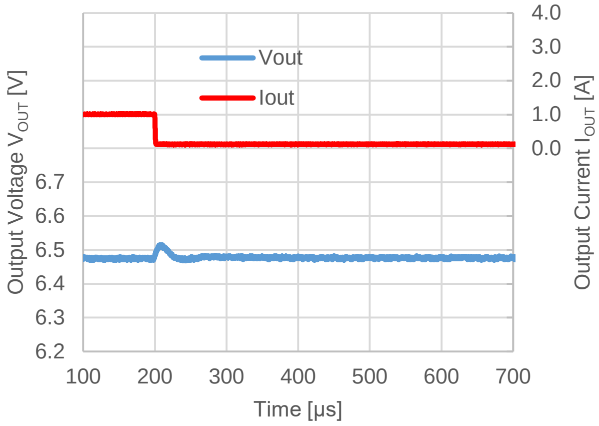
V_{OUT} = 6.5 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 3 A → 0 A, Mode = L, Tf = 1 A/μs



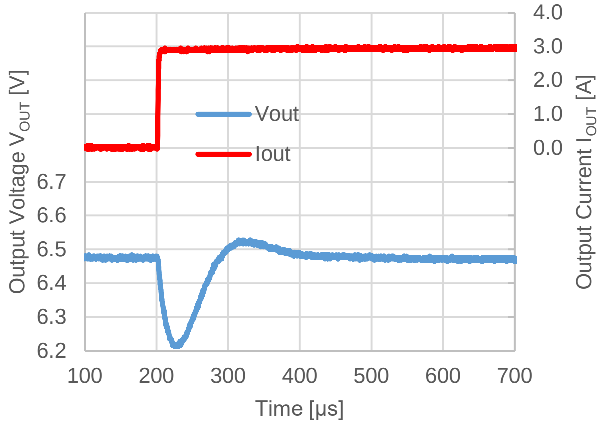
V_{OUT} = 6.5 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0.1 A → 1 A, Mode = H, Tr = 1 A/μs



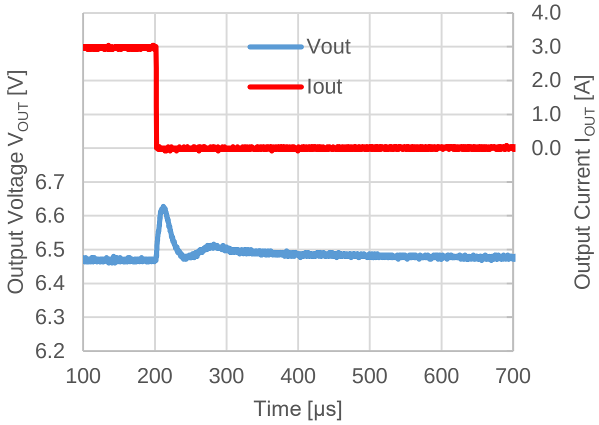
V_{OUT} = 6.5 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 1 A → 0.1 A, Mode = H, Tf = 1 A/μs



V_{OUT} = 6.5 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 0 A → 3 A, Mode = H, Tr = 1 A/μs

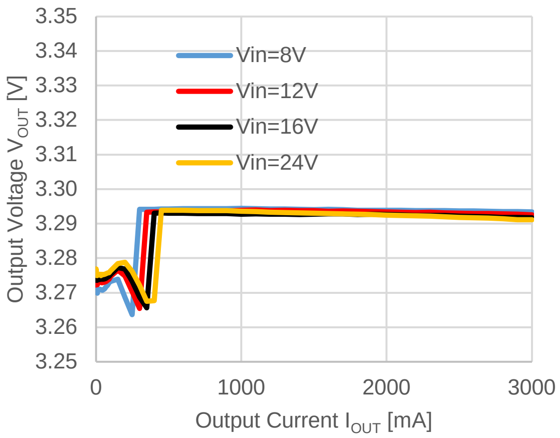


V_{OUT} = 6.5 V, V_{IN} = 12 V, f_{OSC} = 500 kHz
I_{OUT} = 3 A → 0 A, Mode = H, Tf = 1 A/μs

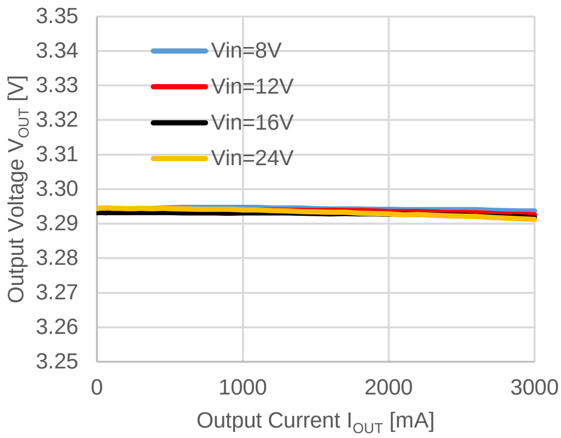


10) Load Regulation

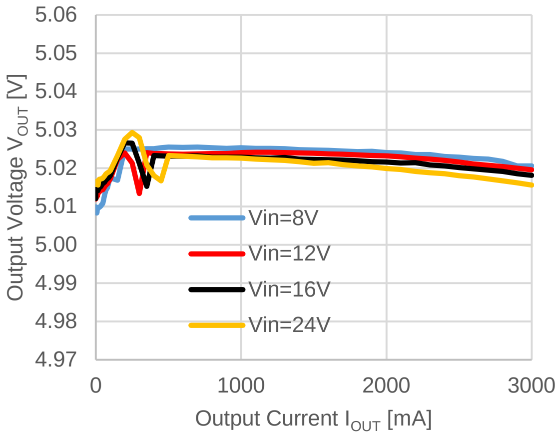
V_{OUT} = 3.3 V, f_{OSC} = 500 kHz, Mode = L



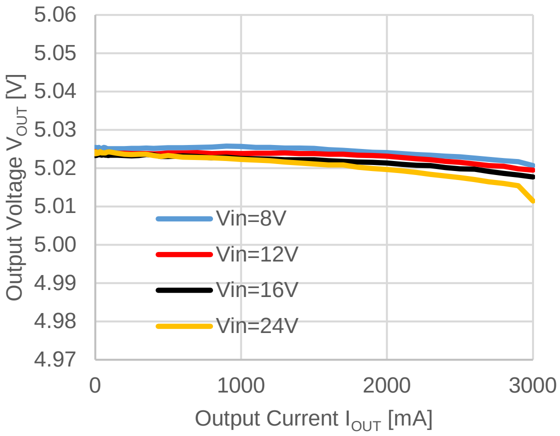
V_{OUT} = 3.3 V, f_{OSC} = 500 kHz, Mode = H



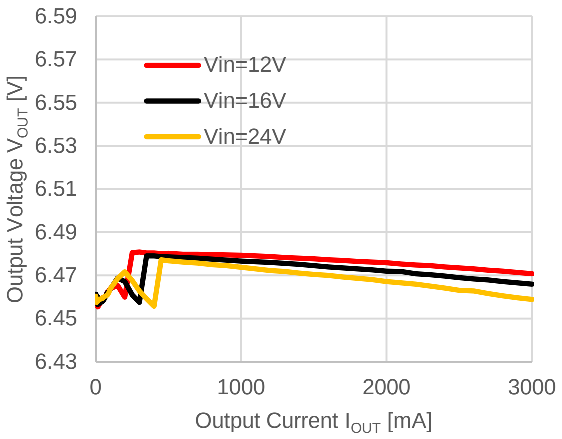
V_{OUT} = 5.0 V, f_{OSC} = 500 kHz, Mode = L



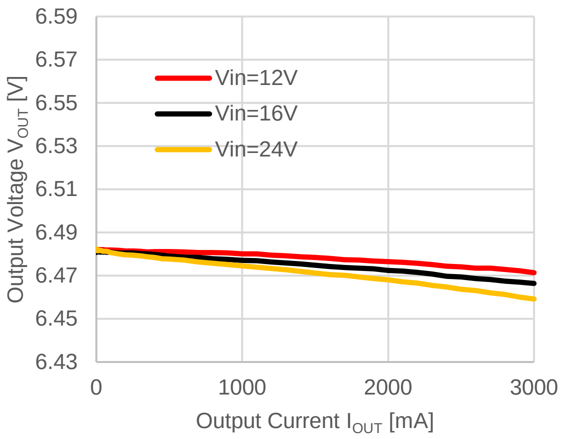
V_{OUT} = 5.0 V, f_{OSC} = 500 kHz, Mode = H



V_{OUT} = 6.5 V, f_{OSC} = 500 kHz, Mode = L

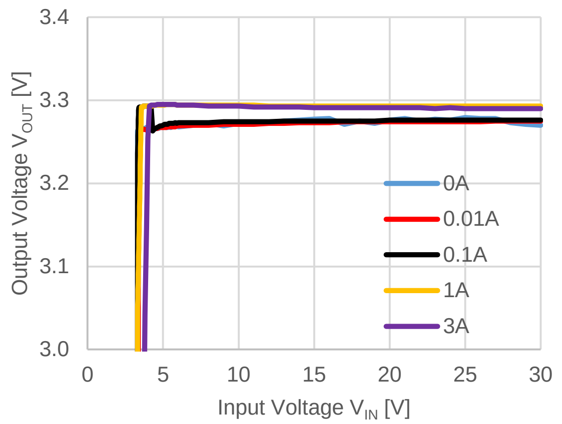


V_{OUT} = 6.5 V, f_{OSC} = 500 kHz, Mode = H

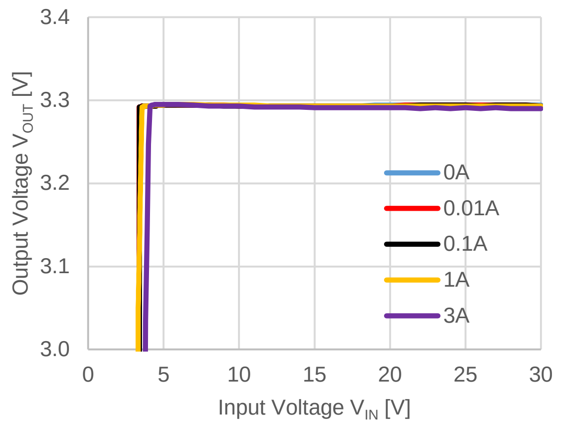


11) Line Regulation

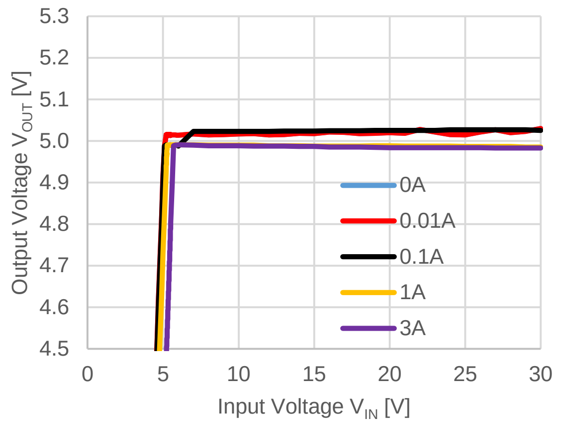
V_{OUT} = 3.3 V, f_{OSC} = 500 kHz, Mode = L



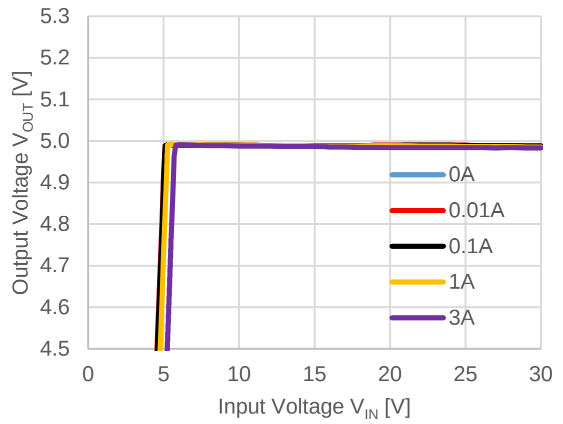
V_{OUT} = 3.3 V, f_{OSC} = 500 kHz, Mode = H



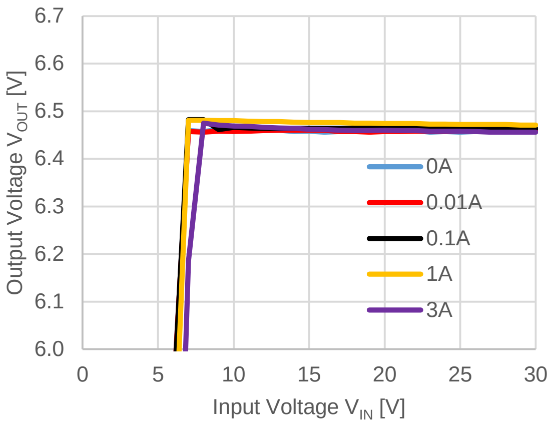
V_{OUT} = 5.0 V, f_{OSC} = 500 kHz, Mode = L



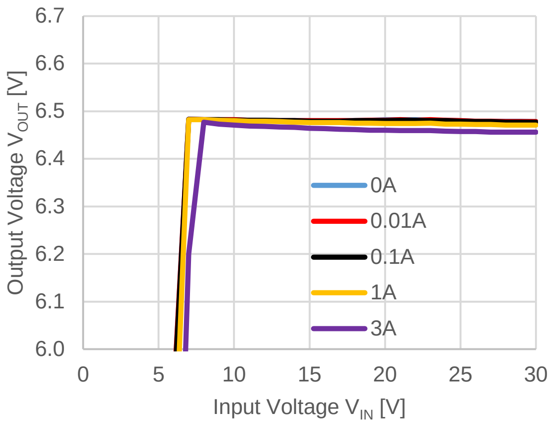
V_{OUT} = 5.0 V, f_{OSC} = 500 kHz, Mode = H



V_{OUT} = 6.5 V, f_{OSC} = 500 kHz, Mode = L

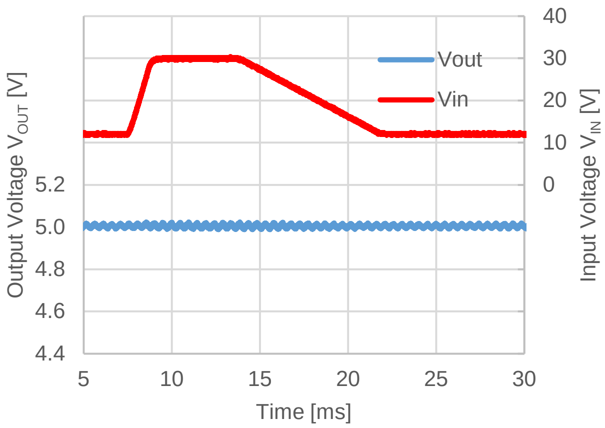


V_{OUT} = 6.5 V, f_{OSC} = 500 kHz, Mode = H

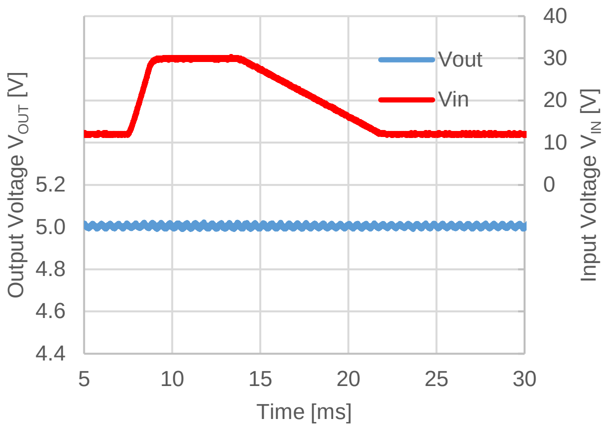


12) Transient Voltage Surge

f_{OSC} = 250 kHz, V_{IN} = 12 V ↔ 30 V
Mode = L, I_{OUT} = 0.1 A

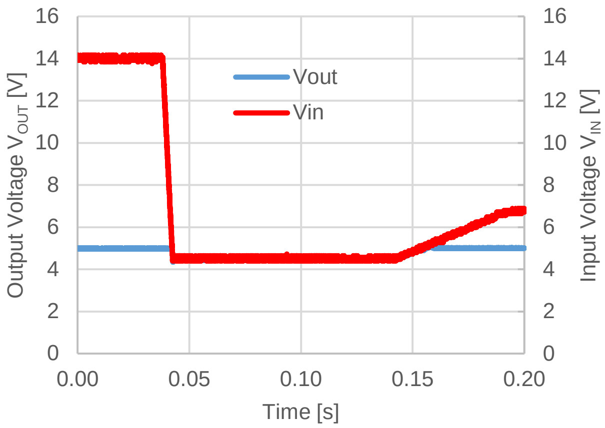


f_{OSC} = 250 kHz, V_{IN} = 12 V ↔ 30 V
Mode = H, I_{OUT} = 0.1 A

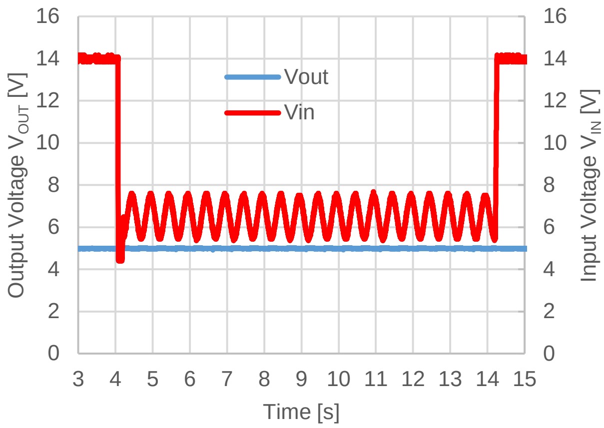


13) Cranking

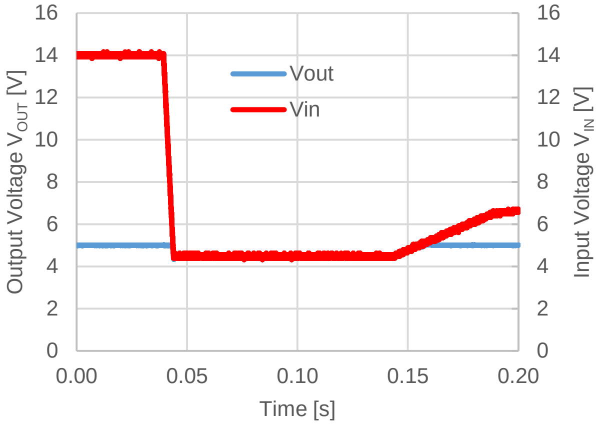
f_{OSC} = 250 kHz
Mode = L, I_{OUT} = 0.1 A



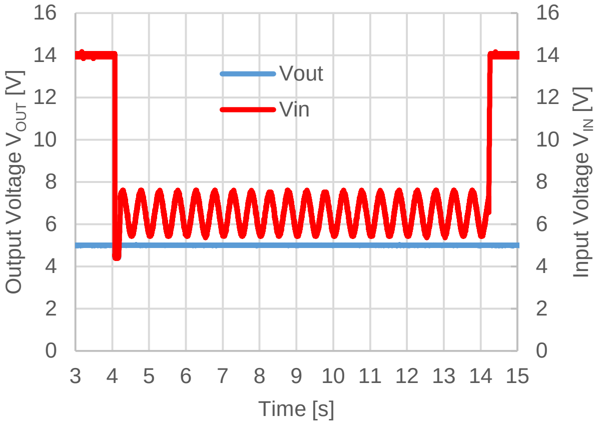
f_{OSC} = 250 kHz
Mode = L, I_{OUT} = 0.1 A



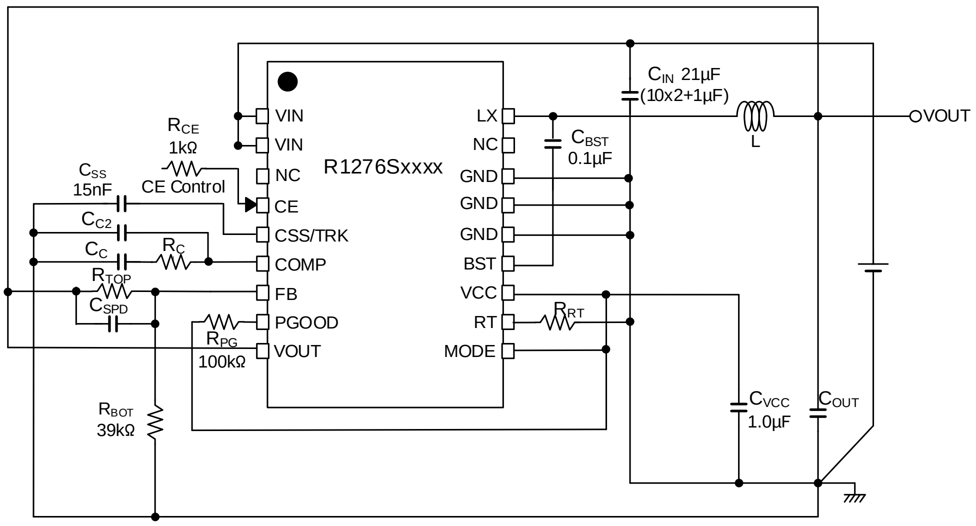
f_{OSC} = 250 kHz
Mode = H, I_{OUT} = 0.1 A



f_{OSC} = 250 kHz
Mode = H, I_{OUT} = 0.1 A



Test Circuit



Test Circuit for Typical Characteristics

Measurement Components of Typical Characteristics

R1276SxxxA/C Constant Table

Code (xxx)	F_{OSC} [kHz]	V_{OUT} [V]	L [µH]	C_{OUT} [µF]	C_{SPD} [pF]	R_{TOP} [kΩ]	R_{RT} [kΩ]	R_C [kΩ]	C_C [nF]	C_{C2} [pF]
001	250	3.3	15	200 (100×2)	100	162 (150+12)	121 (220‖270)	22	10	100
		5.0	22	200 (100×2)	100	267 (240+27)	121 (220‖270)	27	10	100
	500	3.3	10	66 (22×3)	22	162 (150+12)	56	22	3.3	33
		5.0	10	100	22	267 (240+27)	56	22	4.7	33
	1000	3.3	4.7	48.7 (22×2+4.7)	22	162 (150+12)	28.7 (220‖33)	12	3.3	15
		5.0	4.7	48.7 (22×2+4.7)	22	267 (240+27)	28.7 (220‖33)	12	3.3	15
002	500	6.5	15	147 (100+47)	22	357 (330+27)	56	22	4.7	33
004	250	0.7	3.3	430 (100+330)	1500	3.7 (2.2+1.5)	121 (220‖270)	5.1	47	150

‖: Parallel connection

Measurement Components of Typical Characteristics

Symbol	Specification	Manufacture	Parts number
Capacitor			
C_{IN}	1.0 µF, 50 V, 125°C	TDK	CGA4J3X7R1H105K
	10 µF, 50 V, 125°C		CGA6P3X7S1H106K
C_{BST}	0.1 µF, 25 V, 125°C		CGA3E2X7R1E104K
C_{VCC}	1.0 µF, 16 V, 125°C		CGA3E1X7R1V105K
C_{OUT}	4.7 µF, 25 V, 125°C		CGA5L1X7R1E475K
	22 µF, 16 V, 125°C		CGA6P1X7R1C226M
	47 µF, 16 V, 125°C		CGA9N3X7R1C476M
	100 µF, 16 V, 125°C		CKG57NX7S1C107M
Inductor			
L	3.3 µH, 5.0 A	TDK	CLF7045T-3R3-D
	4.7 µH, 5.4 A		CLF10040T-4R7N-D
	10 µH, 6.7 A		CLF12555T-100M-D
	15 µH, 5.4 A		CLF12555T-150M-D
	22 µH, 4.2 A		CLF12555T-220M-D

Ver. C

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

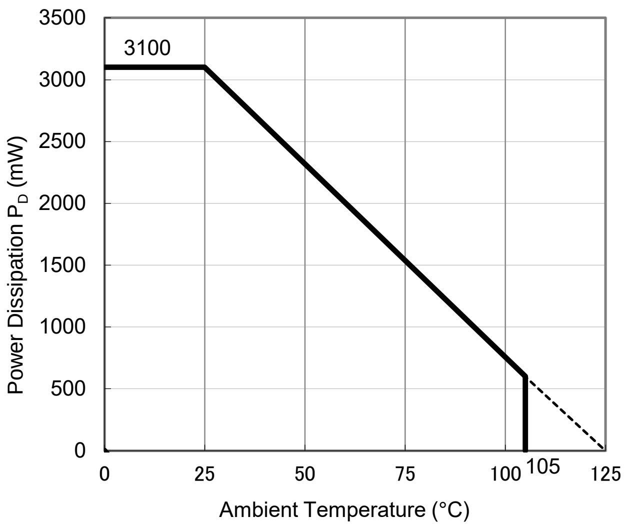
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

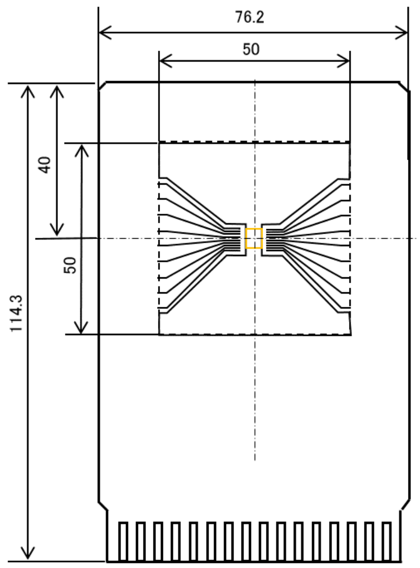
Item	Measurement Result
Power Dissipation	3100 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

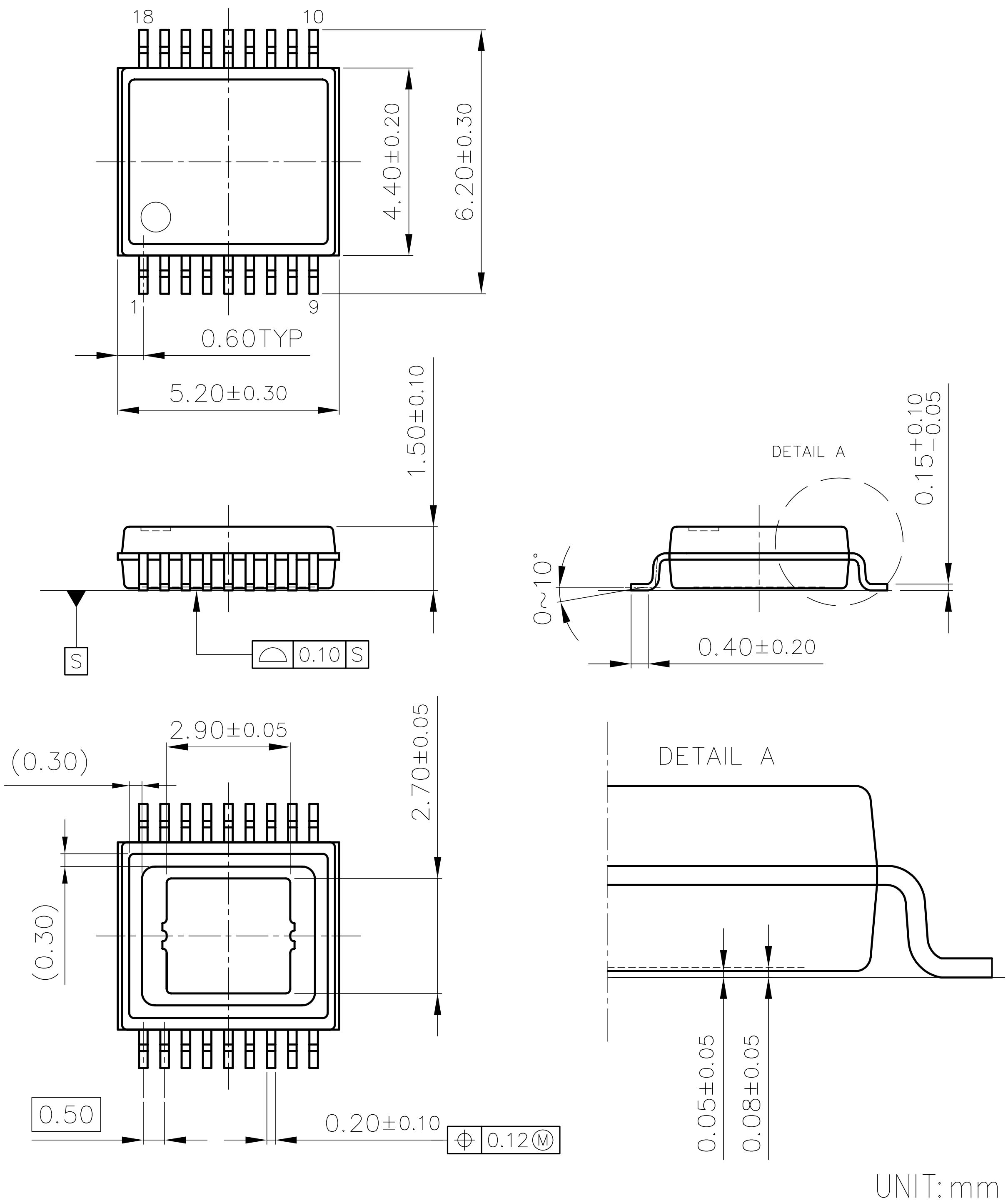


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

Ver. A



HSOP-18 Package Dimensions

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