
High Noise Immunity 42 V Input Voltage 70 mA Voltage Tracker Evaluation Board

NO.EEV-513-N001B-200703

R1540N001B-EV is the evaluation board for R1540 which has the below features, benefits and specifications.

OVERVIEW

The R1540N is a voltage tracker featuring input voltage in the range of 3.5 V to 42 V. Highly accurate output voltage which attributes to CE/ADJ pin achieves successful sequence control of the integrated off-board sensor module. Strong enough not to require the circuit to avoid external electromagnetic interference (EMI) and this contributes space saving.

KEY BENEFITS

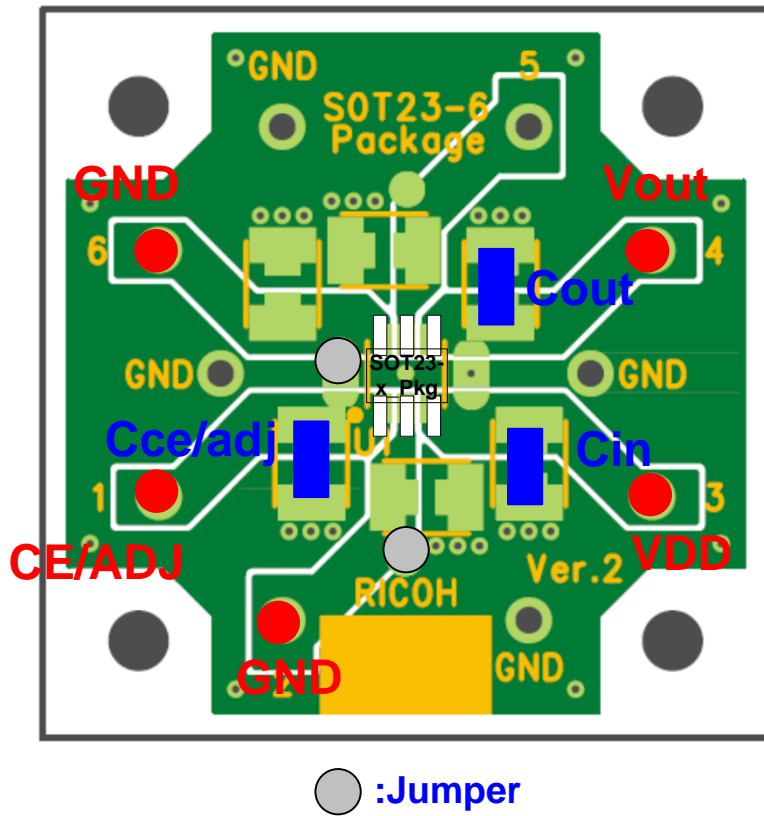
- Excellent noise immunity provides effective shielding against EMI.
- Lower stand-by current consumption leads to energy saving of the whole system to prolong battery life.
- Response to requirements for sequence control in the system with integrated sensors.

KEY SPECIFICATIONS

- Input Voltage Range (Maximum Rating): 3.5 V to 42.0 V (50.0 V)
- Supply Current: Typ. 60 μ A
- Standby Current: Typ. 0.1 μ A
- Tracking Voltage Range: 2.2 V to 14 V
- Tracking Voltage Accuracy: ± 15 mV
($-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$, $V_{\text{CE/ADJ}} = 5$ V)
- Output Current 70 mA
- Ripple Rejection: Typ. 80 dB ($f = 100$ Hz)
- Protections: Thermal Shutdown, Output Current Limiting and Short-circuit Current Limiting
- Package: SOT-23-5
- For more details on R1540 IC, please refer to
<https://www.n-redc.co.jp/en/pdf/datasheet/r1540-ea.pdf>.

PCB LAYOUT

R1540N (Package: SOT-23-5) PCB Layout



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Rating	Unit
V_{IN}	Input Voltage		-0.3 to 50	V
	Peak Voltage ⁽¹⁾		60	V
$V_{CE/ADJ}$	CE/ADJ Pin Input Voltage		-0.3 to 50	V
V_{OUT}	VOUT Pin Output Voltage		-0.3 to $V_{IN} + 0.3 \leq 50$	V
I_{OUT}	Output Current		95	mA
P_D	Power Dissipation ⁽²⁾	SOT-23-5	660	mW
	JEDEC STD. 51			
T_j	Junction Temperature Range		-40 to 125	°C
T_{stg}	Storage Temperature Range		-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

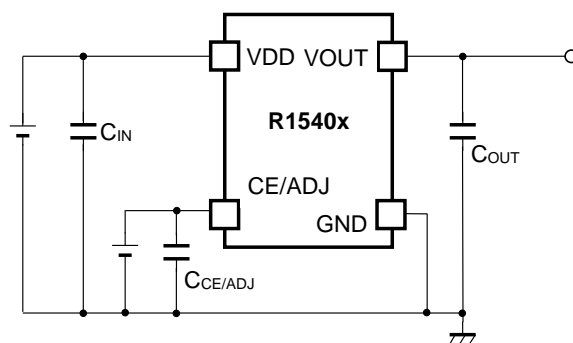
Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	3.5 to 42	V
$V_{CE/ADJ}$	CE/ADJ Input Pin Voltage	0 to 14	V
T_a	Operating Temperature Range	-40 to 105	°C

RECOMMENDED OPERATING CONDITONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Duration time: 200 ms.

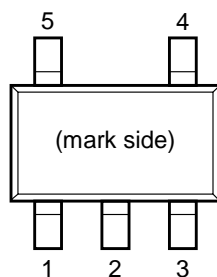
⁽²⁾ Refer to POWER DISSIPATION in the product data sheet.

TYPICAL APPLICATION**R1540N Typical Application****Recommended External Components⁽¹⁾**

Symbol Value	
C _{IN}	0.1 μF
C _{OUT}	10 μF
C _{CE/ADJ}	0.1 μF

⁽¹⁾The bill of materials will be attached on the shipment of each purchased evaluation board.

PIN DESCRIPTION



R1540N (SOT-23-5) Pin Configuration

R1540N Pin Description

Pin No.	Symbol	Description
1	CE/ADJ	Chip Enable and Adjustment Pin (Active - High)
2	GND ⁽¹⁾	Ground Pin
3	VDD	Input Pin
4	VOUT	Output Pin
5	GND ⁽¹⁾	Ground Pin

⁽¹⁾ The GND pins must be wired together on the board.

TECHNICAL NOTES

Phase Compensation

R1540N adopts capacitance and Equivalent Series Resistance (ESR) for phase compensation to ensure stable operation even with load varying current. For this end, the capacitor of 10 μF or more is essential. A certain amount of ESR may cause unstable output voltage. Fully take temperature and frequency characteristics into consideration when evaluating the circuit. Place the capacitor of 0.1 μF or more between VDD and GND with using short leads and short printed circuit traces.

PCB Layout

SOT-23-5 package: connect Nos. 2 and 5 of GND pin together.



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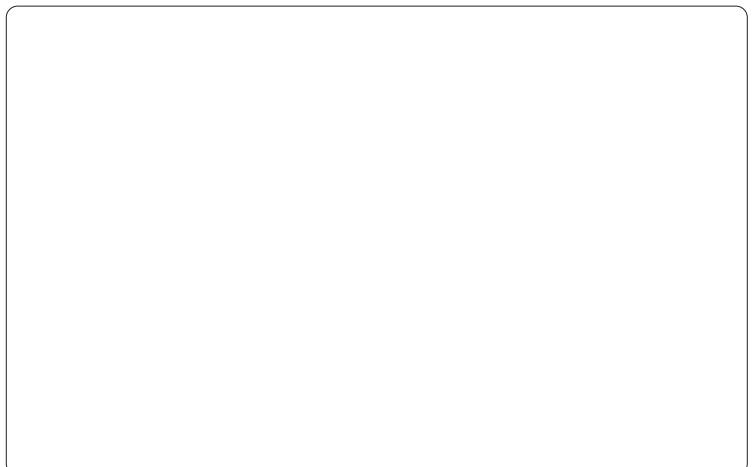
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