36V System Power Supply with Watchdog Timer for Automotive Applications

No. EC-326-191212

OUTLINE

R5110x is the system power supply and supervisor IC based on the high-voltage CMOS process technology, and has high accuracy and ultra low supply current voltage.
R5110x consists of a voltage regulator (VR), a voltage detector (VD), and a normal / window type of watchdog timer (WDT) in a chip, and can provide three functions of the system power supply, the supply voltage supervisor, and the supervision of system's misoperation.
Voltage Regulator allows the output current of 500 mA. And, VR has the inrush current protection circuit for rising pulse (Typ.400 mA or less). Voltage Detector outputs a reset signal when a reduction of supply voltage (SENSE / V_{OUT}) is detected, and the reset signal is used as system reset. The detection voltage is internally fixed in an IC. And, the delay time is adjustable with an external capacitor because VD has the built-in release delay circuit (the power-on reset circuit). When the supply voltage is higher than the release output voltage, VD maintains the reset state during the delay time. The output type of RESETB and D_{OUT} are Nch open-drain. In addition, R5110xxx2C and R5110xxx2D (Detector with SENSE pin) have a manual reset (MR) pin.
Watchdog Timer detects the microprocessor output pulse. In addition to the normal type of WDT (R5110Sxx1A / R5110xxx2C) that outputs a reset signal when the detected pulse period is longer than normal, R5110x supports the window type of WDT (R5110Sxx1B / R5110xxx2D) that outputs a reset signal when the detected pulse period is shorter or longer. RESETB outputs the reset signal when using R5110Sxx1A / R5110Sxx1B, and the WDO pin outputs "L" as the reset signal when using R5110xxx2C / R5110xxx2D. The output type of WDO is Nch open-drain. In addition, R5110xxx2C and R5110xxx2D have an inhibiting (INH) pin to stop the watchdog timer's monitoring function. The time out period of Watchdog Timer is also adjustable with an external capacitor. R5110x supports the packages of HSOP-8E, HSOP-18 and HQFN0808-28.

FEATURES

- Operating Voltage Range (Maximum Rating) ········ 3.5 V to 36.0 V (50.0 V)
- Operating Temperature Range ·························· −40°C to 125°C
- Supply Current ·· Typ. 25 µA
- Supply Current (On standby) ···························· Typ. 0.2 µA

<Voltage Regulator (VR)>

- Output Voltage Range ····································· 1.8 V to 5.0 V
- Dropout Voltage ·· Typ. 0.5 V (V_{OUT} = 5.0 V, 500 mA)
- Output Voltage Accuracy ·································· ±1.5% (−40°C ≤ Ta ≤ 125°C)
- Output Voltage Temperature Coefficient ·············· Typ. ±100 ppm/°C
- Built-in Short Current Limit Circuit ······················ Typ. 80 mA
- Built-in Overcurrent Protection Circuit ·················· Min. 500 mA

- Built-in Thermal Shutdown Circuit ······················ Typ.165°C
- Recommended Ceramic Capacitor····················· 0.1 µF or more

<Voltage Detector (VD)>

- Detector Threshold Range································ 1.6 V to 5.5 V
- Detector Threshold Accuracy ···························· ±1.8% (−40°C ≤ Ta ≤ 125°C)
- Release Delay Accuracy ································· ±20% (−40°C ≤ Ta ≤ 125°C)
- Release Delay Time······································ Typ. 242 ms (C_D = 0.22 µF)

  Delay Time is adjustable with an external capacitor.

<Watchdog Timer (WDT)>

- Open Window Accuracy··································· ±20% (−40°C ≤ Ta ≤ 125°C)
- Open Window Time ······································· Typ.18 ms (C_{TW} = 10 nF)
- Closed Window Time ····································· Typ.18 ms (C_{TW} = 10 nF)
- Long Open Window Time ································ Typ.72 ms (C_{TW} = 10 nF)
- Ignoring Time ·· Typ.18 ms (C_{TW} = 10 nF)
- Monitoring Time ·· Typ.18 ms (C_{TW} = 10 nF)
- Reset Time ··· Typ.9.5 ms (C_{TW} = 10 nF)

  Each time is adjustable with an external capacitor.

APPLICATIONS

- Power source for car accessories including car audio equipment, car navigation system, and ETC system.
- Power source for control units including EV inverter and charge control.

SELECTION GUIDE

R5110x user selectable options (Watchdog Timer type, Detector type, and additional functions with using MR / INH / WDO pins) are as follows:

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5110Sxx1∗-E2-#E	HSOP-8E	1,000 pcs	Yes	Yes
R5110Sxx2∗-E2-#E	HSOP-18	1,000 pcs	Yes	Yes
R5110Lxx2∗-TR-#E	HQFN0808-28	2,000pcs	Yes	Yes

xx: Specify the set output voltage (V_{SET}) and the set detector threshold ($-V_{SET}$) by using serial numbers starting from 01.
Refer to "*Mark Specification Table*" for details.

∗:

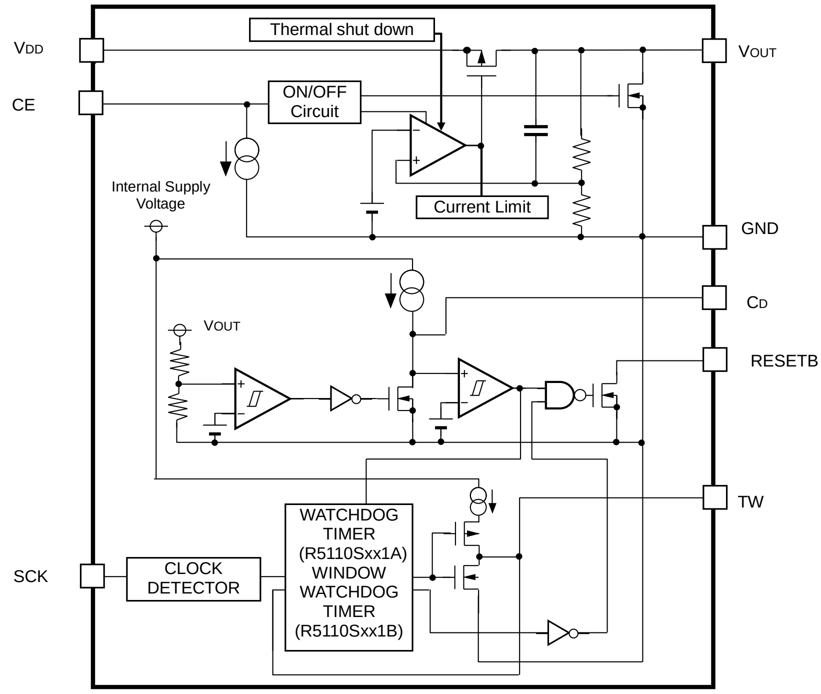
	Detector Monitoring Voltage	Package	Watchdog Timer Type	MR / INH / WDO pins	RESETB/ D_{OUT} pins
A	V_{OUT}	HSOP-8E	Normal	−	RESETB
B	V_{OUT}	HSOP-8E	Window	−	RESETB
C	SENSE	HSOP-18 HQFN0808-28	Normal	Yes	D_{OUT}
D	SENSE	HSOP-18 HQFN0808-28	Window	Yes	D_{OUT}

#: Quality Class

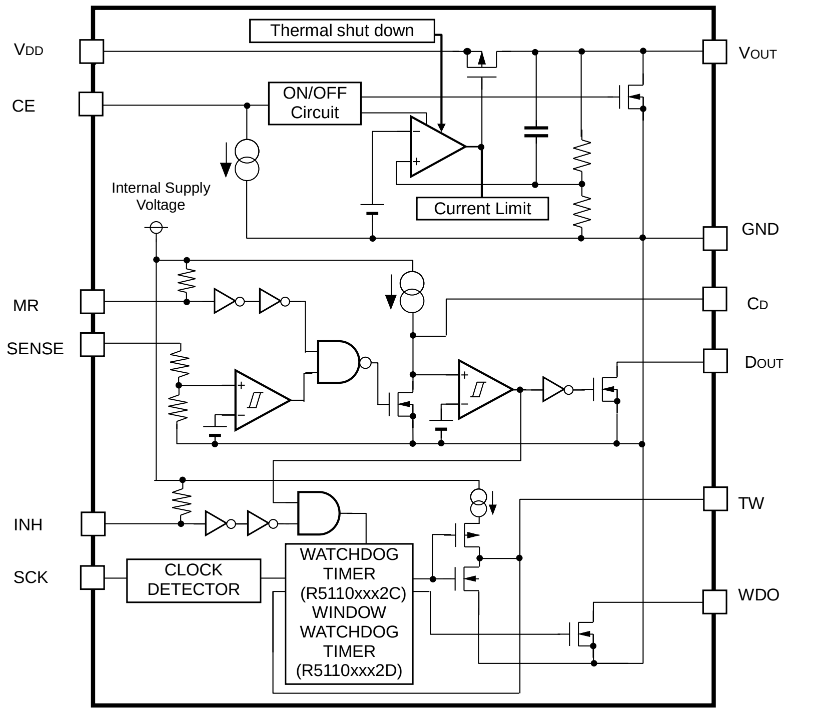
#	Operating Temperature Range	Test Temperature	AEC-Q100
A	-40°C to 125°C	25°C, High	Grade 1
K	-40°C to 125°C	Low, 25°C, High	Grade 1

BLOCK DIAGRAMS

R5110Sxx1A / R5110Sxx1B



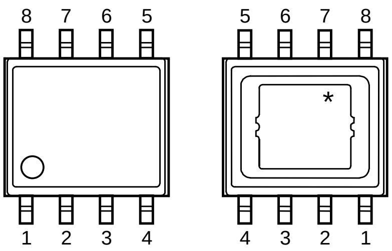
R5110xxx2C / R5110xxx2D



PIN DESCRIPTION

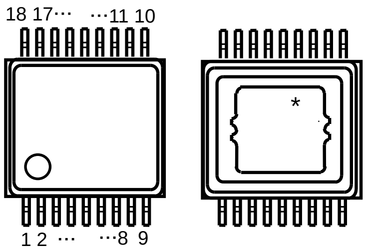
• **HSOP-8E**

Top View **Bottom View**



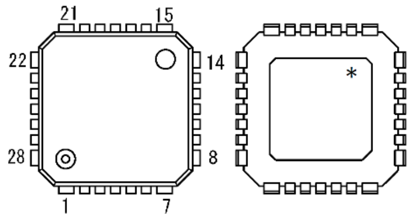
• **HSOP-18**

Top View **Bottom View**



• **HQFN0808-28**

Top View **Bottom View**



HSOP-8E (R5110Sxx1A / R5110Sxx1B)

Pin No.	Symbol	Description
1	V_{DD}	Supply Voltage pin
2	CE	Chip Enable pin (Active "H")
3	GND	GND pin
4	C_D	VD Release Delay Time Set pin
5	TW	WDT Monitoring Time Set pin
6	SCK	WDT Pulse Input pin
7	RESETB[(1)]	Reset Output pin (Active "L"), Nch Open Drain Output type
8	V_{OUT}	VR Output pin

∗ The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left open.

(1) RESETB pin is required to pull up to a suitable voltage with an external capacitor.

HSOP-18 (R5110Sxx2C / R5110Sxx2D)

Pin No.	Symbol	Description
1	V_{DD}	Supply Voltage pin
2	CE	Chip Enable pin (Active "H")
3	NC	No Connection
4	NC	No Connection
5	GND	GND pin
6	NC	No Connection
7	NC	No Connection
8	C_D	VD Release Delay Time Set pin
9	MR	Manual Reset pin (Active "L")
10	TW	WDT Monitoring Time Set pin
11	INH	Inhibition pin (Active "L")
12	SCK	WDT Pulse Input pin
13	WDO[1]	WDT Output pin, Nch Open Drain Output type
14	D_{OUT}[2]	Reset Output pin (Active "L"), Nch Open Drain Output type
15	SENSE	VD Voltage SENSE pin
16	NC	No Connection
17	NC	No Connection
18	V_{OUT}	VR Output pin

∗ The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left open.

[1] WDO pin is required to pull up to a suitable voltage with an external capacitor.
[2] D_{OUT} pin is required to pull up to a suitable voltage with an external capacitor.

HQFN0808-28 (R5110Lxx2C / R5110Lxx2D)

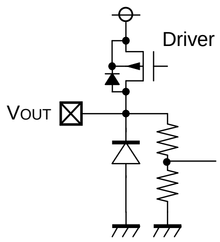
Pin No.	Symbol	Description
1	GND	GND pin
2	NC	No Connection
3	V_{DD}	Supply Voltage pin
4	NC	No Connection
5	CE	Chip Enable pin (Active "H")
6	NC	No Connection
7	GND	GND pin
8	GND	GND pin
9	GND	GND pin
10	C_D	VD Release Delay Time Set pin
11	MR	Manual Reset pin (Active "L")
12	TW	WDT Monitoring Time Set pin
13	INH	Inhibition pin (Active "L")
14	GND	GND pin
15	GND	GND pin
16	SCK	WDT Pulse Input pin
17	NC	No Connection
18	WDO(1)	WDT Output pin, Nch Open Drain Output type
19	D_{OUT}(2)	Reset Output pin (Active "L"), Nch Open Drain Output type
20	SENSE	VD Voltage SENSE pin
21	GND	GND pin
22	GND	GND pin
23	NC	No Connection
24	NC	No Connection
25	NC	No Connection
26	V_{OUT}	VR Output pin
27	NC	No Connection
28	GND	GND pin

∗ The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left open.

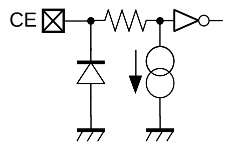
(1) WDO pin is required to pull up to a suitable voltage with an external capacitor.
(2) DOUT pin is required to pull up to a suitable voltage with an external capacitor.

PIN EQUIVALENT CIRCUIT DIAGRAMS

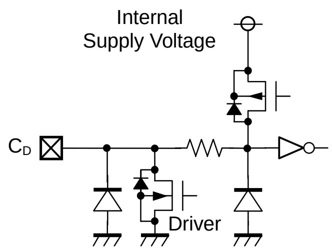
<V_{OUT} pin>



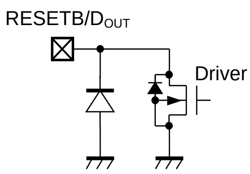
<CE pin>



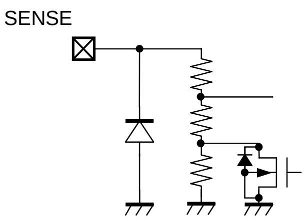
<C_D pin>



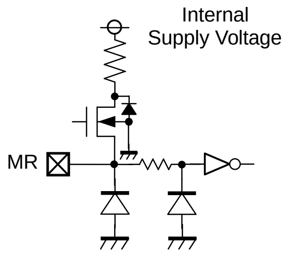
<RESETB pin(R5110Sxx1x) / D_{OUT} pin(R5110xxx2x)>



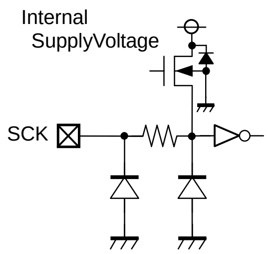
<SENSE pin (R5110xxx2x)>



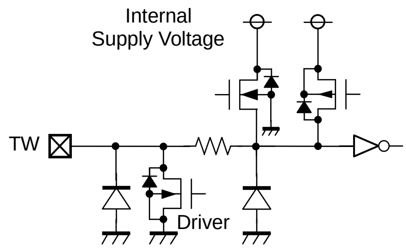
<MR pin (R5110xxx2x)>



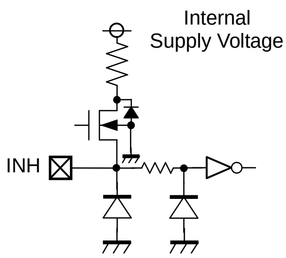
<SCK pin>



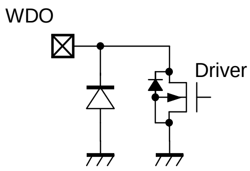
<TW pin>



<INH pin (R5110xxx2x)>



<WDO pin (R5110xxx2x)>



ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	−0.3 to 50	V
V_{IN}	Peak Voltage[1]	60	V
V_{CE}	CE Pin Input Voltage	−0.3 to 50	V
V_{OUT}	Output Voltage	−0.3 to V_{IN} +0.3 ≤ 50	V
V_{CD}	C_D Pin Output Voltage	-0.3 to 7.0	V
V_{TW}	TW Pin Output Voltage	-0.3 to 7.0	V
V_{RESETB}	RESETB Pin Output Voltage	-0.3 to 7.0	V
V_{DOUT}	D_{OUT} Pin Output Voltage	-0.3 to 7.0	V
V_{WDO}	WDO Pin Output Voltage	-0.3 to 7.0	V
V_{SCK}	SCK Pin Input Voltage	-0.3 to 7.0	V
V_{INH}	INH Pin Input Voltage	-0.3 to 7.0	V
V_{MR}	MR Pin Input Voltage	-0.3 to 7.0	V
V_{SENSE}	SENSE Pin Input Voltage	-0.3 to 7.0	V
P_D	Power Dissipation [2] HSOP-8E (JEDEC STD.51)	3600	mW
P_D	Power Dissipation [2] HSOP-18 (JEDEC STD.51)	3900	mW
P_D	Power Dissipation [2] HQFN0808-28 (JEDEC STD.51)	5800	mW
Tj	Junction Temperature	−40 to 150	°C
Tstg	Storage Temperature	−55 to 150	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	3.5 to 36.0	V
V_{CE}	CE Pin Input Voltage	0 to 36.0	V
V_{SCK}	SCK Pin Input Voltage	0 to 5.5	V
V_{INH}	INH Pin Input Voltage	0 to 5.5	V
V_{MR}	MR Pin Input Voltage	0 to 5.5	V
V_{SENSE}	SENSE Pin Input Voltage	0 to 5.5	V
Ta	Operating Temperature Range	−40 to 125	°C

RECOMMENDED OPERATING CONDITONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

[1] Within application time of 200 ms
[2] Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

C_{IN} = C_{OUT} = 0.1µF, V_{IN} = 14 V, unless otherwise noted.
The specification in ☐ is checked and guaranteed by design engineering at −40°C ≤ Ta ≤ 125°C.

R5110xxxxx-AE

(Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Supply Current	I_{OUT} = 0 mA		25	38	µA
Istandby	Power Consumption (on standby)	V_{IN} = 36 V, V_{CE} = 0 V		0.2	4.0	µA
I_{PD}	CE Pull-downConstant Current	VCE = 5 V		0.2	0.6	µA
		VCE = 36 V		0.5	1.3	µA
V_{CEH}	CE Input Voltage «H»		2.2		36	V
V_{CEL}	CE Input Voltage «L»				1.0	V

VR Part

(Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	I_{OUT} = 1 mA	×0.985		×1.015	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = V_{SET} + 2.0 V 1mA ≦ I_{OUT} ≦ 500 mA	-20	0	30	mV
V_{DIF}	Dropout Voltage	I_{OUT} = 500mA, V_{SET} = 1.8		1.70	1.90	V
		V_{SET} = 2.5		1.00	1.55	V
		V_{SET} = 3.3		0.60	1.20	V
		V_{SET} = 5.0		0.50	0.95	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	3.5V ≦ V_{SET} + 0.5V ≦ V_{IN} ≦ 36V I_{OUT} = 1 mA		0.01	0.02	%/V
I_{LIM}	Output Current Limit	V_{IN} = V_{SET} + 3.0 V	500	750	1000	mA
I_{SC}	Short current Limit	V_{IN} = 5 V, V_{OUT} = 0 V	35	80	135	mA
T_{TSD}	Thermal Shutdown Temperature	Junction Temperature	150	165		°C
T_{TSR}	Thermal Shutdown Release Temperature	Junction Temperature	125	140		°C
R_{LOW}	V_{OUT} Low Output Nch Tr.ON Resistance	V_{CE} = 0 V, V_{OUT} = 0.1 V		3.2	7.0	kΩ

C_{IN} = C_{OUT} = 0.1 µF, V_{IN} = 14 V, unless otherwise noted.
The specification in ☐ is checked and guaranteed by design engineering at −40°C ≤ Ta ≤ 125°C.

VD Part (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
$-V_{DET}$	Detector Threshold	V_{OUT} Set Detector Threshold	x0.982		x1.018	V
V_{HYS}	Detector Threshold Hysteresis		$(-V_{DET})$ x0.01	$(-V_{DET})$ x0.02	$(-V_{DET})$ x0.03	V
tdelay	Release Output Delay Time (Power-On Reset)	C_D = 0.22 µF	194	242	290	ms
V_{RESETB}	RESETB Pull-up Voltage	R5110Sxx1A / R5110Sxx1B			5.5	V
V_{DOUT}	D_{OUT} Pull-up Voltage	R5110xxx2C / R5110xxx2D			5.5	V
$I_{OUTNRSTB}$	Nch. Output Current (RESETB Output Pin)	R5110Sxx1A / R5110Sxx1B V_{IN} = 3.5 V, V_{RESETB} = 0.1 V	0.7	1.5		mA
$I_{LEAKRSTB}$	Nch. Leakage Current (RESETB Output Pin)	R5110Sxx1A / R5110Sxx1B V_{RESETB} = 5.5 V			0.3	µA
$I_{OUTDOUT}$	Nch. Output Current (D_{OUT} Output Pin)	R5110xxx2C / R5110xxx2D V_{IN} = 3.5 V, V_{DOUT} = 0.1 V	0.7	1.5		mA
$I_{LEAKDOUT}$	Nch. Leakage Current (D_{OUT} Output Pin)	R5110xxx2C / R5110xxx2D V_{DOUT} = 5.5 V			0.3	µA
V_{MRH}	MR Input “H”		1.5		5.5	V
V_{MRL}	MR Input “L”		0		0.6	V
MRW	MR Input Pulse Width		2			µs
RMR	MR Pull-up Resistance		50	110	160	kΩ
R_{LCD}	C_D Pin Discharge Nch Tr.ON Resistance	V_{CE} = 0 V, V_{CD} = 0.1 V		7.5	20	kΩ

No. EC-326-191212

C_{IN} = C_{OUT} = 0.1µF, V_{IN} = 14 V, unless otherwise noted.
The specification in ☐ is checked and guaranteed by design engineering at −40°C ≤ Ta ≤ 125°C.

WDT Part (Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
t_{OW}	Open Window Time	R5110Sxx1B/ R5110xxx2D	C_{TW} = 10 nF	14.4	18.0	21.6	ms
t_{CW}	Closed Window Time			14.4	18.0	21.6	ms
t_{OWL}	Long Open Window Time			36.0	72.0	108.0	ms
t_{IGN}	Ignoring Time	C_{TW} = 10 nF		14.4	18.0	21.6	ms
t_{WD}	Monitoring Time	R5110Sxx1A/ R5110xxx2C	C_{TW} = 10 nF	14.4	18.0	21.6	ms
t_{WR}	Reset Time	C_{TW} = 10 nF		7.6	9.5	11.4	ms
V_{SCKH}	SCK Input "H"			1.5		5.5	V
V_{SCKL}	SCK Input "L"			0		0.65	V
V_{INHH}	INH Input "H"			1.5		5.5	V
V_{INHL}	INH Input "L"			0		0.6	V
R_{INH}	INH Pull-up Resistance			50	110	160	kΩ
t_{SCKWH}	SCK Minimum Input Pulse Width "H"	V_{SCKL} = 0.5, V_{SCKH} = 1.6		500			ns
t_{SCKWL}	SCK Minimum Input Pulse Width "L"	V_{SCKL} = 0.5, V_{SCKH} = 1.6		1500			ns
V_{WDO}	WDO Pull-up Voltage					5.5	V
$I_{OUTNWDO}$	Nch. Output Current (WDO Output Pin)	R5110xxx2C / R5110xxx2D V_{IN} = 3.5 V, V_{DS} = 0.1 V		0.7	1.5		mA
$I_{LEAKWDO}$	Nch. Leakage Current (WDO Output Pin)	R5110xxx2C / R5110xxx2D V_{WDO} = 5.5 V				0.3	µA
R_{LTW}	C_{TW} Discharge Nch Tr.ON Resistance	V_{CE} = 0 V, V_{CTW} = 0.1 V			7.5	20	kΩ

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

Product-specific Electrical Characteristics

The specification in ☐ is checked and guaranteed by design engineering at −40°C ≤ Ta ≤ 125°C.

R5110xxxxx-AE Product-specific Electrical Characteristics

VR Part (Ta = 25°C)

Product Name	V_{OUT} [V]			V_{DIF} [V]	
	Min.	Typ.	Max.	Typ.	Max.
R5110x01xx	4.925	5.000	5.075	0.50	0.95
R5110x02xx	1.773	1.800	1.827	1.70	1.90
R5110x03xx	4.925	5.000	5.075	0.50	0.95
R5110x04xx	4.925	5.000	5.075	0.50	0.95
R5110x05xx	4.925	5.000	5.075	0.50	0.95
R5110x06xx	4.925	5.000	5.075	0.50	0.95
R5110x07xx	4.925	5.000	5.075	0.50	0.95
R5110x08xx	3.251	3.300	3.349	0.60	1.20
R5110x09xx	3.251	3.300	3.349	0.60	1.20
R5110x10xx	3.251	3.300	3.349	0.60	1.20
R5110x11xx	3.251	3.300	3.349	0.60	1.20
R5110x12xx	4.925	5.000	5.075	0.50	0.95
R5110x13xx	3.349	3.400	3.451	0.60	1.20
R5110x142x	3.251	3.300	3.349	0.60	1.20

VD Part (Ta = 25°C)

Product Name	$-V_{DET}$ [V]			V_{HYS} [V]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
R5110x01xx	4.518	4.600	4.682	0.046	0.092	0.138
R5110x02xx	1.572	1.600	1.628	0.016	0.032	0.048
R5110x03xx	4.419	4.500	4.581	0.045	0.090	0.135
R5110x04xx	4.321	4.400	4.479	0.044	0.088	0.132
R5110x05xx	4.223	4.300	4.377	0.043	0.086	0.129
R5110x06xx	4.125	4.200	4.275	0.042	0.084	0.126
R5110x07xx	3.634	3.700	3.766	0.037	0.074	0.111
R5110x08xx	2.946	3.000	3.054	0.030	0.060	0.090
R5110x09xx	2.848	2.900	2.952	0.029	0.058	0.087
R5110x10xx	2.750	2.800	2.850	0.028	0.056	0.084
R5110x11xx	2.652	2.700	2.748	0.027	0.054	0.081
R5110x12xx	4.027	4.100	4.173	0.041	0.082	0.123
R5110x13xx	3.045	3.100	3.155	0.031	0.062	0.093
R5110x142x	4.518	4.600	4.682	0.046	0.092	0.138

No. EC-326-191212

C_{IN} = C_{OUT} = 0.1µF, V_{IN} = 14 V, unless otherwise noted.

R5110xxxxx-KE (−40°C ≤ Ta ≤ 125°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Supply Current	I_{OUT} = 0 mA		25	38	µA
Istandby	Power Consumption (on standby)	V_{IN} = 36 V, V_{CE} = 0 V		0.2	4.0	µA
I_{PD}	CE Pull-down Constant Current	VCE = 5 V		0.2	0.6	µA
		VCE = 36 V		0.5	1.3	µA
V_{CEH}	CE Input Voltage «H»		2.2		36	V
V_{CEL}	CE Input Voltage «L»				1.0	V

VR Part (−40°C ≤ Ta ≤ 125°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	I_{OUT} =1 mA		×0.985		×1.015	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = V_{SET} + 2.0 V 1mA ≤ I_{OUT} ≤ 500 mA		-20	0	30	mV
V_{DIF}	Dropout Voltage	I_{OUT} = 500mA	V_{SET} = 1.8		1.70	1.90	V
			V_{SET} = 2.5		1.00	1.55	V
			V_{SET} = 3.3		0.60	1.20	V
			V_{SET} = 5.0		0.50	0.95	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	3.5V ≤ V_{SET} + 0.5V ≤ V_{IN} ≤ 36V I_{OUT} = 1 mA			0.01	0.02	%/V
I_{LIM}	Output Current Limit	V_{IN} = V_{SET} + 3.0 V		500	750	1000	mA
I_{SC}	Short current Limit	V_{IN} = 5 V, V_{OUT} = 0 V		35	80	135	mA
T_{TSD}	Thermal Shutdown Temperature	Junction Temperature		150	165		°C
T_{TSR}	Thermal Shutdown Release Temperature	Junction Temperature		125	140		°C
R_{LOW}	V_{OUT} Low Output Nch Tr.ON Resistance	V_{CE} = 0 V, V_{OUT} = 0.1 V			3.2	7.0	kΩ

C_{IN} = C_{OUT} = 0.1 µF, V_{IN} = 14 V, unless otherwise noted.

VD Part (−40°C ≤ Ta ≤ 125°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
$-V_{DET}$	Detector Threshold	V_{OUT} Set Detector Threshold	x0.982		x1.018	V
V_{HYS}	Detector Threshold Hysteresis		($-V_{DET}$) x0.01	($-V_{DET}$) x0.02	($-V_{DET}$) x0.03	V
tdelay	Release Output Delay Time (Power-On Reset)	C_D = 0.22 µF	194	242	290	ms
V_{RESETB}	RESETB Pull-up Voltage	R5110Sxx1A / R5110Sxx1B			5.5	V
V_{DOUT}	D_{OUT} Pull-up Voltage	R5110xxx2C / R5110xxx2D			5.5	V
$I_{OUTNRSTB}$	Output Current (RESETB Output Pin)	R5110Sxx1A / R5110Sxx1B Nch, V_{DD} = 3.5 V, V_{DS} = 0.1 V	0.7	1.5		mA
$I_{LEAKRSTB}$	Nch Leakage Current (RESETB Output Pin)	R5110Sxx1A / R5110Sxx1B V_{RESETB} = 5.5 V			0.3	µA
$I_{OUTDOUT}$	Output Current (D_{OUT} Output Pin)	R5110xxx2C / R5110xxx2D Nch, V_{DD} = 3.5 V, V_{DS} = 0.1 V	0.7	1.5		mA
$I_{LEAKDOUT}$	Nch Leakage Current (D_{OUT} Output Pin)	R5110xxx2C / R5110xxx2D V_{DOUT} = 5.5 V			0.3	µA
V_{MRH}	MR Input “H”		1.5		5.5	V
V_{MRL}	MR Input “L”		0		0.6	V
MRW	MR Input Pulse Width		2			µs
RMR	MR Pull-up Resistance		50	110	160	kΩ
R_{LCD}	C_D Pin Discharge Nch Tr.ON Resistance	V_{CE} = 0 V, V_{CD} = 0.1 V		7.5	20	kΩ

C_{IN} = C_{OUT} = 0.1 µF, V_{IN} = 14 V, unless otherwise noted.

WDT Part (−40°C ≤ Ta ≤ 125°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
t_{OW}	Open Window Time	R5110Sxx1B/ R5110xxx2D	C_{TW} = 10 nF	14.4	18.0	21.6	ms
t_{CW}	Closed Window Time	R5110Sxx1B/ R5110xxx2D	C_{TW} = 10 nF	14.4	18.0	21.6	ms
t_{OWL}	Long Open Window Time	R5110Sxx1B/ R5110xxx2D	C_{TW} = 10 nF	36.0	72.0	108.0	ms
t_{IGN}	Ignoring Time	C_{TW} = 10 nF		14.4	18.0	21.6	ms
t_{WD}	Monitoring Time	R5110Sxx1A/ R5110xxx2C	C_{TW} = 10 nF	14.4	18.0	21.6	ms
t_{WR}	Reset Time	C_{TW} = 10 nF		7.6	9.5	11.4	ms
V_{SCKH}	SCK Input “H”			1.5		5.5	V
V_{SCKL}	SCK Input “L”			0		0.65	V
V_{INHH}	INH Input “H”			1.5		5.5	V
V_{INHL}	INH Input “L”			0		0.6	V
R_{INH}	INH Pull-up Resistance			50	110	160	kΩ
t_{SCKWH}	SCK Minimum Input Pulse Width “H”	V_{SCKL} =0.5, V_{SCKH} =1.6		500			ns
t_{SCKWL}	SCK Minimum Input Pulse Width “L”	V_{SCKL} =0.5, V_{SCKH} =1.6		1500			ns
V_{WDO}	WDO Pull-up Voltage					5.5	V
$I_{OUTNWDO}$	Output Current (WDO Output Pin)	R5110xxx2C / R5110xxx2D V_{DD} = 3.5 V, V_{DS} = 0.1 V		0.7	1.5		mA
$I_{LEAKWDO}$	Nch Leakage Current (WDO Output Pin)	R5110xxx2C / R5110xxx2D V_{WDO} = 5.5 V				0.3	µA
R_{LTW}	C_{TW} Discharge Nch Tr.ON Resistance	V_{CE} = 0 V, V_{CTW} = 0.1 V			7.5	20	kΩ

Product-specific Electrical Characteristics

R5110xxxxx-KE Product-specific Electrical Characteristics

VR Part (−40°C ≤ Ta ≤ 125°C)

Product Name	V_{OUT} [V]			V_{DIF} [V]	
	Min.	Typ.	Max.	Typ.	Max.
R5110x01xx	4.925	5.000	5.075	0.50	0.95
R5110x02xx	1.773	1.800	1.827	1.70	1.90
R5110x03xx	4.925	5.000	5.075	0.50	0.95
R5110x04xx	4.925	5.000	5.075	0.50	0.95
R5110x05xx	4.925	5.000	5.075	0.50	0.95
R5110x06xx	4.925	5.000	5.075	0.50	0.95
R5110x07xx	4.925	5.000	5.075	0.50	0.95
R5110x08xx	3.251	3.300	3.349	0.60	1.20
R5110x09xx	3.251	3.300	3.349	0.60	1.20
R5110x10xx	3.251	3.300	3.349	0.60	1.20
R5110x11xx	3.251	3.300	3.349	0.60	1.20
R5110x12xx	4.925	5.000	5.075	0.50	0.95
R5110x13xx	3.349	3.400	3.451	0.60	1.20
R5110x142x	3.251	3.300	3.349	0.60	1.20

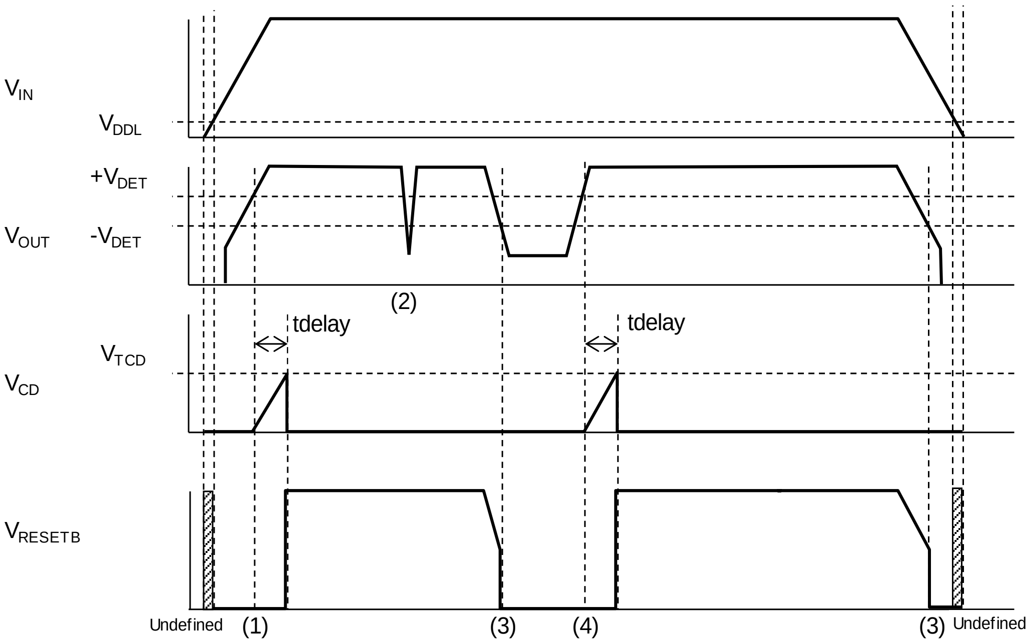
VD Part (−40°C ≤ Ta ≤ 125°C)

Product Name	$-V_{DET}$ [V]			V_{HYS} [V]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
R5110x01xx	4.518	4.600	4.682	0.046	0.092	0.138
R5110x02xx	1.572	1.600	1.628	0.016	0.032	0.048
R5110x03xx	4.419	4.500	4.581	0.045	0.090	0.135
R5110x04xx	4.321	4.400	4.479	0.044	0.088	0.132
R5110x05xx	4.223	4.300	4.377	0.043	0.086	0.129
R5110x06xx	4.125	4.200	4.275	0.042	0.084	0.126
R5110x07xx	3.634	3.700	3.766	0.037	0.074	0.111
R5110x08xx	2.946	3.000	3.054	0.030	0.060	0.090
R5110x09xx	2.848	2.900	2.952	0.029	0.058	0.087
R5110x10xx	2.750	2.800	2.850	0.028	0.056	0.084
R5110x11xx	2.652	2.700	2.748	0.027	0.054	0.081
R5110x12xx	4.027	4.100	4.173	0.041	0.082	0.123
R5110x13xx	3.045	3.100	3.155	0.031	0.062	0.093
R5110x142x	4.518	4.600	4.682	0.046	0.092	0.138

OPERATION DESCRIPTION

Timing Chart

R5110Sxx1A / R5110Sxx1B Voltage Detector



R5110Sxx1A / R5110Sxx1B VD Timing Chart

(1) When the V_{OUT} pin voltage (V_{OUT}) becomes more than the release voltage ($+V_{DET}$), the RESETB pin voltage (V_{RESETB}) becomes "H" after the release output delay time (tdelay).

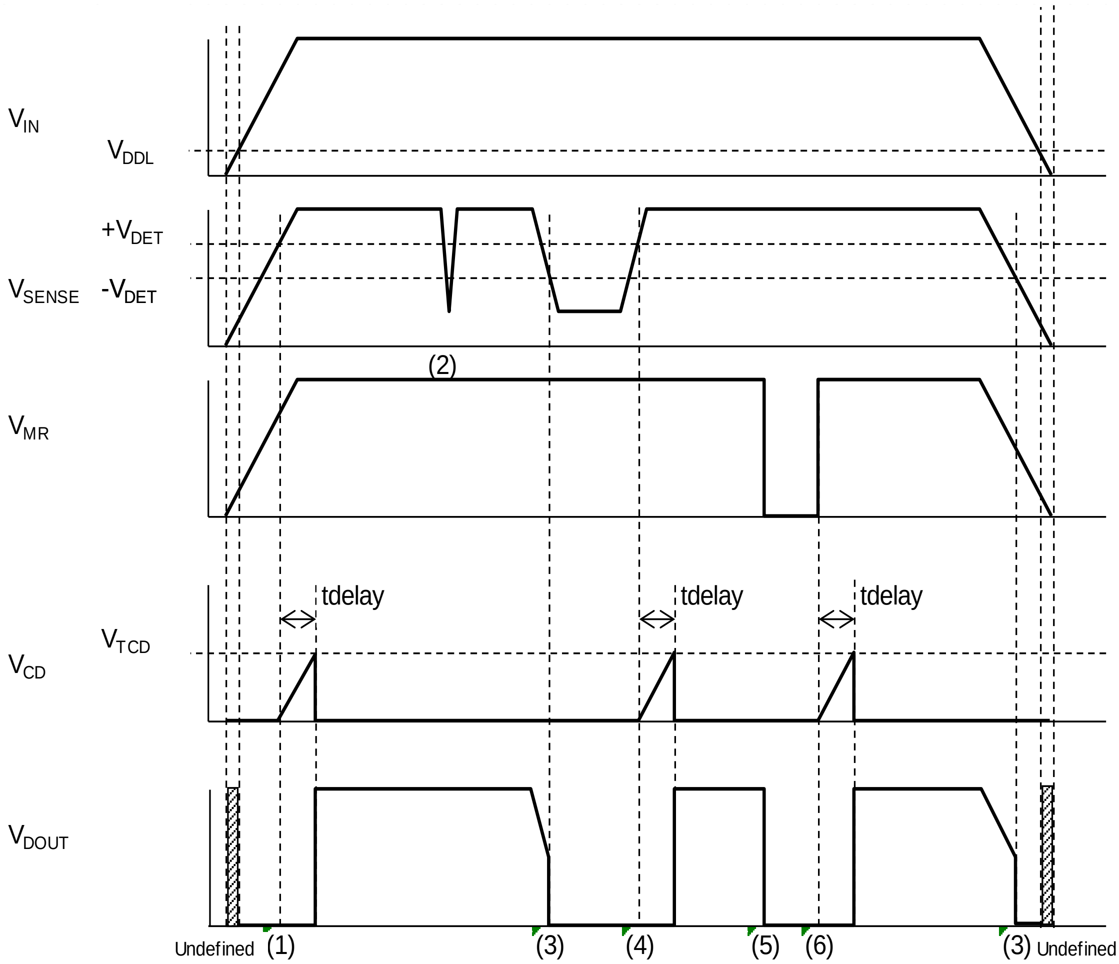
(2) When the detect output delay time is less than 30 µs (Typ.) even if V_{OUT} becomes lower than the detector threshold ($-V_{DET}$), the voltage detector (VD) does not go into the detecting state.

(3) When V_{OUT} becomes lower than $–V_{DET}$, V_{RESETB} becomes "L" after the detect output delay time (Typ.30 µs) and the VD goes into the detecting state.

(4) When V_{OUT} becomes more than $+V_{DET}$. V_{RESETB} becomes "H" after the release output delay time. (V_{TCD} = Typ.1 V)

RICOH

R5110xxx2C / R5110xxx2D Voltage Detector



R5110xxx2C / R5110xxx2D VD Timing Chart

(1) When the SENSE pin voltage (V_{SENSE}) becomes more than the release voltage ($+V_{DET}$), the D_{OUT} pin voltage (V_{DOUT}) becomes "H" after the release output delay time (tdelay).

(2) When the detect output delay time is 30 µs (Typ.) or less even if V_{SENSE} becomes lower than the detector threshold ($-V_{DET}$), the voltage detector (VD) does not go into the detecting state.

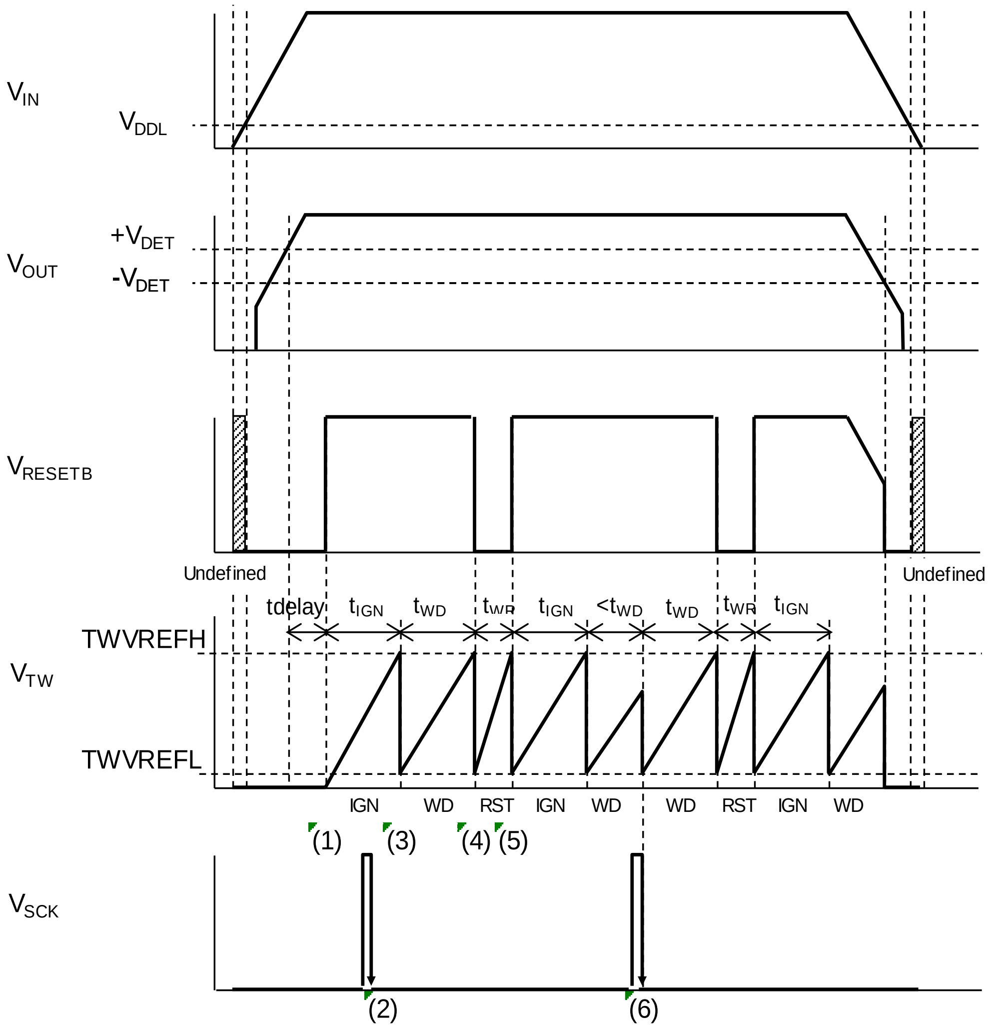
(3) When V_{SENSE} becomes lower than $-V_{DET}$, V_{DOUT} becomes "L" after the detect output delay time (Typ. 30 µs) and the VD goes into the detecting state.

(4) When V_{SENSE} becomes more than $+V_{DET}$, V_{DOUT} becomes "H" after the release output delay time. (V_{TCD} = Typ.1 V)

(5) When the MR pin voltage (V_{MR}) becomes "L", V_{DOUT} is fixed to "L".

(6) When V_{MR} becomes "L" to "H", V_{DOUT} becomes "H" after the release output delay time.

R5110Sxx1A Watchdog Timer (Normal Type)



R5110Sxx1A WDT Timing Chart

(1) When the V_{OUT} pin voltage (V_{OUT}) becomes more than the release voltage ($+V_{DET}$), the RESETB pin voltage (V_{RESETB}) becomes "H" after the release output delay time (tdelay) and the watchdog timer (WDT) starts monitoring a pulse. After that, the TW pin voltage (V_{TW}) repeats charge and discharge. As a result, a sawtooth wave is generated. The WDT has three states: Ignoring, Reset, and Monitoring. In each state, the TW pin is charged from 0 V or TWFREFL (Typ.0.08 V).

(2) After the WDT starts, the WDT is in an ignoring state until V_{TW} is charged up to TWVREFH (Typ.2 V). So, a pulse to the SCK pin is ignored during the ignoring state.

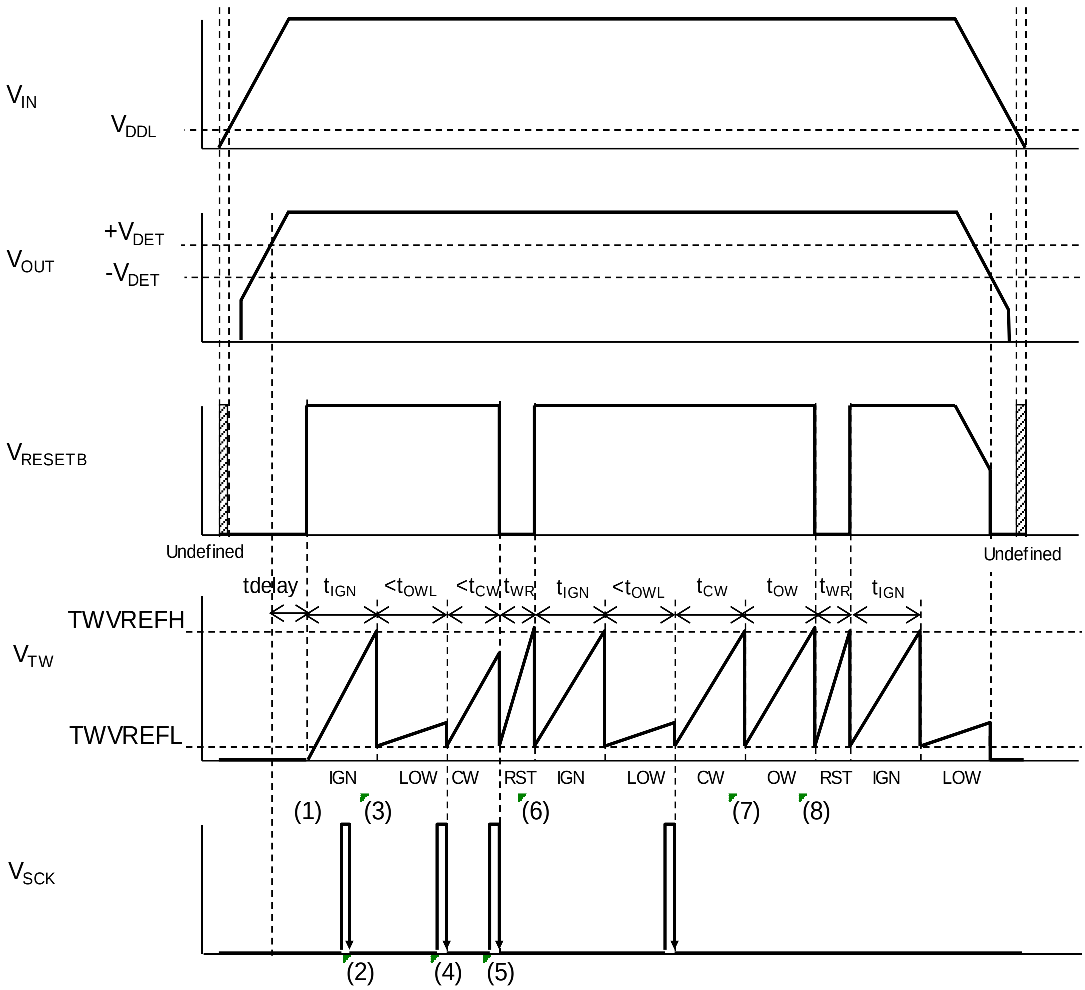
(3) When charging V_{TW} up to TWVREFH has completed, the TW pin starts discharging and the WDT goes into a monitoring state.

(4) When a pulse is not sent to the SCK pin before V_{TW} reaches TWVREFH during the monitoring state, the TW pin starts discharging and the WDT goes into a reset state. During the reset state, V_{RESETB} becomes "L.

(5) When V_{TW} is charged up to TWVREFH during the reset state, the TW pin starts discharging and the WDT goes into the ignoring state.

(6) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREFH during the monitoring state, the TW pin start discharging and the WDT goes into the next open window state.

R5110Sxx1B Watchdog Timer (Window Type)



R5110Sxx1B WDT Timing Chart

(1) When the V_{OUT} pin voltage (V_{OUT}) becomes more than the release voltage ($+V_{DET}$), the RESETB pin voltage (V_{RESETB}) becomes "H" after the release output delay time (tdelaly) and the watchdog timer (WDT) starts monitoring a pulse. After that, the TW pin voltage (V_{TW}) repeats charge and discharge. As a result, a sawtooth wave is generated. The WDT has four states: Ignoring, Reset, Open Window, and Closed Window. In each state, the TW pin is charged from 0 V or TWVREFL (Typ.0.08 V).

(2) After WDT starts, the WDT is in an ignoring state until V_{TW} is charged up to TWVREFH (Typ.2 V). So, a pulse to the SCK pin is ignored during the ignoring state.

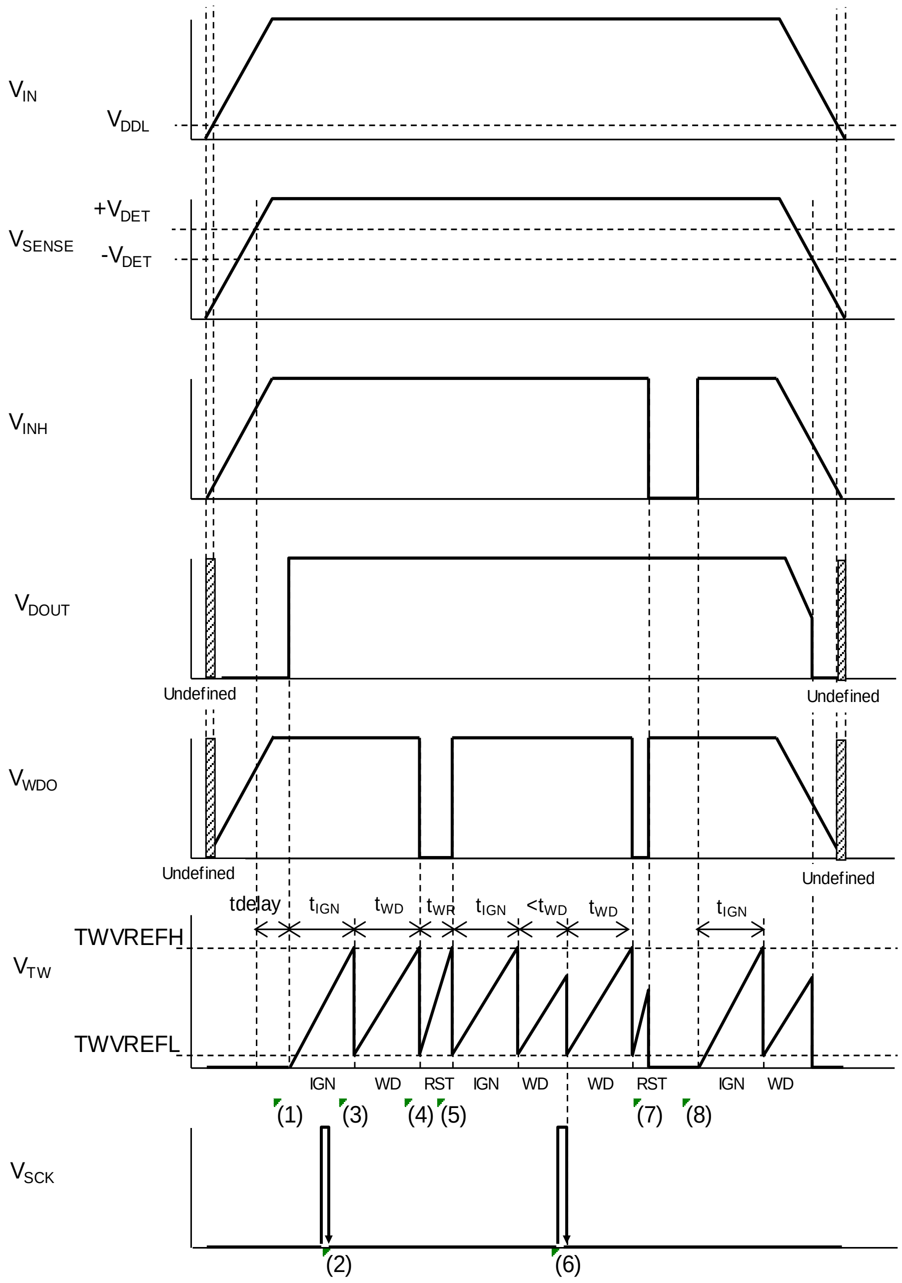
(3) When V_{TW} is charged up to TWVREFH during the ignoring state, the TW pin starts discharging and the WDT goes into an open window state. This open window state is four times longer than the normal open window state.

(4) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREFH during the open window state, the TW pin starts discharging and the WDT goes into a closed window state.

(5) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREF during the closed window state, the TW pin starts discharging and the WDT goes into a reset state. During the reset state, V_{RESETB} becomes "L".

(6) When V_{TW} reaches TWVREFH during the reset state, the TW pin starts discharging and the WDT goes into the ignoring state.
(7) When a pulse is not sent to the SCK pin before V_{TW} reaches TWVREFH during the closed window state, the TW pin starts discharging and the WDT goes into the open window state.
(8) When a pulse is not sent to the SCK pin before V_{TW} reaches TWVREFH during the open window state, the TW pin starts discharging and the WDT goes into the reset state.

R5110xxx2C Watchdog Timer (Normal Type)



R5110xxx2C WDT Timing Chart

(1) When the SENSE pin voltage (V_{SENSE}) becomes more than the release voltage ($+V_{DET}$), the D_{OUT} pin voltage (V_{DOUT}) becomes "H" after the release output delay time (tdelay) and the watchdog timer (WDT) starts monitoring a pulse. After that, the TW pin voltage (V_{TW}) repeats charge and discharge. As a result, a sawtooth wave is generated. The WDT has three states: Ignoring, Reset, and Monitoring. In each state, the TW pin is charged from 0 V or TWVREFL (Typ.0.08 V).

(2) After the WDT starts, the WDT is in an ignoring state until V_{TW} is charged up to TWVREFH. So, a pulse to the SCK pin is ignored during the ignoring state.

(3) When V_{TW} is charged up to TWVREFH during the ignoring state, the TW pin starts discharging and the WDT goes into a monitoring state.

(4) When a pulse is not sent to the SCK pin before V_{TW} reaches TWVREFH during the monitoring state, the TW pin starts discharging and the WDT goes into a reset state. During the reset state, the WDO pin voltage (V_{WDO}) becomes "L".

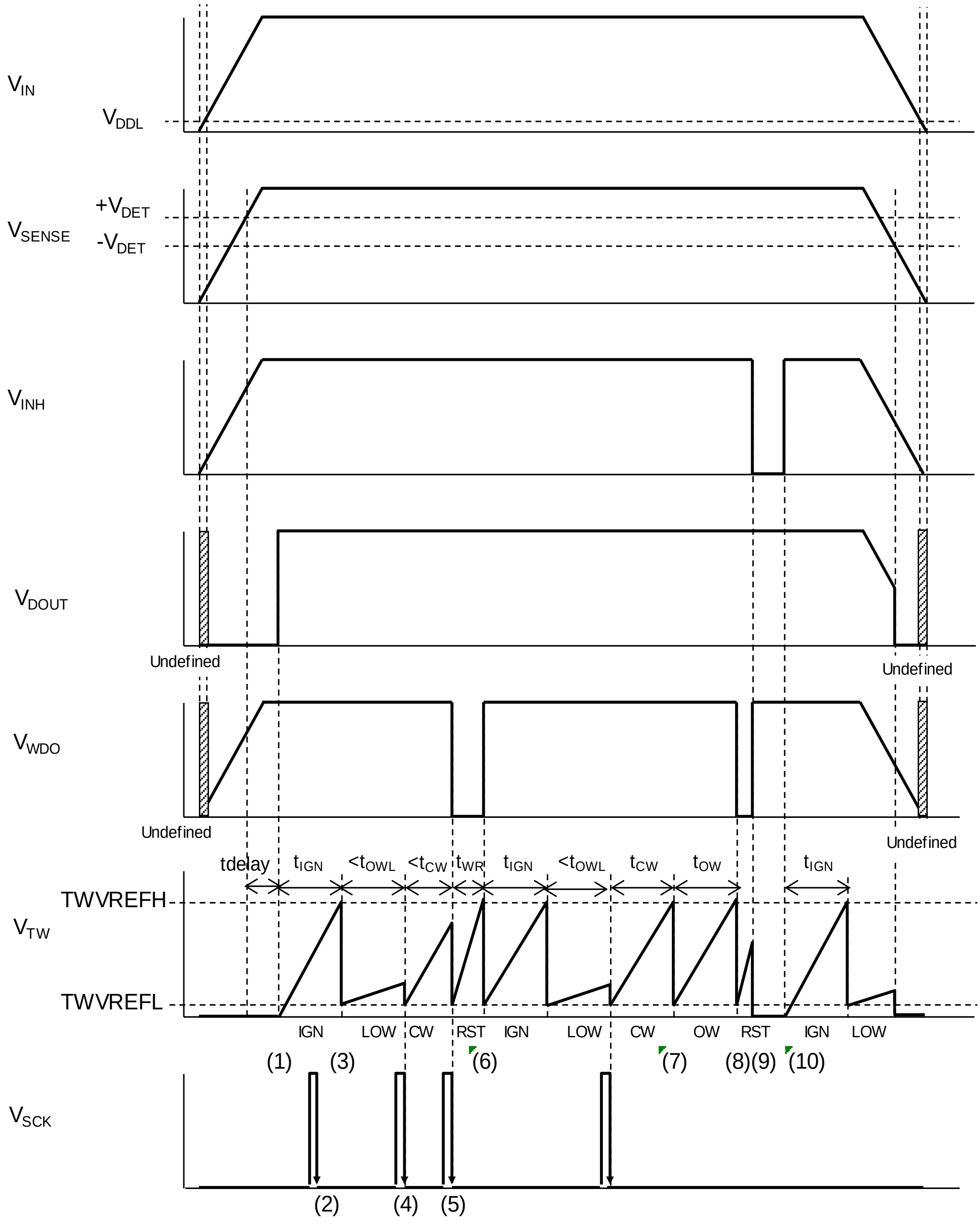
(5) When V_{TW} reaches TWVREFH during the reset state, the TW pin starts discharging and the WDT goes into an ignoring state.

(6) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREFH during the monitoring, the TW pin starts discharging and the WDT goes into the next monitoring state.

(7) The WDT stops monitoring by setting the INH pin voltage (V_{INH}) to "L". Then, V_{WDO} is fixed to "H" and V_{TW} is fixed to "L".

(8) When changed V_{INH} from "L" to "H", the WDT goes into the ignoring state and restarts monitoring.

R5110xxx2D Watchdog Timer (Window Type)



R5110xxx2D WDT Timing Chart

(1) When the SENSE pin voltage (V_{SENSE}) becomes more than the release voltage ($+V_{DET}$), the D_{OUT} pin voltage (V_{DOUT}) becomes “H” after the release output delay time (tdelay) and the watchdog timer (WDT) starts monitoring a pulse. After that, the TW pin voltage (V_{TW}) repeats charge and discharge. As a result, a sawtooth wave is generated. The WDT has four states: Ignoring, Reset, Open Window, and Closed Window. In each state, the TW pin is charged from 0 V or TWVREFL (Typ.0.08 V).

(2) After WDT starts, the WDT is in an ignoring state until V_{TW} is charged up to TWVREFH. So, a pulse to the SCK pin is ignored during the ignoring state.

(3) When V_{TW} is charged up to TWVREFH during the ignoring state, the TW pin starts discharging and the WDT goes into an open window state. This open window state is four times longer than the normal open window state.

(4) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREFH during the open window state, the TW pin starts discharging and the WDT goes into a closed window state.

(5) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREFH during the close window state, the TW pin starts discharging and the WDT goes into a reset state. During the reset state, V_{DOUT} becomes “L”.

(6) When V_{TW} reaches TWVREFH during the reset state, the TW pin starts discharging and the WDT goes into an ignoring state.

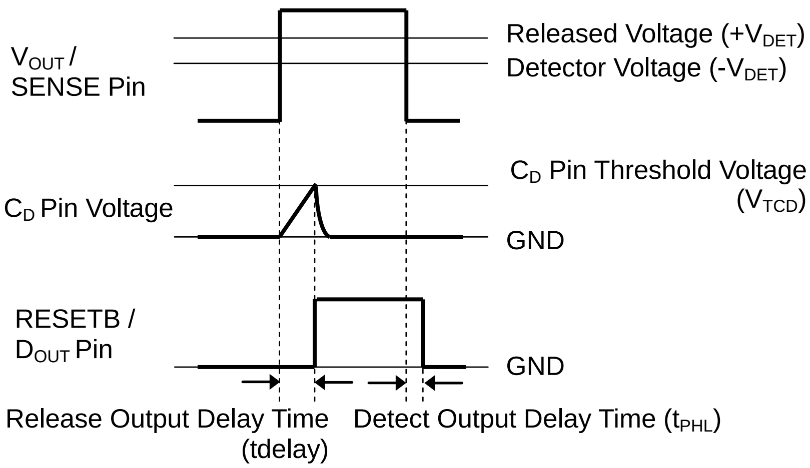
(7) When a pulse is not sent to the SCK pin before V_{TW} reaches TWVREFH during a closed window state, the TW pin starts discharging and the WDT goes into an open window state.

(8) When a pulse is not sent to the SCK pin before V_{TW} reaches TWVREFH during the open window state, the TW pin starts discharging and the WDT goes into a reset state.

(9) The WDT stops monitoring by setting the INH pin voltage (V_{INH}) to “L”. Then, V_{WDO} is fixed to “H” and V_{TW} is fixed to “L”.

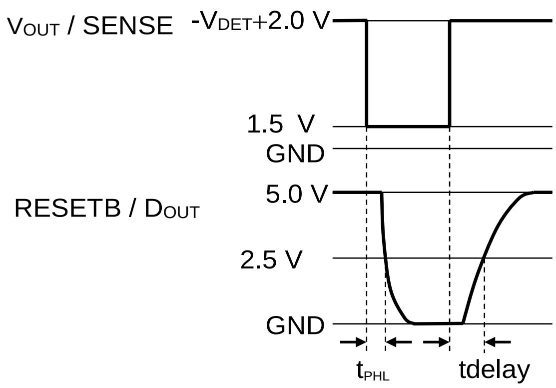
(10) When changed V_{INH} from “L” to “H”. the WDT goes into the ignoring state and restarts monitoring.

Delay Operation and Released Output Delay Time (tdelay)



Released Output Delay Timing Diagram

When the operating voltage higher than the released voltage is applied to VOUT pin (R5110Sxx1A/R5110Sxx1B) or SENSE pin (R5110xxx2C/R5110xxx2D), charge to an external capacitor starts, then CD pin voltage (VCD) increases. RESETB pin (R5110Sxx1A/R5110Sxx1B) or DOUT pin (R5110xxx2C/R5110xxx2D) maintains the released output until VCD reaches the threshold voltage of the release output delay pin (VTCD). And when VCD is over VTCD, RESETB pin or DOUT pin is inverted from “L” to “H”. That is, the charged external capacitor starts discharging.
When the operating voltage lower than the detector threshold is applied to VDD pin, the detect output delay time, which is the time until the output voltage is inverted from “H” to “L”, remains constant independent of the external capacitor.

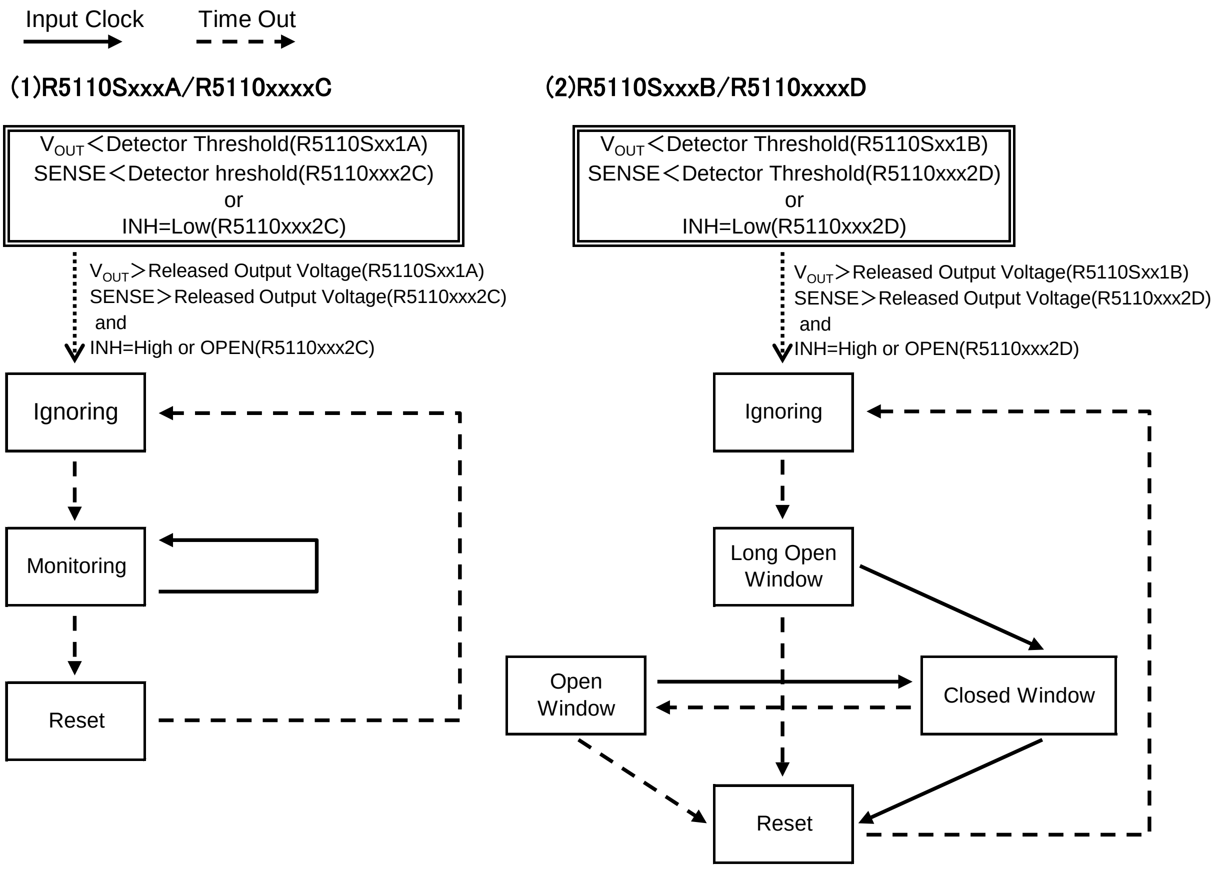


Released Output Delay Time

Released Output Delay Time (tdelay) indicates the time between the instance when V_{OUT} pin (R5110Sxx1A / R5110Sxx1B) or SENSE pin (R5110xxx2C / R5110xxx2D) shifts from “1.5 V” to “$-V_{DET}$ + 2.0 V” by the application of a pulse voltage and the instance when the output voltage reaches 2.5 V after pulled up RESETB pin (R5110Sxx1A / R5110Sxx1B) or D_{OUT} pin (R5110xxx2C/ R5110xxx2D) to 5.0 V with a resistor of 100 kΩ.
This is given by the expression tdelay (s) = 1.1 × C_D (F) / (1.0×10^{-6}), where C_D (F) represents capacitance of

the external capacitor.
If V_{OUT} / SENSE pin goes up at a mild pace of 0.1V/s or less, connect a capacitor of 100 pF or more to C_D pin.

WDT State Transition Diagram



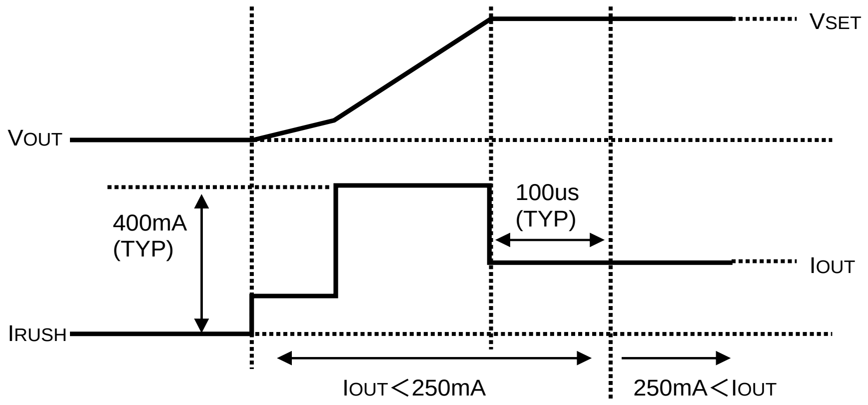
Time Setting for Watchdog Timer

The following time of WDT is dependent on a capacitor connecting to the TW pin. Relationship between the value of capacitor and time can be expressed by the following equations.

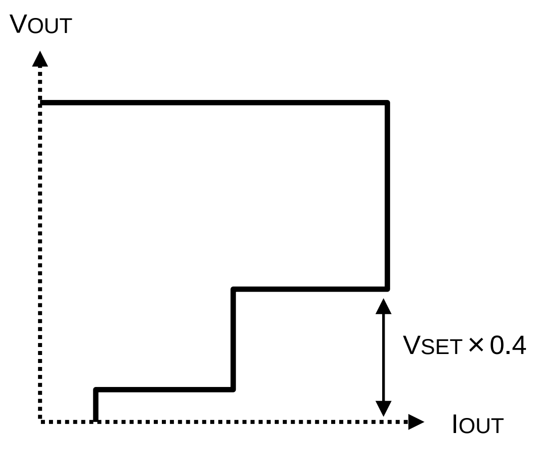
T_{OW} (s) = 1.8 x C(F) / (1.0 x 10^{-6})
t_{CW} (s) = 1.8 x C(F) / (1.0 x 10^{-6})
t_{OWL} (s) = 1.8 x C(F) / (0.25 x 10^{-6})
t_{IGN} (s) = 1.8 x C(F) / (1.0 x 10^{-6})
t_{WD} (s) = 1.8 x C(F) / (1.0 x 10^{-6})
t_{WR} (s) = 1.9 x C(F) / (2.0 x 10^{-6})

Inrush Current Prevention at Rising Characteristics

R5110x has the inrush current preventing circuit to control the inrush current within about 400mA limited. This circuit works during the rising periods. Therefore, the load current must be increased after rising up the output voltage (at typ.100 µs after being out of the inrush current limited condition) by the sequence control. When the load current is increased during the rising periods, the inrush current must be controlled within 250 mA.



Likewise, on the thermal shutdown and the foldback characteristic, the inrush current preventing circuit works when the output voltage re-rises after the output voltage fall down to a guideline (V_{SET} x 0.4) or less.



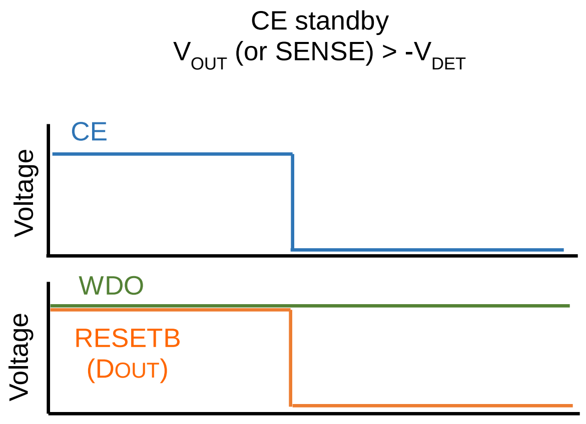
Standby Function

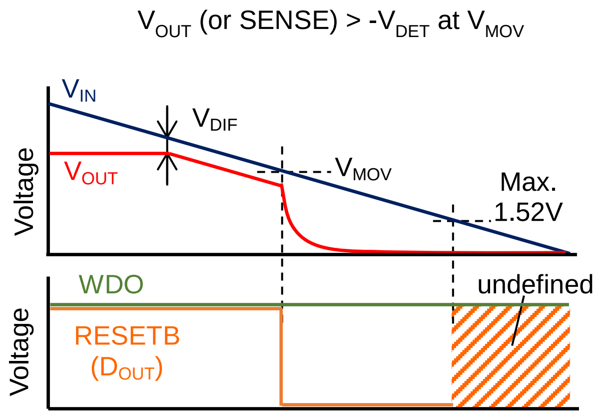
When CE turns to low, the R5110x goes into the standby mode. During this mode, the voltage regulator (VR) stops the output, the watchdog timer (WDT) stops the pulse monitoring, and the voltage detector (VD) stops the voltage monitoring.
Even if V_{IN} < 3.5 V (Minimum Operating Voltage V_{MOV}), VR stops the output, WDT stops the pulse monitoring, and VD stops the voltage monitoring. When CE = low or V_{IN} < 3.5 V (Minimum Operating Voltage), the output of WDT and VD become as follows regardless of SENSE voltage.

R5110Sxx1A/ R5110Sxx1B: The RESETB output is fixed to "L".

R5110xxx2C/ R5110xxx2D: The D_{OUT} is fixed to "L", and WDO output is fixed to the pull-up voltage.

When V_{IN} is under 1.52 V, values of RESETB output (R5110Sxx1A/ R5110Sxx1B) and D_{OUT} output (R5110xxx2C/ R5110xxx2D) become indefinite, 0.1 V or more (pull-up voltage 5 V, pull-up resistance 100 kΩ).





Voltage Setting (R5110Sxx1A / R5110Sxx1B)

VD detects the drop of the VR output voltage (V_{OUT}). When the VD release voltage ($+V_{DET}$) is set to a voltage above the VR output voltage, the reset signal of VD is not released even if VD monitors the VR output voltage returns to the normal value after detecting the drop of VR. To prevent this issue, the following condition is required between V_{OUT} and $+V_{DET}$.

(VR Set Output Voltage) x 0.985 – 30 mV > (VD Set Detector Threshold) x 1.018 x 1.030

When using a device with the above conditions of V_{OUT} and $+V_{DET}$, careful consideration must be given to the system operation before use.

Manual Reset (MR) Function (R5110xxx2C, R5110xxx2D)

Setting the MR pin to "L" forcefully sets D_{OUT} to "L". The maximum value of the delay time (t_{MR}), which is until D_{OUT} outputs "L", is 1µs as an index of the performance. The MR pin is pulled-up by an internal resistor (Typ.110kΩ). Current is passed to the MR pin when the voltage of MR > V_{DD}. But, this current has no effect to the operation because the current is limited with a pull-up resistor.
When setting the MR pin from "L" to "H", D_{OUT} is changed from "L" to "H" after the released output delay time and the WDT starts from the ignoring state.
When the MR pin is "L", the WDO pin outputs "H".

SENSE Function (R5110xxx2C, R5110xxx2D)

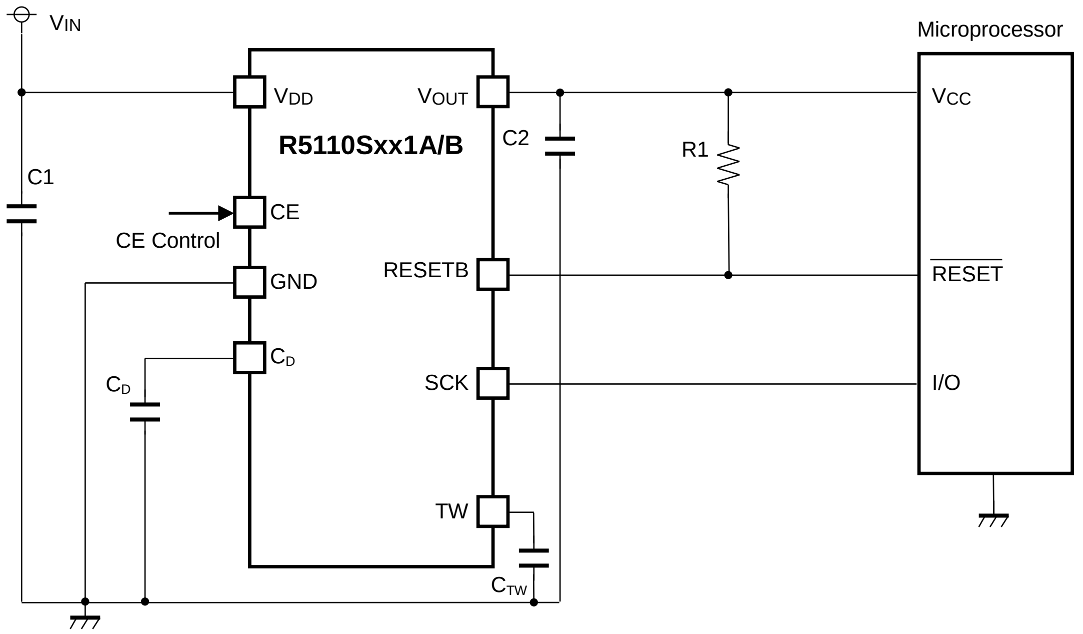
The internal voltage detector monitors the input voltage to the SENSE pin. To measure the proper detector threshold, setting of $V_{IN} \geq 3.5$ V is required.

Inhibition (INH) Function (R5110xxx2C, R5110xxx2D)

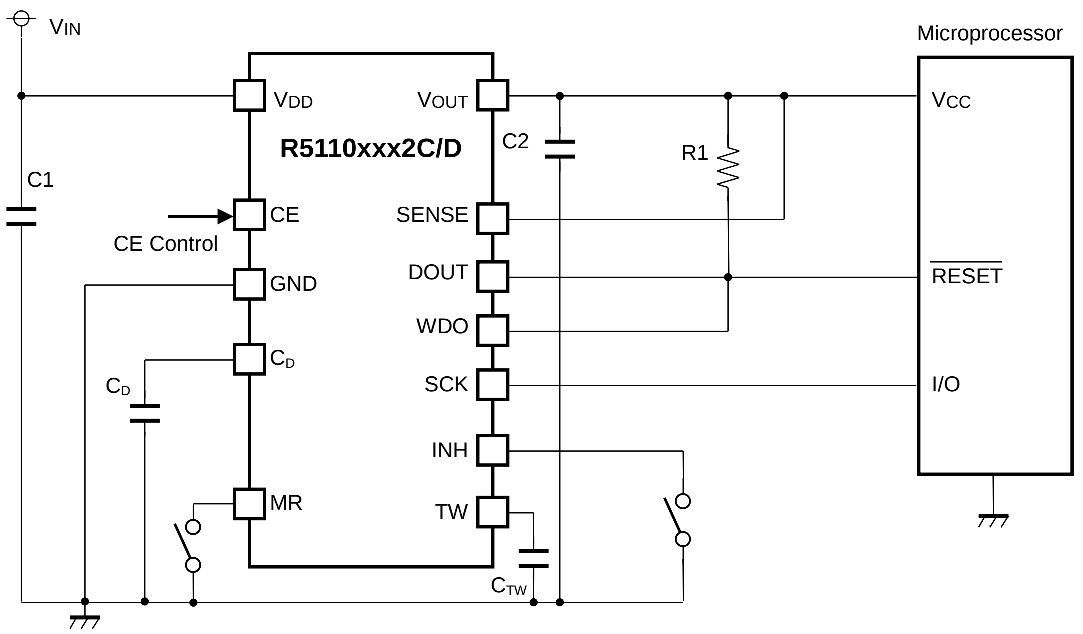
Setting the INH pin to "L" stops the WDT pulse monitoring function and the WDO pin is fixed to "H". The INH pin is pulled up with an internal resistor (Typ.110 kΩ).

APPLICATION INFORMATION

Typical Application Circuits



R5110Sxx1A/B Typical Application



R5110xxx2C/D Typical Application

External Components

Symbol	Description
C1 (C_{IN})	0.1 µF, Ceramic Capacitor
C2 (C_{OUT})	0.1 µF, Ceramic Capacitor
C_{TW}	A capacitor corresponding to time setting for Watchdog Timer is required. Refer to "*Time Setting for WDT*" in Operation Description for details.
C_D	A capacitor corresponding to setting for Release Output Delay Time is required. Refer to "*Delay Operation and Release Output Delay Time (tdelay)*" in Operation Description for details.
R1	A resistor is required to set with consideration of the output current and the leakage current. Refer to "*Electrical Characteristic*" for details.

TECHNICAL NOTES

Phase Compensation

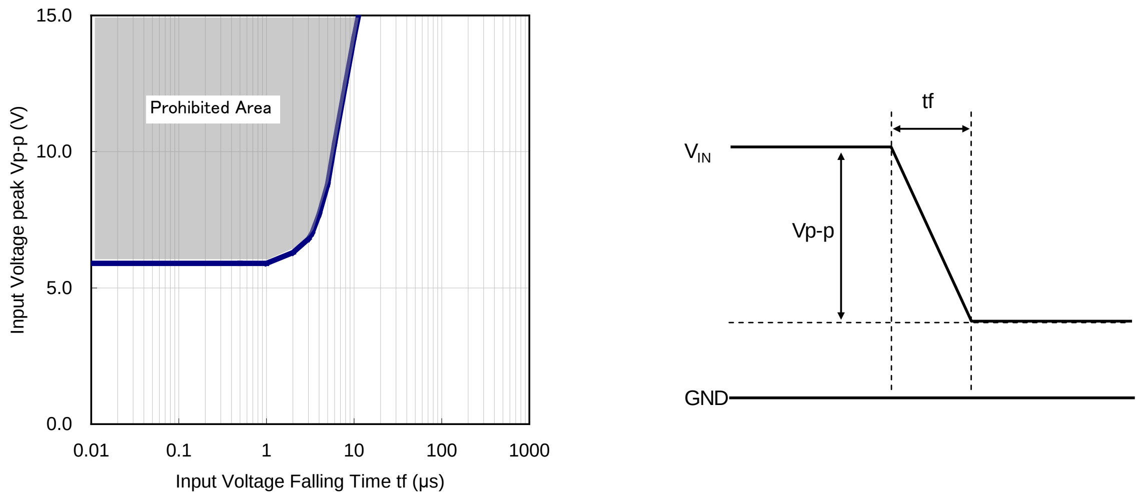
In the Ics, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a capacitor C2 with 0.1 µF or more.
If a tantalum capacitor is used, and its ESR (Equivalent Series Resistance) of C2 is large, the loop oscillation may result. Because of this, select C2 carefully considering its frequency characteristics.

PCB Layout

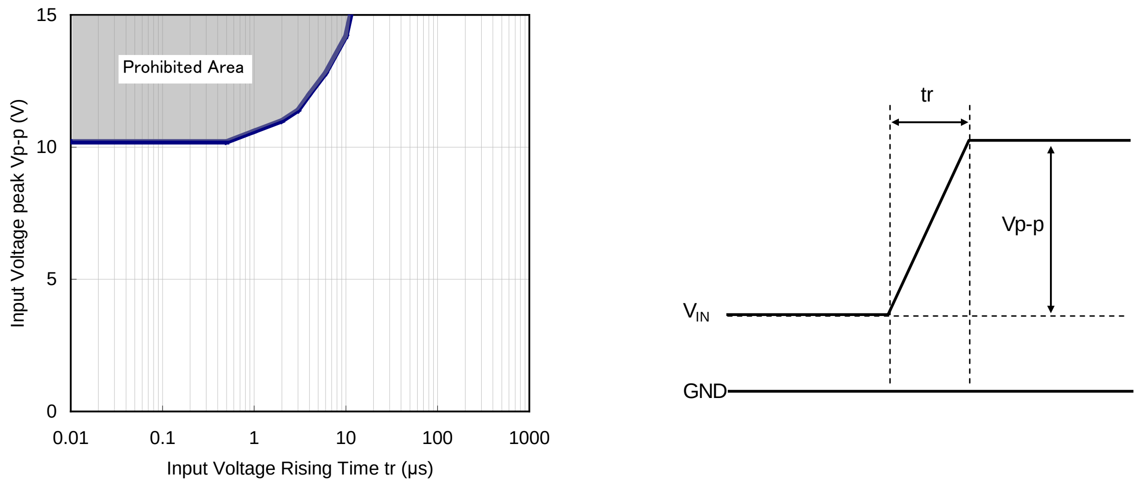
Make V_{DD} and GND lines sufficient. If their impedance is too high, noise pickup or unstable operation may result. Connect 0.1 µF or more of the capacitor C1 between the V_{DD} and GND, and as close as possible to the pins.
In addition, connect the capacitor C2 between V_{OUT} and GND, and as close as possible to the pins.

Prohibited Area for Fluctuations in Input Voltage

Please take note that miss-detection or miss-release might be invited when changing an input voltage abruptly in the following prohibited area.

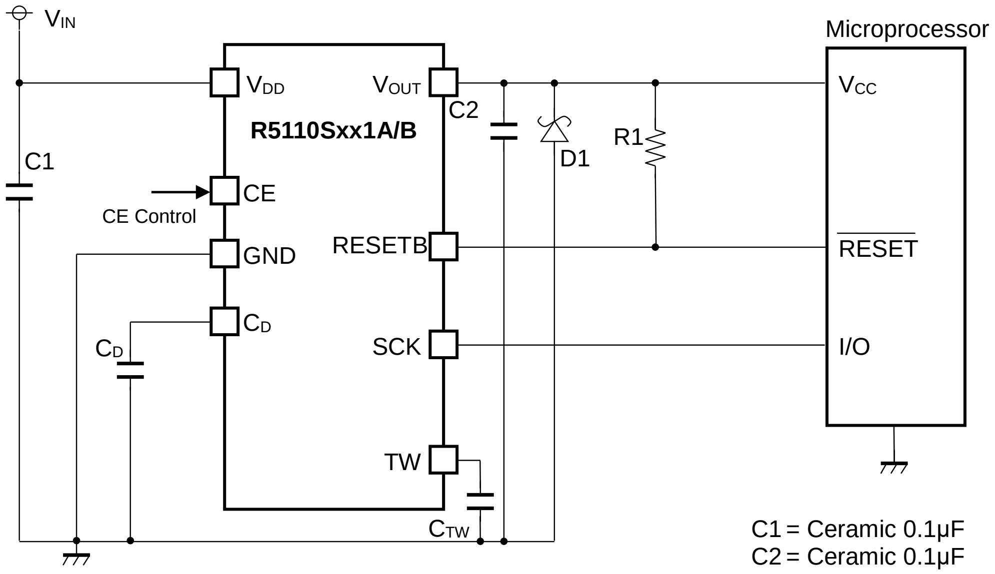


Prohibited Area of Fluctuation at Falling of V_{IN}



Prohibited Area of Fluctuation at Rising of V_{IN}

Typical Application for IC Chip Breakdown Prevention



R5110Sxxxx Typical Application

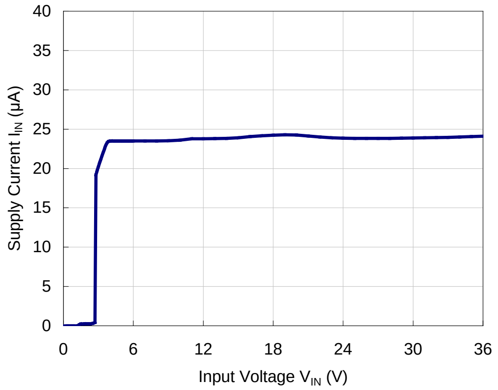
When a sudden surge of electrical current travels along the VOUT pin and GND due to a short-circuit, electrical resonance of a circuit involving an output capacitor (C2) and a short circuit inductor generates a negative voltage and may damage the device or the load devices. Connecting a schottky diode (D1) between the VOUT pin and GND has the effect of preventing damage to them.

TYPICAL CHARACTERISTICS

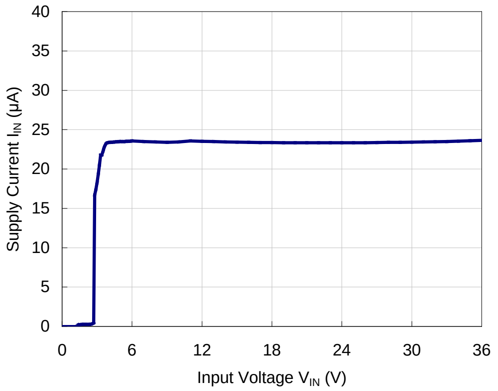
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Power Consumption vs. Input Voltage (Ta = 25°C)

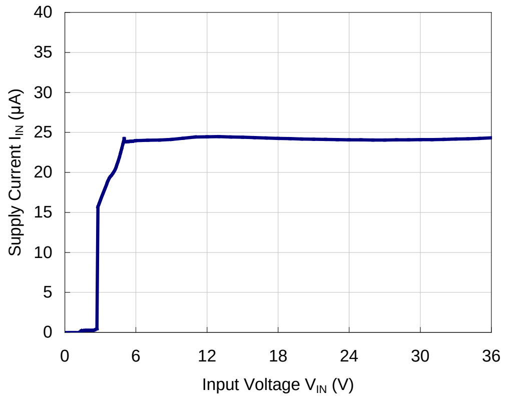
VR=1.8V



VR=3.3V

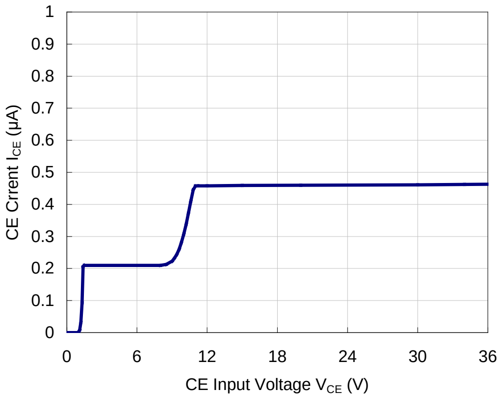


VR=5.0V



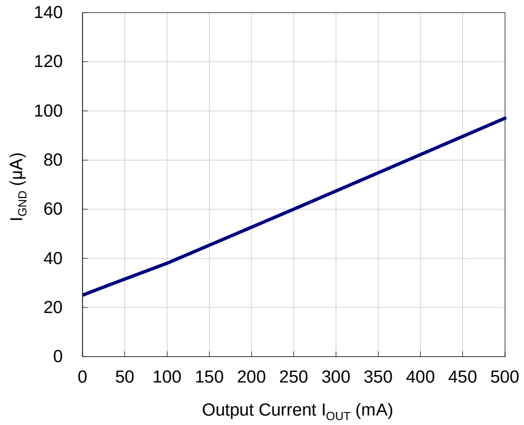
2) CE Pin Current vs. CE Pin Voltage (Ta = 25°C, V_{IN}=14V)

VR=5.0V



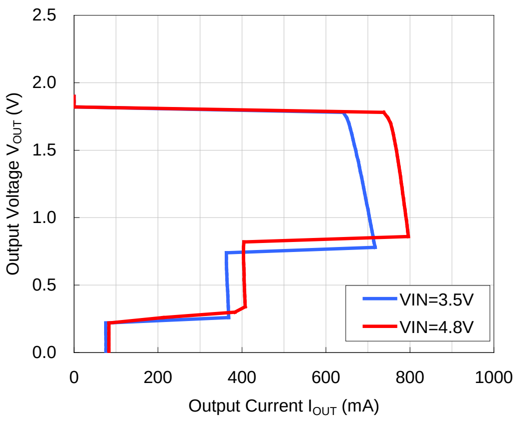
RICOH

3) GND Pin Current vs. Output Current (Ta = 25°C)

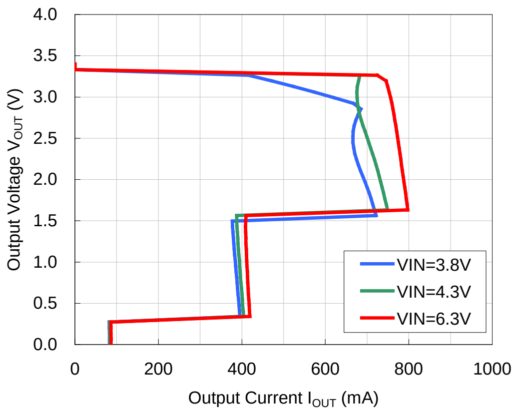


4) Output Voltage vs. Output Current (Ta = 25°C)

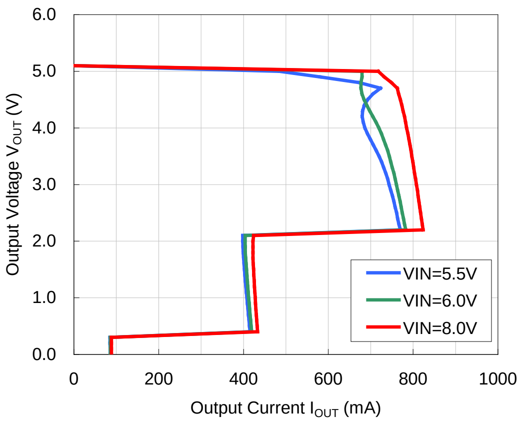
VR=1.8V



VR=3.3V

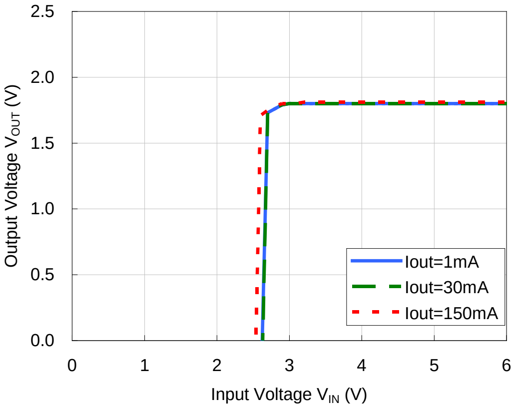


VR=5.0V

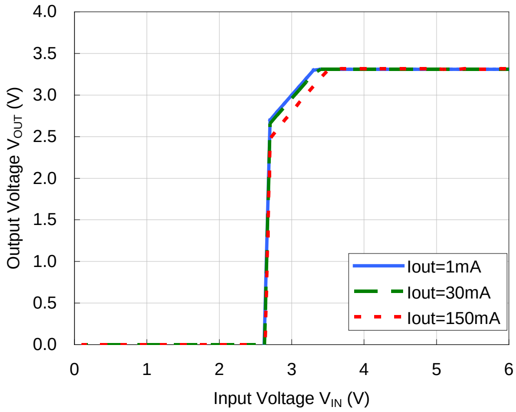


5) Output Voltage vs. Input Voltage (Ta = 25°C)

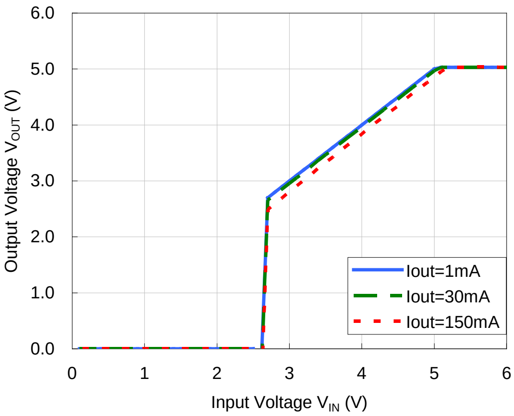
VR=1.8V



VR=3.3V

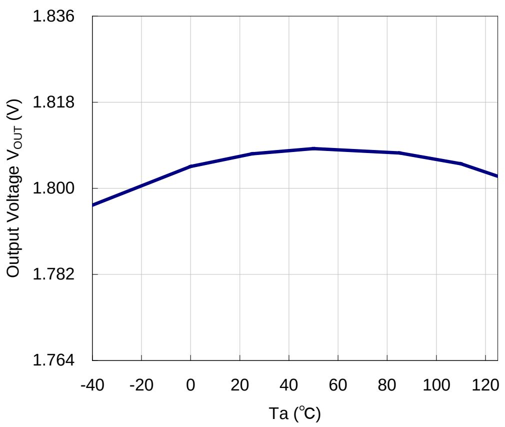


VR=5.0V

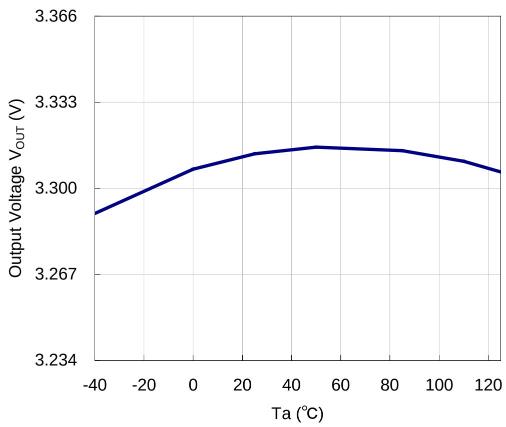


6) Output Voltage vs. Temperature (V_{IN}=14V, I_{OUT}=1mA)

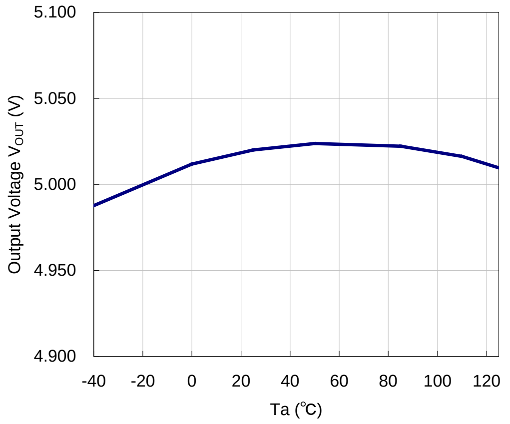
VR=1.8V



VR=3.3V

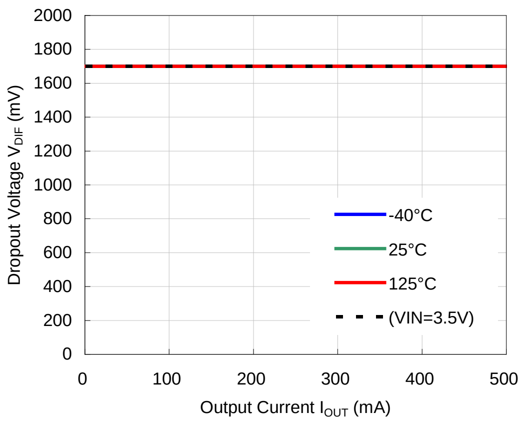


VR=5.0V

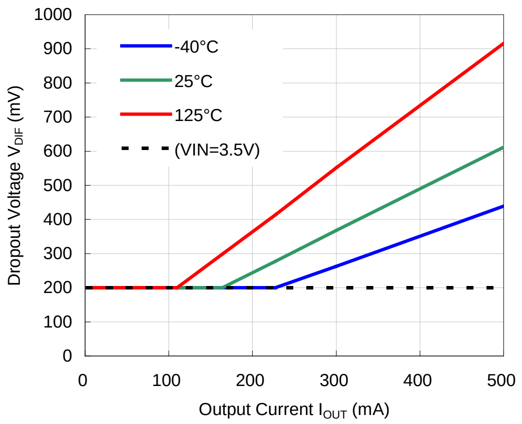


7) Dropout Voltage vs. Output Current

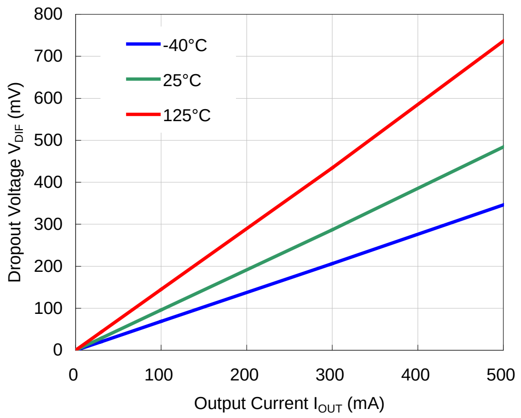
VR=1.8V



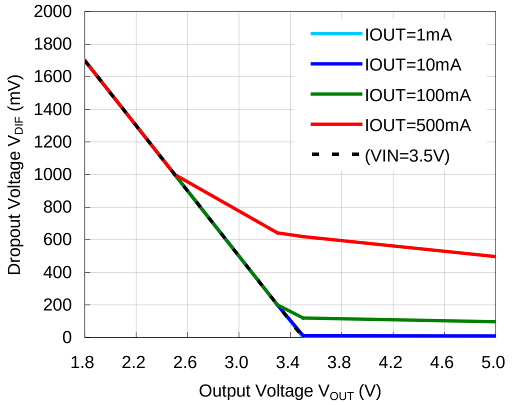
VR=3.3V



VR=5.0V

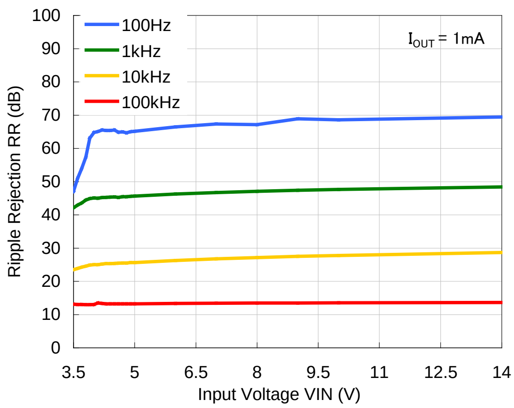


8) Dropout Voltage vs. Output Voltage (Ta=25°C)

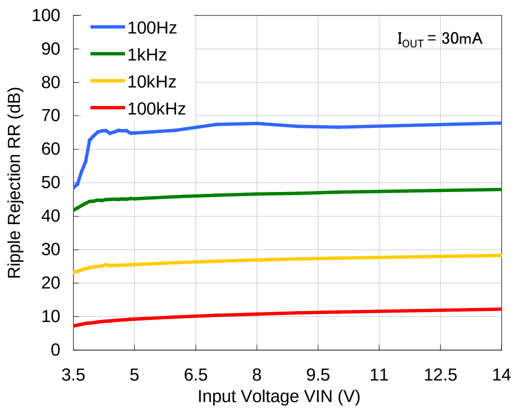


9) Ripple Rejection vs. Input Voltage (Ta=25°C, Ripple = 0.2 Vpp)

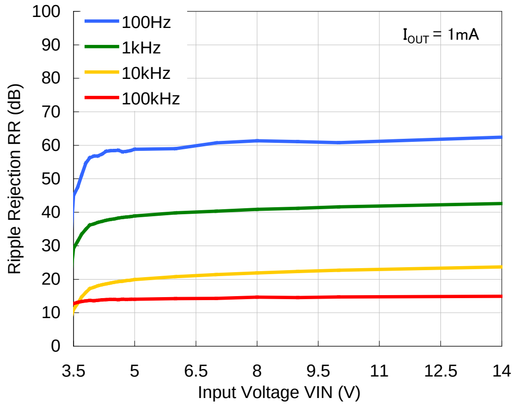
VR=1.8V, I_{OUT}=1mA



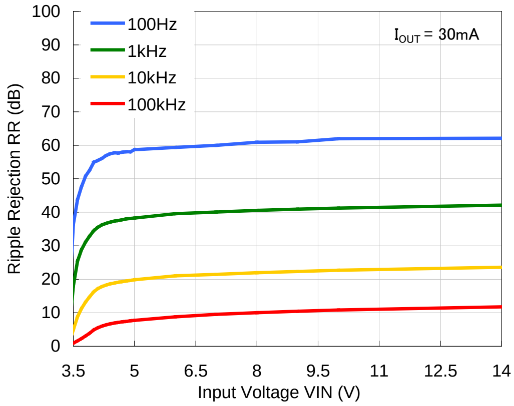
VR=1.8V, I_{OUT}=30mA



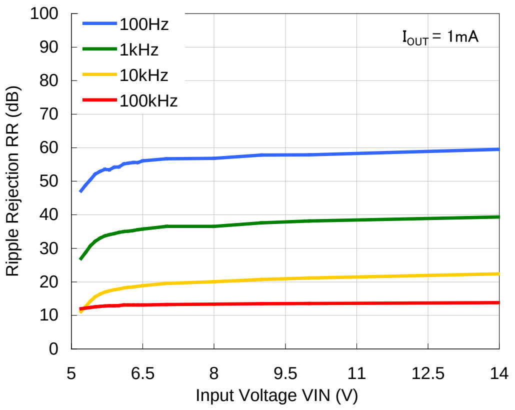
VR=3.3V, I_{OUT}=1mA



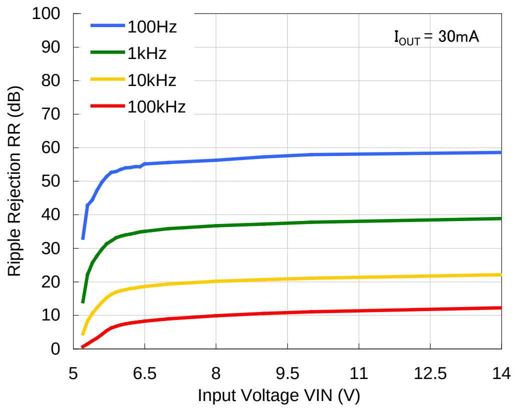
VR=3.3V, I_{OUT}=30mA



VR=5.0V, I_{OUT}=1mA

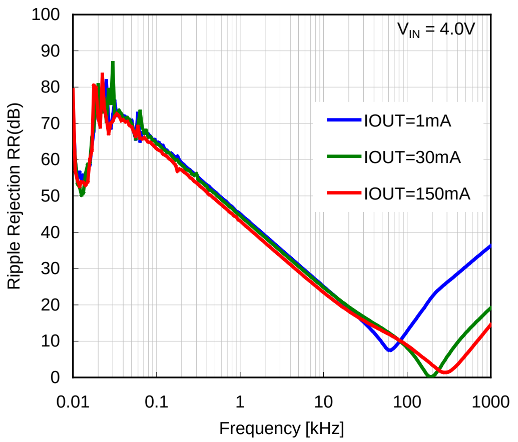


VR=5.0V, I_{OUT}=30mA

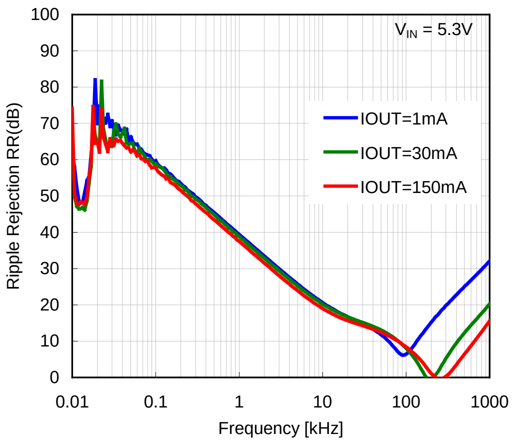


10) Ripple Rejection vs. Frequency (Ta=25℃, Ripple=0.2 Vpp)

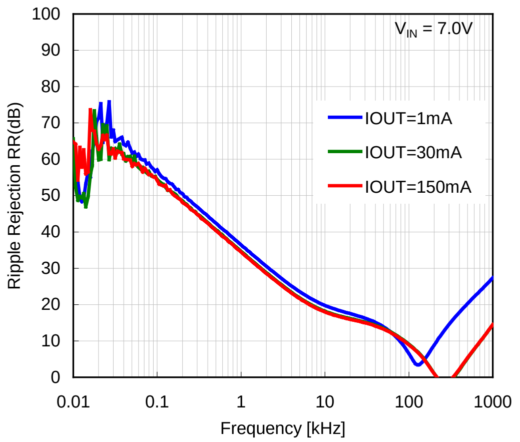
VR=1.8V



VR=3.3V



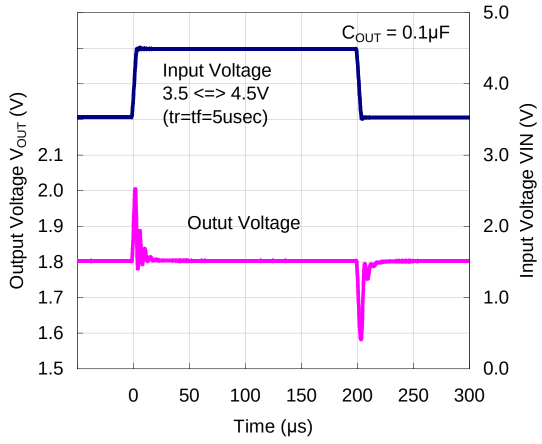
VR=5.0V



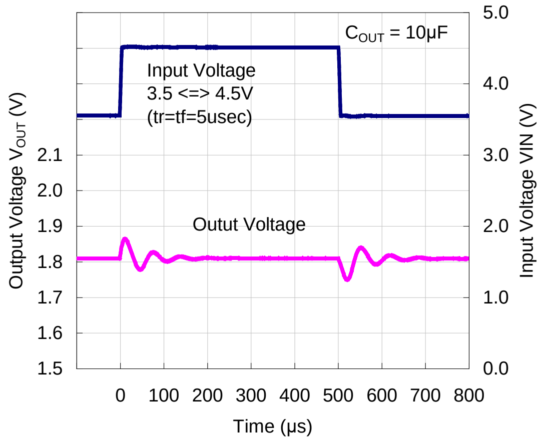
RICOH

11) Input Transient Respon (Ta=25°C)

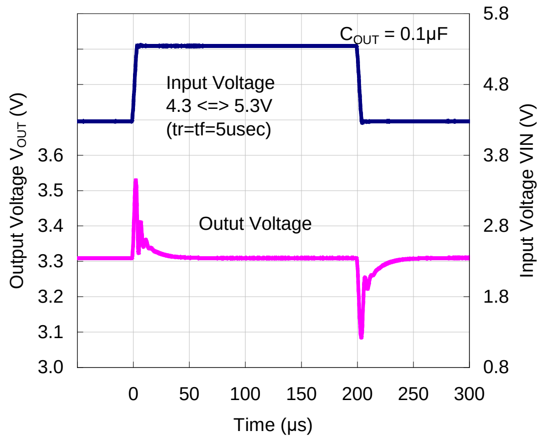
VR=1.8V, I_{OUT}=30mA, C_{OUT}=0.1μF



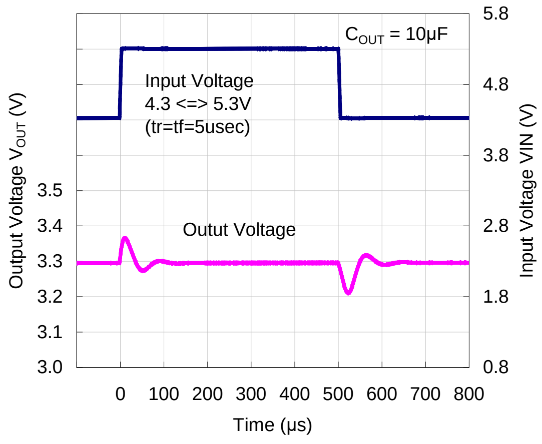
VR=1.8V, I_{OUT}=30mA, C_{OUT}=10μF



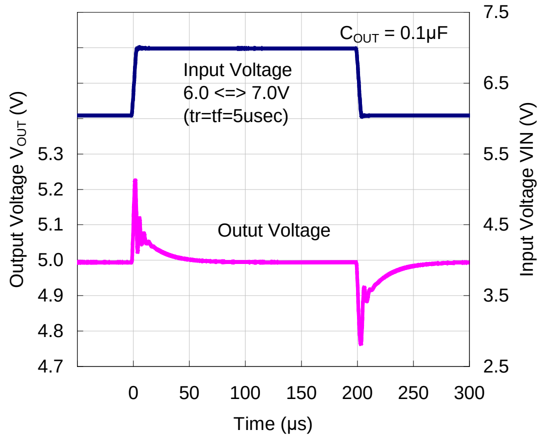
VR=3.3V, I_{OUT}=30mA, C_{OUT}=0.1μF



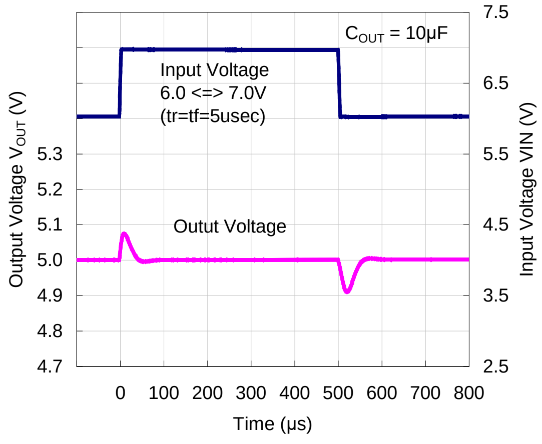
VR=3.3V, I_{OUT}=30mA, C_{OUT}=10μF



VR=5.0V, I_{OUT}=30mA, C_{OUT}=0.1μF

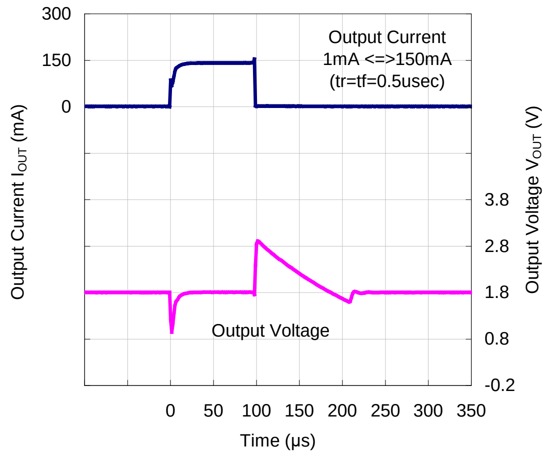


VR=5.0V, I_{OUT}=30mA, C_{OUT}=10μF

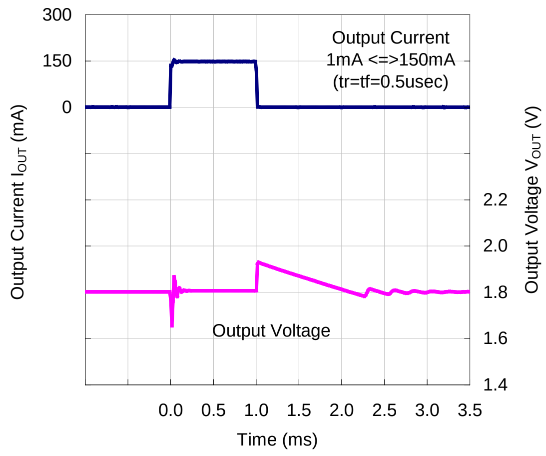


12) Load Transient Response (Ta=25°C)

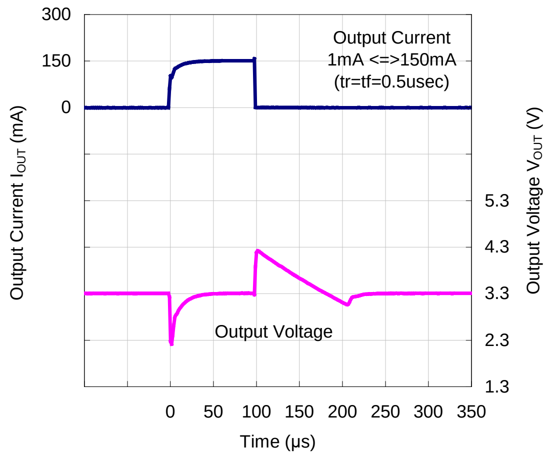
VR=1.8V, C_{OUT}=0.1µF



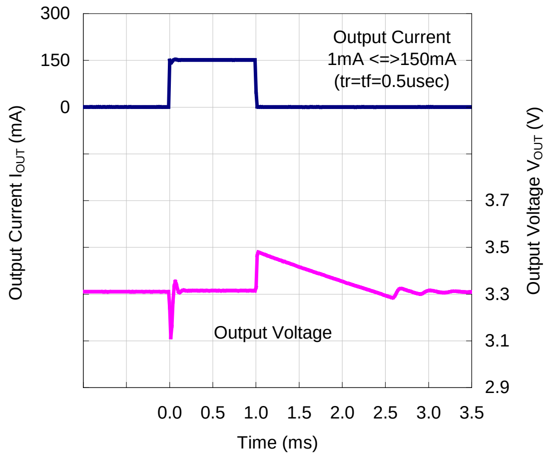
VR=1.8V, C_{OUT}=10µF



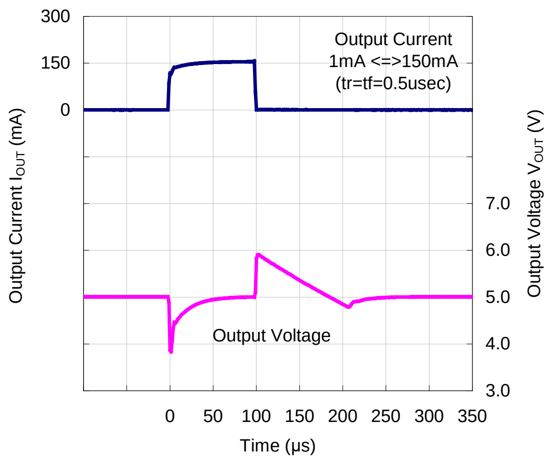
VR=3.3V, C_{OUT}=0.1µF



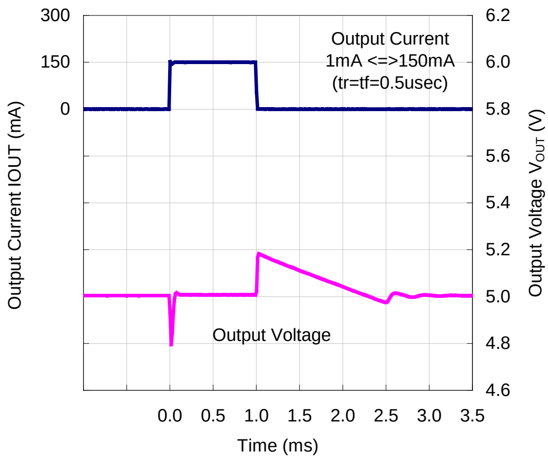
VR=3.3V, C_{OUT}=10µF



VR=5.0V, C_{OUT}=0.1µF

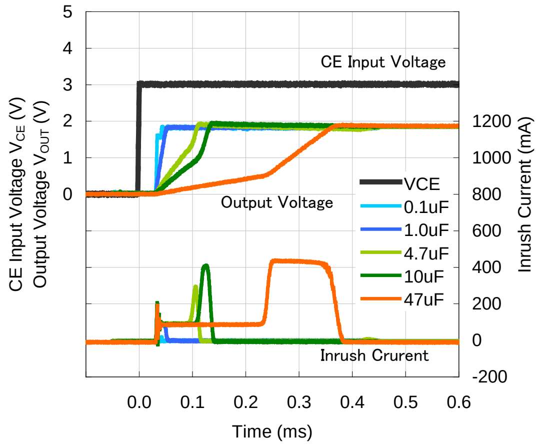


VR=5.0V, C_{OUT}=10µF

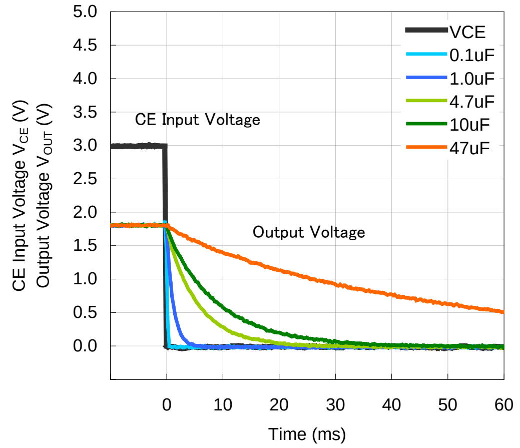


13) CE Transient Response (Ta=25℃, V_{IN}=14V, I_{OUT}=1mA, C_{OUT}=0.1μ∼47μF)

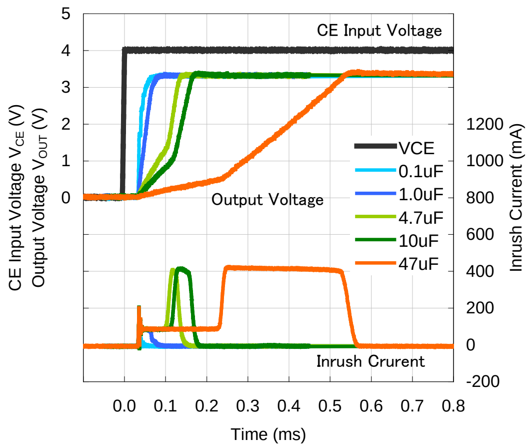
VR=1.8V, CE at rising



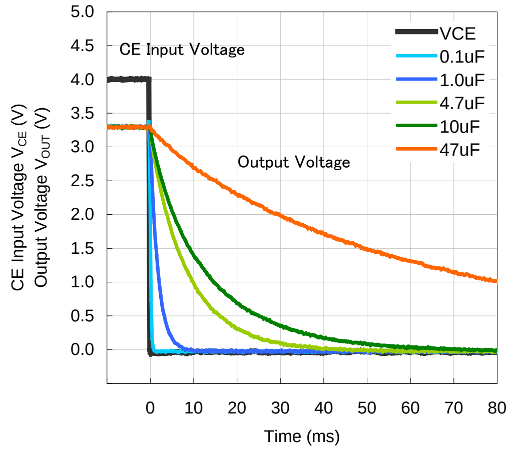
VR=1.8V, CE at falling



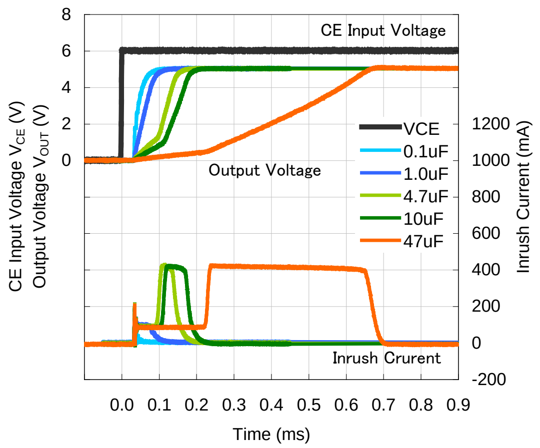
VR=3.3V, CE at rising



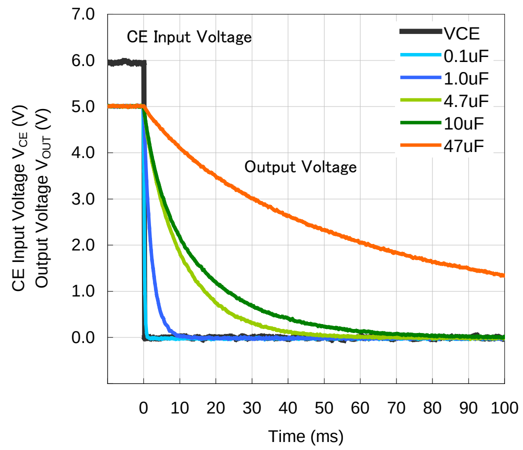
VR=3.3V, CE at falling



VR=5.0V, CE at rising

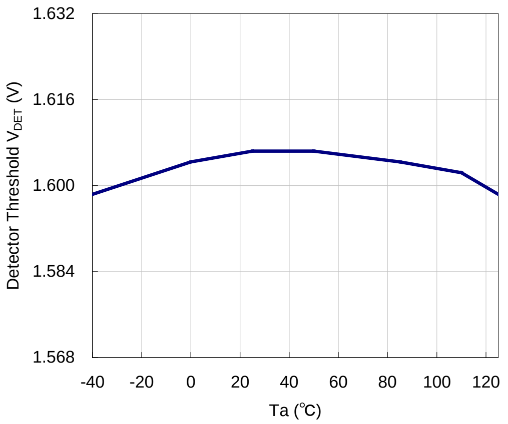


VR=5.0V, CE at falling

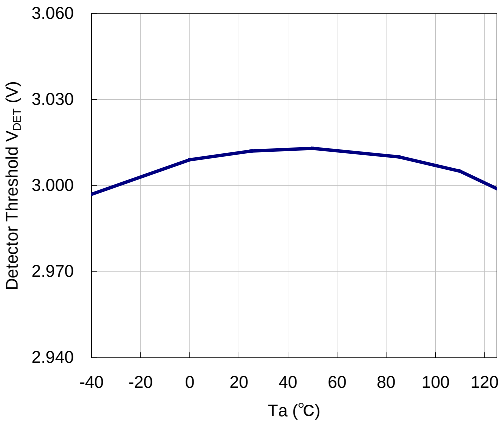


14) Detector Threshold vs. Temperature

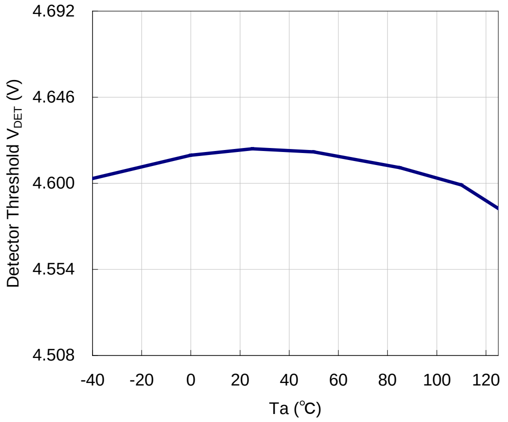
VD=1.6V



VD=3.0V

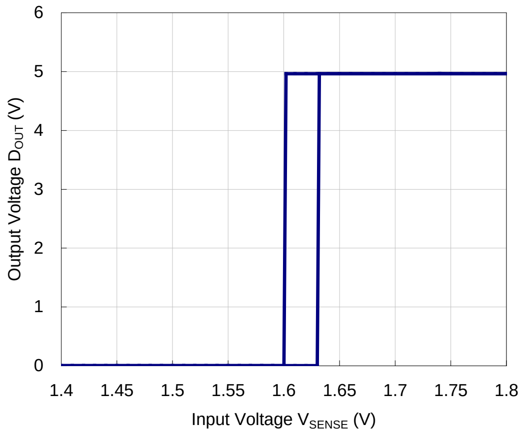


VD=4.6V

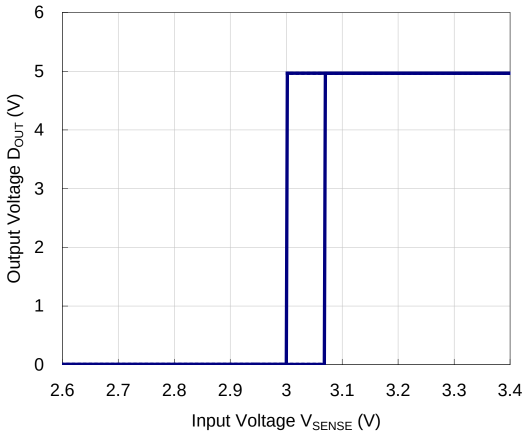


15) D_{OUT} Pin Voltage vs. SENSE Pin Input Voltage (D_{OUT} pulled-up to 5V with 100kΩ)

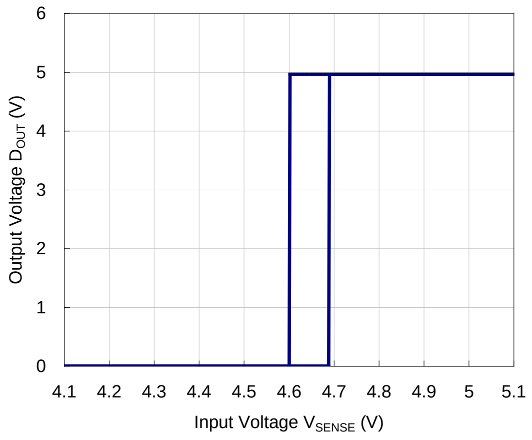
VD=1.6V



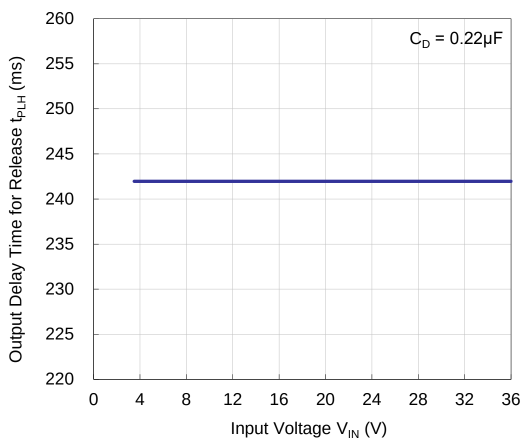
VD=3.0V



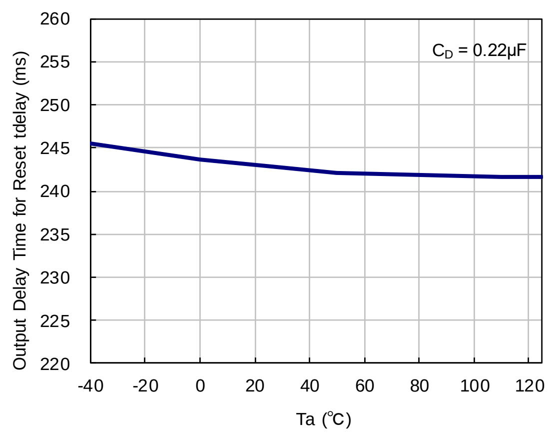
VD=4.6V



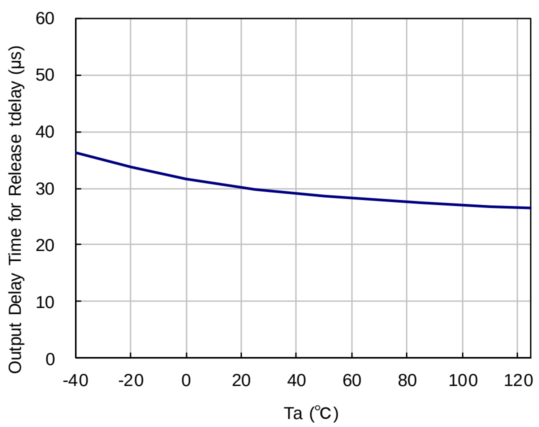
16) Release Output Delay Time vs. Input Voltage



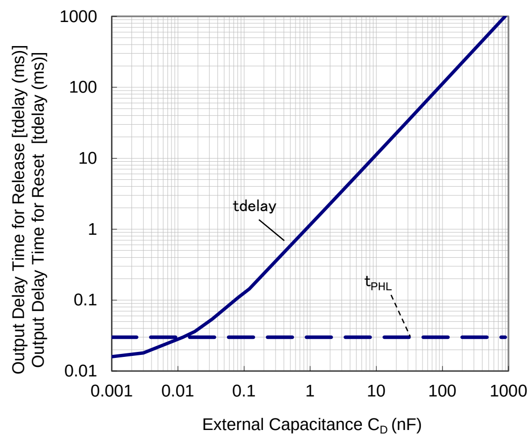
17) Release Output Delay Time vs. Temperature



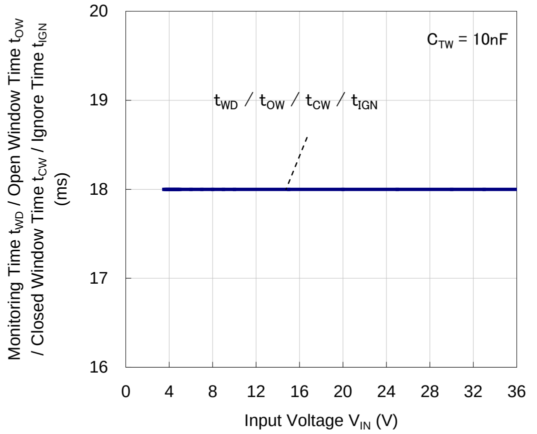
17) Detect Output Delay Time vs. Temperature



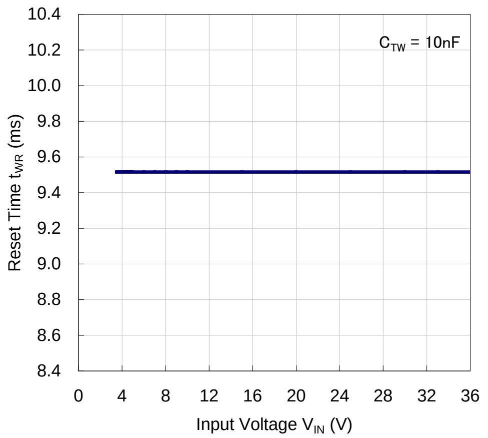
19) Release Output Delay Time and Detect Delay Time vs. External Capacitor for C_D Pin



20) WDT t_{WD} / t_{OW} / t_{CW} / t_{IGN} vs. Input Voltage

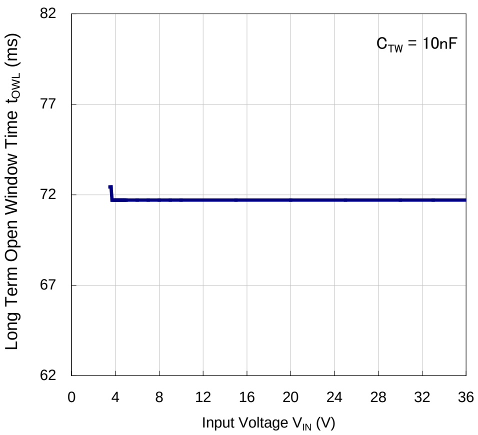


21) Reset Time vs. Input Voltage

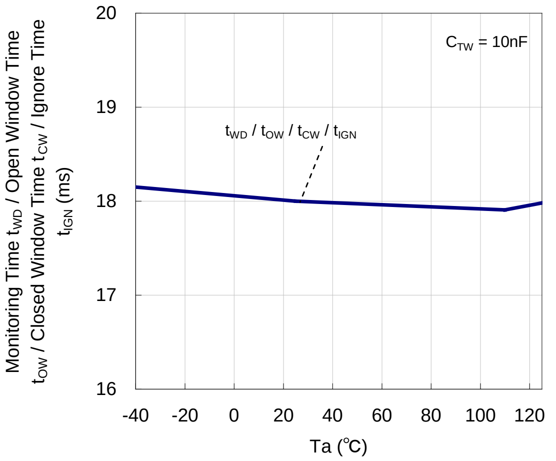


22) Long Open Window Time vs. Input Voltage

R5110SxxxB/D

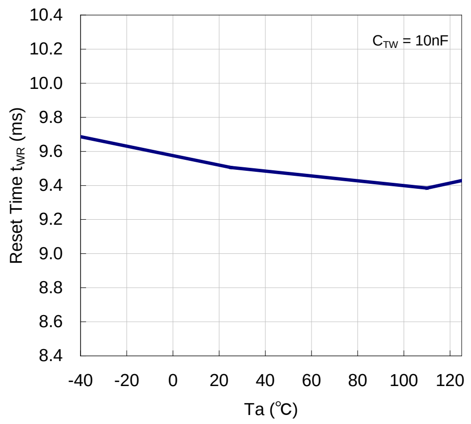


23) WDT t_{WD} / t_{OW} / t_{CW} / t_{IGN} vs. Temperature



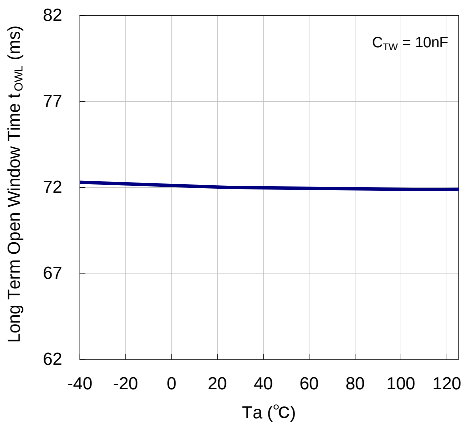
RICOH

24) Reset Time vs. Temperature

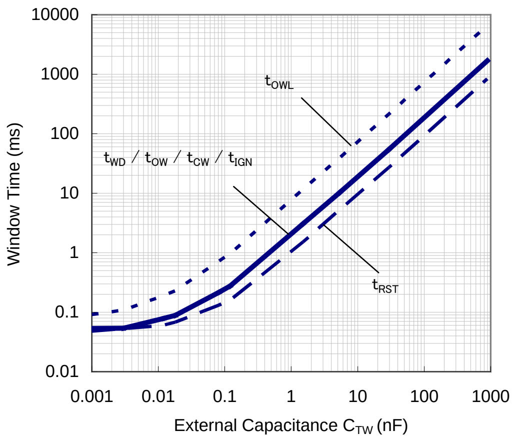


25) Long Open Window Time vs. Temperature

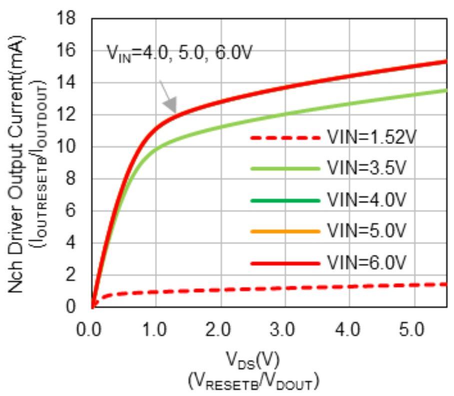
R5110SxxxB/D



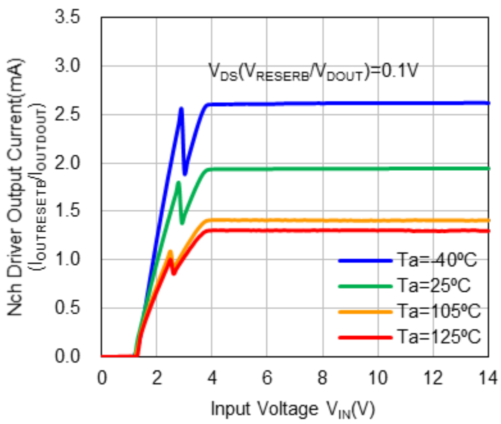
26) WDT t_{WD} / t_{OW} / t_{CW} / t_{IGN} /t_{OWL} / t_{RST} Vs. External Capacitor for C_{TW} Pin



27) Nch. Driver Output Current vs. V_{DS}



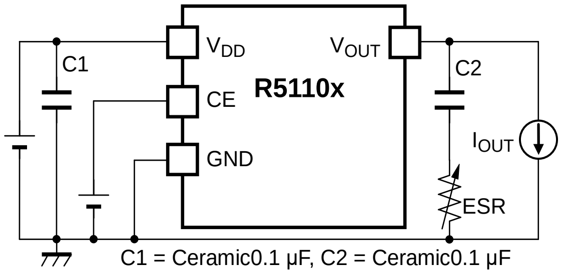
28) Nch. Driver Output Current vs. Input Voltage



RICOH

ESR vs. Output Current

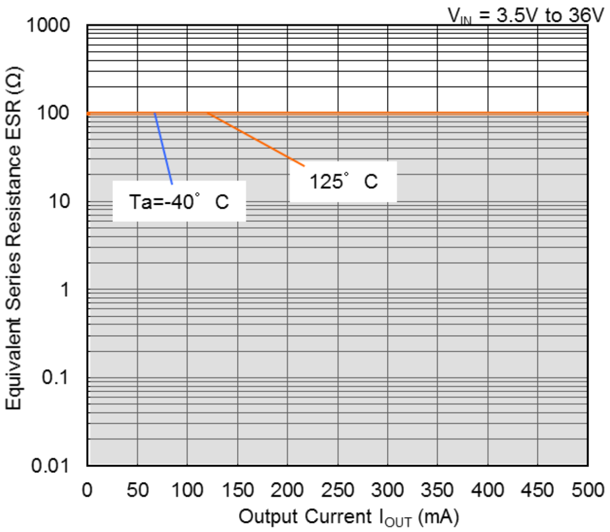
The IC is recommended to use a ceramic type capacitor, but the IC can be used other capacitors of the lower ESR type. The relation between the output current (I_{OUT}) and the ESR of output capacitor is shown below.



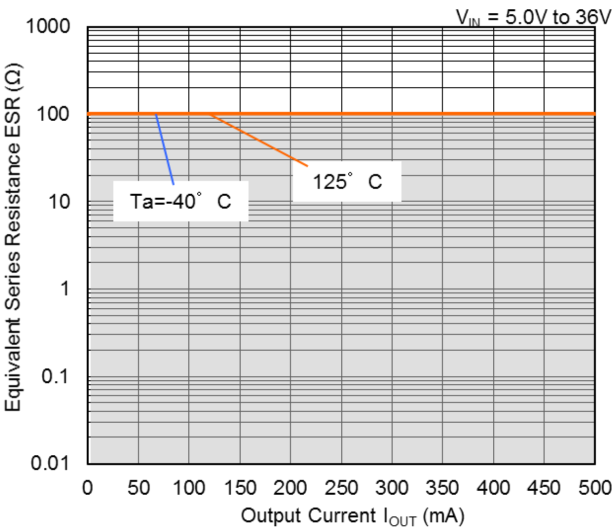
Measurement conditions:

Frequency Band: 10 Hz to 2 MHz
Measurement Temperature: −40°C to 125°C
Hatched area: Noise level is 40 µV (average) or below
Ceramic Capacitor: C1 = C2 = Ceramic 0.1 µF

VR = 1.8V, 3.3V



VR = 5.0V



Ver. B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

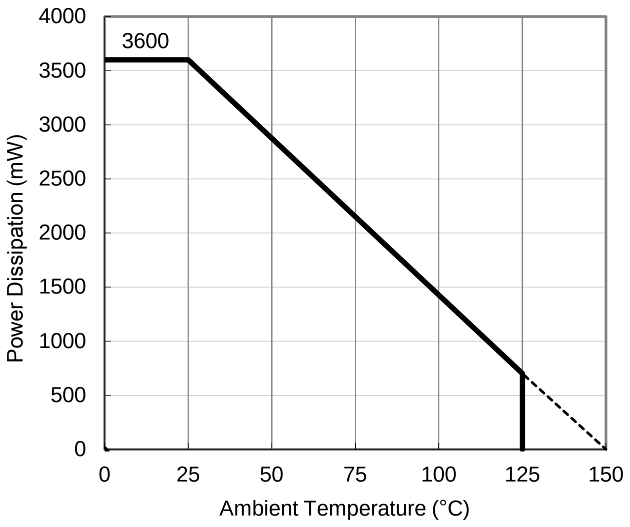
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 150°C)

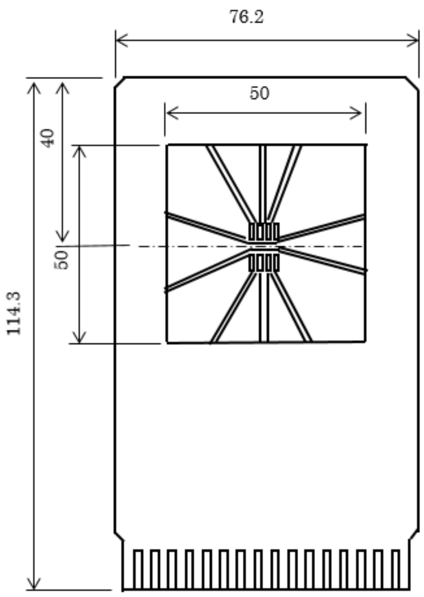
Item	Measurement Result
Power Dissipation	3600 mW
Thermal Resistance (θja)	θja = 34.5°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 10°C/W

θja: Junction-to-Ambient Thermal Resistance

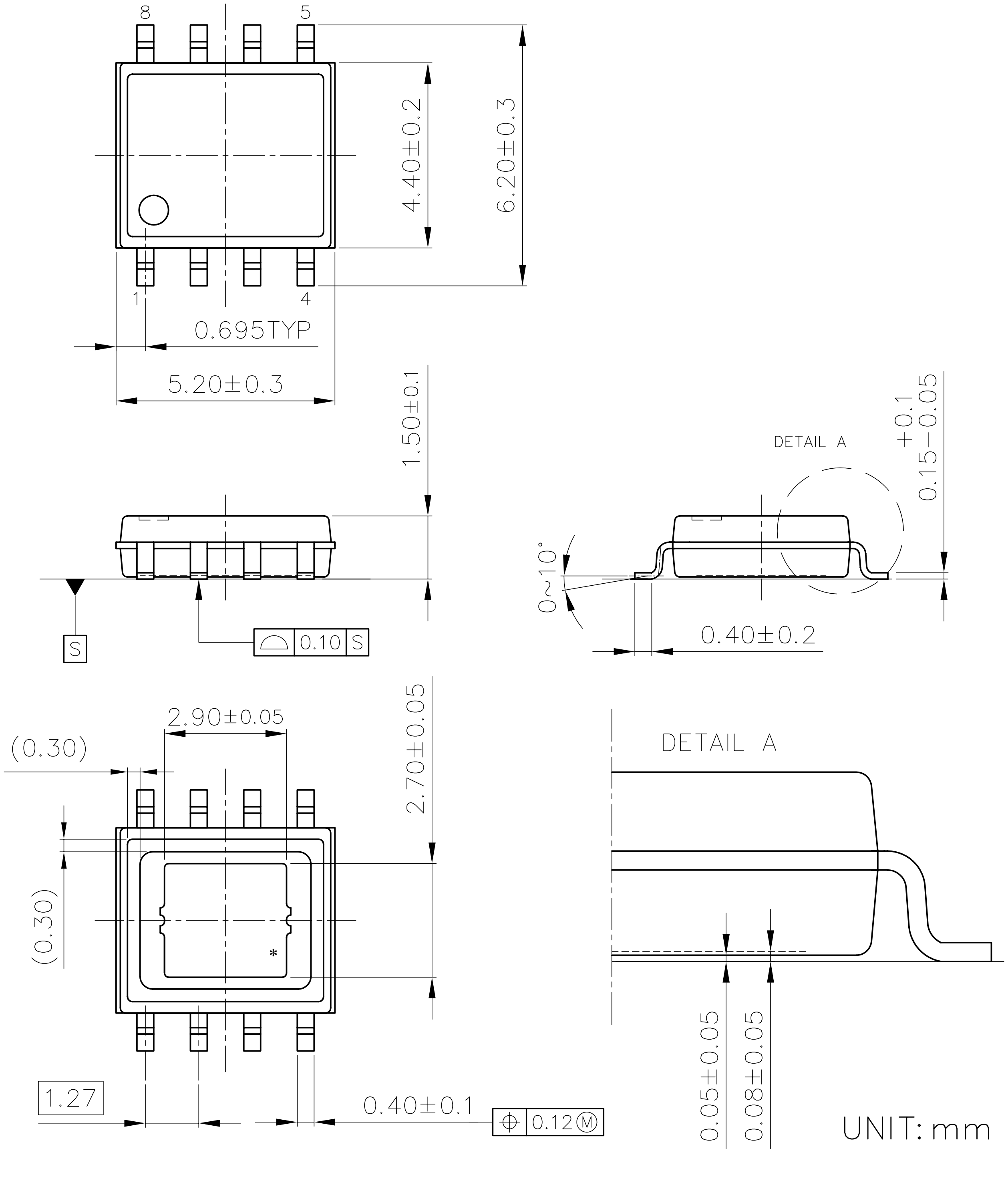
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



HSOP-8E Package Dimensions

∗ The tab on the bottom of the package shown by blue circle is substrate potential (GND). It is recommended that this tab be connected to the ground plane pin on the board but it is possible to leave the tab floating.

Ver. B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

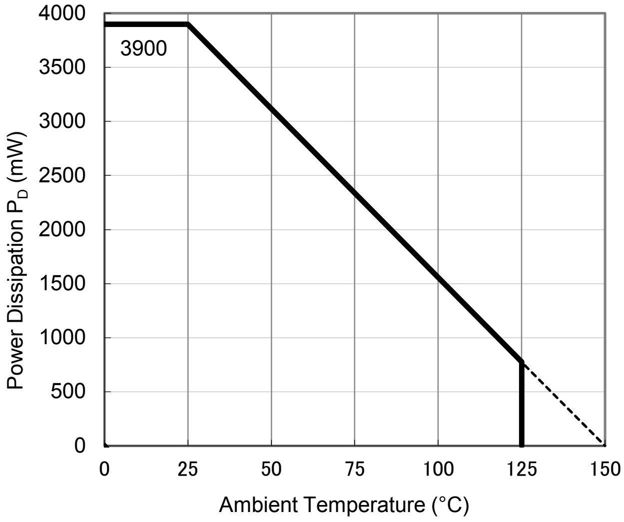
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 150°C)

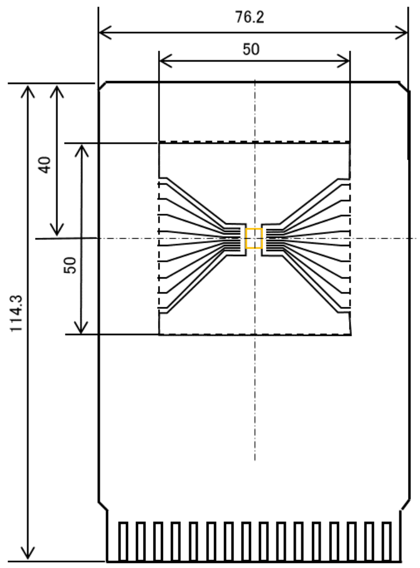
Item	Measurement Result
Power Dissipation	3900 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

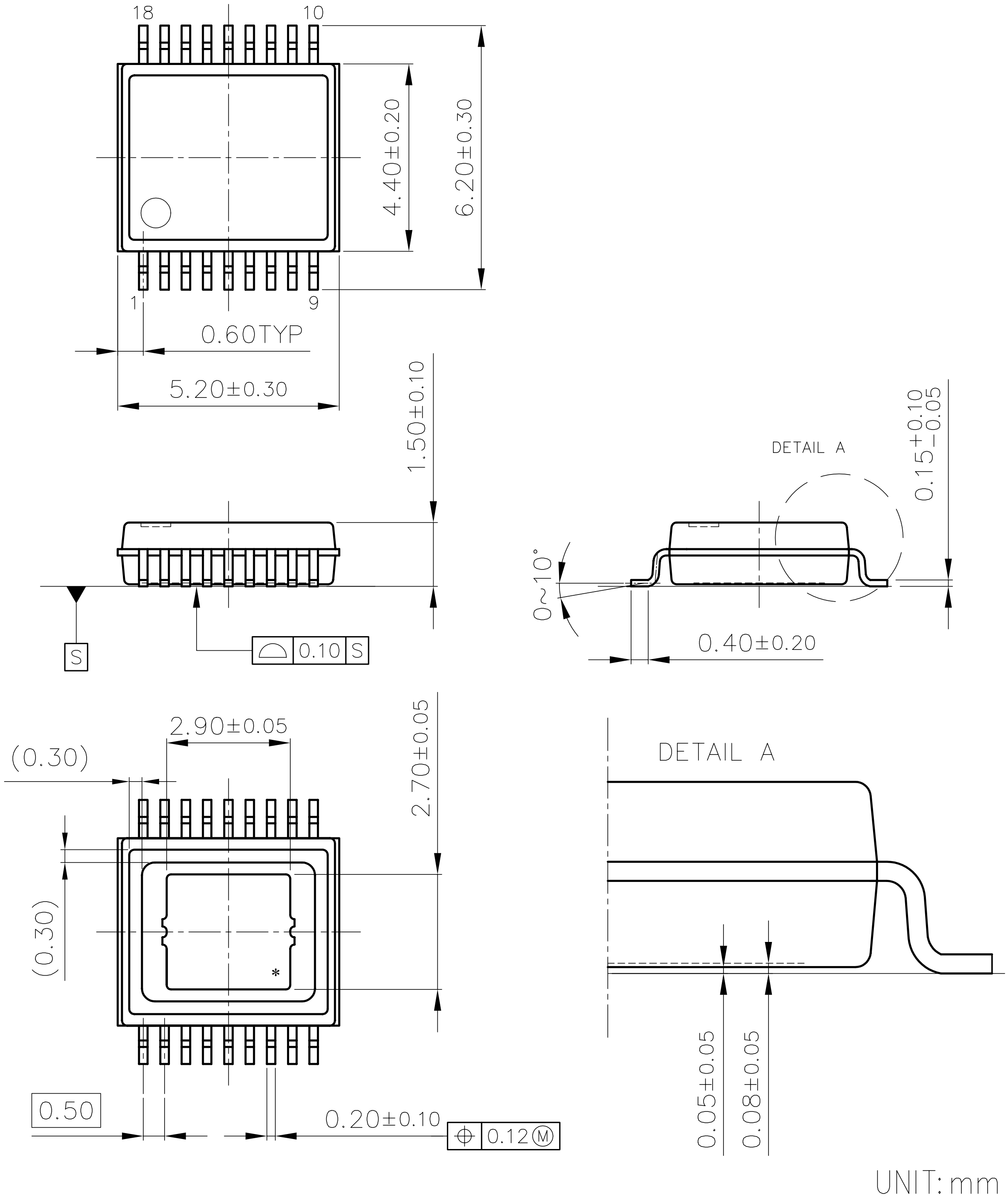


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

Ver. A



HSOP-18 Package Dimensions

∗ The tab on the bottom of the package shown by blue circle is substrate potential (GND). It is recommended that this tab be connected to the ground plane pin on the board but it is possible to leave the tab floating.

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

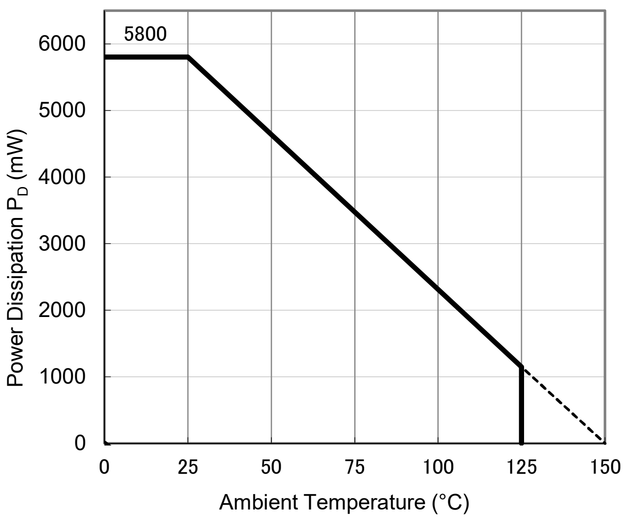
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 72 pcs

Measurement Result (Ta = 25°C, Tjmax = 150°C)

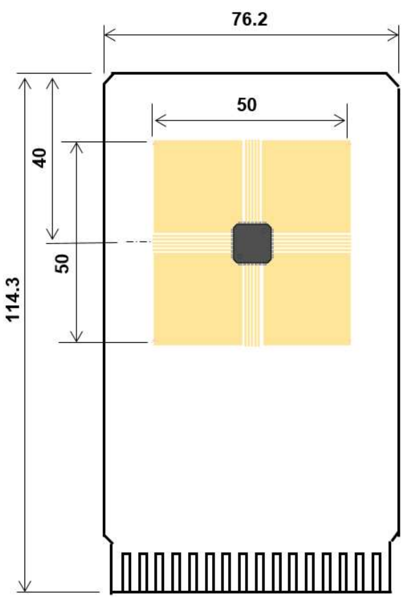
Item	Measurement Result
Power Dissipation	5800 mW
Thermal Resistance (θja)	θja = 21.5°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 5°C/W

θja: Junction-to–ambient thermal resistance.

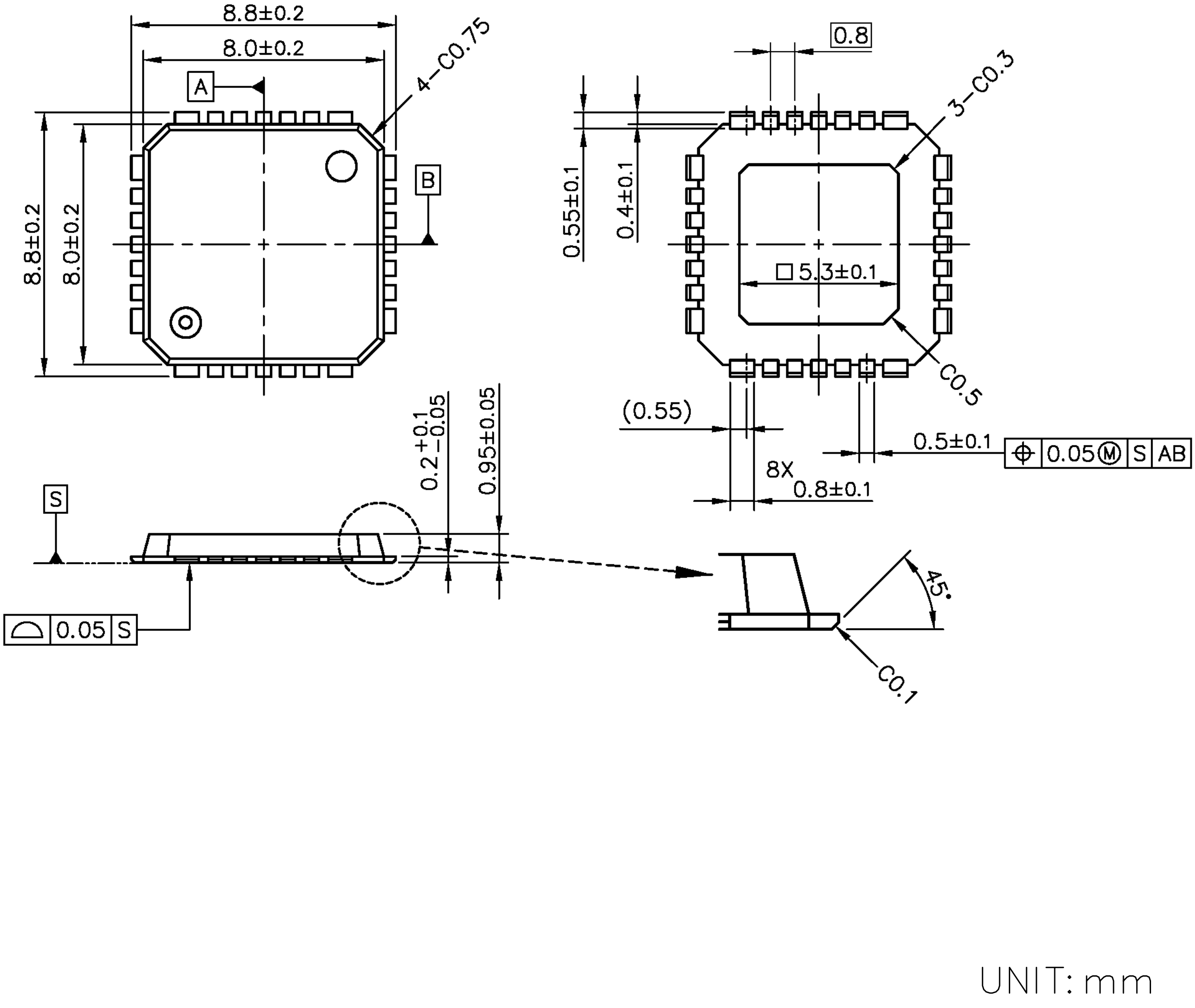
ψjt: Junction–to-top of package thermal characterization parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



HQFN0808-28 Package Dimensions

*The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane pin on the board but it is possible to leave the tab floating.

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to Ricoh sales representatives for the latest information thereon.
2. The materials in this document may not be copied or otherwise reproduced in whole or in part without prior written consent of Ricoh.
3. Please be sure to take any necessary formalities under relevant laws or regulations before exporting or otherwise taking out of your country the products or the technical information described herein.
4. The technical information described in this document shows typical characteristics of and example application circuits for the products. The release of such information is not to be construed as a warranty of or a grant of license under Ricoh's or any third party's intellectual property rights or any other rights.
5. The products in this document are designed for automotive applications. However, when using the products for automotive applications, please make sure to contact Ricoh sales representative in advance due to confirming the quality level.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. Anti-radiation design is not implemented in the products described in this document.
8. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
9. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
10. There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact Ricoh sales or our distributor before attempting to use AOI.
11. Please contact Ricoh sales representatives should you have any questions or comments concerning the products or the technical information.

RoHS Compliant
Halogen Free

Ricoh is committed to reducing the environmental loading materials in electrical devices with a view to contributing to the protection of human health and the environment.
Ricoh has been providing RoHS compliant products since April 1, 2006 and Halogen-free products since April 1, 2012.

RICOH ELECTRONIC DEVICES CO., LTD.

Official website
https://www.e-devices.ricoh.co.jp/en/
Contact us
https://www.e-devices.ricoh.co.jp/en/support/