RICOH

R5434D Series

2 to 5 Serial Cell Li-Ion / Li-Polymer Battery Protection IC for Secondary Protection

NO.EA-267-201201

OUTLINES

The R5434D is an overcharge protection IC for 2 to 5 serial Li-ion/Li-polymer secondary battery. When an overcharge is detected, after the IC internally fixed delay time, the output of COUT becomes "H". After detecting the overcharge, when the cell voltage becomes lower than the overcharge release voltage, the overcharge state is released.

By forcing VDD+3.0V or more to the CTLC pin, the test time of protection circuit board can be shortened, and overcharge delay time becomes about 1/30. The output type is CMOS.

FEATURES

- Manufactured with High Voltage Tolerant Process
  Absolute Maximum Rating ····· 30V
- Low Supply Current
  Cell Voltage 3.9V, for 5-cell ····· Typ. 3.0µA
- High-accuracy Detector Threshold
  Overcharge Detector ····· ±25mV (Ta=25°C)
- Variety of Detector Threshold
  Overcharge Detector Threshold (V_{DET1n}[(1)]) ····· 3.6V - 4.6V (in 5mV step)
  Overcharge Release Voltage (V_{REL1n}[(1)]) ····· V_{DET1n} - 0.1V to V_{DET1n} - 0.4V (in 50mV steps)
  Overcharge Detector Output Delay ····· Typ.1.5s
  Overcharge Released Condition ····· Voltage Released Type
- 2 to 5 Cells Selectable Protection
- COUT Output (CMOS Output, Active-high) ····· Typ. 3.7V
  (“Low” at normal times, “High” at detecting times)
- Overcharge Delay Time Shortening Function with CTLC pin
  VDD+3.0V or more ····· 1sec to about 1/30
  2.0V to VDD-2.0V ····· about 4ms.
- Small Package ····· SON-8

APPLICATIONS

- Li-ion or Li-polymer Battery Protection

(1) V_{DET1n}, V_{REL1n} : n =1, 2, 3, 4, 5

SELECTION GUIDE

The overcharge and the delay time are user-selectable options.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5434Dxxx$∗-TR -FE	SON-8	3,000 pcs	Yes	Yes

xxx: Specify the combination of the overcharge detector threshold (V_{DET1n}) and the overcharge release voltage (V_{REL1n}) [(1)].

V_{DET1n}[(2)]: 3.6 V to 4.6 V in 5 mV step
V_{REL1n}[(2)]: V_{DET1n} – 0.1 V to V_{DET1n} – 0.4 V in 50 mV step

$: Specify the delay time option.
A: Overcharge Detection Delay Time (t_{VDET1}) : 1.5s

∗: Specify the overcharge release option.
A: Voltage Released Type

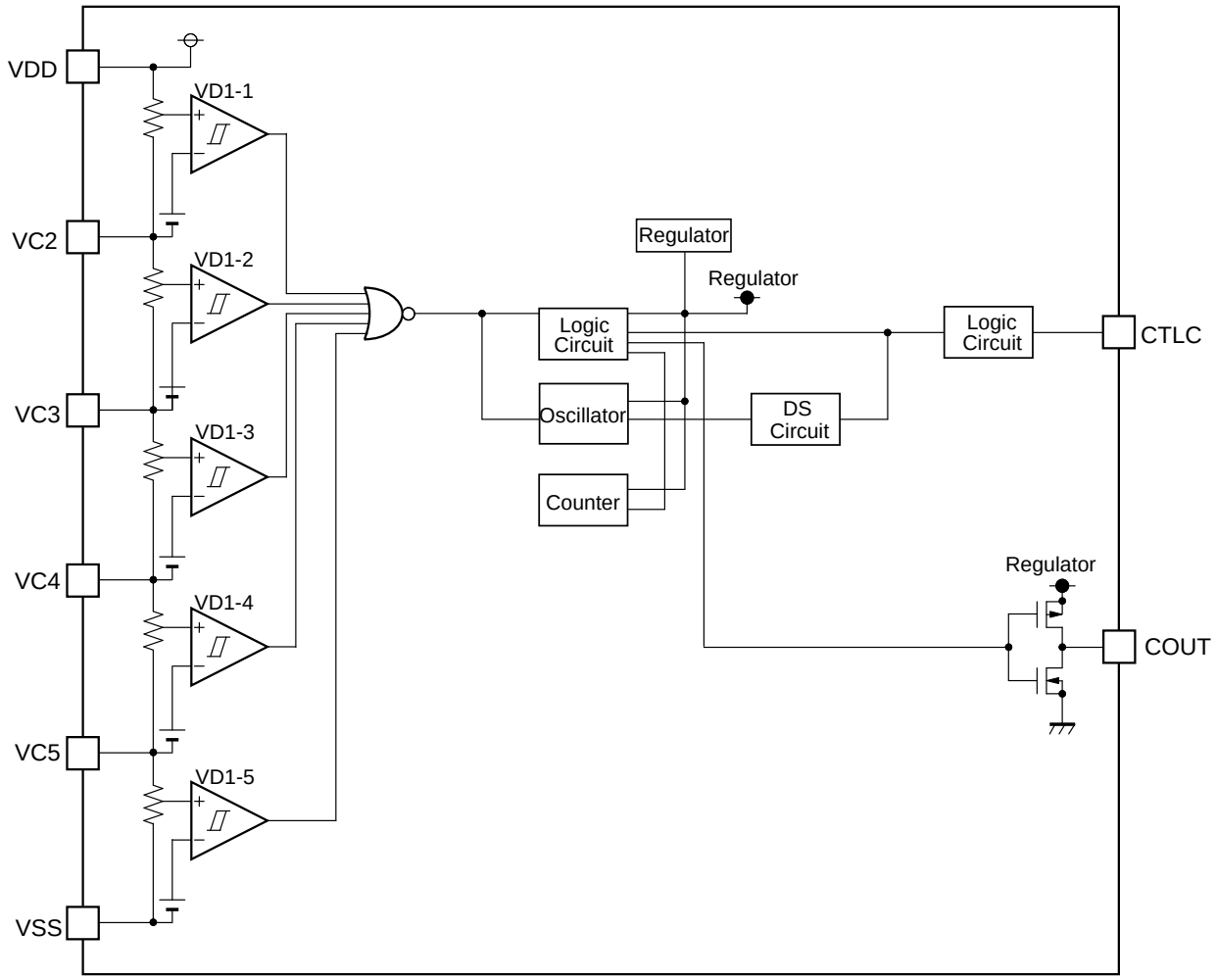
Product Code List

The product code is determined by the combination of the set output voltage (overcharge detection voltage: V_{DET1n}, overcharge release voltage: V_{REL1n}), the delay time (overcharge detection delay time: t_{VDET1}), and the overcharge release options.

Product Code	Set Voltages [V]		Overcharge Detection Delay Time [s]	Overcharge Released Type
	V_{DET1n}	V_{REL1n}	t_{VDET1}	
R5434D401AA	4.300	4.000	1.5	Voltage Release
R5434D402AA	4.220	4.120	1.5	Voltage Release
R5434D403AA	4.250	4.000	1.5	Voltage Release
R5434D404AA	4.350	4.050	1.5	Voltage Release
R5434D405AA	3.825	3.575	1.5	Voltage Release
R5434D406AA	4.220	3.820	1.5	Voltage Release
R5434D407AA	4.250	4.200	1.5	Voltage Release

(1) Refer to *Product Code Table* for details.
(2) V_{DET1n}, V_{REL1n}: n = 1, 2, 3, 4, 5

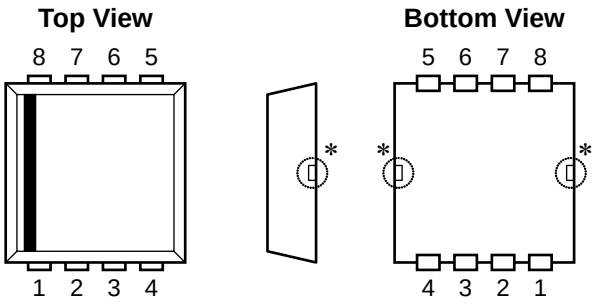
BLOCK DIAGRAM



R5434DxxxAA Block Diagram

PIN DESCRIPTION

SON-8



Pin No.	Symbol	Description
1	VC5	Positive terminal pin for Cell-5
2	VC4	Positive terminal pin for Cell-4
3	VC3	Positive terminal Pin for Cell-3
4	VC2	Positive terminal pin for Cell-2
5	VDD	VDD pin, positive terminal pin for Cell-1
6	CTLC	COUT control pin / Output delay time shortening pin
7	COUT	Output pin of overcharge detection, CMOS output
8	VSS	VSS pin. Ground pin for the IC

* The tab suspended leads are connected to the GND level. Do not short or wire those parts to other voltage level parts.

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, V_{SS} = 0V)

Symbol	Item	Ratings	Unit
V_{DD}	Supply voltage (Positive terminal pin voltage of Cell-1)	-0.3 to 30 V_{C2}-0.3 to V_{C2}+6.5	V
V_{C2}	Positive input pin voltage for Cell-2	V_{C3} -0.3 to V_{C3}+6.5	V
V_{C3}	Positive input pin voltage for Cell-3	V_{C4} –0.3 to V_{C4}+6.5	
V_{C4}	Positive input pin voltage for Cell-4	VC5–0.3 to V_{C5}+6.5	
V_{C5}	Positive input pin voltage for Cell-5	-0.3 to 6.5	
V_{CTLC}	CTLC pin voltage	-0.3 to 30	
V_{COUT}	COUT pin output voltage	-0.3 to V_{OH1}+0.3	V
P_D	Power Dissipation (1)	Refer to Appendix “Power Dissipation”.	
Tj	Junction Temperature Range	-40 to 125	°C
Tstg	Storage Temperature Range	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITION

Symbol	Item	Rating	Unit
V_{DD}	Operating Input Voltage	4.0 to 25	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to *POWER DISSIPATION* in *SUPPLEMENTSRY ITEMS* for detail information.

ELECTRICAL CHARACTERISTICS

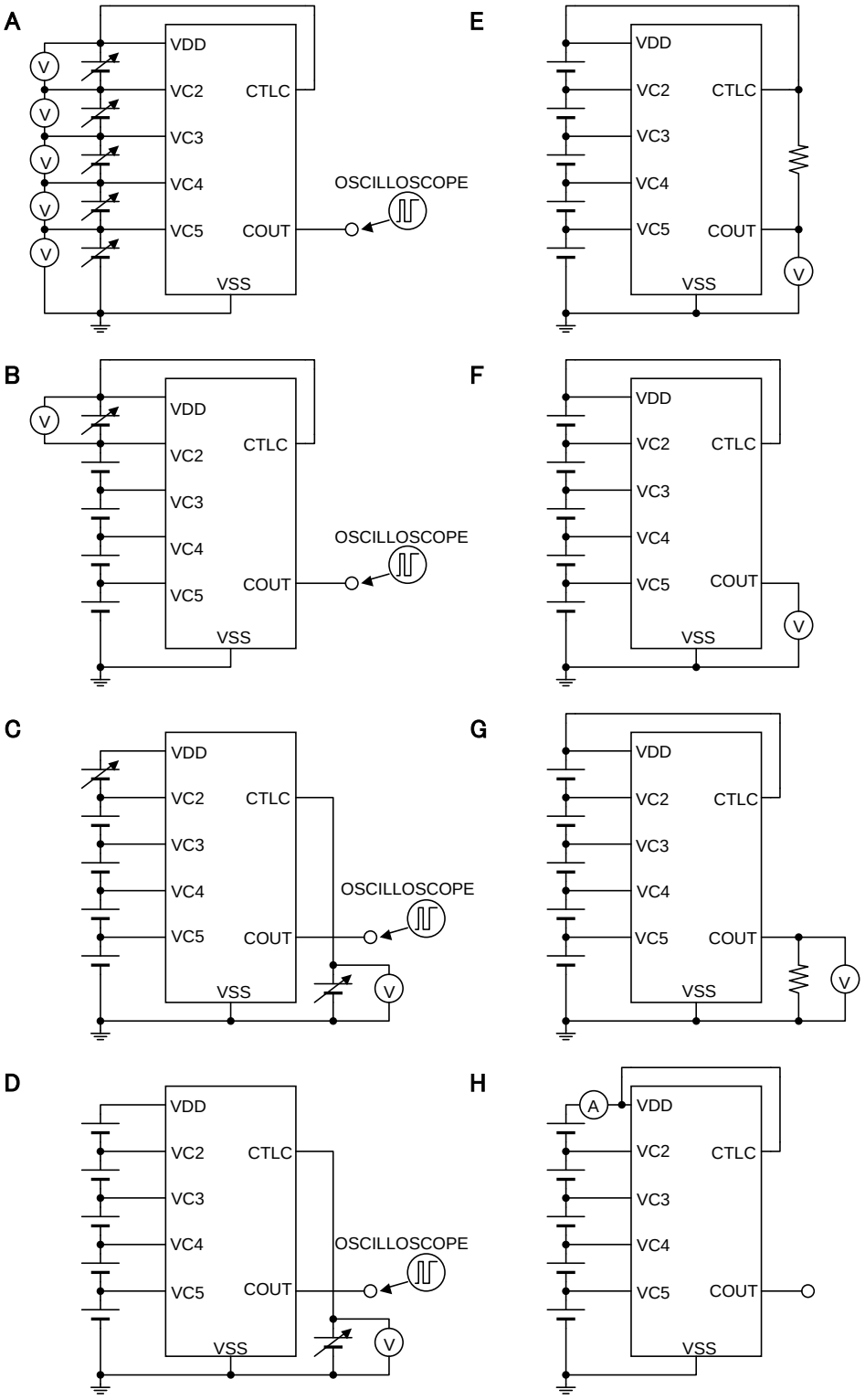
V_{CELLn} = CELLn (Ex. V_{CELL1} is a voltage difference between VDD and VC2), n = 1, 2, 3, 4, 5, unless otherwise noted. The specifications surrounded by ☐ are guaranteed by Design Engineering at 0°C ≤ Ta ≤ 60°C.

R5434DxxxAA Electrical Characteristics (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Circuit (1)
V_{DET1n}	CELLn Overcharge Detection Threshold	Detect rising edge of supply voltage (25°C)	V_{DET1n} -0.025V	V_{DET1n}	V_{DET1n} +0.025V	V	A
		Detect rising edge of supply voltage (0 to 60°C)	V_{DET1n} -0.030V	V_{DET1n}	V_{DET1n} +0.030V		
V_{REL1n}	CELLn Overcharge Release Voltage	Detect falling edge of supply voltage	V_{REL1n} -0.050V	V_{REL1n}	V_{REL1n} +0.050V	V	A
t_{VDET1}	Overcharge Detection Delay Time	V_{CELLn}=3.5V (n=2,3,4,5), V_{CELL1}=3.5V to 4.5V,	1.05	1.50	1.95	s	B
t_{VREL1}	Overcharge Release Delay Time	V_{CELLn}=3.5V (n=2,3,4,5), V_{CELL1}=4.5V to 3.5V,	11	16	21	ms	B
t_{VDTR1}	Overcharge Detection Timer Reset Delay Time	V_{CELLn}=V_{DET1n}+0.050V to V_{REL1n}-0.100V to V_{DET1n}+0.050V to V_{REL1n}-0.100V	8	16	24	ms	B
V_{IH-1}	CTLC Pin "High1" Input Voltage		V_{DD} -0.7V		V_{DD} +0.3V	V	C
V_{IH-2}	CILC Pin "High2" Input Voltage		V_{DD} +3.0V			V	C
V_{IM}	CTLC Pin "Middle" Input Voltage	V_{DD} ≥ 4 V	2.0		V_{DD} -2.0V	V	C
V_{IL}	CTLC Pin "Low" Input Voltage	V_{DD} ≥ 4 V	V_{SS} -0.3V		0.5	V	D
V_{OL}	COUT Nch. ON Voltage	I_{OL}=50µA, V_{CELLn}= 3.5V, CTLC= VDD		0.1	0.5	V	E
V_{OH1}	COUT Pch. ON Voltage1 (at no load)	I_{OH} = 0µA, V_{CELLn} = 3.5V, CTLC= VSS	3.0	3.7	4.5	V	F
V_{OH}	COUT Pch. ON Voltage	I_{OH}= -50µA, V_{CELLn} = 3.5V, CTLC= VSS	V_{OH1} -0.5V	V_{OH1} -0.1V		V	G
I_{SS}	Supply Current	V_{CELLn}=3.9V		3.0	7.0	µA	H

(1) Refer to *TEST CIRCUITS* for detail information.

TEST CIRCUITS



THEORY OF OPERATION

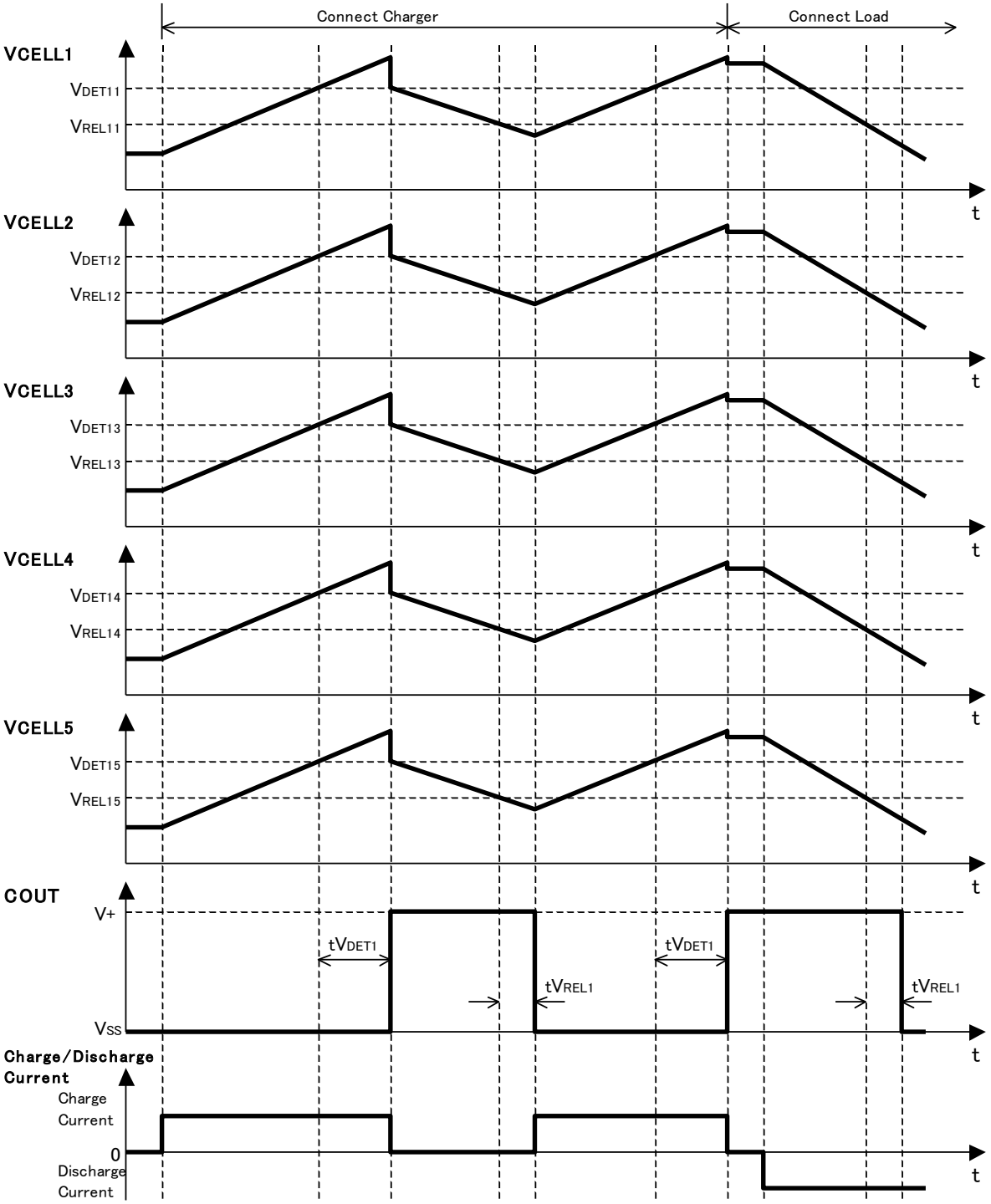
Overcharge Detectors, V_{DET1n} (n=1, 2, 3, 4, 5)

While the cells are charged, the voltage between VDD pin and VC2 pin (voltage of the Cell-1), the voltage between VC2 pin and VC3 pin (voltage of the Cell-2), the voltage between VC3 pin and VC4 pin (voltage of the Cell-3), the voltage between VC4 pin and VC5 pin (voltage of the Cell-4), and the voltage between VC5 and VSS pin (voltage of the Cell-5) are supervised. If at least one of the cells' voltage becomes equal or more than the overcharge detection voltage, the overcharge is detected, and an external charge control Nch. FET turns ON with COUT pin being at "H" level and by cutting off a fuse on the charger path, and the charge operation stops.

To reset the overcharge and make the COUT pin level to "Low" again after detecting overcharge, in such conditions that a time when all the cells' voltages are down to a level lower than overcharge release voltage.

Internal fixed output delay times for overcharge detection, overcharge detector timer reset, release from overcharge exist. Even if one of voltage of the cells keeps its level more than the overcharge detection voltage, and output delay time passes, overcharge voltage is detected. If all the cell voltages become lower than the overcharge detection voltage within the overcharge detection delay time by noise or other reasons, the time period is less than overcharge detector timer reset output delay time, the overcharge delay time is accumulated and maintained, and the accumulated delay time reaches the overcharge delay time, the overcharge is detected. After detecting overcharge, even if all the cell voltages become equal or less than the release voltage from overcharge, if at least one of the cells voltage becomes higher than the release voltage from overcharge within the overcharge release delay time from overcharge, then overcharge is not released.

The output type of the COUT pin is a CMOS output between VSS and the built-in regulator, and "High" level of COUT pin is the output voltage of the built-in regulator.



Overcharge Operation Timing Chart

Delay Shortening (DS) Function

The COUT pin is forcibly set to "High" output with applying the VSS level voltage to the CTLC pin.
By applying VDD+3.0V or more voltage to the CTLC pin, the overcharge detect and release delay times can be shorten into approximately 1/30. (DS mode 1)
By applying the voltage in the range from 2.0V to VDD-2.0V to CTLC pin, the overcharge detect delay time can be shorten into approximately 4ms. (DS mode 2)
The CTLC pin has internally the input delay time (approximately 1ms).

Table. CTLC Pin Input Conditions and IC's Operating Conditions ($V_{DD} \geq 4.0$ V)

Input Conditions to CTLC Pin	IC Operating Conditions
V_{DD}+3.0V or more	DS mode 1
V_{DD}-0.8V to V_{DD}+0.3V	Normal operation
2.0V to V_{DD}-2.0V	DS mode 2
V_{SS}-0.3V to 0.5V	COUT output "H"
Open	Indefinite

Setting for 2 to 4 Cell Protection

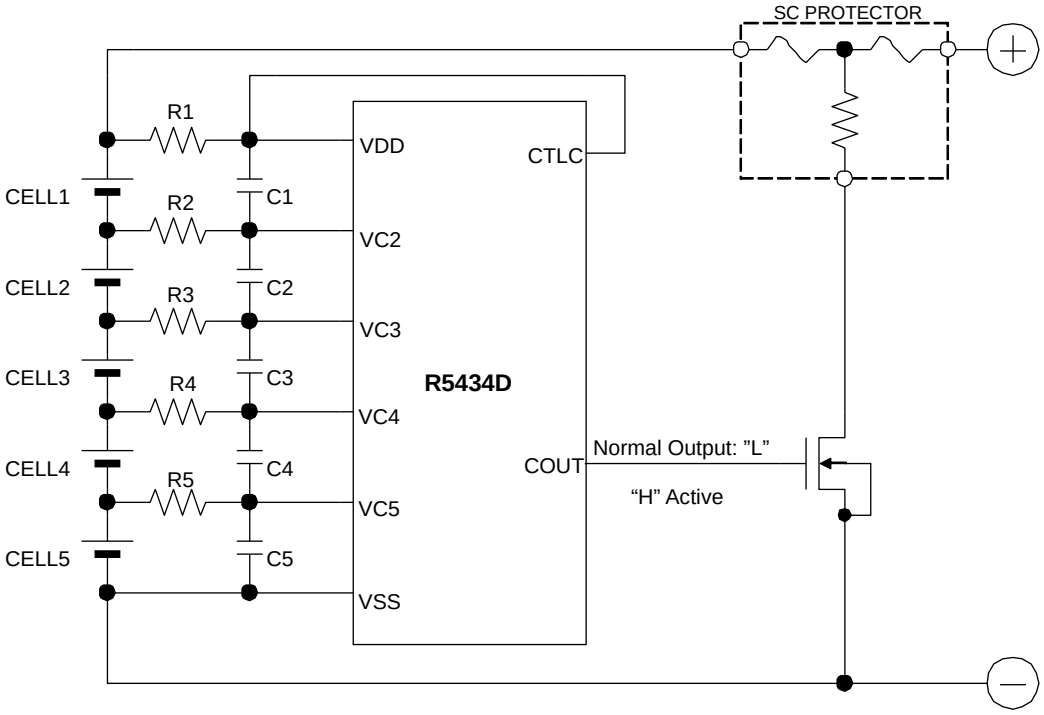
By short-circuiting between cells, the R5434D can meet as a protection IC for 2, 3, or 4 cells placed in series. The following table indicates pins to short-circuit to VSS depending on protected cells.

Protected Cells	Pins to Short-circuit to VSS
2-cell protection	VC3, VC4, and VC5 pins
3-cell protection	VC4 and VC5 pins
4-cell protection	VC5 pin

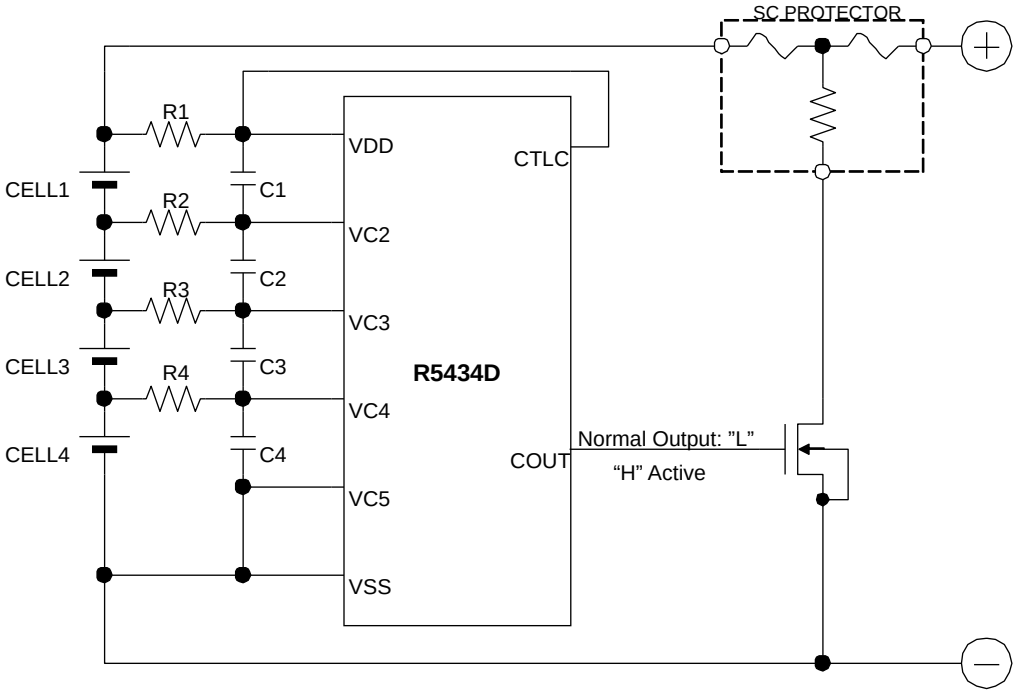
If providing other connections except above short-circuit for 2, 3, or 4 cells protection, perform thorough evaluation using the actual devices.

TYPICAL APPLICATIONS

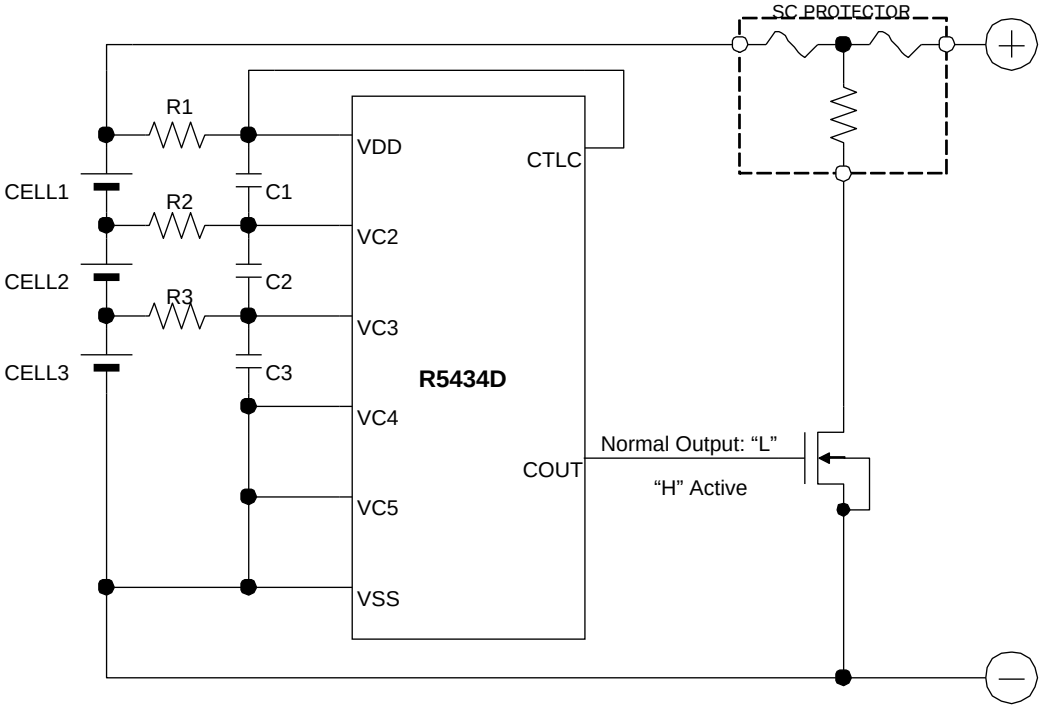
Typical Application Circuits



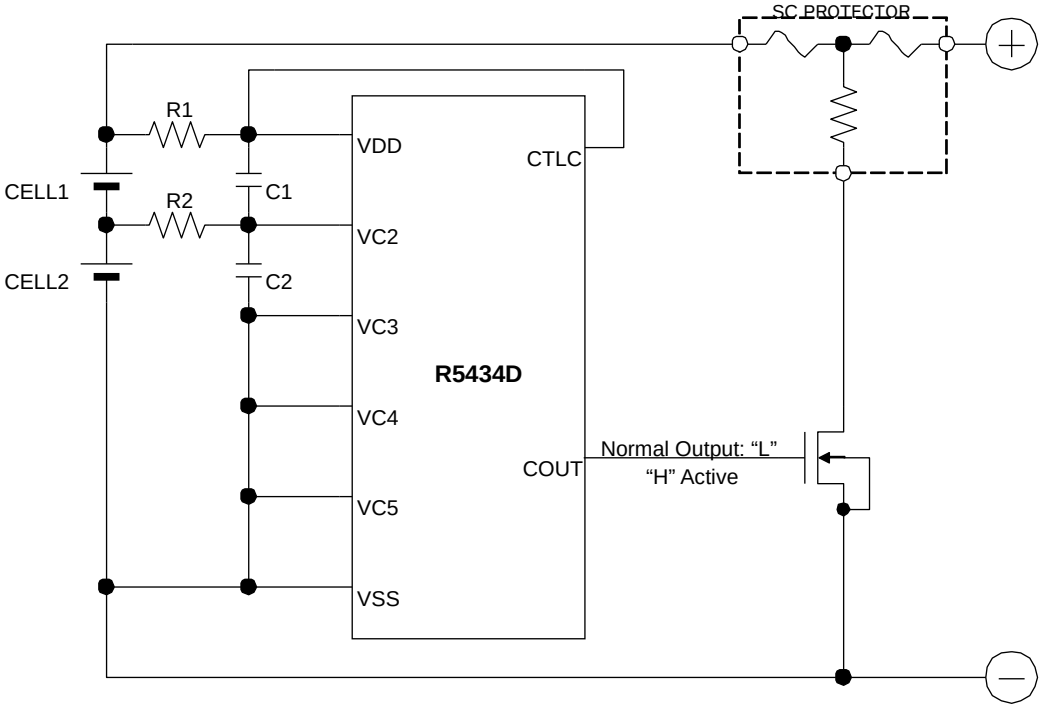
5-cell Protection Circuit



4-cell Protection Circuit



3-cell Protection Circuit



2-cell Protection Circuit

External Components

Symbol	Min.	Typ.	Max.	Unit
R1 / R2 / R3 / R4 / R5	330	330	1000	Ω
C1 / C2 / C3 / C4 / C5	0.01	0.1	1	μF

Technical Notes on Selection Components

- The voltage fluctuation is stabilized with R1 to R5 and C1 to C5. If a R1 to R5 is too large, by the conduction current at detection, the detector threshold may shift higher. Therefore, the appropriate value range of R1 to R5 is equal or less than 1kΩ. To make a stable operation of the IC, the appropriate value range of C1 to C5 is 0.01μF or more.
- The typical application circuit diagrams are just examples. This circuit performance largely depends on the PCB layout and external components. In the actual application, fully evaluation is necessary.
- Overvoltage and the over current beyond the absolute maximum rating should not be forced to the protection IC and external components. During the time until the fuse is open after detecting overcharge, a large current may flow through the FET. Select an FET with large enough current capacity in order to endure the large current.
- To connect the SC protector, connect the SC protector to the cell must be the last.

Contact Information for Inquiries regarding SC PROTECTOR

Dexerials Corporation (Sony Chemical & Information Device Company Ltd.)
Gate-city Osaki East Tower 8F, 1-11-2 Osaki, Shinagawa, Tokyo, 141-0032
TEL: 03-5435-3946
URL: http://www.dexerials.jp

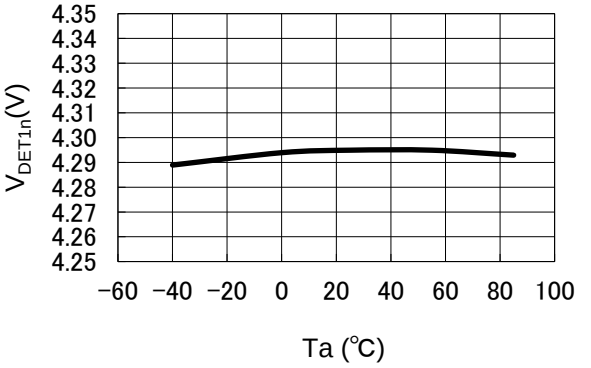
TYPICAL CHARACTERISTICS

Vs. Temperature

1) CELLn Overcharge Detector Threshold vs. Temperature

R5434D401AA n=1, 2, 3, 4, 5

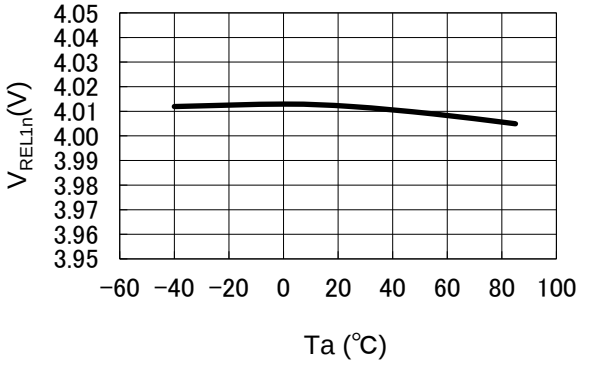
V_{CELLn}=3.2V



2) CELLn Overcharge Release Voltage vs. Temperature

R5434D401AA n=1, 2, 3, 4, 5

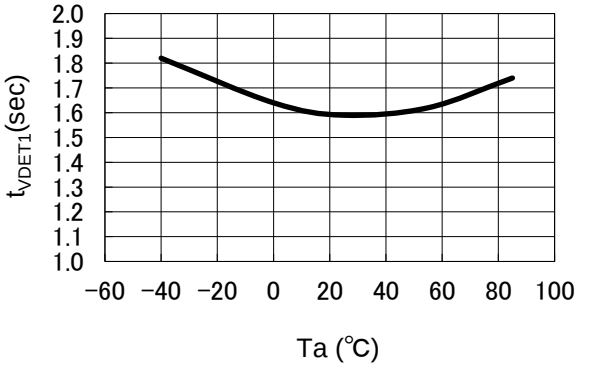
V_{CELLn}=3.2V



3) Overcharge Detection Delay Time vs. Temperature

R5434D401AA n=1, 2, 3, 4, 5

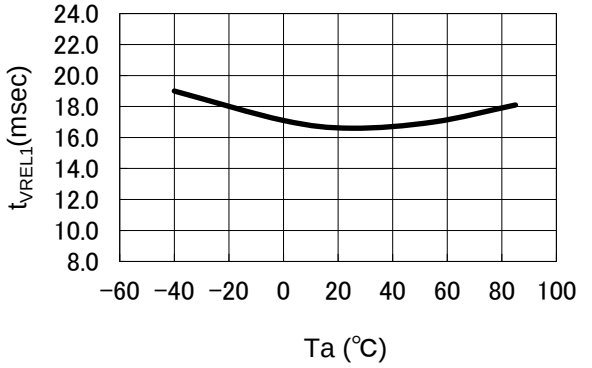
V_{CELLn}=3.5V、V_{CELL1}=3.5V→4.5V



4) Overcharge Release Delay Time vs. Temperature

R5434D401AA n=1, 2, 3, 4, 5

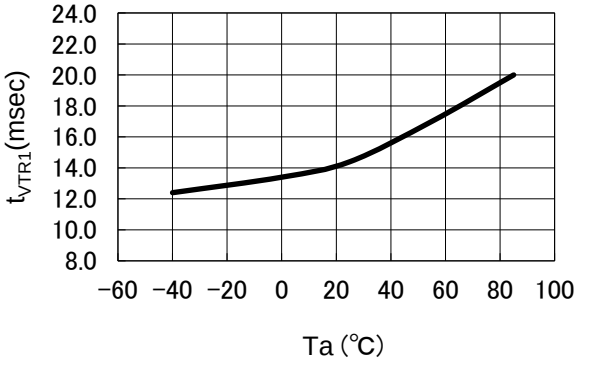
V_{CELLn}=3.5V、V_{CELL1}=4.5V→3.5V



5) Timer Reset Delay Time vs. Temperature

R5434D401AA n=1, 2, 3, 4, 5

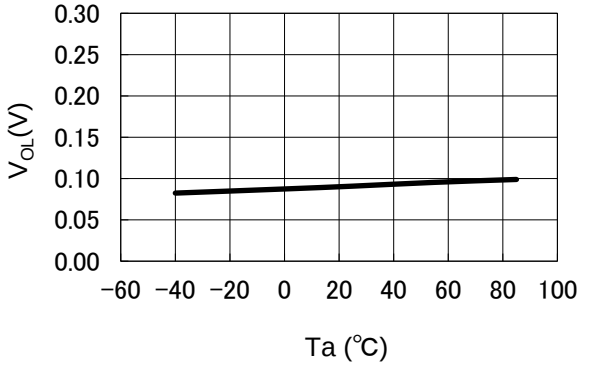
V_{CELLn}=3.5V、V_{CELL1}=4.5V→3.5V→4.5V



6) COUT Nch. ON Voltage vs. Temperature

R5434D401AA n=1, 2, 3, 4, 5

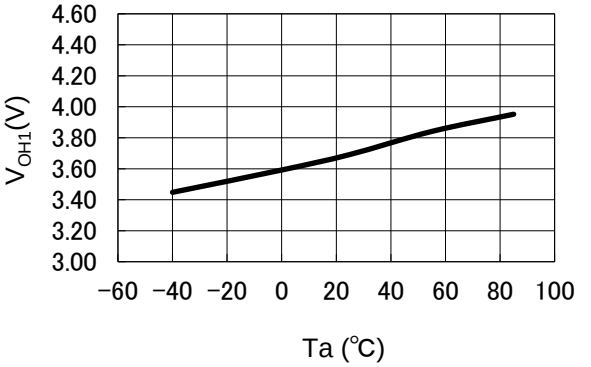
V_{CELLn}=3.5V、V_{CELL1}=4.5V→3.5V→4.5V



7) COUT Pch. ON Voltage vs. Temperature (at No Load)

R5434D401AA n=1, 2, 3, 4, 5

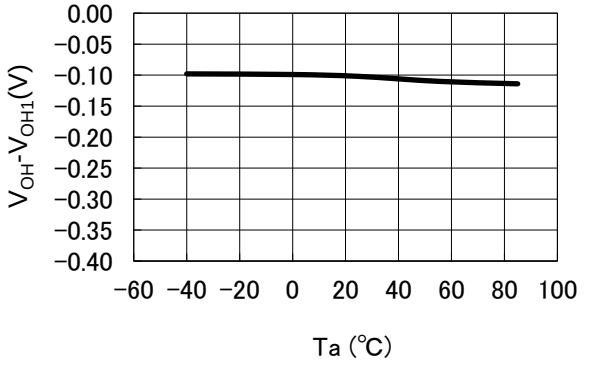
V_{CELLn}=3.5V、I_{LOAD}=0μA



8) COUT Pch. ON Voltage vs. Temperature

R5434D401AA n=1, 2, 3, 4, 5

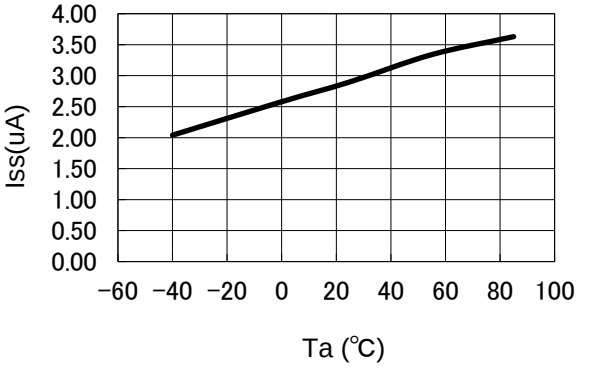
V_{CELLn}=3.5V、I_{LOAD}=-50μA



9) Supply Current vs. Temperature

R5434D401AA n=1, 2, 3, 4, 5

V_{CELLn}=3.9V

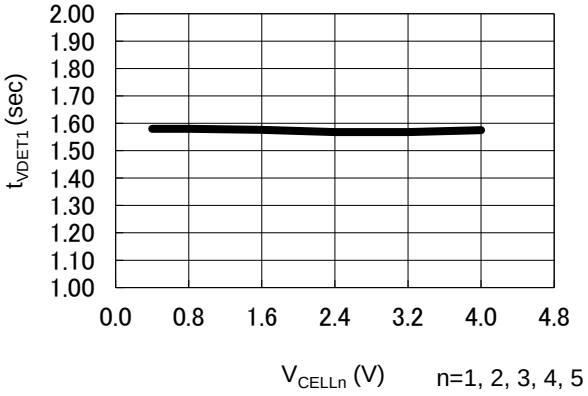


Output Delay Time vs. Supply Voltage (V_{DD}) Dependence

1) Overcharge Detection Delay Time vs. V_{DD}

R5434D401AA

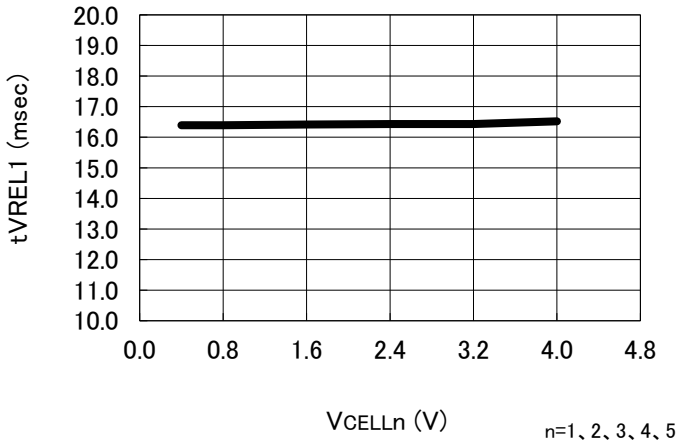
V_{CELL1}=0.4V, 1.6V, 2.4V, 3.2V,4.0V→4.5V



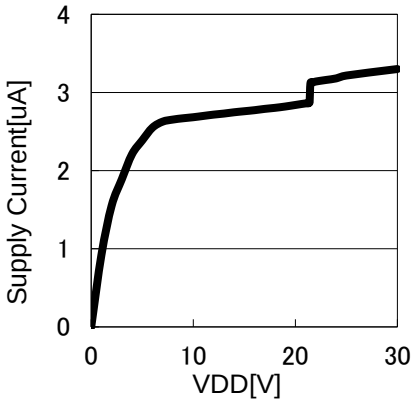
2) Overcharge Release Delay Time vs. V_{DD}

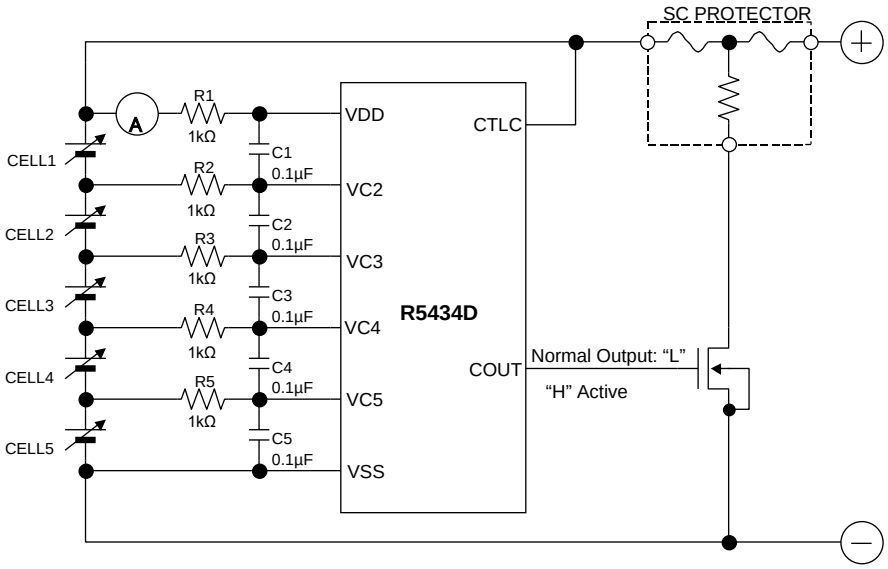
R5434D401AA

VCELL1=0.4V、1.6V、2.4、3.2V、4.0V→4.5V



Supply Current vs. V_{DD} (for 5 Cells Protection)

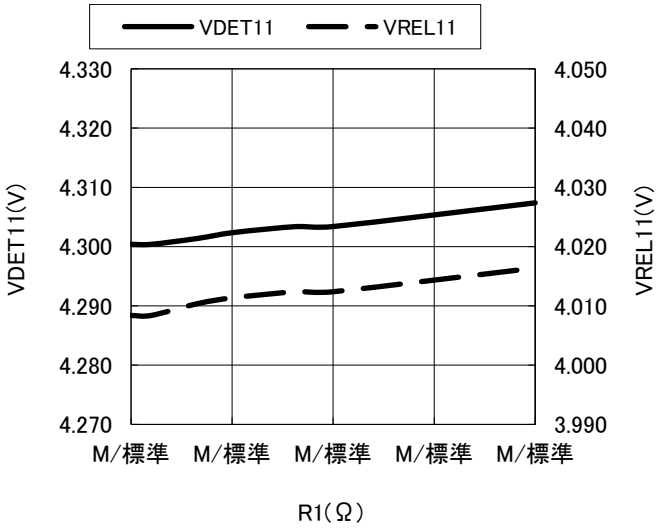


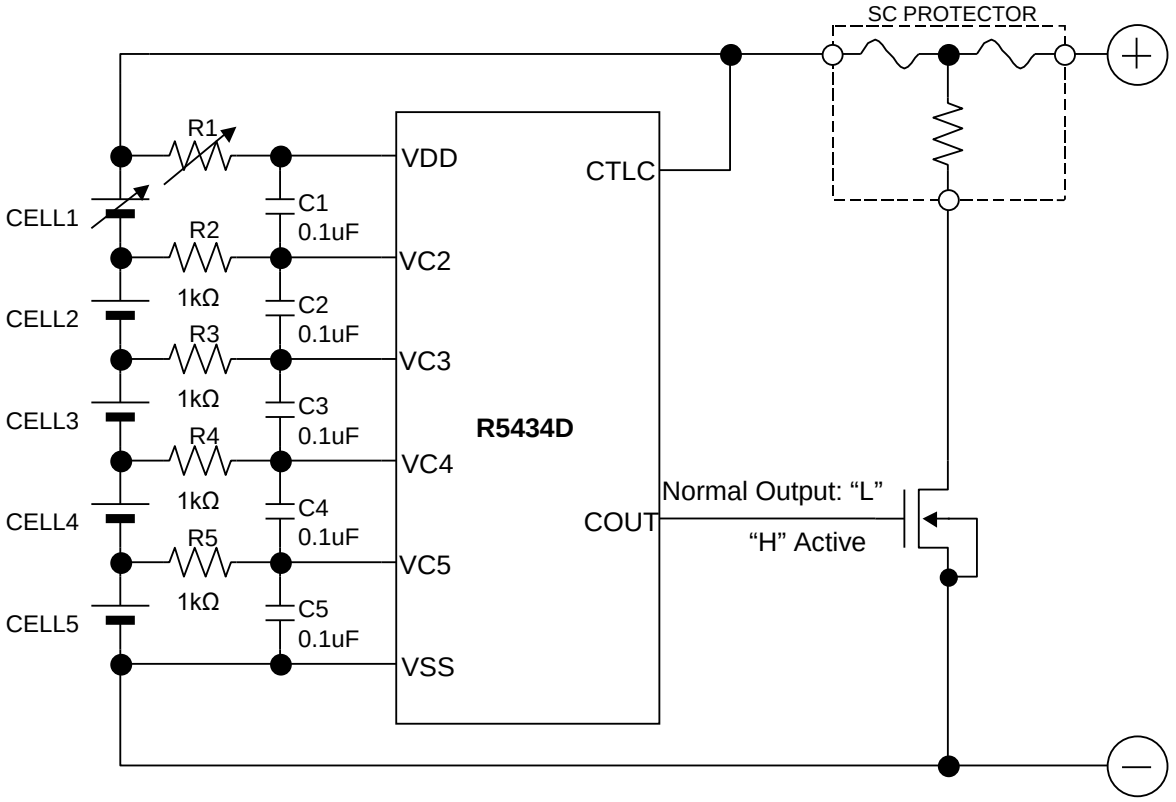


Test Circuit

Vs. External Resister dependence

Overcharge Detection Voltage / Overcharge Release Voltage vs. R1





Test Circuit

Ver. A

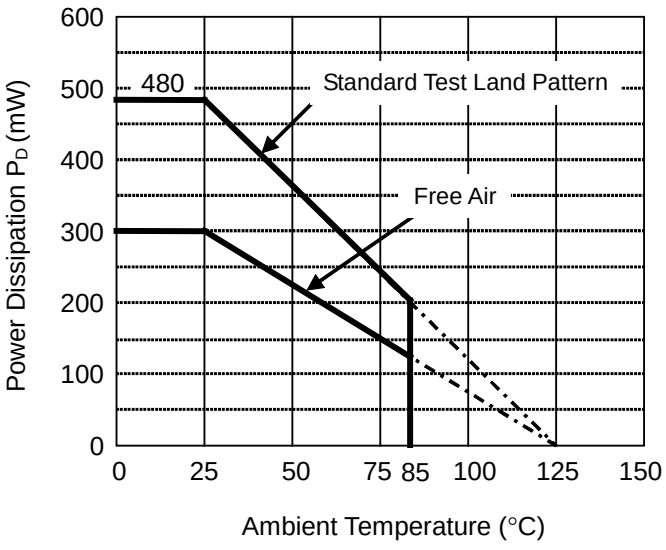
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

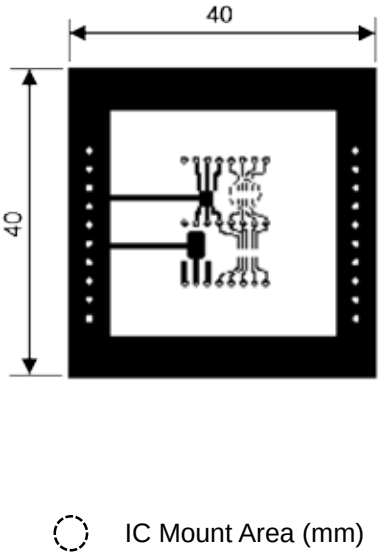
	Standard Test Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-Sided Board)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top Side: Approx. 50% Bottom Side: Approx. 50%
Through-holes	f 0.5 mm × 44 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Test Land Pattern	Free Air
Power Dissipation	480 mW	300 mW
Thermal Resistance	qja = (125 − 25°C) / 0.48 W = 208°C/W	333℃/W



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

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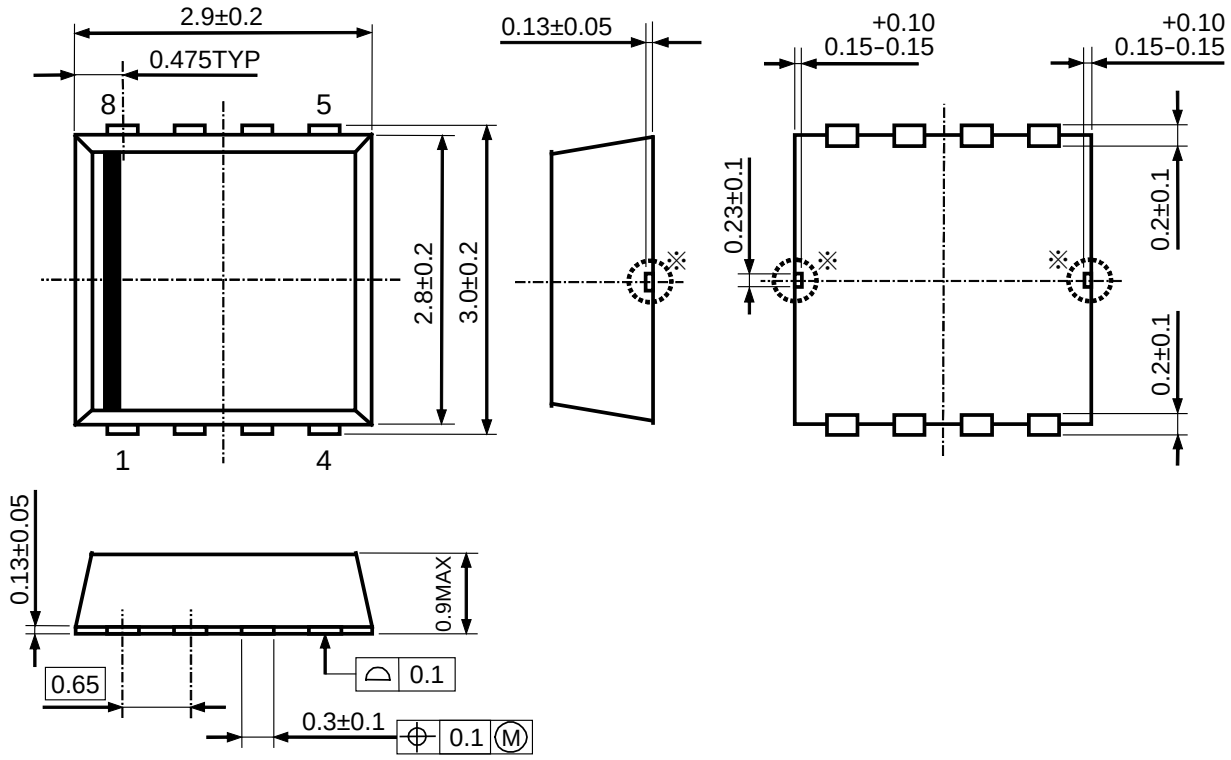
Ver. A



SON-8-18 Package Dimensions (Unit: mm)

* The tab suspension leads on the bottom of the package is substrate level (GND). It is recommended that the tab suspension leads be connected to the ground plane on the board, or otherwise be left floating. Also, the tab suspension leads should not connect to other wires or land patterns.

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