

## 1 to 3 Cells Li-Ion Battery Protection IC for Secondary Protection

No. EA-417-210518

### OUTLINE

The R5438L is an overcharge protection IC for 1 to 3 serial cells Li-ion / Li-polymer rechargeable battery. This device provides the high-accuracy voltage detection function and the shutdown function can reduce the supply current to the minimum when all cell's voltage becomes less than the shutdown detection voltage.

### FEATURES

- High Voltage Tolerant Process  
Absolute Maximum Ratings ..... 26 V
- Low Supply Current  
During Operation, Cell-voltage: 3.9 V, 3-Cells ..... Typ. 0.85  $\mu$ A
- High-accuracy Voltage Detection  
Overcharge Detector Threshold ( $V_{DET1n}^{(1)}$ ) ..... 4.10 V to 4.65 V, in 5 mV step  
Overcharge Detector Threshold Accuracy .....  $\pm 0.02$  V ( $T_a = 25^\circ\text{C}$ )  
 $\pm 0.025$  V ( $0^\circ\text{C} \leq T_a \leq 60^\circ\text{C}$ )  
  
Overcharge Release Voltage ( $V_{REL1n}^{(1)}$ ) .....  $V_{DET1n} - 0\text{V}$  to  $V_{DET1n} - 0.5\text{V}$ , in 50 mV step  
  
Overcharge Detection Delay Time ..... 1-, 2-, 4-, or 6-sec with Delay Time Shortening Function<sup>(2)</sup>  
Overcharge Release Voltage Condition ..... Voltage Release Type
- COUT Output (CMOS Output, Active-high) ..... Typ. 4.7 V
- Shutdown Functions  
Shutdown Detector Threshold ..... Typ. 3.5 V  $\pm 0.3$  V  
Shutdown Current ..... Max. 0.1  $\mu$ A
- 1 to 3 Cells Selectable Battery Protection
- Compact Package  
DFN1814-6C ..... 1.4mm x 1.8mm

### APPLICATIONS

- Li-Ion or Li-Polymer Battery Protection

<sup>(1)</sup>  $V_{DET1n}, V_{REL1n}$  : n = 1, 2, 3

<sup>(2)</sup> The delay time can be reduced down to approx. 1/90 by applying a 4 V  $\pm 0.2$  V to the VDD – VC1 pins.

## SELECTION GUIDE

The overcharge and the delay time are user-selectable options.

### Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5438Lxxx\$*-TR	DFN1814-6C	5,000 pcs	Yes	Yes

xxx: Specify the combination of the overcharge detector threshold ( $V_{DET1n}$ ) and the overcharge release voltage ( $V_{REL1n}$ )<sup>(1)</sup>.

$V_{DET1n}$ <sup>(2)</sup>: 4.10 V to 4.65 V in 5 mV step

$V_{REL1n}$ <sup>(2)</sup>:  $V_{DET1n} - 0$  V to  $V_{DET1n} - 0.5$  V in 50 mV step

\$: Specify the combination of the overcharge detection delay time ( $t_{VDET1}$ ) and the overcharge release delay time ( $t_{VREL1}$ ). Refer to *Delay Time Code Table* for details.

**Delay Time Code Table**

Code	$t_{VDET1}$ (s)	$t_{VREL1}$ (ms)
A	2	16
B	4	16
C	6	16
D	1	16

\*: Specify the function code.

**Function Code Table**

Code	Overcharge Released Condition	COUT Output	
A	Voltage Release	CMOS	"H" Active

<sup>(1)</sup> Refer to *Product Code Table* for details.

<sup>(2)</sup>  $V_{DET1n}, V_{REL1n}$ :  $n = 1, 2, 3$

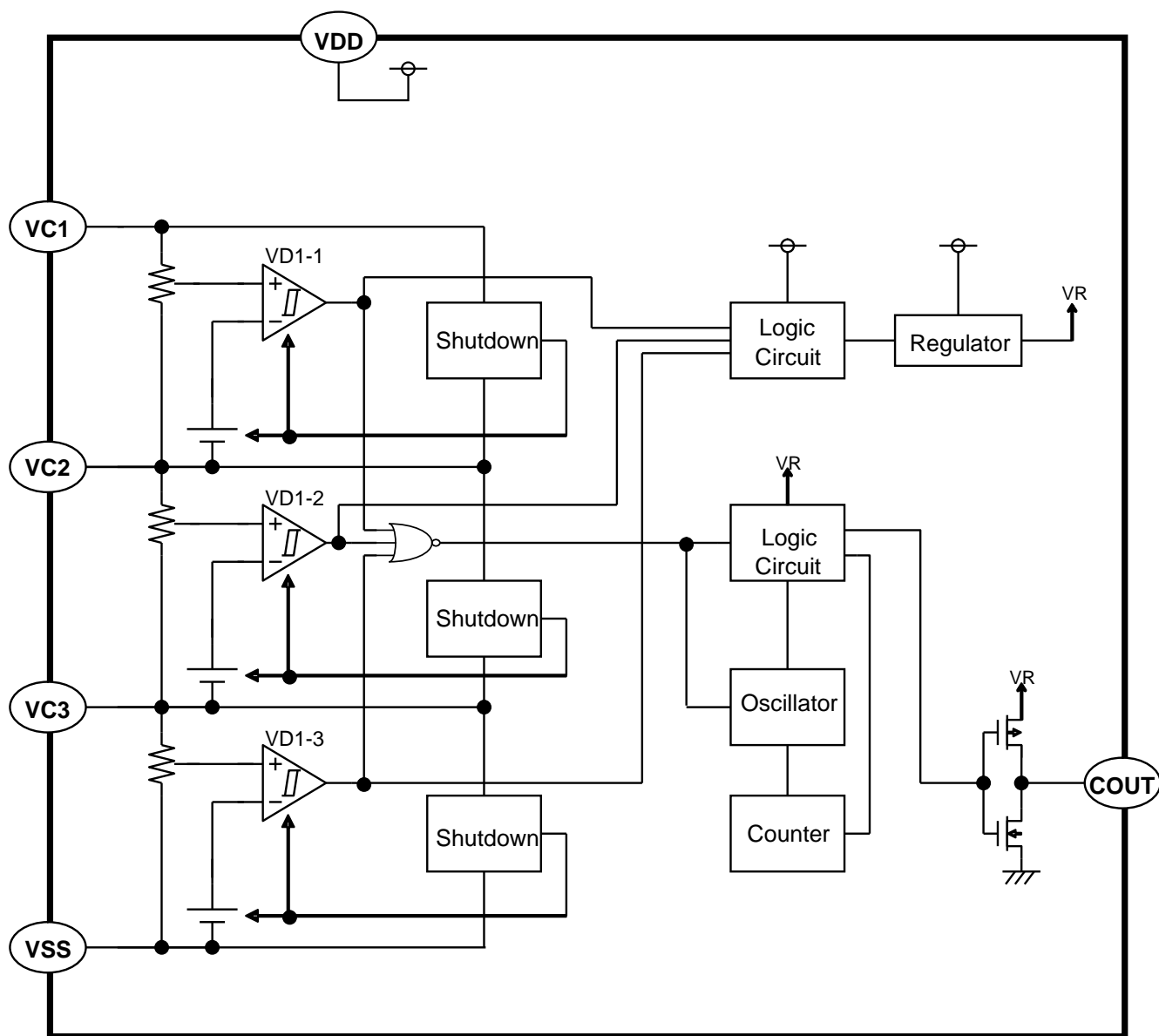
**Product Code List**

The product code is determined by the combination of the settable voltage (overcharge detector threshold:  $V_{DET1n}$  and overcharge release voltage:  $V_{REL1n}$ ) and the delay time (overcharge detection delay time:  $t_{VDET1}$  and overcharge release delay time:  $t_{VREL1}$ ) and the function code.

**Product Code Table**

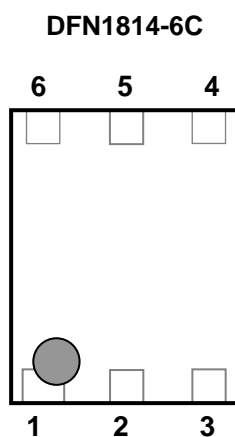
Product Name	Settable Voltage (V)		Delay Time	
	$V_{DET1n}$	$V_{REL1n}$	$t_{VDET1}(s)$	$t_{VREL1}(ms)$
R5438L301AA	4.450	4.150	2	16
R5438L301BA	4.450	4.150	4	16
R5438L303AA	4.350	4.050	2	16
R5438L303BA	4.350	4.050	4	16
R5438L304AA	4.400	4.100	2	16
R5438L304BA	4.400	4.100	4	16
R5438L305AA	4.300	4.000	2	16
R5438L305BA	4.300	4.000	4	16
R5438L306CA	4.450	3.950	6	16
R5438L308BA	4.400	4.000	4	16
R5438L312AA	4.550	4.150	2	16
R5438L312BA	4.550	4.150	4	16
R5438L315AA	4.500	4.150	2	16
R5438L317BA	4.500	4.200	4	16
R5438L322BA	4.600	4.150	4	16
R5438L327AA	4.300	4.200	2	16
R5438L328BA	4.600	4.250	4	16
R5438L329BA	4.650	4.300	4	16

### BLOCK DIAGRAM



R5438L Block Diagram

## PIN DESCRIPTIONS



### DFN1814-6C Pin Assignment

Pin No.	Symbol	Description
1	COUT	Overcharge Detection Output Pin
2	VDD	Power Supply Pin
3	VC1	CELL1 Plus Pin
4	VC2	CELL2 Plus Pin
5	VC3	CELL3 Plus Pin
6	VSS	IC Ground Pin

## ABSOLUTE MAXIMUM RATINGS

### Absolute Maximum Ratings

(Ta = 25°C, V<sub>SS</sub> = 0 V)

Symbol	Item	Rating	Unit
V <sub>DD</sub>	Power Supply Voltage	V <sub>C1</sub> -0.3 to V <sub>C1</sub> +6.5	V
		V <sub>C1</sub> -0.3 to 26	V
V <sub>C1</sub>	CELL1 Plus Pin Input Voltage	V <sub>C2</sub> -0.3 to V <sub>C2</sub> +6.5	V
V <sub>C2</sub>	CELL2 Plus Pin Input Voltage	V <sub>C3</sub> -0.3 to V <sub>C3</sub> +6.5	V
V <sub>C3</sub>	CELL3 Plus Pin Input Voltage	-0.3 to 6.5	V
V <sub>COU</sub> T	COU T Pin Output Voltage	-0.3 to V <sub>OH1</sub> +0.3	V
P <sub>D</sub>	Power Dissipation (Standard Land Pattern)	150	mW
T <sub>j</sub>	Junction Temperature Range	-40 to 125	°C
T <sub>stg</sub>	Storage Temperature Range	-55 to 125	°C

### ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

## RECOMMENDED OPERATING CONDITION

Symbol	Item	Rating	Unit
V <sub>DD</sub>	Operating Input Voltage	1.5 to 20 /	V
		V <sub>C1</sub> +5 V	
T <sub>a</sub>	Operating Temperature Range	-40 to 85	°C

### RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

## ELECTRICAL CHARACTERISTICS

$V_{CELLn} = CELLn$  (Ex.  $V_{CELL1}$  is a voltage difference between VC1 and VC2)

$n = 1, 2, 3$ , unless otherwise noted

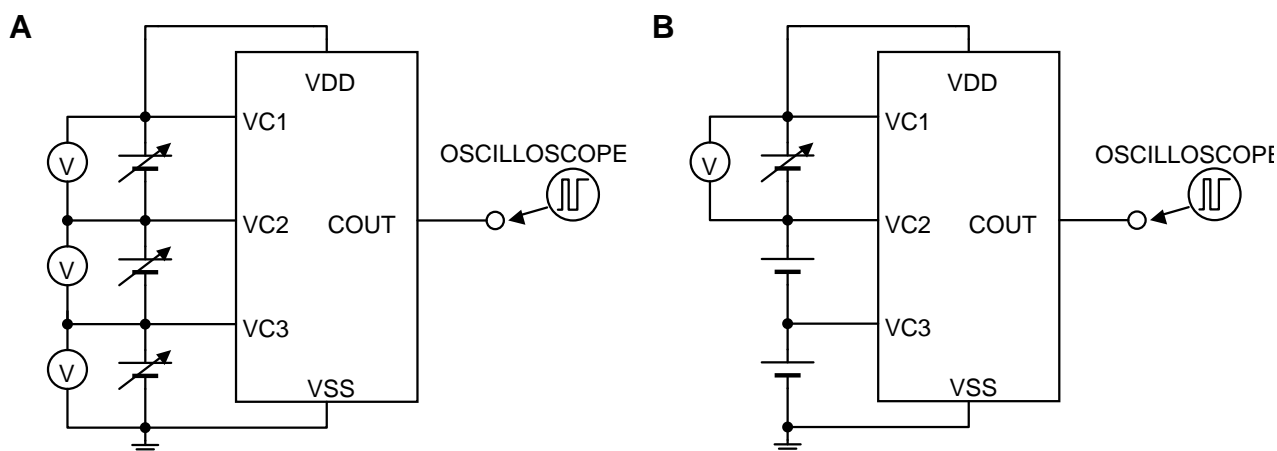
The specifications surrounded by   are guaranteed by Design Engineering at  $0^{\circ}\text{C} \leq T_a \leq 60^{\circ}\text{C}$ .

### R5438L Electrical Characteristics

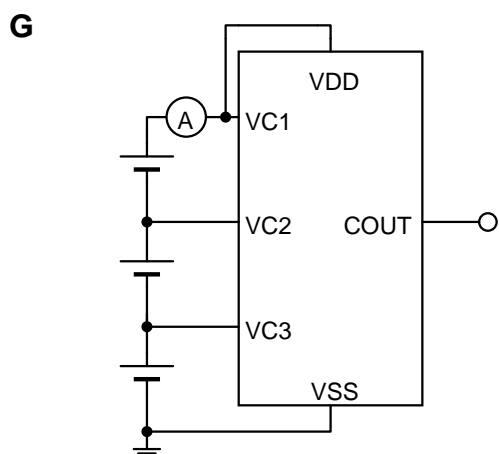
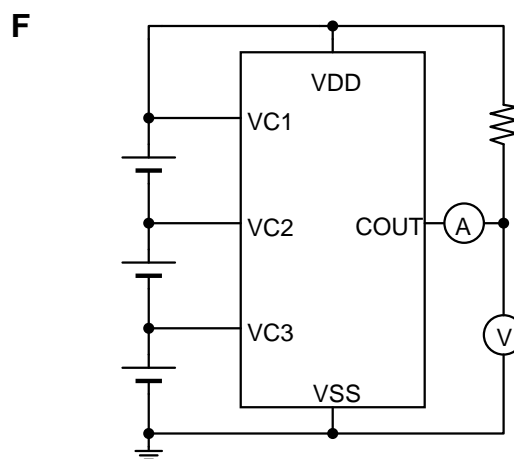
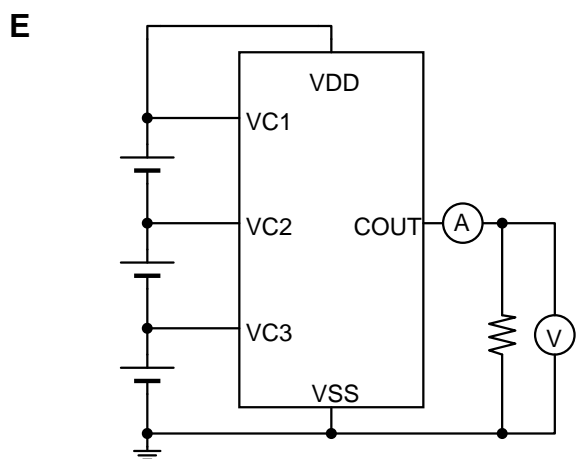
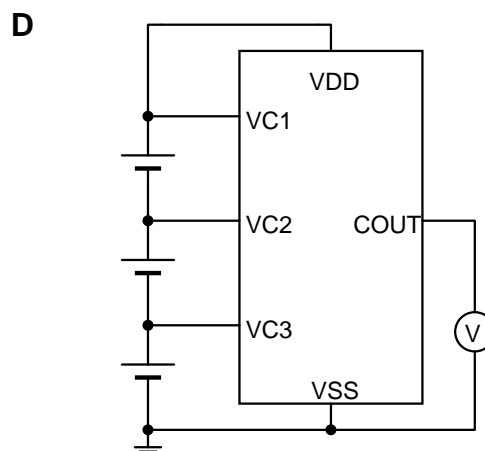
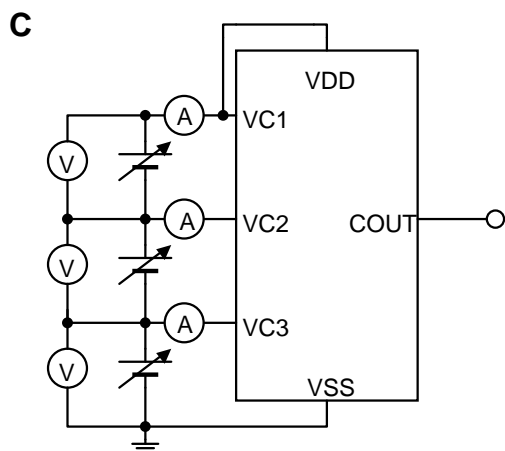
( $T_a = 25^{\circ}\text{C}$ )

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Circuit (1)
$V_{DET1n}$	CELLn Overcharge Detection Voltage	Detect rising edge of supply voltage	$V_{DET1n}$	$V_{DET1n}$	$V_{DET1n}$	V	A
			<span style="border: 1px solid black; padding: 0 2px;"><math>V_{DET1n}</math></span> -0.020V		<span style="border: 1px solid black; padding: 0 2px;"><math>V_{DET1n}</math></span> +0.020V		
$V_{REL1n}$	CELLn Overcharge Release Voltage	Detect falling edge of supply voltage	$V_{REL1n}$	$V_{REL1n}$	$V_{REL1n}$	V	A
			<span style="border: 1px solid black; padding: 0 2px;"><math>V_{REL1n}</math></span> -0.050V		<span style="border: 1px solid black; padding: 0 2px;"><math>V_{REL1n}</math></span> +0.050V		
$t_{VDET1}$	Overcharge Detection Delay Time	$V_{CELLn}=3.9\text{ V}$ ( $n=2,3$ ) $V_{CELL1}=3.9\text{ V} \rightarrow 4.7\text{ V}$	$t_{VDET1}$ x 0.8	$t_{VDET1}$	$t_{VDET1}$ x 1.2	s	B
$t_{VREL1}$	Overcharge Release Delay Time	$V_{CELLn}=3.9\text{ V}$ ( $n=2,3$ ) $V_{CELL1}=4.7\text{ V} \rightarrow 3.9\text{ V}$	12.8	16	19.2	ms	B
$V_{SHT}$	Shutdown Detection Voltage	Detect falling edge of supply voltage	3.2	3.5	3.8	V	C
$V_{OH1}$	$C_{OUT}$ Pch. ON Voltage 1	$I_{OH}=0\mu\text{A}, V_{CELLn} = 4.7\text{ V}$	4.0	4.7	5.4	V	D
		$I_{OH}=0\mu\text{A}, V_{CELLn} = 4.7\text{ V}$ ( $n=1$ , at 1 cell protection)		$V_{DD}$			
$V_{OH2}$	$C_{OUT}$ Pch. ON Voltage 2	$I_{OH} = -50\mu\text{A},$ $V_{CELLn} = 4.7\text{V}$	$V_{OH1}$ -0.5V	$V_{OH1}-0.1\text{V}$		V	E
$V_{OL}$	$C_{OUT}$ Nch. ON Voltage	$I_{OL}=50\mu\text{A}, V_{CELLn}=3.9\text{ V}$		0.1	0.5	V	F
$I_{SHT}$	Shutdown Current	$V_{CELLn} = 3.1\text{ V}$			0.1	$\mu\text{A}$	G
$I_{SS}$	Supply Current	$V_{CELLn} = 3.9\text{ V}$		0.85	1.7	$\mu\text{A}$	G

### TEST CIRCUITS



(1) Refer to TEST CIRCUITS for detail information.





## THEORY OF OPERATION

### Overcharge Detection Circuit, VD1-n (n = 1, 2, 3)

(See the following timing chart)

While the cells are charged, the voltage between VC1 pin and VC2 pin (Cell-1 voltage), the voltage between VC2 pin and VC3 pin (Cell-2 voltage), and the voltage between VC3 pin and VSS pin (Cell-3 voltage) are supervised. If at least one of the cells' voltage becomes equal or more than the overcharge detector threshold, the overcharge is detected, and an external charge control Nch. FET turns on with COUT pin being at "H" level and by cutting a fuse on the charger path, and charge stops.

To reset the overcharge and make the COUT pin level to "L" again after detecting over-charge, in such conditions that a time when all the cells' voltages are down to a level lower than overcharge released voltage. Internal fixed output delay times for overcharge detection and release from over-charge exist. Even if one of voltage of the cells keeps its level more than the overcharge detector threshold, and output delay time passes, overcharge voltage is detected. After detecting overcharge, even if all the cell voltages become equal or less than the released voltage from overcharge, if at least one of the cells voltage becomes higher than the released voltage from overcharge within the output delay time of the release from overcharge, then overcharge is not released.

The output type of the COUT pin is CMOS output between VSS and the built-in regulator, and "H" level of COUT pin is the output voltage of the built-in regulator.

### Shutdown Function

The voltage between VC1 pin and VC2 pin (Cell-1 voltage), the voltage between VC2 pin and VC3 pin (Cell-2 voltage), and the voltage between VC3 pin and VSS pin (Cell-3 voltage) are supervised. If the cell voltage becomes equal or less than the shutdown detector threshold, the overcharge detector of the cell is halted, as a result, the consumption current of IC itself (Shutdown current) is extremely reduced. If at least one of the cells voltage becomes higher than the shutdown detection voltage, the shutdown detection is released.

### Delay Shortening (DS) Function

Applying a voltage of  $4\text{ V} \pm 0.2\text{ V}$  between VDD and VC1 can shorten the overcharge detection delay time ( $t_{\text{VDET1}}$ ) into approximately 1/90, likewise, the overcharge release delay time ( $t_{\text{VREL1}}$ ) into approximately 1/60.

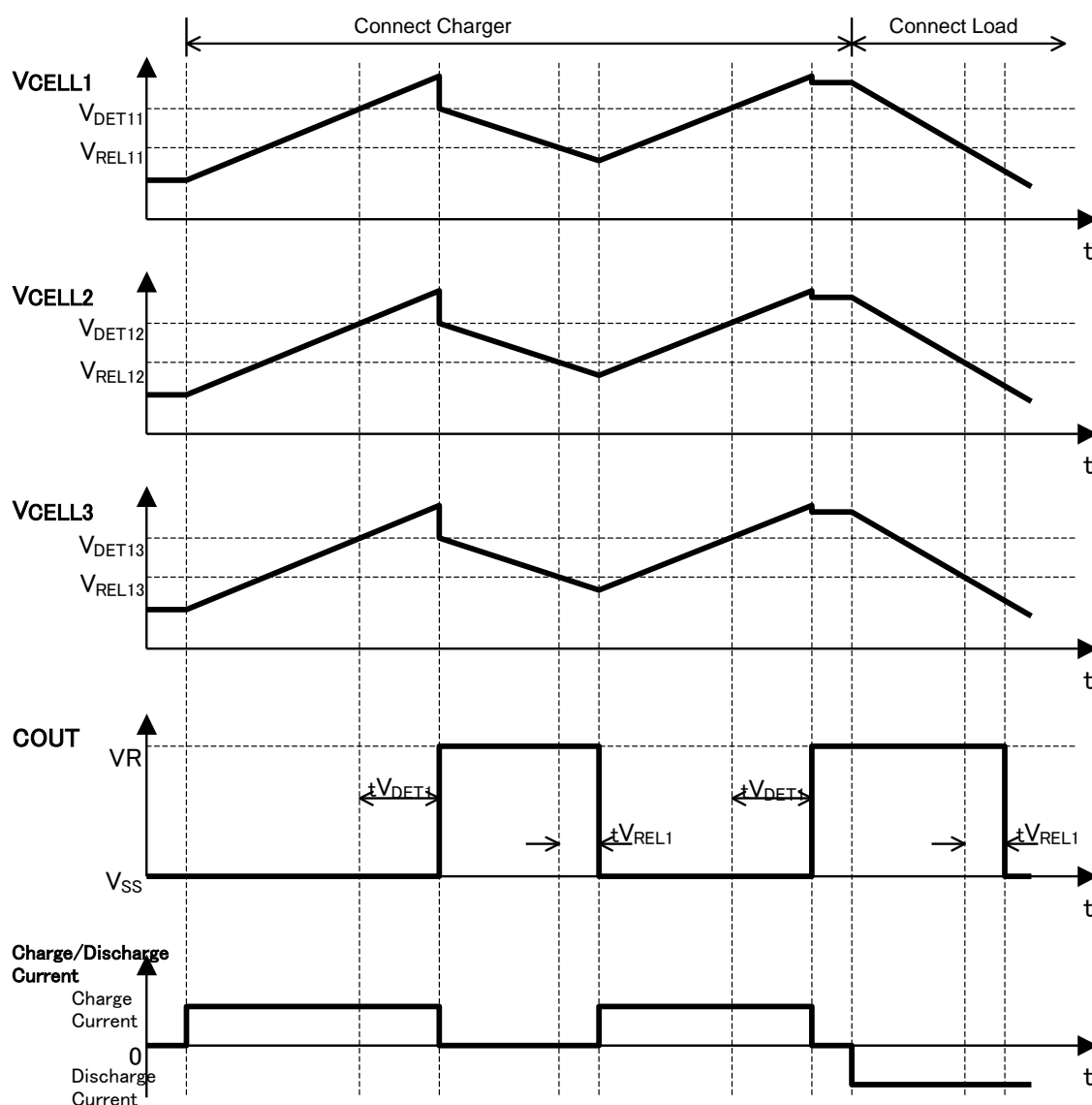
### 1-cell/ 2-cell Protection Alternative

By short-circuiting between cells, this device can meet as a protection IC for 1 or 3 cells placed in series.

The following table indicates pins to short-circuit depending on protected cells.

Protected Cells	Pins to short-circuit
1-cell protection	VC1 and VC2 pins, and VC3 and VSS pins
2-cell protection	VC1 and VC2 pins, or VC3 and VSS pins

If providing other connections except above short-circuit for 1 or 2 cells protection, perform thorough evaluation using the actual devices.

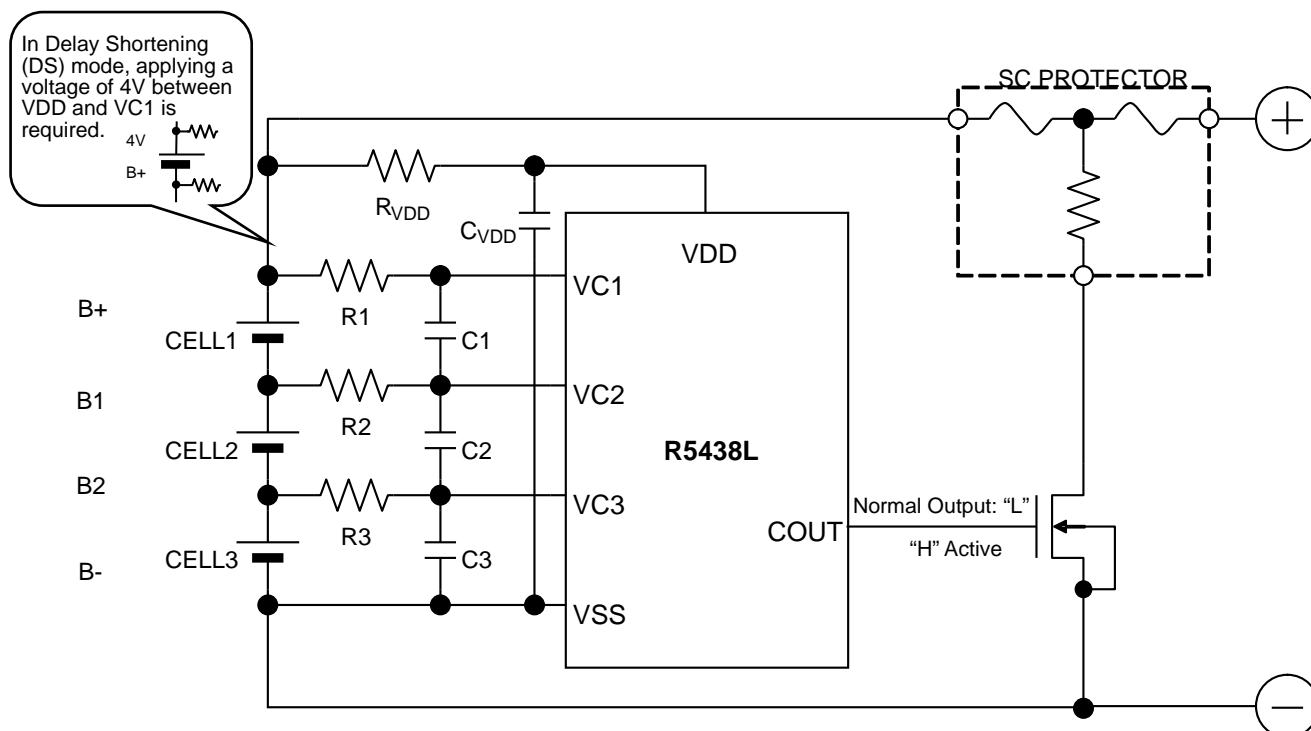


Overcharge Operation Timing Chart

## APPLICATION INFORMATION

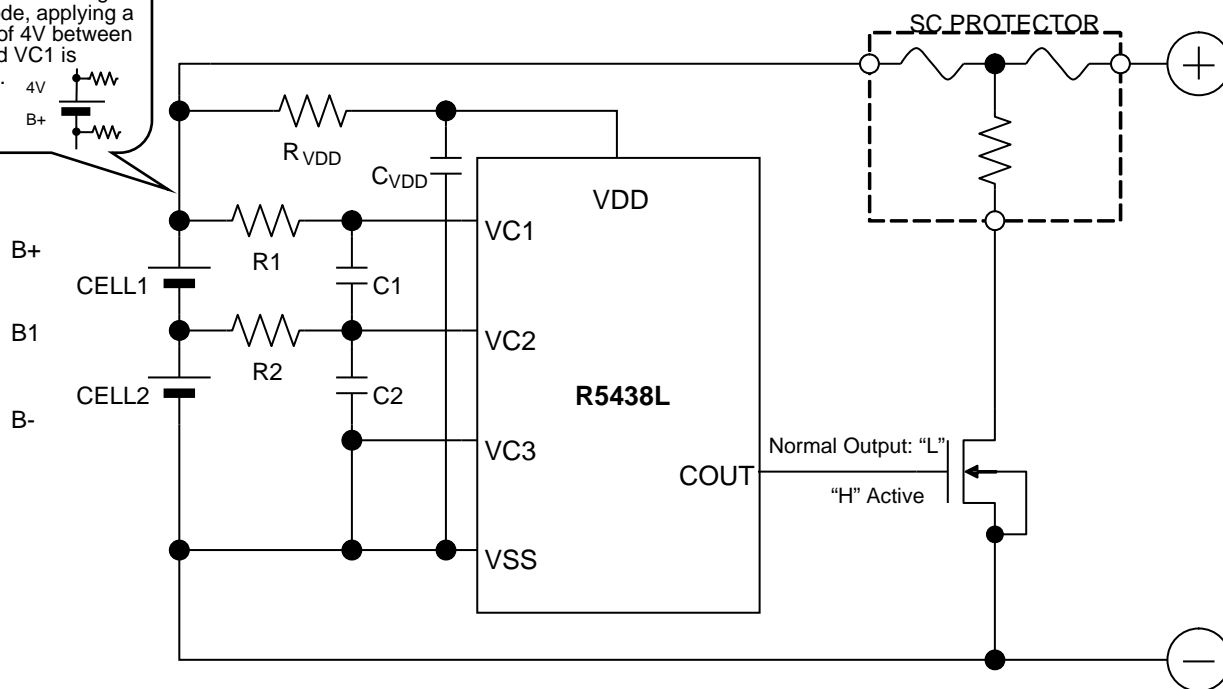
### Typical Application Circuits in Normal Mode (CMOS Output, Active-high)

As for the order of cell's connection, connect a positive terminal of CELL1 as the end terminal. If connected another terminal, a fuse blowout might be caused by transiently "High" output of the COUT pin.



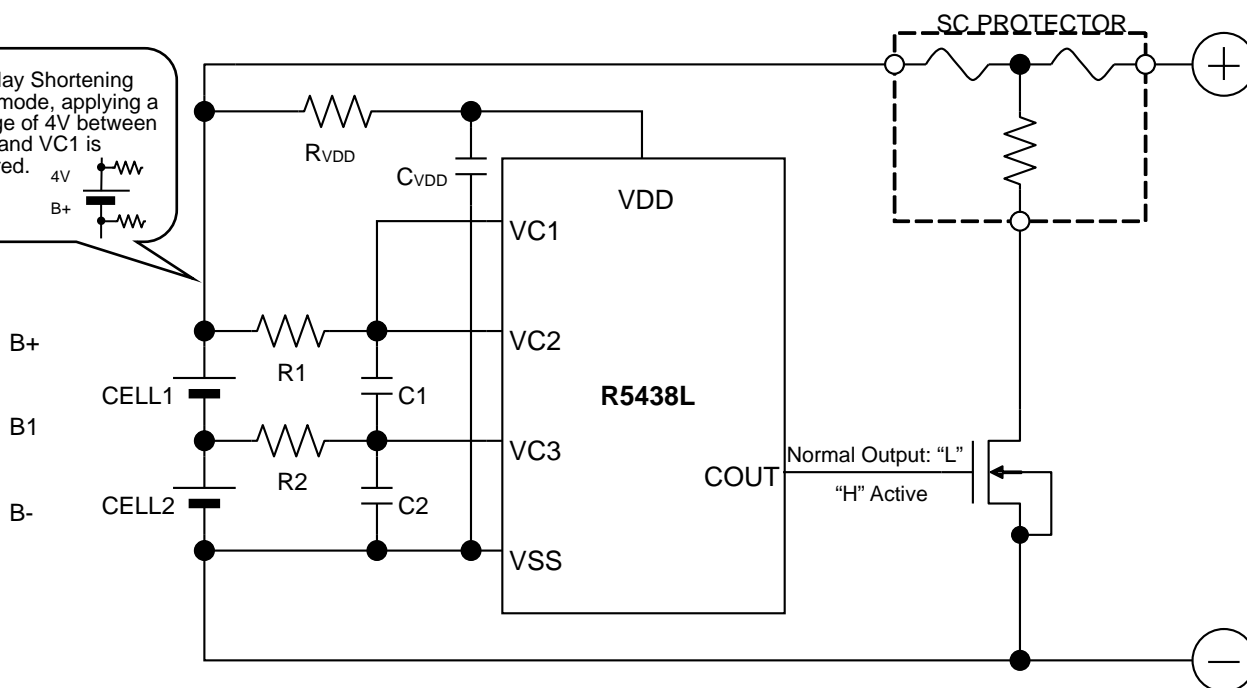
Typical Application Circuit for 3-cell Protection

In Delay Shortening (DS) mode, applying a voltage of 4V between VDD and VC1 is required.

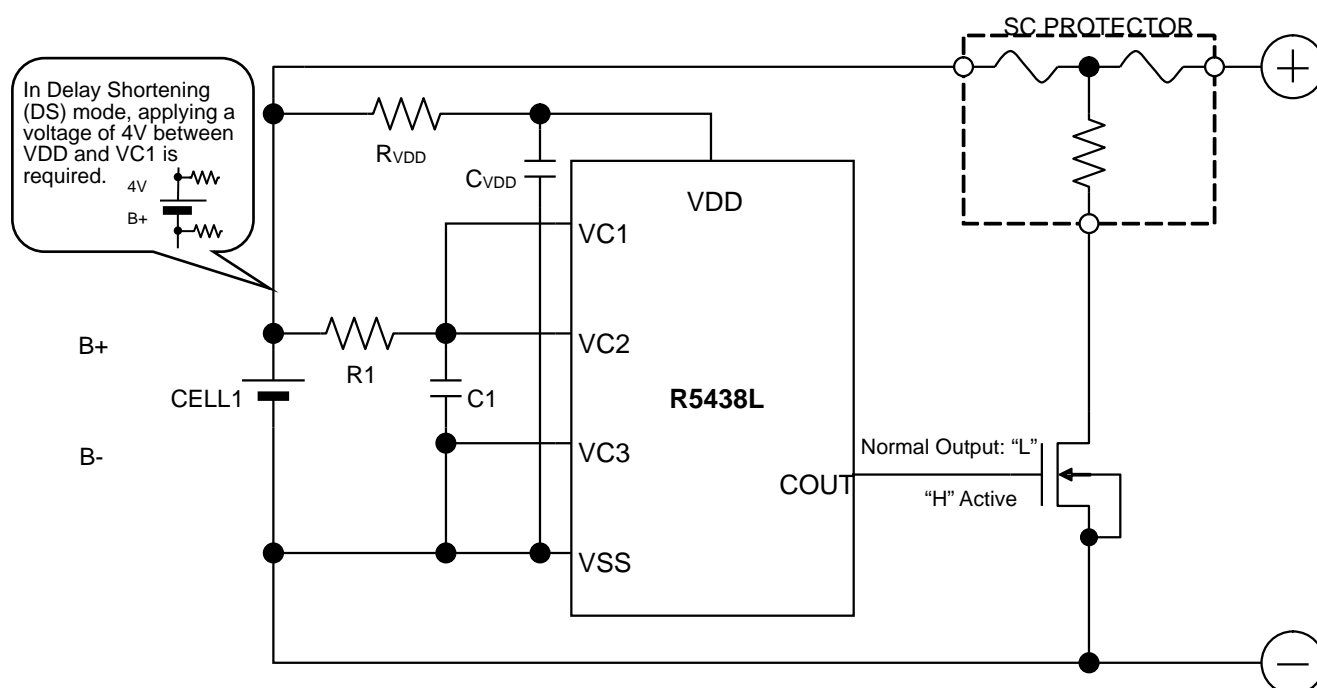


Typical Application Circuit for 2-cell Protection -1

In Delay Shortening (DS) mode, applying a voltage of 4V between VDD and VC1 is required.



Typical Application Circuit for 2-cell Protection -2



Typical Application Circuit for 1-cell Protection

## External Components

Symbol	Typ.	Unit	Range
R <sub>vDD</sub>	100	Ω	100 to 1000
R <sub>1</sub>	1000	Ω	330 to 1000
R <sub>2</sub>	1000	Ω	330 to 1000
R <sub>3</sub>	1000	Ω	330 to 1000
C <sub>vDD</sub>	0.1	μF	0.01 to 1
C <sub>1</sub>	0.1	μF	0.01 to 1
C <sub>2</sub>	0.1	μF	0.01 to 1
C <sub>3</sub>	0.1	μF	0.01 to 1

**Technical Notes on the Selection Components**

- The voltage fluctuation is stabilized with  $R_{VDD}$  and  $C_{VDD}$ . If a small  $R_{VDD}$  is set, in the case of the large transient may happen to the cell voltage, by the flowing current, the IC may be unstable. If a large  $R_{VDD}$  is set, by the consumption current of the IC itself, the voltage difference between VDD pin and VC1 pin is generated, and unexpected operation may result. Therefore, the appropriate value range of  $R_{VDD}$  is from 100  $\Omega$  to 1 k $\Omega$ . To make a stable operation of the IC, the appropriate value range of  $C_{VDD}$  is from 0.01  $\mu$ F to 1.0  $\mu$ F.
- The voltage fluctuation is stabilized with R1 to R3 and C1 to C3. If a R1 to R3 is too large, by the conduction current at detection, the detector threshold may shift higher. Therefore, the appropriate value range of R1 to R3 is equal or less than 1 k $\Omega$ . To make a stable operation of the IC, the appropriate value range of C1 to C3 is 0.01  $\mu$ F or more.
- The typical application circuit diagrams are just examples. This circuit performance largely depends on the PCB layout and external components. In the actual application, fully evaluation is necessary.
- Overvoltage and the over current beyond the absolute maximum rating should not be forced to the protection IC and external components. During the time until the fuse is open after detecting overcharge, a large current may flow through the FET. Select an FET with large enough current capacity in order to endure the large current.
- To connect the SC protector, connect the SC protector to the cell must be the last.

**Contact Information for Inquiries regarding SC PROTECTOR**

Dexerials Corporation (Sony Chemical & Information Device Company Ltd.)

Gate-city Osaki East Tower 8F, 1-11-2 Osaki, Shinagawa, Tokyo, 141-0032

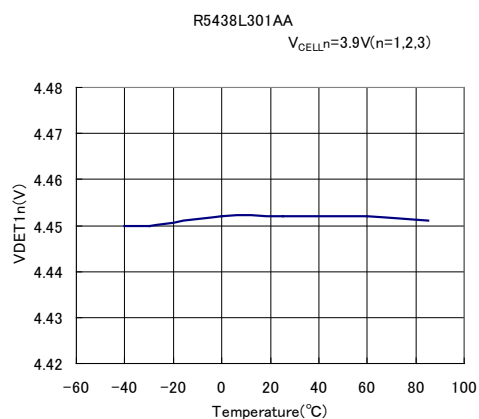
TEL: 03-5435-3946

URL: <http://www.dexerials.jp>

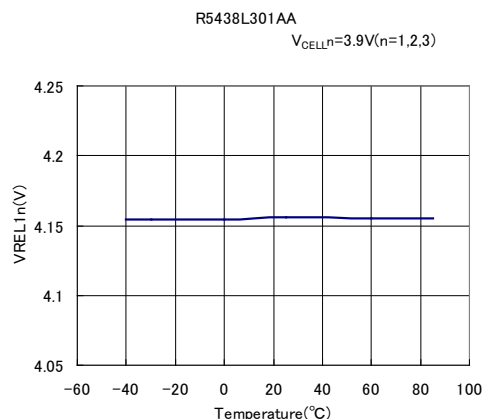
## TYPICAL CHARACTERISTICS

### Part1. vs. Temperature

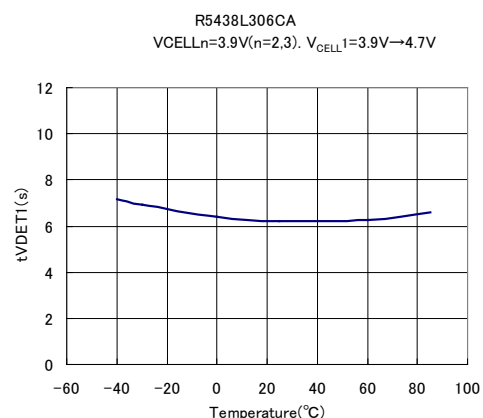
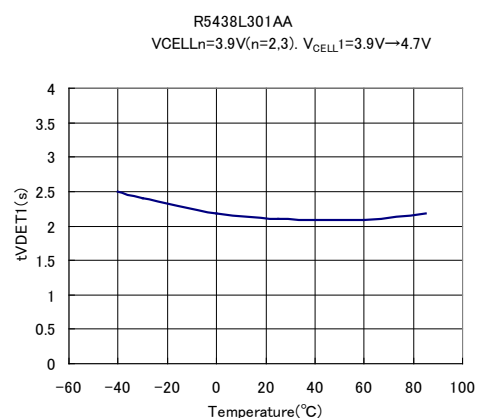
#### 1) Celln Overcharge Detection Threshold vs. Temperature



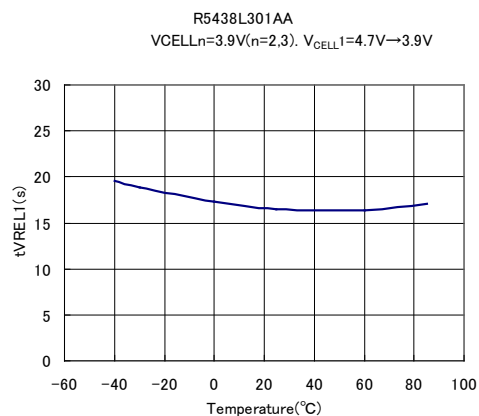
#### 2) Celln Overcharge Release Voltage vs. Temperature



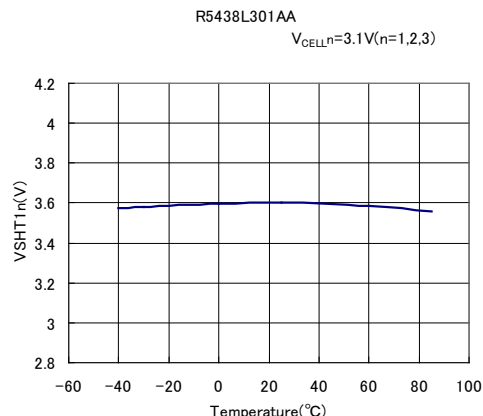
#### 3) Overcharge Output delay Time vs. Temperature



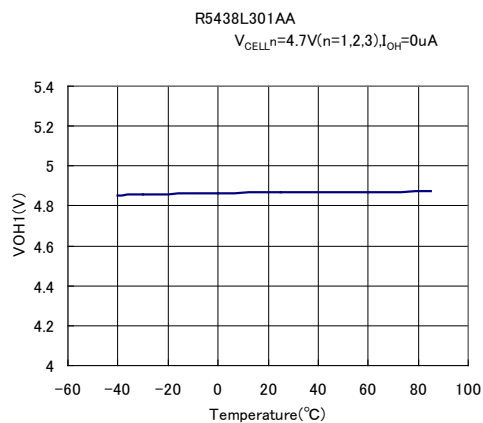
#### 4) Released Delay Time from Overcharge vs. Temperature



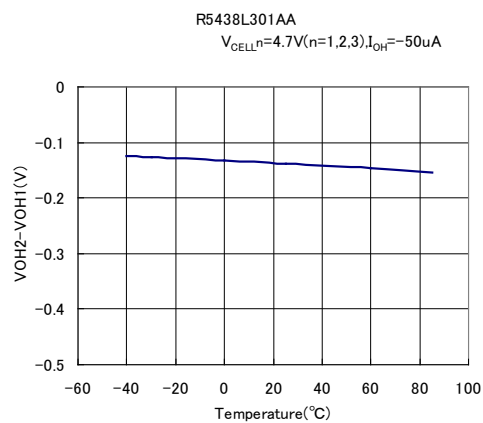
#### 5) Celln Shutdown Threshold vs. Temperature



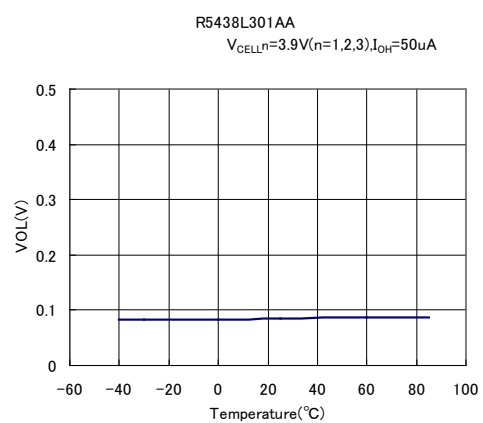
**6) COUT Pch. On Voltage (No Load) vs. Temperature**



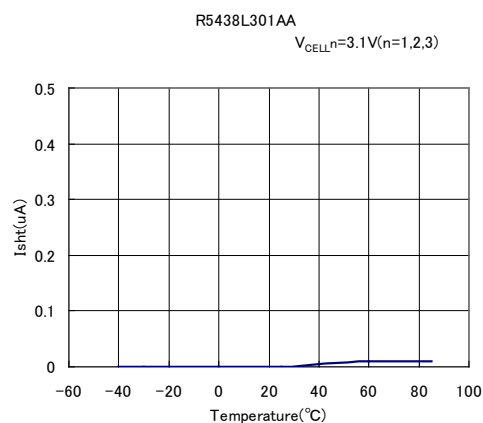
**7) COUT Pch. On Voltage vs. Temperature**



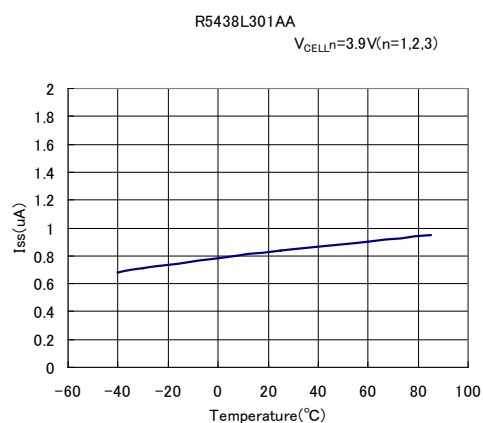
**8) COUT Nch. On Voltage vs. Temperature**



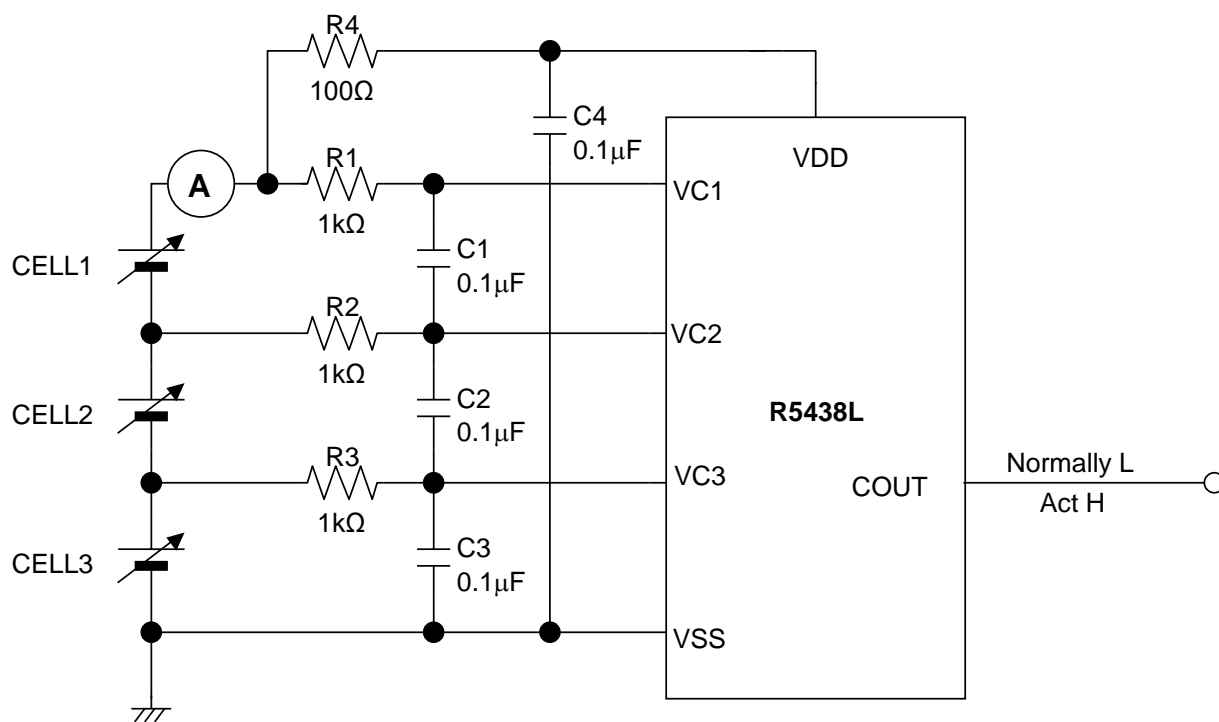
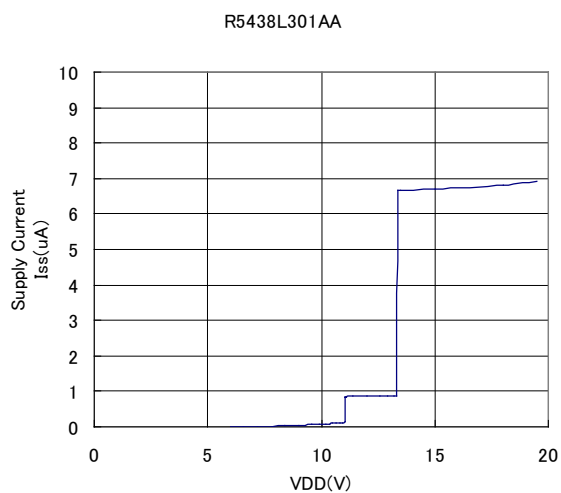
**9) Shutdown Current vs. Temperature**



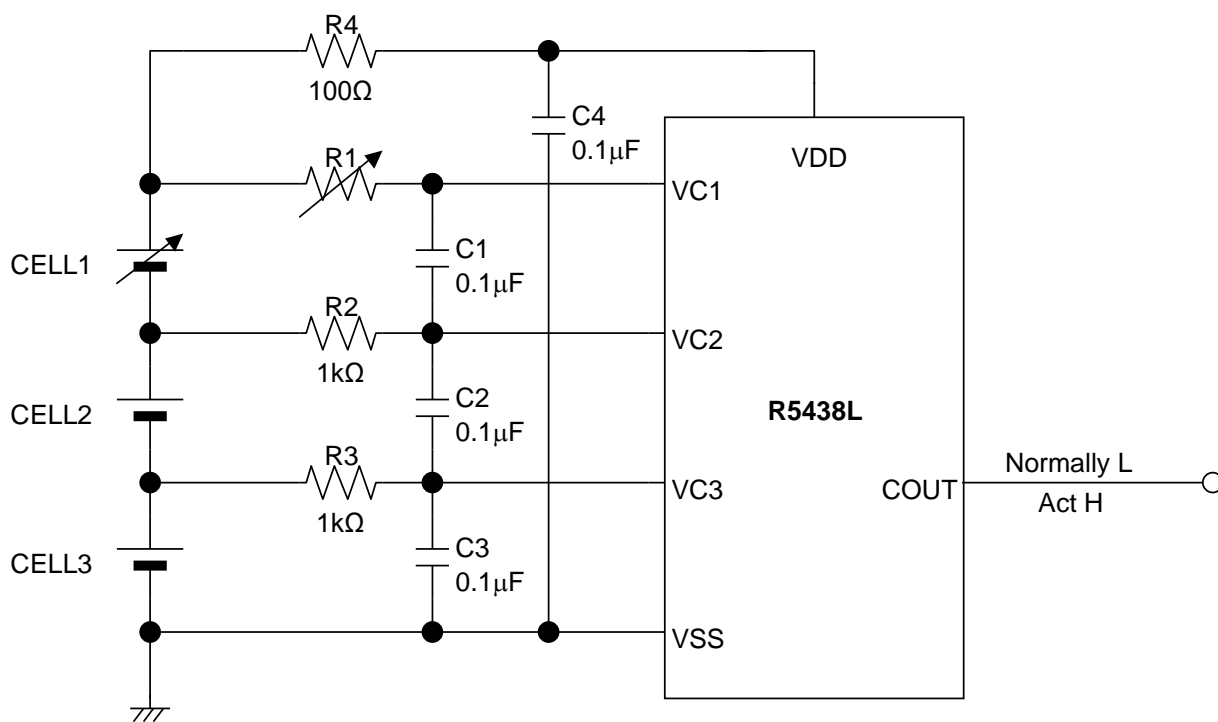
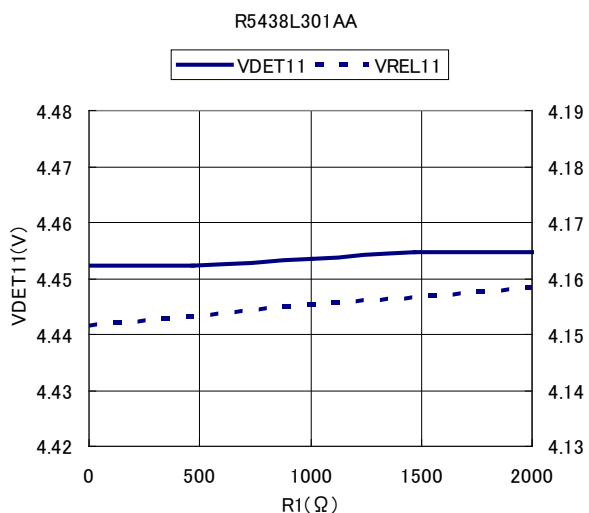
**10) Supply Current vs. Temperature**



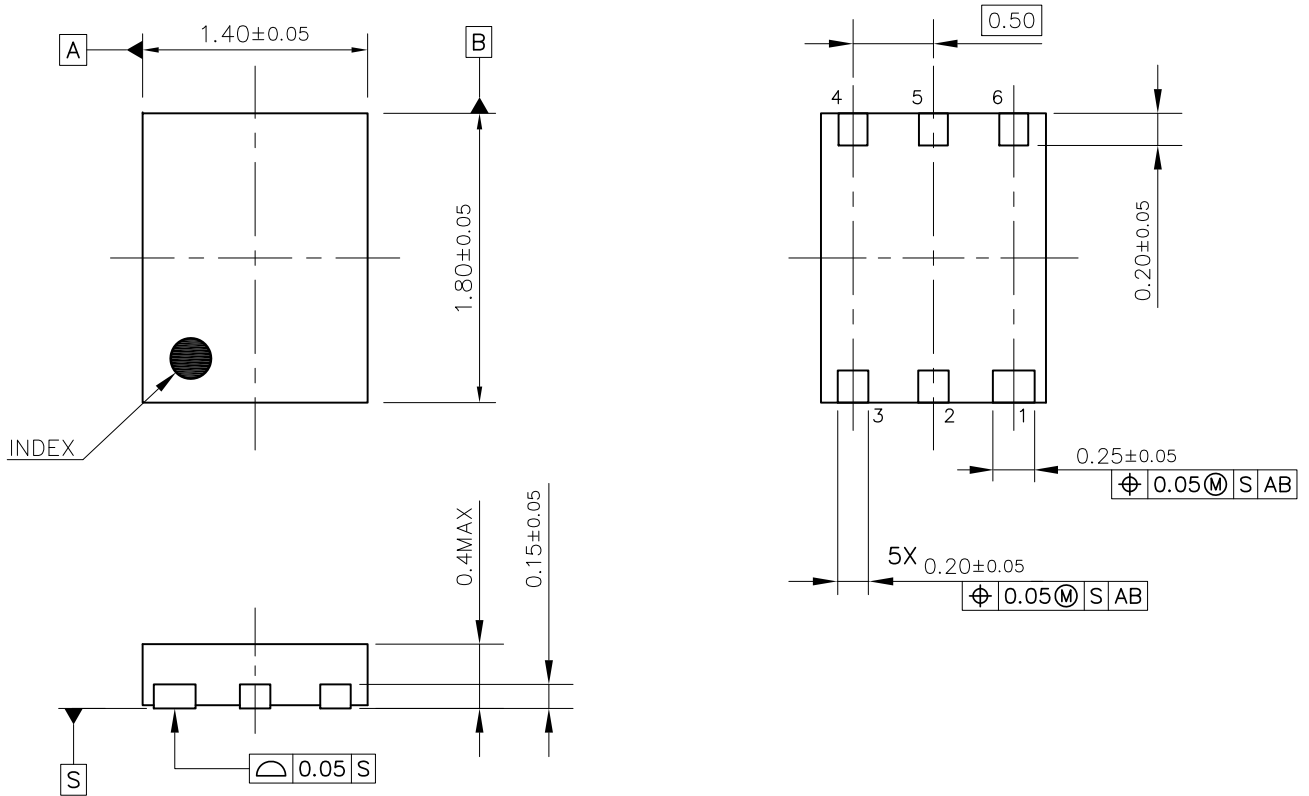


**Part2. Supply Current vs. VDD (R5438L301AA)****3-cell Protection Supply Current vs. VDD**

**Part3. vs. External Resister Dependence (R5438L301AA)**  
**Overcharge Detection Voltage / Overcharge Release Voltage vs. R1**



Test Circuit



DFN1814-6C Package Dimensions (Unit: mm)



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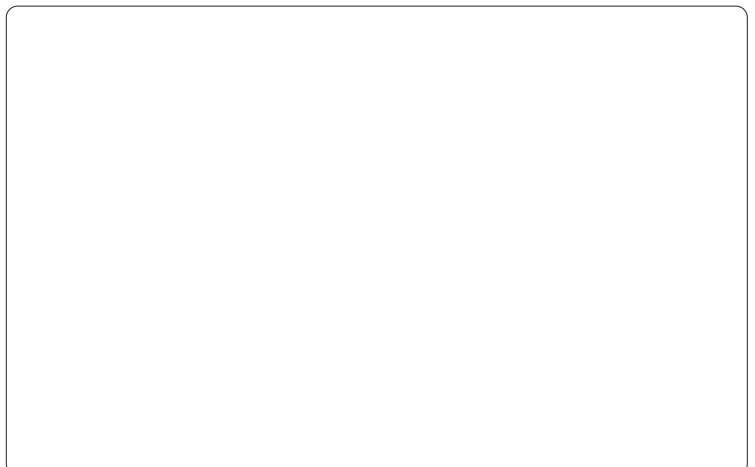
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