

## OUTLINE

The R5475N/R5478Nxxxxx Series are high voltage CMOS-based protection ICs for over-charge/discharge of rechargeable one-cell Lithium-ion (Li+) / Lithium polymer excess load current, further include a short circuit protector for preventing large external short circuit current and Excess discharge-current.

Each of these ICs is composed of three voltage detectors, a reference unit, a delay circuit, a short circuit protector, an oscillator, a counter, and a logic circuit. When the over-charge voltage crosses the detector threshold from a low value to a high value, the output of C<sub>OUT</sub> pin switches to low level after internal fixed delay time. The conditions to release over-charge detector are different by mask options. In terms of so called "Latch function" version, after detecting over-charge, the detector can be reset and the output of C<sub>OUT</sub> becomes "H" when a kind of load is connected to V<sub>DD</sub> after a charger is disconnected from the battery pack, and the cell voltage becomes lower than over-charge detector threshold. If a charger is continue to be connected to the battery pack, even the cell voltage becomes lower than over-charge detector threshold, over-charge state is not released. On the other hand, in terms of so called, "Released by voltage level" version, after detecting over-charge, when the cell voltage reaches the released voltage from over-charge, the output of C<sub>OUT</sub> becomes "H"

The output of D<sub>OUT</sub> pin, the output of Over-discharge detector and Excess discharge-current detector, switches to "L" level after internally fixed delay time, when discharged voltage crosses the detector threshold from a high value to a value lower than V<sub>DET2</sub>.

The conditions to release over-discharge detector are also different by mask options. In terms of so called "Latch function" version, after detecting over-discharge voltage, connect a charger to the battery pack, and when the battery supply voltage becomes higher than over-discharge detector threshold, VD2 is released and the voltage of D<sub>OUT</sub> pin becomes "H" level. On the other hand, in terms of so called "Released by voltage level" version, in case that the charger is not connected, when the cell voltage becomes equal released voltage from over-discharge, over-discharge detector is released. In case that a charger is connected, and when the cell voltage becomes the released voltage from over-discharge, the over-discharge detector is released.

An excess discharge-current and short circuit state can be sensed and cut off through the built in excess current detector, VD3, with D<sub>OUT</sub> being enabled to low level. Once after detecting excess discharge-current or short circuit, the VD3 is released and D<sub>OUT</sub> level switches to high by detaching a battery pack from a load system.

After detecting over-discharge, supply current will be kept extremely low by halting internal circuits' operation.

When the output of C<sub>OUT</sub> is "H", if V- pin level is set at V<sub>ss</sub>-2V, the delay time of detector can be shortened. Especially, the delay time of over-charge detector can be reduced into approximately 1/57. Therefore, testing time of protector circuit board can be reduced. Output type of C<sub>OUT</sub> and D<sub>OUT</sub> are CMOS. 6-pin, SOT-23-6 is available.

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**R5475N/R5478Nxxxxx**

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**FEATURES**

- Manufactured with High Voltage Tolerant Process ...Absolute Maximum Rating 30V
- Low supply current .....Supply current (At normal mode) Typ. 3.0μA
  - C version: (detecting over-discharge) Max. 0.1μA
  - D/J/K version: (detecting over-discharge) Typ. 1.2μA/Max. 2.0μA
- High accuracy detector threshold .....Over-charge detector (Topt=25°C) ±25mV
  - (Topt=-5 to 55°C) ±30mV
  - Over-discharge detector ±2.5%
  - Excess discharge-current detector ±15mV
- Variety of detector threshold .....Over-charge detector threshold
  - C/D version: 4.2V-4.5V step of 0.005V
  - J version: 3.65V
  - K version: 3.90V
  - Over-discharge detector threshold
  - C/D/J version: 2.1V-3.0V step of 0.100V
  - K version: 1.9V-3.0V step of 0.100V
  - Excess discharge-current threshold 0.05V-0.20V step of 0.005V
  - Short Detector Threshold Fixed at 0.75V
- Internal fixed Output delay time.....Over-charge detector Output Delay 1s
  - (Select among the options) Over-discharge detector Output Delay 20ms
  - Excess discharge-current detector Output Delay 12ms(C Type) / 6ms(E Type)
  - Short Circuit detector Output Delay 300μs(C Type) / 200μs(E Type)
- Output Delay Time Shortening Function..At COUT is “H”, if V- level is set at -2V, the Output Delay time of all items except short-circuit can be reduced. (Delay Time for over-charge becomes about 1/57 of normal state.)
- Conditions for release over-charge detector With Latch function (C version)
  - With Released voltage (D/J/K version)
- Conditions for Release over-discharge detector Latch Type: (C version)
  - Released Voltage (D/J/K version)
- Ultra Small package .....SOT-23-5(R5475N) , SOT-23-6(R5478N)

**APPLICATIONS**

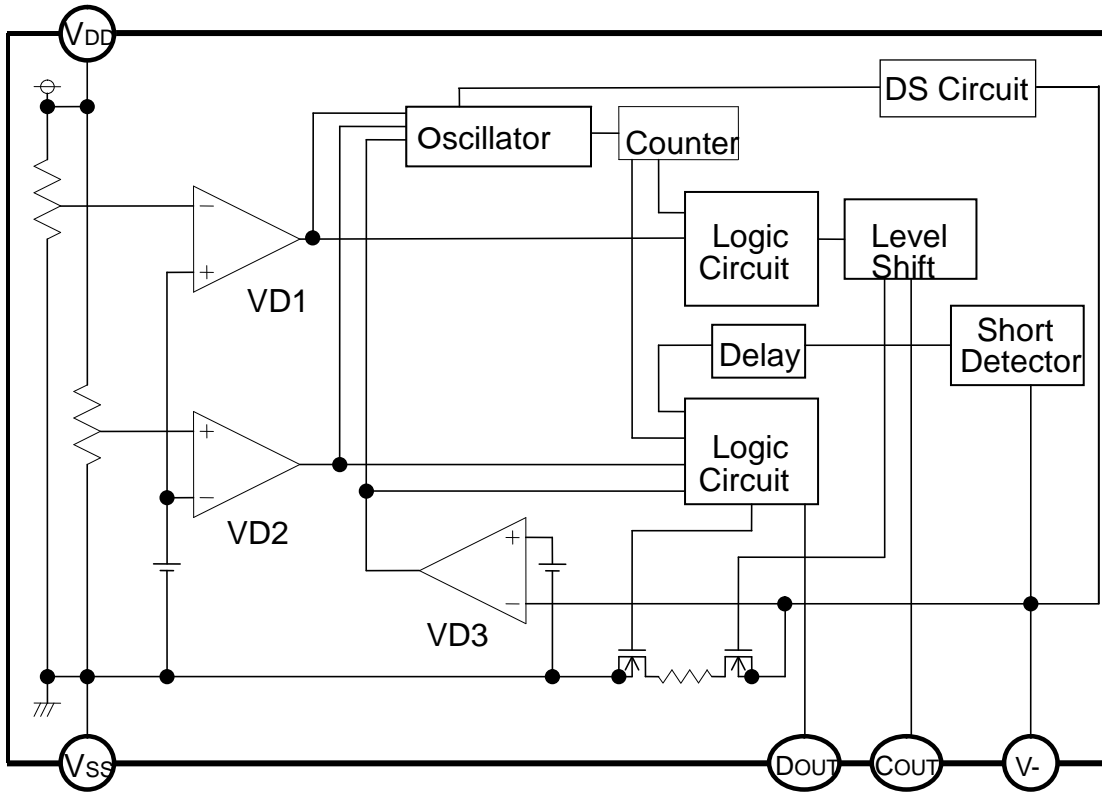
- Li+ / Li Polymer protector of over-charge, over-discharge, excess-current for battery pack
- High precision protectors for cell-phones and any other gadgets using on board Li+ / Li Polymer battery

\* R5475N (SOT-23-5) is the discontinued product as of January, 2017.

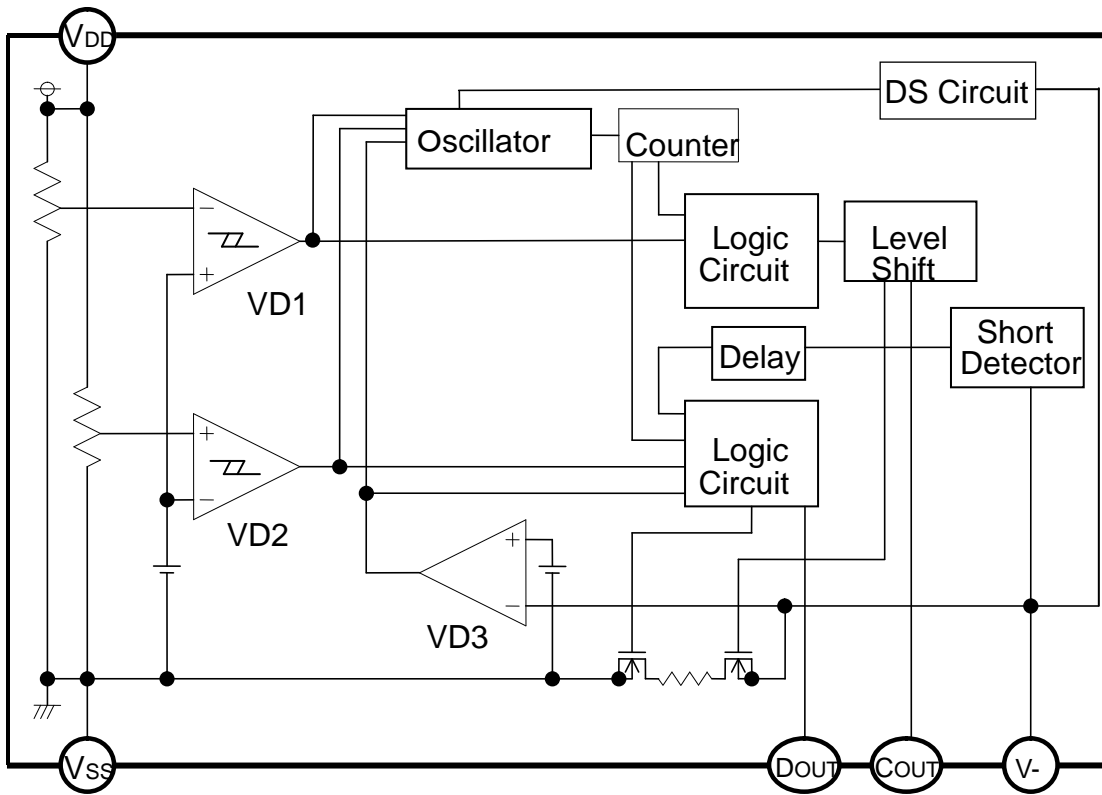
R5475N/R5478Nxxxxx

## BLOCK DIAGRAMS

C version



D/J/K version



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**R5475N/R5478Nxxxxx**

**SELECTION GUIDE**

In the R5475/R5478xxxxx Series, three of the input threshold for over-charge, over-discharge, and excess discharge current detectors can be designated.

Part Number is designated as follows:

R547xN xxx x x-xx-xx ←Part Number

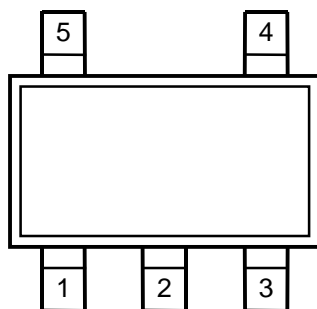
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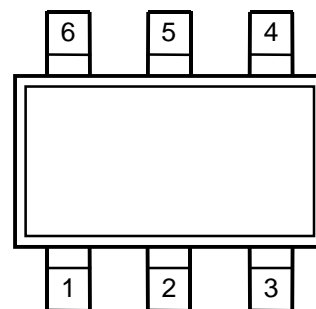
Code	Contents
a	Package Type R5475N: SOT-23-5 , R5478N: SOT-23-6
b	Serial Number for the R5475/R5478 Series designating input four threshold for over-charge, over-discharge, and excess discharge-current detectors.
c	Designation of Output delay option of over-charge, and excess discharge-current.
d	Designation of version symbols C version: With Latch function after Over-charge and Over-discharge D version: Released by voltage level from Over-charge and Over-discharge J version: Released by voltage level from Over-charge and Over-discharge Over-charge level = 3.65V Only K version: Released by voltage level from Over-charge and Over-discharge Over-charge level = 3.90V Only
e	Taping Type: TR (refer to Taping Specification)
f	FF : Using Pb-free solder.

**PIN CONFIGURATIONS**

**SOT-23-5 (R5475N)**



**SOT-23-6 (R5478N)**



\* R5475N (SOT-23-5) is the discontinued product as of January, 2017.

R5475N/R5478Nxxxxx

## PIN DESCRIPTION

Pin No.		Symbol	Description
SOT23-5	SOT23-6		
4	1	D <sub>OUT</sub>	Output of over-discharge detection, CMOS output
1	2	V-	Pin for charger negative input
5	3	C <sub>OUT</sub>	Output of over-charge detection, CMOS output
—	4	NC	No Connection
2	5	V <sub>DD</sub>	Power supply pin, the substrate voltage level of the IC.
3	6	V <sub>SS</sub>	V <sub>SS</sub> pin. Ground pin for the IC

## ABSOLUTE MAXIMUM RATINGS

V<sub>SS</sub>=0V

Symbol	Item	Ratings	Unit
V <sub>DD</sub>	Supply voltage	-0.3 to 12	V
V-	Input Voltage V- pin	V <sub>DD</sub> -30 to V <sub>DD</sub> +0.3	V
V <sub>C<sub>OUT</sub></sub>	Output voltage C <sub>OUT</sub> pin	V <sub>DD</sub> -30 to V <sub>DD</sub> +0.3	V
V <sub>D<sub>OUT</sub></sub>	D <sub>OUT</sub> pin	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3	V
P <sub>D</sub>	Power dissipation	150	mW
T <sub>opt</sub>	Operating temperature range	-40 to 85	°C
T <sub>stg</sub>	Storage temperature range	-55 to 125	°C

\*Note: Exposure to the condition exceeded Absolute Maximum Ratings may cause the permanent damages and affects the reliability and safety of both device and systems using the device.

The functional operations cannot be guaranteed beyond specified values in the Recommended conditions.

### ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

### RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

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**R5475N/R5478Nxxxxx**

**ELECTRICAL CHARACTERISTICS**

Unless otherwise specified, T<sub>opt</sub>=25°C

\*R5478N1xxEC

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Note2
V <sub>DD1</sub>	Operating input voltage	Voltage defined asV <sub>DD</sub> -V <sub>SS</sub>	1.5		5.0	V	F
V <sub>st</sub>	Minimum operating Voltage for 0V charging	Voltage defined asV <sub>DD</sub> -V <sub>-</sub> , V <sub>DD</sub> -V <sub>SS</sub> =0V			1.8	V	A
V <sub>DET1</sub>	Over-charge threshold	Detect rising edge of supply voltage R1=330Ω R1=330Ω (T <sub>opt</sub> =-5 to 55°C)*Note1	V <sub>DET1</sub> -0.025 V <sub>DET1</sub> -0.030	V <sub>DET1</sub> V <sub>DET1</sub>	V <sub>DET1</sub> +0.025 V <sub>DET1</sub> +0.030	V V	B
t <sub>VDET1</sub>	Output delay of over-charge	V <sub>DD</sub> =3.6V to 4.4V	0.7	1.0	1.3	s	B
t <sub>VREL1</sub>	Output delay of release from over-charge	V <sub>DD</sub> =4.5V to 3.6V, V <sub>-</sub> =0V to 0.4V	11	16	21	ms	C
V <sub>DET2</sub>	Over-discharge threshold	Detect falling edge of supply voltage	V <sub>DET2</sub> ×0.975	V <sub>DET2</sub>	V <sub>DET2</sub> ×1.025	V	D
t <sub>VDET2</sub>	Output delay of over-discharge	V <sub>DD</sub> =3.6V to 2.2V	14	20	26	ms	D
t <sub>VREL2</sub>	Output delay of release from over-discharge	V <sub>DD</sub> =2.2V to 3.6V	0.7	1.2	1.7	ms	D
V <sub>DET3</sub>	Excess discharge-current threshold	Detect rising edge of 'V-' pin voltage	V <sub>DET3</sub> -0.015	V <sub>DET3</sub>	V <sub>DET3</sub> +0.015	V	E
t <sub>VDET3</sub>	Output delay of excess discharge-current	V <sub>DD</sub> =3.0V, V <sub>-</sub> =0V to 0.4V	4	6	8	ms	E
t <sub>VREL3</sub>	Output delay of release from excess discharge-current	V <sub>DD</sub> =3.0V, V <sub>-</sub> =3V to 0V	0.7	1.2	1.7	ms	E
V <sub>short</sub>	Short protection voltage	V <sub>DD</sub> =3.0V	0.50	0.75	0.95	V	E
T <sub>short</sub>	Output Delay of Short protection	V <sub>DD</sub> =3.0V, V <sub>-</sub> =0V to 3V	150	200	300	μs	E
R <sub>short</sub>	Reset resistance for Excess discharge-current protection	V <sub>DD</sub> =3.6V, V <sub>-</sub> =1V	25	50	75	kΩ	F
V <sub>DS</sub>	Delay Shortening Mode input voltage	V <sub>DD</sub> =4.4V	-2.6	-2.0	-1.4	V	G
V <sub>OL1</sub>	Nch ON voltage of COUT	I <sub>ol</sub> =50μA, V <sub>DD</sub> =4.5V		0.4	0.5	V	H
V <sub>OH1</sub>	Pch ON voltage of COUT	I <sub>oh</sub> =-50μA, V <sub>DD</sub> =3.9V	3.4	3.7		V	I
V <sub>OL2</sub>	Nch ON voltage of DOUT	I <sub>ol</sub> =50μA, V <sub>DD</sub> =2.0V		0.2	0.5	V	J
V <sub>OH2</sub>	Pch ON voltage of DOUT	I <sub>oh</sub> =-50μA, V <sub>DD</sub> =3.9V	3.4	3.7		V	K
I <sub>DD</sub>	Supply current	V <sub>DD</sub> =3.9V, V <sub>-</sub> =0V		3.0	7.0	μA	L
I <sub>S</sub>	Standby current	V <sub>DD</sub> =2.0V			0.1	μA	L

\*Note1: Considering of variation in process parameters, we compensate for this characteristic related to temperature by laser-trim, however, this specification is guaranteed by design, not mass production tested.

\*Note2: indicates test circuits shown in page 17-20.

\* R5475N (SOT-23-5) is the discontinued product as of January, 2017.

**R5475N/R5478Nxxxxx**

\*R5475N/R5478N1xxCD

Unless otherwise specified, T<sub>opt</sub>=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Note2
VDD1	Operating input voltage	Voltage defined as VDD-VSS	1.5		5.0	V	F
Vst	Minimum operating Voltage for 0V charging	Voltage defined as VDD-V-, VDD-VSS=0V			1.8	V	A
VDET1	Over-charge threshold	Detect rising edge of supply voltage R1=330Ω R1=330Ω (T <sub>opt</sub> =-5 to 55°C)*Note	VDET1-0.025 VDET1-0.030	VDET1 VDET1	VDET1+0.025 VDET1+0.030	V V	B
VREL1	Released Voltage from Over-charge	Detect falling edge of supply voltage	VREL1-0.05	VREL1	VREL1+0.05	V	B
tVDET1	Output delay of over-charge	VDD=3.6V to 4.4V	0.7	1.0	1.3	s	B
tVREL1	Output delay of release from over-charge	VDD=4.5V to 3.6V	11	16	21	ms	B
VDET2	Over-discharge threshold	Detect falling edge of supply voltage	VDET2×0.975	VDET2	VDET2×1.025	V	D
VREL2	Released Voltage from Over-discharge	Detect rising edge of supply voltage	VREL2×0.975	VREL2	VREL2×1.025	V	D
tVDET2	Output delay of over-discharge	VDD=3.6V to 2.2V	14	20	26	ms	D
tVREL2	Output delay of release from over-discharge	VDD=3V V-=3V to 0V	0.7	1.2	1.7	ms	E
VDET3	Excess discharge-current threshold	Detect rising edge of 'V-' pin voltage	VDET3-0.015	VDET3	VDET3+0.015	V	E
tVDET3	Output delay of excess discharge-current	VDD=3.0V, V-=0V to 0.4V	8	12	16	ms	E
tVREL3	Output delay of release from excess discharge-current	VDD=3.0V, V-=3V to 0V	0.7	1.2	1.7	ms	E
Vshort	Short protection voltage	VDD=3.0V	0.50	0.75	0.95	V	E
Tshort	Output Delay of Short protection	VDD=3.0V, V-=0V to 3V	230	300	500	μs	E
Rshort	Reset resistance for Excess discharge-current protection	VDD=3.6V, V-=1V	25	50	75	kΩ	F
VDS	Delay Shortening Mode input voltage	VDD=4.4V	-2.6	-2.0	-1.4	V	G
VOL1	Nch ON voltage of COUT	I <sub>ol</sub> =50μA, VDD=4.5V		0.4	0.5	V	H
VOH1	Pch ON voltage of COUT	I <sub>oh</sub> =-50μA, VDD=3.9V	3.4	3.7		V	I
VOL2	Nch ON voltage of DOUT	I <sub>ol</sub> =50μA, VDD=2.0V		0.2	0.5	V	J
VOH2	Pch ON voltage of DOUT	I <sub>oh</sub> =-50μA, VDD=3.9V	3.4	3.7		V	K
IDD	Supply current	VDD=3.9V, V-=0V		3.0	7.0	μA	L
IS	Standby current	VDD=2.0V		1.2	2.0	μA	L

\*Note: Considering of variation in process parameters, we compensate for this characteristic related to temperature by laser-trim, however, this specification is guaranteed by design, not mass production tested.

\*Note2: indicates test circuits shown in page 17-20.

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**R5475N/R5478Nxxxxx**

\*R5478N1xxCJ

Unless otherwise specified, T<sub>opt</sub>=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Note2
V <sub>DD1</sub>	Operating input voltage	Voltage defined as V <sub>DD</sub> -V <sub>SS</sub>	1.5		5.0	V	F
V <sub>st</sub>	Minimum operating Voltage for 0V charging	Voltage defined as V <sub>DD</sub> -V <sub>-</sub> , V <sub>DD</sub> -V <sub>SS</sub> =0V			1.8	V	A
V <sub>DET1</sub>	Over-charge threshold	Detect rising edge of supply voltage R1=330Ω R1=330Ω (T <sub>opt</sub> =-5 to 55°C)*Note	V <sub>DET1</sub> -0.025 V <sub>DET1</sub> -0.030	V <sub>DET1</sub> V <sub>DET1</sub>	V <sub>DET1</sub> +0.025 V <sub>DET1</sub> +0.030	V V	B
V <sub>REL1</sub>	Released Voltage from Over-charge	Detect falling edge of supply voltage	V <sub>REL1</sub> -0.05	V <sub>REL1</sub>	V <sub>REL1</sub> +0.05	V	B
tV <sub>DET1</sub>	Output delay of over-charge	V <sub>DD</sub> =3.2V to 3.75V	0.7	1.0	1.3	s	B
tV <sub>REL1</sub>	Output delay of release from over-charge	V <sub>DD</sub> =3.9V to 3.2V	11	16	21	ms	B
V <sub>DET2</sub>	Over-discharge threshold	Detect falling edge of supply voltage	V <sub>DET2</sub> ×0.975	V <sub>DET2</sub>	V <sub>DET2</sub> ×1.025	V	D
V <sub>REL2</sub>	Released Voltage from Over-discharge	Detect rising edge of supply voltage	V <sub>REL2</sub> ×0.975	V <sub>REL2</sub>	V <sub>REL2</sub> ×1.025	V	D
tV <sub>DET2</sub>	Output delay of over-discharge	V <sub>DD</sub> =3.2V to 2.2V	14	20	26	ms	D
tV <sub>REL2</sub>	Output delay of release from over-discharge	V <sub>DD</sub> =2V to 3.1V	0.7	1.2	1.7	ms	E
V <sub>DET3</sub>	Excess discharge-current threshold	Detect rising edge of 'V-' pin voltage	V <sub>DET3</sub> -0.015	V <sub>DET3</sub>	V <sub>DET3</sub> +0.015	V	E
tV <sub>DET3</sub>	Output delay of excess discharge-current	V <sub>DD</sub> =3.0V, V <sub>-</sub> =0V to 0.4V	8	12	16	ms	E
tV <sub>REL3</sub>	Output delay of release from excess discharge-current	V <sub>DD</sub> =3.0V, V <sub>-</sub> =3V to 0V	0.7	1.2	1.7	ms	E
V <sub>short</sub>	Short protection voltage	V <sub>DD</sub> =3.0V	0.50	0.75	0.95	V	E
T <sub>short</sub>	Output Delay of Short protection	V <sub>DD</sub> =3.0V, V <sub>-</sub> =0V to 3V	230	300	500	μs	E
R <sub>short</sub>	Reset resistance for Excess discharge-current protection	V <sub>DD</sub> =3.2V, V <sub>-</sub> =1.0V	25	50	75	kΩ	F
V <sub>DS</sub>	Delay Shortening Mode input voltage	V <sub>DD</sub> =4.4V	-2.6	-2.0	-1.4	V	G
V <sub>OL1</sub>	Nch ON voltage of COUT	I <sub>ol</sub> =50μA, V <sub>DD</sub> =4.5V		0.4	0.5	V	H
V <sub>OH1</sub>	Pch ON voltage of COUT	I <sub>oh</sub> =-50μA, V <sub>DD</sub> =3.2V	2.7	3.0		V	I
V <sub>OL2</sub>	Nch ON voltage of DOUT	I <sub>ol</sub> =50μA, V <sub>DD</sub> =2.0V		0.2	0.5	V	J
V <sub>OH2</sub>	Pch ON voltage of DOUT	I <sub>oh</sub> =-50μA, V <sub>DD</sub> =3.2V	2.7	3.0		V	K
I <sub>DD</sub>	Supply current	V <sub>DD</sub> =3.2V, V <sub>-</sub> =0V		3.0	7.0	μA	L
I <sub>S</sub>	Standby current	V <sub>DD</sub> =2.0V		1.2	2.0	μA	L

\*Note: Considering of variation in process parameters, we compensate for this characteristic related to temperature by laser-trim, however, this specification is guaranteed by design, not mass production tested.

\*Note2: indicates test circuits shown in page 17-20.



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**R5475N/R5478Nxxxxx**

\*R5478N1xxCK

Unless otherwise specified, T<sub>opt</sub>=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Note2
VDD1	Operating input voltage	Voltage defined as VDD-VSS	1.5		5.0	V	F
Vst	Minimum operating Voltage for 0V charging	Voltage defined as VDD-V-, VDD-VSS=0V			1.8	V	A
VDET1	Over-charge threshold	Detect rising edge of supply voltage R1=330Ω R1=330Ω (T <sub>opt</sub> =-5 to 55°C)*Note	VDET1-0.025 VDET1-0.030	VDET1 VDET1	VDET1+0.025 VDET1+0.030	V V	B
VREL1	Released Voltage from Over-charge	Detect falling edge of supply voltage	VREL1-0.05	VREL1	VREL1+0.05	V	B
tVDET1	Output delay of over-charge	VDD=3.2V to 3.75V	0.7	1.0	1.3	s	B
tVREL1	Output delay of release from over-charge	VDD=3.9V to 3.2V	11	16	21	ms	B
VDET2	Over-discharge threshold	Detect falling edge of supply voltage	VDET2×0.975	VDET2	VDET2×1.025	V	D
VREL2	Released Voltage from Over-discharge	Detect rising edge of supply voltage	VREL2×0.975	VREL2	VREL2×1.025	V	D
tVDET2	Output delay of over-discharge	VDD=3.2V to 1.9V	14	20	26	ms	D
tVREL2	Output delay of release from over-discharge	VDD=1.9V to 3.1V	0.7	1.2	1.7	ms	E
VDET3	Excess discharge-current threshold	Detect rising edge of 'V-' pin voltage	VDET3-0.015	VDET3	VDET3+0.015	V	E
tVDET3	Output delay of excess discharge-current	VDD=3.0V, V-=0V to 0.4V	8	12	16	ms	E
tVREL3	Output delay of release from excess discharge-current	VDD=3.0V, V-=3V to 0V	0.7	1.2	1.7	ms	E
Vshort	Short protection voltage	VDD=3.0V	0.50	0.75	0.95	V	E
Tshort	Output Delay of Short protection	VDD=3.0V, V-=0V to 3V	230	300	500	μs	E
Rshort	Reset resistance for Excess discharge-current protection	VDD=3.2V, V-=1.0V	25	50	75	kΩ	F
VDS	Delay Shortening Mode input voltage	VDD=4.4V	-2.6	-2.0	-1.4	V	G
VOL1	Nch ON voltage of COUT	I <sub>ol</sub> =50μA, VDD=4.5V		0.4	0.5	V	H
VOH1	Pch ON voltage of COUT	I <sub>oh</sub> =-50μA, VDD=3.2V	2.7	3.0		V	I
VOL2	Nch ON voltage of DOUT	I <sub>ol</sub> =50μA, VDD=1.9V		0.2	0.5	V	J
VOH2	Pch ON voltage of DOUT	I <sub>oh</sub> =-50μA, VDD=3.2V	2.7	3.0		V	K
IDD	Supply current	VDD=3.2V, V-=0V		3.0	7.0	μA	L
IS	Standby current	VDD=2.0V		1.2	2.0	μA	L

\*Note: Considering of variation in process parameters, we compensate for this characteristic related to temperature by laser-trim, however, this specification is guaranteed by design, not mass production tested.

\*Note2: indicates test circuits shown in page 17-20.

## OPERATION

### • VD1 / Over-Charge Detector

The VD1 monitors  $V_{DD}$  pin voltage while charge the battery pack. When the  $V_{DD}$  voltage crosses over-charge detector threshold  $V_{DET1}$  from a low value to a value higher than the  $V_{DET1}$ , the VD1 can detect over-charge and an external charge control Nch MOSFET turn off with  $C_{OUT}$  pin being at "L" level.

In terms of C version, to reset the VD1 making the  $C_{OUT}$  pin level to "H" again after detecting over-charge, in such conditions that a time when the  $V_{DD}$  voltage is down to a level lower than over-charge voltage, by connecting a kind of loading to  $V_{DD}$  after disconnecting a charger from the battery pack. Output voltage of  $C_{OUT}$  pin becomes "H", and it makes an external Nch MOSFET turn on, and charge cycle is available. In other words, once over-charge is detected, even if the supply voltage becomes low enough, if a charger is continuously connected to the battery pack, recharge is not possible. Therefore this over-charge detector has no hysteresis. To judge whether or not load is connected, the built-in excess-discharge current detector is used. In other words, by connecting some load,  $V_{-}$  pin voltage becomes equal or more than excess-discharge current detector threshold, and reset the over-charge detecting state.

In terms of D/J/K version, after detecting over-charge, if  $V_{DD}$  pin voltage is lower than released from over-charge, even if a charger is connected, over-charge detector is released. Further, in case that  $V_{DD}$  pin level is lower than detector threshold and higher than released voltage from over-charge, if a charger is removed and some load is connected, over-charge detector is also released.

After detecting over-charge with the  $V_{DD}$  voltage of higher than  $V_{DET1}$ , connecting system load to the battery pack makes load current allowable through parasitic diode of external charge control FET.

The  $C_{OUT}$  level would be "H" when the  $V_{DD}$  level is down to a level below the  $V_{DET1}$  by continuous drawing of load current.

Internal fixed output delay times for over-charge detection and release from over-charge exist. Even when the  $V_{DD}$  pin level becomes equal or higher level than  $V_{DET1}$  if the  $V_{DD}$  voltage would be back to a level lower than the  $V_{DET1}$  within a time period of the output delay time, VD1 would not output a signal for turning off the charge control FET. Besides, after detecting over-charge, while the  $V_{DD}$  is lower than over-charge detector, even if a charger is removed and a load is connected, if the voltage is recovered within output delay time of release from over-charge, over-charge state is not released.

A level shifter incorporated in a buffer driver for the  $C_{OUT}$  pin makes the "L" level of  $C_{OUT}$  pin to the  $V_{-}$  pin voltage and the "H" level of  $C_{OUT}$  pin is set to  $V_{DD}$  voltage with CMOS buffer.

### • VD2 / Over-Discharge Detector

The VD2 is monitoring a  $V_{DD}$  pin voltage. When the  $V_{DD}$  voltage crosses the over-discharge detector threshold  $V_{DET2}$  from a high value to a value lower than the  $V_{DET2}$ , the VD2 can detect an over-discharge and the external discharge control Nch MOSFET turns off with the  $D_{OUT}$  pin being at "L" level.

In terms of C version, to reset the VD2 with the  $D_{OUT}$  pin level being "H" again after detecting over discharge, it is necessary to connect a charger to the battery pack. When the  $V_{DD}$  voltage stays under over-discharge detector threshold  $V_{DET2}$ , charge-current can flow through parasitic diode of an external discharge control MOSFET, then after the  $V_{DD}$  voltage comes up to a value larger than  $V_{DET2}$ , then,  $D_{OUT}$  becomes "H" and discharging process would be able to advance through ON state MOSFET for discharge control.

Connecting a charger to the battery pack makes the  $D_{OUT}$  level being "H" instantaneously when the  $V_{DD}$  voltage is higher than  $V_{DET2}$ .

In terms of D/J/K version, released operation by connecting a charger is same as C version. However, without a charger, if  $V_{DD}$  pin voltage is equal or more than the released voltage from over-discharge,  $D_{OUT}$  pin becomes "H" immediately.

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When a cell voltage equals to zero, if the voltage of a charger is equal or more than 0V-charge minimum voltage (Vst), C<sub>OUT</sub> pin becomes "H" and a system is allowable to charge.

An output delay time for over-discharge detection is fixed internally. When the V<sub>DD</sub> level is down to a equal or lower level than V<sub>DET2</sub> if the V<sub>DD</sub> voltage would be back to a level higher than the V<sub>DET2</sub> within a time period of the output delay time, VD2 would not output a signal for turning off the discharge control FET. Output delay time for release from over-discharge is also set.

After detecting over-discharge by VD2, supply current would be reduced and be into standby by halting unnecessary circuits and consumption current of IC itself is made as small as possible.

The output type of D<sub>OUT</sub> pin is CMOS having "H" level of V<sub>DD</sub> and "L" level of V<sub>SS</sub>.

• **VD3 /Excess discharge-current Detector, Short Circuit Protector**

Both of the excess current detector and short circuit protection can work when the both of control FETs are in "ON" state.

When the V- pin voltage is up to a value between the short protection voltage V<sub>short</sub> /V<sub>DD</sub> and excess discharge-current threshold V<sub>DET3</sub>, VD3 operates and further soaring of V- pin voltage higher than V<sub>short</sub> makes the short circuit protector enabled. This leads the external discharge control Nch MOSFET turns off with the D<sub>OUT</sub> pin being at "L" level.

An output delay time for the excess discharge-current detector is internally fixed.

A quick recovery of V- pin level from a value between V<sub>short</sub> and V<sub>DET3</sub> within the delay time keeps the discharge control FET staying "H" state. Output delay time for Release from excess discharge-current detection is also set.

When the short circuit protector is enabled, the D<sub>OUT</sub> would be "L" and the delay time is also set.

The V - pin has a built-in pull-down resistor to the V<sub>SS</sub> pin, that is, the resistance to release from excess-discharge current.

After an excess discharge-current or short circuit protection is detected, removing a cause of excess discharge-current or external short circuit makes an external discharge control FET to an "ON" state automatically with the V- pin level being down to the V<sub>SS</sub> level through built-in pulled down resistor. The reset resistor of excess discharge-current is off at normal state. Only when detecting excess discharge-current or short circuit, the resistor is on.

Output delay time of excess discharge-current is set shorter than the delay time for over-discharge detector. Therefore, if V<sub>DD</sub> voltage would be lower than V<sub>DET2</sub> at the same time as the excess discharge-current is detected, the R5478xxxxxx is at excess discharge-current detection mode. By disconnecting a load, VD3 is automatically released from excess discharge-current.

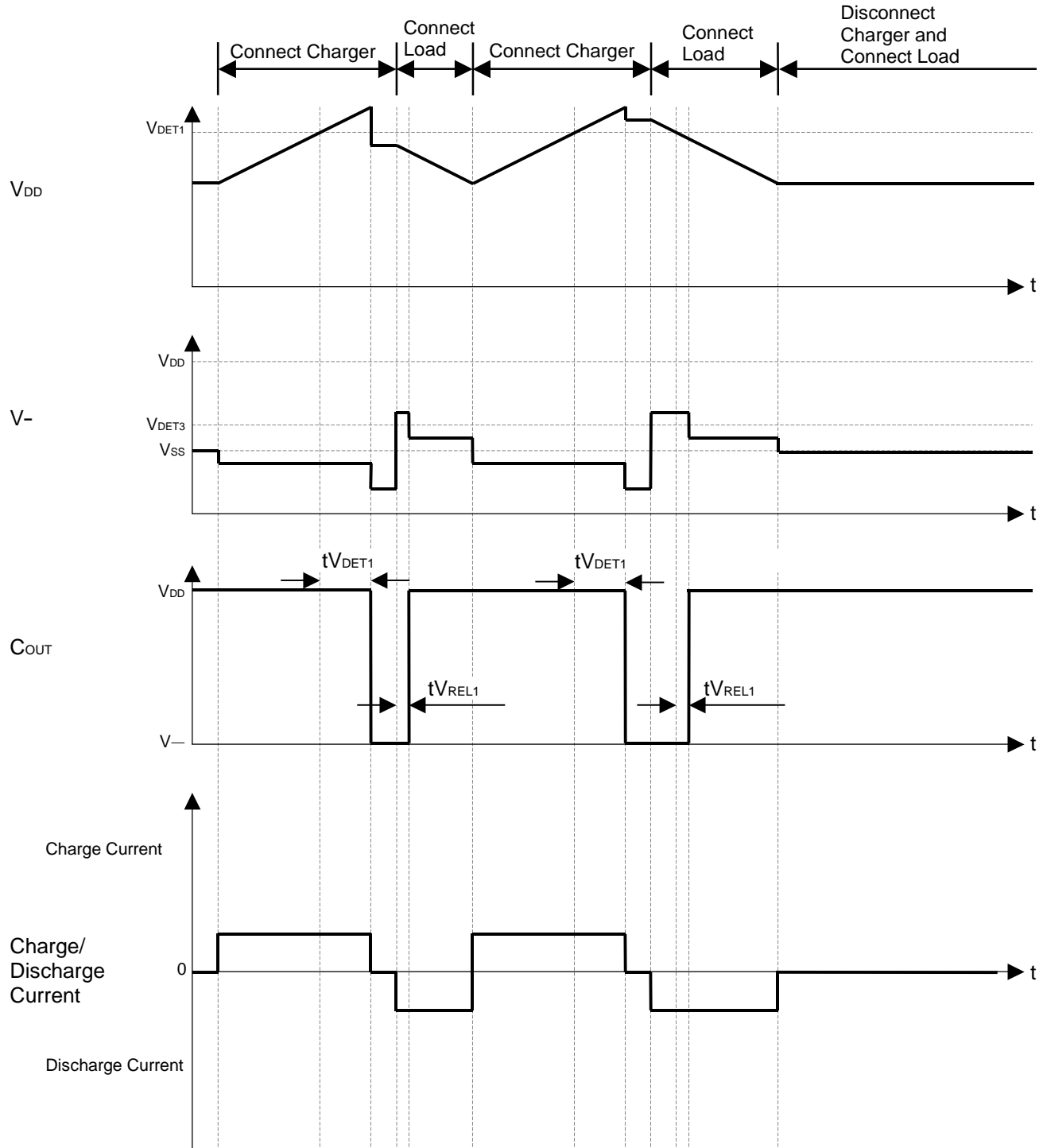
• **DS (Delay Shorten) function**

Output delay time of over-charge, over-discharge, and release from those detecting modes can be shorter than those setting value by forcing equal or less than the delay shortening mode voltage to V- pin.

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### TIMING CHART

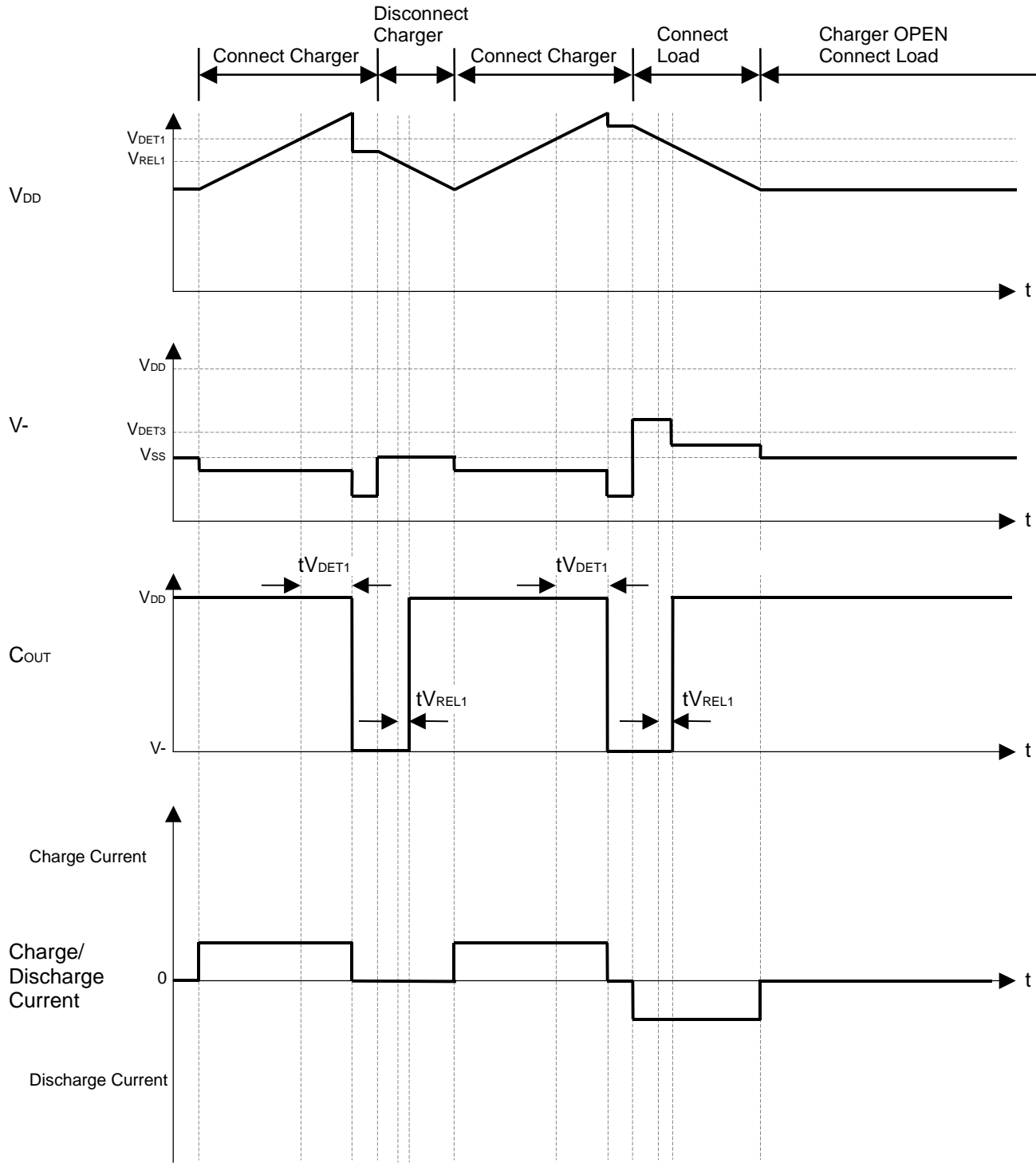
1. Over-charge (Latch Type) voltage, Excess charge current Operation



\* R5475N (SOT-23-5) is the discontinued product as of January, 2017.

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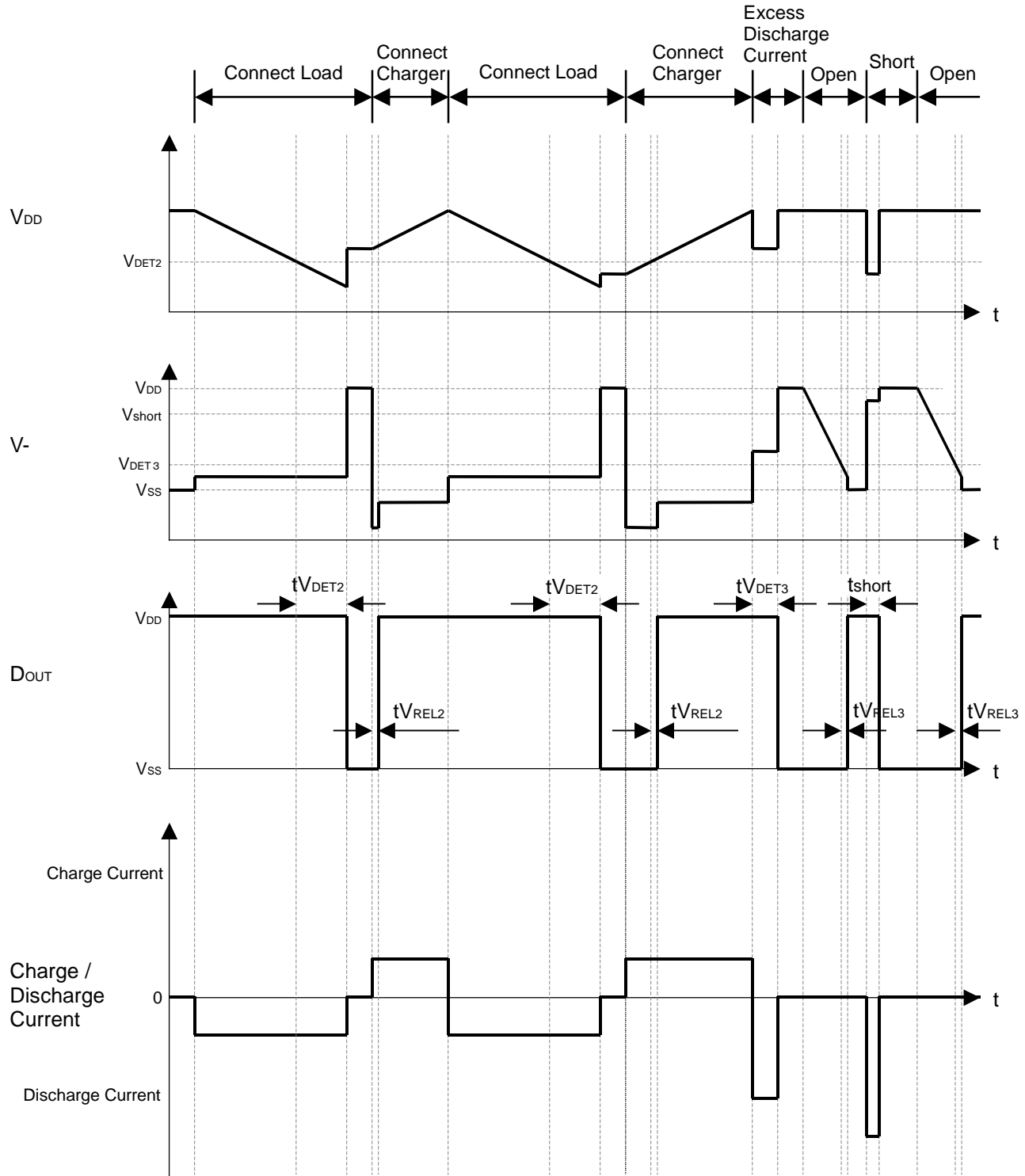
2. Over-charge (Released by voltage Type) voltage, Excess charge current Operation



\* R5475N (SOT-23-5) is the discontinued product as of January, 2017.

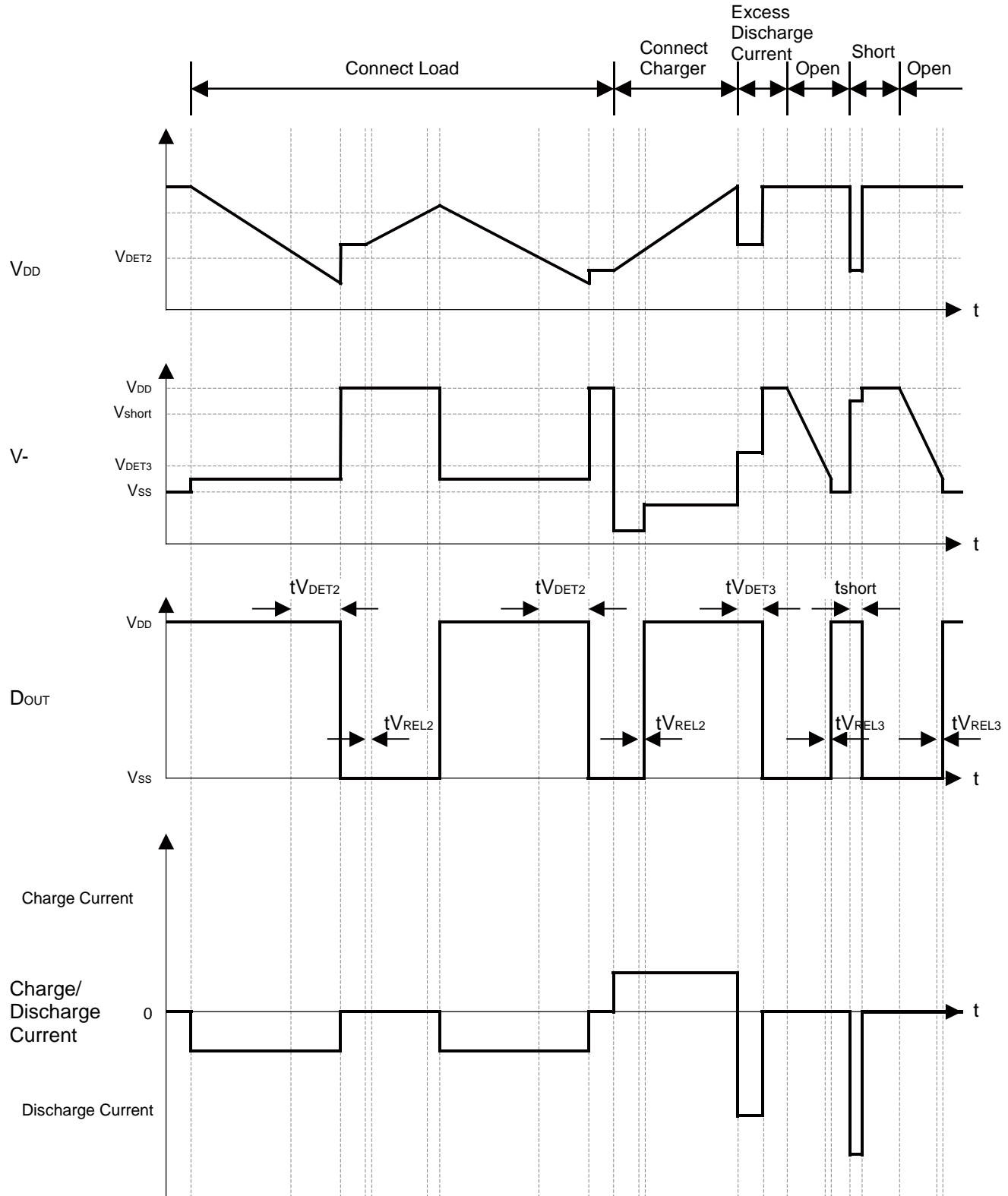
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3. Over-discharge (Latch Type), Excess discharge current, Short circuit



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4. Over-discharge (Released by voltage Type), Excess discharge current, Short circuit

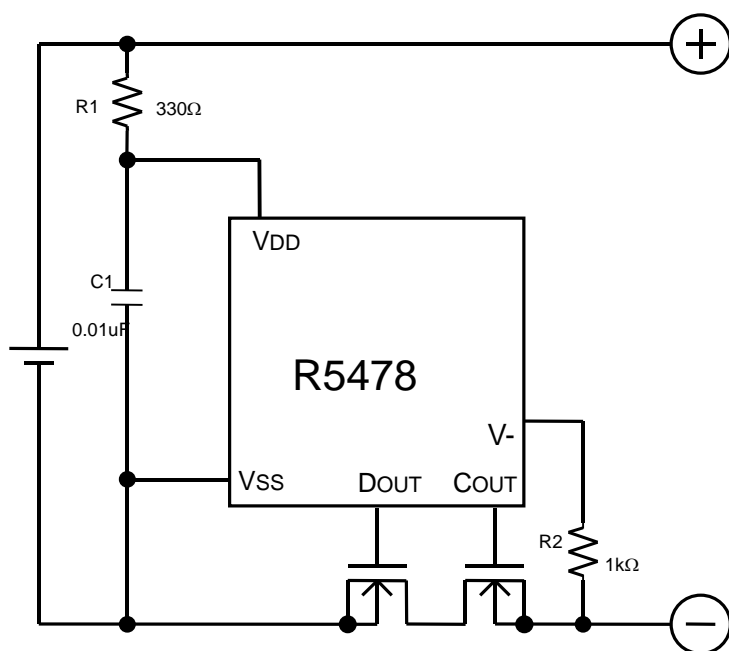


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## TYPICAL APPLICATION



## APPLICATION HINTS

R1 and C1 will stabilize a supply voltage to the R5478xxxxxx. A recommended R1 value is less than 1kΩ. A larger value of R1 leads higher detection voltage, makes some errors because of some conduction current may flow in the R5478xxxxxx.

Further, to stabilize the operation of the R5478, use the C1 with the value in the range from 0.001μF to 0.01μF. To choose the most suitable value of C1, fully evaluation is necessary.

R1 and R2 can operate also as parts for current limit circuit against reverse charge or applying a charger with excess charging voltage to the R5478xxxxxx, battery pack. Small value of R1 and R2 may cause over-power consumption rating of power dissipation of the R5478xxxxxx. Thus, the total value of 'R1+R2' should be equal or more than 1kΩ.

On the other hand, if large value of R2 is set, release from over-discharge by connecting a charger might not be possible. Recommended R2 value is equal or less than 10kΩ.

The typical application circuit diagram is just an example. This circuit performance largely depends on the PCB layout and external components. In the actual application, fully evaluation is necessary.

Over-voltage and the over current beyond the absolute maximum rating should not be forced to the protection IC and external components.

We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire-containment feature and fail-safe feature.

We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.



## TEST CIRCUITS

### 1, Minimum Operating Voltage for 0V Charging(0V battery charge function “available”)(Test circuit A)

The minimum operating voltage for 0V charging ( $V_{st}$ ) is defined as the voltage between the VDD pin and the V- pin at which COUT goes to “H” ( $V_{DD} - 0.1V$  or higher) when the voltage  $V_2$  is gradually decreased from the starting condition of  $V_1 = 0V$ ,  $V_2 = -0.3V$ .

### 2, Over-charge Threshold Voltage (Test circuit B)

The over-charge threshold voltage( $V_{DET1}$ ) is defined as the voltage between the VDD pin and the VSS pin at which COUT goes from “H” to “L” when the voltage  $V_1$  is gradually increased from the starting condition of  $V_1 = 3.5V$  with  $R_1=330\Omega$  between VDD and Pack+.

### 3, Release voltage from Over-charge (Test circuit B) \*Except EC version

The release voltage from over-charge ( $V_{REL1}$ ) is defined as the voltage between the VDD pin and the VSS pin at which COUT goes from “L” to “H” when the voltage  $V_1$  is then gradually decreased with  $R_1=330\Omega$  between VDD and Pack+.

### 4, Output Delay of Over-charge (Test circuit B)

The output delay of over-charge ( $t_{VDET1}$ ) is the time needed for COUT to change from “H” to “L” just after the voltage  $V_1$  momentarily increases (within  $10\mu s$ ) from over-charge threshold voltage ( $V_{DET1}$ ) -  $0.2V$  to over-charge threshold voltage ( $V_{DET1}$ ) +  $0.2V$  under the set conditions of  $V_2 = 0V$ .

### 5, Release Delay for VD1 (Test circuit B) \*Except EC version

The release Delay for VD1 ( $t_{VREL1}$ ) is the time needed for COUT to change from “L” to “H” just after the voltage  $V_1$  momentarily decreases (within  $10\mu s$ ) from over-charge threshold voltage ( $V_{DET1}$ ) +  $0.2V$  to overcharge release voltage ( $V_{REL1}$ ) -  $0.2V$  under the set conditions of  $V_2 = 0V$ .

### 6, Release Delay for VD1 (Test circuit C) \*for EC version

The release Delay for VD1 ( $t_{VREL1}$ ) is the time needed for COUT to change from “L” to “H” just after the voltage  $V_2$  momentarily increases (within  $10\mu s$ ) from  $0V$  to excess discharge-current threshold ( $V_{DET3}$ ) +  $0.1V$  under the set conditions of  $V_1$  from over-charge threshold voltage ( $V_{DET1}$ ) +  $0.2V$  to over-charge threshold voltage ( $V_{DET1}$ ) -  $0.2V$ .

### 7, Overdischarge Threshold Voltage (Test circuit D)

The overdischarge threshold voltage( $V_{DET2}$ ) is defined as the voltage between the VDD pin and the VSS pin at which DOUT goes from “H” to “L” when the voltage  $V_1$  is gradually decreased from the starting condition of  $V_1 = 3.5V$ ,  $V_2 = 0V$ .

### 8, Released Voltage from Over-discharge (Test circuit E) \*Except EC version

The released voltage from over-discharge ( $V_{REL2}$ ) is defined as the voltage between the VDD pin and the VSS pin at which DOUT goes from “L” to “H” when the voltage  $V_1$  is then gradually increased under the set conditions of  $V_2 = V_1$ .

### 9, Output Delay of Over-discharge (Test circuit D)

The output delay of over-discharge ( $t_{VDET2}$ ) is the time needed for DOUT to change from “H” to “L” just after the voltage  $V_1$  momentarily decreases (within  $10\mu s$ ) from over-discharge threshold voltage ( $V_{DET2}$ ) +  $0.2V$  to over-discharge threshold voltage ( $V_{DET2}$ ) -  $0.2V$  under the set conditions of  $V_2 = 0V$ .

### 10, Release Delay for VD2 (Test circuit E) \*Except EC version

The release delay for VD2 ( $t_{VREL2}$ ) is the time needed for DOUT to change from “L” to “H” just after the voltage  $V_1$  momentarily increases (within  $10\mu s$ ) from over-discharge threshold voltage ( $V_{DET2}$ ) -  $0.2V$  to

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over-discharge release voltage (VREL2) + 0.2V under the set conditions of V2 = V1.

11, Release Delay for VD2 (Test circuit D) \*For EC version

The release delay for VD2 (tVREL2) is the time needed for DOUT to change from “L” to “H” just after the voltage V1 momentarily increases (within 10 $\mu$ s) from over-discharge threshold voltage (VDET2) - 0.2V to over-discharge release voltage (VREL2) + 0.2V under the set conditions of V2 = 0V.

12, Excess discharge-current threshold (Test circuit E)

Excess discharge-current threshold (VDET3) is defined as the voltage between the V- pin and the VSS pin at which DOUT goes from “H” to “L” when the voltage V2 is then gradually increased from the starting condition of V1 = 3.0V , V2 = 0V.

13, Output delay of excess discharge-current, Release Delay for VD3 (Test circuit E)

The output delay of excess discharge-current (tVDET3) is the time needed for DOUT to go to “L” after the voltage V2 momentarily increases (within 10 $\mu$ s) from 0V to 0.40V under the set conditions of V1 =3.0V. The Release Delay for VD3 (tVREL3) is the time needed for DOUT to go to “H” after the voltage V2 momentarily decreases (within 10 $\mu$ s) from 3.0V to 0V under the set conditions of V1 =3.0V.

14, Short Protection Voltage (Test circuit E)

The short protection voltage (Vshort) is defined as the voltage between the V- pin and the VSS pin whose delay time for changing DOUT from “H” to “L” lies between the minimum and the maximum value of load short-circuiting delay time when the voltage V2 is increased rapidly (within 10 $\mu$ s) from the starting condition of V1 = 3.0V , V2 = 0V.

15, Delay Time for Short Protection (Test circuit E)

The delay time for short protection (tshort) is the time needed for DOUT to go to “L” after the voltage V2 momentarily increases (within 10 $\mu$ s) from 0V to 3.0V under the set conditions of V1 =3.0V.

16, Reset Resistance for Excess Current Protection (Test circuit F)

The Reset Resistance for Excess Current Protection (Rshort) is the resistance between the V- pin and the VSS pin under the set conditions of V1 =3.6V, V2 = 1.0V.

17, Delay Time Shortening Mode Voltage (Test circuit G)

The Delay Time Shortening Mode Voltage (VDS) is the voltage is defined as the voltage between the V- pin and VSS pin at which tVDET1 becomes about 1/57 at V2 = 0V when the voltage V2 is then gradually decreased from the starting condition of V2 = 0V.

18, Nch ON-Voltage of C<sub>OUT</sub> (Test circuit H)

The Nch ON-Voltage of C<sub>OUT</sub> (VoL1) is the resistance at the COUT pin under the set conditions of V1 = 4.5V, V2 = 0V, I3 = 50 $\mu$ A.

19, Pch ON-Voltage of C<sub>OUT</sub> (Test circuit I)

The Pch ON-Voltage of C<sub>OUT</sub> (VoH1) is the Voltage at the COUT pin under the set conditions of V1 = 3.9V for EC,CD version / 3.8V for CK version / 3.5V for CJ version, V2 = 0V, I3 = -50 $\mu$ A.

20, Pch ON-Voltage of D<sub>OUT</sub> (Test circuit J)

Pch ON-Voltage of D<sub>OUT</sub> (VoH2) is the Voltage at the DOUT pin under the set conditions of V1 = 3.9V for EC,CD version / 3.8V for CK version / 3.5V for CJ version, V2 = 0V, I4 = -50 $\mu$ A.

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21, Nch ON-Voltage of D<sub>OUT</sub> (Test circuit K)

Nch ON-Voltage of D<sub>OUT</sub> (VoL2) is the Voltage at the D<sub>OUT</sub> pin under the set conditions of V1 = 2.0V, V2 = 0V, I4 = 50 $\mu$ A.

22, Supply Current (Test circuit L)

The supply current (IDD) is the current that flows through the VDD pin(IDD) under the set conditions of V1 = 3.9V for EC,CD version / 3.8V for CK version / 3.5V for CJ version and V2 = 0V (normal status).

23, Standby Current (Test circuit L)

The standby current (Istandby) is the current that flows through the VDD pin(IDD) under the set conditions of V1 = V2 = 2.0V (overdischarge status).

V1 : The voltage between VDD pin and VSS pin.

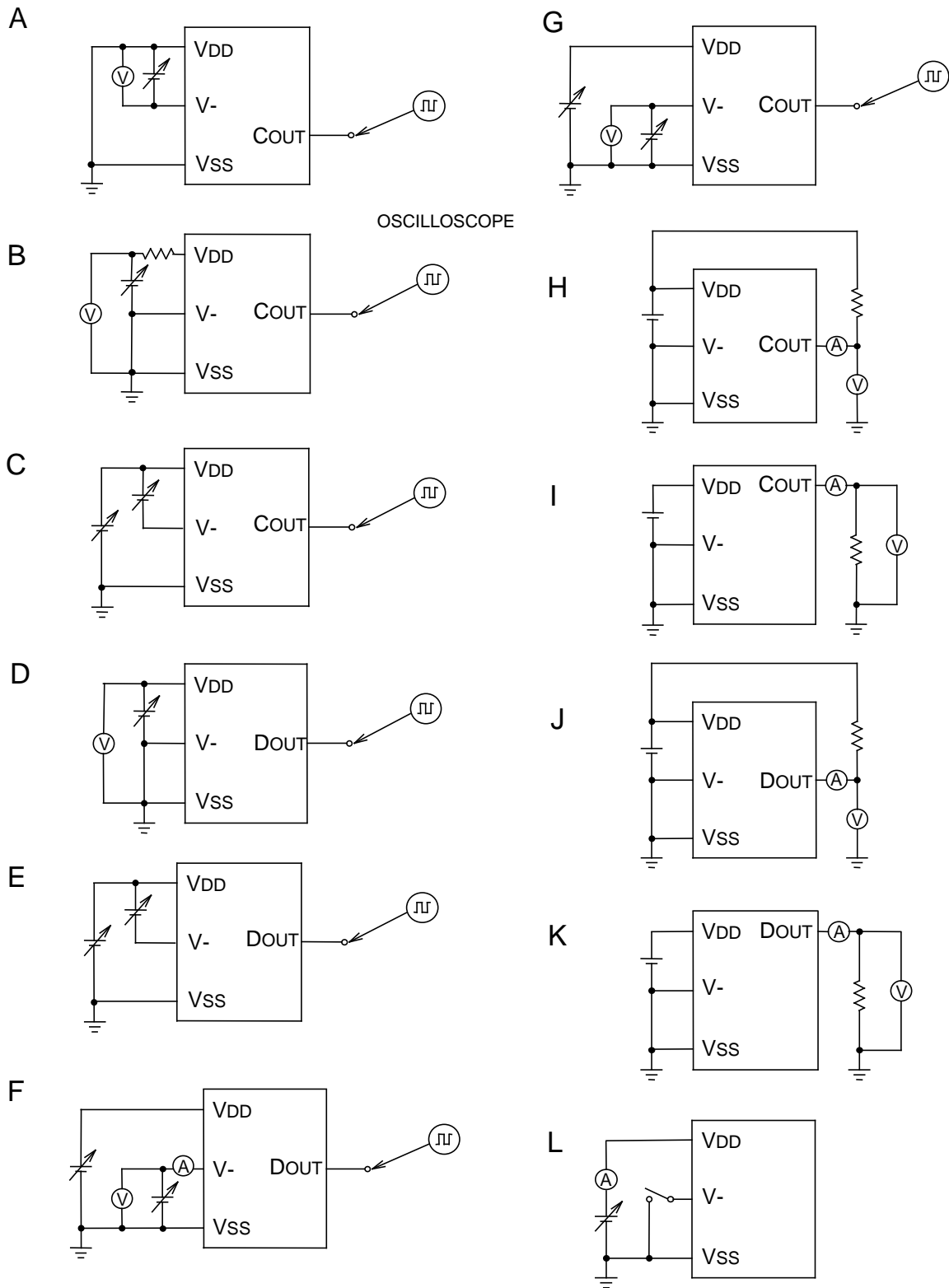
V2 : The voltage between V- pin and VSS pin.

I3 : The current flow into C<sub>OUT</sub> pin.

I4 : The current flow into D<sub>OUT</sub> pin.

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Typical Characteristics were obtained with using those above circuits:

Test Circuit A: Typical characteristics 1)

Test Circuit B: Typical characteristics 2)

Test Circuit C: Typical characteristics 3) 4)

Test Circuit D: Typical characteristics 5) 6) 7)

Test Circuit E: Typical characteristics 8) 9) 10) 11) 12)

Test Circuit F: Typical characteristics 13)

Test Circuit G: Typical characteristics 14)

Test Circuit H: Typical characteristics 15)

Test Circuit I: Typical characteristics 16)

Test Circuit J: Typical characteristics 17)

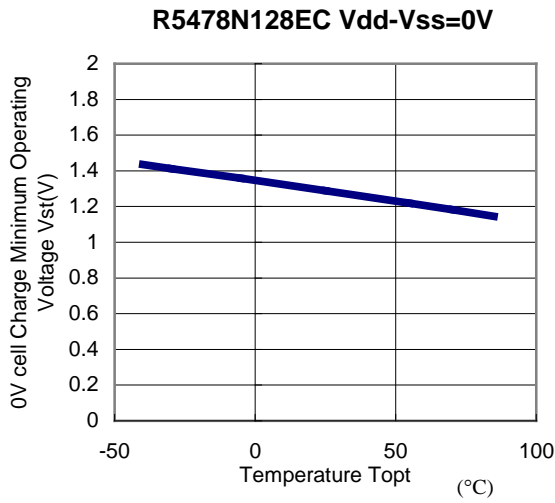
Test Circuit K: Typical characteristics 18)

Test Circuit L: Typical characteristics 19) 20)

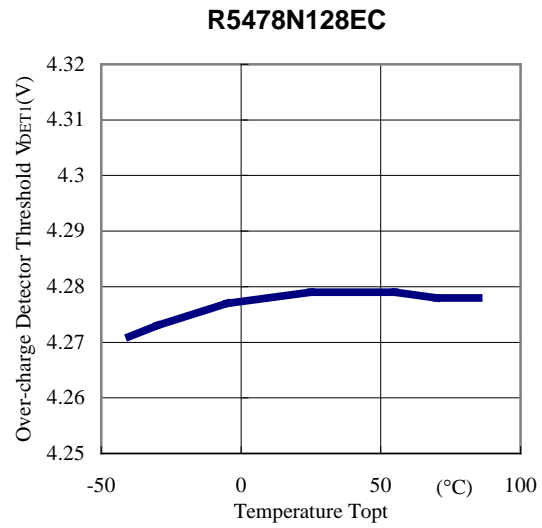
R5475N/R5478Nxxxxx

**TYPICAL CHARACTERISTICS**

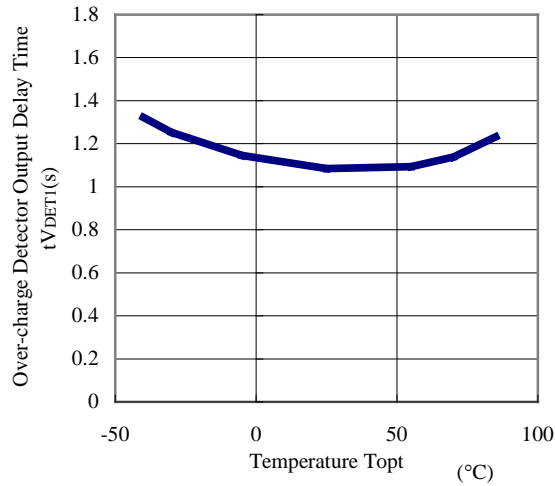
1) Minimum Operating Voltage for 0V Cell Charging vs. Temperature



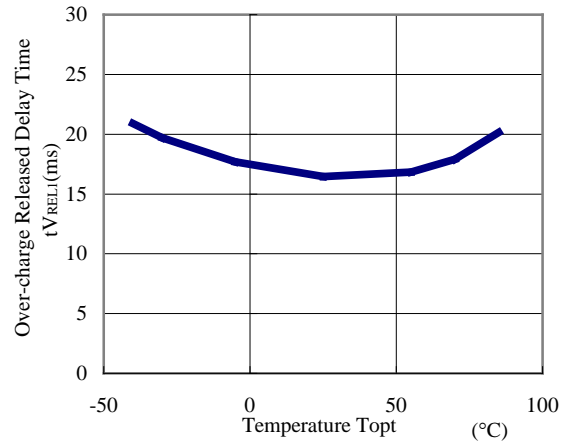
2) Over-Charge Threshold vs. Temperature



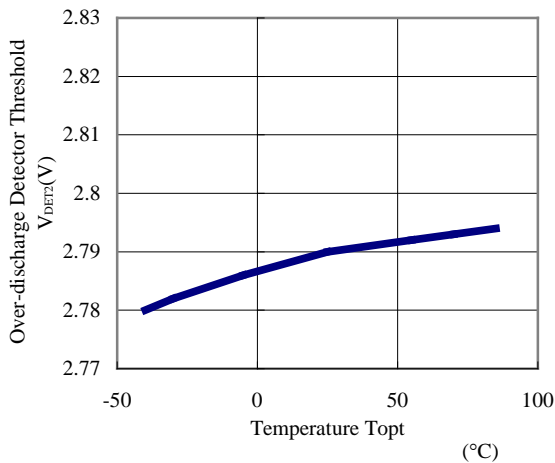
3) Output Delay of Over-charge vs. Temperature  
**R5478N128EC**



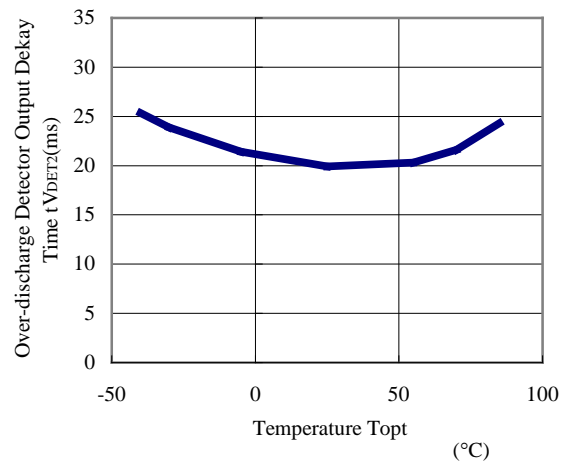
4) Output Delay of Release from Over-charge vs. Temperature  
**R5478N128EC**



5) Over discharge Threshold vs. Temperature  
**R5478N128EC**



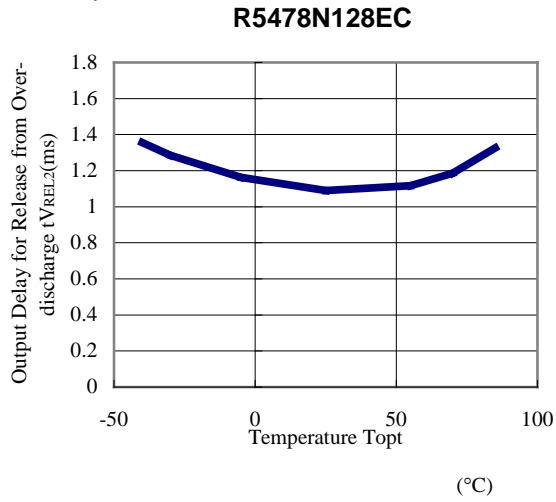
6) Output Delay of Over-discharge vs. Temperature  
**R5478N128EC**



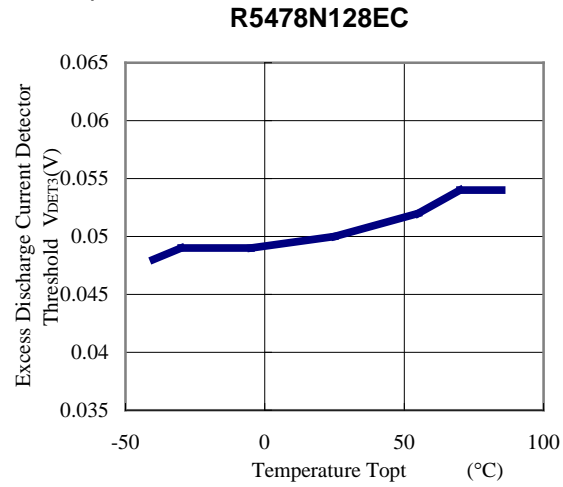
\* R5475N (SOT-23-5) is the discontinued product as of January, 2017.

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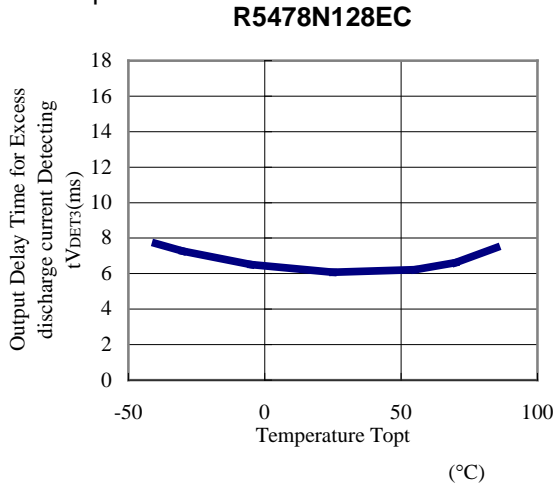
7) Output Delay of Release from Over-discharge vs. Temperature



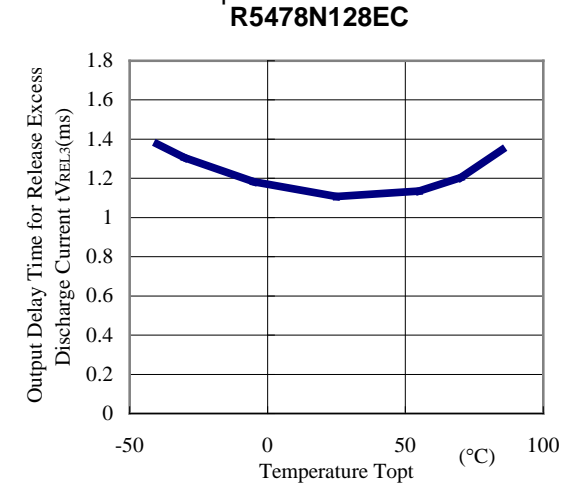
8) Excess Discharge-current Threshold vs. Temperature



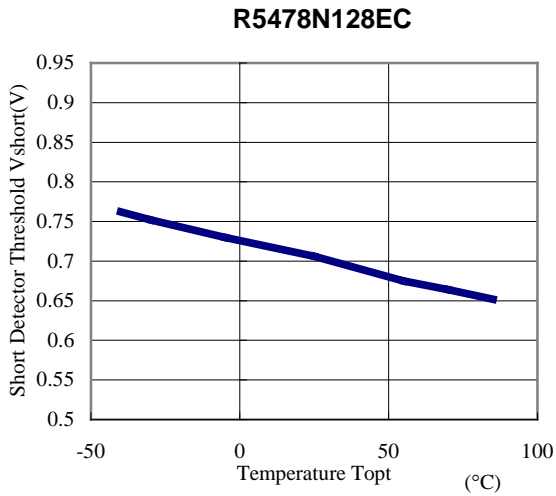
9) Output Delay of Excess Discharge-current vs. Temperature



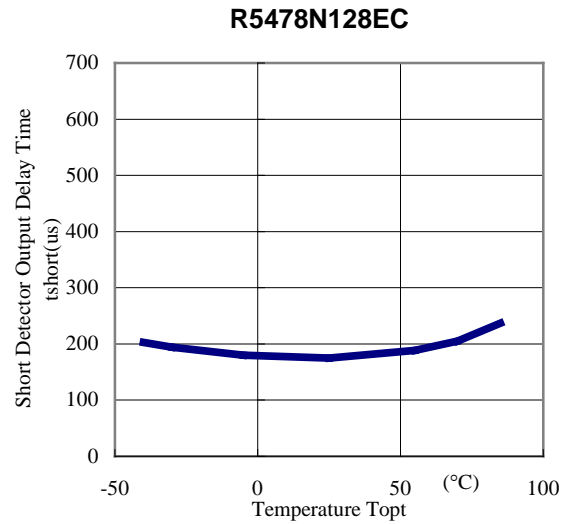
10) Output Delay of Release from Excess Discharge-current vs. Temperature



11) Short Detector Voltage vs. Temperature



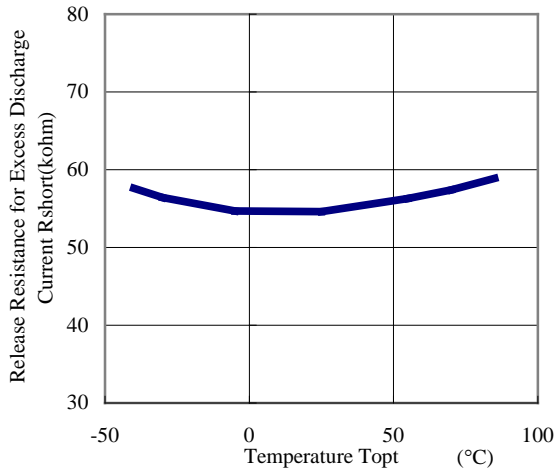
12) Output Delay of Short Protection vs. Temperature



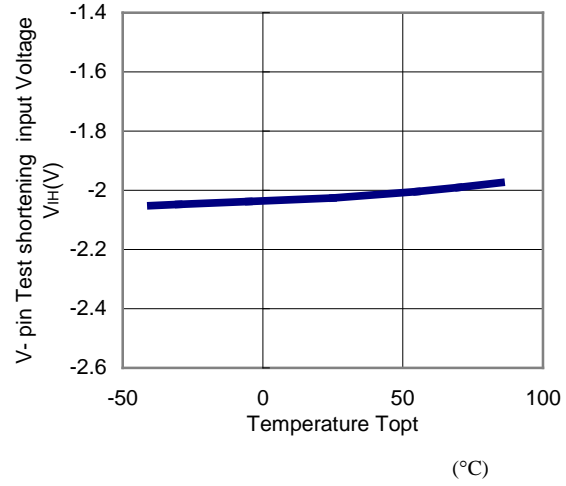
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**R5475N/R5478Nxxxxx**

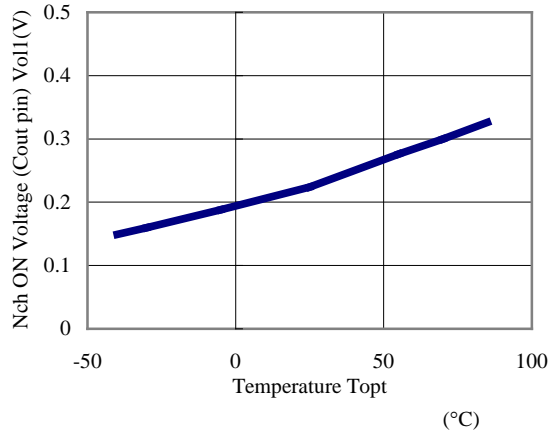
13) Reset Resistance for Excess Discharge current Protection vs. Temperature  
**R5478N128EC**



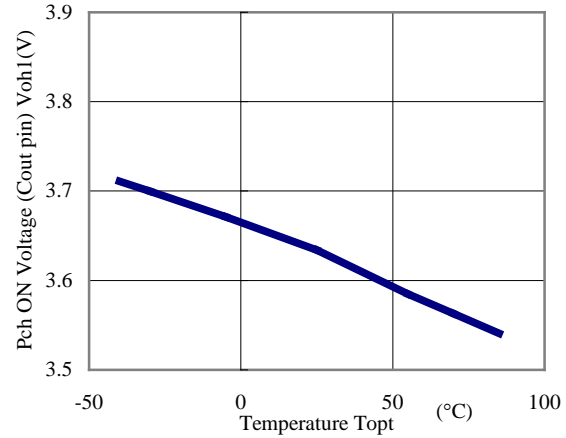
14) V- pin Test time shortening input Voltage vs. Temperature  
**R5478N128EC**



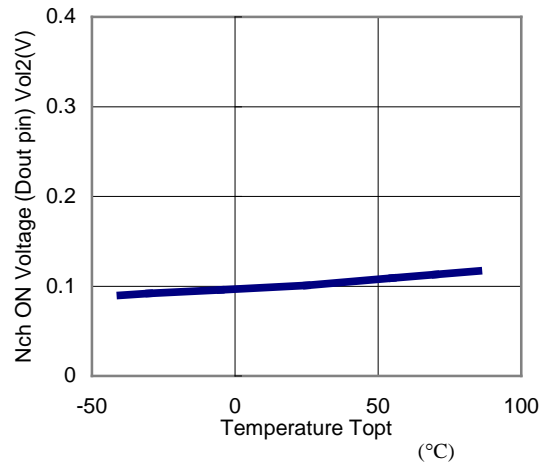
15) Nch On Voltage (COUT pin) vs. Temperature  
IOL=50uA, Vdd=4.5V  
**R5478N128EC**



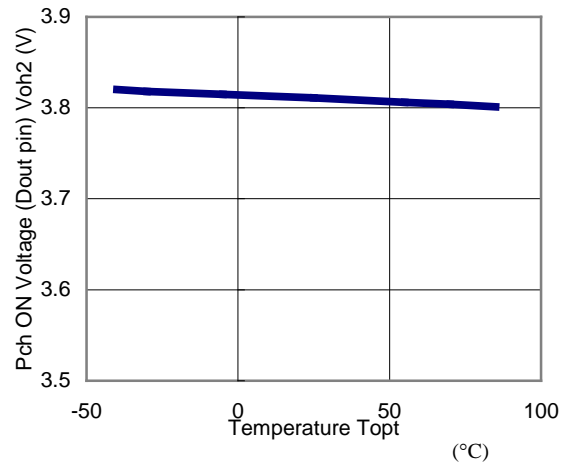
16) Pch On Voltage (COUT pin) vs. Temperature  
Ioh=-50uA, Vdd=3.9V  
**R5478N128EC**



17) Nch On Voltage (DOUT pin) vs. Temperature  
Iol=50uA, VDD=2V  
**R5478N128EC**



18) Pch ON Voltage of DOUT vs. Temperature  
Ioh=-50uA, Vdd=3.9V  
**R5478N128EC**





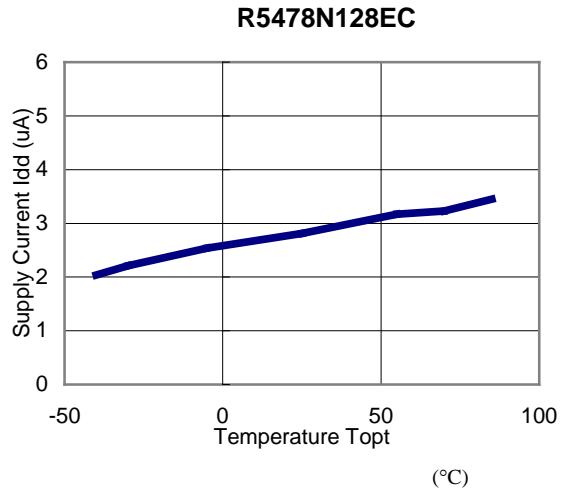
\* R5475N (SOT-23-5) is the discontinued product as of January, 2017.

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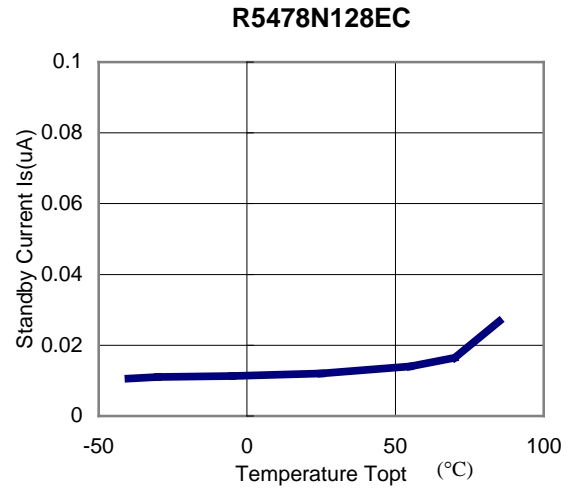
**R5475N/R5478Nxxxxx**

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19) Supply Current vs. Temperature  
Vdd=3.9V, V-=0V



20) Standby Current vs. Temperature  
Vdd=3.9V, V-=0V



\* R5475N (SOT-23-5) is the discontinued product as of January, 2017.

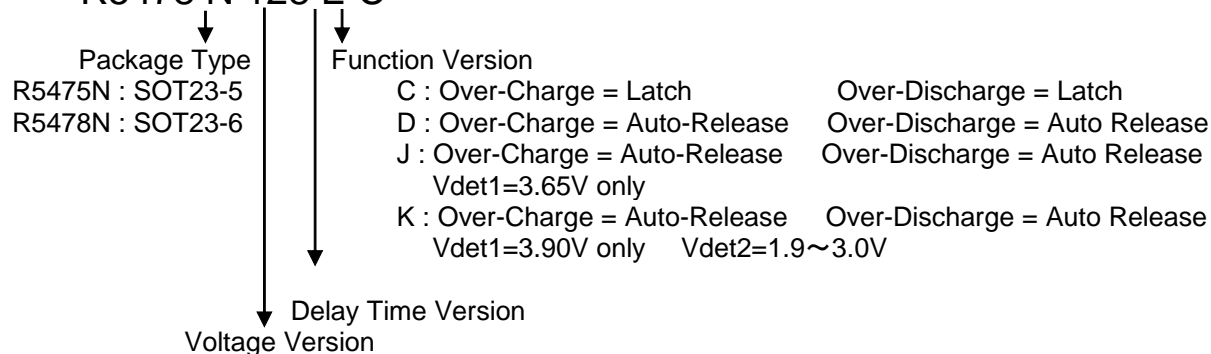
R5475N/R5478Nxxxxx

## R5475N/R5478N Series

Code	Vdet1 (V)	Vrel1 (V)	Vdet2 (V)	Vrel2 (V)	Vdet3 (V)	tVdet1 (s)	tVdet2 (ms)	tVdet3 (ms)	tShort ( $\mu$ s)	OV Charge	Package
R5478N128EC	4.280	-	2.800	-	0.050	1	20	6	200	OK	SOT-23-6
R5478N176EC	4.280	-	2.300	-	0.130	1	20	6	200	OK	SOT-23-6
R5478N101CD	4.250	4.050	2.500	3.000	0.200	1	20	12	300	OK	SOT-23-6
R5478N102CD	4.350	4.150	2.500	3.000	0.200	1	20	12	300	OK	SOT-23-6
R5478N106CD	4.275	4.075	2.300	3.000	0.100	1	20	12	300	OK	SOT-23-6
R5478N110CD	4.280	4.080	2.300	3.000	0.125	1	20	12	300	OK	SOT-23-6
R5478N120CD	4.325	4.125	2.300	3.000	0.150	1	20	12	300	OK	SOT-23-6
R5478N149CD	4.280	4.080	2.900	3.100	0.125	1	20	12	300	OK	SOT-23-6
R5478N163CD	4.280	4.100	3.000	3.200	0.100	1	20	12	300	OK	SOT-23-6
R5478N173CD	4.200	4.100	2.800	2.900	0.100	1	20	12	300	OK	SOT-23-6
R5478N187CD	4.250	4.050	3.000	3.200	0.150	1	20	12	300	OK	SOT-23-6
R5478N204CD	4.200	3.900	2.500	3.000	0.200	1	20	12	300	OK	SOT-23-6
R5478N205CD	4.200	3.900	3.000	3.200	0.200	1	20	12	300	OK	SOT-23-6
R5478N215CD	4.200	4.100	2.500	3.000	0.100	1	20	12	300	OK	SOT-23-6
R5478N216CD	4.170	4.170	2.500	3.000	0.100	1	20	12	300	OK	SOT-23-6
R5478N217CD	4.325	4.125	2.300	3.000	0.200	1	20	12	300	OK	SOT-23-6
R5478N218CD	4.250	4.050	2.800	3.000	0.150	1	20	12	300	OK	SOT-23-6
R5478N184CJ	3.650	3.650	2.500	3.000	0.200	1	20	12	300	OK	SOT-23-6
R5478N185CJ	3.650	3.450	2.500	3.000	0.200	1	20	12	300	OK	SOT-23-6
R5478N242CD	4.180	4.080	2.500	3.000	0.200	1	20	12	300	OK	SOT-23-6
R5478N248CD	4.280	4.080	2.300	2.800	0.150	1	20	12	300	OK	SOT-23-6
R5478N203CK	3.900	3.800	2.000	2.500	0.100	1	20	12	300	OK	SOT-23-6
R5475N110CD	4.280	4.080	2.300	3.000	0.125	1	20	12	300	OK	SOT-23-5

(as of 2012/07/04)

### R5478 N 128 E C



Code	Return from Over-Charge	Return from Over-Discharge	tVdet1 (s)	tVdet2 (ms)	tVdet3 (ms)	tShort ( $\mu$ s)
R5478N xxx EC	Latch	Latch	1	20	6	200
R5475N xxx CD	Auto-Release	Auto-Release	1	20	12	300
R5478N xxx CD	Auto-Release	Auto-Release	1	20	12	300
R5478N xxx CJ	Auto-Release	Auto-Release	1	20	12	300
R5478N xxx CK	Auto-Release	Auto-Release	1	20	12	300



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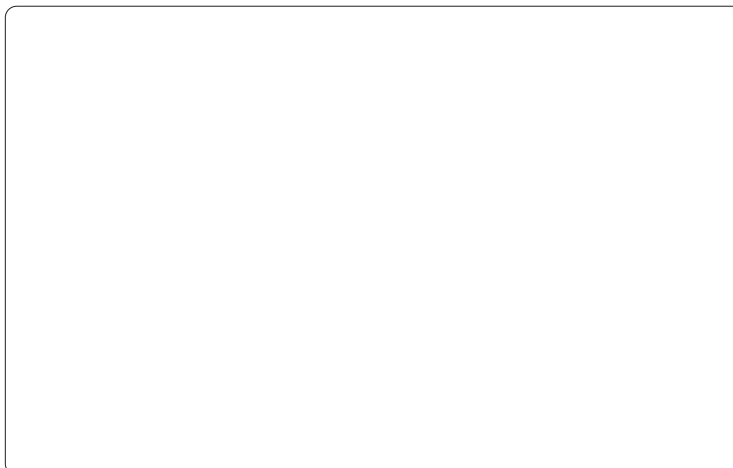
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