RICOH **R5650T Series**

3 to 5 Serial Cell Li-ion Battery Protection IC

NO.EA-401-200629

OUTLINE

The R5650T is an overcharge and discharge protection IC for 3- to 5- series cell Li-ion / Li-polymer rechargeable battery pack, further includes a short-circuit and protection circuits for charge / discharge overcurrent. The R5650T supports 3 to 5 cells connected in series, forcing a certain voltage on SEL1 and SEL2 pins can select any number of cells.

FEATURES

- High Voltage Tolerant Process
  - Absolute Maximum Ratings ……30 V
- Low Supply Current
  - Normal operation with using 5 cells ……Typ. 12.0 μA
  - Standby……Typ. 5.0 μA
- High-accuracy Voltage Detection
  - Overcharge detection voltage (V_{DET1n}[(1)]) ……3.6 V to 4.5 V (in 5 mV steps)
  - Overcharge detection voltage accuracy……± 25 mV (Ta = 25°C)
  - Overcharge release voltage……V_{DET1n} - 0.1V to V_{DET1n} - 0.4V (in 50mV steps)
  - Overdischarge detection voltage (V_{DET2n}[(1)]) ……2.0 V to 3.2 V (in 5 mV steps)
  - Overdischarge detection voltage accuracy……± 50 mV (Ta = 25°C)
  - Overdischarge release voltage……V_{DET2n} + 0.0 V to V_{DET2n} + 0.7 V (in 100mV steps) - provided, Max.value is 3.2 V.
  - Discharge overcurrent detection voltage1 (V_{DET31}) ……0.03 V to 0.10 V (in 10 mV steps)
  - Discharge overcurrent detection voltage accuracy……0.03 V to 0.05 V: ± 5 mV, 0.05 V to 0.10 V: ± 10%
  - Discharge overcurrent detection voltage2 (V_{DET32}) ……2 / 2.5 / 3 times V_{DET31}
  - Short-circuit detection voltage[(2)]……0.1 V to 0.6 V (in 20 mV steps)
  - Charge overcurrent detection voltage (V_{DET4})……-0.015 V to -0.025 V, -0.030 V to -0.050 V (in 5 mV steps)
  - Charge overcurrent detection voltage accuracy……-0.015 V to -0.025 V: ± 5 mV, -0.030 V to -0.050 V: ± 20%, or Disable
- Temperature Protection
  - Charge high-temperature (T_{DCH}) ……45 / 50 / 55 °C
  - Charge high-temperature accuracy ……± 5°C
  - Charge low-temperature (T_{DCL})……-5 / -3 / 0 °C
  - Charge low-temperature accuracy……± 3°C
  - Discharge high-temperature (T_{DDH})……70 / 75 °C
  - Discharge high-temperature accuracy……± 5°C

(1) V_{DET1n}: n =1, 2, 3, 4, 5
(2) V_{DET32} is not detected when V_{DET32} is higher than V_{SHORT}.

- Each Detection Delay Time
  - Overcharge detection delay time ·····1.0 sec
  - Overdischarge detection delay time settable by external capacitor
  - Discharge overcurrent detection delay time 1/2 settable by external capacitor
  - Charge overcurrent detection delay time ·····R5650TxxxAx: 256 ms
    R5650TxxxBx: 8 ms
  - Short-circuit detection delay time ·····Typ. 500 µs
- Selectable 0 V Battery Charging ·····Permit / Inhibition
- Overcharge Release Condition·····Voltage release type
- Overdischarge Release Condition·····Voltage release type
- 3 to 5 Cells Selectable Battery Protection
- Delay Time Shortening Function
- Temperature Protection by External NTC Thermistor
- Discharging Current Detection for Temperature Protection
- Package·····TSSOP-20 (EIJA: 225 MIL)

APPLICATIONS

■ Li-Ion or Li-Polymer Battery Protection for a power tool and cordless / robot vacuum cleaners.

SELECTION GUIDE

Set voltages, Delay times are, and Optional functions can be designated.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5650Txxx$∗-E2-FE	TSSOP-20	3,000 pcs	Yes	Yes

xxx: Specify the combination of the following set output voltages. Refer to *Product Code List* for details.

V_{DET1n} [(1)] : 3.6 V to 4.5 V in 5 mV steps
V_{REL1n} [(1)]: V_{DET1n} – 0.1 V to V_{DET1n} – 0.4 V in 50 mV steps
V_{DET2n} [(1)]: 2.0 V to 3.2 V in 5 mV steps
V_{REL2n} [(1)]: V_{DET2n} + 0.0 V to V_{DET2n} + 0.7 V in 100 mV steps (Max. 3.2 V)
V_{DET31}: 0.03 V to 0.10 V in 10 mV steps
V_{DET32}: 2 or 2.5 or 3 times V_{DET31}
V_{SHORT}: 0.1 V to 0.6 V in 20 mV steps
V_{DET4}: -0.015 V to -0.050 V, in 5 mV steps

$: Specify the charge overcurrent delay time (t_{VDET4}).

Delay Time Code Table

Code	t_{VDET4} (ms)
A	256
B	8

∗: Specify the combination of functions. Refer to *Function Code Table* for details.

Function Code Table

Code	Overcharge Detection	Overdischarge Detection	Charge Overcurrent	0V Battery Charging
A	Release	Release	Enable	Permit
B	Release	Release	Disable	Permit
C	Release	Release	Enable	Inhibition
D	Release	Release	Disable	Inhibition

(1) V_{DET1n}, V_{REL1n}, V_{CBDn}, V_{CBRn}, V_{DET2n}, V_{REL2n} : n =1, 2, 3, 4, 5

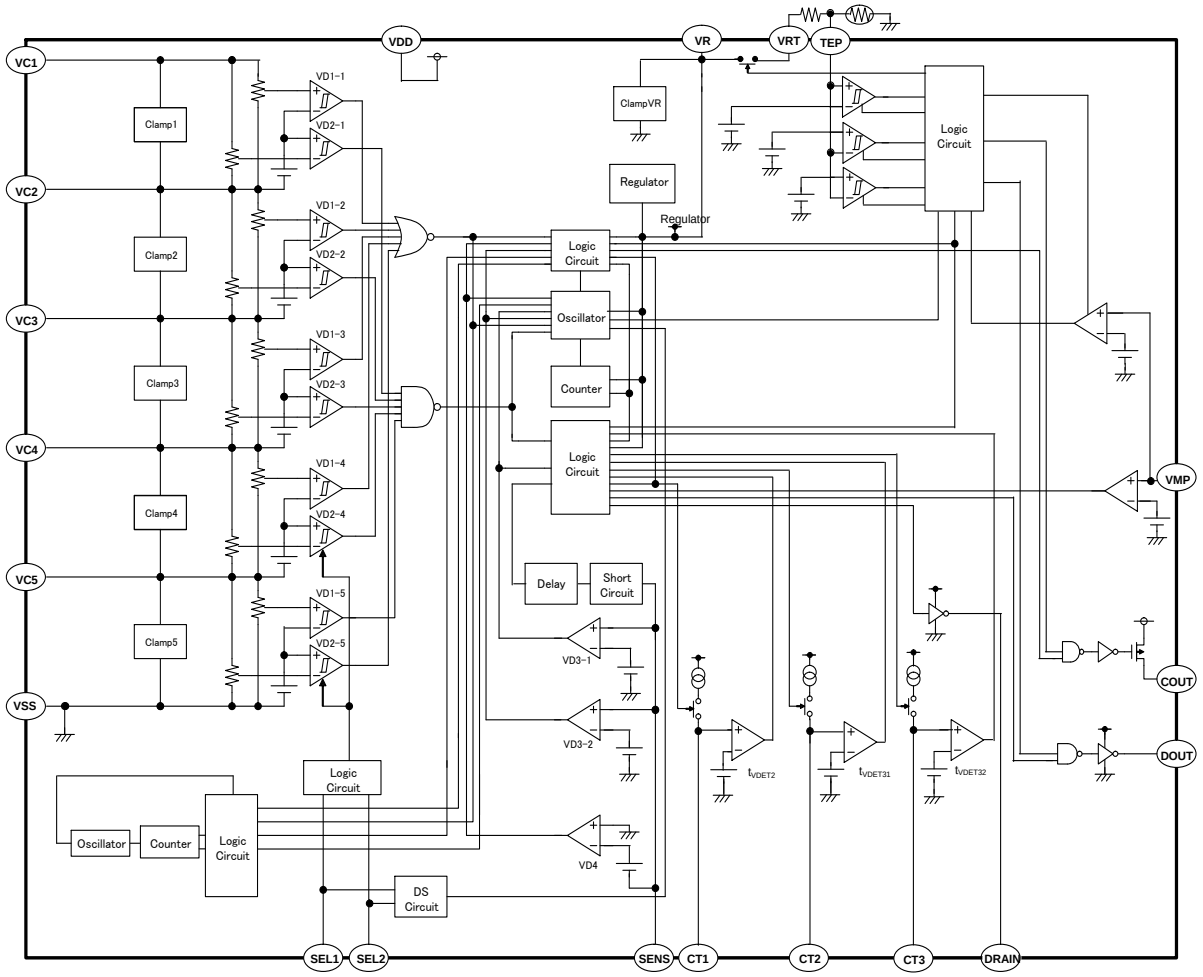
Product Code List

The product code is determined by the combination of the set output voltages (Overcharge detection/release voltage: V_{DET1n}/V_{REL1n}, Overdischarge detection/release voltage: V_{DET2n}/V_{REL2n}, Discharge overcurrent detection voltage1/2: V_{DET31}/V_{DET32}, Short-circuit detection voltage: V_{SHORT}, Charge overcurrent detection voltage: V_{DET4}) and the threshold temperatures for the temperature protection (Charge high-temperature: T_{DCH}, Charge low-temperature: T_{DCL}, Discharge high-temperature: T_{DDH}).

Product Code Table

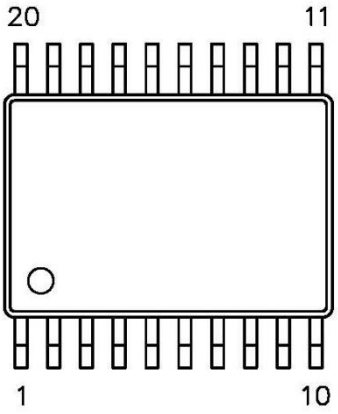
Product Name	Set Voltage (V)									Threshold Temperature(°C) [Release Temperature]		
	V_{DET1n}	V_{REL1n}	V_{DET2n}	V_{REL2n}	V_{DET31}	V_{DET32}	V_{SHORT}	V_{DET4}	V_{NOCHGN}	T_{DCH}	T_{DCL}	T_{DDH}
R5650T**401**AA	4.250	4.150	2.700	3.000	0.070	0.140	0.240	-0.050	—	45 [40]	0 [5]	70 [55]
R5650T**401**BC									0.9			
R5650T**402**AA	4.250	4.150	2.700	3.000	0.030	0.060	0.100	-0.015	—	45 [40]	-3 [2]	70 [55]
R5650T**402**BC									0.9			
R5650T**403**AA	4.400	4.250	2.700	3.000	0.100	0.300	0.420	-0.030	—	55 [50]	-3 [2]	70 [55]
R5650T**403**BC									0.9			
R5650T**404**BC	4.250	4.150	2.700	3.000	0.030	0.060	0.100	-0.015	1.3	45 [40]	-3 [2]	70 [55]
R5650T**405**AA	4.350	4.150	2.700	3.000	0.050	0.100	0.200	-0.040	—	55 [50]	-3 [2]	70 [55]
R5650T**406**AA	4.175	3.975	2.700	3.000	0.050	0.100	0.200	-0.040	—	55 [50]	-3 [2]	70 [55]
R5650T**407**BC	4.170	4.050	2.700	3.000	0.030	0.060	0.100	-0.015	1.3	45 [40]	-3 [2]	70 [55]
R5650T**408**BC	4.225	4.100	2.700	3.000	0.080	0.160	0.240	-0.015	0.9	50 [45]	0 [5]	70 [55]
R5650T**409**AA	4.220	4.120	2.700	3.000	0.070	0.140	0.240	-0.015	—	50 [45]	0 [5]	70 [55]
R5650T**410**AA	4.250	4.200	2.800	3.000	0.100	0.200	0.400	-0.015	—	50 [45]	-5 [0]	75 [60]
R5650T**411**AA	3.900	3.800	2.300	2.700	0.070	0.140	0.240	-0.035	—	50 [45]	-5 [0]	75 [60]
R5650T**412**AA	3.650	3.450	2.500	3.000	0.050	0.100	0.300	-0.030	—	55 [50]	0 [5]	75 [60]

BLOCK DIAGRAM



R5650T Block Diagram

PIN DESCRIPTIONS



TSSOP-20 Pin Configuration

Pin No	Symbol	Pin Description
1	VDD	VDD pin
2	VC1	Positive terminal pin for CELL1
3	VC2	Positive terminal pin for CELL 2
4	VC3	Positive terminal pin for CELL 3
5	VC4	Positive terminal pin for CELL 4
6	VC5	Positive terminal pin for CELL 5
7	VSS	VSS / Ground pin for the IC
8	SENS	Current sense pin
9	DRAIN	Discharge overcurrent release output pin
10	DOUT	Overdischarge detection output pin, CMOS output
11	COUT	Overcharge detection output pin, Pch. Open-drain output
12	VMP	Charger negative input pin
13	CT1	Capacitor connection pin for t_{VDET2} setting
14	CT2	Capacitor connection pin for t_{VDET31} setting
15	CT3	Capacitor connection pin for t_{VDET32} setting
16	TEP	Temperature protection input pin
17	VRT	Thermistor reference voltage pin
18	VR	Internal VR output pin
19	SEL1	3- / 4- / 5-cell selectable pins
20	SEL2	

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (Ta = 25°C, VSS = 0 V)

Symbol	Item	Rating	Unit
V_{DD}	Power Supply Voltage	−0.3 to 30	V
V_{VC1}	VC1 Pin Input Voltage for CELL1	V_{VC2} - 0.3 to V_{VC2} + 6.5	V
V_{VC2}	VC2 Pin Input Voltage for CELL2	V_{VC3} - 0.3 to V_{VC3} + 6.5	V
V_{VC3}	VC3 Pin Input Voltage for CELL3	V_{VC4} - 0.3 to V_{VC4} + 6.5	V
V_{VC4}	VC4 Pin Input Voltage for CELL4	V_{VC5} - 0.3 to V_{VC5} + 6.5	V
V_{VC5}	VC5 Pin Input Voltage for CELL5	- 0.3 to + 6.5	V
V_{VMP}	VMP Pin Input Voltage	V_{DD} - 30 to V_{DD} + 0.3	V
V_{SEL1}	SEL1 Pin Input Voltage	−0.3 to V_{DD} + 0.3	V
V_{SEL2}	SEL2 Pin Input Voltage	−0.3 to V_{DD} + 0.3	V
V_{SENS}	SENS Pin Input Voltage	V_{DD} - 30 to V_{VR} + 0.3	V
V_{CT1}	CT1 Pin Input Voltage	−0.3 to V_{VR} + 0.3	V
V_{CT2}	CT2 Pin Input Voltage	−0.3 to V_{VR} + 0.3	V
V_{CT3}	CT3 Pin Input Voltage	−0.3 to V_{VR} + 0.3	V
V_{TEP}	TEP Pin Input Voltage	−0.3 to V_{VR} + 0.3	V
V_{COUT}	COUT Pin Output Voltage	V_{DD} - 30 to V_{DD} + 0.3	V
V_{DOUT}	DOUT Pin Output Voltage	−0.3 to V_{OH2} + 0.3	V
V_{DRAIN}	DRAIN Pin Output Voltage	−0.3 to V_{OH3} + 0.3	V
V_{VR}	VR Pin Output Voltage	−0.3 to VR + 0.3	V
V_{VRT}	VRT Pin Output Voltage	−0.3 to VR + 0.3	V
P_D	Power Dissipation	Refer to Appendix “Power Dissipation”	
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITION

Symbol	Item	Rating	Unit
V_{DD}	Operating Input Voltage	4.0 to 25.0	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{CELLn} n = 1, 2, 3, 4, 5 (Ex. V_{CELL1} is a voltage difference between VC1 and VC2), unless otherwise noted.

R5650T Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Conditions		Ratings Min.	Ratings Typ.	Ratings Max.	Unit	Circuit (1)
V_{DET1n}	CELLn overcharge detection voltage	at rising edge of supply voltage		V_{DET1n} -0.025	V_{DET1n}	V_{DET1n} +0.025	V	A
V_{REL1n}	CELLn overcharge release voltage	at falling edge of supply voltage		V_{REL1n} -0.050	V_{REL1n}	V_{REL1n} +0.050	V	A
t_{VDET1}	Overcharge detection delay time	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{CELL1} = 3.4 V → V_{DET1n}+0.2 V		0.7	1.0	1.3	s	B
t_{VREL1}	Overcharge release delay time	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{CELL1} = V_{DET1n}+0.2 V→ 3.4 V		11	16	21	ms	B
V_{DET2n}	CELLn overdischarge detection voltage	Detect falling edge of supply voltage		V_{DET2n} -0.050	V_{DET2n}	V_{DET2n} +0.050	V	C
V_{REL2n}	CELLn overdischarge release voltage	Detect rising edge of supply voltage		V_{REL2n} -0.050	V_{REL2n}	V_{REL2n} +0.050	V	C
I_{CT1}	CT1 pin charge current	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{CELL1} = 3.4 V →1.5 V		350	500	650	nA	D
V_{DCT1}	CT1 pin detection voltage	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{CELL1} = 1.5 V		1.44	1.80	2.16	V	E
t_{VDET2}	Overdischarge detection delay time	$t_{VDET2} = C_{CT1} \times V_{DCT1} / I_{CT1}$, C_{CT1} = 33 nF		83	119	155	ms	-
t_{VREL2}	Overdischarge release delay time	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{CELL1} = 1.5 V → 3.4 V		0.7	1.1	1.7	ms	F
V_{DET31}	Discharge overcurrent detection voltage1	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V V_{MP} = 4.0 V, at rising edge of SENS	V_{DET31} < 0.05	V_{DET31} -0.005	V_{DET31}	V_{DET31} +0.005	V	G
			V_{DET31} ≥ 0.05	V_{DET31} -10%		V_{DET31} +10%		
V_{DET32}	Discharge overcurrent detection voltage2	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4V V_{VMP} = 4.0 V, at rising edge of SENS	V_{DET32} < 0.1	V_{DET32} -0.0125	V_{DET32}	V_{DET32} +0.0125	V	H
			V_{DET32} ≥ 0.1	V_{DET32} -12.5%		V_{DET32} +12.5%		
V_{REL3}	Discharge overcurrent release voltage	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V V_{SENS} = 0 V, at falling edge of VMP		0.8	1.0	1.2	V	G
I_{CT2}	CT2 pin charge current	$V_{DD} = V_{VC1}$, V_{CELLn} = 3.4 V V_{SENS} = 0 V → V_{DET31} + 0.02 V		350	500	650	nA	H

(1) Refer to *TEST CIRCUITS* for detail information.

V_{CELLn} n = 1, 2, 3, 4, 5 (Ex. V_{CELL1} is a voltage difference between VC1 and VC2), unless otherwise noted.

R5650T Electrical Characteristics (continued) (Ta = 25°C)

Symbol	Parameter	Conditions	Ratings Min.	Ratings Typ.	Ratings Max.	Unit	Circuit (1)
V_{DCT2}	CT2 pin charge detection voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{SENS} = V_{DET31} + 0.02 V V_{MP} = 4.0 V	1.20	1.50	1.80	V	I
I_{CT3}	CT3 pin charge current	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V V_{SENS} = 0 V →V_{DET31} + 0.02 V	2.0	3.0	4.0	µA	J
V_{DCT3}	CT3 pin charge detection voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5) V_{SENS} = V_{DET32} + 0.02 V, V_{MP} = 4.0 V	1.20	1.50	1.80	V	K
t_{VDET31}	Discharge overcurrent delay time1	t_{VDET31} = C_{CT2} ×V_{DCT2} / I_{CT2} C_{CT2} = 3.3 nF	6.9	9.9	12.9	ms	-
t_{VDET32}	Discharge overcurrent delay time2	t_{VDET32} = C_{CT3} ×V_{DCT3} / I_{CT3} C_{CT3} = 3.3 nF	1.15	1.65	2.15	ms	-
t_{VREL3}	Discharge overcurrent release delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V V_{SENS} = V_{SS}, V_{MP} = 4.0 V → VSS	0.7	1.1	1.7	ms	I
V_{SHORT}	Short protection voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{MP} = 4.0 V, at rising edge of SENS	V_{SHORT} ×0.8	V_{SHORT}	V_{SHORT} ×1.2	V	L
t_{SHORT}	Short protection delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V V_{SENS} = 0 V → 2.0 V, VMP = 4.0 V	350	500	650	µs	L
V_{DET4}	Charge overcurrent detection voltage4	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{MP} = −1.0 V, at falling edge of SENS; V_{DET4} ≥ -0.025	V_{DET4} -0.005	V_{DET4}	V_{DET4} +0.005	V	M
		V_{DET4} < -0.025	V_{DET4} -20%		V_{DET4} +20%		
V_{REL4}	Charge overcurrent release voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, at rising edge of VMP	0.05	0.1	0.15	V	M
t_{VDET4}	Charge overcurrent delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{SENS} = 0 V→−1.0 V	t_{VDET4} -37.5%	t_{VDET4}	t_{VDET4} +37.5%	ms	M
t_{VREL4}	Charge overcurrent release delay time	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{SENS} = V_{SS}, V_{MP} = −1.0 V →1.0 V	0.7	1.1	1.7	ms	M
V_{IH1}	SEL1 pin input voltage, high	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{DD} - 0.3 V		V_{DD} + 0.3 V	V	N
V_{IM1}	SEL1 pin input voltage, middle	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	4.0		V_{DD}/2 - 0.5 V	V	N
V_{IL1}	SEL1 pin input voltage, low	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{SS} - 0.3 V		V_{SS} + 0.3 V	V	N

(1) Refer to *TEST CIRCUITS* for detail information.

V_{CELLn} n = 1, 2, 3, 4, 5 (Ex. V_{CELL1} is a voltage difference between VC1 and VC2), unless otherwise noted.

R5650T Electrical Characteristics (continued) (Ta = 25°C)

Symbol	Parameter	Conditions	Ratings			Unit	Circuit (1)
V_{IH2}	SEL2 pin input voltage, high	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{DD} - 0.3 V		V_{DD} + 0.3 V	V	O
V_{IM2}	SEL2 pin input voltage, middle	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	4.0		V_{DD}/2 - 0.5 V	V	O
V_{IL2}	SEL2 pin input voltage, low	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{SS} - 0.3 V		V_{SS} + 0.3 V	V	O
V_{OL2}	DOUT pin Nch. ON voltage	I_{OL} = 50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V		0.02	0.10	V	P
V_{OL3}	DRAIN pin Nch. ON voltage	I_{OL} = 50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V		0.04	0.20	V	Q
V_{OH1}	COUT pin Pch. ON voltage	I_{OH} = −50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{DD} - 0.5 V	V_{DD} - 0.1 V		V	R
V_{VR12}	VR12V output voltage	I_{OH} = −5 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V Measured to draw the current through D_{OUT}	9.5	12	14	V	S
V_{OH2}	DOUT pin Pch ON voltage(2)	I_{OH} = −50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	V_{VR12} - 0.5 V	V_{VR12} - 0.1 V		V	S
V_{OH3}	DRAIN pin Pch. ON voltage(2)	I_{OH} = −50 µA, V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V V_{SENS} = V_{MP} = 4.0 V	V_{VR12} - 0.5 V	V_{VR12} - 0.1 V		V	T
I_{LCOUT}	COUT pin off-leakage current	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, C_{OUT} = −13 V	-0.1			µA	U
V_{VR}	VR pin output voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	3.5	3.6	3.7	V	V
V_{VRT}	VRT pin output voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V I_{VRT} = -80µA	3.47	3.57	3.67	V	W
T_{DCH}	Detection temperature for charge high-temperature	V_{DD} = V_{C1}, V_{CELLn} = 3.4 V	T_{DCH} -5	T_{DCH}	T_{DCH} +5	°C	X
T_{RCH}	Release temperature for charge high-temperature	V_{DD} = V_{C1}, V_{CELLn} = 3.4 V	T_{DCH} -10	T_{DCH} -5	T_{DCH}	°C	X
t_{DCHT}	Detection delay time for charge high-temperature	V_{DD} = V_{C1}, V_{CELLn} = 3.4 V, V_{TEP} = 0.9 V → 0.3 V	42	60	78	ms	X
t_{RCHT}	Release delay time for charge high-temperature	V_{DD} = V_{C1}, V_{CELLn} = 3.4 V, V_{TEP} = 0.3 V → 0.9 V	42	60	78	ms	X

(1) Refer to *TEST CIRCUITS* for detail information.

(2) If the VDD pin voltage becomes lower than the output of the regulator, the output voltage (DOUT, DRAIN) becomes almost equal to V_{DD}.

V_{CELLn} n = 1, 2, 3, 4, 5 (Ex. V_{CELL1} is a voltage difference between VC1 and VC2), unless otherwise noted.

R5650T Electrical Characteristics (continued) (Ta = 25°C)

Symbol	Parameter	Conditions	Ratings			Unit	Circuit (1)
T_{DCL}	Detection temperature for charge low-temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DCL} -3	T_{DCL}	T_{DCL} +3	°C	X
T_{RCL}	Release temperature for charge low-temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DCL} +2	T_{DCL} +5	T_{DCL} +8	°C	X
t_{DCLT}	Detection delay time for charge low-temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{TEP} = 0.9 V → 3.5 V	42	60	78	ms	X
t_{RCLT}	Release delay time for charge low-temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{TEP} = 3.5 V → 0.9 V	42	60	78	ms	X
T_{DDH}	Detection temperature for discharge high-temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DDH} -5	T_{DDH}	T_{DDH} +5	°C	X
T_{RDH}	Release temperature for discharge high-temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	T_{DDH} -20	T_{DDH} -15	T_{DDH} -10	°C	X
t_{DDHT}	Detection delay time for discharge high-temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{TEP} = 0.9 V → 0 V	42	60	78	ms	X
t_{RDHT}	Release delay time for discharge high-temperature	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V, V_{TEP} = 0 V → 0.9 V	42	60	78	ms	X
t_{VTT}	Temperature scanning cycle	V_{DD} = V_{VC1}, V_{CELLn} = 3.4 V	0.7	1	1.3	s	Y
V_{DSG}	Discharge state detection voltage	(V_{MP} – V_{SS}) Detect rising edge of VMP	5	10	15	mV	a
V_{NOCHGn}	0V battery charge inhibition voltage	V_{DD} = V_{VC1}, V_{CELLn} = 3.2 V	V_{NOCHGn} -0.2	V_{NOCHGn}	V_{NOCHGn} +0.2	V	A
I_{SS1}	Supply current 1	V_{DD} = V_{VC1}, C_{OUT} = OPEN V_{CELLn} = V_{DET1}n - 0.4 V		12	25	µA	Z
I_{SS2}	Supply current 2	V_{DD} = V_{VC1}, C_{OUT} = OPEN V_{CELLn} = 1.5 V		5	9	µA	Z
V_{STB}	Standby mode threshold voltage	V_{DD} = V_{VC1} = 1.5 V, V_{CELLn} = 3.4 V (n = 2, 3, 4, 5), Detect rising edge of VMP	0.9	1.13	1.35	V	G

(1) Refer to *TEST CIRCUITS* for detail information.

TEST CIRCUITS

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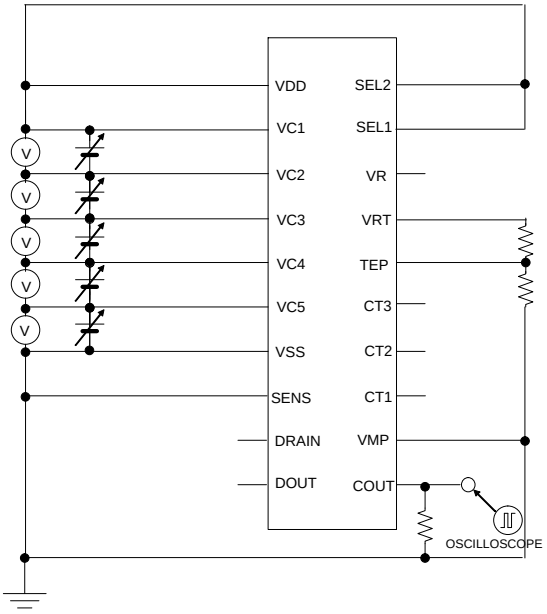

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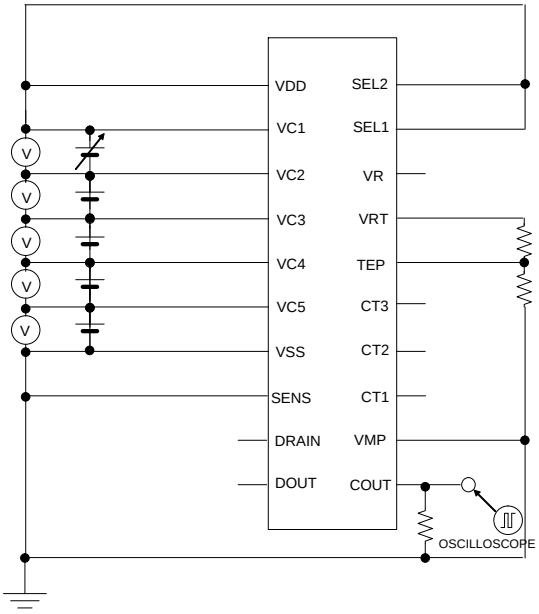

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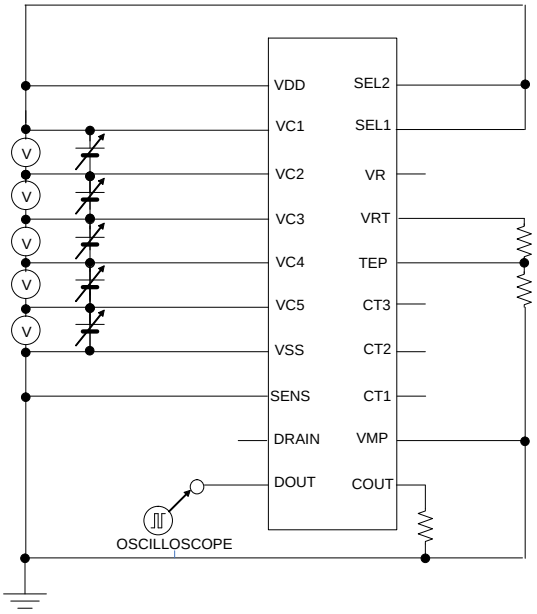

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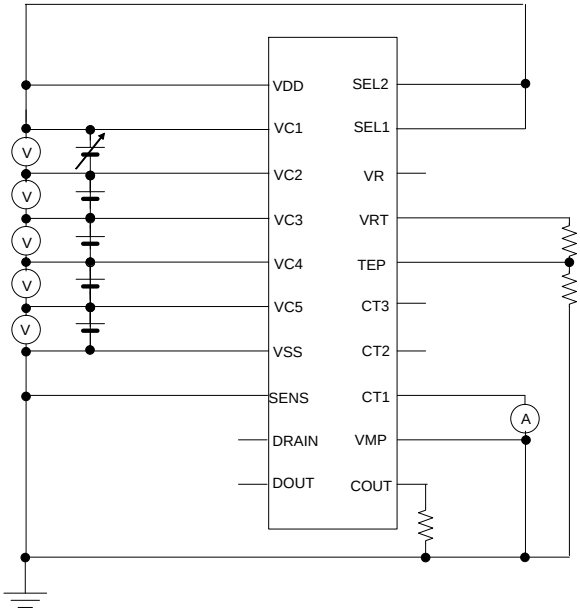

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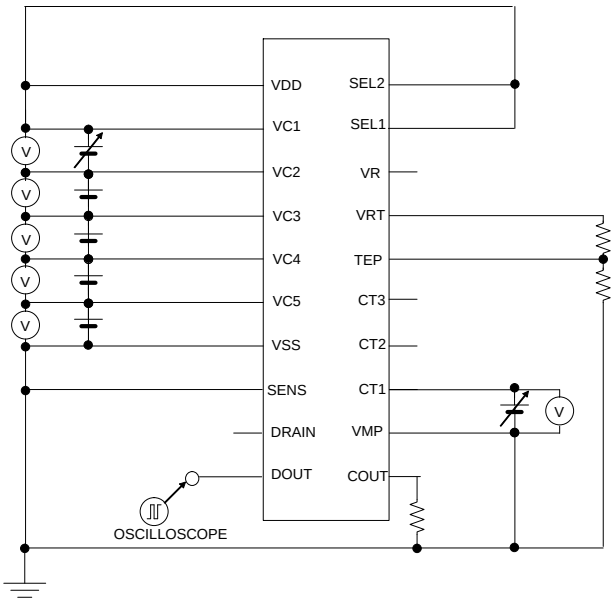
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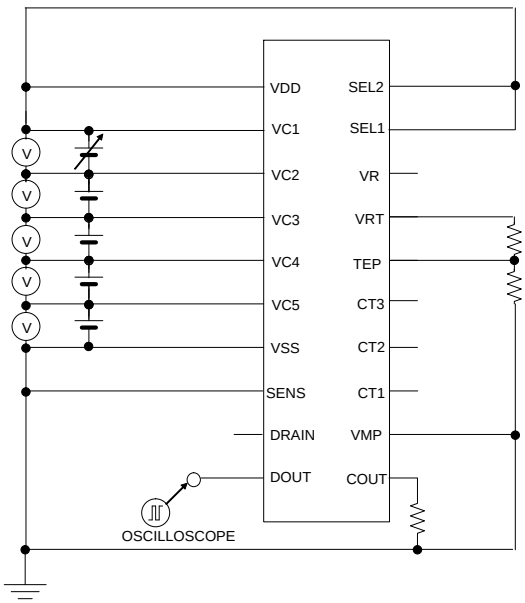
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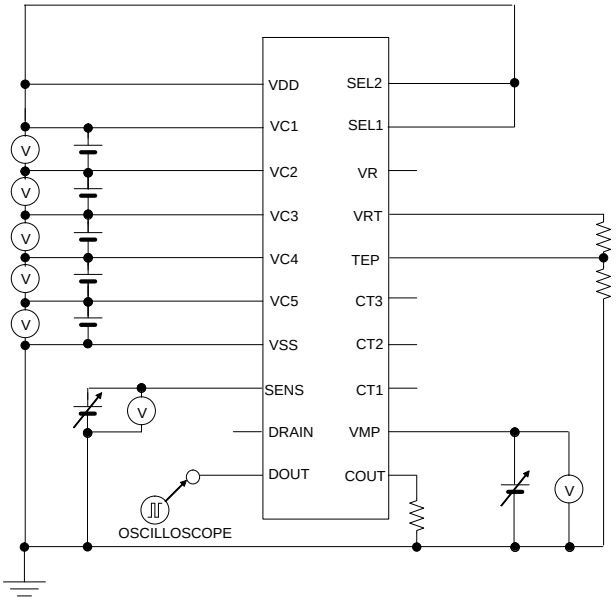
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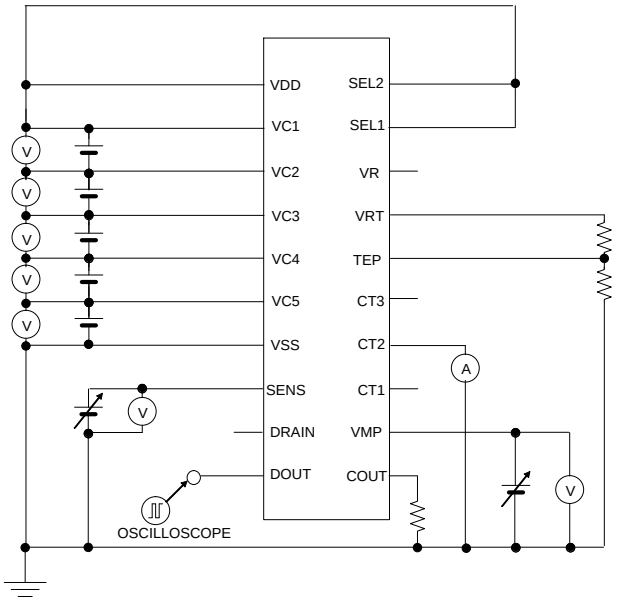
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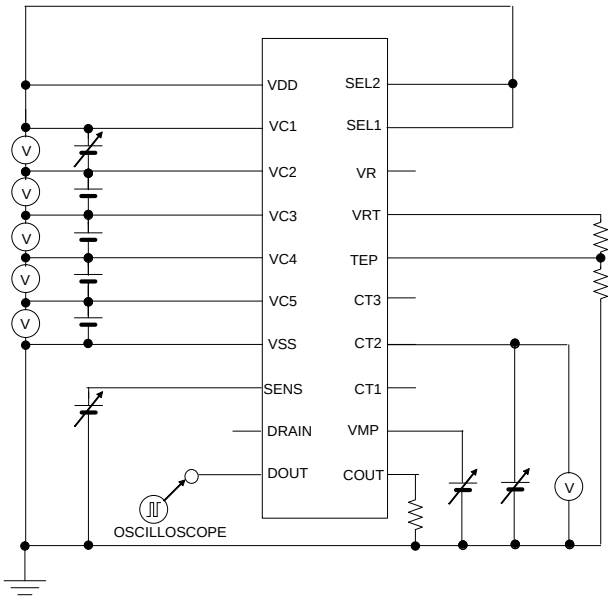
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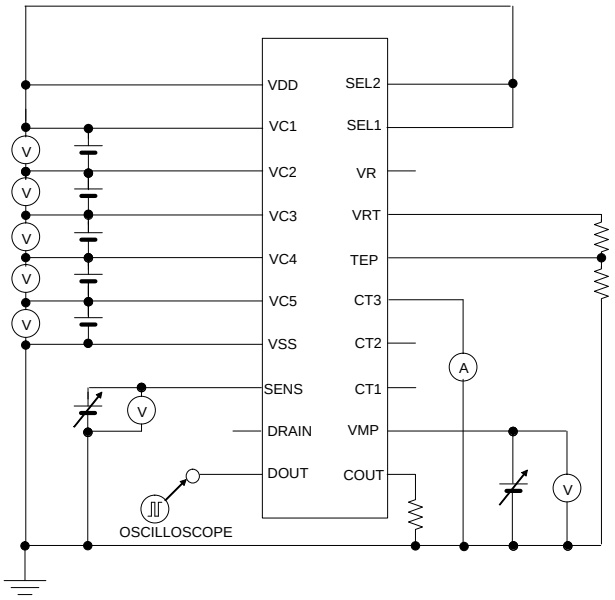
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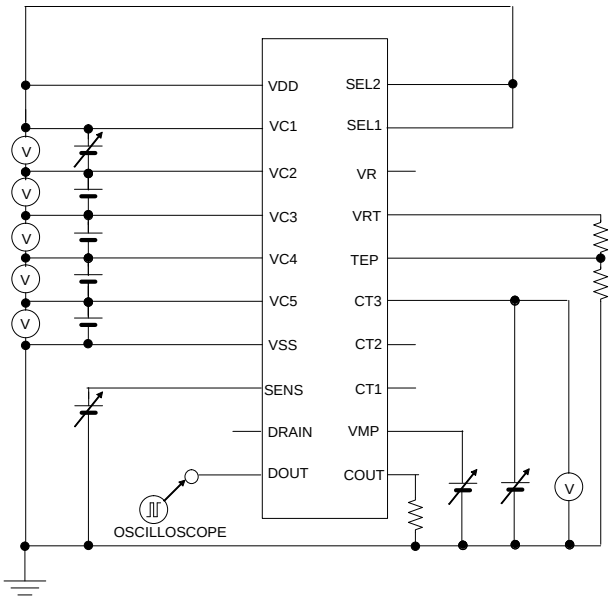
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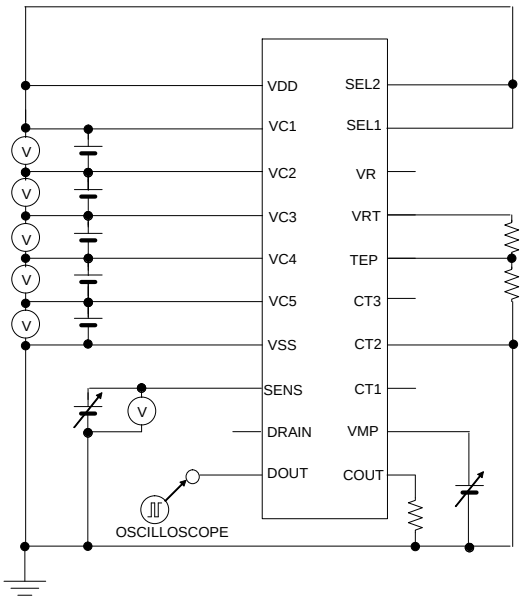
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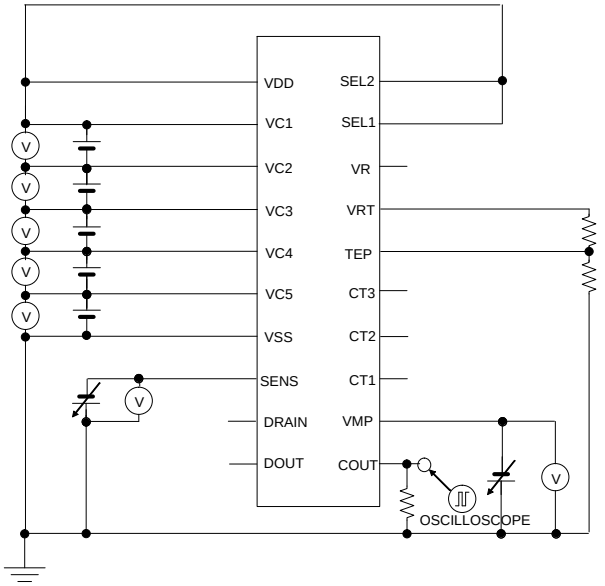
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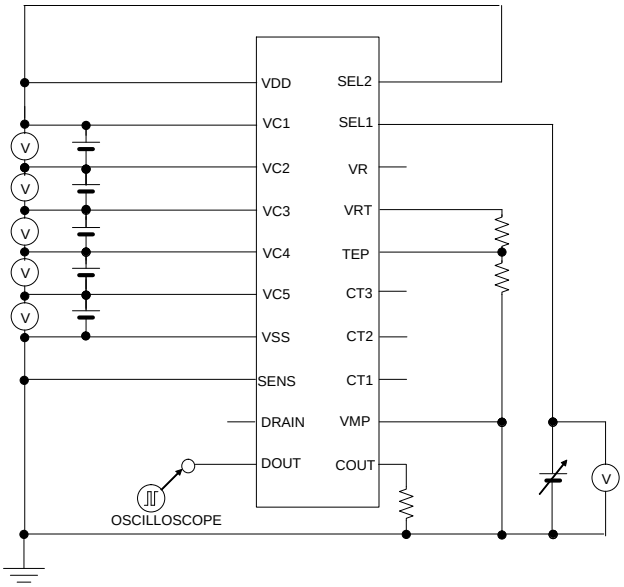
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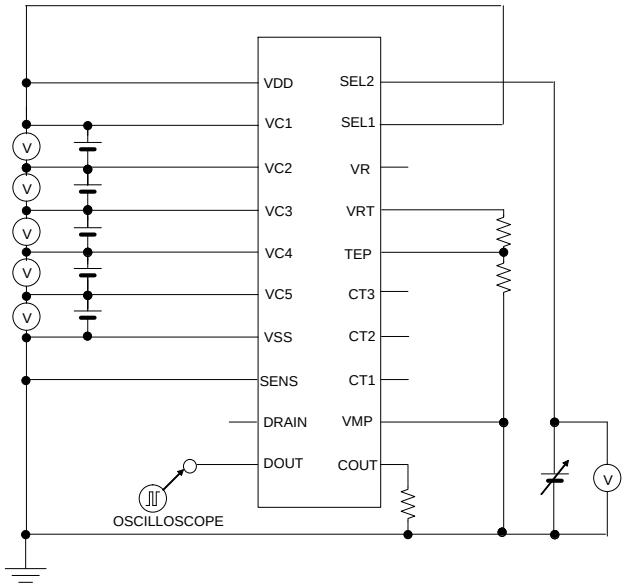
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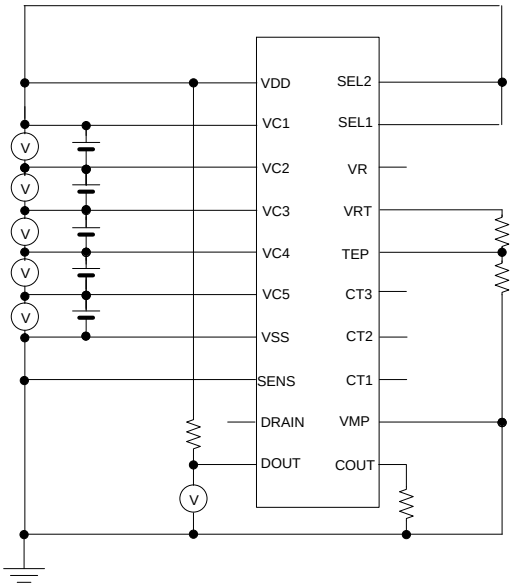
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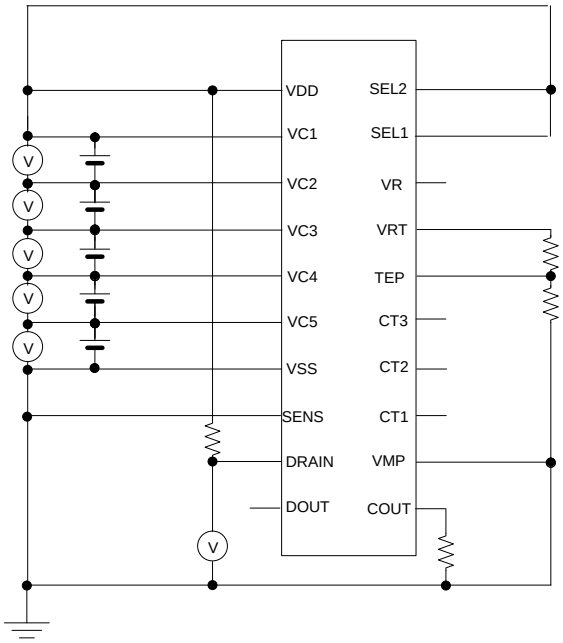
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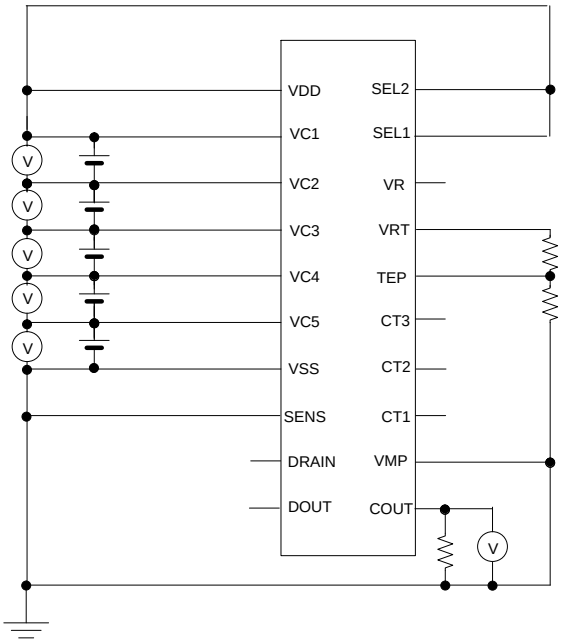
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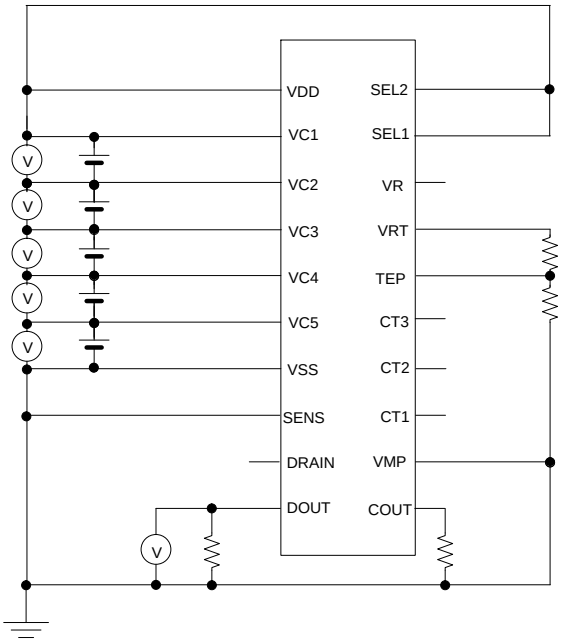
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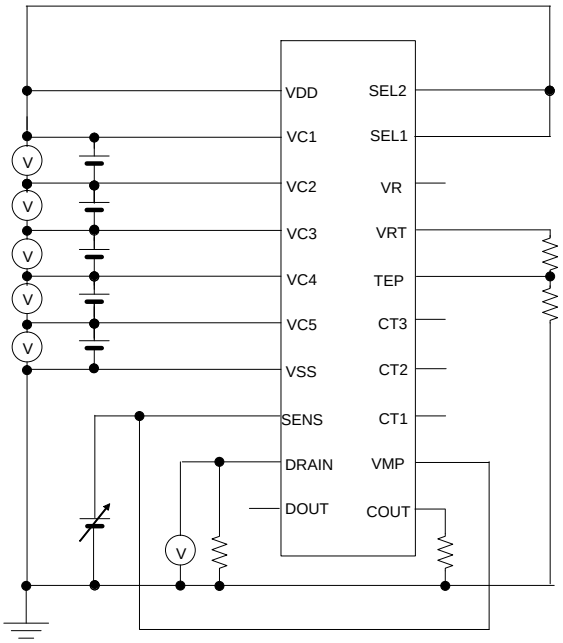
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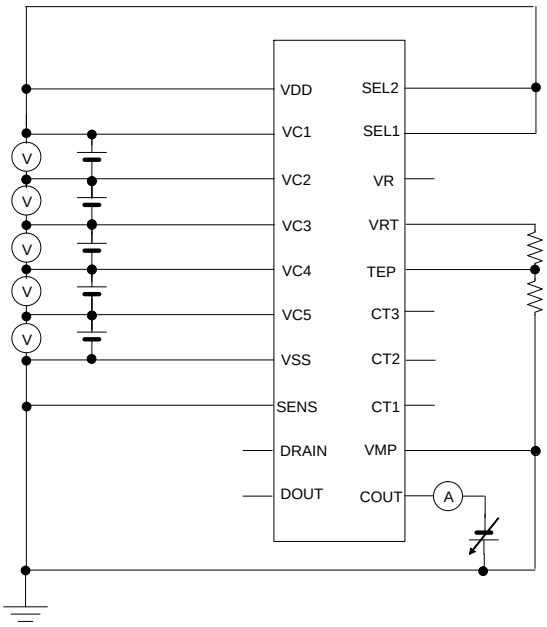
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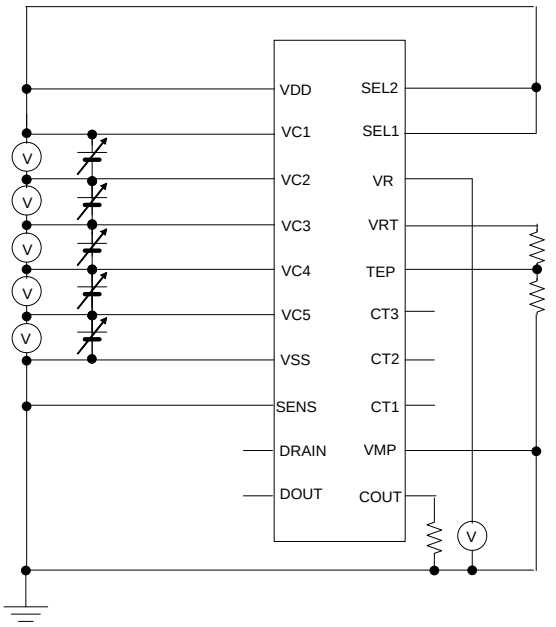
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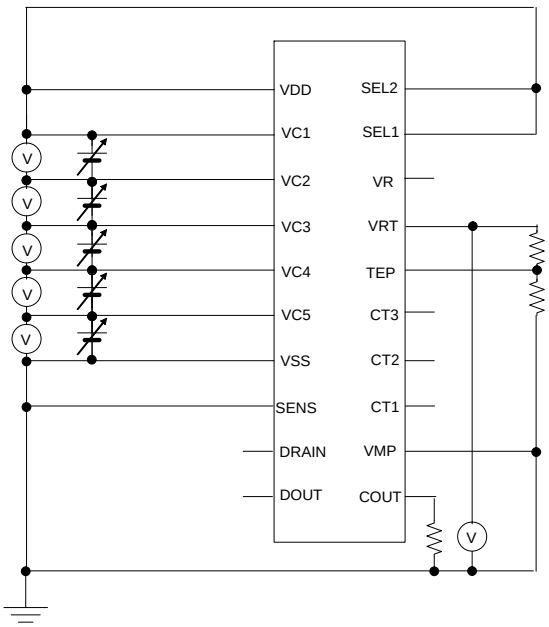
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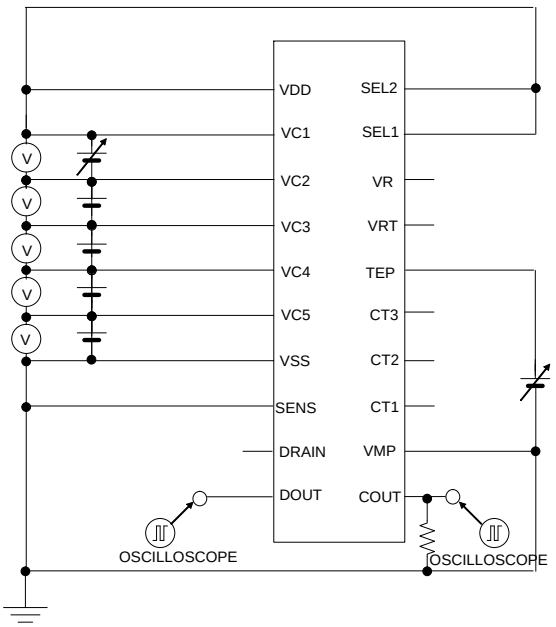
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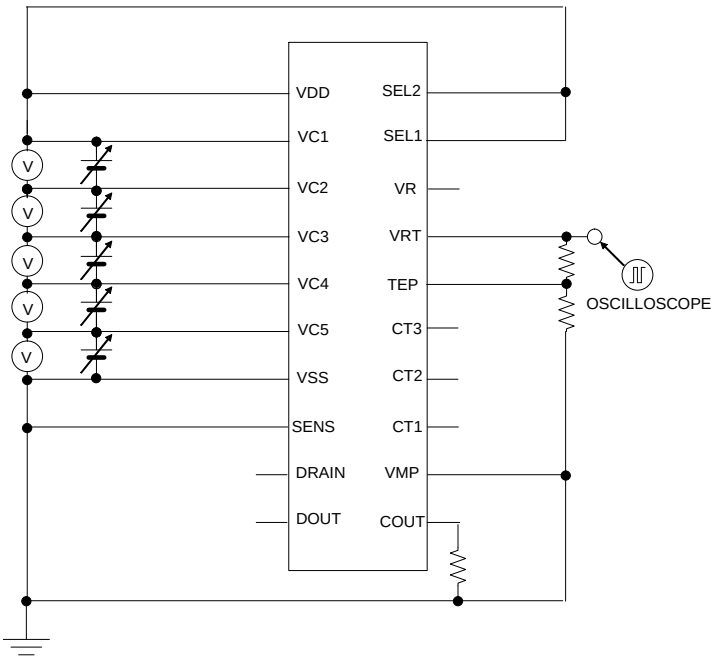
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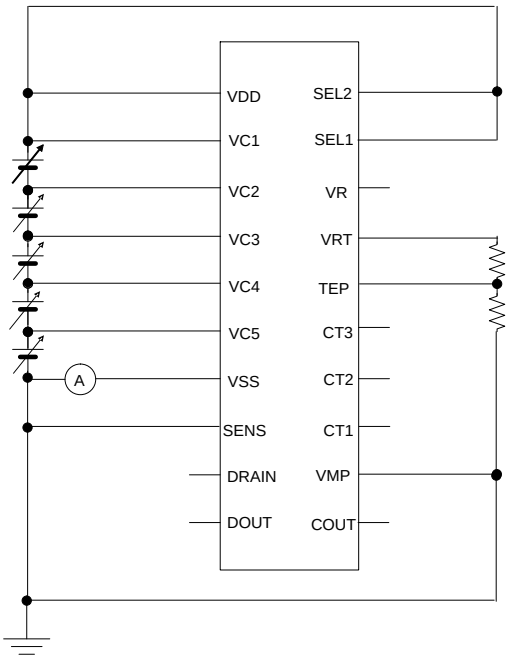
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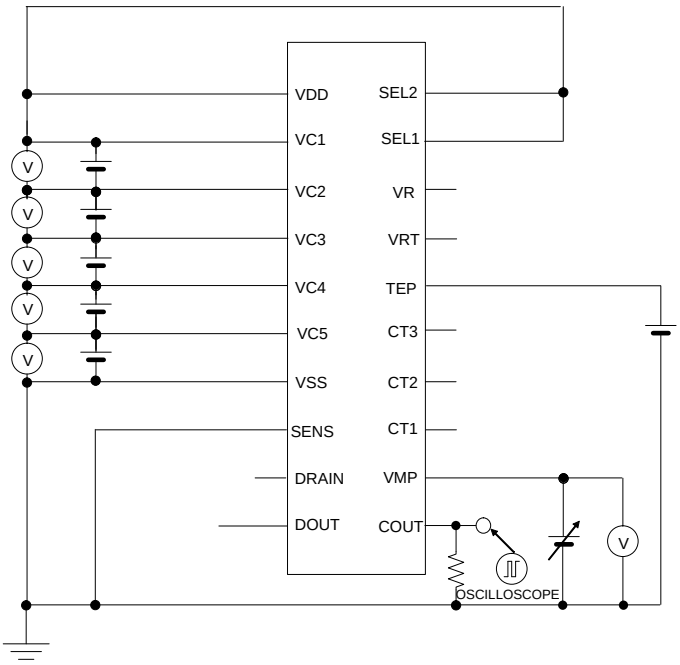
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THEORY OF OPERATION

Overcharge Detector: VD1n (n = 1, 2, 3, 4, 5)

During charging, the R5650T supervises the CELL1 voltage (V_{CELL1}) between VC1 and VC2 pins, the CELL2 voltage (V_{CELL2}) between VC2 and VC3 pins, the CELL3 voltage (V_{CELL3}) between VC3 and VC4 pins, the CELL4 voltage (V_{CELL4}) between VC4 and VC5 pins, and the CELL5 voltage (V_{CELL5}) between VC5 and VSS pins. If at least one of the cells' voltage becomes more than the overcharge detection voltage (V_{DET1n}), the overcharge is detected, and COUT pin connected to an external pull-down resistor becomes "Hi-z", and it makes the external FET turn off. Then, the charging stops.

After detecting the overcharge, when the VMP pin input voltage (V_{VMP}) becomes higher than the charge overcurrent release voltage (V_{REL4}) by taking off the charger and connecting a load, all the cell voltage become lower than V_{DET1n}, then COUT pin becomes "High", and then the charging is available. Likewise, when V_{VMP} becomes lower than V_{REL4} and all the cell voltage become lower than V_{REL1n}, COUT pin becomes "High" and then the charging is available.

The device has internal fixed delay times for overcharge detection and overcharge release. When the delay time passes while any one of cell voltages (V_{CELLn}) is more than V_{DET1n}, the overcharge is detected. However, all cell voltage (V_{CELLn}) becomes lower than V_{DET1n} within the overcharge detection delay time (t_{VDET1}), the overcharge is not detected.

Besides, if the release conditions do not hold within the overcharge release delay time (t_{VREL1}) even though the release conditions hold once after detecting the overcharge, the device cannot release from the overcharge.

Since COUT pin is a Pch. open-drain type, a "High" level of COUT pin is as same potential as the VDD pin voltage (V_{DD}).

Overdischarge Detector: VD2n (n = 1, 2, 3, 4, 5)

During discharging, the R5650T supervises V_{CELL1}, V_{CELL2}, V_{CELL3}, V_{CELL4}, and V_{CELL5} as same as charging. If at least one of the cell voltages becomes less than the overdischarge detection voltage (V_{DET2n}), the overdischarge is detected, and DOUT pin becomes "Low". Then, the external FET is turned off and the discharging stops.

The overdischarge detection is released even if the charger is not connected when the all cell voltage (V_{CELLn}) becomes higher than V_{REL2n}, and then DOUT pin becomes "High".

The overdischarge detection delay time (t_{VDET2}) is settable by the external capacitor (C_{CT1}) connected to CT1 pin. When the delay time passes while any one of cell voltages (V_{CELLn}) is lower than V_{DET2n}, the overdischarge is detected. However, all cell voltage (V_{CELLn}) becomes higher than V_{DET2n} within t_{VDET2}, the overdischarge is not detected. The overdischarge release delay time (t_{VREL2}) is fixed internally.

After detecting the overdischarge, the device stops unnecessary circuits to reduce the supply current to a minimum when VMP pin becomes "High". DOUT pin, which is a CMOS output, outputs the internal regulator's voltage (about 12 V) when "High" level and outputs the VSS pin voltage (V_{SS}) when "Low" level.

Discharge Overcurrent Detector: VD3 (n = 1, 2), Short-circuit Protector

During charging and discharging, the R5650T supervises SENS pin voltage (V_{SENS}). The discharge overcurrent is detected when V_{SENS} becomes in between the discharge overcurrent detection voltage (V_{DET3n}) and the short-circuit detection voltage (V_{SHORT}) owing to a large load, and the short-circuit is detected when V_{SENS} becomes more than V_{SHORT}. Then, to prevent from flowing large current to circuits, DOUT pin is set to “Low” and the external FET is turned OFF.

The device has two detection voltages (V_{DET31}, V_{DET32}) to detect the discharge overcurrent. Each detection voltages (V_{DET31}, V_{DET32}) has the delay time each other. The discharge overcurrent detection delay time 2 (t_{VDET32}) is set to be shorter than the discharge overcurrent detection delay time 1 (t_{VDET31}).

The discharge overcurrent detection delay time 1 (t_{VDET31}) are settable by the external capacitor (C_{CT2}) connected to CT2 pin. Likewise, the discharge overcurrent detection delay time2 (t_{VDET32}) is settable by the C_{CT3} connected to CT3 pin. When V_{SENS} becomes lower than V_{DET3n} within the delay time, the discharge overcurrent is not detected. The discharge overcurrent release delay time (t_{VREL3}) and the short-circuit detection delay time (t_{SHORT}) are fixed internally.

An external resistor for discharge overcurrent release must be mounted among each drain of the external FETs connected to DRAIN, COUT, and DOUT pins. After detecting the discharge overcurrent or the short-circuit, the external FET connected to DRAIN pin is turned ON, and the resistor for overcurrent release is connected to VSS.

When a load is removed after detecting the discharge overcurrent or the short-circuit, the VMP pin voltage (V_{VMP}) is pulled down to VSS via the resistor for the overcurrent release, and V_{VMP} becomes less than V_{REL3}. After a certain delay time, the discharge overcurrent detection state or the short-circuit protection state is released. When the discharge overcurrent detection is released, the external FET connected to DRAIN pin is turned OFF, and the resistor for the overcurrent release is disconnected from VSS.

Charge Overcurrent Detector: VD4

During charging or discharging, the R5650T supervises the SENS pin voltage (V_{SENS}). When an inappropriate current flow by an inappropriate charger, V_{SENS} becomes less than the charge overcurrent detection voltage, and the charge overcurrent is detected. And, COUT pin with the external pull-down resistor becomes “Hi-z”. Tuning OFF the external FET can prevent from flowing large current to circuits.

When SENS pin voltage (V_{SENS}) becomes higher than V_{DET4} within the delay time, the charge overcurrent is not detected. The output delay times for charge overcurrent detection and charge overcurrent release are fixed internally.

The VMP pin voltage (V_{VMP}) becomes higher than the charge overcurrent release voltage (V_{REL4}) when a load is connected after disconnecting the charger, and the charge overcurrent is released after passing the charge overcurrent release delay time (t_{VREL4}).

Standby Mode

After the overdischarge protection, the R5650T shifts from normal mode to standby mode when VMP pin voltage (V_{VMP}) is more than V_{STB}. In standby mode, some unnecessary circuits stop to reduce the supply current to a minimum. This device can return from standby mode to normal mode when V_{VMP} is lower than V_{STB} by connecting a charger.

Operating Mode Switch by SEL1 and SEL2 Pins

SEL1 and SEL2 pins are switching-control pins to select among 3- / 4- / 5-cell protection. When using for the 4-cell protection, connecting SEL1 pin to VSS and the SEL2 pin to VDD is required to stop the 5th cell protection circuit and shut signals. The overdischarge is not detected when VC5 pin is shortened to VSS.

When using for the 3-cell protection, likewise, connecting SEL1 pin to VDD and SEL2 pin to VSS is required to stop the 5th and 4th cells protection circuits and shut signals. The overdischarge is not detected when VC4 and VC5 pins are shortened to VSS. SEL1 / SEL2 pin must be fixed to VDD / VSS when using the 3- / 4- / 5-cell protection. Setting SEL1 and SEL2 pins can select disabling/enabling the shorten mode 1 (approx. 1/70) or the shorten mode 2 (t_{VDET1}:approx. 4ms). Refer to the following table for details of the operating mode.

Operating Modes

Input Voltage[1]		Operation Mode
SEL1 Pin	SEL2 Pin	
High	High	5-cell protection mode
Low	High	4-cell protection mode
High	Low	3-cell protection mode
Low	Low	Delay time shortening mode 2 for 5-cell protection
Low	Middle	Prohibition of use[2]
Middle	Low	Prohibition of use[2]
Middle	Middle	Delay time shortening mode 1 for 5-cell protection
Middle	High	Delay time shortening mode 1 for 4-cell protection
High	Middle	Delay time shortening mode 1 for 3-cell protection

[1] "High": VDD level, "Middle": (VDD/2-0.5) V to (VDD-3) V, "Low": VSS level

[2] Reserved for Ricoh's test mode

Delay Time Setting by CT1, CT2, and CT3 Pins

CT1, CT2, and CT3 pins are used for setting each delay time of the overdischarge detection (t_{VDET2}), the discharge overcurrent detection 1 (t_{VDET31}) and the discharge overcurrent2 (t_{VDET32}) by connecting external capacitors C_{CTX}. Each of t_{VDET2}, t_{VDET31}, and t_{VDET32} be calculated by the equation of CV = iΔt.

(1) t_{VDET2} setting by external capacitor C_{CT1}

$t_{VDET2} = C_{CT1}$ (nF) × V_{DCT1} / I_{CT1}

For example, if C_{CT1} = 33 nF, VDCT1 = 1.80 V, and I_{CT1} = 500 nA, t_{VDET2} = 118.8 ms.

(2) t_{VDET31} setting by external capacitor C_{CT2}

$t_{VDET31} = C_{CT2}$ (nF) × V_{DCT2} / I_{CT2}

For example, if C_{CT2} = 3.3 nF, V_{DCT2} = 1.50 V, and I_{CT2} = 500 nA, t_{VDET31} = 9.9 ms.

(3) t_{VDET32} setting by external capacitor C_{CT3}

$t_{VDET32} = C_{CT3}$ (nF) × V_{DCT3} / I_{CT3}

For example, if C_{CT3} = 3.3 nF, V_{DCT3} = 1.50 V, and I_{CT3} = 3 μA, t_{VDET32} = 1.65 ms.

Temperature Protection by External NTC

The R5650T has three temperature detectors to protect the charge high temperature, the charge low temperature, and the discharge high temperature.

VRT and TEP pins are used to supervise the temperature. VRT pin supplies a voltage divided between external series resistors of R_{TEP} and NTC to TEP pin. The temperature is supervised only for 10 ms in the 1 s period to reduce supply current between R_{TEP} and NTC. The discharge high temperature is detected when the supervised temperature is greater than T_{DDH} in discharge state, and DOUT pin becomes "Low" to stop the discharge current. After that, the discharge high temperature is released when the supervised temperature is lower than T_{RDH}, and DOUT pin becomes "High" to permit discharging. The charge high temperature is detected when the supervised temperature is greater than T_{DCH} in non-discharge state, and COUT pin becomes "Hi-Z" to stop the charge current. After that, the charge high temperature is released when the supervised temperature is lower than T_{RCH}, and COUT pin becomes "High" to permit charging. The charge low temperature is detected when the supervised temperature is lower than T_{DCL} in non-discharge state, and COUT pin becomes "Hi-Z" to stop the charge current. After that, the charge low temperature is released when the supervised temperature is greater than T_{RCL}, and COUT pin becomes "High" to permit charging.

VMP pin supervises the discharge current by its input voltage. After detecting the charge high / low temperature, these protected states are released immediately when VMP pin voltage (V_{VMP}) becomes higher than V_{DSG}. The device has internal fixed delay times for temperature protection. For example, in the case of detecting the discharge high temperature, the internal timer counts 64 ms until the discharge high temperature is detected. Detecting and releasing at other temperatures also are set at the same delay time.

Since VRT pin supplies a voltage source for the voltage divider. In standby mode, the temperature protection does not work.

Reference resistance values for R_{TEP} and NTC [(1)]

- R_{TEP} : 33 kΩ ±1%
- NTC : 10 kΩ ±1% (Ta = 25°C, B-value($B_{25/85}$) = 3435K ±1%

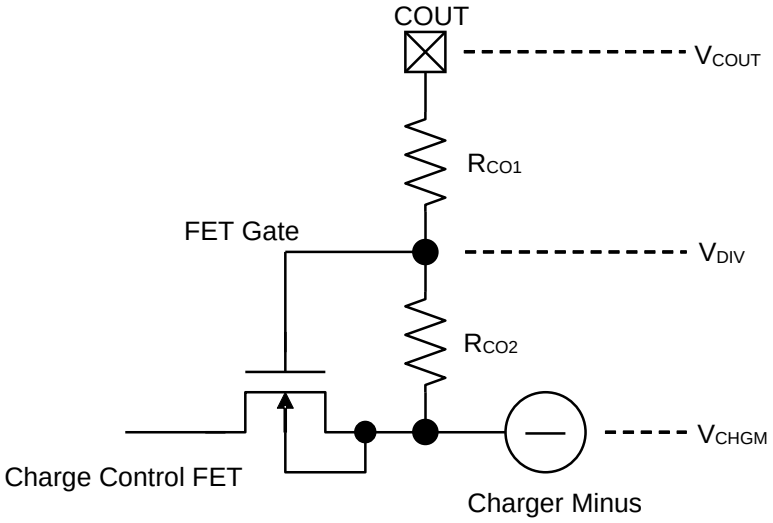
COUT and DOUT settings for temperature protection

State	Pin	to 0°C (T_{DCL})	0°C (T_{DCL}) to 45°C (T_{DCH})	45°C (T_{DCH}) to 70°C (T_{DDH})	70°C (T_{DDH}) and more
Charge	COUT	Hi-z	High	Hi-z	Hi-z
	DOUT	High	High	High	Low
Discharge	COUT	High			Hi-z
	DOUT	High			Low

(1) Refer to *Technical Notes on External Components* for recommended parts.

0 V Battery Charging [R5650TxxxxA/B Only]

Charging to each cell is enabled when COUT pin is “High” even if the voltage of one or more cells is 0 V. Since COUT pin is impossible to maintain the “High” output when the power supply voltage (V_{DD}) becomes lower than 2.5 V, V_{DD} of 2.5 V or more must be provided to charge cells. The below reference circuit indicates the charge control FET and its surrounding circuits.



The input voltage of FET gate is the divided voltage between COUT and Charger Minus, V_{DIV}. So, it is necessary to satisfy following condition to turn on the FET when its threshold voltage is defined as V_{TH}.

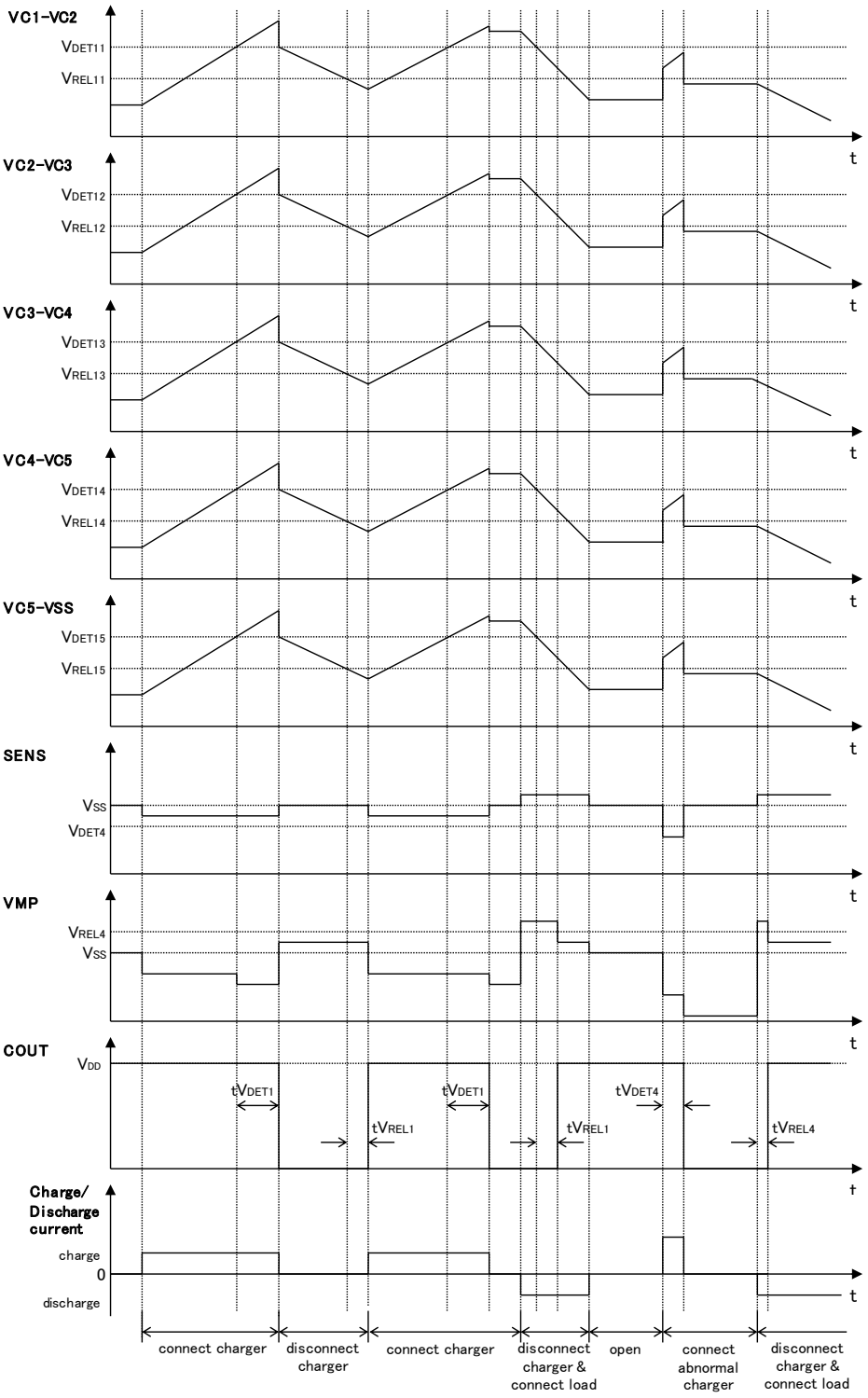
$$V_{DIV} = (V_{COUT} – V_{CHGM}) \text{ X } R_{CO2} / (R_{CO1} + R_{CO2}) > V_{TH}$$

0 V Battery Detector: VNOCHG-n (n = 1, 2, 3, 4, 5) [R5650TxxxxC/D Only]

Since the device detects a charge inhibition voltage for each cell, if either of cell voltages is lower than the charge inhibition voltage, the charge inhibition is detected with the charger being connected to the battery pack. After detecting, COUT pin becomes “Hi-z”, and charging stops.

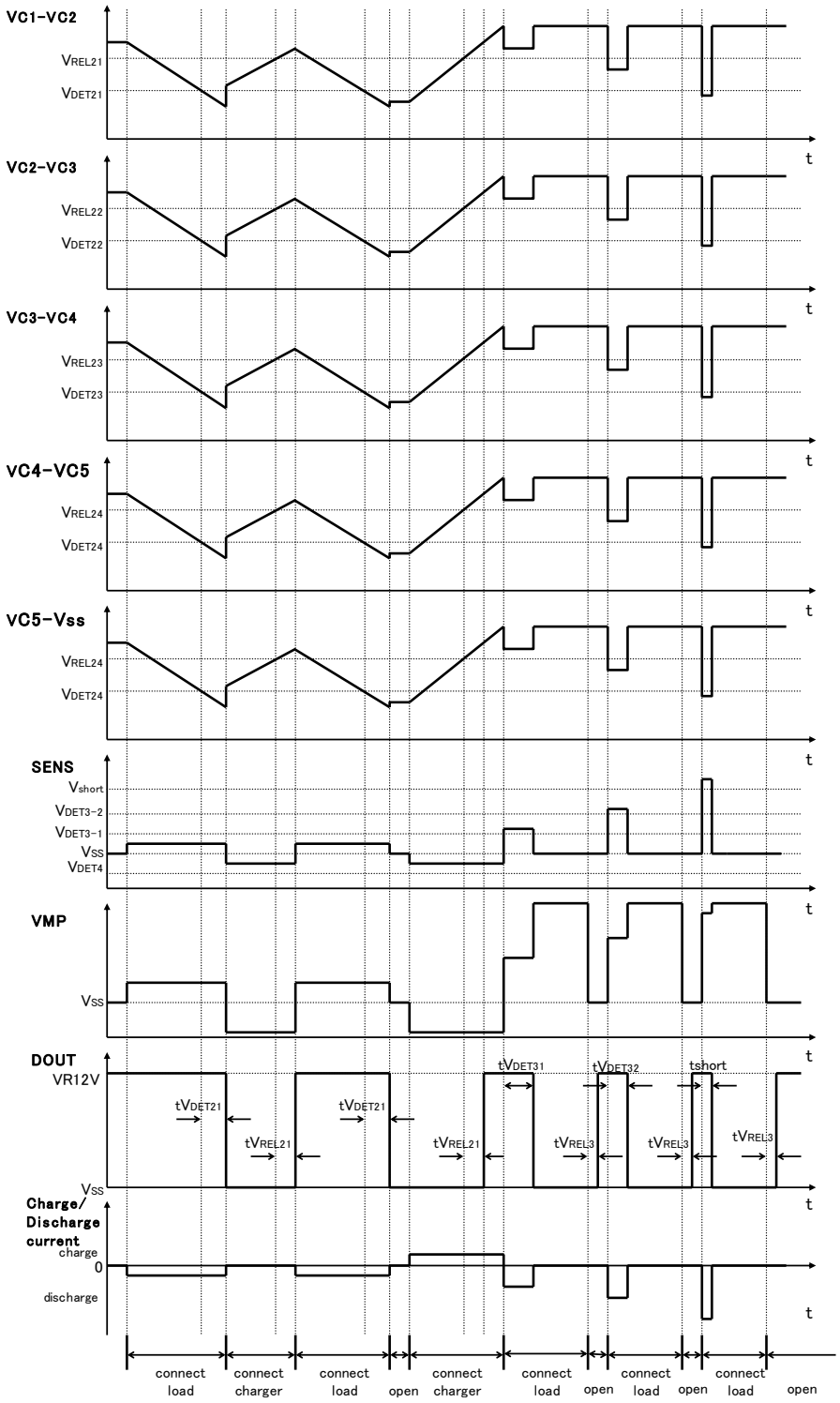
Timing Charts

Overcharge Voltage and Charge Overcurrent



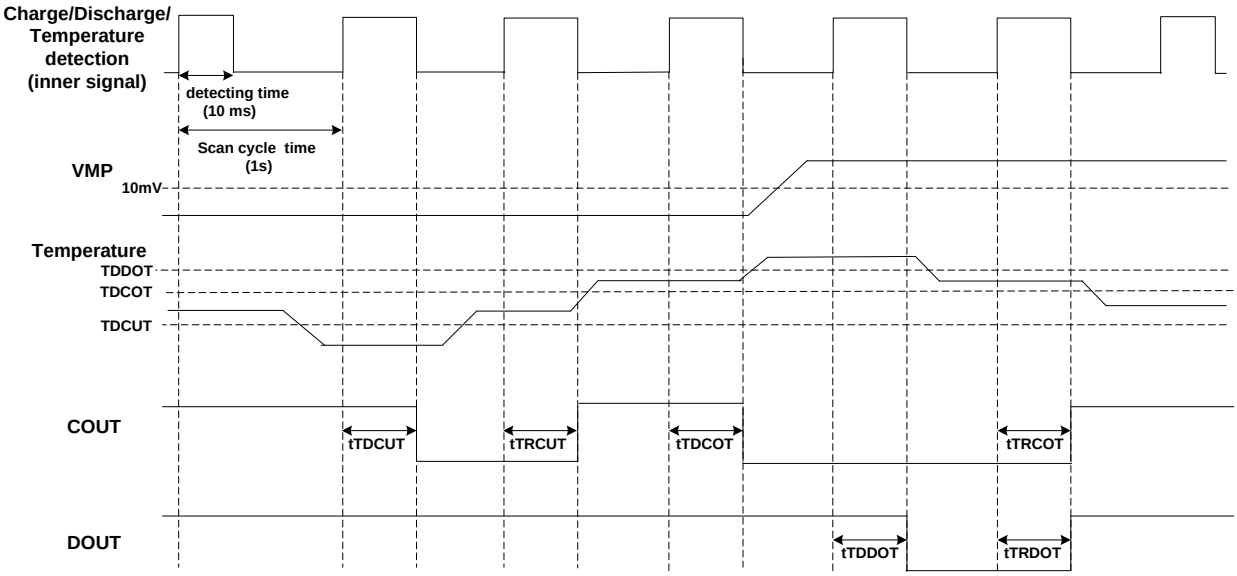
Timing Diagram for Overcharge Voltage and Charge Overcurrent

Overdischarge, Discharge Overcurrent 1/2, and Short-circuit Detection



Timing Diagram for Overdischarge, Discharge Overcurrent, and Short-circuit

Temperature Detection

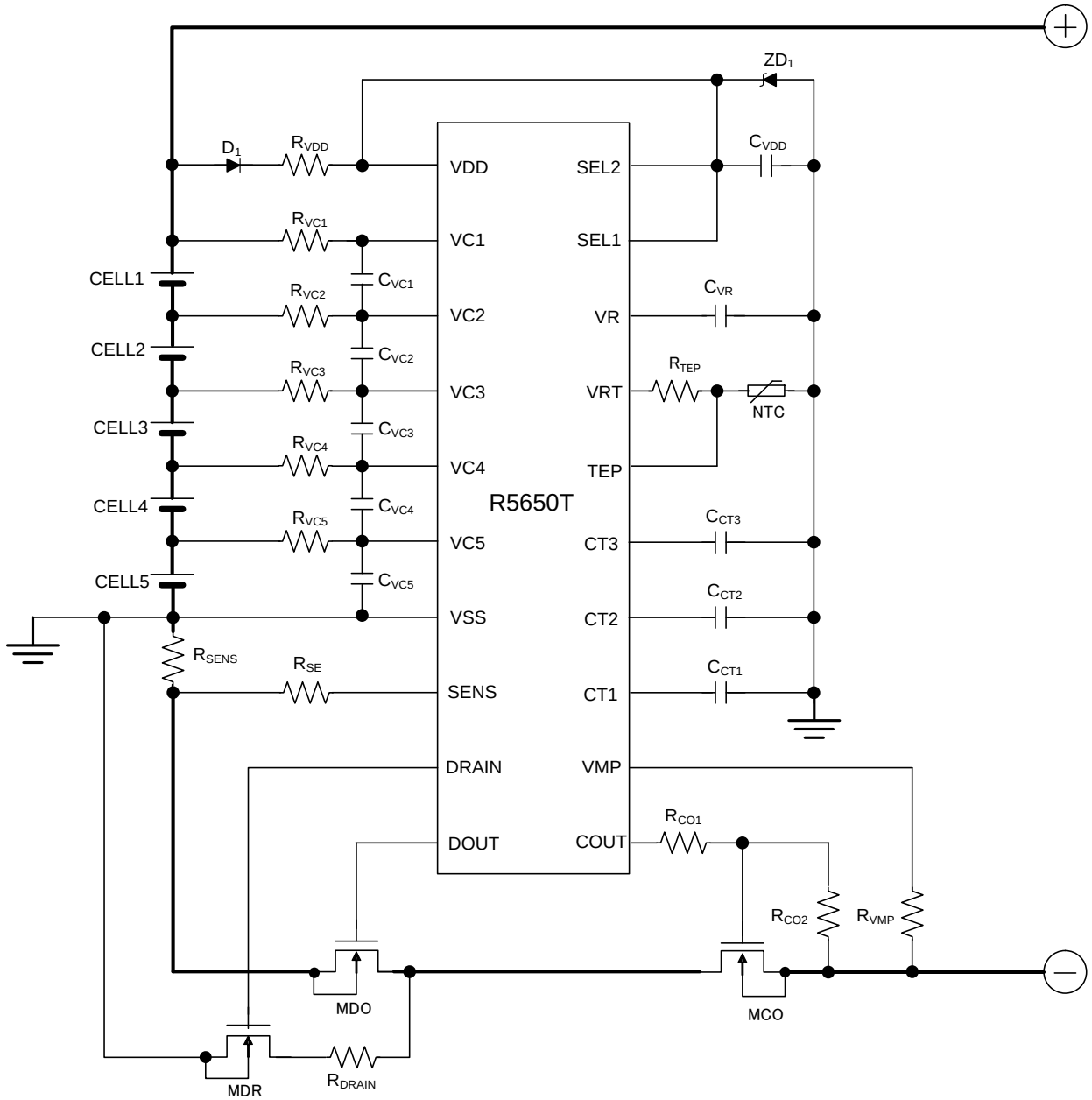


Timing Diagram for Temperature Detection

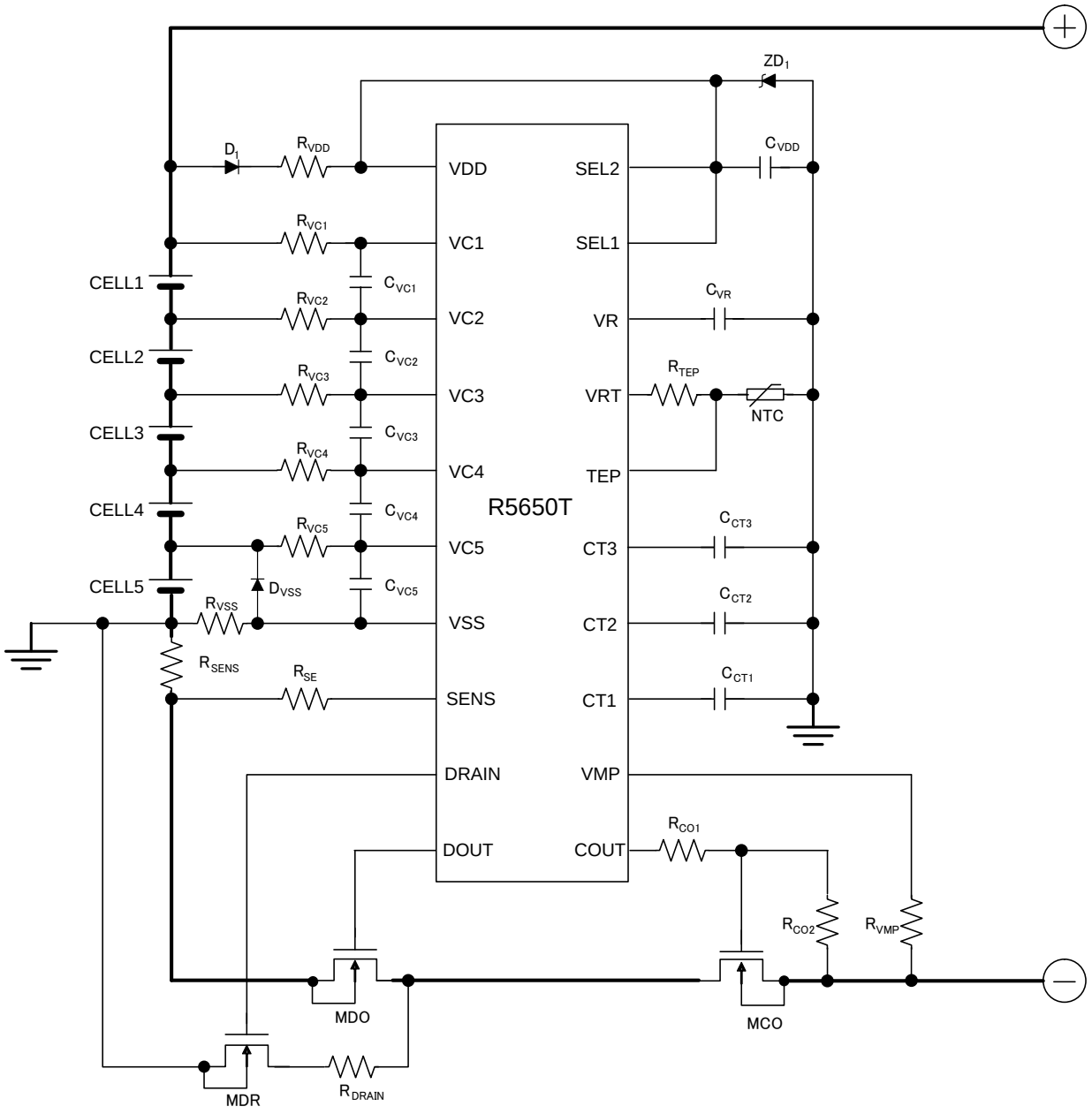
APPLICATION INFORMATION

Typical Application Circuits

The discharge current flows through a parasitic diode of its FET when the FET connected to COUT pin is turned OFF and a load is connected between Pack+ and Pack-. And, the charge current flows through the parasitic diode of its FET when the FET connected to DOUT pin is turned OFF and a charger is connected between Pack+ and Pack-. Thus, the FETs must be enough to flow the current.

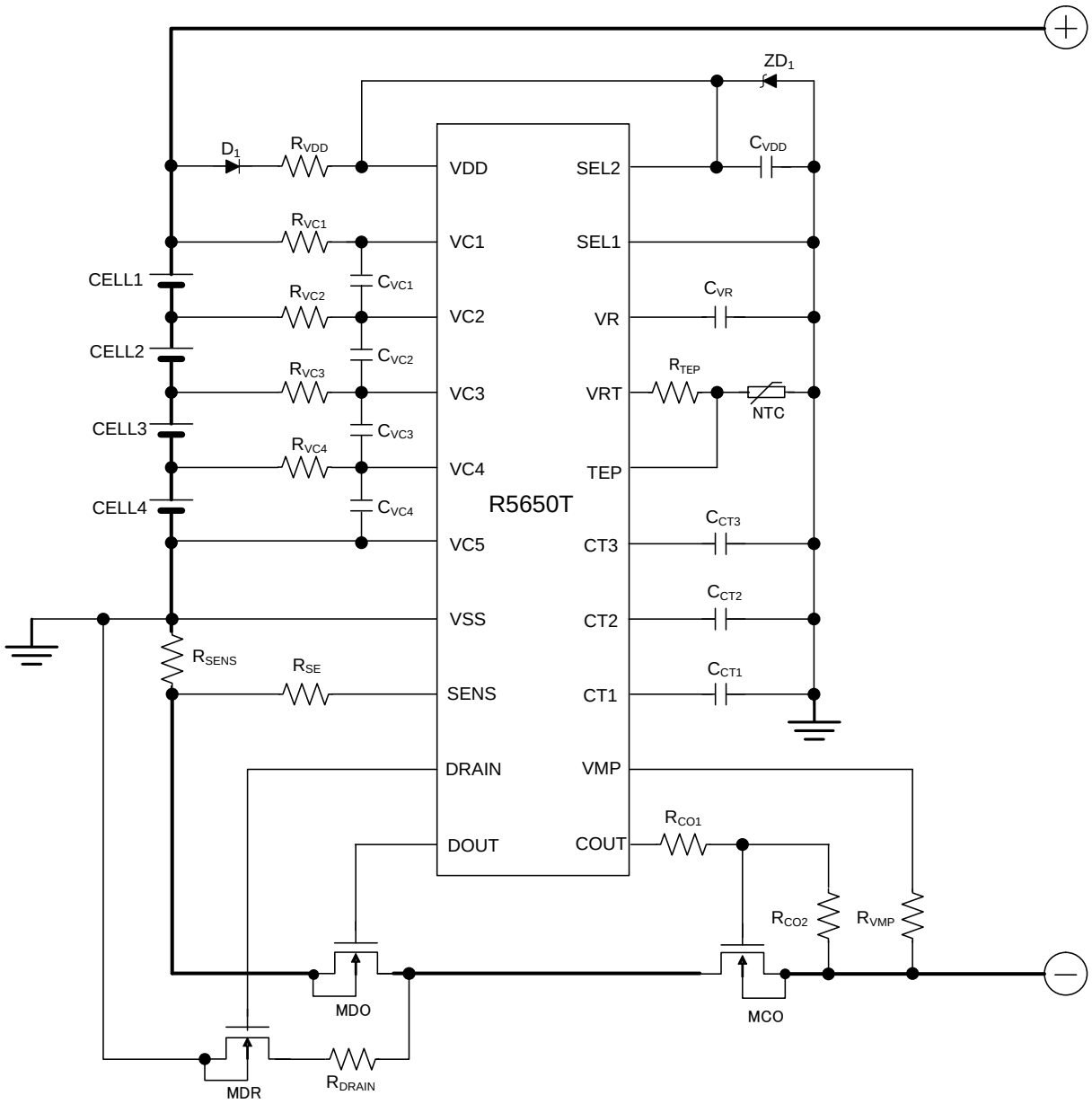


Typical Application Circuit for 5-cell Protection

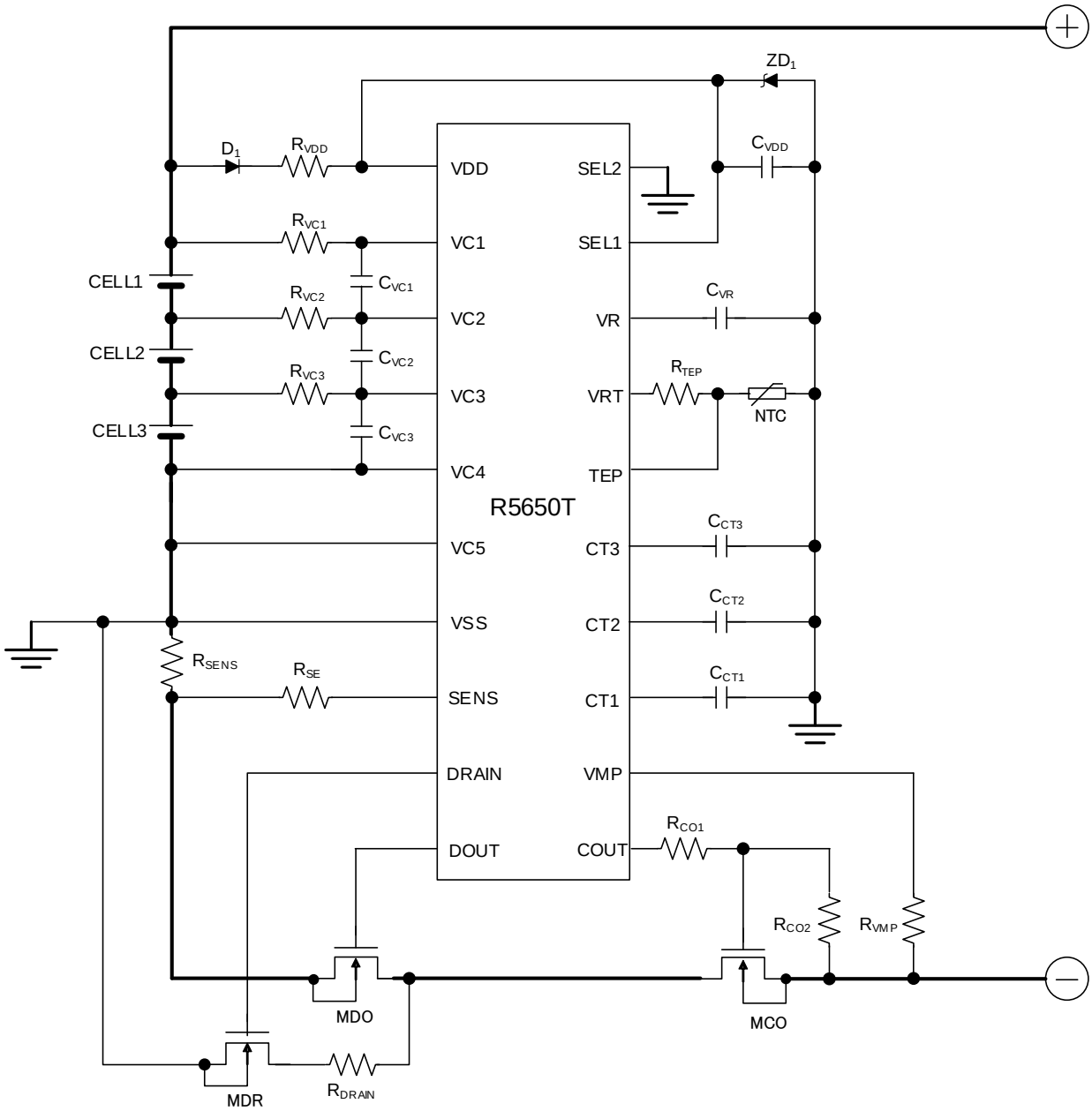


Typical Application Circuit for 5-cell Protection with Diode (D_{VSS})

If <Battery- to Board-> line resistance is large, the discharge overcurrent causes a voltage difference between Battery- and VSS. Since V_{DET31}, V_{DET32}, and V_{SHORT} become smaller than normal values owing to the difference value, please take notice to <Battery- to Board-> line resistance.



Typical Application Circuit for 4-cell Protection



Typical Application Circuit for 3-cell Protection

External Components Selection Guide

Symbol	Value (Typ.)	Range	Unit	Remarks[1]
R_{VDDX}	330	330 to 1000	Ω	Refer to *Technical Note [1]*.
R_{VC1X}	330	330 to 1000	Ω	Refer to *Technical Note [2]*.
R_{VC2X}	330	330 to 1000	Ω	
R_{VC3X}	330	330 to 1000	Ω	
R_{VC4X}	330	330 to 1000	Ω	
R_{VC5X}	330	330 to 1000	Ω	
R_{SENS}	100	1 or more	mΩ	Depending on set value for overcurrent
R_{SE}	1	1 to 10	kΩ	Refer to *Technical Note [3]*.
R_{DRAIN}	75	Note [4]	kΩ	Refer to *Technical Note [4]*.
R_{CO1}	1	Note [4]	MΩ	
R_{CO2}	2	Note [4]	MΩ	
R_{VMP}	0.01	0.01 to 10	MΩ	
C_{VDDX}	1	0.1 to 1	µF	Refer to *Technical Note [1]*.
C_{VC1X}	0.1	0.1	µF	Refer to *Technical Note [2]*.
C_{VC2X}	0.1	0.1	µF	
C_{VC3X}	0.1	0.1	µF	
C_{VC4X}	0.1	0.1	µF	
C_{VC5X}	0.1	0.1	µF	
C_{CT1}	33	10 to 1000	nF	-
C_{CT2}	3.3	2.2 or more	nF	Refer to *Technical Note [5]*.
C_{CT3}	3.3	2.2 or more	nF	
C_{VR}	1	1	µF	Refer to *Technical Note [6]*.
ZD_1	30	30 or less	V	Refer to *Technical Note [7]*. Recommended Component: MM1Z30 0.5W 30V J SOD-123 EIC
R_{TEP}	33	33	kΩ	
NTC	10	10	kΩ	Recommended Components: 103AT-4-040 (SEMITEC) NTCG103JF103F or NTCG163JF103F(TDK)
D_1		−	−	Refer to *Technical Note [10]*.
MCO		−	−	Refer to *Technical Note [8]*.
MDO		−	−	
MDR		−	−	Refer to *Technical Note [9]*.

[1] Refer to "*Technical Notes for External Components*" for details.

Technical Notes on the Selection Components

【1】 R_{VDD} and C_{VDD} stabilize the supply voltage to the device.

【2】 R_{VCx} and C_{VCx} stabilize the voltage fluctuation. If R_{VCx} is large, the detection voltage increases due to the internal conduction current of the device.

【3】 Since a large R_{SE} may shift the overcurrent detection voltage, a resistor of appror.10kΩ is appropriate.

【4】 Choose appropriate values for R_{DRAIN}, R_{CO1}, and R_{CO2} to satisfy the next equation, otherwise, the release from the discharge overcurrent and the short-circuit may be impossible.

$$R_{DRAIN} < V_{REL3} \times (R_{CO1} + R_{CO2})/(V_{DD} - V_{REL3})$$

If small R_{CO1} or R_{CO2} is set, when the output of C_{OUT} is "H", the supply current of protection circuit board increases. If large R_{CO1} or R_{CO2} is set, when the output of C_{OUT} is "Hi-z", the speed for pull-down the gate of the charge FET becomes slow and turning off the FET will be slow.

【5】 If too small C_{CT2} or C_{CT3} is set, the discharge overcurrent detection delay time 1(t_{VDET31}) or 2 (t_{VDET32}) becomes shorter than the short-circuit delay time (t_{SHORT}).

【6】 Connecting a 1.0μF capacitor to VR pin is required to make a stable VR output

【7】 It is recommended that a zener diode is connected to prevent a high voltage to the device. The zener diode must be directly connected between VDD pin of the device and VSS pin.

【8】 As for the charge control FET (MCO) and the discharge control FET (MDO), please make a sufficient consideration to their maximum voltage tolerance, current rating, maximum power consumption, and peak consumption when short-circuit.

【9】 As for the pull-down FET (MDR), please make a sufficient consideration to its maximum voltage tolerance.

【10】 Diode (D_1) is required to prevent a drop in the VDD pin voltage (V_{DD}), along with the battery voltage drop during the short-circuit.

TECHNICAL NOTES

The performance of power source circuits using this IC largely depends on peripheral circuits. When selecting the peripheral components, please consider the conditions of use. Do not allow each component, PCB pattern or the IC to exceed their respected rated values (voltage, current, and power) when designing the peripheral circuits.

- The typical application circuit diagrams are just examples. The operation in application circuits is not guaranteed. Be sure to perform a sufficient evaluation with the external components under the actual usage conditions for selection.

- Be careful not to apply the overvoltage and the overcurrent which exceed the rating to the protection IC and external components. Especially, select an FET with enough current capacity to endure the large current because a large current might flow through the FET during the time between an overcharge detection a blown fuse.

- When the cells are connected to IC first, the minus terminal of the lowest voltage side cell should be connected to IC at the first and other terminals should be connected to IC in turn from lower voltage side.

PD-TSSOP-20-(85125)-JE- B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51.

Measurement Conditions

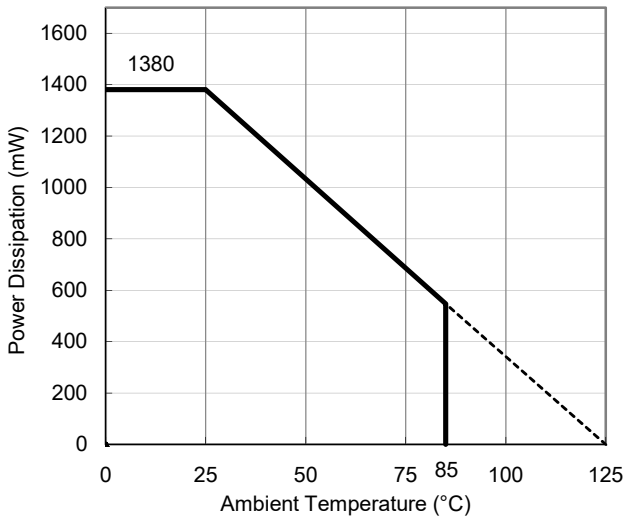
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Outer Layer (First Layer): Less than 10% of 62 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 74.2 mm Square Outer Layer (Fourth Layer): Less than 10% of 62 mm Square
Through-holes	None

Measurement Result (Ta = 25°C, Tjmax = 125°C)

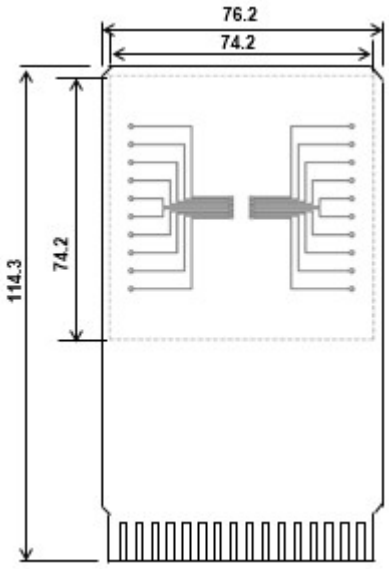
Item	Measurement Result
Power Dissipation	1380 mW
Thermal Resistance (θja)	θja = 72°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 22°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

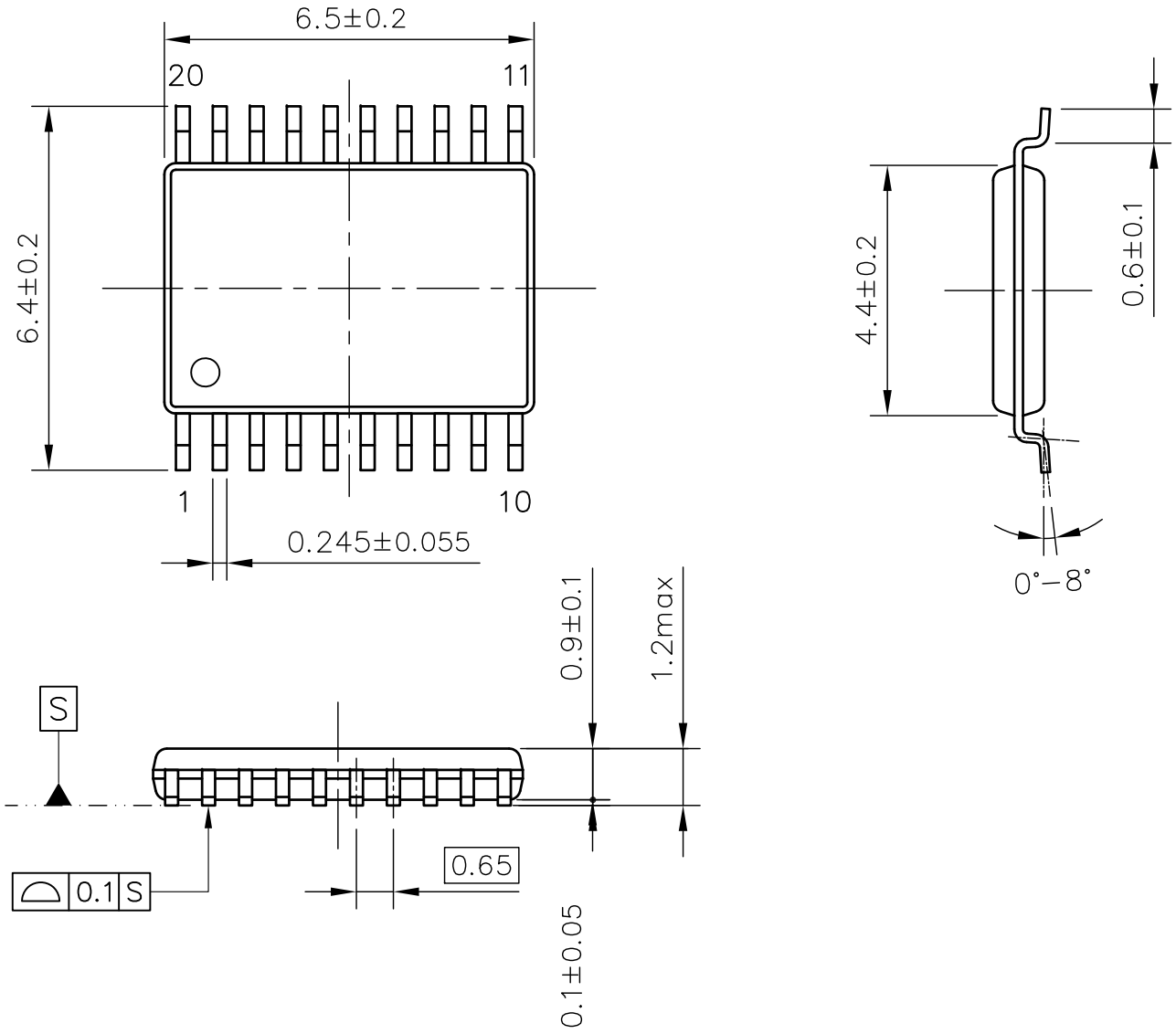


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH



TSSOP-20 Package Dimensions (Unit: mm)

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