

Low Voltage 1A Voltage Regulator (LDO Regulator)

NO.EA-265-190408

OUTLINE

The RP132x is a voltage-regulator with a built-in low ON-resistance transistor and output current is 1A capability. This IC has two versions: fixed output voltage type and externally adjustable output voltage type. The minimum output voltage can be set from 1.4V. Otherwise, the load regulation of RP132x has much improved when compared with conventional regulators. It's Typ.5mV at $I_{OUT}=0.1mA$ to 1A.

This IC consists of a voltage reference unit, an error amplifier, a resistor net for setting output voltage, current limit circuits to prevent over-current and a thermal-shutdown circuit. A standby mode with ultra low supply current can be realized with the chip enable function. Additionally, E/F Version with delay pin for inrush current limit time setting are also available.

The packages for these ICs are DFN(PLP)1820-6, SOT-89-5, HSOP-6J and TO-252-5-P2. DFN(PLP)1820-6 is suitable for high density mounting of the ICs on boards. SOT-89-5, HSOP-6J and TO-252-5-P2 are supporting high wattage.

FEATURES

- Output Current Min. 1A
- Supply Current Typ. 65 μ A
- Standby Current Typ. 0.15 μ A
- Input Voltage Range 1.4V to 6.5V
- Output Voltage Range Fixed Output Voltage Type: 0.8V to 5.5V (0.1V steps)
Adjustable Output Voltage Type: 0.8V to 5.5V
(For other voltages, please refer to MARK INFORMATIONS.)
- Dropout Voltage Typ. 0.52V ($V_{OUT}=2.8V$, $I_{OUT}=1A$)
- Ripple Rejection Typ. 70dB ($f=1kHz$, $V_{OUT}=2.8V$)
- Output Voltage Accuracy $\pm 1.0\%$
- Output Voltage Temperature-Drift Coefficient Typ. $\pm 60ppm/^{\circ}C$
- Line Regulation Typ. 0.052%/V
- Load Regulation Typ. 3mV at $I_{OUT}=300mA$, Typ. 5mV at $I_{OUT}=1A$
- Packages DFN(PLP)1820-6, SOT-89-5, HSOP-6J, TO-252-5-P2
- Inrush Current Limit Circuit Typ. 500mA
B/D version: Inrush current limit time is 500 μ s.
E/F version: Inrush current limit time is adjustable.
- Fold-Back Protection Circuit Typ. 250mA (Current at short mode)
- Thermal Shutdown Circuit Thermal Shutdown Temperature: Typ. 165 $^{\circ}C$
Released Temperature: Typ. 95 $^{\circ}C$
- Auto Discharge Function D, F version
- Ceramic capacitors are recommended to be used with this IC 2.2 μ F or more ($V_{OUT} \leq 3.6V$)
4.7 μ F or more ($V_{OUT} > 3.6V$)

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APPLICATIONS

- Power source for battery-powered equipment.
- Power source for portable communication equipment
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for home appliances and Notebook PC.

SELECTION GUIDE

The output voltage, the auto discharge function⁽¹⁾, and the package type for the IC can be selected at the user's request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP132K001*-TR	DFN(PLP)1820-6	5,000 pcs	Yes	Yes
RP132Kxx1*-TR				
RP132H001#-T1-FE	SOT-89-5	1,000 pcs	Yes	Yes
RP132Hxx1#-T1-FE				
RP132S001#-E2-FE	HSOP-6J	1,000 pcs	Yes	Yes
RP132Sxx1*-E2-FE				
RP132J001#-T1-FE	TO-252-5-P2	3,000 pcs	Yes	Yes
RP132Jxx1#-T1-FE				

RP132x001x is the adjustable output voltage type.

xx: The output voltage can be designated in the range from 0.8V(08) to 5.5V(55) in 0.1V step.

The voltage in 0.05 V step is shown as follows:

Ex. 1.05 V : RP132x101x5

Contact our sales representatives for other voltages.

*: The combination of the auto discharge function and delay pin (for setting inrush current limit time) are as follows.

B: without auto discharge function

D: with auto discharge function

E: without auto discharge function, with delay pin (for setting inrush current limit time)

F: with auto discharge function and delay pin (for setting inrush current limit time)

#: The auto discharge function at off state are options as follows.

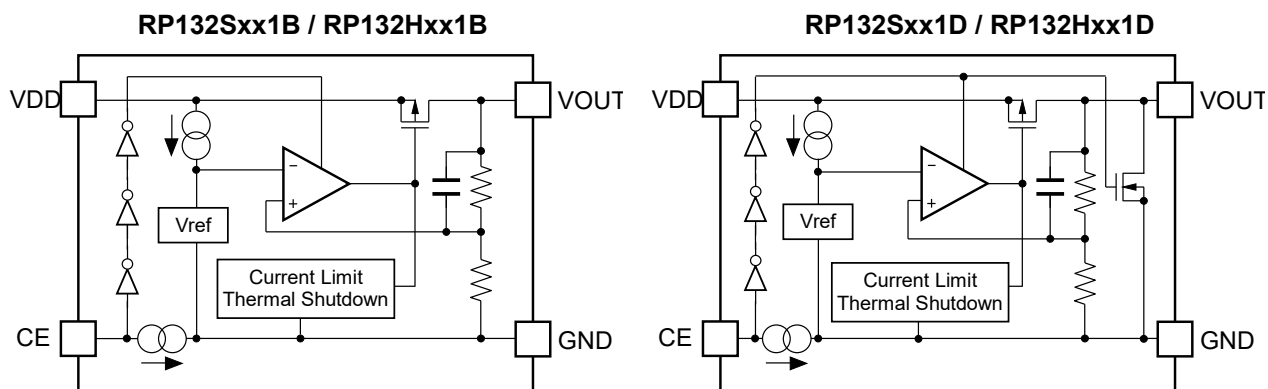
B: without auto discharge function at off state

D: with auto discharge function at off state

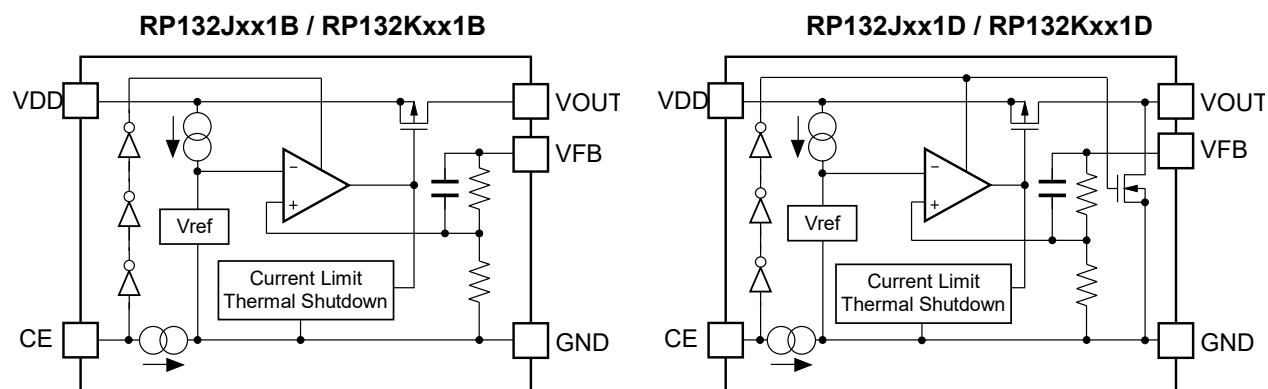
⁽¹⁾ Auto-discharge function quickly lowers the output voltage to 0V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

BLOCK DIAGRAMS

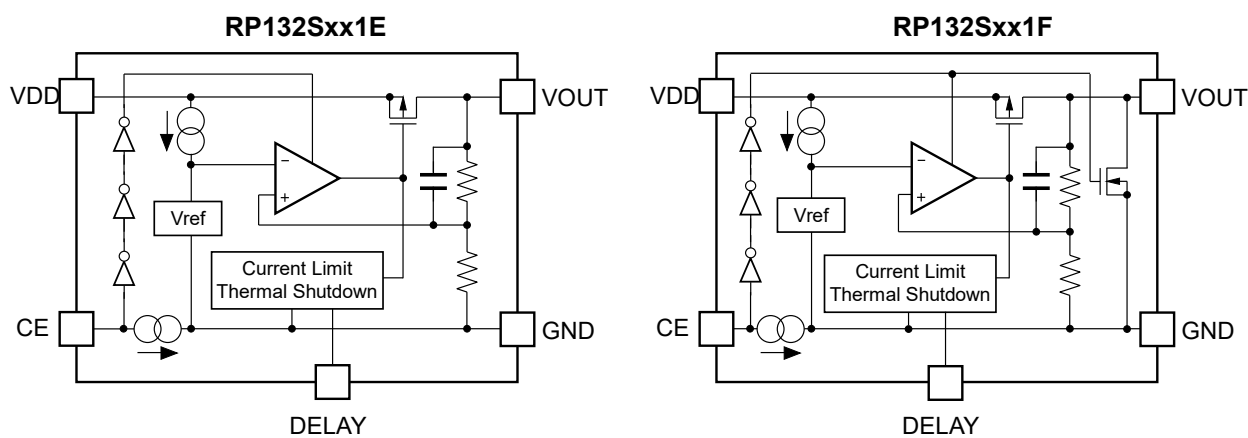
- Fixed Output Voltage Type (HSOP-6J / SOT89-5)



- Fixed Output Voltage Type (TO-252-5-P2 / DFN(PLP)1820-6)



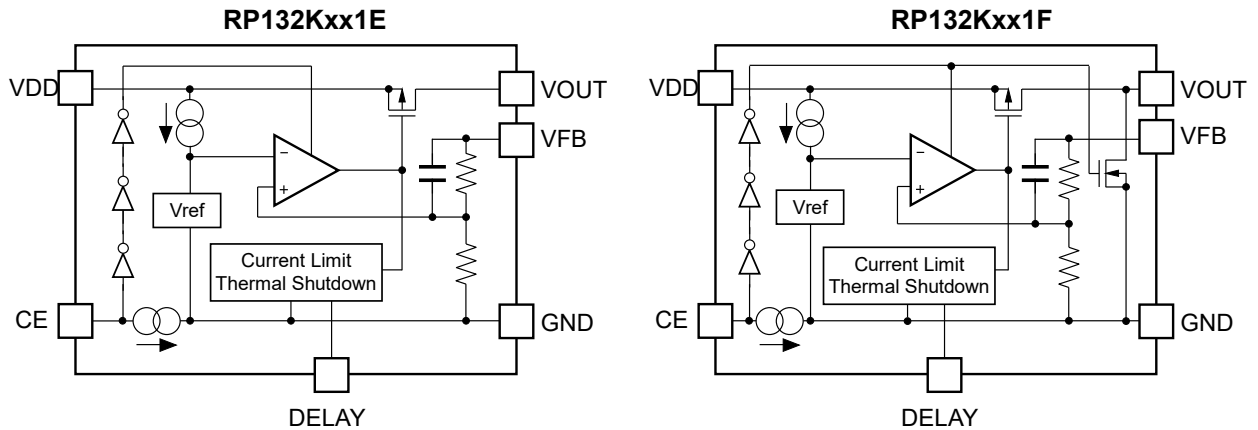
- Fixed Output Voltage Type with DELAY pin (HSOP-6J)



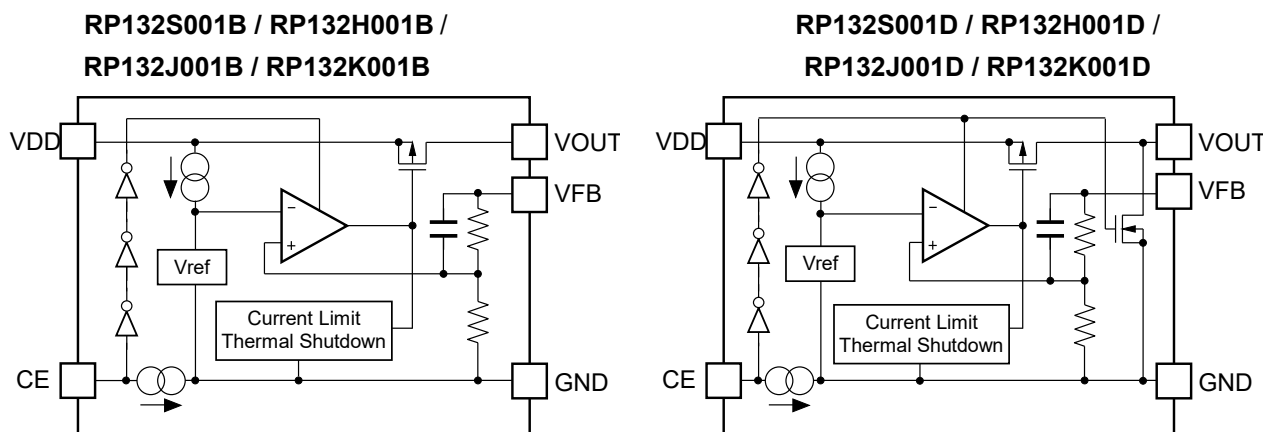
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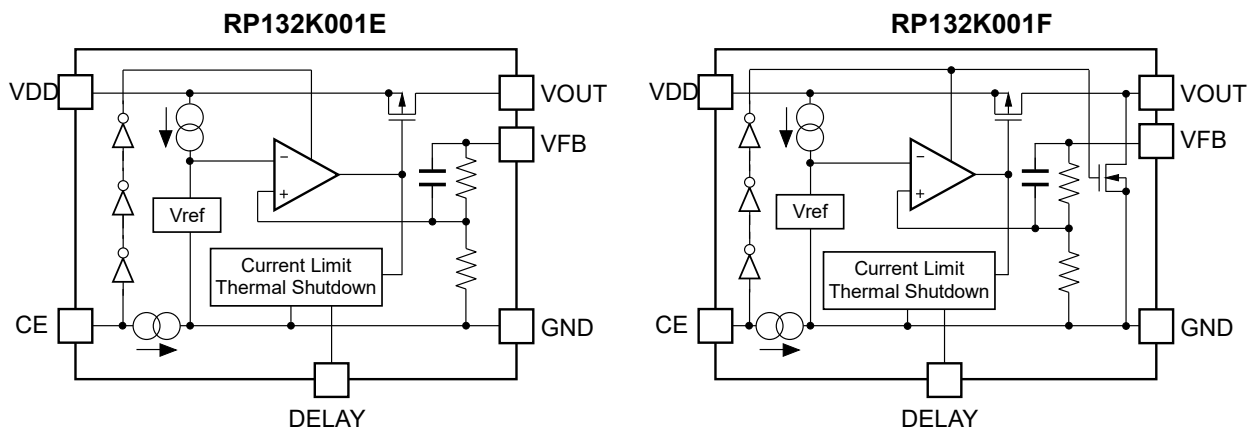
- **Fixed Output Voltage Type with DELAY pin (DFN(PLP)1820-6)**



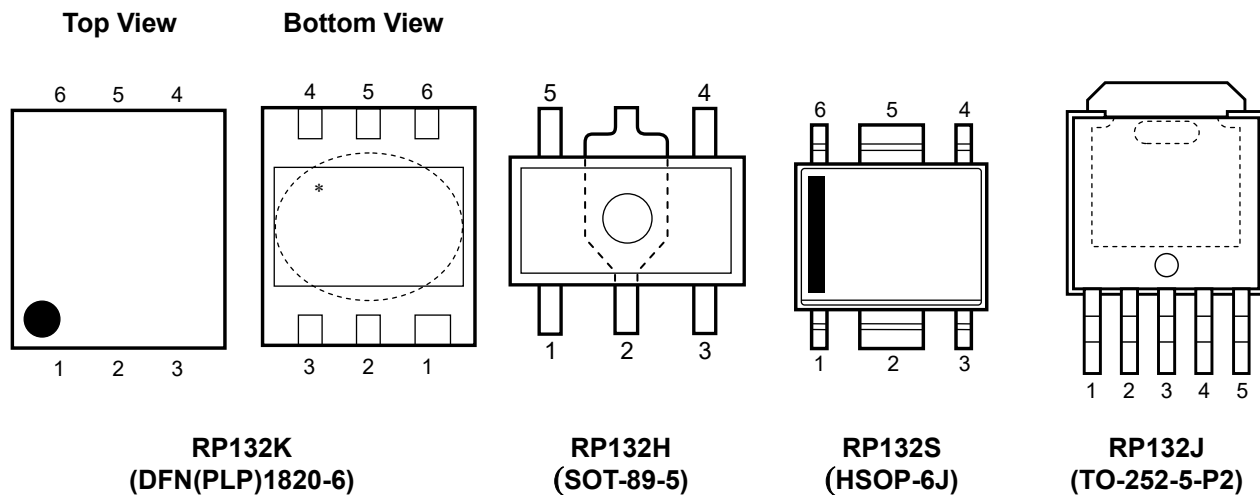
- **Adjustable Output Voltage Type (HSOP-6J / SOT-89-5 / TO-252-5-P2 /DFN(PLP)1820-6)**



- **Adjustable Output Voltage Type with DELAY pin (DFN(PLP)1820-6)**



PIN DESCRIPTIONS



RP132K⁽¹⁾ (DFN(PLP)1820-6) Pin Description

Pin No.	Symbol	Pin Description
1	VOUT	Output Pin ⁽²⁾
2	VFB	Feed Back Pin ⁽²⁾
3	GND	Ground Pin
4	CE	Chip Enable Pin ("H" Active)
5	NC	No Connection (RP132K001B/D, RP132Kxx1B/D)
	DELAY	Delay Pin for setting inrush current limit time (RP132K001E/F, RP132Kxx1E/F)
6	VDD	Input Pin

*Tab is GND level. (They are connected to the reverse side of this IC.) The tab is better to be connected to the GND, but leaving it open is also acceptable.

⁽¹⁾ When using Adjustable Output Voltage Type (RP132K001x), please follow "Notes on the Adjustable Output Voltage Type Settings".

⁽²⁾ When using Fixed Output Voltage Type (RP132Kxx1x), the VOUT pin and the VFB pin should be connected.

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RP132H⁽¹⁾ (SOT-89-5) Pin Description

Pin No.	Symbol	Pin Description
1	CE	Chip Enable Pin ("H" Active) (RP132Hxx1B/D)
	VFB	Feed Back Pin (RP132H001B/D)
2	GND	Ground Pin
3	NC	No Connection (RP132Hxx1B/D)
	CE	Chip Enable Pin ("H" Active) (RP132H001B/D)
4	VDD	Input Pin
5	VOUT	Output Pin

RP132S⁽¹⁾ (HSOP-6J) Pin Description

Pin No.	Symbol	Pin Description
1	VOUT	Output Pin
2	GND	Ground Pin ⁽²⁾
3	NC	No Connection (RP132Sxx1B/D)
	VFB	Feed Back Pin (RP132S001B/D)
	DELAY	Delay Pin for setting inrush current limit time (RP132Sxx1E/F)
4	CE	Chip Enable Pin ("H" Active)
5	GND	Ground Pin ⁽²⁾
6	VDD	Input Pin

RP132J⁽¹⁾ (TO-252-5-P2) Pin Description

Pin No.	Symbol	Pin Description
1	CE	Chip Enable Pin ("H" Active)
2	VDD	Input Pin
3	GND	Ground Pin
4	VOUT	Output Pin ⁽³⁾
5	VFB	Feed Back Pin ⁽³⁾

*Tab is GND level. (They are connected to the reverse side of this IC.) The tab is better to be connected to the GND, but leaving it open is also acceptable.

⁽¹⁾ When using Adjustable Output Voltage Type (RP132x001x), please follow "Notes on Adjustable Output Voltage Type Settings".

⁽²⁾ GND pins must be wired each other when mounted on boards.

⁽³⁾ When using Fixed Output Voltage Type (RP132Jxx1x), VOUT pin and VFB pin should be connected.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit	
V_{IN}	Input Voltage	7.0	V	
V_{CE}	Input Voltage (CE Pin)	-0.3 to 7.0	V	
V_{FB}	Input Voltage (VFB Pin)	-0.3 to 7.0	V	
V_{OUT}	Output Voltage	-0.3 to $V_{IN}+0.3$	V	
P_D	Power Dissipation ⁽¹⁾	DFN(PLP)1820-6, JEDEC STD.51-7	2200	mW
		SOT-89-5, JEDEC STD.51-7	2600	
		HSOP-6J, JEDEC STD.51-7	2700	
		TO-252-5-P2, JEDEC STD.51-7	3800	
T_j	Junction Temperature Range	-40 to 125	°C	
T_{stg}	Storage Temperature Range	-55 to 125	°C	

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	1.4 to 6.5	V
T_a	Operating Temperature Range	-40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Refer to *POWER DISSIPATION* for detailed information.

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ELECTRICAL CHARACTERISTICS

$V_{IN} = \text{Set } V_{OUT} + 1.0V$, $I_{OUT} = 1mA$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 2.2\mu F$ ($V_{OUT} \leq 3.6V$) / $4.7\mu F$ ($V_{OUT} > 3.6V$)

The specification in is checked and guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 85^{\circ}C$, unless otherwise noted.

RP132xxx1B/D(Fixed Output Voltage Type) /

RP132S/Kxx1E/F(Fixed Output Voltage Type with DELAY pin)

($T_a = 25^{\circ}C$)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
V_{OUT}	Output Voltage	$T_a = 25^{\circ}C$	$V_{OUT} > 1.5V$	$\times 0.99$	$\times 1.01$	V	
			$V_{OUT} \leq 1.5V$	-15	15	mV	
		$-40^{\circ}C \leq T_a \leq 85^{\circ}C$	$V_{OUT} > 1.5V$	$\times 0.981$		$\times 1.019$	V
			$V_{OUT} \leq 1.5V$	-29		29	mV
I_{LIM}	Output Current Limit		1		A		
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation	$0.1mA \leq I_{OUT} \leq 300mA$		3	20	mV	
		$0.1mA \leq I_{OUT} \leq 1A$		5	60		
V_{DIF}	Dropout Voltage	Refer to the following "Dropout Voltage"					
I_{SS}	Supply Current	$I_{OUT} = 0mA$ ($V_{IN} = 6.5V$)		65	85	μA	
$I_{standby}$	Standby Current	$V_{CE} = 0V$, $V_{IN} = 6.5V$		0.15	0.60	μA	
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation	Set $V_{OUT} + 0.5V \leq V_{IN} \leq 6.5V$ * However, $V_{IN} \geq 1.6V$		0.05	0.10	%/V	
R_R	Ripple Rejection	f=1kHz Ripple 0.2Vp-p $I_{OUT} = 100mA$	$V_{OUT} \leq 3.3V$		70	dB	
			$V_{OUT} > 3.3V$		60		
V_{IN}	Input Voltage		1.4		6.5	V	
I_{SC}	Short Current Limit	$V_{OUT} = 0V$		250		mA	
I_{PD}	CE Pull-down Current			0.3	0.7	μA	
V_{CEH}	CE Input Voltage "H"		1.0			V	
V_{CEL}	CE Input Voltage "L"				0.4	V	
en	Output Noise	BW=10Hz to 100kHz		70		μV_{rms}	
T_{TSD}	Thermal Shutdown Detection Temperature	Junction Temperature		165		$^{\circ}C$	
T_{TSR}	Thermal Shutdown Released Temperature	Junction Temperature		95		$^{\circ}C$	
R_{LOW}	Low Output Nch Tr. ON Resistance (D/F version)	$V_{IN} = 4.0V$, $V_{CE} = 0V$		50		Ω	
I_{DELAY}	DELAY pin Current (DELAY pin version)	$V_{IN} = 4.0V$	0.7	1.2	1.7	μA	

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}C$) except Output Noise, Ripple Rejection, Dropout Voltage at 1A Output Current and Load Regulation and Thermal Shutdown.

The specification in is checked and guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$, unless otherwise noted.

Dropout Voltage
(Ta = 25°C)

Output Voltage V_{OUT} (V)	Dropout Voltage V_{DIF} (V)					
	Condition	Typ.	Max.	Condition	Typ.	Max.
$0.8 \leq V_{\text{OUT}} < 0.9$	$I_{\text{OUT}}=300\text{mA}$	0.67	<input type="checkbox"/> 0.89	$I_{\text{OUT}}=1\text{A}$	1.20	<input type="checkbox"/> 1.54
$0.9 \leq V_{\text{OUT}} < 1.0$		0.59	<input type="checkbox"/> 0.82		1.10	<input type="checkbox"/> 1.46
$1.0 \leq V_{\text{OUT}} < 1.1$		0.51	<input type="checkbox"/> 0.73		1.05	<input type="checkbox"/> 1.39
$1.1 \leq V_{\text{OUT}} < 1.2$		0.42	<input type="checkbox"/> 0.63		0.96	<input type="checkbox"/> 1.31
$1.2 \leq V_{\text{OUT}} < 1.5$		0.36	<input type="checkbox"/> 0.54		0.90	<input type="checkbox"/> 1.23
$1.5 \leq V_{\text{OUT}} < 2.6$		0.24	<input type="checkbox"/> 0.33		0.78	<input type="checkbox"/> 1.05
$2.6 \leq V_{\text{OUT}} < 3.3$		0.15	<input type="checkbox"/> 0.21		0.52	<input type="checkbox"/> 0.72
$3.3 \leq V_{\text{OUT}} \leq 5.5$		0.13	<input type="checkbox"/> 0.18		0.46	<input type="checkbox"/> 0.68

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 $V_{IN} = \text{Set } V_{OUT} + 1.0V, I_{OUT} = 1mA, C_{IN} = 2.2\mu F, C_{OUT} = 2.2\mu F, V_{OUT} \leq 3.6V, 4.7\mu F, V_{OUT} > 3.6V$ The specification in is checked and guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 85^{\circ}C$, unless otherwise noted.**RP132x001B/D(Adjustable Output Voltage Type) /****RP132K001E/F(Adjustable Output Voltage Type with DELAY pin)**

(Ta = 25°C)

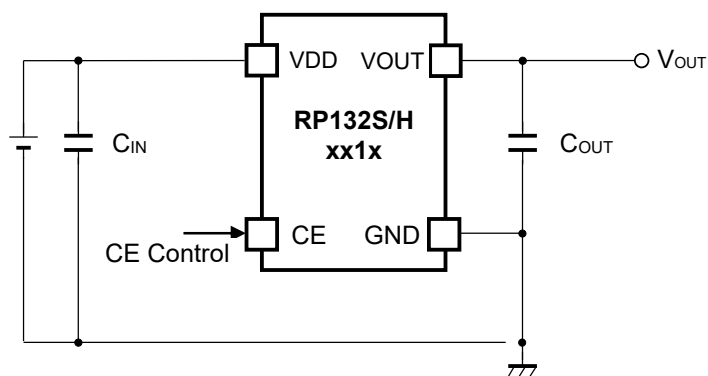
Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{FB}	Feedback Voltage	$T_a = 25^{\circ}C$	0.785	0.800	0.815	V
		$-40^{\circ}C \leq T_a \leq 85^{\circ}C$	<input type="checkbox"/> 0.771		<input type="checkbox"/> 0.829	
V_{OUT}	Output Voltage Adjusting Range		0.8		5.5	V
I_{LIM}	Output Current Limit	$V_{OUT} = V_{FB}$	<input type="checkbox"/> 1			A
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$0.1mA \leq I_{OUT} \leq 300mA$		3	<input type="checkbox"/> 20	mV
		$0.1mA \leq I_{OUT} \leq 1A$		5	<input type="checkbox"/> 60	
V_{DIF}	Dropout Voltage	$V_{OUT} = V_{FB}$	$I_{OUT} = 300mA$	0.67	<input type="checkbox"/> 0.89	V
			$I_{OUT} = 1A$	1.20	<input type="checkbox"/> 1.54	
ISS	Supply Current	$V_{OUT} = V_{FB}, I_{OUT} = 0mA$ ($V_{IN} = 6.5V$)		65	<input type="checkbox"/> 85	μA
Istandby	Standby Current	$V_{CE} = 0V, V_{IN} = 6.5V$		0.15	0.60	μA
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$V_{OUT} = V_{FB}, 1.6V \leq V_{IN} \leq 6.5V$		0.05	<input type="checkbox"/> 0.10	%/V
R_R	Ripple Rejection	$f = 1kHz,$ Ripple 0.2Vp-p, $I_{OUT} = 100mA$		70		dB
V_{IN}	Input Voltage		<input type="checkbox"/> 1.4		<input type="checkbox"/> 6.5	V
I_{SC}	Short Current Limit	$V_{OUT} = V_{FB} = 0V$		250		mA
I_{PD}	CE Pull-down Current			0.3	<input type="checkbox"/> 0.7	μA
V_{CEH}	CE Input Voltage "H"		<input type="checkbox"/> 1.0			V
V_{CEL}	CE Input Voltage "L"				<input type="checkbox"/> 0.4	V
en	Output Noise	BW=10Hz to 100kHz		70		μV_{rms}
T_{TSD}	Thermal Shutdown Detection Temperature	Junction Temperature		165		$^{\circ}C$
T_{TSR}	Thermal Shutdown Released Temperature	Junction Temperature		95		$^{\circ}C$
R_{LOW}	Low Output Nch Tr. ON Resistance (D/F version)	$V_{IN} = 4.0V, V_{CE} = 0V$		50		Ω
I_{DELAY}	DELAY pin Current (DELAY pin version)	$V_{IN} = 4.0V$	<input type="checkbox"/> 0.7	1.2	<input type="checkbox"/> 1.7	μA

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}C$) except Output Noise, Ripple Rejection, Dropout Voltage at 1A Output Current and Load Regulation and Thermal Shutdown.

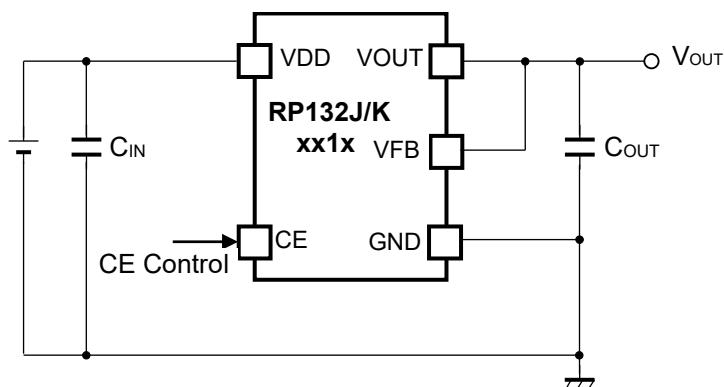
APPLICATION INFORMATION

Typical Application Circuits

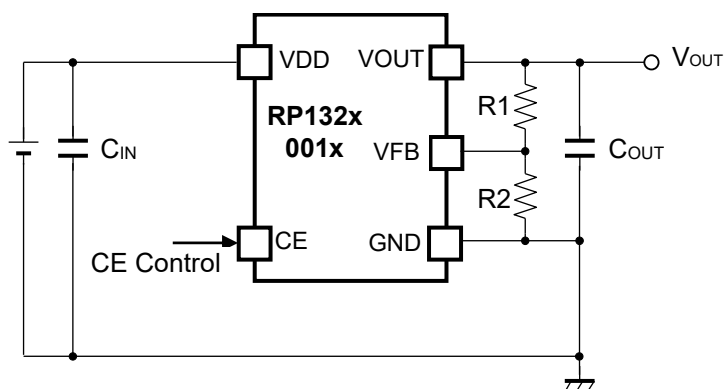
Fixed Output Voltage Type (HSOP-6J/ SOT89-5)



Fixed Output Voltage Type (TO-252-5-P2/ DFN(PLP)1820-6)

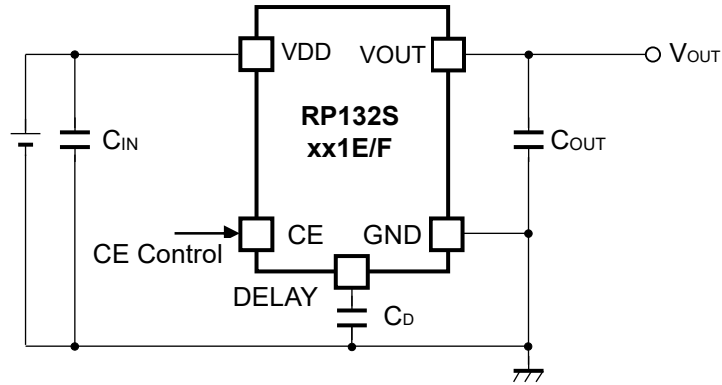
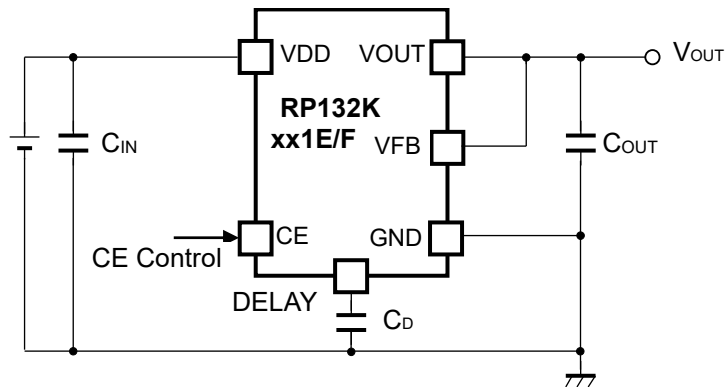
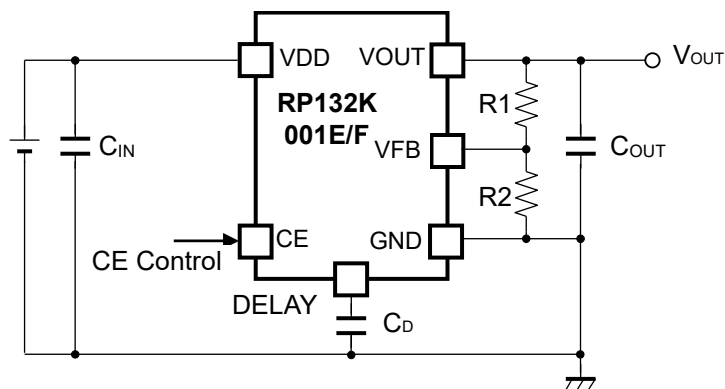


Adjustable Output Voltage Type (HSOP-6J / SOT89-5/ TO-252-5-P2 / DFN(PLP)1820-6)



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Fixed Output Voltage Type with DELAY pin (HSOP-6J)**Fixed Output Voltage Type with DELAY pin (DFN(PLP)1820-6)****Adjustable Output Voltage Type with DELAY pin (DFN(PLP)1820-6)**

Recommended External Components

V_{OUT}	Capacitors	
$V_{OUT} \leq 3.6V$	C_{IN} (C1)	Kyocera 2.2 μ F (size:1005) [CM05X5R225M06A]
	C_{OUT} (C2)	Kyocera 2.2 μ F (size:1608) [CM105X5R225K06AB]
$V_{OUT} > 3.6V$	C_{IN} (C1)	Kyocera 2.2 μ F (size:1005) [CM05X5R225K06A]
	C_{OUT} (C2)	Kyocera 4.7 μ F (size:1608) [CM105X5R475M06AB]

Please refer to "Technical Notes on Adjustable Output Voltage Type" when using R1 and R2 as output capacitors. Also refer to "Inrush Current Limit Time Settings" concerning with C_D .

Technical Notes on the External Components

When using this IC, consider the following points:

Phase Compensation

In this IC, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a 4.7 μ F or more capacitor C_{OUT} between V_{OUT} pin and GND pin, and as close as possible to the pins.

If a tantalum capacitor is used, and its ESR (Equivalent Series Resistance) of C_{OUT} is large, the loop oscillation may result. Because of this, select C_{OUT} carefully considering its frequency characteristics.

PCB Layout

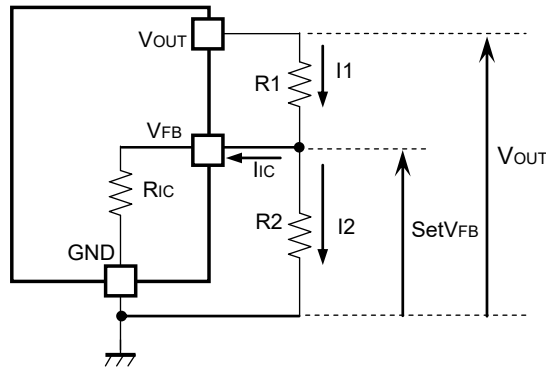
Make V_{DD} and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a 2.2 μ F or more capacitor C_{IN} between V_{DD} and GND pin with a capacitance value as "Recommendation value of the external capacitors" above or more, and as close as possible to the pins.

Set external components, especially the output capacitor C_{OUT} , as close as possible to the IC, and make wiring as short as possible.

When using the Adjustable Output Voltage Type, the transient response could be affected by the external resistors. Evaluate the circuit taking the actual conditions of use into account.

Output Voltage Setting Method (Adjustable Output Voltage Type)

RP132x081x can be adjusted the output voltage up to 5.5V by using the external divider resistors. Also, please use 16k Ω or less for R2 resistor. If the V_{FB} voltage is described as $setV_{FB}$, the output voltage can be set by using the following equations. $setV_{FB}$ is equal to 0.8V. The V_{OUT} pin of RP132x081x should be connected to the V_{FB} pin.



$$I1 = I_{ic} + I2 \dots\dots\dots (1)$$

$$I2 = \text{set}V_{FB} / R2 \dots\dots\dots (2)$$

Thus,

$$I1 = I_{ic} + \text{set}V_{FB} / R2 \dots\dots\dots (3)$$

Therefore,

$$V_{OUT} = \text{set}V_{FB} \times R1 \times I1 \dots\dots\dots (4)$$

Put Equation (3) into Equation (4), then

$$\begin{aligned} V_{OUT} &= \text{set}V_{FB} + R1(I_{ic} + \text{set}V_{FB} / R2) \\ &= \text{set}V_{FB} \times (1 + R1 / R2) + R1 \times I_{ic} \dots\dots\dots (5) \end{aligned}$$

In Equation (5), $R1 \times I_{ic}$ is the error-causing factor in V_{OUT} .

As for I_{ic} ,

$$I_{ic} = \text{set}V_{FB} / R_{ic} \dots\dots\dots (6)$$

Therefore, the error-causing factor $R1 \times I_{ic}$ can be described as follows.

$$\begin{aligned} R1 \times I_{ic} &= R1 \times \text{set}V_{FB} / R_{ic} \\ &= \text{set}V_{FB} \times R1 / R_{ic} \dots\dots\dots (7) \end{aligned}$$

For better accuracy, choosing $R1 \ll R_{ic}$ reduces this error.

Without the error-causing factor $R1 \times I_{ic}$, the output voltage can be calculated by the following equation

$$V_{OUT} = \text{set}V_{FB} \times ((R1 + R2) / R2) \dots\dots\dots (8)$$

R_{ic} of RP132x is approximately Typ.1.3MΩ ($T_a=25^\circ\text{C}$, this value is guaranteed by design.). The value could be affected by the temperature, therefore evaluate the circuit taking the actual conditions of use into account.

Inrush Current Limit Time Settings

The RP132xSeries include the circuit which can limit the inrush current at start-up to 500mA or less. The current limit time of B/D version is fixed internally as approximately Typ.500μs. On the other hand, the current limit times of E/F versions are adjustable by controlling the DELAY pin value, which is the capacitance value connected between DLEAY pin and GND pin. The relation between Inrush Current Limit Time (t_D [s]) and the DELAY pin capacitance (C_D [F]) can be described in the following equation.

$$t_D = (C_D + 70 \times 10^{-12}) \times 0.525 \times 10^6$$

When not using C_D on E/F versions, DELAY pin should be open. In this case, $C_D=0$ is applied to the above equation and as a result, $37\mu s$ can be obtained. That means, when using C_D on E/F versions, the inrush current limit time will be more than $37\mu s$. Please note that during the inrush current limit time, the load current cannot be more than the limited current.

ESR vs. Output Current

The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below. The conditions when the white noise level is under $40\mu V$ (Avg.) are marked as the hatched area in the graph.

Measurement Conditions

Frequency Band : 10Hz to 2MHz

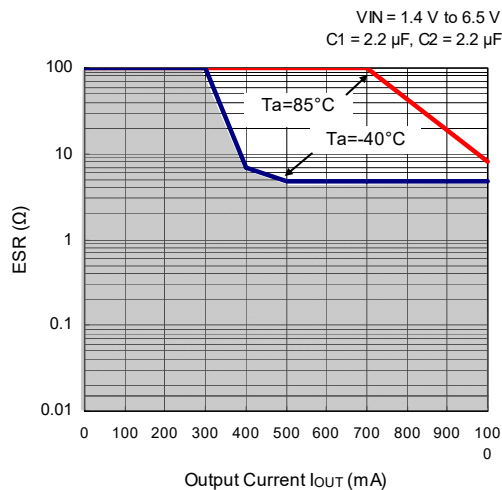
Temperature : $-40^\circ C$ to $85^\circ C$

Hatched Area : Noise level is under $40\mu V$ ms (Avg.)

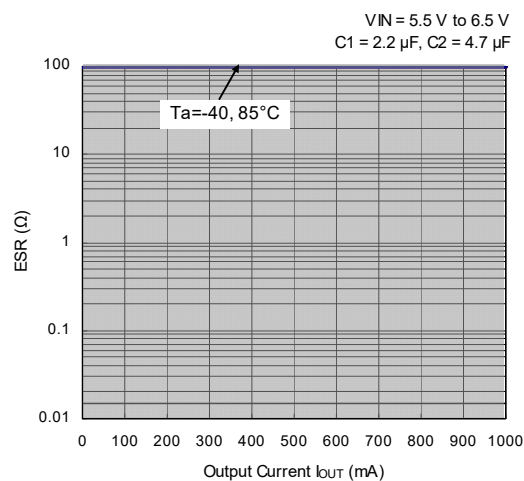
C_{IN} (C1) : $2.2\mu F$ (Kyocera CM05X5R225M06A)

C_{OUT} (C2) : $2.2\mu F$ ($V_{OUT} = 0.8V$, Kyocera CM105X5R225K06AB)
 $4.7\mu F$ ($V_{OUT} = 5.5V$, Kyocera CM105X5R475M06AB)

RP132x081x



RP132x551x

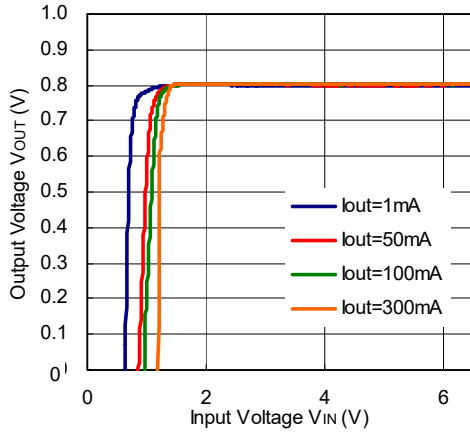


TYPICAL CHARACTERISTICS

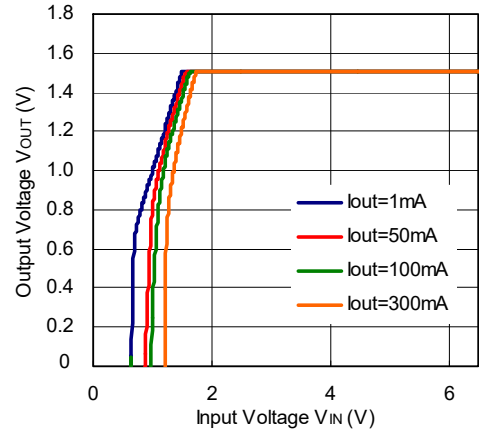
Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Output Voltage vs. Input Voltage (Ta=25°C)

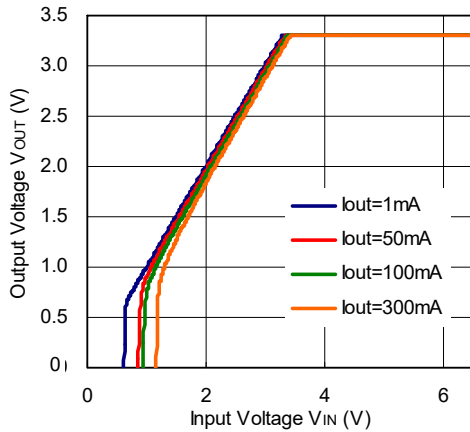
RP132x081x



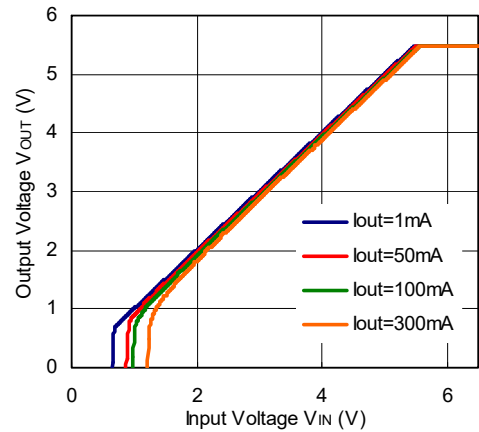
RP132x151x



RP132x331x

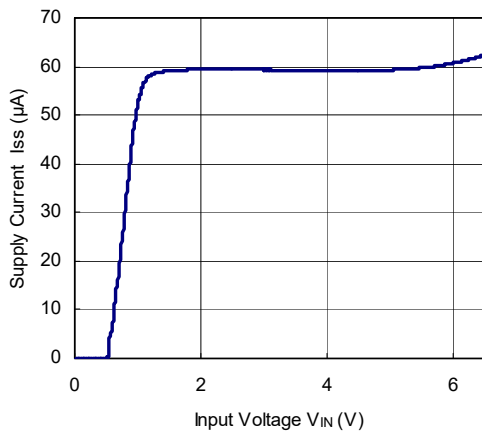


RP132x551x

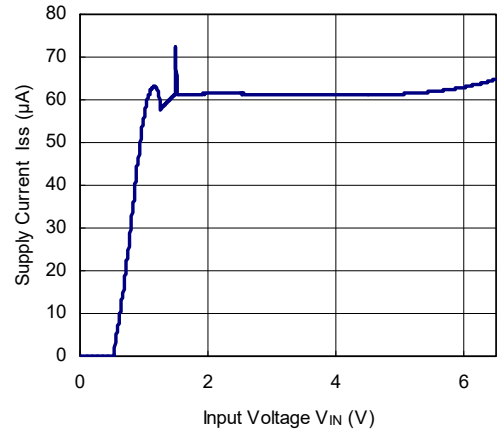


2) Supply Current vs. Input Voltage (Ta=25°C)

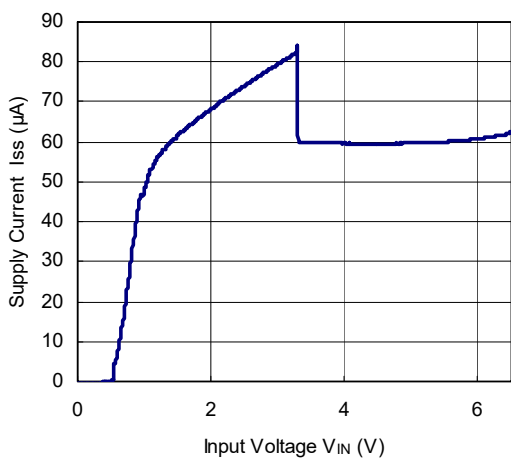
RP132x081x



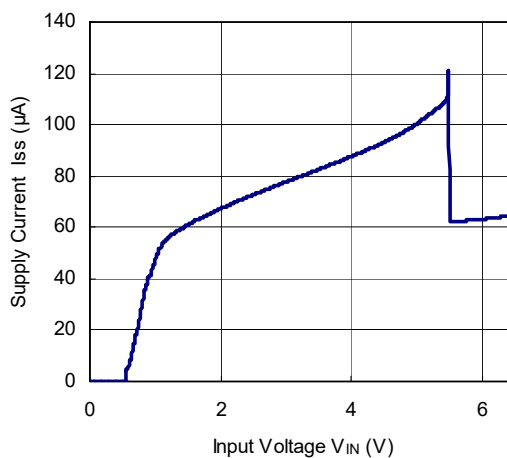
RP132x151x



RP132x331x

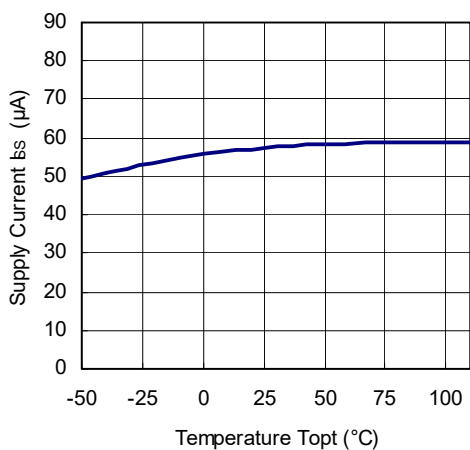


RP132x551x

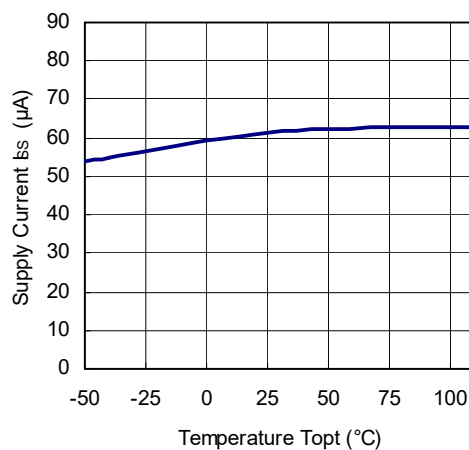


3) Supply Current vs. Temperature

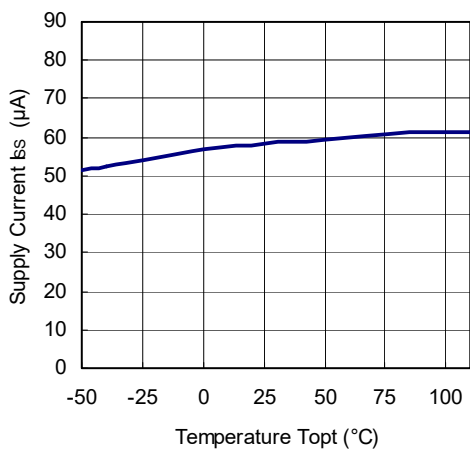
RP132x081x



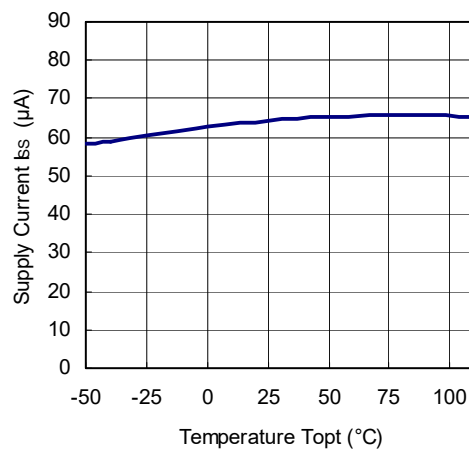
RP132x151x



RP132x331x



RP132x551x

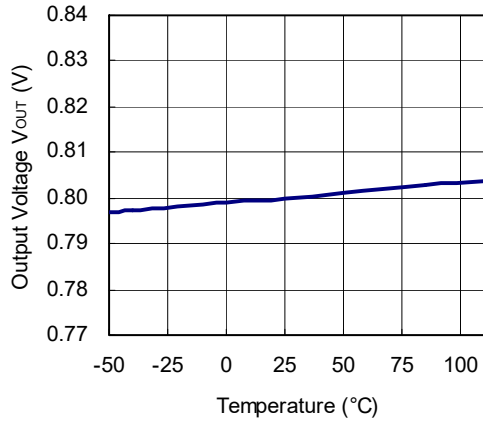


RP132x

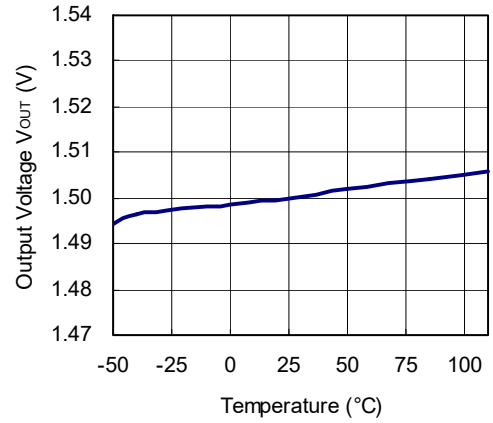
NO.EA-265-190408

4) Output Voltage vs. Temperature

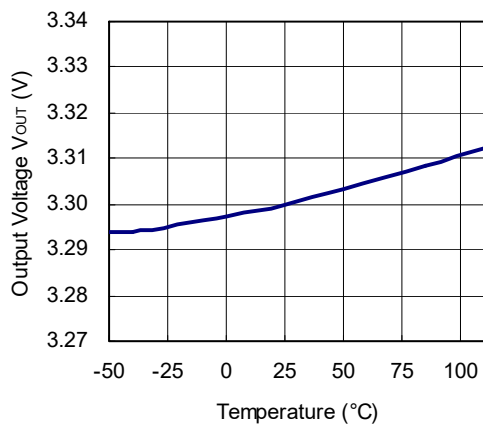
RP132x081x



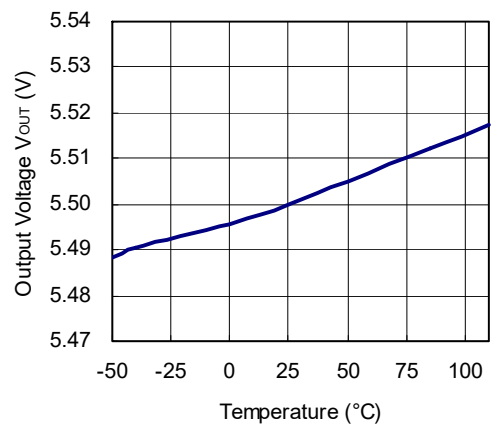
RP132x151x



RP132x331x

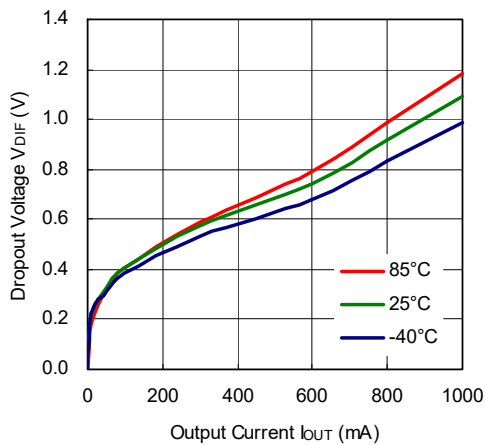


RP132x551x

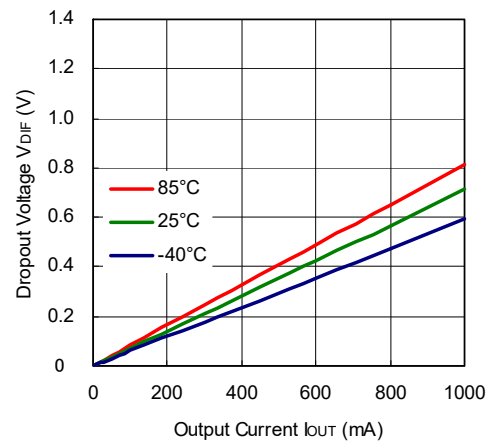


5) Dropout Voltage vs. Output Current

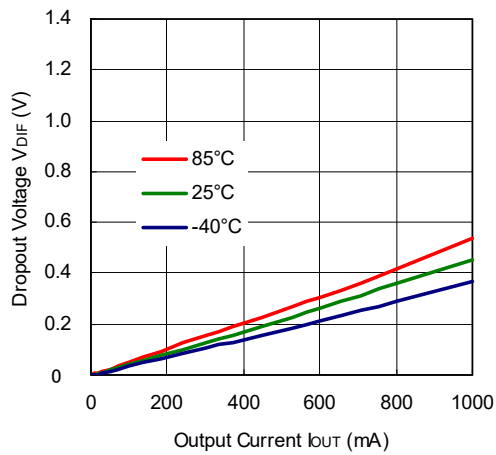
RP132x081x



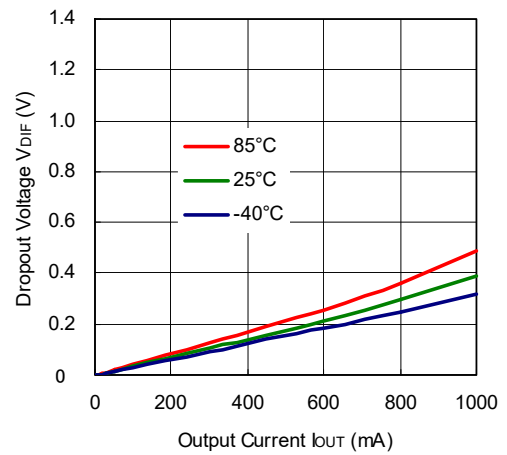
RP132x151x



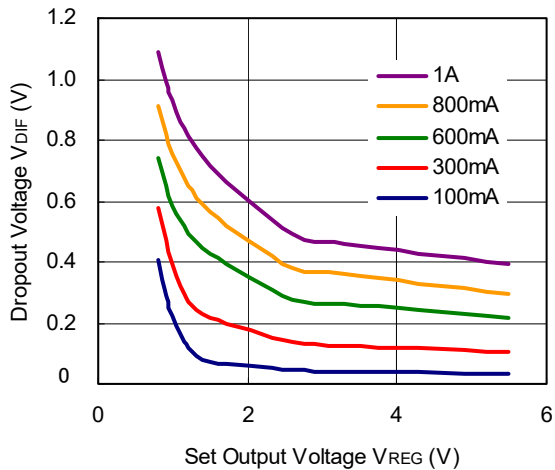
RP132x331x



RP132x551x

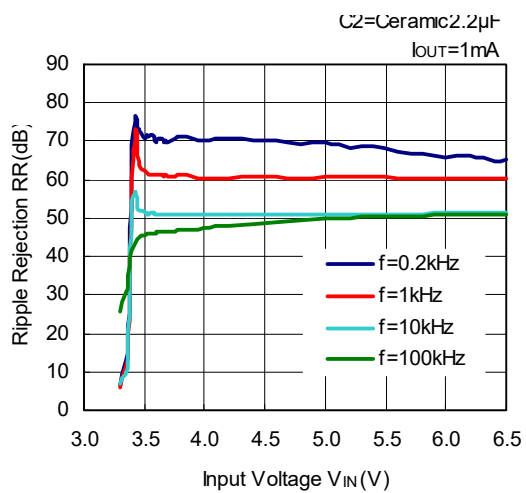


6) Dropout Voltage vs. Set Output Voltage

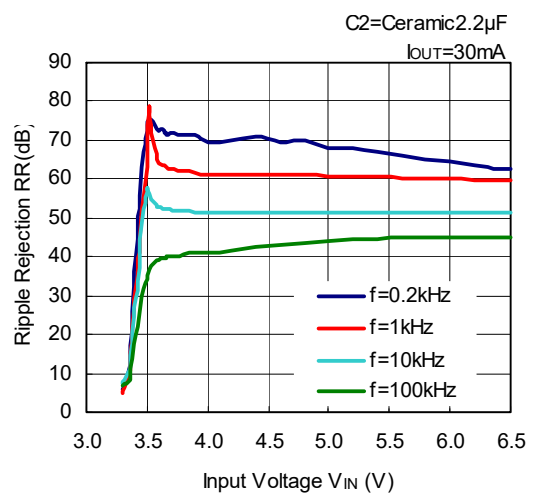


7) Ripple Rejection vs. Input Voltage (C_{IN} =none, Ripple=0.2Vp-p, T_a =25°C)

RP132x331x



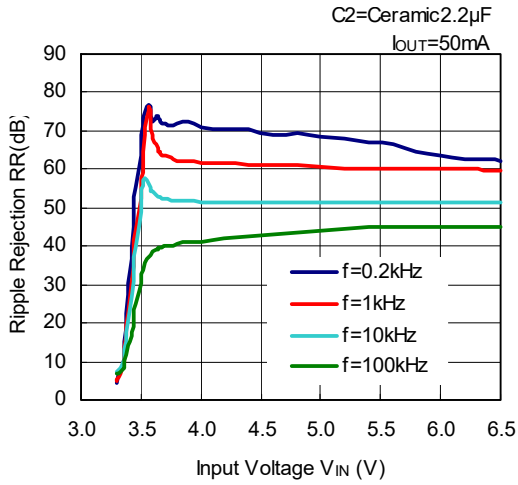
RP132x331x



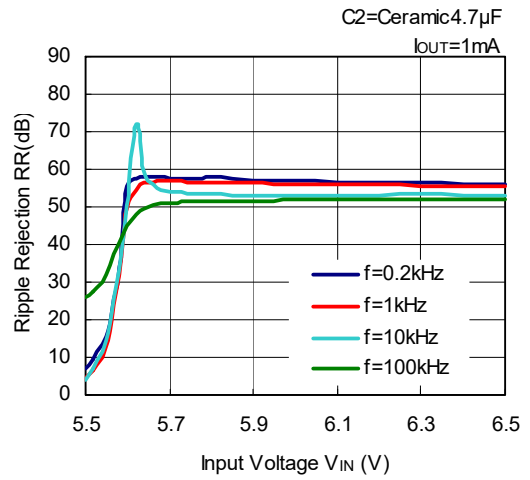
RP132x

NO.EA-265-190408

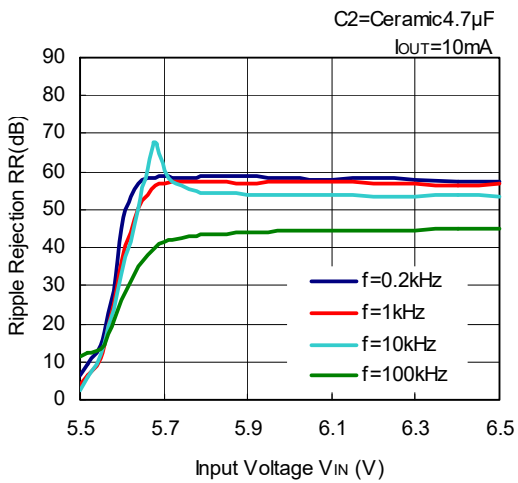
RP132x331x



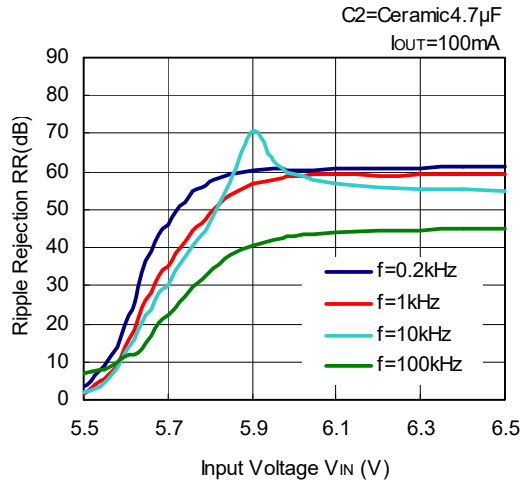
RP131x551x



RP132x551x

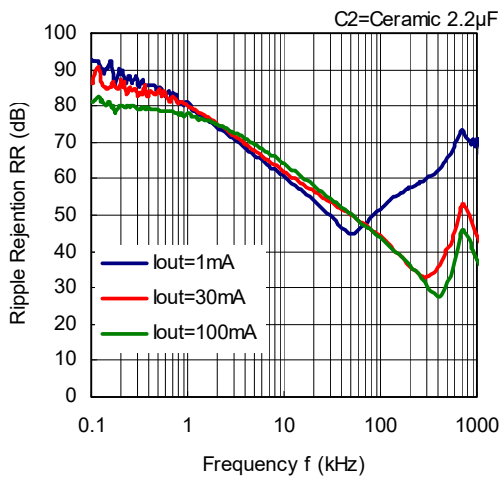


RP132x551x

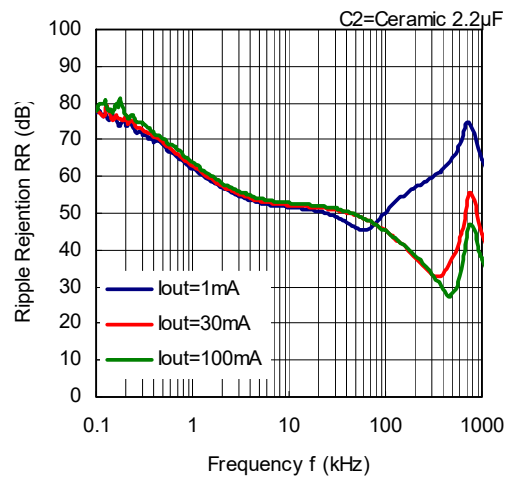


8) Ripple Rejection vs. Frequency (C_{IN} =none, T_a=25°C)

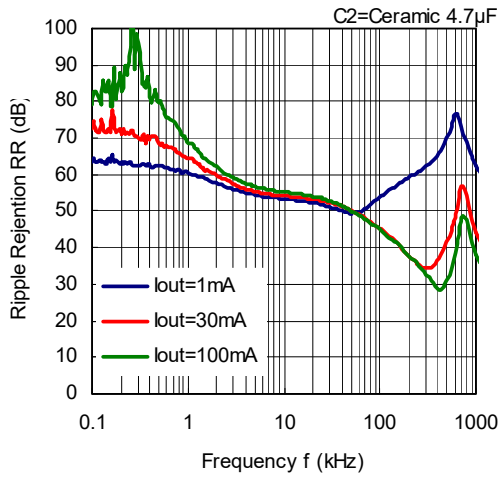
RP132x081x



RP132x331x

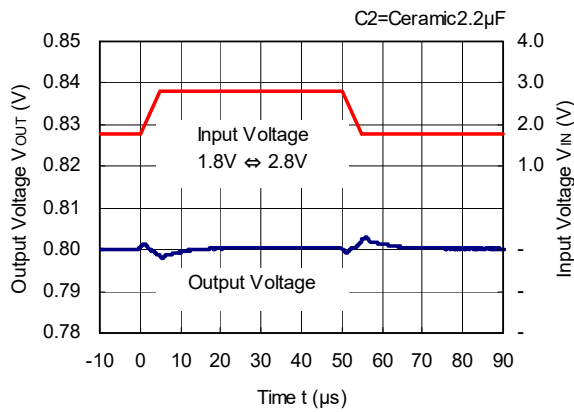


RP132x551x

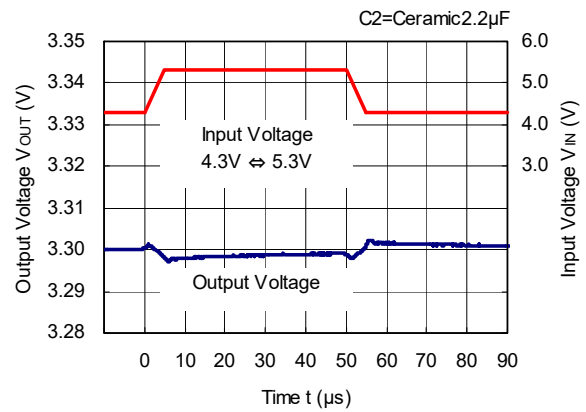


9) Input Transient Response (C_{IN} =none, I_{OUT}=100mA, tr=tf=5µs, Ta=25°C)

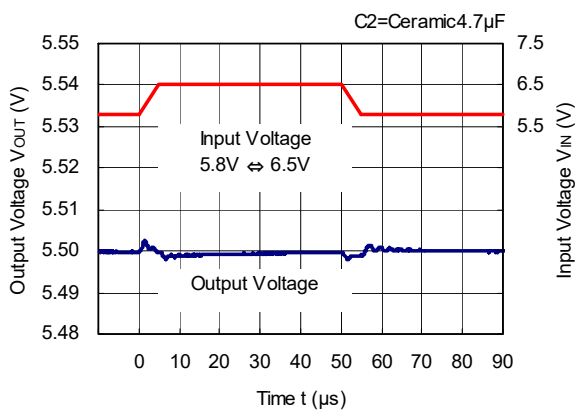
RP132x081x



RP132x331x



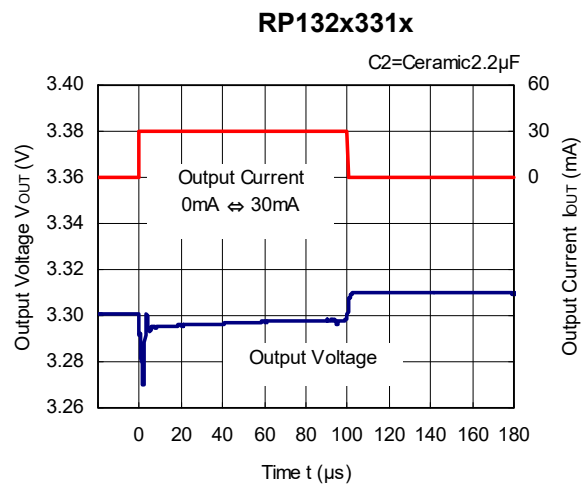
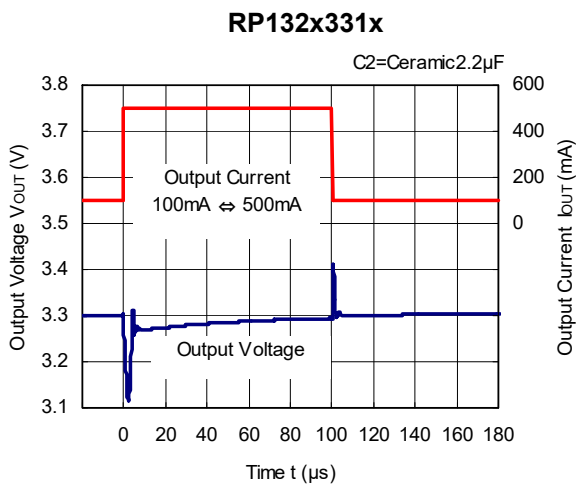
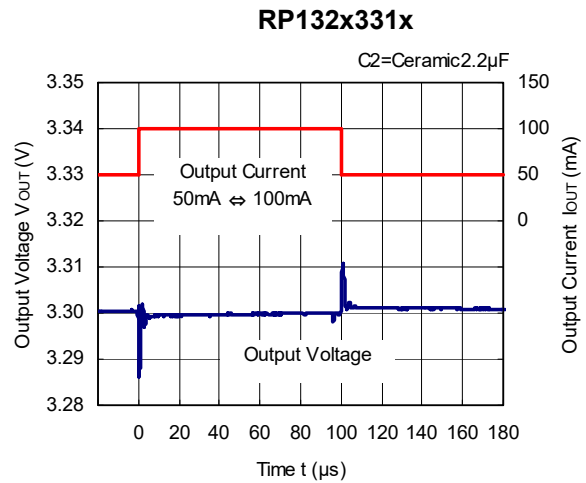
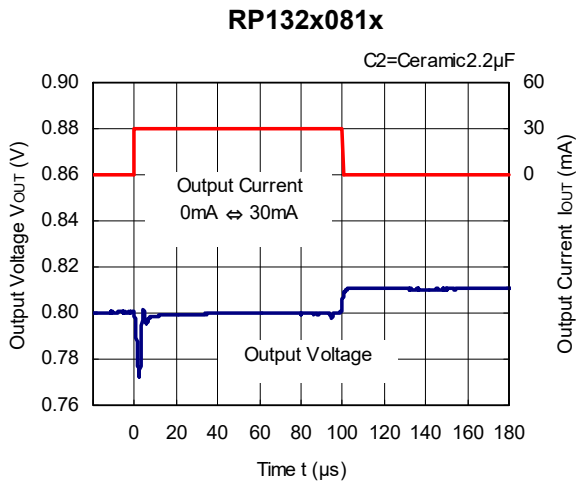
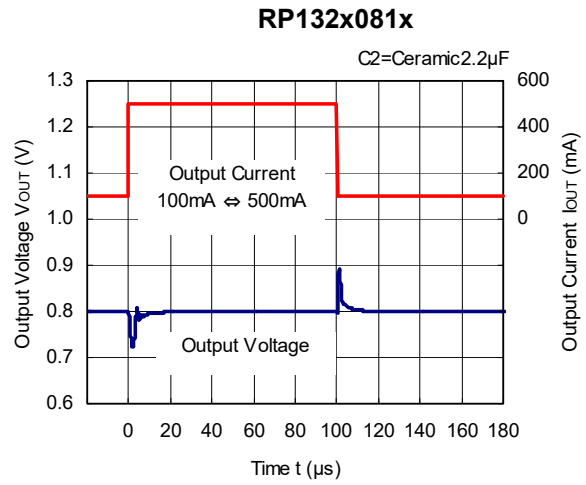
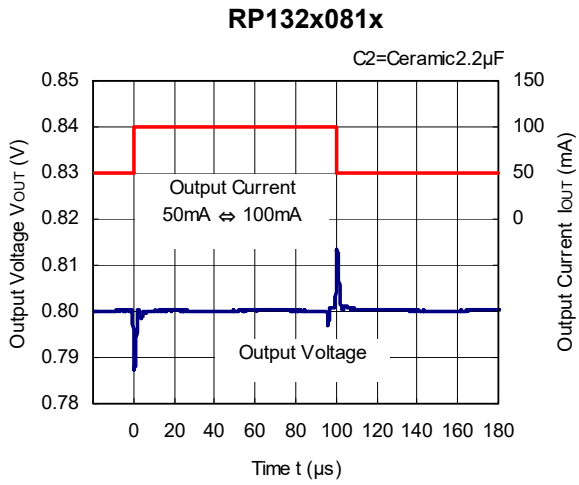
RP132x551x



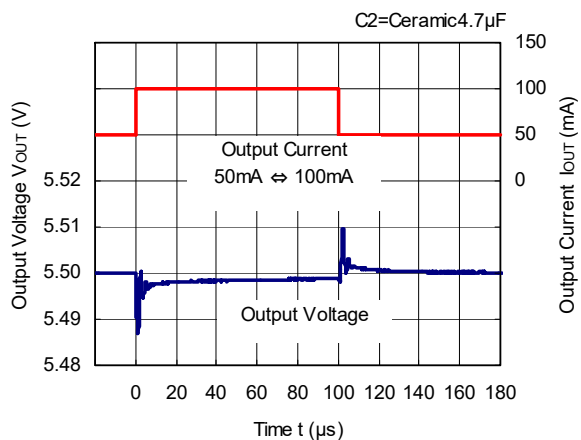
RP132x

NO.EA-265-190408

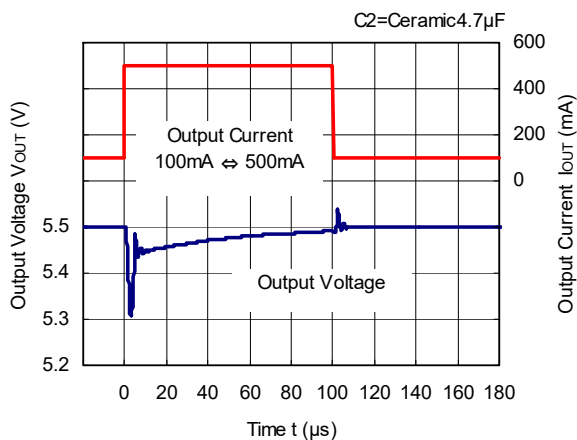
10) Load Transient Response ($V_{IN}=V_{OUT}+1.0V$, C_{IN} =Ceramic $2.2\mu F$, $t_r=t_f=0.5\mu s$, $T_a=25^\circ C$)



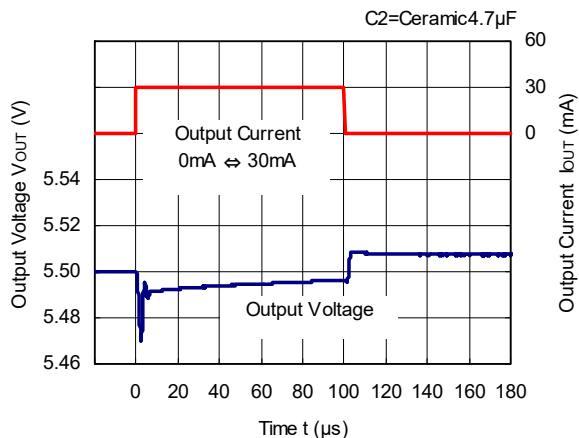
RP132x551x



RP132x551x

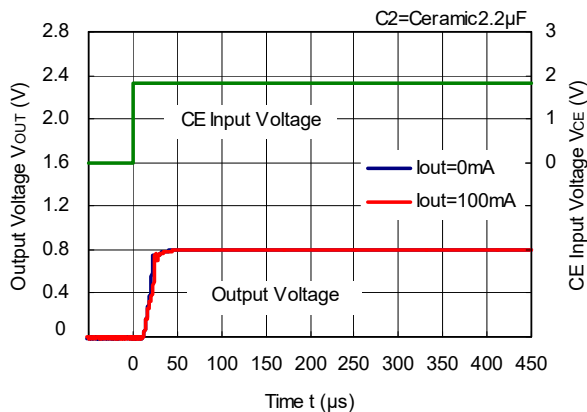


RP132x551x

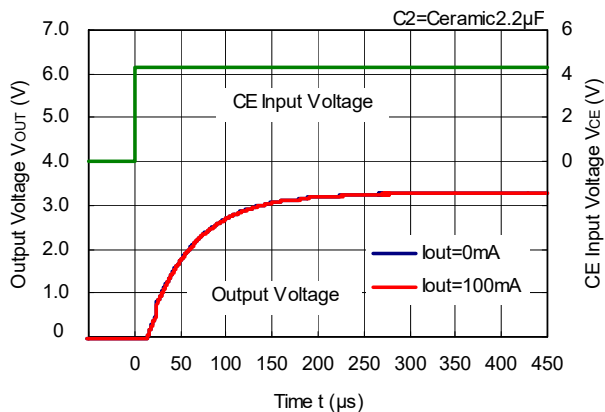


11) Turn on Speed with CE pin (C_{IN} =Ceramic 2.2μF, Ta=25°C)

RP132x081x



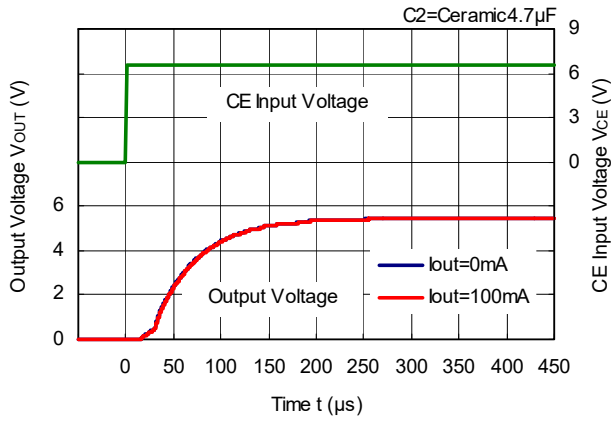
RP132x331x



RP132x

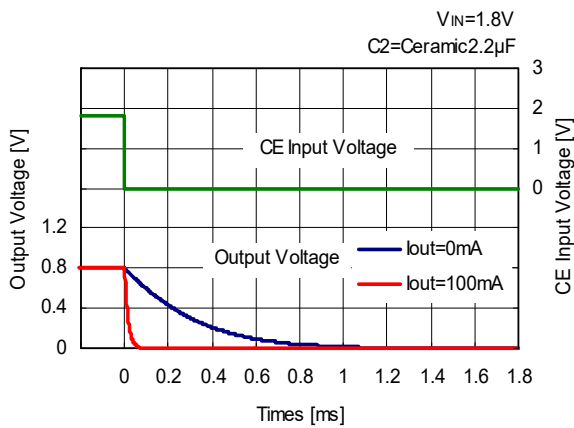
NO.EA-265-190408

RP132x551x

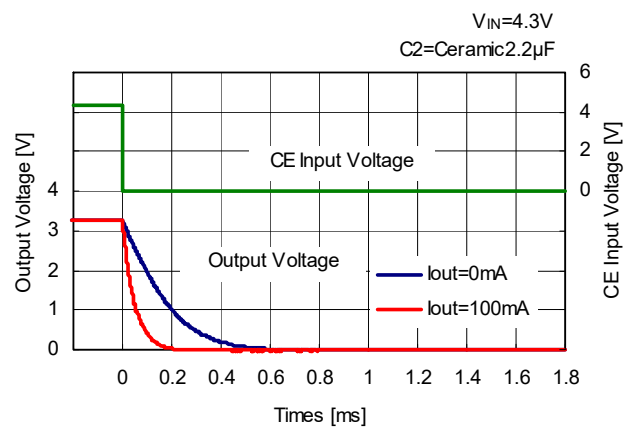


12) Turn off Speed with CE pin (D version) (C_{IN} =Ceramic 2.2 μ F, $T_a=25^\circ C$)

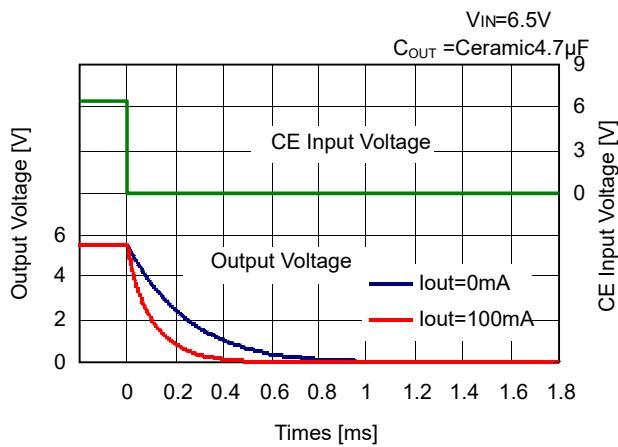
RP132x081D



RP132x331D

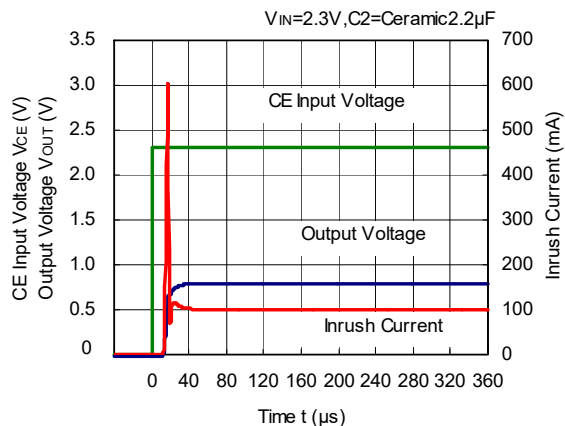


RP132x551D

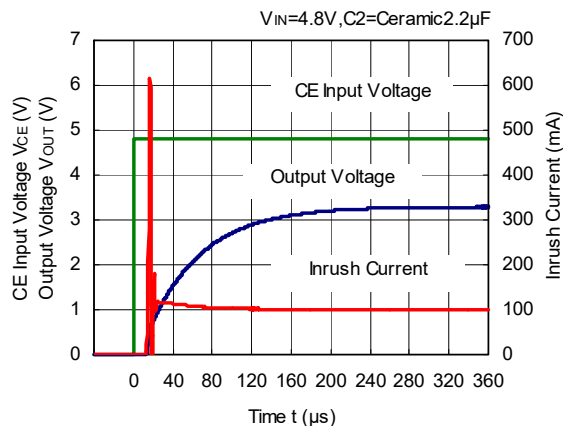


13) Inrush Current (C_{IN} =Ceramic 2.2 μ F, I_{OUT} =100mA, T_a =25 $^{\circ}$ C)

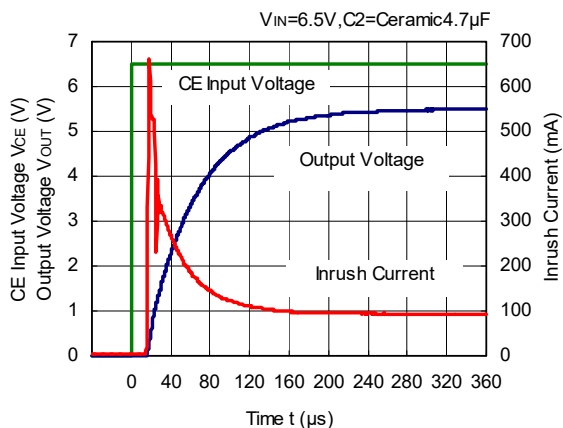
RP132x081x



RP132x331x

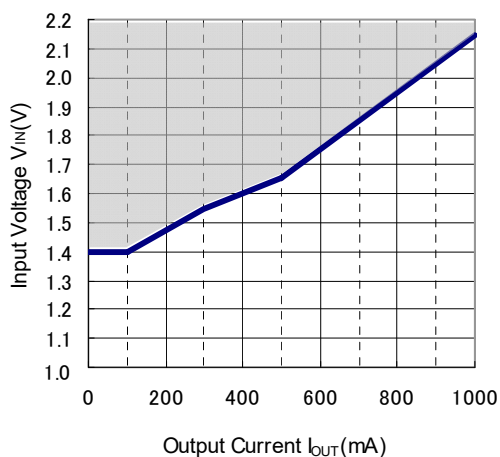


RP132x551x



14) Minimum Operating Voltage

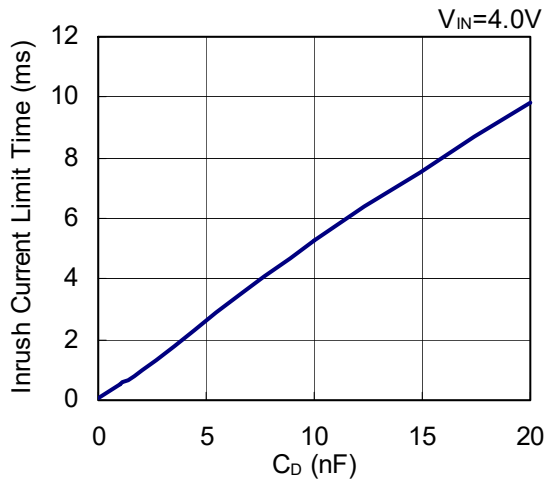
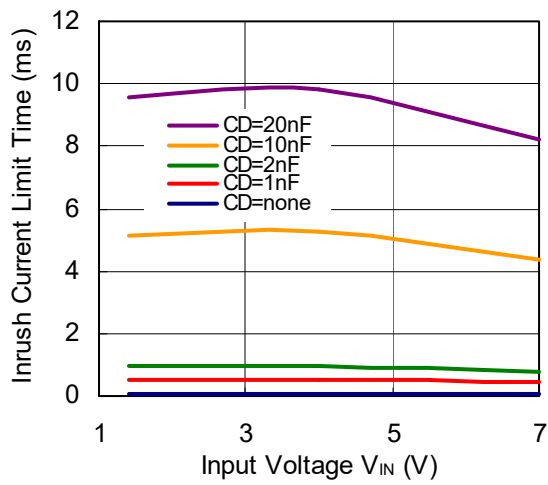
RP132x081x



The operation range that can output 0.8V is shown by the hatched area in the graph.

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15) Inrush Current Limit Time vs. C_D Capacitance (E / F Version)**RP132x081x****16) Inrush Current Limit Time vs. Input Voltage (E / F Version)****RP132x081x**

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.2 mm × 34 pcs

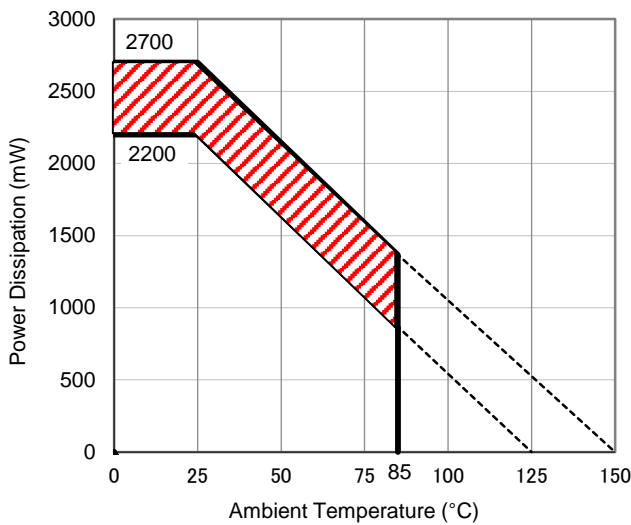
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

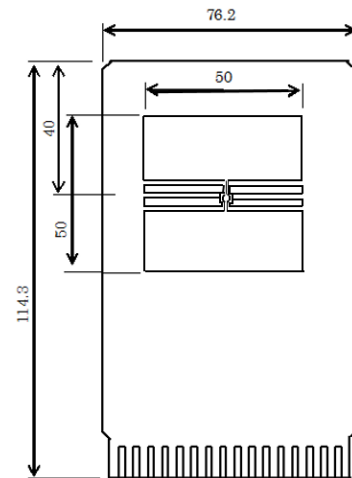
Item	Measurement Result
Power Dissipation	2200 mW
Thermal Resistance (θja)	θja = 45°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 18°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



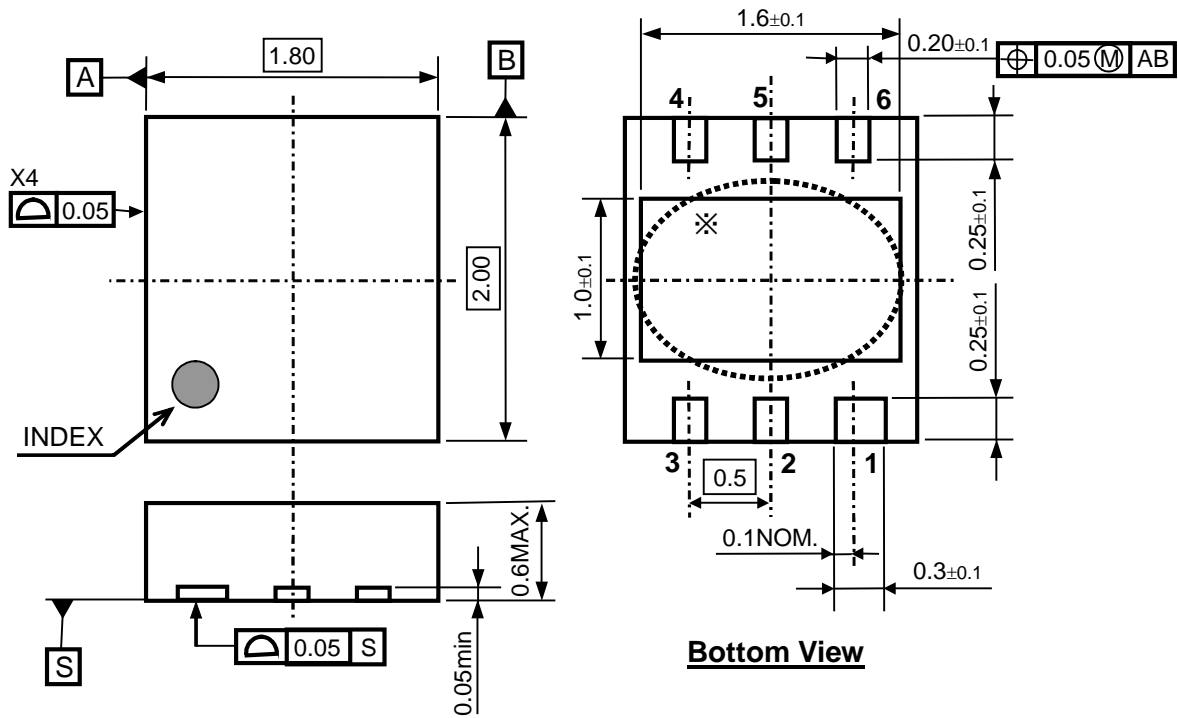
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years



DFN(PLP)1820-6 Package Dimensions (Unit: mm)

* The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 13 pcs

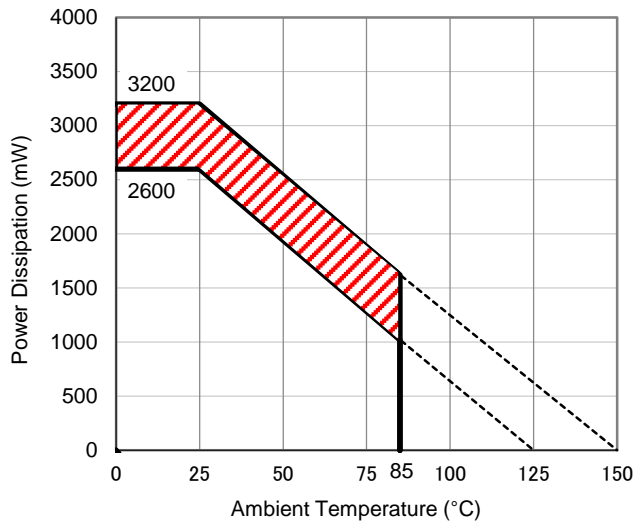
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

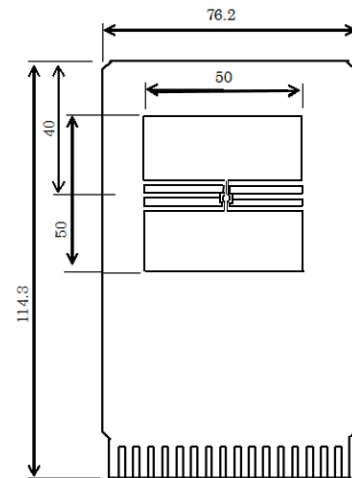
Item	Measurement Result
Power Dissipation	2600 mW
Thermal Resistance (θja)	θja = 38°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 13°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



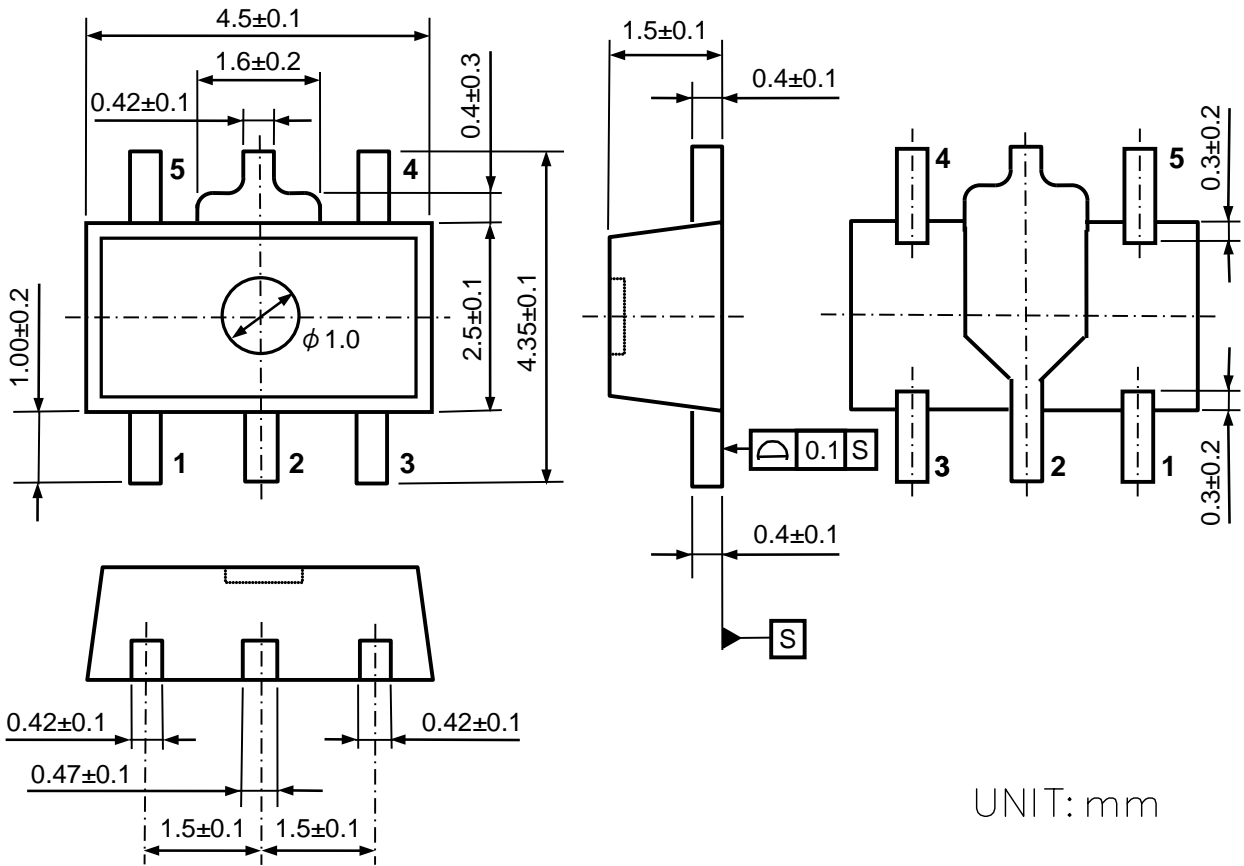
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years



SOT-89-5 Package Dimensions

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 28 pcs

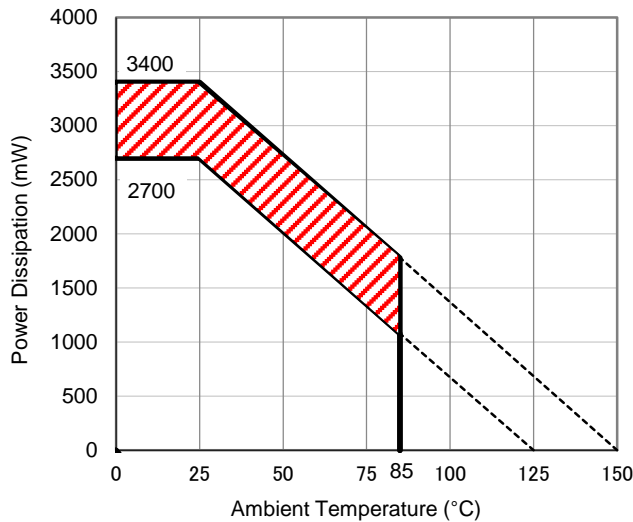
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

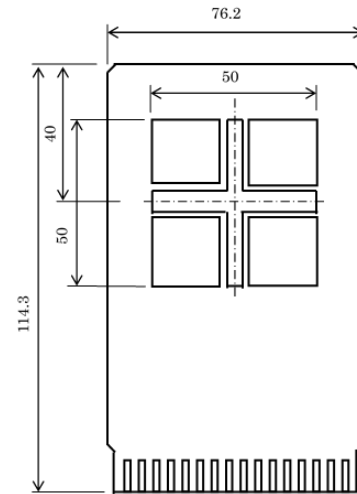
Item	Measurement Result
Power Dissipation	2700 mW
Thermal Resistance (θja)	θja = 37°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 7°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



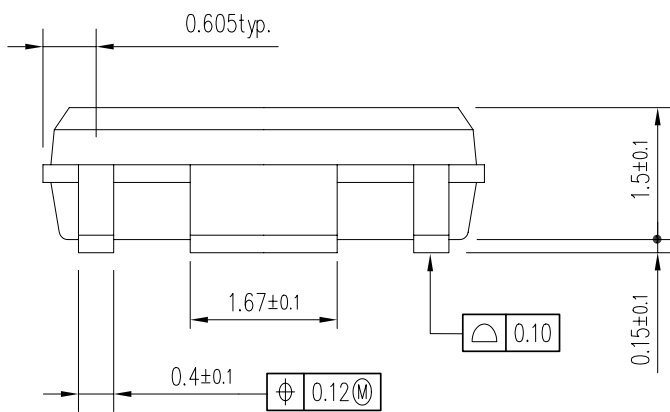
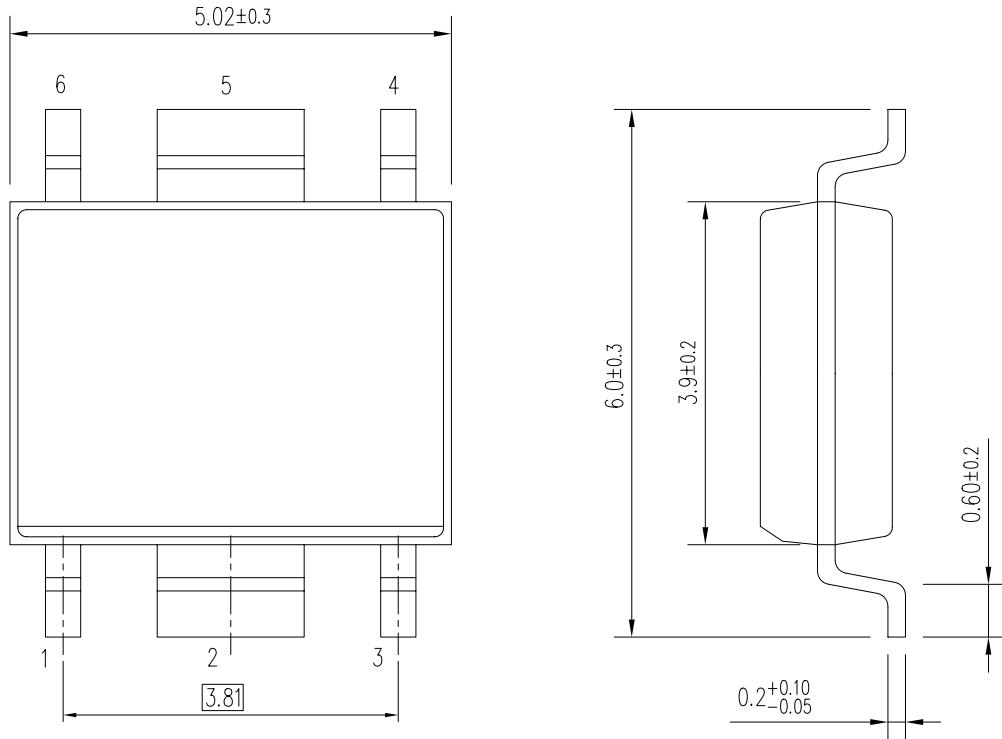
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years



UNIT: mm

HSOP-6J Package Dimensions

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

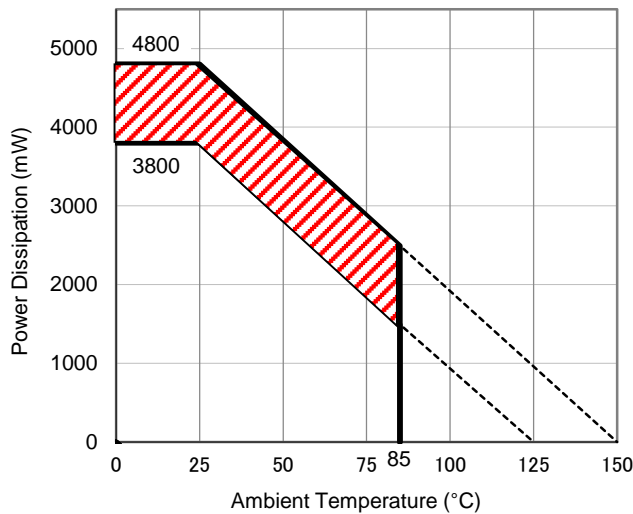
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 21 pcs

Measurement Result

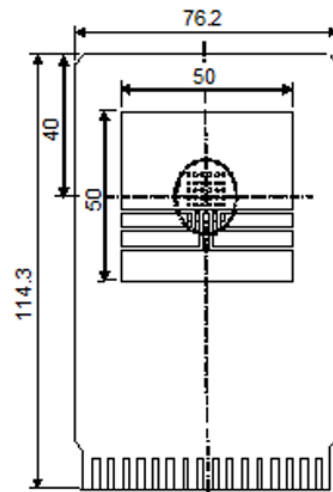
(Ta = 25°C, Tjmax = 125°C)

Item	Measurement Result
Power Dissipation	3800 mW
Thermal Resistance (θja)	θja = 26°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 7°C/W

θja: Junction-to-Ambient Thermal Resistance
ψjt: Junction-to-Top Thermal Characterization Parameter



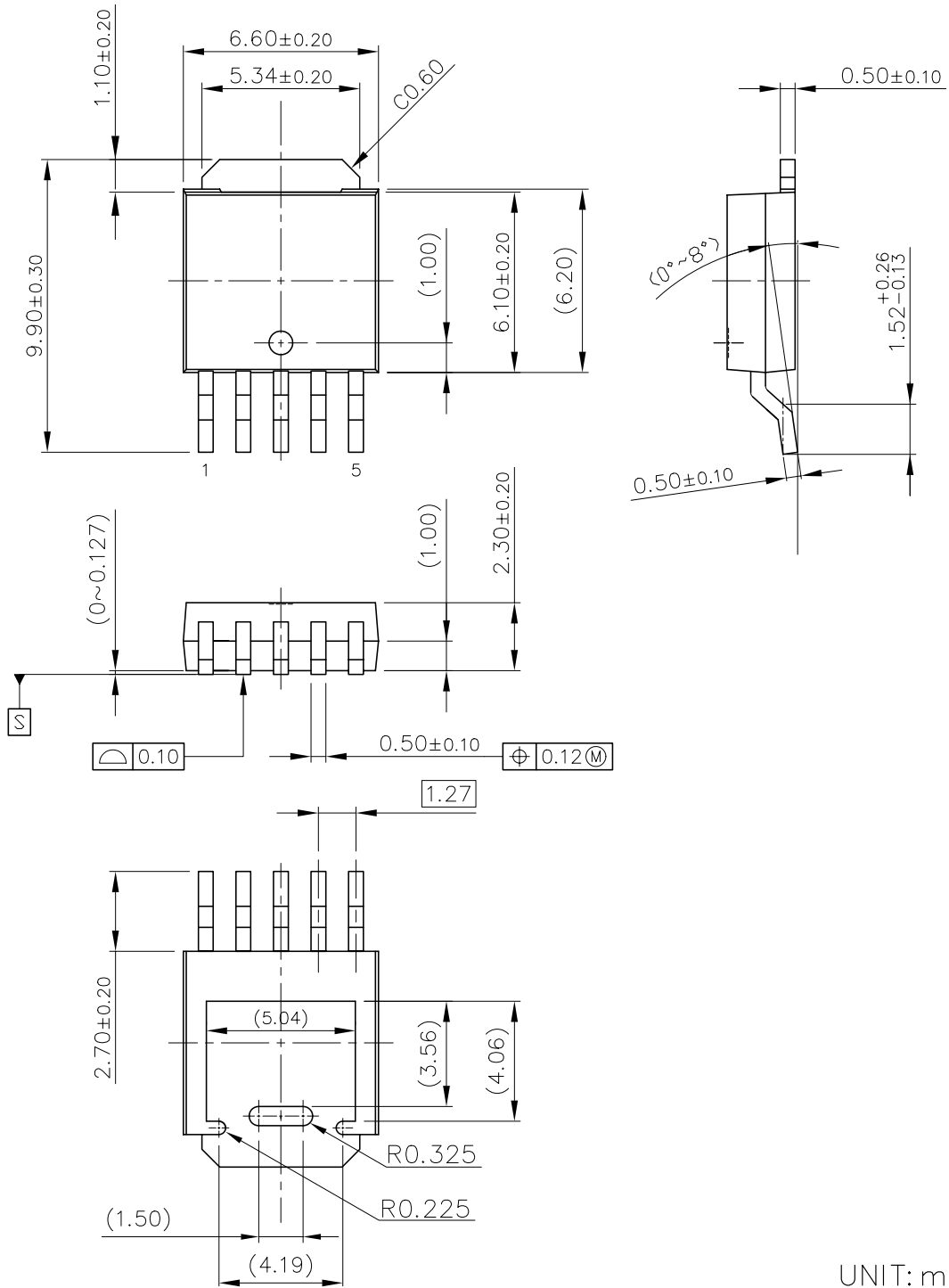
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years



UNIT: mm

TO-252-5-P2 Package Dimensions

* The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.



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