

High Accuracy Voltage Detector with Delay Function (Internal Counter Type)

No.EA-306-210329

OUTLINE

The RP300x is a voltage detector (VD) IC with a built-in output delay circuit. The RP300x is available in internally fixed detector threshold type. When the V_{DD} voltage becomes lower than the preset voltage, the RP300xxxxA/C generates a “L” reset signal and the RP300xxxxB⁽¹⁾ generates a “H” reset signal. The detector threshold accuracy is as high as $\pm 1.0\%$ when $-V_{SET}^{(2)} < 1.7\text{ V}$ and $\pm 0.8\%$ when $1.7\text{ V} \leq -V_{SET}$.

The reset output signal remains asserted for 50 ms, 100 ms⁽³⁾ or 200 ms after the V_{DD} voltage rises above the threshold voltage or when manual reset is canceled. The RP300x is designed to ignore fast transients on the V_{DD} pin. The output delay time accuracy is as high as $\pm 5.0\%$. The RP300x is available in an Nch open drain output type or in a CMOS output type. The RP300x is offered in a small DFN(PLP)1010-4B package or in a SOT-23-5 package.

FEATURES

- Operating Voltage Range (Maximum Rating) 0.72 V to 5.50 V (6.0V)
- Supply Current Typ. 0.95 μA ($-V_{SET} = 3.08\text{ V}$, $V_{DD} = 3.18\text{ V}$)
- Detector Threshold Range 1.1 V, 2.32 V, 2.63 V, 2.7 V, 2.8 V, 2.93 V, 3.08 V, 4.2 V, 4.38 V, 4.6 V
- Detector Threshold Accuracy $\pm 1.0\%$ ($-V_{SET} < 1.7\text{ V}$), $\pm 0.8\%$ ($1.7\text{ V} \leq -V_{SET}$)
- Detector Threshold Temperature Coefficient Typ. $\pm 50\text{ ppm}/^\circ\text{C}$
- Released Output Delay Time Typ. 50 ms, 100 ms (Custom IC), 200 ms
- Released Output Delay Time Accuracy $\pm 5\%$ ($T_a = 25^\circ\text{C}$), $\pm 15\%$ ($-40^\circ\text{C} \leq T_a \leq 85^\circ\text{C}$)
- Output Type Nch Open Drain output, CMOS Output
- Reset Signal Active-low, Active-high (Custom IC)
- Package DFN(PLP)1010-4B (1.0 mm x 1.0 mm x 0.6 mm)
SOT-23-5 (2.9 mm x 2.8 mm x 1.1 mm)

APPLICATIONS

- Voltage monitoring for handheld communication equipment, camera and VCRs.
- Voltage monitoring for battery-powered equipment

⁽¹⁾ RP300xxxxB is a custom IC. For more information about a custom IC, please contact our sales representatives.

⁽²⁾ $-V_{SET}$ is defined as a preset detector threshold.

⁽³⁾ Delay time of 100ms is offered as a custom IC.

SELECTION GUIDE

With the RP300x, the detector threshold, the package type, the released output delay time and the output type are user-selectable options.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP300Kxy*(z)-TR	DFN(PLP)1010-4B	10,000 pcs	Yes	Yes
RP300Nxy*(z)-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes

xx: Specify $-V_{SET}$ from 1.1 V (11), 2.32 V (23), 2.63 V (26), 2.7 V (27), 2.8 V (28), 2.93 V (29), 3.08 V (30), 4.2 V (42), 4.38 V (43), 4.6 V (46).

z: If $-V_{SET}$ includes the 3rd digit, indicate the digit of 0.01 V.

Ex. If $-V_{SET}$ is 2.63 V, indicate as RP300x26xx3-TR-x.

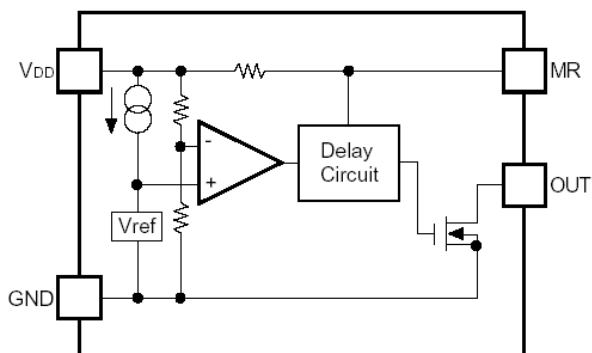
y: Specify the released output delay time.

- (A) 50 ms
- (B) 100 ms (custom IC)
- (D) 200 ms

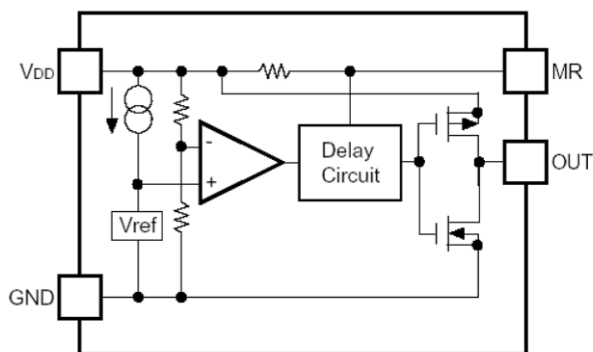
*: Specify the output type.

- (A) Nch Open Drain Output
- (B) Nch Open Drain Inverting Output (custom IC)
- (C) CMOS Output

BLOCK DIAGRAMS

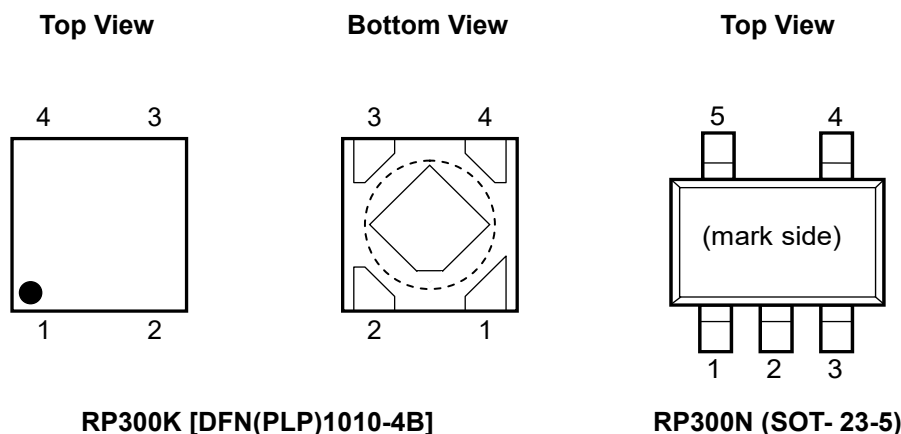


RP300xxxxA/B (Nch Open Drain Output)



RP300xxxxC (CMOS Output)

PIN DESCRIPTION



RP300K Pin Description

Pin No.	Symbol	Pin Description
1	OUT	Output Pin RP300xxxxA/C: asserts an active-low reset signal when a voltage drops below the detector threshold. RP300xxxxB: asserts an active-high reset signal when a voltage drops below the detector threshold. (custom IC)
2	MR	Manual Reset Input Pin: active-low
3	GND	Ground Pin
4	VDD	Power Supply Pin

The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board. If not, the tab can be left open.

RP300N Pin Description

Pin No.	Symbol	Description
1	MR	Manual Reset Input Pin: active-low
2	GND	Ground Pin
3	NC	No Connection
4	OUT	Output Pin RP300xxxxA/C: asserts an active-low reset signal when a voltage drops below the detector threshold. RP300xxxxB: asserts an active-high reset signal when a voltage drops below the detector threshold. (custom IC)
5	VDD	Power Supply Pin

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Rating	Unit
V _{IN}	Input Voltage		6.0	V
OUT	Output Voltage (Nch Open Drain Output)		-0.3 to 6.0	V
	Output Voltage (CMOS Output)		-0.3 to V _{DD} +0.3	
MR	Manual Reset Pin		-0.3 to V _{DD} +0.3	V
I _{OUT}	Output Current		20	mA
P _D	Power Dissipation ⁽¹⁾ (JEDEC STD. 51-7)	DFN(PLP)1010-4B	800	mW
		SOT-23-5	660	
T _j	Junction Temperature Range		-40 to 125	°C
T _{stg}	Storage Temperature Range		-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Unit
V _{DD}	Operating Voltage	0.72 to 5.5	V
T _a	Operating Temperature Range	-40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$.

RP300x Electrical Characteristics

($T_a = 25^{\circ}\text{C}$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
$-V_{\text{DET}}$	Detector Threshold ⁽¹⁾	$T_a = 25^{\circ}\text{C}$	$1.1\text{ V} \leq -V_{\text{SET}} < 1.7\text{ V}$	$\times 0.99$		$\times 1.010$	V
			$1.7\text{ V} \leq -V_{\text{SET}}$	$\times 0.992$		$\times 1.008$	V
		$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$	$1.1\text{ V} \leq -V_{\text{SET}} < 1.7\text{ V}$	0.982		1.018	V
			$1.7\text{ V} \leq -V_{\text{SET}}$	0.984		1.016	V
I_{SS1}	Supply Current 1	$V_{\text{DD}} = -V_{\text{SET}} - 0.1\text{ V}$, $I_{\text{OUT}} = 0\text{ A}$			3.2	μA	
I_{SS2}	Supply Current 2	$V_{\text{DD}} = -V_{\text{SET}} + 0.1\text{ V}$, $I_{\text{OUT}} = 0\text{ A}$			3.1	μA	
V_{DD}	Operating Voltage	$T_a = 25^{\circ}\text{C}$	0.72		5.5	V	
		$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$	0.80		5.5	V	
I_{OUT}	Output Current (Driver Output Pin)	Nch $V_{\text{DD}} = -V_{\text{SET}} - 0.1\text{ V}$ $V_{\text{DS}} = 0.3\text{ V}$	$-V_{\text{SET}} \geq 1.1\text{ V}$	0.45			mA
			$-V_{\text{SET}} \geq 1.6\text{ V}$	2.5			mA
			$-V_{\text{SET}} \geq 2.7\text{ V}$	4.8			mA
		Nch Inverting ⁽²⁾ $V_{\text{DD}} = -V_{\text{SET}} + 0.1\text{ V}$ $V_{\text{DS}} = 0.3\text{ V}$	$-V_{\text{SET}} \geq 1.1\text{ V}$	0.45			mA
			$-V_{\text{SET}} \geq 1.4\text{ V}$	2.5			mA
			$-V_{\text{SET}} \geq 2.5\text{ V}$	4.8			mA
		Pch CMOS $V_{\text{DD}} = -V_{\text{SET}} + 0.1\text{ V}$ $V_{\text{DS}} = -0.3\text{ V}$	$-V_{\text{SET}} \geq 1.1\text{ V}$	-0.15			mA
			$-V_{\text{SET}} \geq 1.6\text{ V}$	-0.45			mA
			$-V_{\text{SET}} \geq 2.7\text{ V}$	-0.8			mA
I_{LEAK}	Nch Driver Leakage Current	RP300xxxxA/C $V_{\text{DD}} = 5.5\text{ V}$ $V_{\text{DS}} = 5.5\text{ V}$				0.15	μA
		RP300xxxxB ⁽³⁾ $V_{\text{DD}} = -V_{\text{SET}} - 0.1\text{ V}$ $V_{\text{DS}} = 5.5\text{ V}$					
R_{MR}	MR Pin Pull-up Resistance		0.21	0.45	0.90	M Ω	
V_{IH}	MR Pin Input Voltage "H"	$V_{\text{DD}} \geq -V_{\text{SET}} + 0.1\text{ V}$	0.75 $\times V_{\text{DD}}$			V	
V_{IL}	MR Pin Input Voltage "L"	$V_{\text{DD}} \geq -V_{\text{SET}} + 0.1\text{ V}$			0.4	V	
t_{DELAY}	Released Output Delay Time ⁽⁴⁾	$V_{\text{DD}} = 0.8\text{ V} \rightarrow -V_{\text{SET}} + 1.0\text{ V}$	RP300xxxAx	47.5	50	52.5	ms
			RP300xxxBx ⁽⁵⁾	95	100	105	
			RP300xxxDx	190	200	210	
		$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$		t_{SET} $\times 0.85$		t_{SET} $\times 1.15$	%
$\Delta -V_{\text{DET}} / \Delta T_a$	Detector Threshold Temperature Coefficient	$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$		± 50		ppm/ $^{\circ}\text{C}$	

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}\text{C}$) except Detector Threshold Temperature Coefficient.

(1) $-V_{\text{DET}}$ is defined as an actual detector threshold and $-V_{\text{SET}}$ is defined as a preset detector threshold.

(2) Nch open drain inverting output type is only applicable to the RP300xxxxB which is a custom IC.

(3) The RP300xxxxB is a custom IC.

(4) t_{DELAY} is defined as an actual released output delay time and t_{SET} is defined as a preset released output delay time.

(5) The RP300xxxBx is a custom IC.

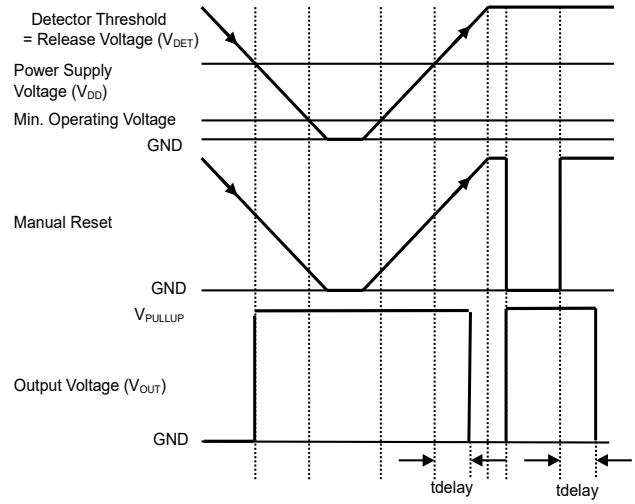
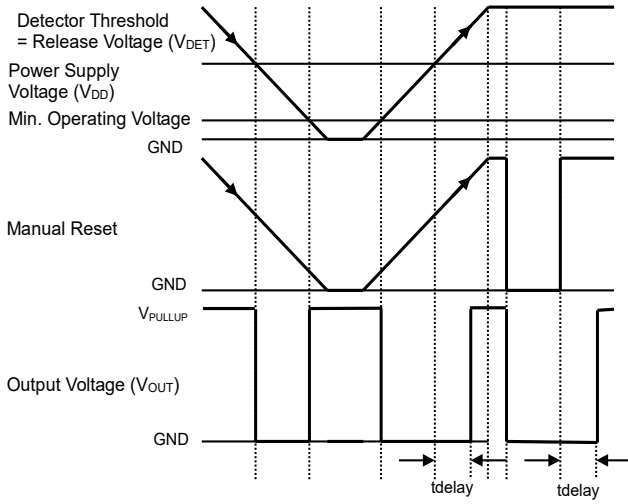
Product-specific Electrical Characteristics

The specifications surrounded by are guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$.

Product Name	-V_{DET} [V]					
	T_a = 25°C			-40°C ≤ T_a ≤ 85°C		
	Min.	Typ.	Max.	Min.	Typ.	Max.
RP300x11xx	1.089	1.100	1.111	1.081	1.100	1.119
RP300x23xx2	2.302	2.320	2.338	2.283	2.320	2.357
RP300x26xx3	2.609	2.630	2.651	2.588	2.630	2.672
RP300x27xx	2.679	2.700	2.721	2.657	2.700	2.743
RP300x28xx	2.778	2.800	2.822	2.756	2.800	2.844
RP300x29xx3	2.907	2.930	2.953	2.884	2.930	2.976
RP300x30xx8	3.056	3.080	3.104	3.031	3.080	3.129
RP300x42xx	4.167	4.200	4.233	4.133	4.200	4.267
RP300x43xx8	4.345	4.380	4.415	4.310	4.380	4.450
RP300x46xx	4.564	4.600	4.636	4.527	4.600	4.673

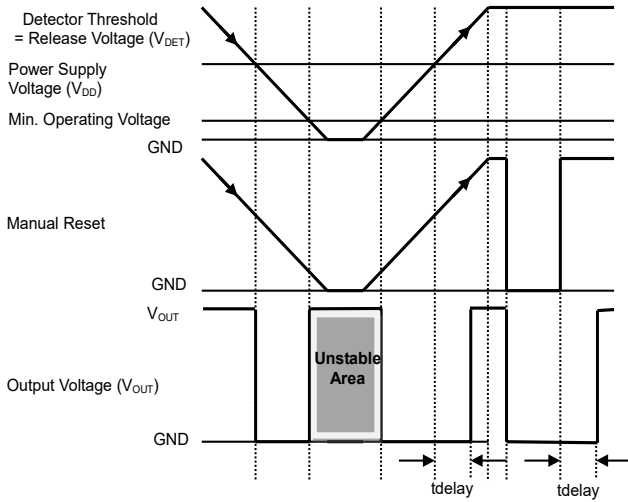
THEORY OF OPERATION

Timing Chart



RP300xxxxA Timing Chart

RP300xxxxB Timing Chart



RP300xxxxC Timing Chart

Release Output Delay Time (t_{DELAY})

t_{DELAY} is defined as follows.

1. Nch Open Drain Output

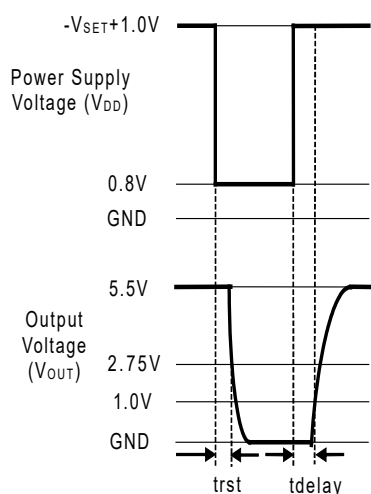
Release output delay time starts after the OUT pin is pulled up to 5.5 V with a 470 kΩ resistor, and the V_{DD} voltage is shifted from 0.8 V to $-V_{SET} + 1.0$ V. It ends when the output voltage reaches 1.0 V.

2. Nch Open Drain Inverting Output (custom IC)

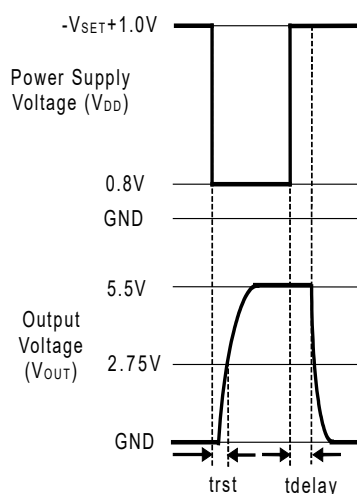
Release output delay time starts after the OUT pin is pulled up to 5.5 V with a 470 kΩ resistor, and the V_{DD} voltage is shifted from 0.8 V to $-V_{SET} + 1.0$ V. It ends when the output voltage reaches $V_{DD} / 2$ V.

3. CMOS Output

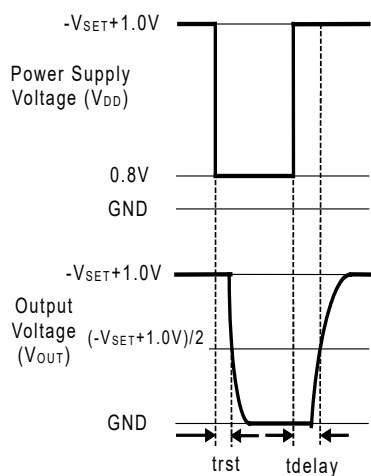
Release output delay time starts when the V_{DD} voltage is shifted from 0.8 V to $-V_{SET} + 1.0$ V and ends when the output voltage reaches $V_{DD} / 2$ V.



Nch Open Drain Output

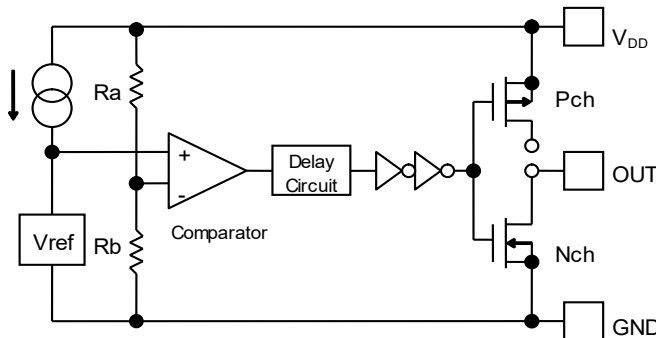


Nch Open Drain Inverting Output



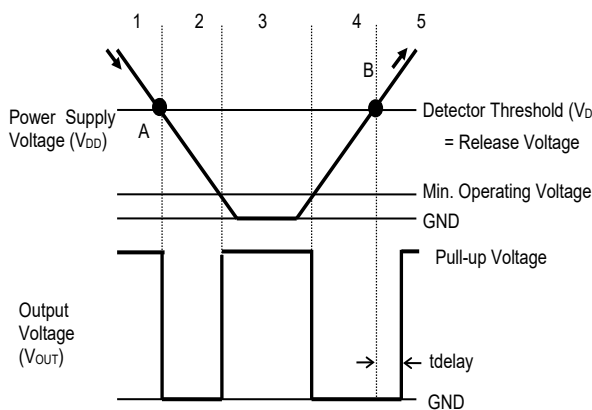
CMOS Output

RP300xxxxA/C Operating

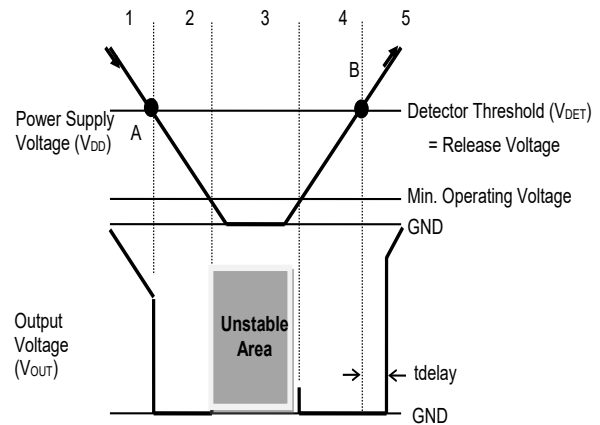


Block Diagram

- For CMOS Output, the Nch Tr. drain and the Pch Tr. drain are connected to the OUT pin inside the IC.
- For Nch Open Drain Output, the Nch Tr. drain is connected to the OUT pin inside the IC. Pull up the OUT pin or V_{DD} pin to the external voltage level.



Timing Chart (A Ver.)

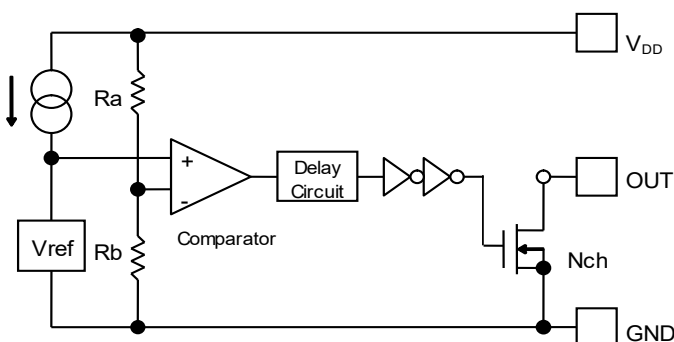


Timing Chart (C Ver.)

1. The output voltage is equalized to the V_{DD} voltage (CMOS Output), or to the pull-up voltage (Nch Open Drain Output).
2. The V_{DD} voltage drops to the detector threshold (A point) which means $V_{ref} \geq V_{DD} \times R_b / (R_a + R_b)$. The comparator output shifts from “L” to “H” voltage and the output voltage will be equalized to the GND voltage.
3. If the V_{DD} voltage is lower than the minimum operating voltage, the output voltage becomes unstable (CMOS Output). The output voltage is equalized to the pull-up voltage (Nch Open Drain Output).
4. The output voltage is equalized to the GND voltage.
5. The V_{DD} voltage becomes higher than the release voltage (B point) which means $V_{ref} < V_{DD} \times R_b / (R_a + R_b)$, and the comparator output shifts from “H” to “L” voltage, and the output voltage is equalized to the V_{DD} voltage (CMOS Output) or to the pull-up voltage (Nch Open Drain Output).

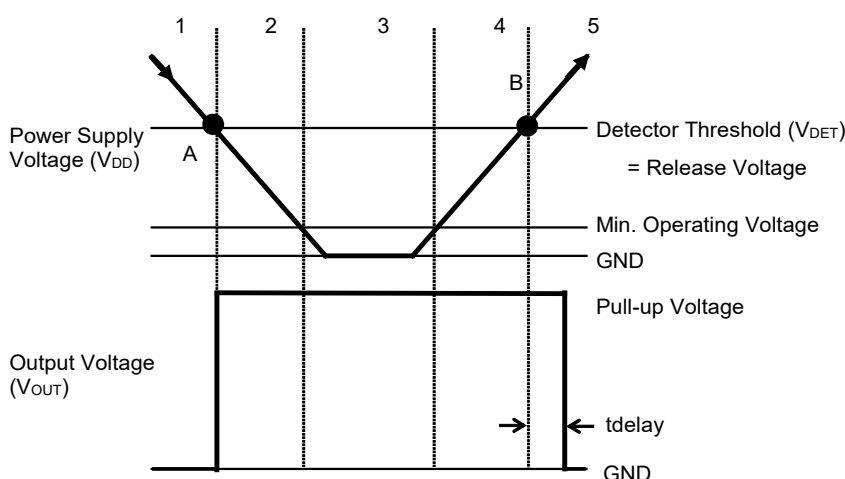
Note: There's no hysteresis between the V_{DD} voltage and the released voltage.

RP300xxxxB Operating



Block Diagram

- The Nch Tr. drain is connected to the OUT pin inside the IC. Pull up the OUT pin or VDD pin to the external voltage level.



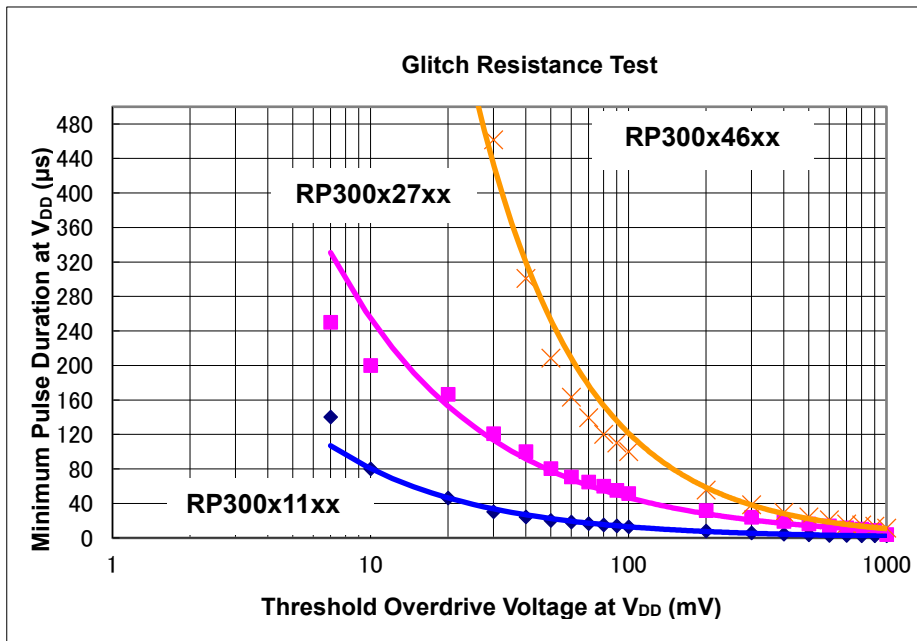
Timing Chart

- The output voltage is equalized to the GND voltage.
- The VDD voltage drops to the detector threshold (A point) which means $V_{ref} \geq V_{DD} \times R_b / (R_a + R_b)$. The comparator output shifts from "H" to "L" voltage and the output voltage shifts from the pull-up voltage to "L" voltage.
- If the VDD voltage is lower than the minimum operating voltage, the output voltage is equalized to the pull-up voltage.
- The output voltage is equalized to the pull-up voltage.
- The VDD voltage becomes higher than the release voltage (B point) which means $V_{ref} < V_{DD} \times R_b / (R_a + R_b)$. The comparator output shifts from "L" to "H" voltage, and the output voltage is equalized to the GND voltage.

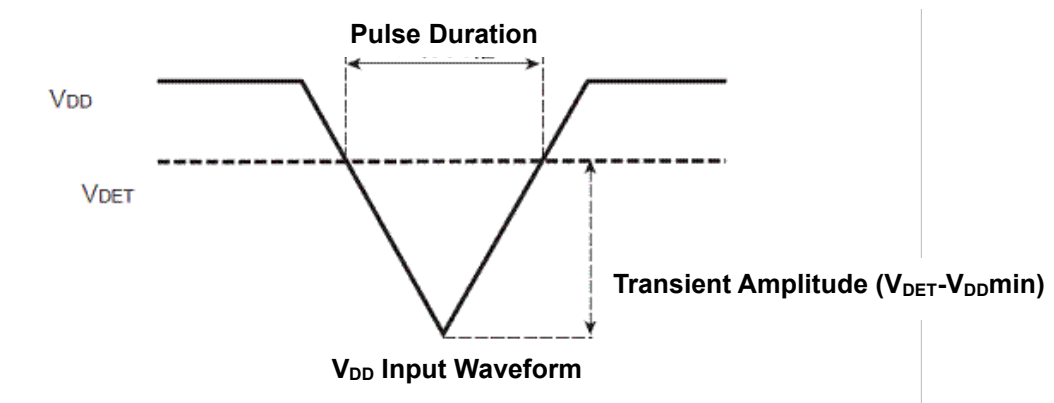
Note: There's no hysteresis between the VDD voltage and the released voltage.

Detector Operation vs. Glitch Input Voltage

The RP300x has built-in rejection of fast transients on the V_{DD} pins. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the RP300x.



Minimum Pulse Duration at V_{DD} vs. Overdrive Voltage at V_{DD}

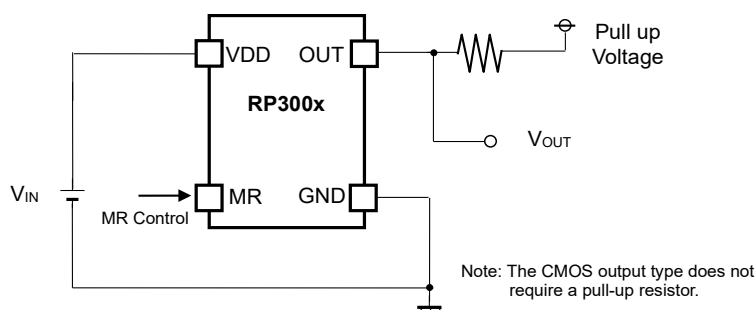


Voltage Transient Measurement

The RP300x does not respond to transients that are fast duration/ low amplitude or long duration/ small amplitude. The above graph shows the relationship between the transient amplitude and duration needed to trigger a reset. Any combination of duration and amplitude above the curve generates a reset signal.

APPLICATION INFORMATION

Typical Applications



RP300x Typical Application Circuit

TECHNICAL NOTES

When connecting resistors to the device's input pin

When connecting a resistor (R1) to an input of this device, the input voltage decreases by [Device's Consumption Current] x [Resistance Value] only. And, the cross conduction current⁽¹⁾, which occurs when changing from the detecting state to the release state, is decreased the input voltage by [Cross Conduction Current] x [Resistance Value] only. And then, this device will enter the re-detecting state if the input voltage reduction is larger than the difference between the detector voltage and the released voltage.

When the input resistance value is large and the VDD is gone up at mildly in the vicinity of the released voltage, repeating the above operation may result in the occurrence of output.

As shown in Figure A/B, set R1 to become 100kΩ or less as a guide, and connect C_{IN}⁽²⁾ of 0.1μF and more to between the input pin and GND. Besides, make evaluations including temperature properties under the actual usage condition, with using the evaluation board like this way. As result, make sure that the cross conduction current has no problem.

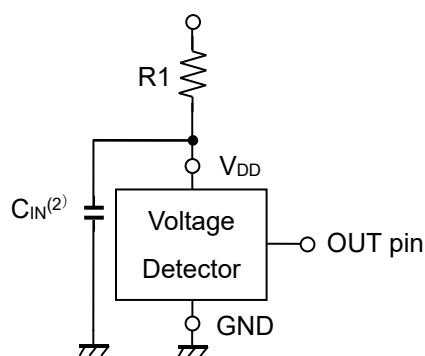


Figure A

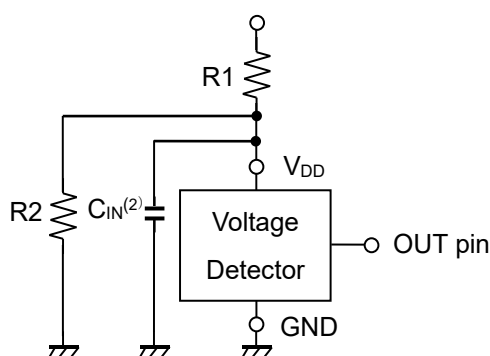


Figure B

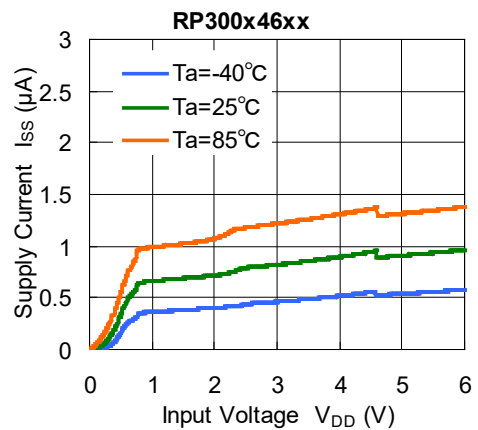
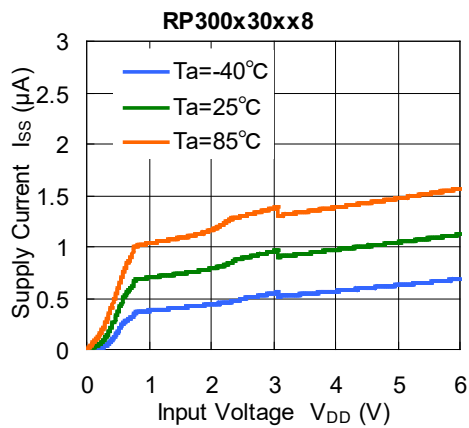
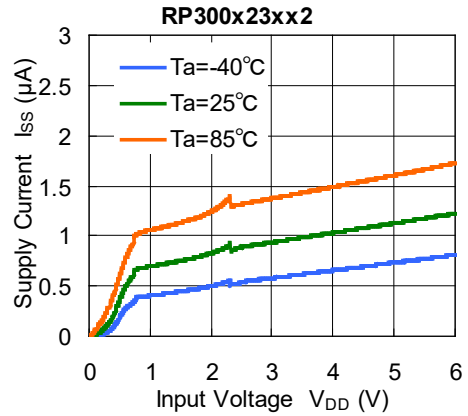
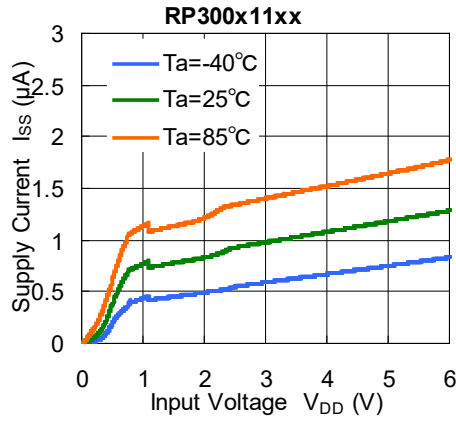
⁽¹⁾ In the CMOS output type, a charging current for OUT pin is included.

⁽²⁾ Note the bias dependence of capacitors.

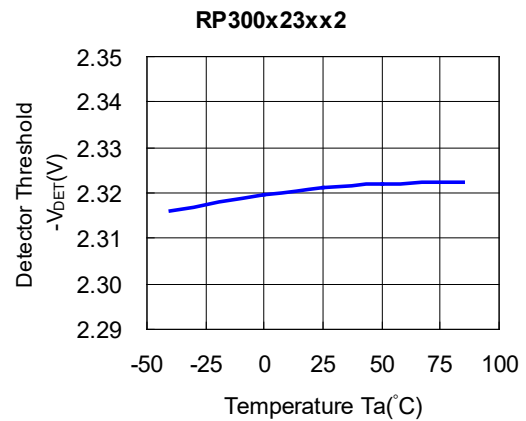
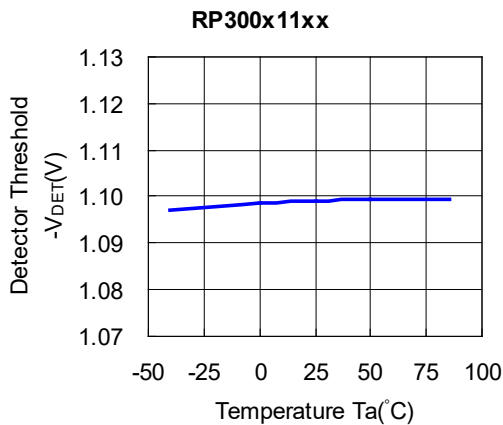
TYPICAL CHARACTERISTICS

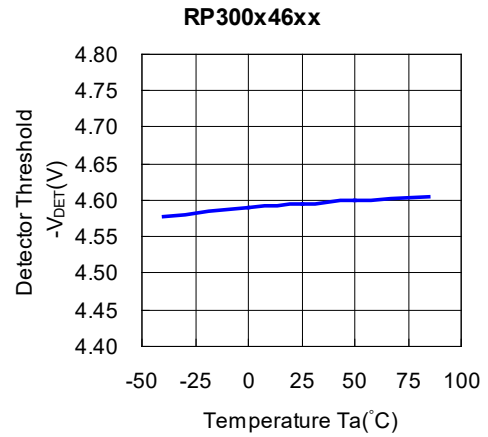
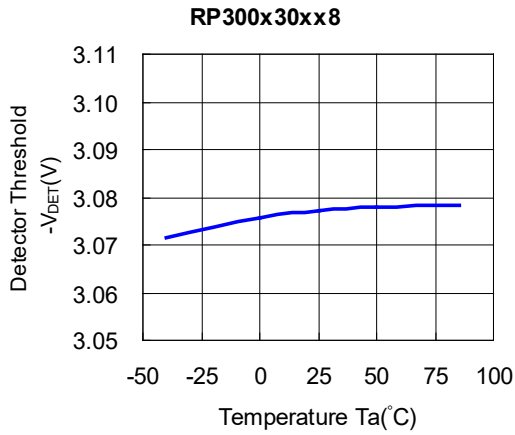
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Supply Current vs. Input Voltage

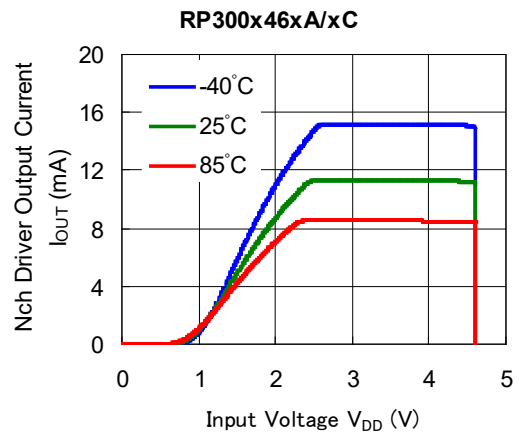
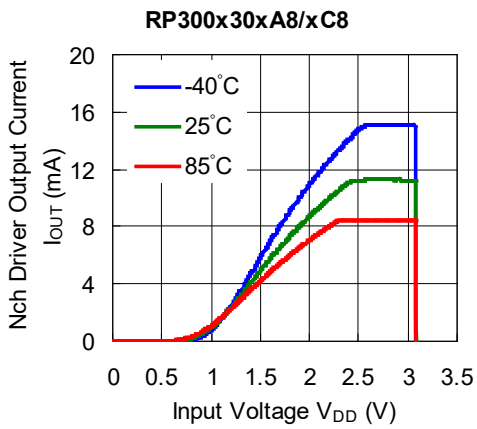
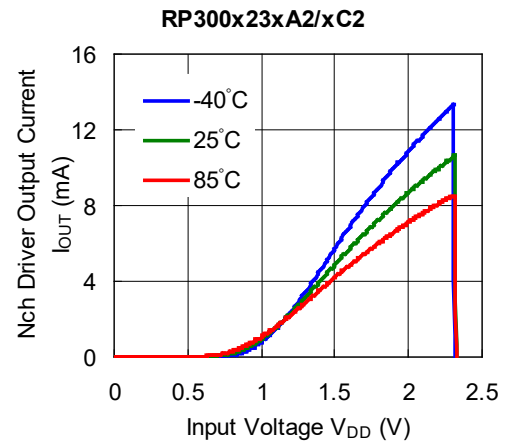
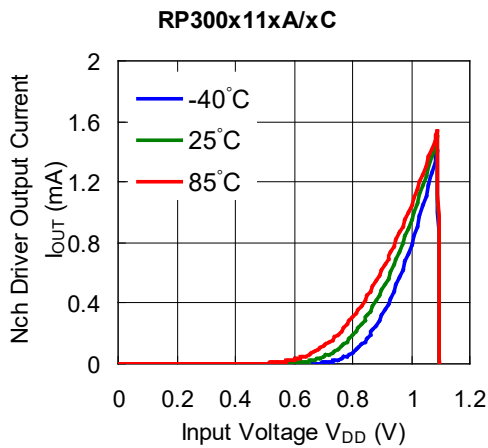


2) Detector Threshold vs. Temperature

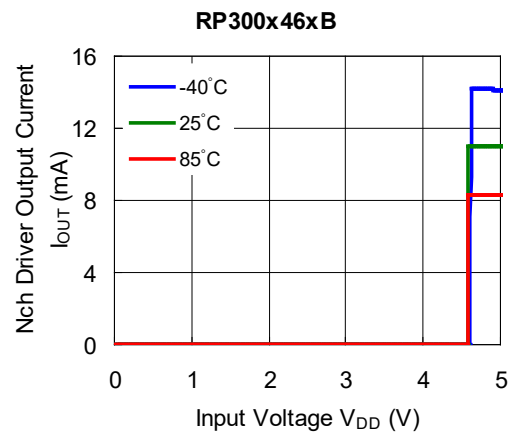
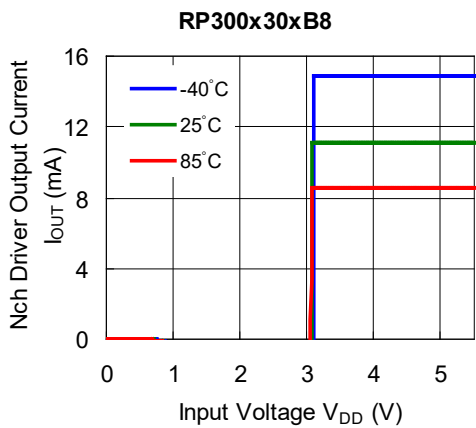
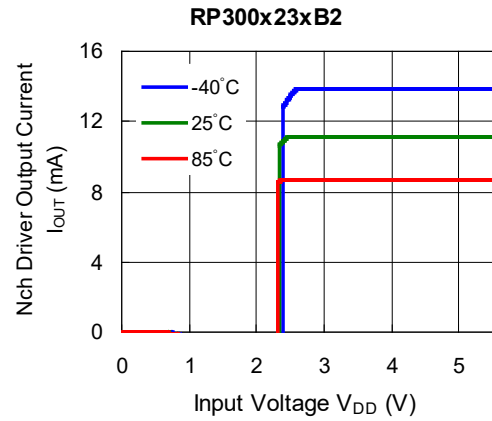
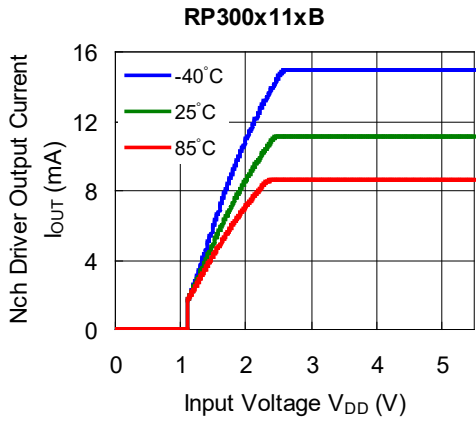




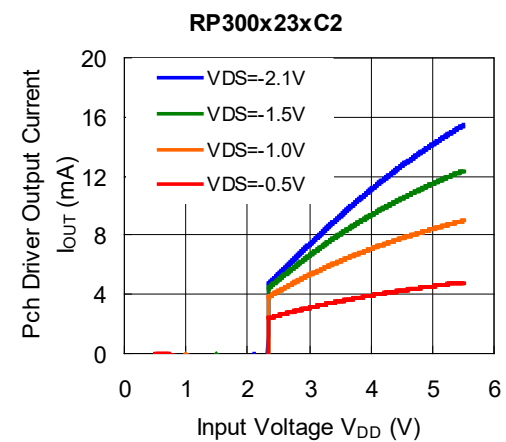
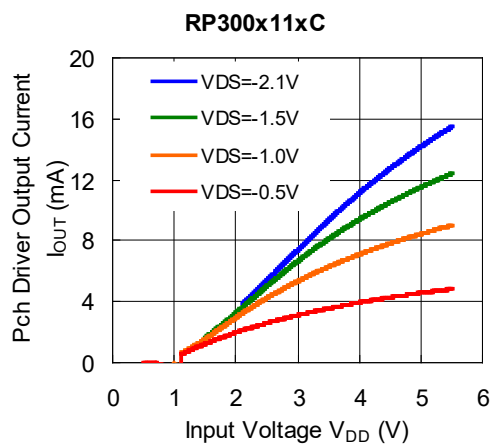
3) Nch Driver Output Current vs. Input Voltage

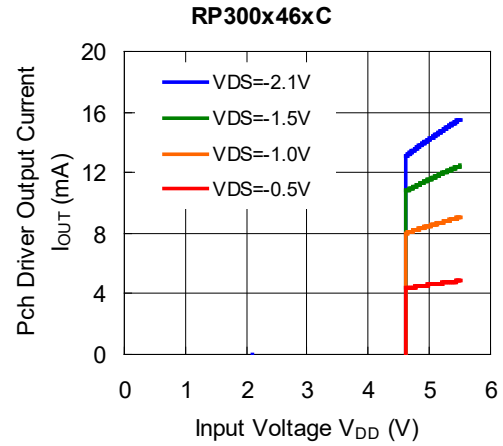
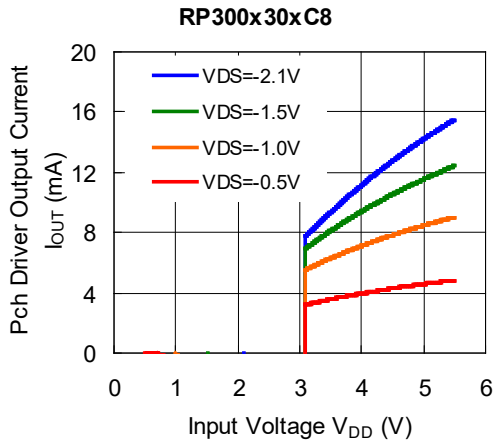


Nch Driver Inverting Output (custom IC)

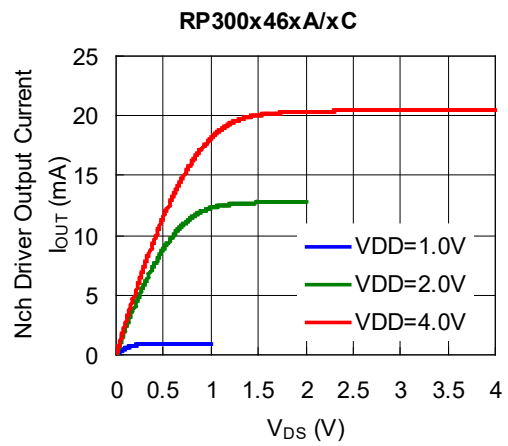
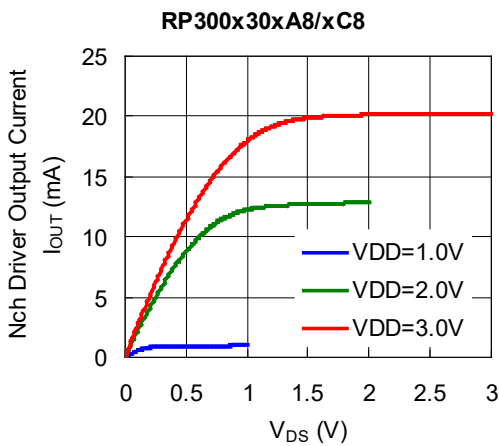
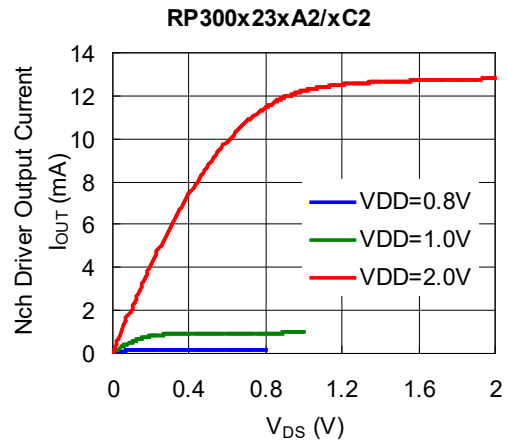
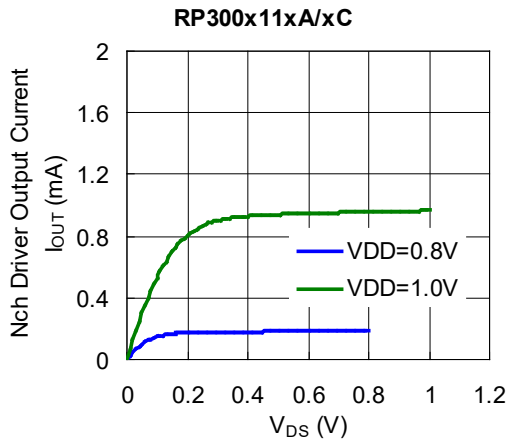


4) Pch Driver Output Current vs. Input Voltage

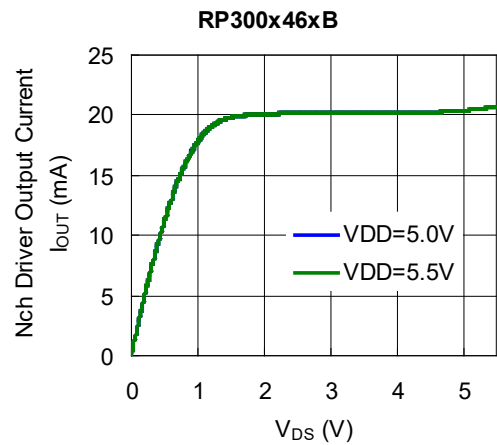
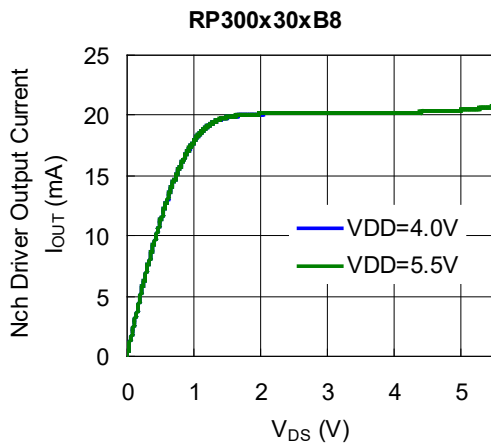
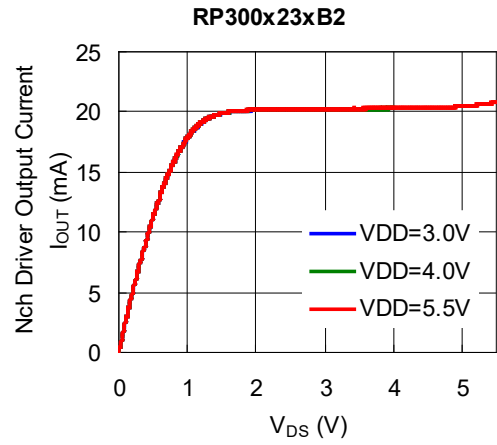
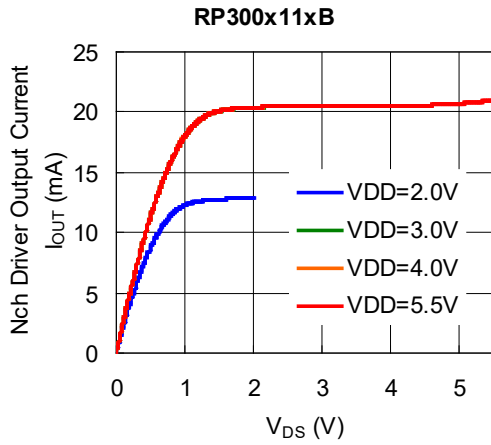




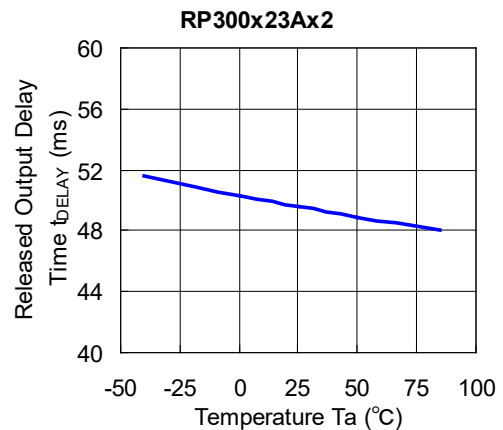
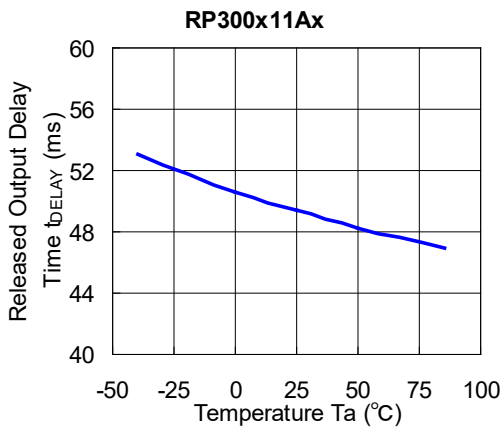
5) Nch Driver Output Current vs. V_{DS}

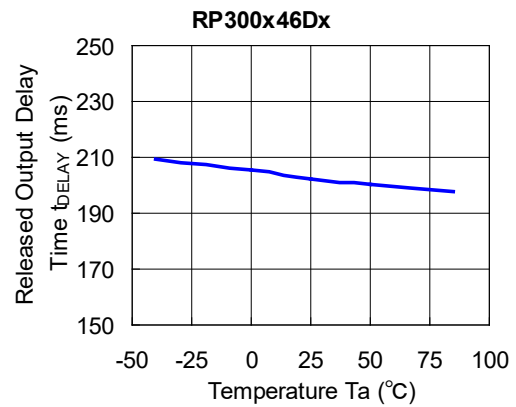
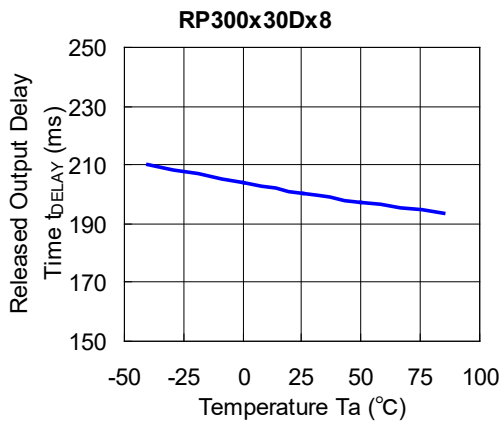
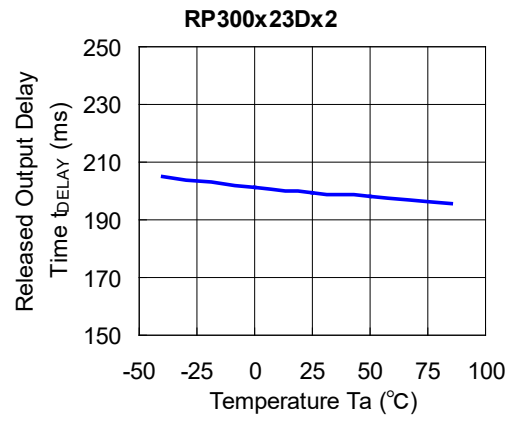
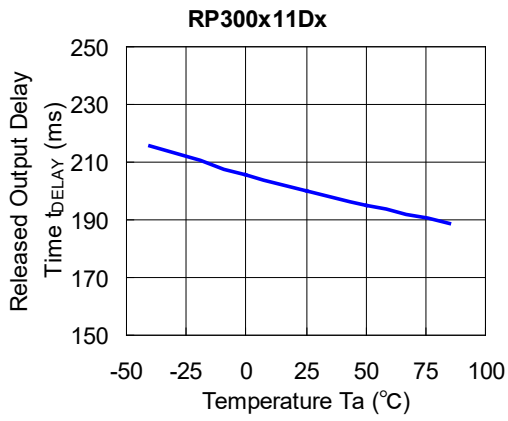
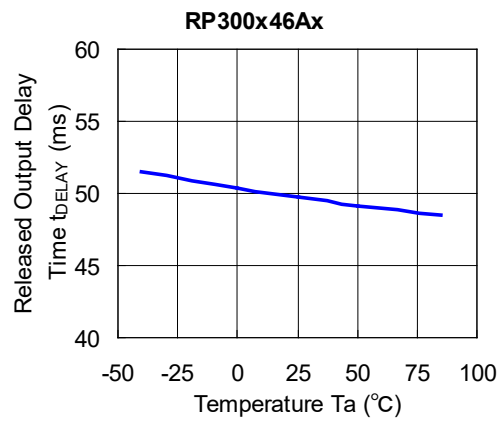
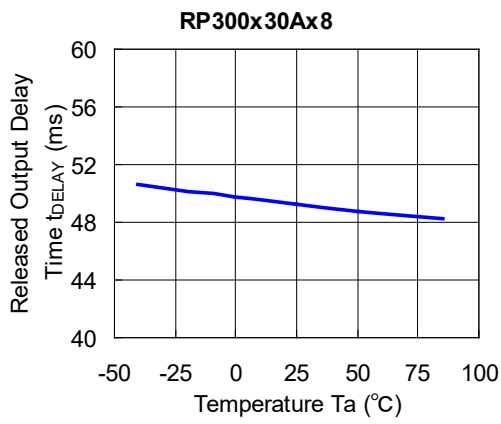


Nch Driver Inverting Output (custom IC)



6) Released Output Delay Time vs. Temperature





The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.2 mm × 11 pcs

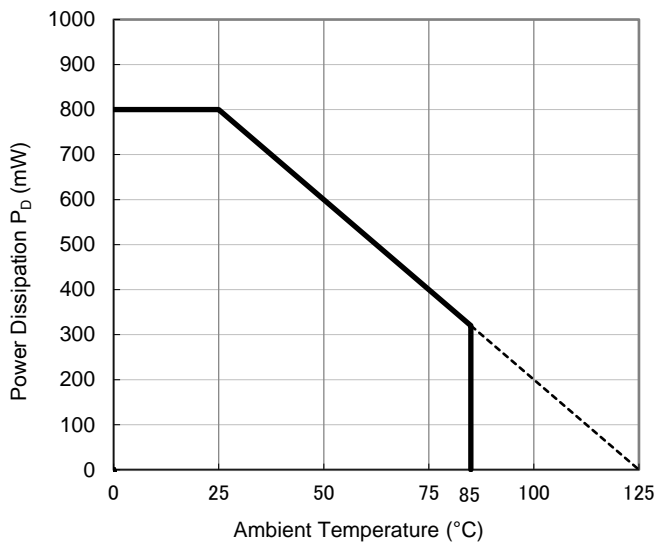
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

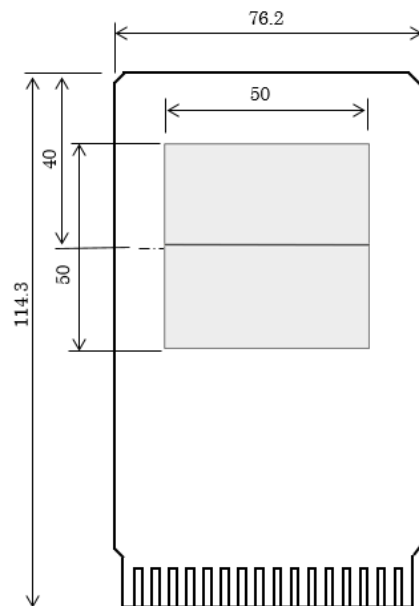
Item	Measurement Result
Power Dissipation	800 mW
Thermal Resistance (θja)	θja = 125°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 58°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



DFN (PLP) 1010-4B Package Dimensions (Unit: mm)

* The tab on the bottom of the package is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 7 pcs

Measurement Result

(Ta = 25°C, Tjmax = 125°C)

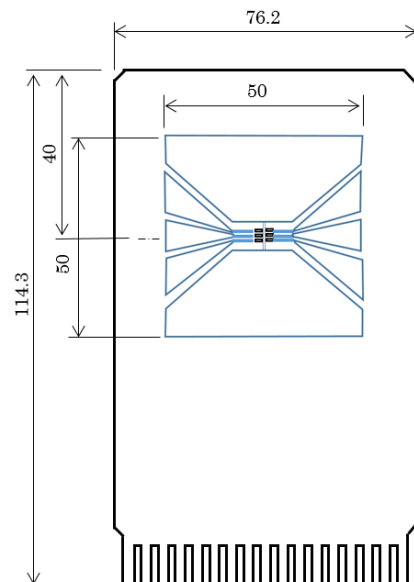
Item	Measurement Result
Power Dissipation	660 mW
Thermal Resistance (θja)	θja = 150°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 51°C/W

θja: Junction-to-Ambient Thermal Resistance

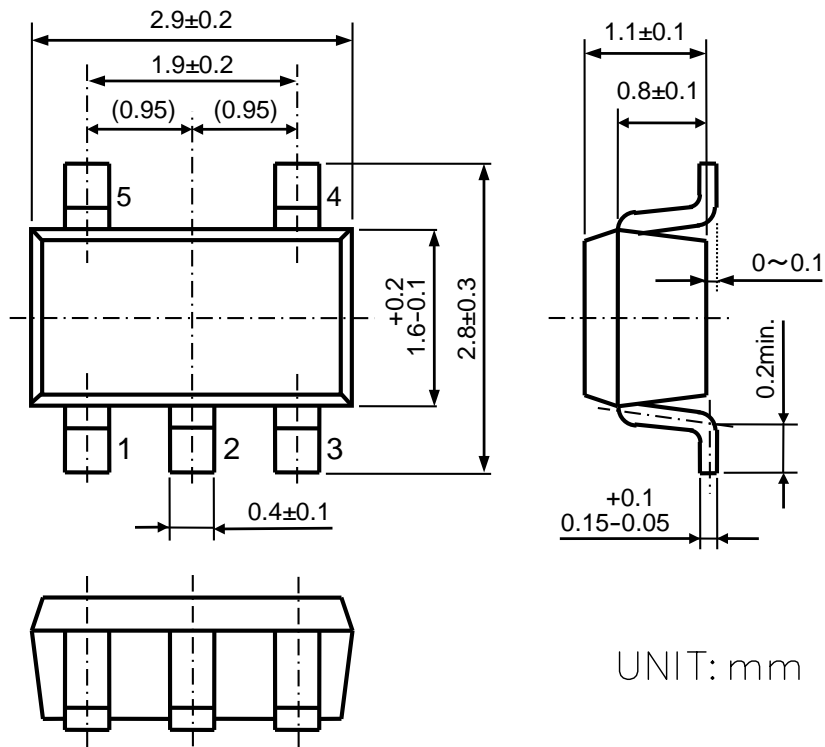
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



UNIT: mm

SOT-23-5 Package Dimensions



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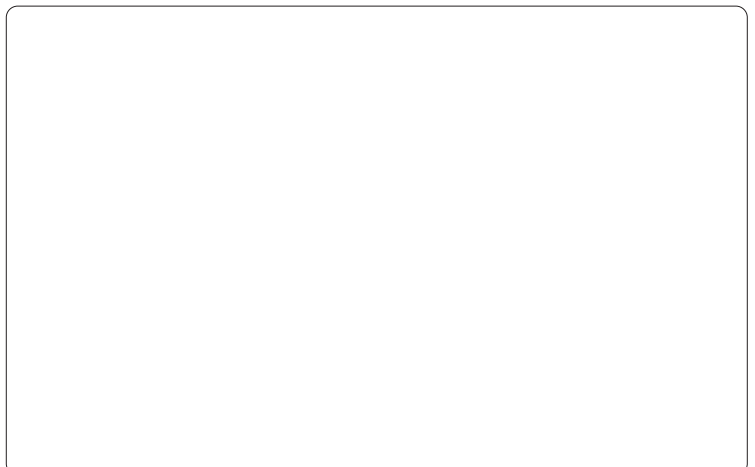
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