Synchronous Step-down DC/DC Converter with VD and VR

NO.EA-156-121225

OUTLINE

The RP901xxxx is a CMOS-based current mode PWM control synchronous step-down DC/DC converter with a voltage detector (VD) and an LDO regulator (VR).

Each of Step-down DC/DC converters is composed of an oscillator, a voltage reference unit, an error amplifier, a switching control circuit, a soft-start circuit, a protection circuit, a UVLO circuit, a switching transistor. Due to the switching elements are built in and synchronous control, a high efficiency step-down DC/DC converter can be made with an inductor and capacitors. To realize high efficiency at light load, automatic PWM/VFM alternative mode can be selected other than the PWM fixed control mode.

As protection circuits, a current limit circuit which limits Lx peak current cycle by cycle and a hiccup mode protection circuit which works if the load current over the limit continues for a certain time*1 are built in. The output voltage can be preset with 0.05V step in the factory due to the built-in feed back resistance, and the tolerance is ±2%. Since the package is DFN (PLP) 2527-10, high density mounting on board is possible.

Built-in LDO regulator (VR) is composed of a voltage reference unit, a voltage detecting resistor-network, an error amplifier, a short current limit circuit, and a driver transistor. After the soft-start time of the DC/DC converter is over and a specified delay time, LDO starts up. The sequence function is fixed internally*2.

Built-in voltage detector (VD) supervises the input voltage or the output of the VR (The reset function works for UVLO and over-current of the DC/DC converter). The option is preset in the factory. The output type is N-channel open drain. The released delay time is built-in, typ.50ms.

If the junction temperature of the IC is over the limit, the system is reset by the built-in thermal shut-down circuit.

*1) A version: As soon as the load current is over the limit, the system restarts by the protection.

*2) C, D versions: No sequence function

FEATURES

- Input Voltage Range ········· 4.5V to 5.5V
- Supply Current ········· Typ. 460µA (at PWM mode)
  Typ. 170µA (at light load applied to B, C, D versions)

Step-down DC/DC Converter

- Output Voltage Range ········· 1.2V to 1.8V, preset is possible by user’s request
- Output Voltage Tolerance ········· ±2%
- Oscillator Frequency ········· Typ. 1.2MHz
- Built-in driver ON resistance ········· Typ. P-channel 0.25Ω, N-channel 0.25Ω (at V_{IN}=5V)
- Soft-start function ········· Typ. 1ms
- Lx peak current limit function ········· Typ. 1.4A (D version: 1.5A)
- Output Current ········· Min. 800mA (D version: 900mA)
- Protection Delay Time ········· Typ. 0.1ms (applied to B, C, D versions)
- UVLO function ········· Typ. 3.5V
- Chip enable function ········· ”H” active

LDO Regulator

- Output Voltage Range ············ 2.5V to 3.3V, preset is possible by user's request
- Output Voltage Tolerance ············ ±1.0%
- Output Current ············ Min. 600mA
- Start-up delay time ············ Typ. 2ms (applied to A, B versions)
- Auto-Discharge function at turning off ············ Discharge resistance Typ.50Ω (at V_{IN}=5V)

VD

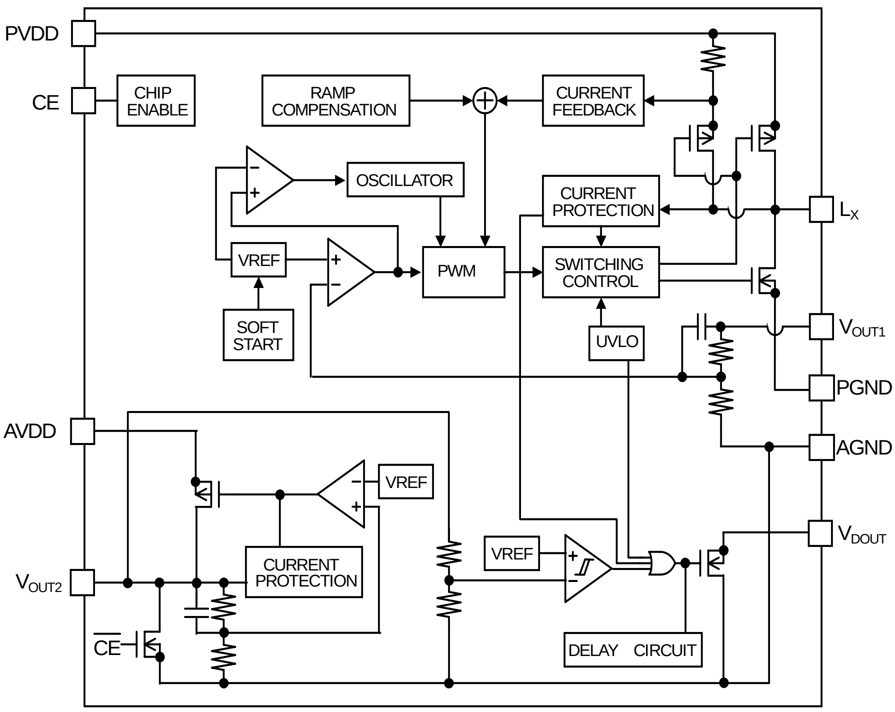
- Voltage Detector Threshold Range ············ 2.0V to 3.0V, preset is possible by user's request (A version: VR output voltage is supervised), 3.0V to 5.0V, preset is possible by user's request (B, C, D versions: Input voltage is supervised)
- Released Delay Time ············ Typ.50ms
- Thermal shutdown circuit ············ Detecting Temperature: Typ. 165°C, Released temperature: Typ. 110°C
- Package ············ DFN(PLP)2527-10
- External Components ············ C_{IN}=10.0µF, C_{OUT1}=10.0µF, L=4.7µH (DC/DC), C_{OUT2}=2.2µF(VR)

APPLICATION

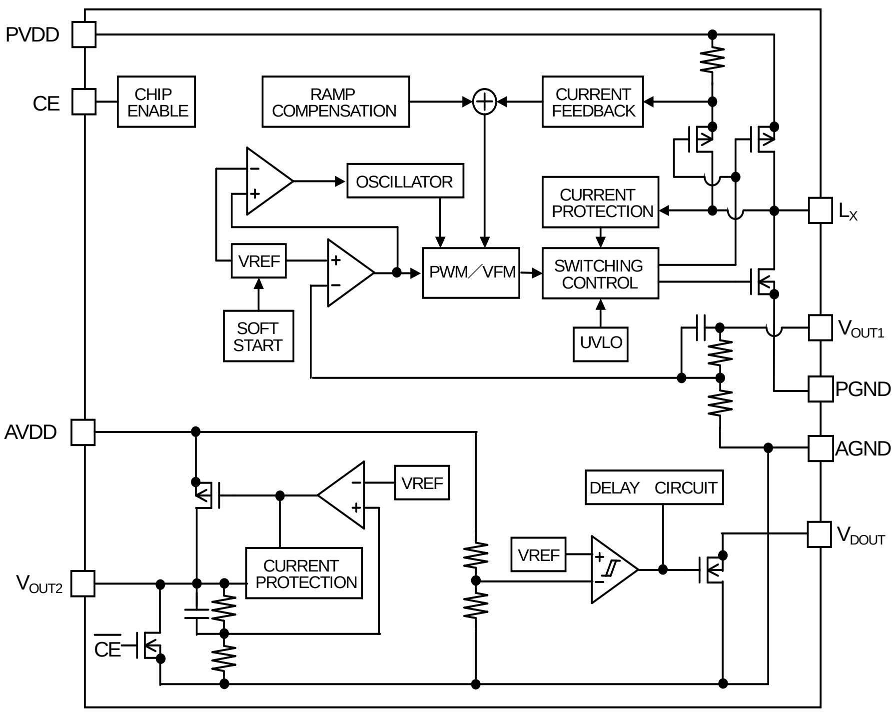
- Optical Disk Equipment

BLOCK DIAGRAMS

A version



B/C/D version



SELECTION GUIDE

In the RP901 series, the output voltage combination and function can be designated.

The selection can be made by the alphanumeric serial number as the next example.

Product Code	Package	Units/ 1 reel	Pb free	Halogen free
RP901Kxxx∗-TR	DFN(PLP)2527-10	5,000pcs	Yes	Yes

xxx: Serial number to describe the voltage combination of DC/DC converter, voltage regulator, and voltage detector.

∗: Function version

A version: DC/DC control type is PWM-fixed, without protection delay time, output current Min. 800mA, VR has start-up delay time to make a sequence. VD supervises the output of VR (Reset is output at UVLO and over current of DC/DC)

B version: DC/DC control type is PWM/VFM automatic mode shift, with protection delay time, output current Min. 800mA, VR has start-up delay time to make a sequence. VD supervises the input voltage.

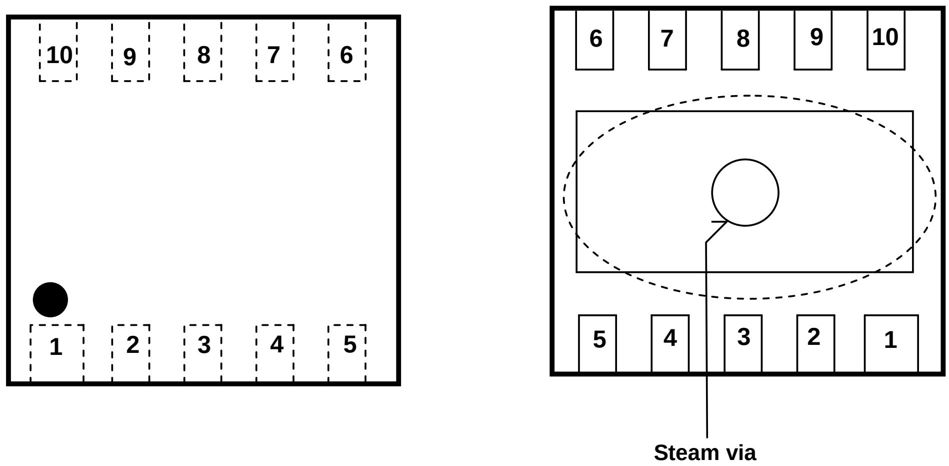
C version: DC/DC control type is PWM/VFM automatic mode shift, with protection delay time, output current Min. 800mA, VR: without delay time to make a sequence, VD supervises the input voltage.

D version: DC/DC control type is PWM/VFM automatic mode shift, with protection delay time, output current Min. 900mA, VR: without delay time to make a sequence, VD supervises the input voltage.

PIN CONFIGURATION

DFN(PLP)2527-10

Mark Side **Bottom Side**



PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	CE	Chip Enable Pin (”H” active)
2	V_{DOUT}	VD Output Pin (N-channel open drain output)
3	AGND	Analog Ground Pin
4	PGND	Power Ground Pin
5	L_X	DC/DC Switching Pin
6	PVDD	Power Supply Input Pin
7	NC	No connection
8	V_{OUT1}	DC/DC Output Pin
9	AVDD	Analog Power Supply Input Pin
10	V_{OUT2}	VR Output Pin

The backside of the package tab is connected to the substrate of the IC (GND). Connect to GND pin (Recommendation), or solder the tab and left open electrically.
Make short 3pin and 4pin, and make short 6pin and 9pin.

ABSOLUTE MAXIMUM RATINGS

(GND=0V)

Symbol	Item	Rating		Unit
V_{IN}	PVDD Pin Voltage AVDD Pin Voltage	6.5		V
V_{CE}	CE Pin Voltage	-0.3 to 6.5		V
V_{LX}	L_X Pin Voltage	-0.3 to V_{IN} + 0.3		V
V_{OUT1}	V_{OUT}1 Pin Voltage	-0.3 to V_{IN} + 0.3		V
V_{OUT2}	V_{OUT}2 Pin Voltage	-0.3 to V_{IN} + 0.3		V
V_{DOUT}	V_{DOUT} Pin Voltage	-0.3 to 6.5		V
P_D	Power Dissipation*	(1)	1750 (Ta=25°C, Tjmax=150°C)	mW
		(2)	1138 (Ta=25°C, Tjmax=150°C)	
Ta	Operating Temperature	-40 to +85		°C
Tstg	Storage Temperature	-55 to +125		°C

* For more information about Power Dissipation and Standard Land Pattern, refer to *PACKAGE INFORMATION*.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the measurement is done by an open loop circuit. Unless otherwise specified, $V_{IN}=V_{CE}=5V$, AGND=PGND=0V.

RP901xxx

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Input Voltage		4.5		5.5	V
I_{SS1}	Supply Current 1	$V_{IN}=V_{CE}=5.5V$ $V_{OUT}1=V_{SET}$ x 0.8		460		µA
I_{SS2}	Supply Current 2 (applied to B/C/D version)	$V_{IN}=V_{CE}=5.5V$ $V_{OUT}1=V_{SET}$ x 1.2		170		µA
Istandby	Standby Current	$V_{IN}=5.5V$, $V_{CE}=0V$: A version		1.0	5.0	µA
		$V_{IN}=5.5V$, $V_{CE}=0V$: B/C/D version		2.0		
V_{CEH}	CE Input Voltage "H"		1.0			V
V_{CEL}	CE Input Voltage "L"				0.3	V
T_{TSD}	Thermal Shutdown Detector Temperature	Junction Temperature		165		°C
T_{TSR}	Thermal Shutdown Release Temperature	Junction Temperature		110		°C

DC/DC SECTION (Ta=25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OUT1}	Output Voltage 1	$V_{IN}=5V$	-2.0%		+2.0%	V
$\Delta V_{OUT1}/\Delta Ta$	Output Voltage 1 Temperature Coefficient	-40°C ≤ Ta ≤ 85°C		±150		ppm/°C
fosc	Oscillator Frequency	$V_{IN}=5V$	-20%	1.2	+20%	MHz
$I_{LXLEAKH}$	L_X leakage Current "H"	$V_{IN}=V_{LX}=5.5V$, $V_{CE}=0V$	-1.0	0.0	5.0	µA
$I_{LXLEAKL}$	L_X leakage Current "L"	$V_{IN}=5.5V$, $V_{CE}=V_{LX}=0V$	-5.0	0.0	1.0	µA
R_{ONP}	P-channel transistor ON resistance	$V_{IN}=5V$, $I_{LX}=-100mA$		0.25		Ω
R_{ONN}	N-channel transistor ON resistance	$V_{IN}=5V$, $I_{LX}=-100mA$		0.25		Ω
Maxduty	Maximum Duty Cycle		100			%
tstart	Soft-start Time	$V_{IN}=V_{CE}=5V$		1.0		ms
I_{LXLIM}	L_X Current Limit	$V_{IN}=V_{CE}=5V$: A/B/C version	1.0	1.4		A
		$V_{IN}=V_{CE}=5V$: D version	1.1	1.5		
tprot	Protection Delay Time	$V_{IN}=V_{CE}=5V$: A version		0.0		ms
		$V_{IN}=V_{CE}=5V$: B/C/D version		0.1		
V_{UVLO1}	UVLO Detector Threshold	$V_{IN}=V_{CE}$	3.40	3.50	3.60	V
V_{UVLO2}	UVLO Release Voltage	$V_{IN}=V_{CE}$	3.63	3.73	3.83	V

All test items listed under *ELECTRICAL CHARACTERISTICS* are done under the pulse load condition (Tj≈Ta=25ºC) except Thermal Shutdown.

VR SECTION (Ta=25°C)

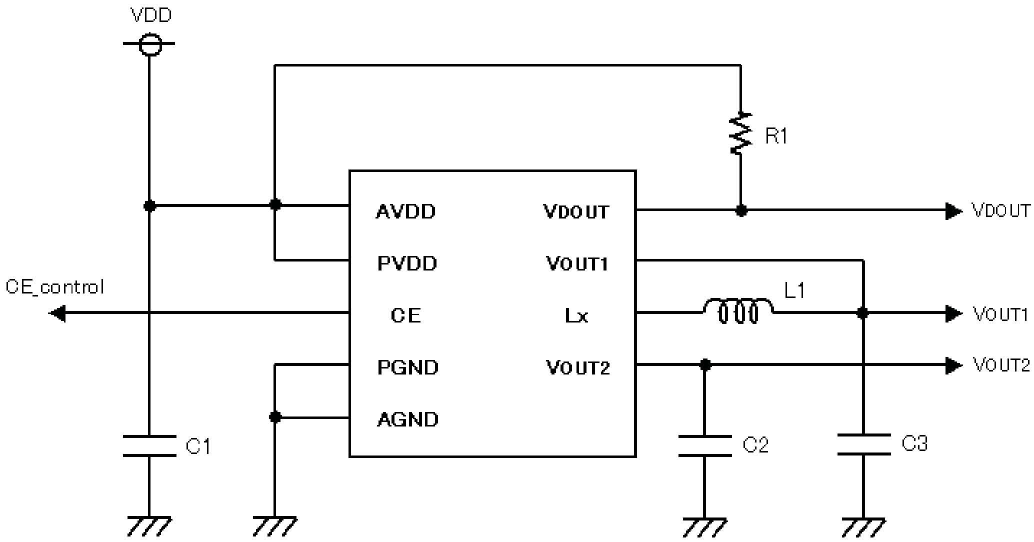
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OUT2}	Output Voltage 2	V_{IN}=5V, I_{OUT}=1mA	-1.0%		+1.0%	V
I_{LIM2}	Current Limit 2		600			mA
I_{SS3}	Supply Current 3	V_{IN}=V_{CE}=5.5V		60		μA
$\Delta V_{OUT2}/\Delta I_{OUT2}$	Load Regulation	1mA ≤ I_{OUT2} ≤ 400mA		40	80	mV
$\Delta V_{OUT2}/\Delta Ta$	Output Voltage 2 Temperature Coefficient	-40°C ≤ Ta ≤ 85°C		±50		Ppm /°C
I_{SC}	Short Current Limit	V_{OUT2}=0V		70		mA
T_{VR} (A/B version)	Start-up Timing Delay	Start from the finish moment of soft start-time of DC/DC converter		2.0		ms
T_{VR} (C/D Version)	Start-up Delay	Start from UVLO release moment of DC/DC converter		50		μs
R_{LOW}	For auto discharge at off, N-channel Tr. ON resistance	V_{IN}=5V, V_{CE}=0V		50		Ω

VD SECTION (Ta=25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$-V_{DET}$	VD Detector Threshold		-2.0%		+2.0%	V
$\Delta -V_{DET}/\Delta Ta$	VD Detector Threshold Temperature Coefficient	-40°C ≤ Ta ≤ 85°C		±40		ppm /°C
V_{HYS}	Hysteresis Range			$-V_{DET}$ x 0.05		V
T_{PLH}	VD Release Delay Time			50		ms
I_{DOUTL}	V_{DOUT} "L" Output Current	V_{IN}=2.0V , V_{DOUT}=0.1V	1.0	4.0		mA

All test items listed under *ELECTRICAL CHARACTERISTICS* are done under the pulse load condition (Tj≈Ta=25ºC) except Thermal Shutdown.

TYPICAL APPLICATION AND TECHNICAL NOTES



External Components Recommendation

Inductor L1: 4.7μH (A/B/C Version VLF4014AT-4R7M1R1 TDK)

4.7μH (D Version VLF4014ST-4R7M1R4 TDK)

Pull-up Resistance R1: 50kΩ

Capacitors C1: 10μF Ceramic capacitor (C2012JB0J106K TDK)

C2: 2.2μF Ceramic capacitor

C3: 10μF Ceramic capacitor (C2012JB0J106K TDK)

TECHNICAL NOTES ON EXTERNAL COMPONENTS

- Place all the external components as close as possible to the IC and make the wiring length as short as possible. Especially, the capacitor between V_{IN} and GND must be as close as possible to the IC. If the impedance of the power supply and ground is high, the power level of the IC may shift by the switching current and the operation may unstable. Make the power line and the ground line sufficient. Through the power line, the ground line, inductor, L_X pin, V_{OUT} line, large current may flow by switching, therefore fully consideration is necessary. The wiring between V_{OUT} pin and the inductor, and load and V_{OUT} pin must be separated.

- PVDD and AVDD must be short and make them close as possible. Place a capacitor as close as possible to PVDD. If the distance between AVDD and PVDD is long, add another 0.1μF capacitor between AVDD and GND.

- Capacitance value between VDD and GND should be 10μF or more and use a low ESR ceramic capacitor. Use a ceramic capacitor for V_{OUT1} pin, and the capacitor should be 10μF or more. Use a ceramic capacitor for V_{OUT2} pin, and the ceramic capacitor should be 2.2μF or more.

- Choose an inductor with low DCR, and enough permissible current and which is hard to reach magnetic saturation. If the inductance value is too small, at the maximum load, the current flows through Lx transistor and inductor may be beyond the absolute maximum rating. Choose an appropriate inductance value.

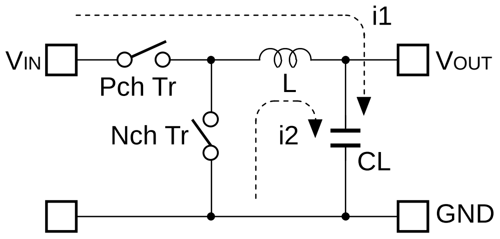
- If the spike noise of Lx pin is large, place a snubber circuit between Lx and GND (CR serial connection, etc.) to reduce the spike noise. Time constants of CR depend on the actual PCB and decide with the evaluation of the PCB.

⋆ The performance of the power circuit with the IC depends on the peripheral circuits. In terms of the external components, PCB pattern, and IC, the peripheral circuit should be designed not to exceed beyond ratings (voltage, current, power).

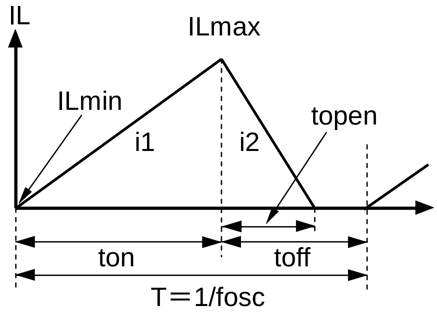
STEP-DOWN DC/DC CONVERTERS' OPERATION AND OUTPUT CURRENT

This explanation is about the general step-down DC/DC converters' operation.
In the step-down DC/DC converter, when the Lx transistor turns on, at the same time, energy is accumulated into an inductor and when the transistor turns off, the current accumulated in the inductor is released and averaged, then make the energy loss reduced and the output voltage lower than the input voltage is supplied.

〈Basic Circuit〉



〈Current flows L〉



Step1. P-channel transistor turns on, current IL=i1, energy is charged into L, CL is charged and the output current I_{OUT} is supplied. While the P-channel transistor turns on (t_{ON}), and in proportion to IL=i1 is from IL=ILmin=0 increases and reaches to ILmax.

Step2. P-channel transistor turns off, L keeps IL=ILmax, and turns on the N-channel transistor, current IL=i2 flows.

Step3. IL=i2 decreases gradually, after $t_{OPEN,}$ IL=ILmin=0 and N-channel transistor turns off.
However, if the cycle is continuous mode, before IL=ILmin=0, t_{OFF} time becomes nothing, the next cycle starts and the P-channel transistor turns on, and the N-channel transistor turns off. In this case, ILmin >0 and charge is remained, and charge is increased from IL=ILmin >0.

In the PWM control, the number of switching in a second (f_{OSC}) is fixed, and t_{ON} is controlled and the output voltage is constantly maintained.

The step-down operation is constant and stable, the current flows through the inductor's maximum value (ILmax) and the minimum value (ILmin) is same as when the P-channel transistor turns on and off as described above.
Supposed that the difference between ILmax and ILmin is ΔI,

$$\Delta I = ILmax – ILmin = V_{OUT} \times t_{OPEN} / L = (VIN – VOUT) \times t_{ON} / L \cdots\cdots\cdots\cdots \text{Formula 1}$$

Thus,

$$T = 1 / f_{OSC} = t_{ON} + t_{OFF}$$
$$\text{duty} (\%) = t_{ON} / T \times 100 = t_{ON} \times f_{OSC} \times 100$$
$$t_{OPEN} \quad t_{OFF}$$

The left side of the equation describes the current level at turning on, and the right side of the equation describes the current level at turning off.

OUTPUT CURRENT AND SELECTION OF EXTERNAL COMPONENS

In the general step-down DC/DC converters, the relation between the output current and external components is described as below:

(Supposed that the peak to peak value of the ripple current is " I_{RP} ", On resistance of the L_X transistor, P-channel transistor, N-channel transistor is respectively described as "R_{ONP}" and "R_{ONN} ", inductor's DCR is described as " R_L")

Supposed that the time when L_X P-channel transistor turns on is described as " t_{ON}",

$V_{IN} = V_{OUT} + (R_{ONP} + R_L) \times I_{OUT} + L \times I_{RP} / t_{ON}$ ············ Formula 1

Supposed that the time when L_X P-channel transistor turns off (N-channel transistor turns on) is described as " t_{OFF}",

$L \times I_{RP} / t_{OFF} = (R_{ONN} + R_L) \times I_{OUT} + V_{OUT}$ ············ Formula 2

Using Formula 1 and Formula 2, and On duty of the P-channel transistor, $t_{ON} /(t_{ON} + t_{OFF})= D_{ON}$ is solved,

$D_{ON} =(V_{OUT} + R_{ONN} \times I_{OUT} + R_L \times I_{OUT}) / (V_{IN} – R_{ONP} \times I_{OUT} + R_{ONN} \times I_{OUT})$ ············ Formula 3

Ripple current is

$I_{RP} = (V_{IN} – V_{OUT} – R_{ONP} \times I_{OUT} – R_L \times I_{OUT}) \times D_{ON} / f_{OSC} / L$ ············ Formula 4

Then the peak current through the inductor and L_X transistor,

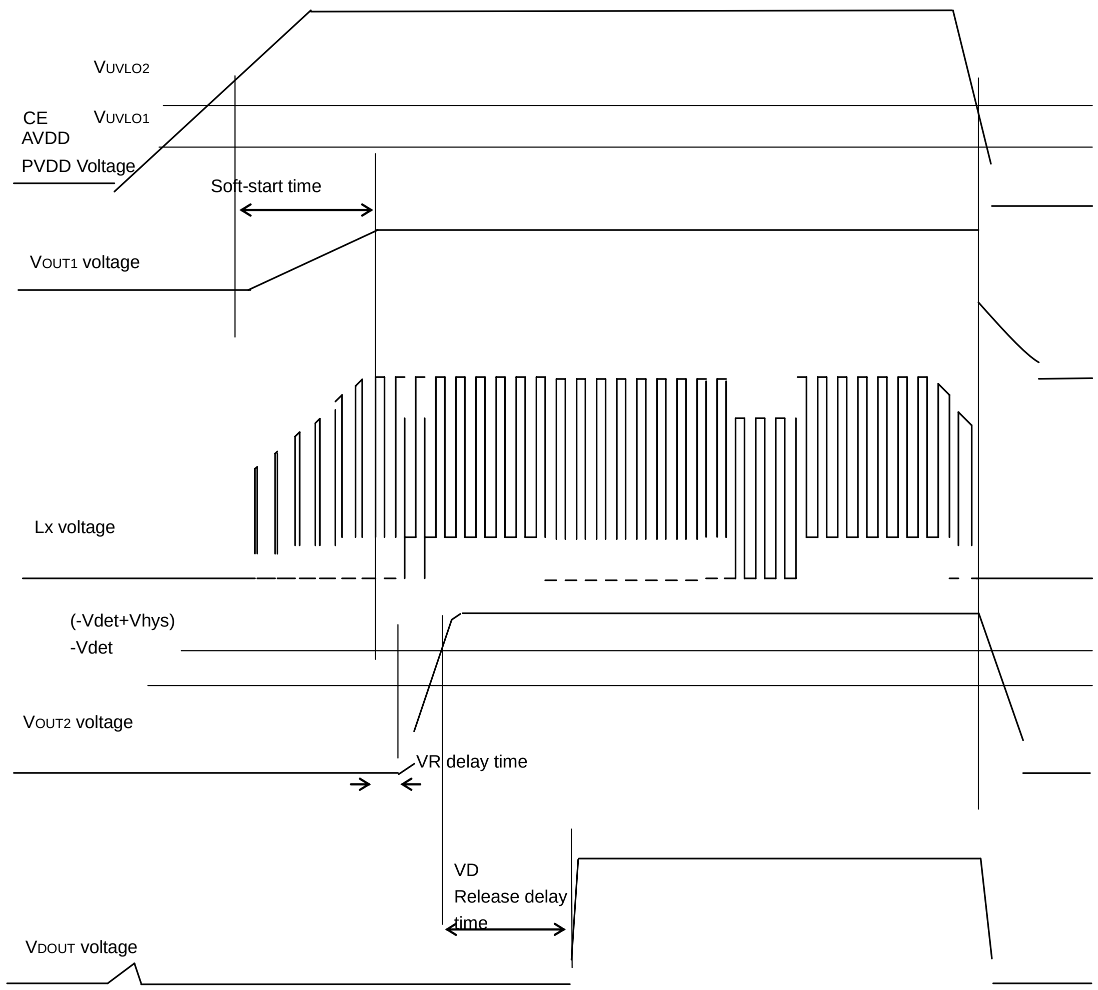
$ILmax = I_{OUT} + I_{RP} / 2$ ············ Formula 5

Decide the peripheral circuits with considering ILmax and input and output conditions.

★ The calculation is based on the ideal operation of the PWM continuous mode.

TIMING CHART (A Version)

(1) Start-up and shutdown by detecting UVLO



Timing chart of the power supply voltage change and DC/DC converter, VD, and VR can be explained as below:

(1) DC/DC converter

Power supply is forced and when VDD voltage increases, if VDD voltage is equal or less than the UVLO release voltage (VUVLO2), the operation of DC/DC converter stops and switching is halted, therefore the voltage, VOUT1 does not rise. When the VDD voltage becomes equal or more than UVLO release voltage, the DC/DC converter starts soft-start and switching begins and the voltage, VOUT1 rises. After the soft-start time, VDD voltage becomes set equal or more than VOUT1 voltage, VOUT1 voltage becomes set output voltage. When VDD voltage becomes eual or less than UVLO detector threshold (VUVLO1), DC/DC converter stops switching and turns off the Lx transistor inside the IC.

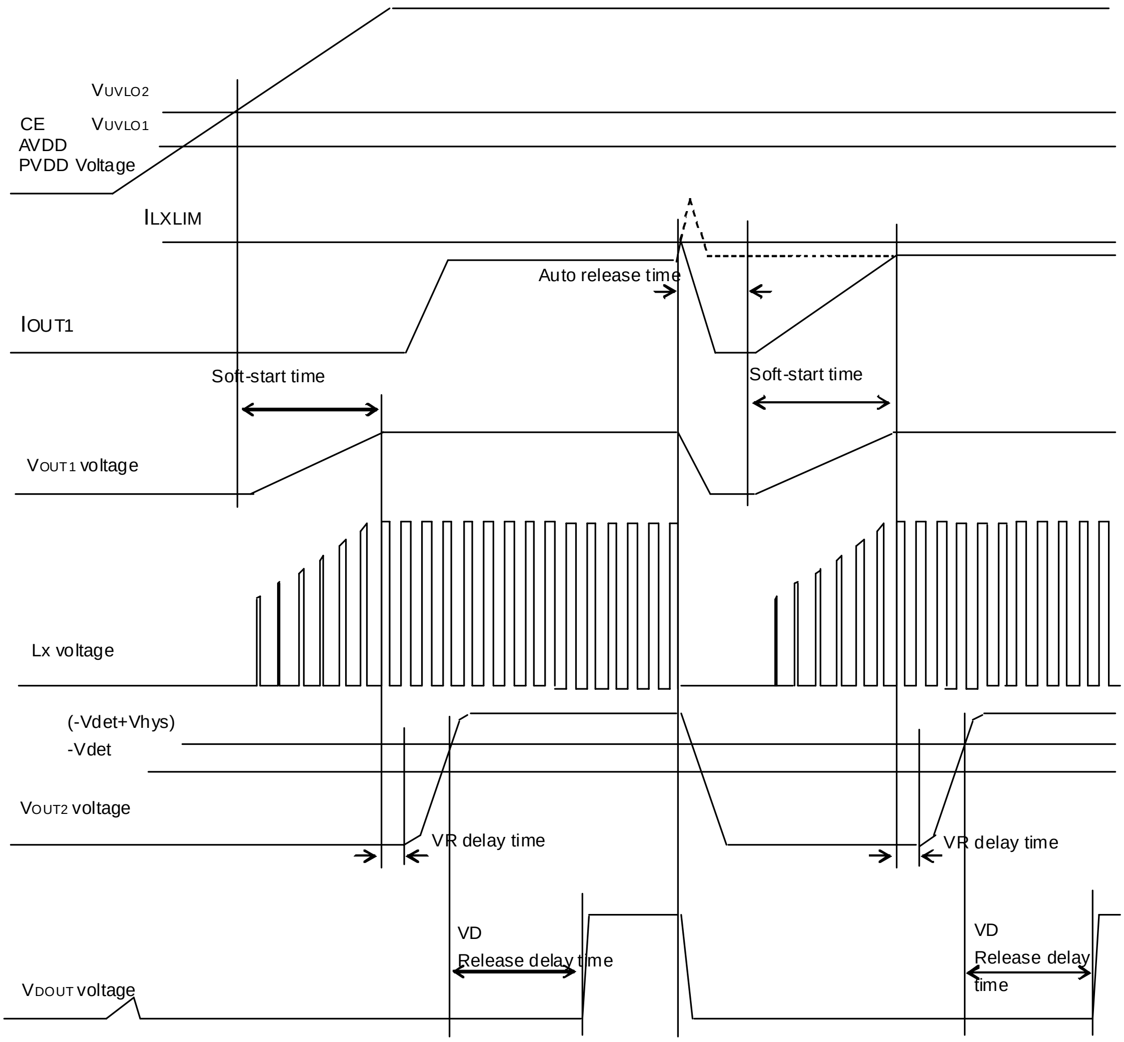
(2) VR

After the soft-start time of the DC/DC converter, VR starts up with delay time. The operation stops when VDD voltage becomes equal or less than UVLO detector threshold (VUVLO1), then auto-discharge function starts.

(3) VD

When VOUT2 voltage becomes equal or more than VD detector threshold voltage + hysteresis width (-VDET + VHYS), after the VD release delay time (TPLH), N-channel transistor of the IC turns off, VDOUT pin is pulled up with an external resistance and becomes pull-up voltage. When VDD voltage becomes equal or less than UVLO detector threshold (VUVLO1), then N-channel transistor of VDOUT pin turns on and VDOUT pin outputs ”L”. (Depending on VOUT1 or VOUT2, VDOUT pin outputs “L”. Refer to the timing chart.)

(2) Start-up and Turning off by detecting over current of DC/DC converter



Timing chart of DC/DC converter output change by load, VD and VR can be explained as below:

(1) DC/DC converter

When LX peak current (IOUT1) is beyond the current limit (ILXLIM),[*1] the protection circuit operates and switching stops and Lx transistor inside the IC turns off and restarts after a certain time.

*1) During soft-start time, if IOUT1 is beyond ILXLIM, the protection circuit does not work.

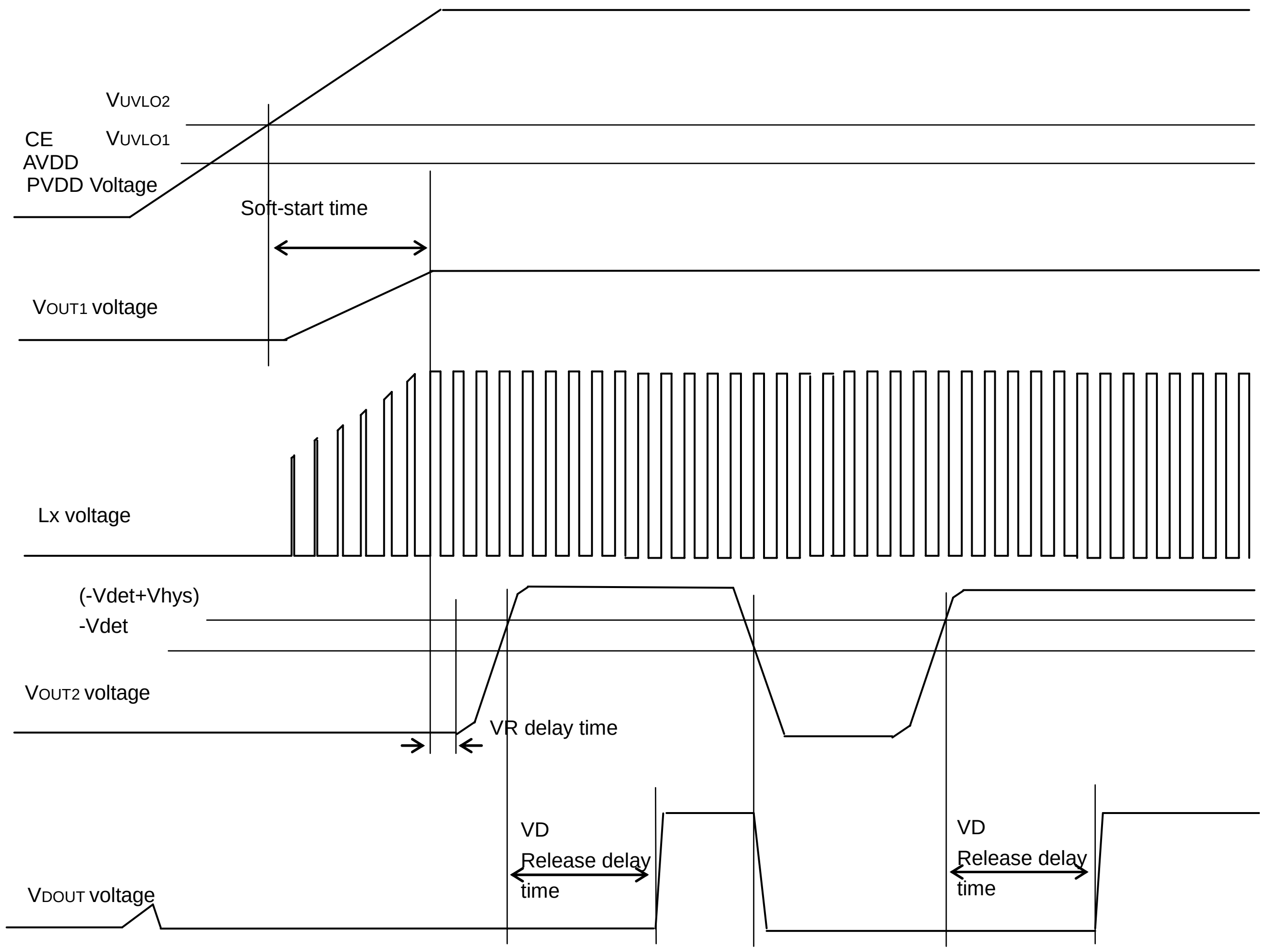
(2) VR

When the DC/DC converter stops and at the same time, VR operation stops and auto-discharge function operates. To release it, after the soft-start time of the DC/DC converter, VR starts up with delay.

(3) VD

When the DC/DC converter stops and at the same time, the N-channel transistor of VDOUT pin turns on, VDOUT pin outputs “L”. To release it, when VOUT2 voltage becomes equal or more than VD detector threshold ＋ hysteresis width (-VDET + VHYS), after VD release delay time (TPLH) the N-channel transistor inside the IC turns off and VDOUT pin becomes pull-up voltage by an external resistance.

(3) Start-up and Turning off by VR output decrease



Timing chart of turning off by VR output voltage decreases, DC/DC converter, VD and VR can be explained as below:

(1) DC/DC converter

DC/DC converter operates regardless of the operation of VR.

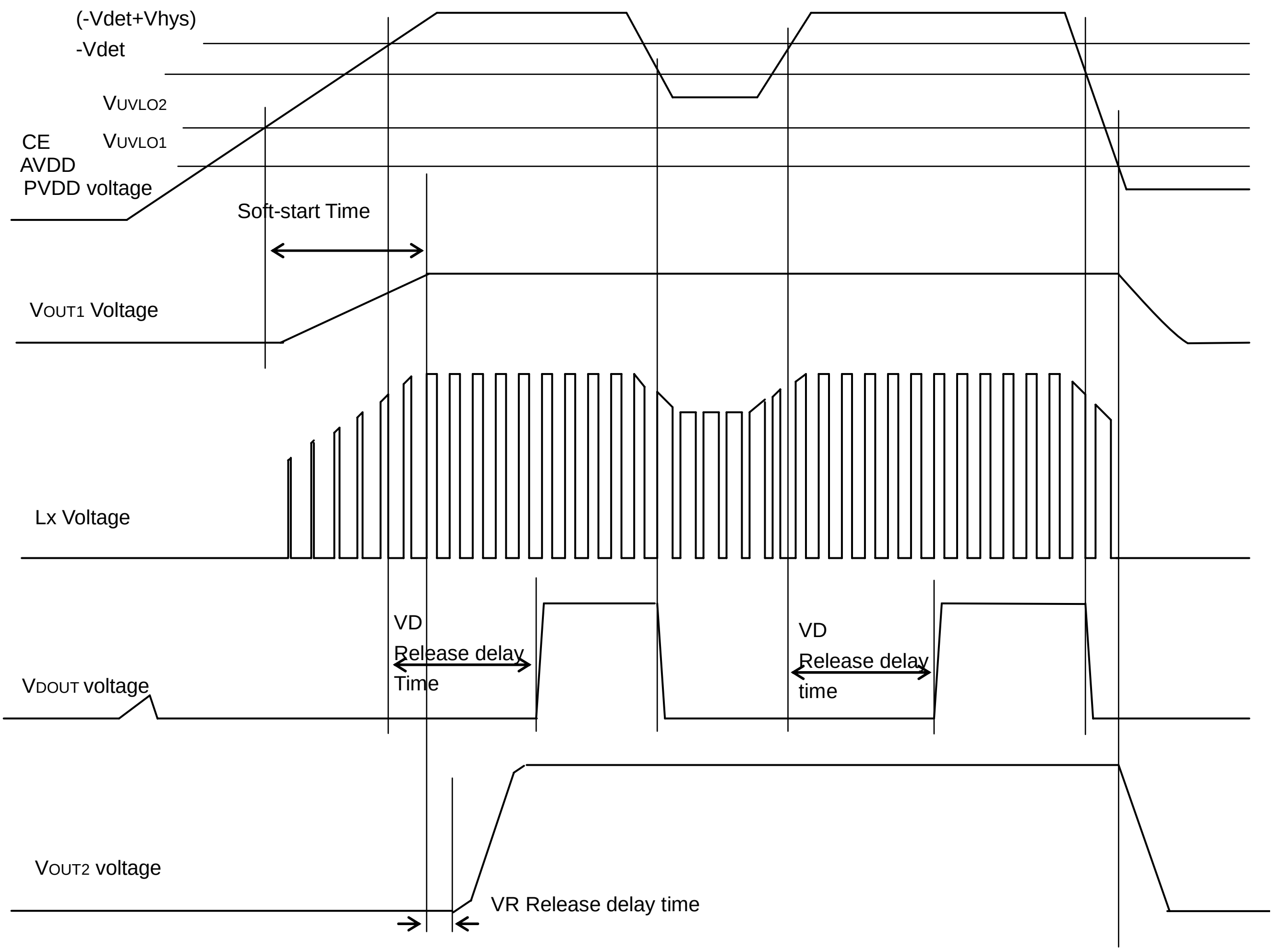
(2) VR

Since the short current limit is built-in, if the output is short to the GND or over- current flows, the output decreases with current limit. If the over current is released and set output voltage appears.

(3) VD

If VOUT2 becomes equal or less than VD detector threshold (-VDET), N-channel transistor of VDOUT pin turns on and VDOUT pin outputs ”L”. To release VD, when the voltage of VOUT2 becomes equal or more than VD detector threshold＋hysteresis width (-VDET + VHYS), after VD release delay time (TPLH), the N-channel transistor inside the IC turns off, VDOUT pin becomes pull-up voltage by an external resistance.

TIMING CHART (B Version)



Timing chart with Power supply change and DC/DC converter, VD and VR can be explained as below:

(1) DC/DC converter

Power supply is forced and VDD voltage increases, and if VDD voltage becomes equal or less than UVLO release voltage (VUVLO2), DC/DC converter operation stops and becomes no switching, therefore, VOUT1 voltage does not rise. When VDD voltage becomes equal or more than UVLO release voltage, the DC/DC converter starts soft-start and switching starts and VOUT1 voltage rises. After the soft-start time, if VDD voltage becomes equal or more than VOUT1 set voltage, VOUT1 voltage becomes set output voltage. When VDD voltage becomes equal or less than UVLO detector threshold (VUVLO1), the DC/DC converter stops switching and Lx transistor inside the IC turns off.

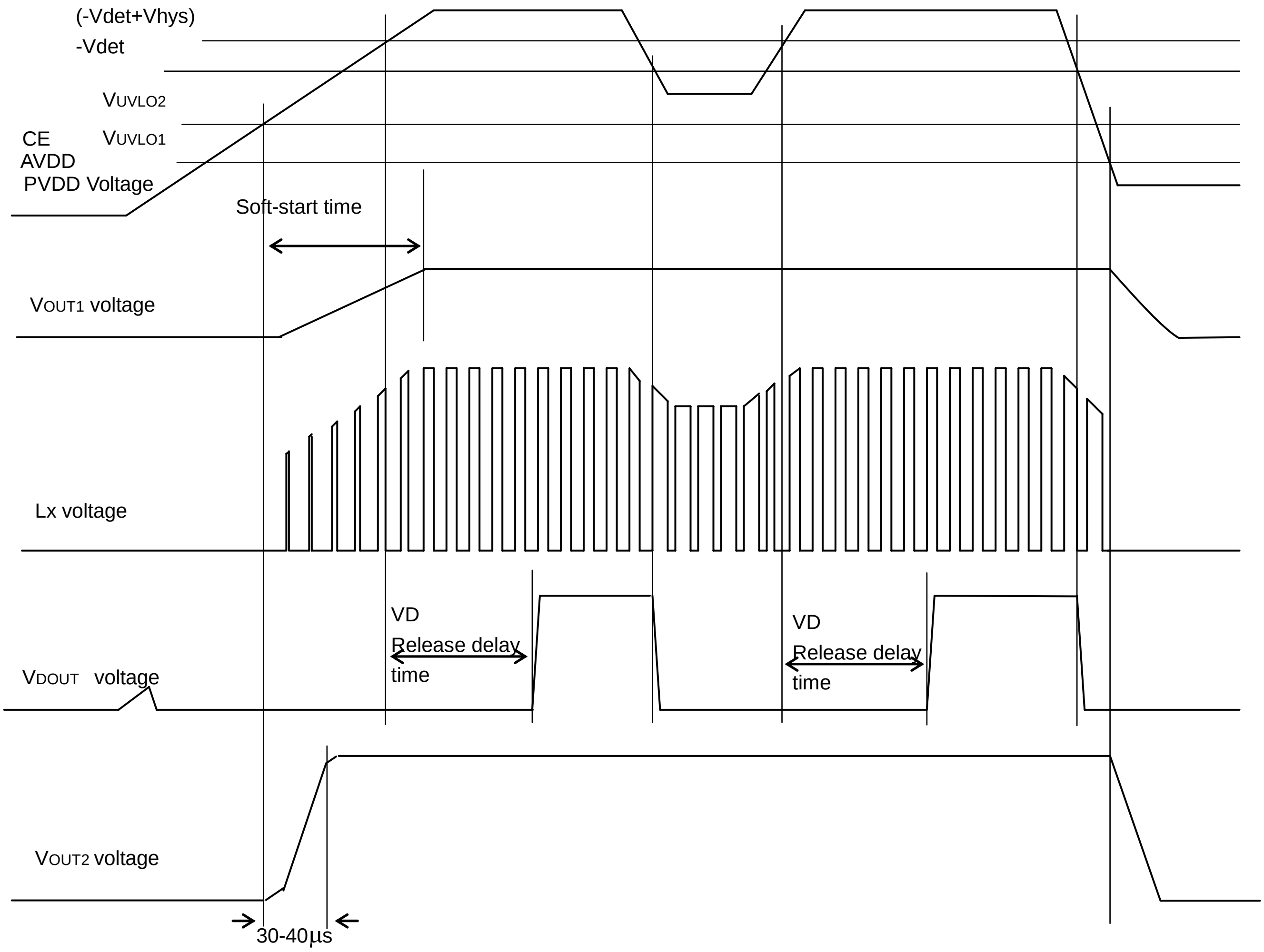
(2) VR

After the soft-start of DC/DC converter, VR starts up with delay. When the voltage of VDD becomes equal or less than UVLO detector threshold (VUVLO1), the operation stops and auto-discharge function starts.

(3) VD

VD operates regardless of the DC/DC converter, VR, thermal shutdown circuit, and chip-enable function. If the voltage of VDD becomes equal or less than VD detector threshold (-VDET), N-channel transistor of VDOUT pin turns on and VDOUT pin outputs ”L”. Then, when the voltage of VDD becomes equal or more than VD detector threshold＋hysteresis width (-VDET + VHYS), after VD release delay time(TPLH), N-channel transistor inside the IC turns off and VDOUT pin becomes pull-up voltage by an external resistance.

TIMING CHART (C/D Version)



Timing chart of the power supply change, DC/DC converter, VD, VR can be explained as below:

(1) DC/DC converter

Power supply is forced and when the voltage of VDD rises, the voltage of VDD is equal or less than UVLO release voltage (VUVLO2), DC/DC converter's operation stops and becomes no switching, therefore the voltage of VOUT1 does not rise. When the voltage of VDD becomes equal or more than UVLO release voltage, DC/DC converter starts soft-start and switching begins and the voltage of VOUT1 rises. After soft-start time, if the voltage of VDD becomes equal or more than the set VOUT1 voltage, the output of VOUT1 becomes set output voltage. When the voltage of VDD becomes equal or less than UVLO detector threshold (VUVLO1), DC/DC converter stops switching, Lx transistor inside the IC turns off.

(2) VR

When the voltage of VDD becomes equal or more than UVLO release voltage, after the 30µs to 40µs or around, VR starts up. (Cout=2.2µF)

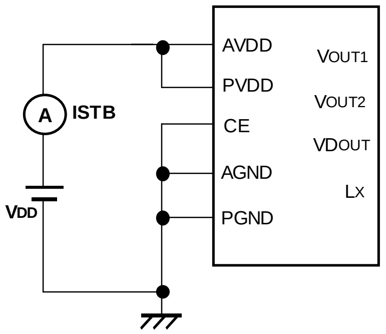
If the voltage of VDD becomes equal or less than UVLO detector threshold (VUVLO1), the operations stops and auto-discharge function operates.

(3) VD

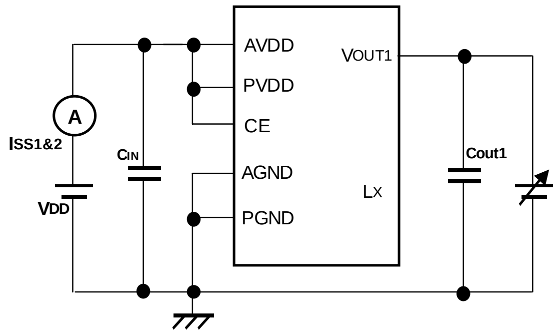
VD operates regardless of DCDC, VR, thermal shutdown circuit, chip-enable function. When the voltage of VDD becomes or less than VD detector threshold (-VDET), N-channel transistor of VDOUT pin turns on, VDOUT pin outputs "L". Then when the voltage of VDD becomes equal or more than VD detector threshold＋hysteresis width (-VDET + VHYS), after VD release delay time (TPLH), N-channel transistor inside the IC turns off, VDOUT pin becomes pull-up voltage by an externa resistance.

TEST CIRCUITS

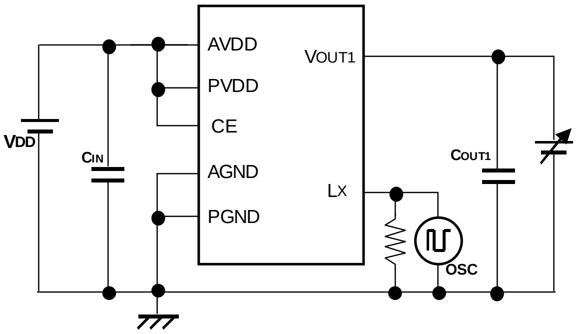
Standby Current Test Circuit



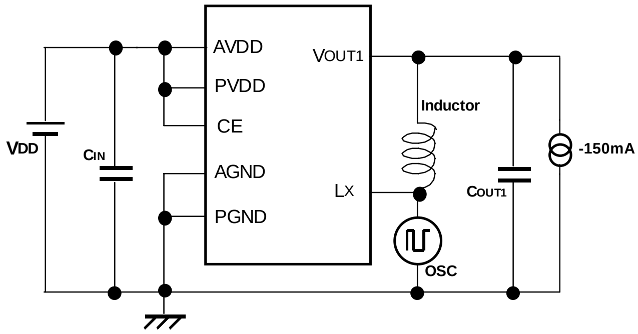
Supply Current 1, 2 Test Circuit



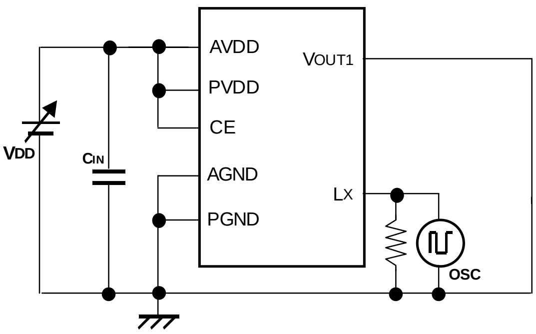
DC/DC Output Voltage Test Circuit



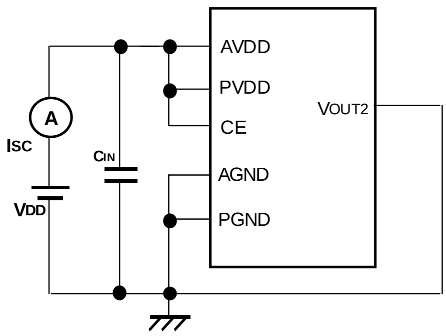
DC/DC Oscillator Frequency Test Circuit



UVLO Detect and Release Voltage Test Circuit

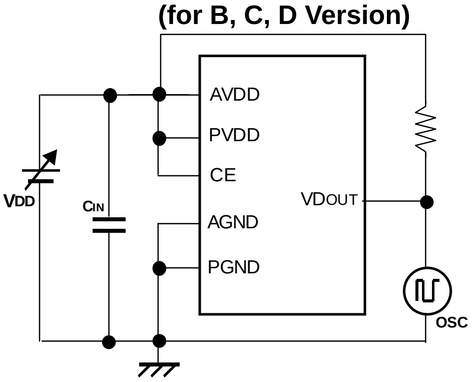


VR Short Current Test Circuit



VD Detect and Release Voltage Test Circuit

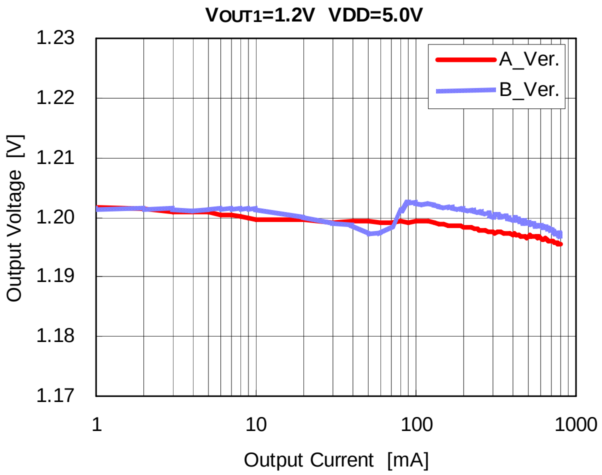
(for B, C, D Version)

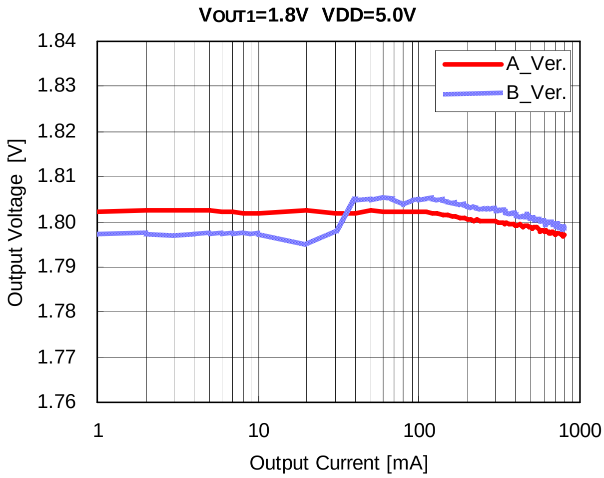


TYPICAL CHARACTERISTIC

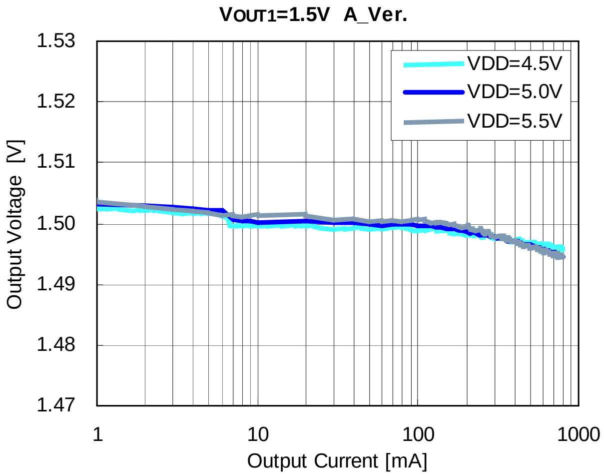
(unless otherwise specified, characteristics of C, D Version are same as B Version)

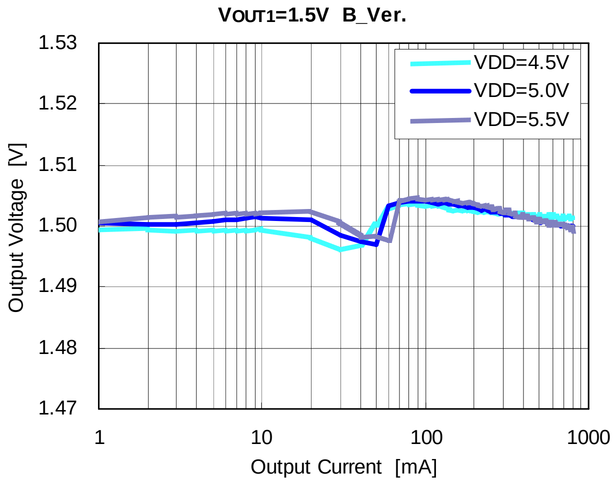
1) DC/DC output voltage vs. output current
Version comparison



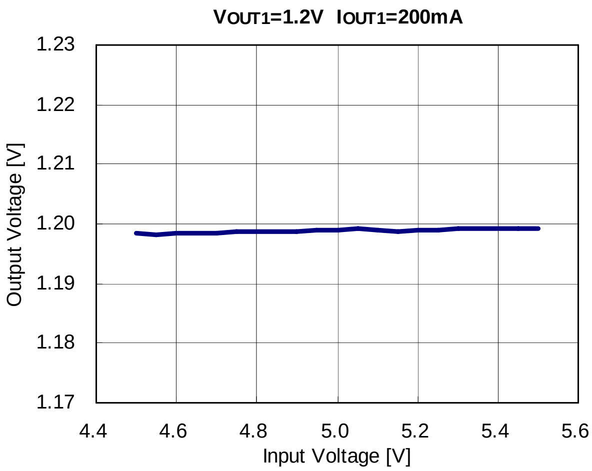


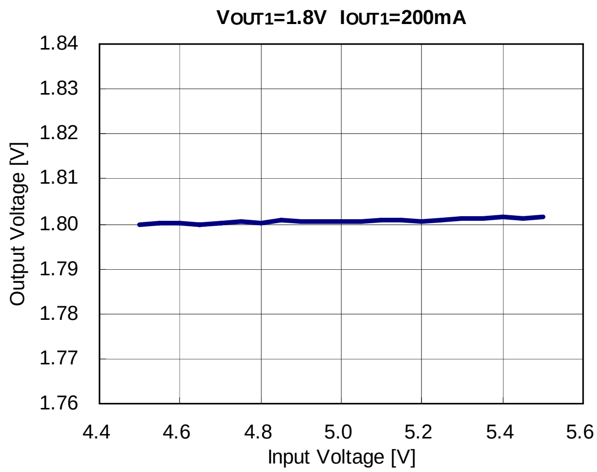
Input voltage comparison





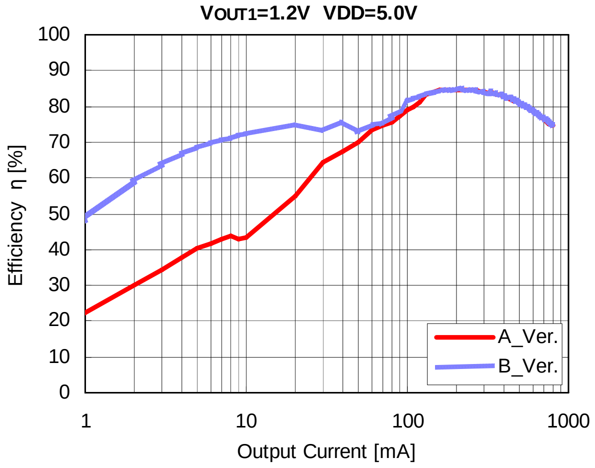
2) DC/DC output voltage vs. Input voltage

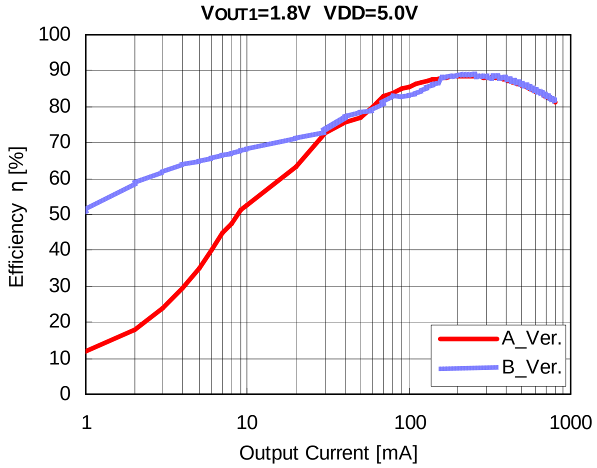




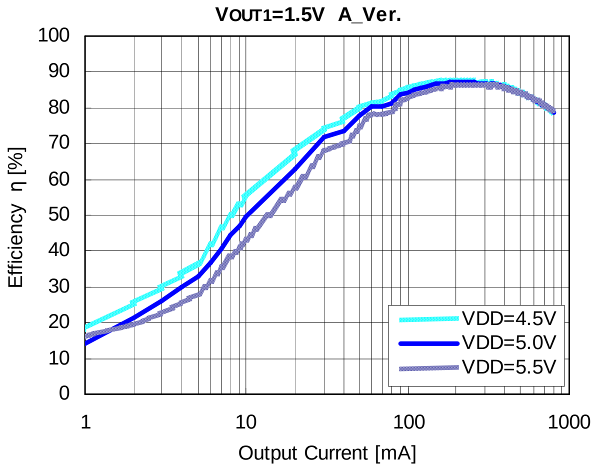
3) Efficiency vs. Output current

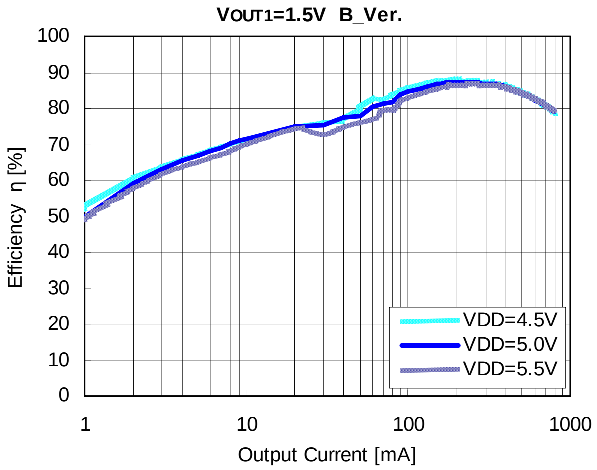
(1) Version comparison



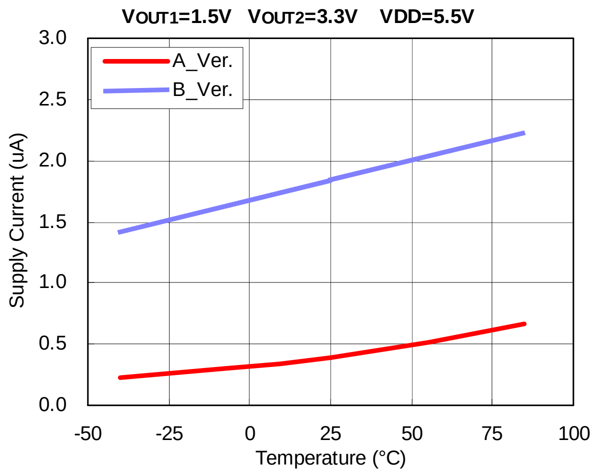


(2) Input voltage comparison

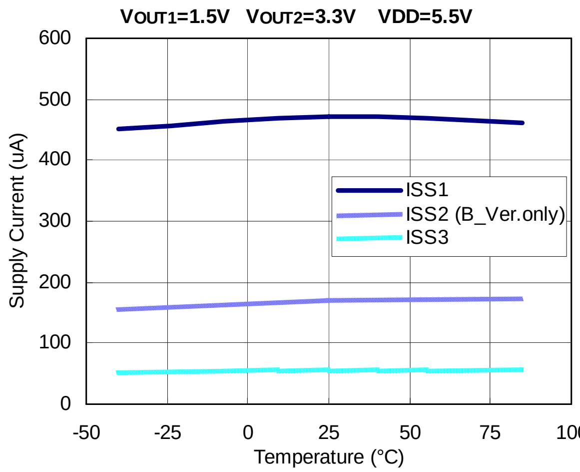




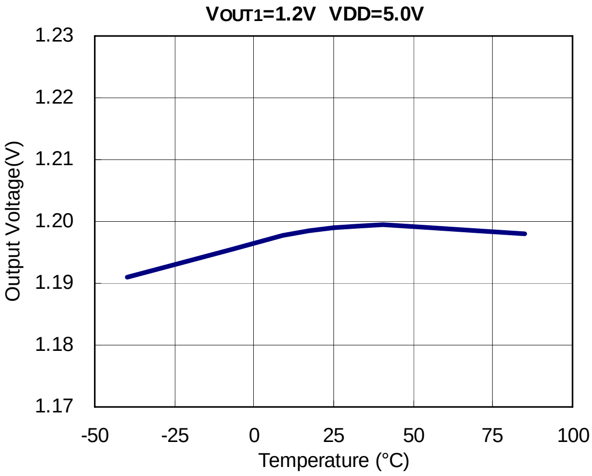
4) Standby Current vs. Temperature

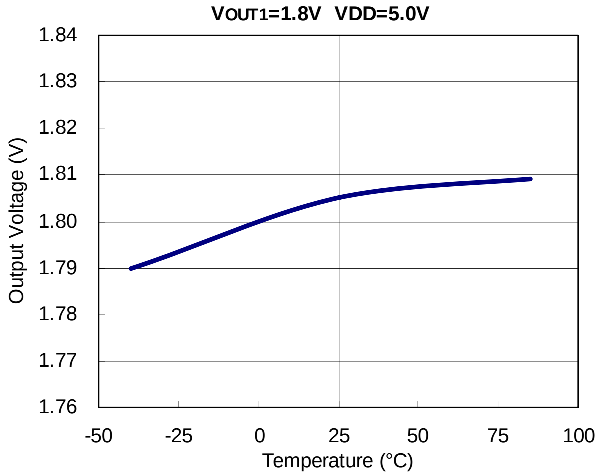


5) Supply Current 1, 2, 3 vs. Temperature

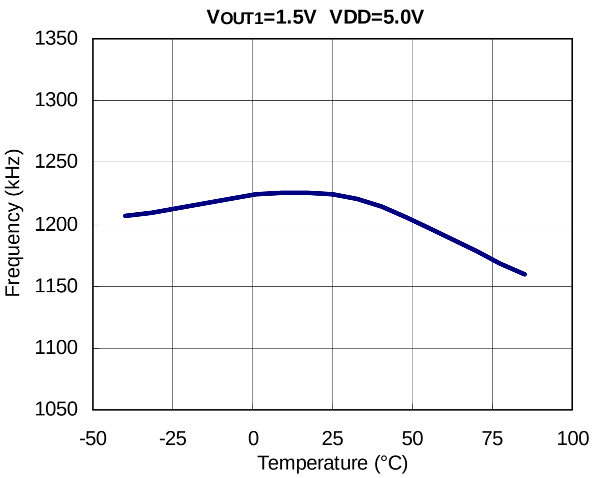


6) DC/DC output voltage vs. Temperature

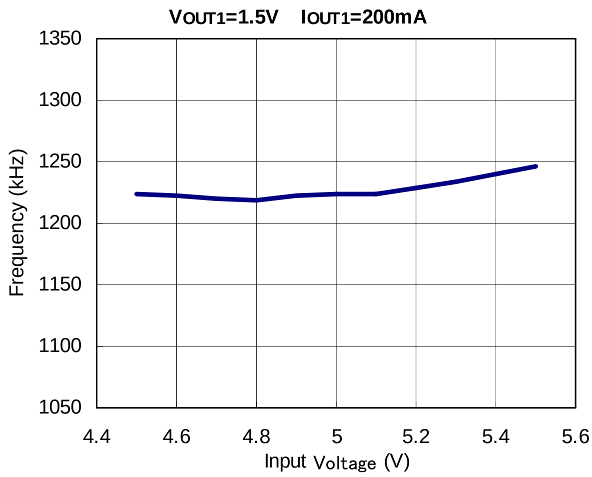




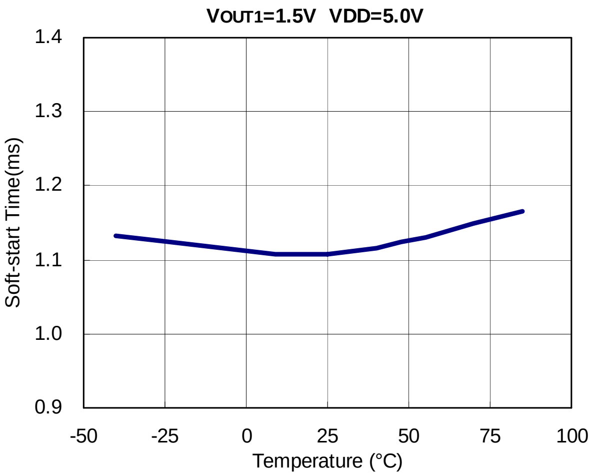
7) Oscillator frequency vs. Temperature



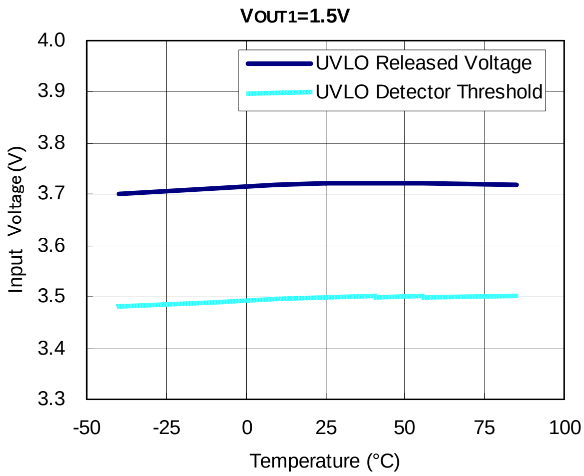
8) Oscillator frequency vs. Input voltage



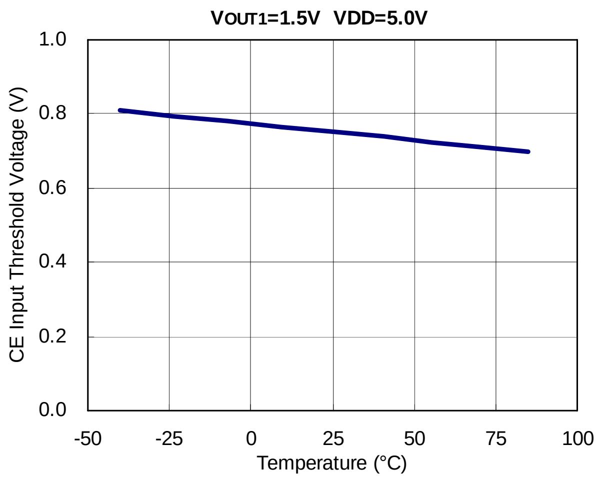
9) Soft-start time vs. Temperature



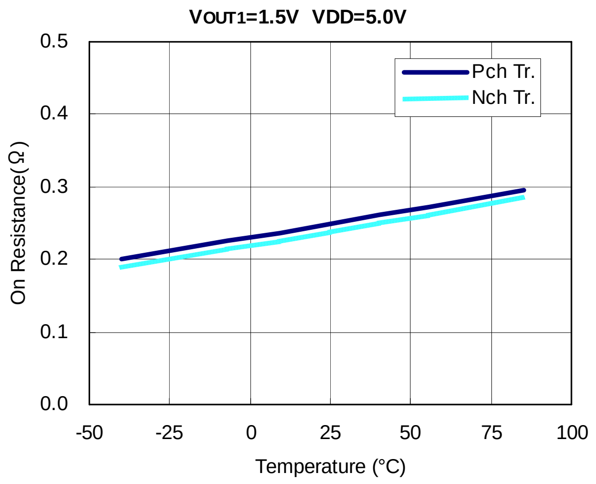
10) UVLO detect / release voltage vs. Input voltage



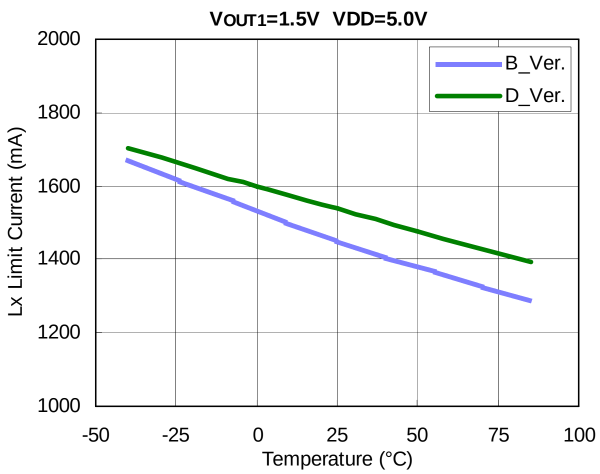
11) CE Input voltage vs. Temperature



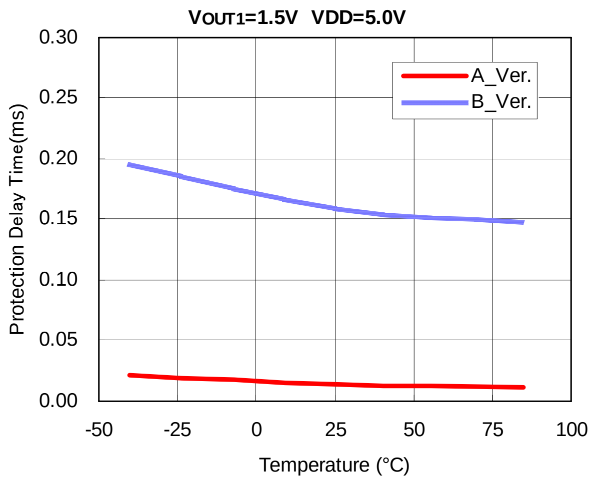
12) P-channel/N-channel Tr. ON resistance vs. Temperature



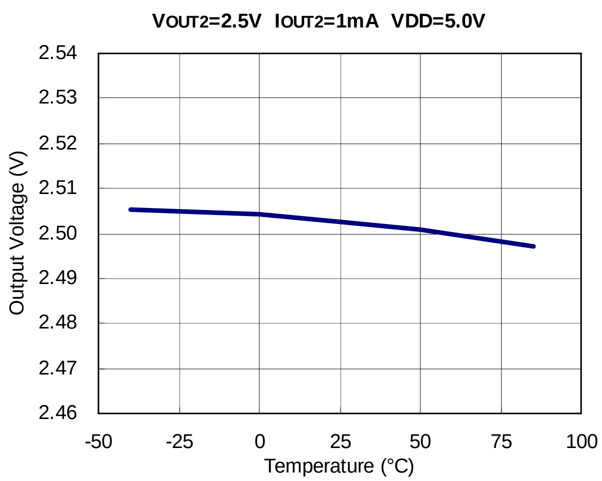
13) Lx Current limit vs. Temperature (Version comparison)

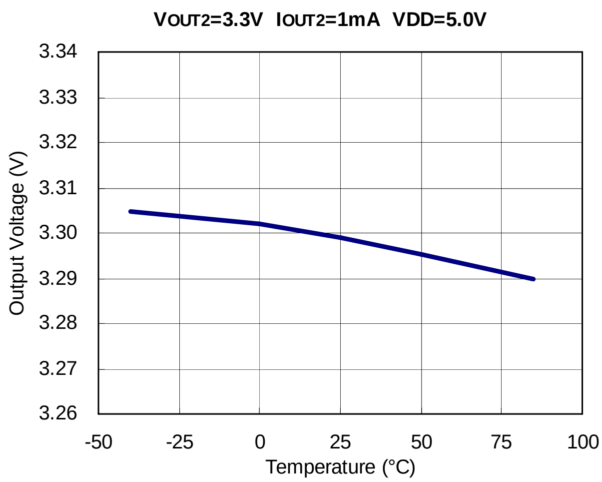


14) Protection delay time vs. Temperature (Version comparison)

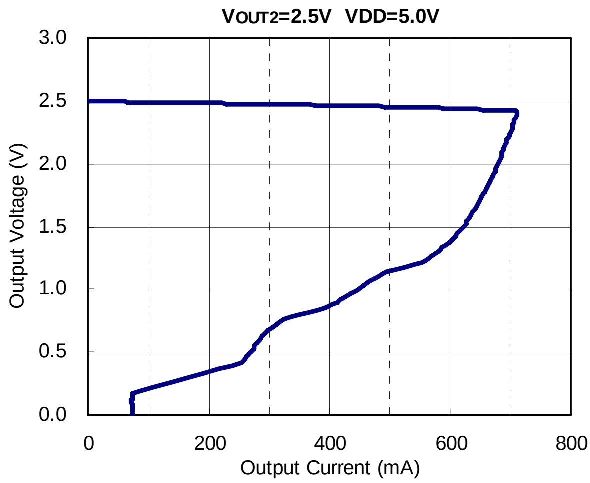


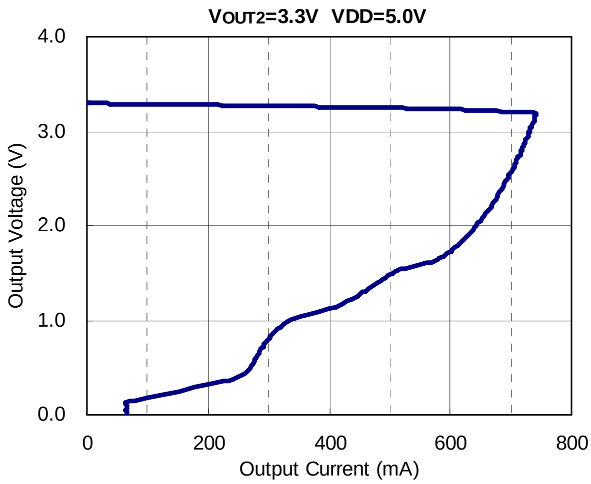
15) VR Output voltage vs. Temperature



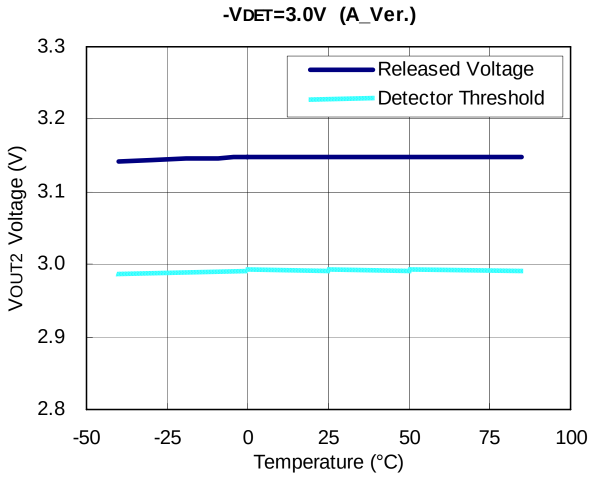


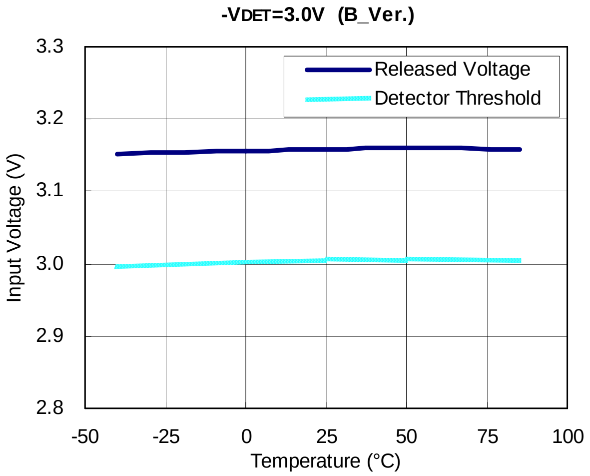
16) VR Output voltage vs. Output current



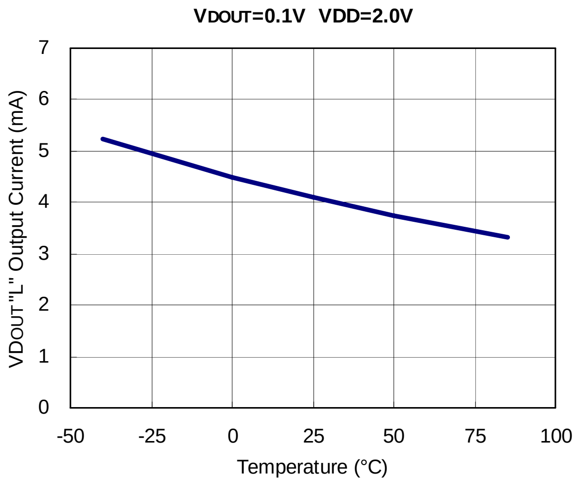


17) VD detect/ release voltage vs. Temperature (Version comparison)

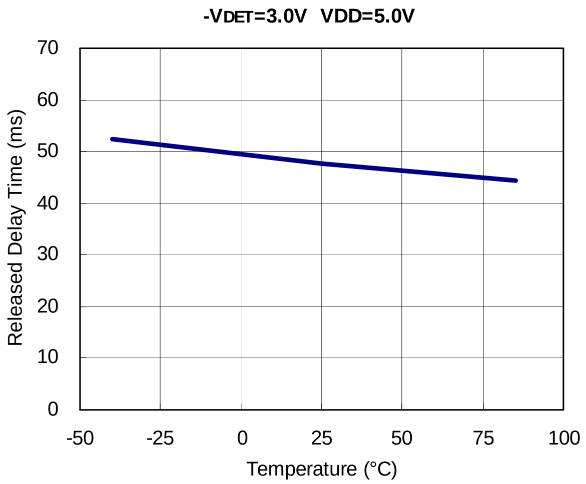




18) VDOUT "L" Output current vs. Temperature



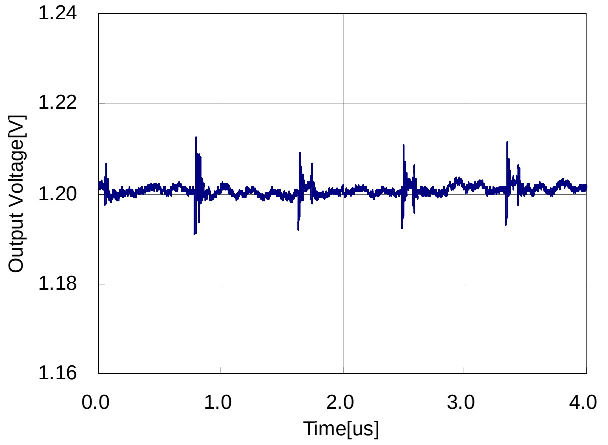
19) Release delay time vs. Temperature



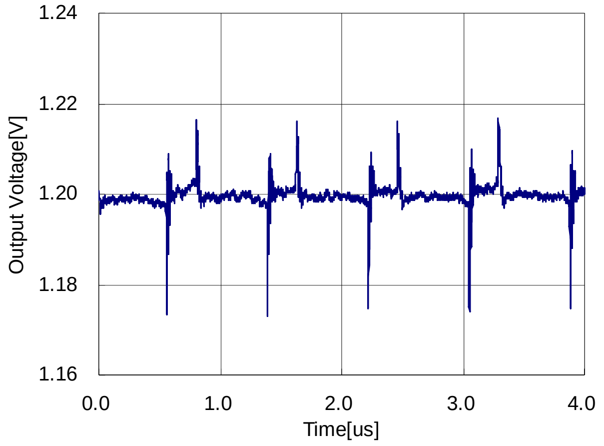
20) DC/DC Output voltage waveform (Version comparison)
(C_{IN}=Ceramic 10uF, C_{OUT1}= Ceramic 10uF, L=4.7uH, V_{DD}=5.0V)

A Version

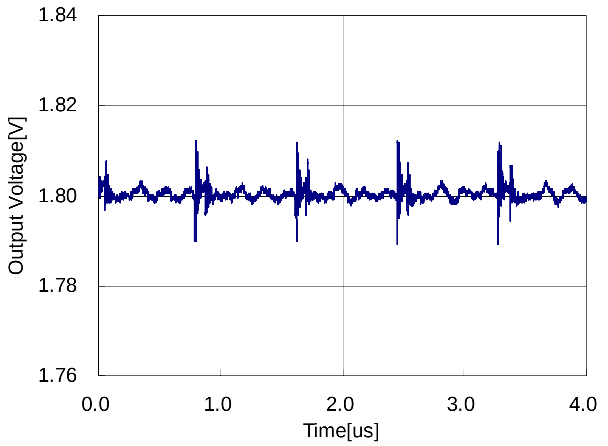
VOUT1=1.2V IOUT1=10mA A_Ver.



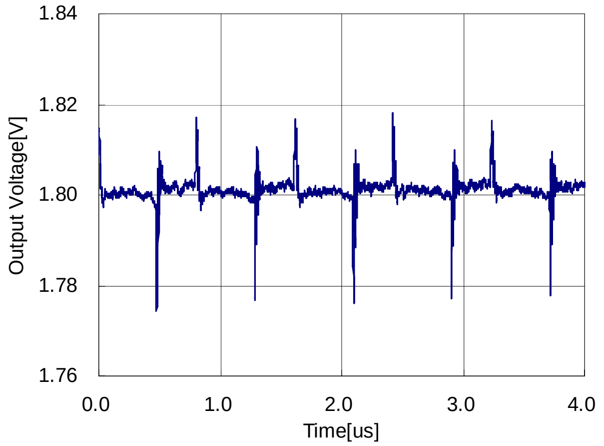
VOUT1=1.2V IOUT1=400mA A_Ver.



VOUT1=1.8V IOUT1=10mA A_Ver.

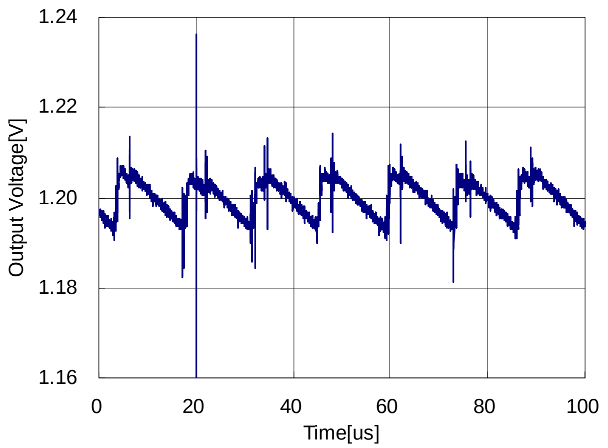


VOUT1=1.8V IOUT1=400mA A_Ver.

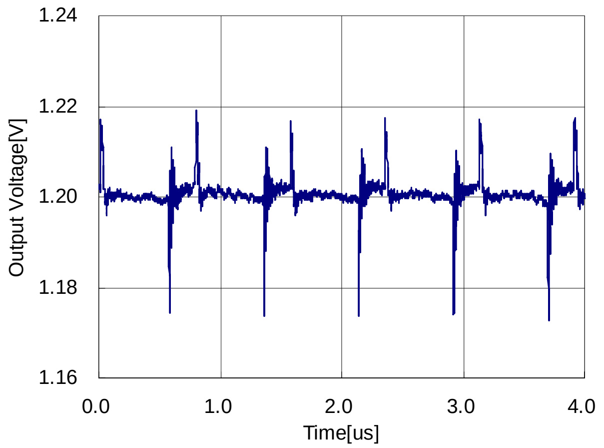


B Version

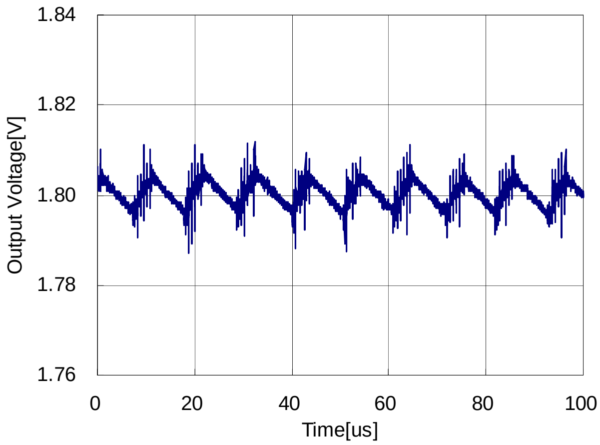
VOUT1=1.2V IOUT1=10mA B_Ver.



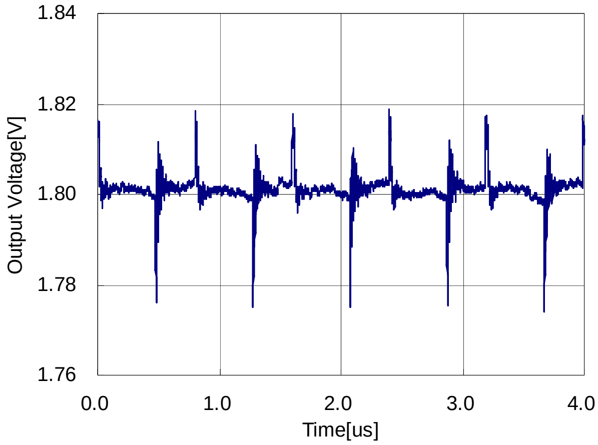
VOUT1=1.2V IOUT1=400mA B_Ver.



VOUT1=1.8V IOUT1=10mA B_Ver.



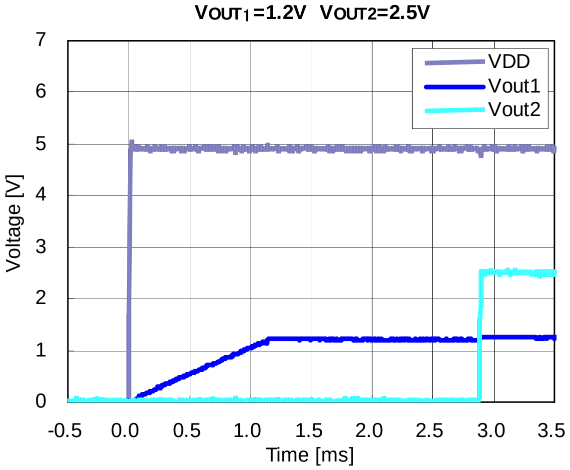
VOUT1=1.8V IOUT1=400mA B_Ver.



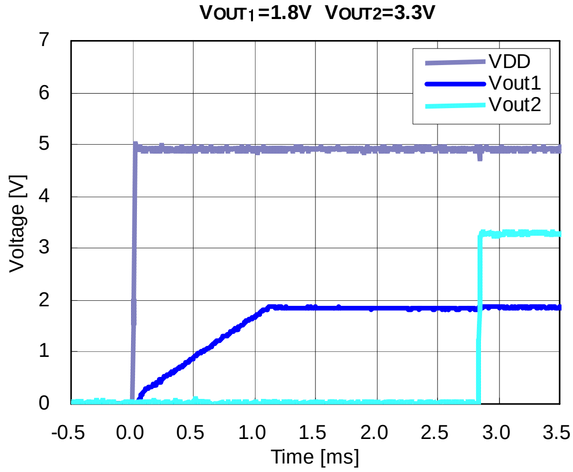
21) VOUT1, VOUT2 start-up waveform (Version comparison)
(CIN=Ceramic 10uF, COUT1= Ceramic 10uF, COUT2= Ceramic 2.2uF, L=4.7uH)

A, B Version

VOUT1=1.2V VOUT2=2.5V

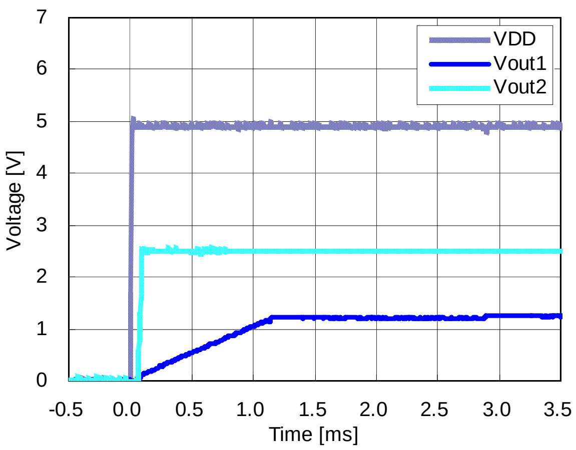


VOUT1=1.8V VOUT2=3.3V

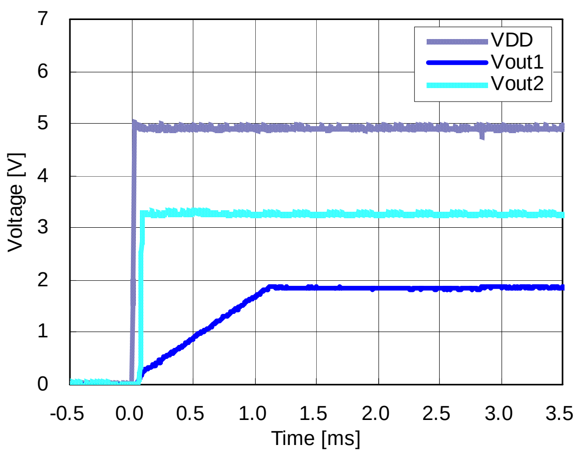


C, D Version

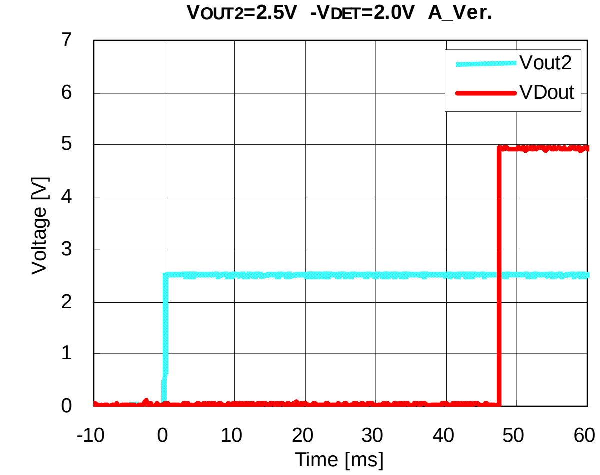
VOUT1=1.2V VOUT2=2.5V

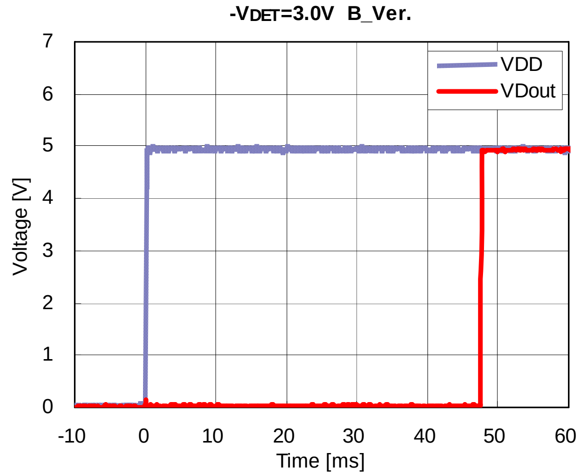


VOUT1=1.8V VOUT2=3.3V



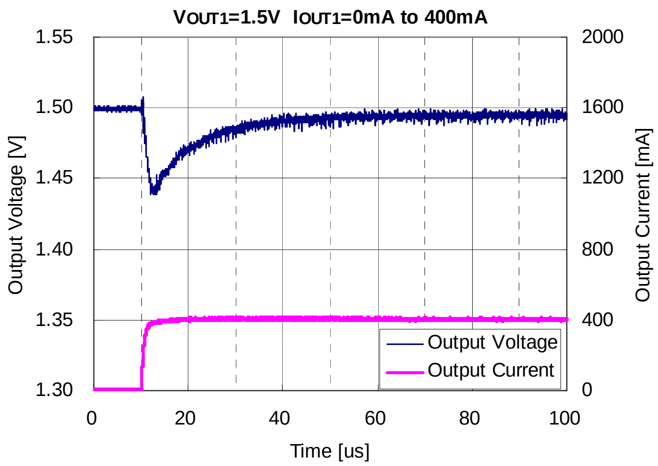
22) VDOUT Release Delay Waveform (Version comparison)
(CIN=Ceramic 10uF, COUT1= Ceramic 10uF, COUT2= Ceramic 2.2uF, L=4.7uH)

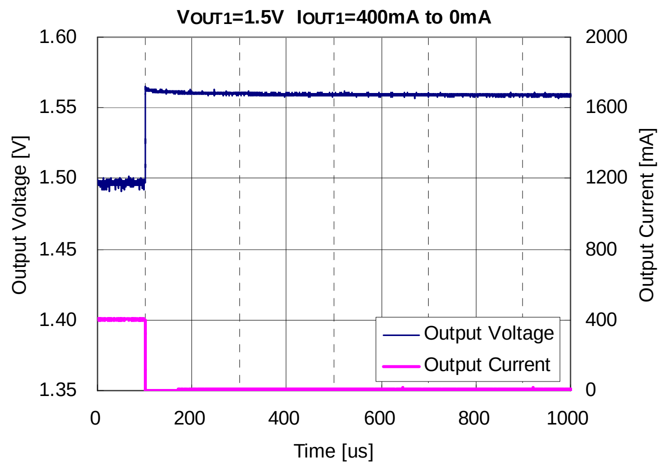


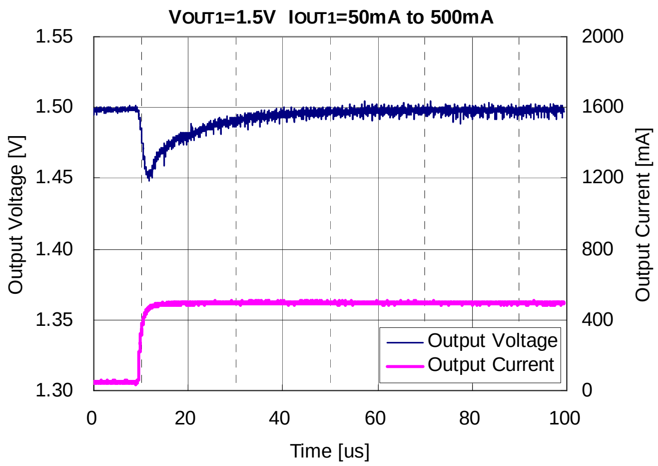


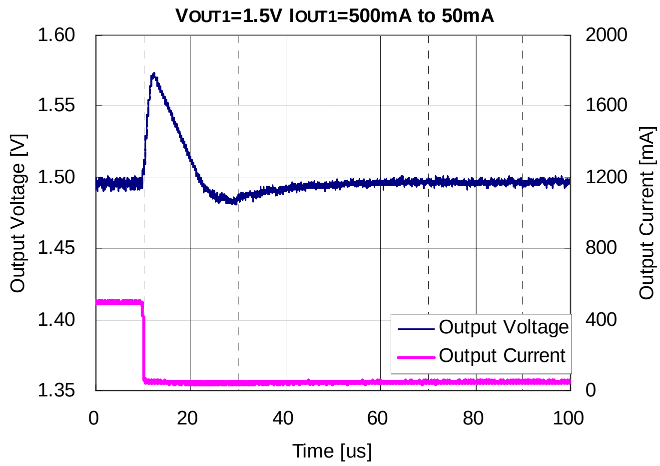
23) DC/DC Load transient response (Version comparison)
(CIN=Ceramic 10uF, COUT1= Ceramic 10uF, L=4.7uH , VDD=5.0V)

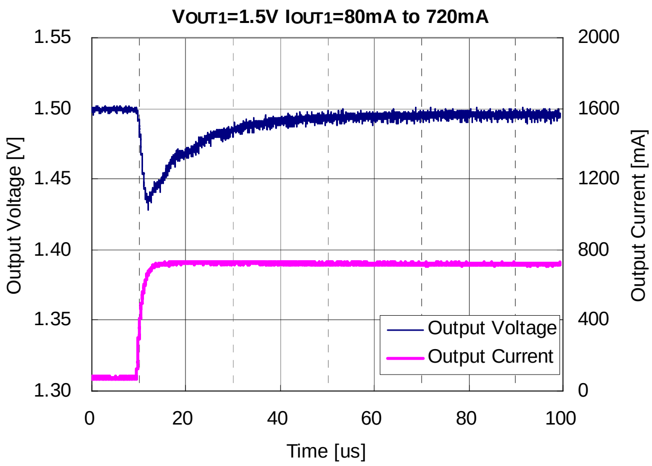
A Version, VOUT1=1.5V

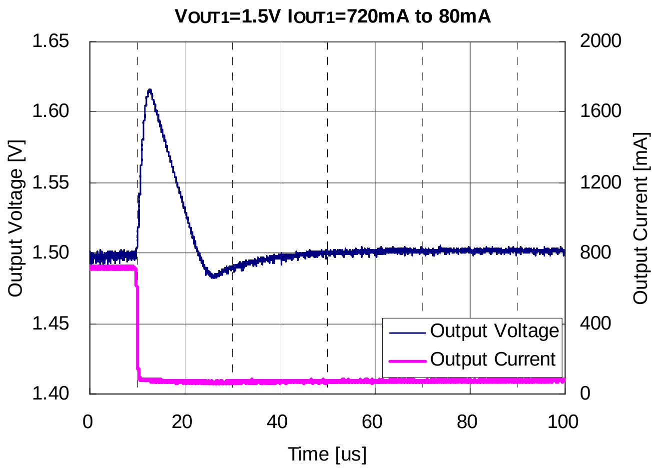




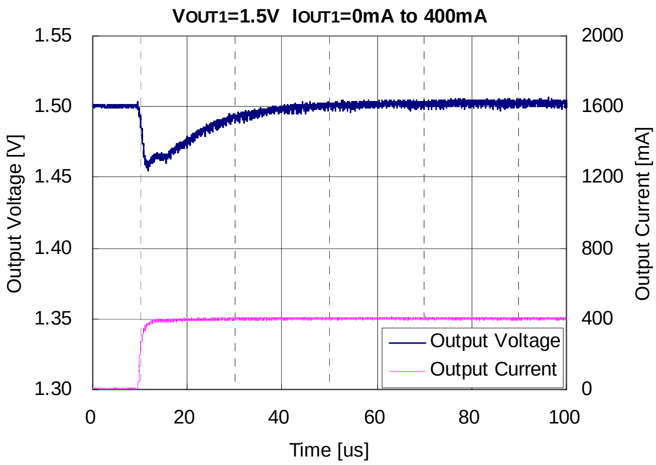


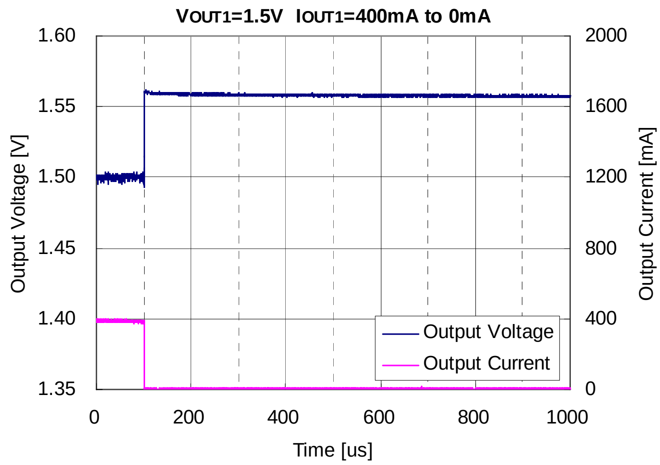


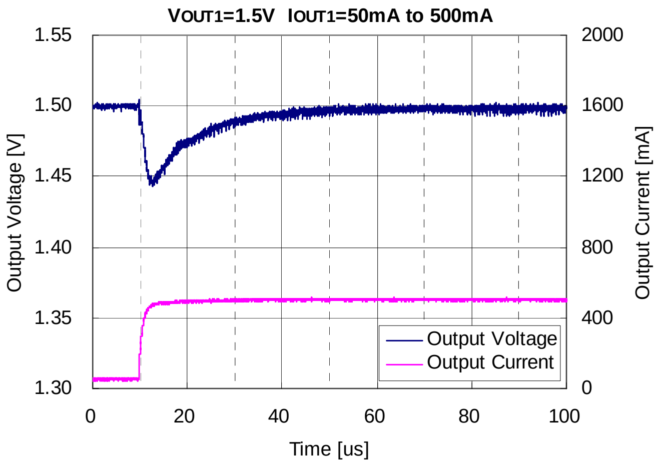


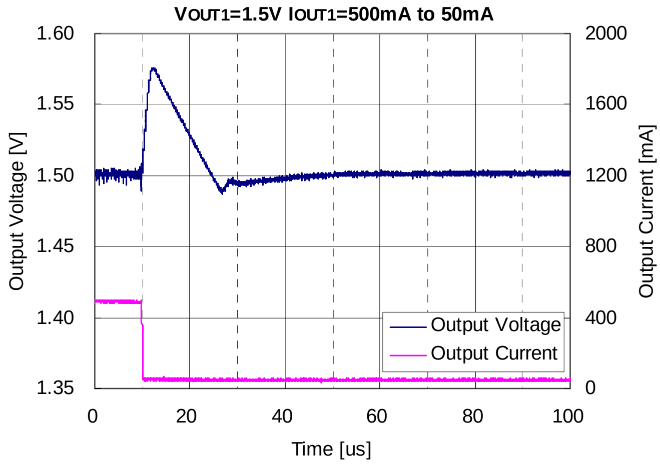


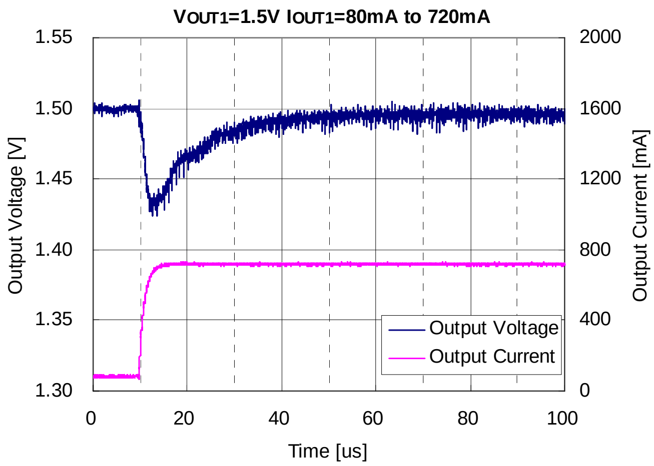
B Version VOUT1=1.5V

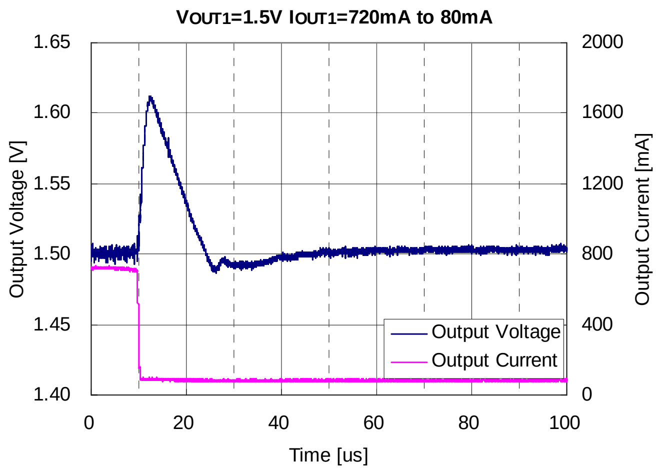






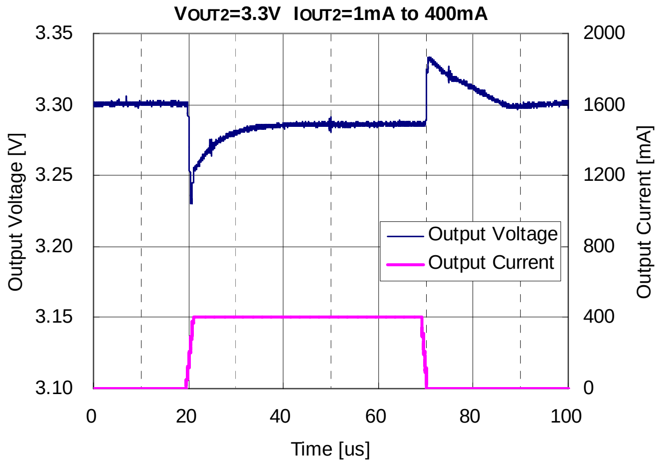


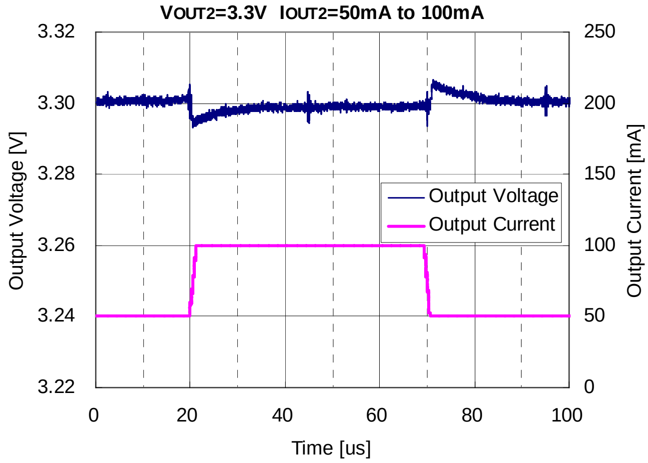




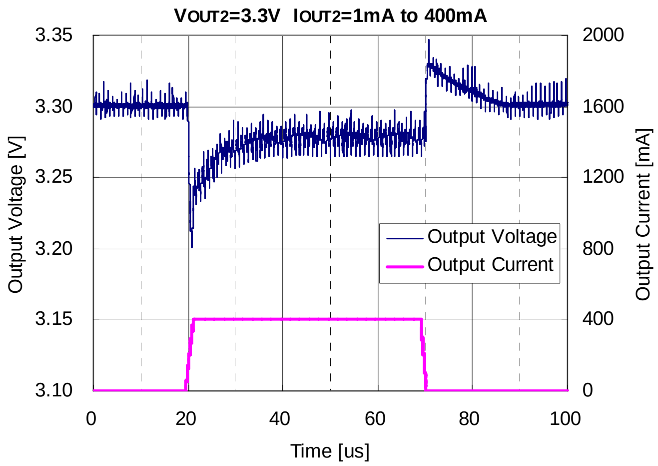
24) VR Load transient response (DC/DC load current comparison) (CIN=Ceramic 10uF, COUT2= Ceramic 2.2uF, VDD=5.0V)

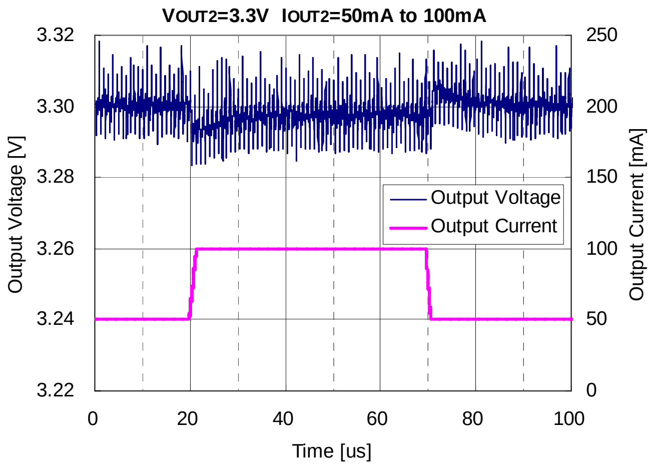
DC/DC load current IOUT2=0mA





DC/DC load current IOUT2=400mA





POWER DISSIPATION-(1) / DFN(PLP)2527-10

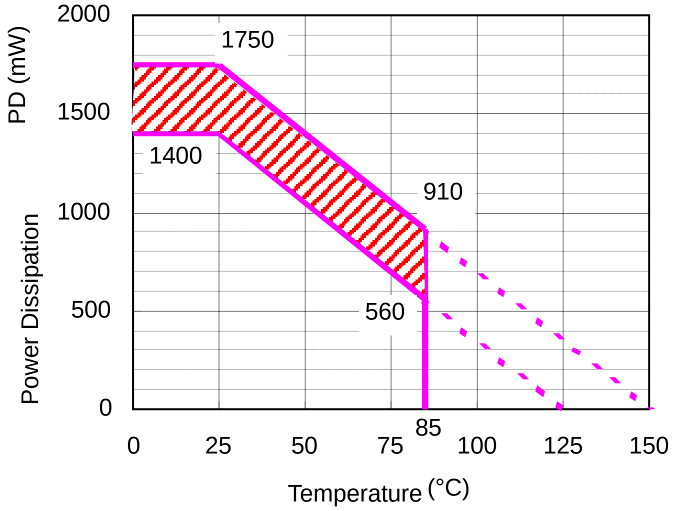
DFN(PLP)2527-10 package power dissipation characteristic is shown below.
The power dissipation depends on the conditions of the mounting on PCB and this is just an example.

Test conditions

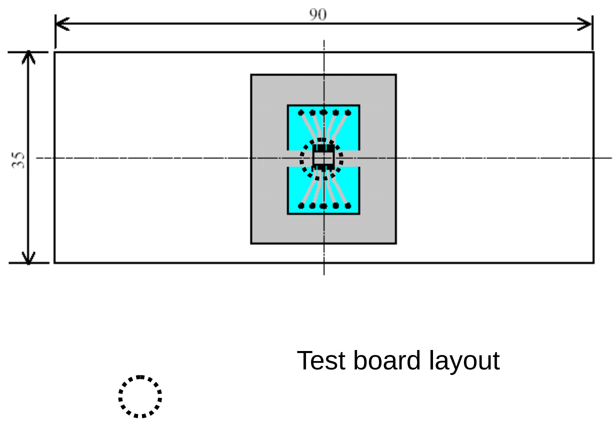
	Standard Mounting on Board Condition
Test Condition	Mounting on board (Wind velocity 0m/s)
Board material	Glass Epoxy Resin (4-layer)
Board dimensions	35mm x 90mm x 0.8mm
Wiring ratio	Each layer 15%
Cupper wire thickness	Top/Bottom layer: 35μm, Middle layer: 18μm
Through holes	9(φ0.3mm) package tab connection land pattern, from top to bottom 10 (φ0.5mm) for each pin connection

Measurement result (Ta=25ºC)

	Standard Mounting on Board Conditions
Power Dissipation	1400mW (Tjmax=125°C) 1750mW (Tjmax=150°C)
Thermal Resistance	θja = (125-25°C) / 1.4W 71°C / W



Power Dissipation Characteristic



Test board layout

IC mount position (Unit : mm)

* The hatched area usage has some impact on the product life time. The time for the usage of the hatched area should be less than 13,000 hours. If four hours a day, the product is used, the time limit is 9 years.

POWER DISSIPATION-(2) / DFN(PLP)2527-10

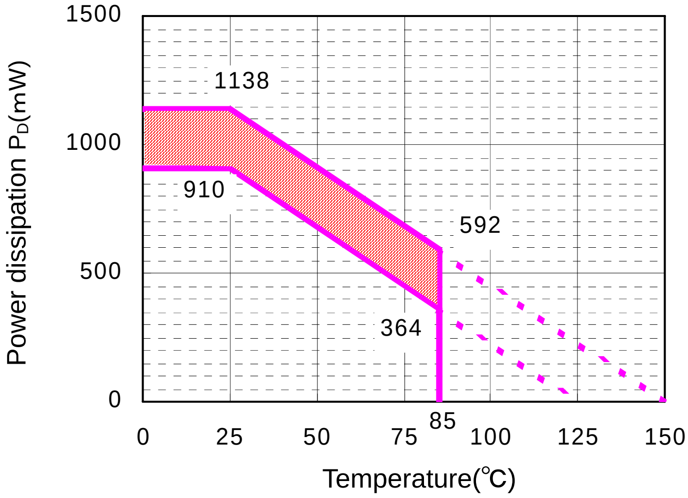
DFN(PLP)2527-10 package another typical characteristic is shown below.

Test Conditions

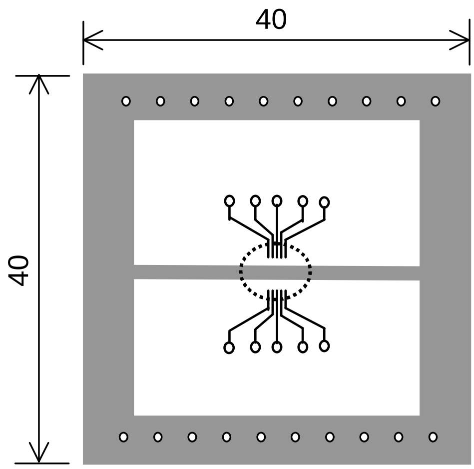
	Mounting on Board Conditions (2)
Test condition	Mounting on Board (Wind Velocity 0m/s)
Board material	Glass Epoxy Resin (Printed on both sides)
Board dimensions	40mm × 40mm × 1.6mm
Wiring ratio	Top side 50%, Bottom side 50%
Through holes	Diameter 0.54mm × 30 pcs

Measurement result (Ta=25°C)

	Mounting on Board Conditions (2)
Power dissipation	910mW (Tjmax=125°C) 1138mW (Tjmax=150°C)
Thermal resistance	θja = (125-25°C) / 0.91W = 110°C /W



Power Dissipation Characteristic



Test Board Layout

IC mount position (Unit: mm)

*Tjmax=125°C and Tjmax=150°C Power dissipation charactetristics are shown in the graph. The hatched area usage has some impact on the product lifetime. Time limit is described in the next table.

Time limit	Product life time (4hours/day usage)
13,000 hrs	9 years

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