

nRF52832 Product Specification v1.4

Key features

- 2.4 GHz transceiver
 - -96 dBm sensitivity in *Bluetooth*® low energy mode
 - Supported data rates: 1 Mbps, 2 Mbps Bluetooth® low energy mode
 - -20 to +4 dBm TX power, configurable in 4 dB steps
 - On-chip balun (single-ended RF)
 - 5.3 mA peak current in TX (0 dBm)
 - 5.4 mA peak current in RX
 - RSSI (1 dB resolution)
- ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz
 - 215 EEMBC CoreMark® score running from flash memory
 - 58 μ A/MHz running from flash memory
 - 51.6 μA/MHz running from RAM
 - Data watchpoint and trace (DWT), embedded trace macrocell (ETM), and instrumentation trace macrocell (ITM)
 - Serial wire debug (SWD)
 - Trace port
- Flexible power management
 - 1.7 V-3.6 V supply voltage range
 - Fully automatic LDO and DC/DC regulator system
 - Fast wake-up using 64 MHz internal oscillator
 - 0.3 μA at 3 V in System OFF mode
 - + 0.7 μA at 3 V in System OFF mode with full 64 kB RAM retention
 - 1.9 μA at 3 V in System ON mode, no RAM retention, wake on RTC
- Memory
 - 512 kB flash/64 kB RAM
 - 256 kB flash/32 kB RAM
- Nordic SoftDevice ready
- Support for concurrent multi-protocol
- Type 2 near field communication (NFC-A) tag with wakeup-on-field and touchto-pair capabilities
- 12-bit, 200 ksps ADC 8 configurable channels with programmable gain
- 64 level comparator
 15 level low power c
- 15 level low power comparator with wakeup from System OFF mode
- Temperature sensor
- 32 general purpose I/O pins
- 3x 4-channel pulse width modulator (PWM) unit with EasyDMA
- Digital microphone interface (PDM)
- 5x 32-bit timer with counter mode
- Up to 3x SPI master/slave with EasyDMA
- Up to 2x I2C compatible 2-wire master/slave
- I2S with EasyDMA
- UART (CTS/RTS) with EasyDMA
- Programmable peripheral interconnect (PPI)
- Quadrature decoder (QDEC)
- AES HW encryption with EasyDMA
- Autonomous peripheral operation without CPU intervention using PPI and EasyDMA
- 3x real-time counter (RTC)
- Single crystal operation
- Package variants
 - QFN48 package, 6 × 6 mm
 - WLCSP package, 3.0 × 3.2 mm

Application:

- Internet of Things (IoT)
 - Home automation
 - Sensor networks
 - Building automation
 - Industrial
 - Dotoi

Personal area networks

- Health/fitness sensor and monitor devices
 - Medical devices
 - Key fobs and wrist watches

Interactive entertainment devices

- Remote controls
 - Gaming controllers

Reacons

- A4WP wireless chargers and devices
- Remote control toys
- Computer peripherals and I/O devices
- Mouse
 - Keyboard
 - Multi-touch trackpad
 - Gaming



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1 Revision history

Date	Version	Description
October 2017	1.4	The following content has been added or updated:
		 Recommended operating conditions on page 20: Added WLCSP light sensitivity information. FICR — Factory information configuration registers on page 43: Added registers PARTNO,
		HWREVISION and PRODUCTIONREVISION. • UICR — User information configuration registers
		on page 54: Changed width of PSELRESETn port fields.
		 SPIM: Polarity in SPI mode table corrected. COMP — Comparator on page 392: Documentation structure improvements/changes.
		 Liability disclaimer updated: Directive 2011/65/EU (RoHS 2).
February 2017	1.3	 The following content has been added or updated: RADIO — 2.4 GHz Radio on page 205:
		Introduced 2 Mbps Bluetooth* low energy mode. • FICR — Factory information configuration registers
		on page 43: Updated INFO.PACKAGE register (new package added).
		 UARTE: Corrected the pin configuration table. PPI — Programmable peripheral interconnect on
		page 168: Timing information corrected. • Updated the liability disclaimer.
September 2016	1.2	Updated the following:
		 Power and clock management, Current consumption: Ultra-low power on page 77. Power, Current consumption, sleep on page
July 2016	1.1	99 Added documentation for nRF52832 CIAA WLCSP.
July 2010		Added or updated the following content:
		Cover: Added Key features.
		Pin assignments on page 13: Added WLCSP ball assignments. Moved GPIO usage restrictions here from GPIO/Notes on usage and restrictions.
		Absolute maximum ratings on page 19: Added environmental information for WLCSP to the
		 Memory on page 23: Added QFAB and CIAA information to the table.
		FICR — Factory information configuration registers on page 43: Updated INFO.PACKAGE register.
		UICR — User information configuration registers on page 54: Updated APPROTECT register.
		 Debug and trace on page 72: Updated DAP - Debug access port. POWER — Power supply on page 78: Updated
		Pin reset.
		CLOCK — Clock control on page 101: Updated information on external 32 kHz clock support.
		 GPIO — General purpose input/output on page 111: Added GPIO located near the RADIO. RADIO — 2.4 GHz Radio on page 205: Updated
		Figure 29 and Interframe spacing.
		 CCM: Updated SCRATCHPTR register. SPIM: Updated Master mode pin configuration.
		UARTE: Added RXDRDY and TXDRDY events.
		 NFCT: Updated Electrical specifications. PWM — Pulse width modulation on page 495: Updated SEQ[1].REFRESH register.
		Mechanical specifications on page 540: Added WLCSP package.
		 Ordering information on page 542: Updated with CIAA and QFAB information.
		 Reference circuitry on page 545: QFAB information added. CIAA WLCSP schematics added.
February 2016	1.0	First release.



2 About this document

This product specification is organized into chapters based on the modules and peripherals that are available in this IC.

The peripheral descriptions are divided into separate sections that include the following information:

- A detailed functional description of the peripheral
- · Register configuration for the peripheral
- Electrical specification tables, containing performance data which apply for the operating conditions described in *Recommended operating conditions* on page 20.

2.1 Document naming and status

Nordic uses three distinct names for this document, which are reflecting the maturity and the status of the document and its content.

Table 1: Defined document names

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 0.7.
Preliminary Product Specification (PPS)	This product specification contains target specifications for product development. Applies to document versions 0.7 and up to 1.0.
Product Specification (PS)	This product specification contains preliminary data. Supplementary data may be published from Nordic Semiconductor ASA later. Applies to document versions 1.0 and higher.
	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

2.2 Peripheral naming and abbreviations

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the ARM® Cortex® Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.3.1 Fields and values

The **Id** (**Field Id**) row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as 0 to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.



Values are usually provided as decimal or hexadecimal. Hexadecimal values have a 0x prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.
- Implicit values. If no values are indicated in the Value column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value** Id, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.4 Registers

Table 2: Register Overview

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

2.4.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		D D [D C C C B A A
Reset 0x00050002		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0$
Id RW Field	Value Id	Value	Description
A RW FIELD_A			Example of a field with several enumerated values
	Disabled	0	The example feature is disabled
	NormalMode	1	The example feature is enabled in normal mode
	ExtendedMode	2	The example feature is enabled along with extra functionality
B RW FIELD_B			Example of a deprecated field Deprecated
	Disabled	0	The override feature is disabled
	Enabled	1	The override feature is enabled
C RW FIELD_C			Example of a field with a valid range of values
	ValidRange	[27]	Example of allowed values for this field
D RW FIELD D			Example of a field with no restriction on the values



3 Block diagram

This block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

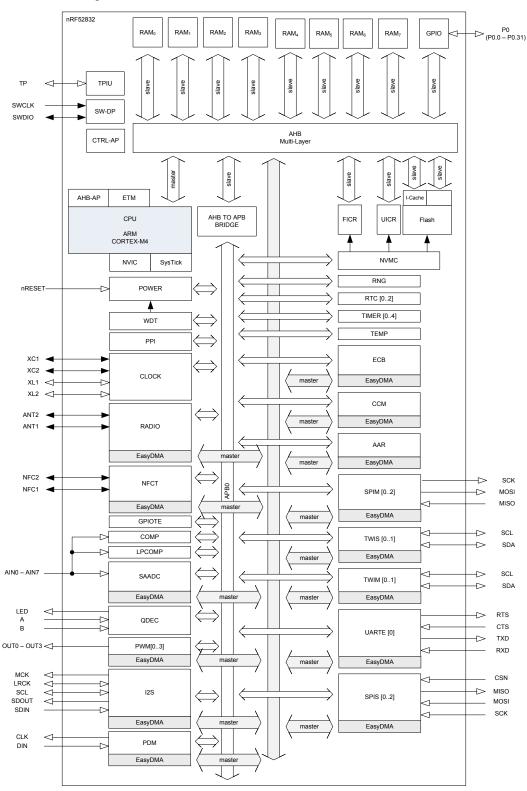


Figure 1: Block diagram



4 Pin assignments

Here we cover the pin assignments for each variant of the chip.

4.1 QFN48 pin assignments

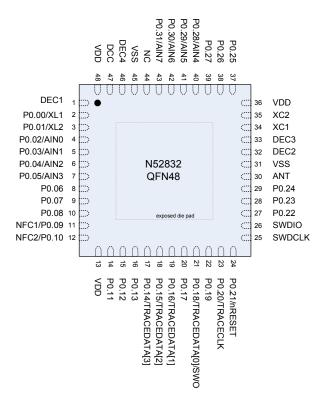


Figure 2: QFN48 pin assignments, top view

Table 3: QFN48 pin assignments

Pin	Name	Туре	Description
Left Side of chip			
1	DEC1	Power	0.9 V regulator digital supply decoupling
2	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
3	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
4	P0.02	Digital I/O	General purpose I/O
	AIN0	Analog input	SAADC/COMP/LPCOMP input
5	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	SAADC/COMP/LPCOMP input
6	P0.04	Digital I/O	General purpose I/O
	AIN2	Analog input	SAADC/COMP/LPCOMP input
7	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC/COMP/LPCOMP input
8	P0.06	Digital I/O	General purpose I/O
9	P0.07	Digital I/O	General purpose I/O



		_	
Pin	Name	Туре	Description
10	P0.08	Digital I/O	General purpose I/O
11	NFC1	NFC input	NFC antenna connection
	P0.09	Digital I/O	General purpose I/O ¹
12	NFC2	NFC input	NFC antenna connection
	P0.10	Digital I/O	General purpose I/O ¹
Bottom side of chip			
13	VDD	Power	Power supply
14	P0.11	Digital I/O	General purpose I/O
15	P0.12	Digital I/O	General purpose I/O
16	P0.13	Digital I/O	General purpose I/O
17	P0.14	Digital I/O	General purpose I/O
	TRACEDATA[3]		Trace port output
18	P0.15	Digital I/O	General purpose I/O
	TRACEDATA[2]		Trace port output
19	P0.16	Digital I/O	General purpose I/O
19		Digital I/O	• • •
	TRACEDATA[1]		Trace port output
20	P0.17	Digital I/O	General purpose I/O
21	P0.18	Digital I/O	General purpose I/O
	TRACEDATA[0] / SWO		Single wire output
			Trace port output
22	P0.19	Digital I/O	General purpose I/O
23	P0.20	Digital I/O	General purpose I/O
		5 ,	
24	TRACECLK P0.21	Digital I/O	Trace port clock output
24	PU.21	Digital I/O	General purpose I/O
	nRESET		Configurable as pin reset
Right Side of chip			
25	SWDCLK	Digital input	Serial wire debug clock input for debug
		21.11.12	and programming
26	SWDIO	Digital I/O	Serial wire debug I/O for debug and
27	DO 22	Digital I/O	programming General purpose I/O ²
28	P0.22 P0.23	Digital I/O	General purpose I/O ²
29	P0.24	Digital I/O Digital I/O	General purpose I/O ²
30	ANT	RF	Single-ended radio antenna connection
31	VSS	Power	Ground (Radio supply)
32	DEC2	Power	1.3 V regulator supply decoupling (Radio
32	DECE	1 ower	supply)
33	DEC3	Power	Power supply decoupling
34	XC1	Analog input	Connection for 32 MHz crystal
35	XC2	Analog input	Connection for 32 MHz crystal
36	VDD	Power	Power supply
Top side of chip			
37	P0.25	Digital I/O	General purpose I/O ²
38	P0.26	Digital I/O	General purpose I/O ²
39	P0.27	Digital I/O	General purpose I/O ²
40	P0.28	Digital I/O	General purpose I/O ²
	AIN4	Analog input	SAADC/COMP/LPCOMP input
41	P0.29	Digital I/O	General purpose I/O ²
		-	
42	AIN5	Analog input	SAADC/COMP/LPCOMP input
42	P0.30	Digital I/O	General purpose I/O ²
	AIN6	Analog input	SAADC/COMP/LPCOMP input
43	P0.31	Digital I/O	General purpose I/O pin ²
	AIN7	Analog input	SAADC/COMP/LPCOMP input
	••	0	-,,pac



Pin	Name	Туре	Description
44	NC		No connect
			Leave unconnected
45	VSS	Power	Ground
46	DEC4	Power	1.3 V regulator supply decoupling
			Input from DC/DC regulator
			Output from 1.3 V LDO
47	DCC	Power	DC/DC regulator output
48	VDD	Power	Power supply
Bottom of chip			
Die pad	VSS	Power	Ground pad
			Exposed die pad must be connected
			to ground (VSS) for proper device
			operation.

4.2 WLCSP ball assignments

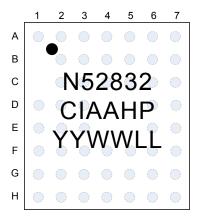


Figure 3: WLCSP ball assignments, top view

Table 4: WLCSP ball assignments

Ball	Name		Description
A1	XC2	Analog input	Connection for 32 MHz crystal
A2	DEC2	Power	1.3 V regulator supply decoupling (Radio
			supply)
A3	P0.28	Digital I/O	General purpose I/O ³
	AIN4	Analog input	SAADC/COMP/LPCOMP input
A4	P0.29	Digital I/O	General purpose I/O ³
	AIN5	Analog input	SAADC/COMP/LPCOMP input
A5	P0.30	Digital I/O	General purpose I/O ³
	AIN6	Analog input	SAADC/COMP/LPCOMP input
A6	DEC4	Power	1.3 V regulator supply decoupling
			Input from DC/DC converter. Output
			from 1.3 V LDO
A7	VDD	Power	Power supply
B2	XC1	Analog input	Connection for 32 MHz crystal
В3	P0.25	Digital I/O	General purpose I/O ³

See *GPIO located near the radio* on page 17 for more information.

See *NFC antenna pins* on page 17 for more information.



Ball	Name		Description
B4	P0.27	Digital I/O	General purpose I/O ³
B5	P0.31	Digital I/O	General purpose I/O ³
	AINIZ	_	
B6	AIN7 DCC	Analog input Power	SAADC/COMP/LPCOMP input DC/DC converter output
B7	DEC1	Power	0.9 V regulator digital supply decoupling
C2	DEC3	Power	Power supply decoupling
C3	NC NC	N/A	Not connected
C4	VSS	Power	Ground
C5	VSS	Power	Ground
C6	P0.02	Digital I/O	General purpose I/O
	AINO	Analog input	SAADC/COMP/LPCOMP input
C7	P0.01	Digital I/O	General purpose I/O
	XL2	Analog input	Connection for 32.768 kHz crystal (LFXO)
D1	ANT	RF	Single-ended radio antenna connection
D2	VSS_PA	Power	Ground (Radio supply)
D3	P0.26	Digital I/O	General purpose I/O ³
D6	P0.03	Digital I/O	General purpose I/O
	AIN1	Analog input	SAADC/COMP/LPCOMP input
D7	P0.00	Digital I/O	General purpose I/O
	XL1	Analog input	Connection for 32.768 kHz crystal (LFXO)
E1	P0.24	Digital I/O	General purpose I/O ³
E2	P0.23	Digital I/O	General purpose I/O ³
E3	VSS	Power	Ground
E6	P0.04	Digital I/O	General purpose I/O
	41912		
F2	AIN2	Analog input	SAADC/COMP/LPCOMP input
E7	P0.05	Digital I/O	General purpose I/O
	AIN3	Analog input	SAADC/COMP/LPCOMP input
F1	SWDCLK	Digital input	Serial wire debug clock input for debug
			and programming
F2	P0.22	Digital I/O	General purpose I/O ³
F3	P0.19	Digital I/O	General purpose I/O
EΛ		Digital I/O	General purpose I/O
F4	P0.11		
F5	VSS	Power	Ground
F5 F6	VSS P0.07	Digital I/O	General purpose I/O
F5 F6 F7	VSS P0.07 P0.06	Digital I/O Digital I/O	General purpose I/O General purpose I/O
F5 F6	VSS P0.07	Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and
F5 F6 F7 G1	VSS P0.07 P0.06 SWDIO	Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming
F5 F6 F7	VSS P0.07 P0.06	Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and
F5 F6 F7 G1	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK	Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output
F5 F6 F7 G1 G2	PO.07 PO.06 SWDIO PO.20 TRACECLK PO.17	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O
F5 F6 F7 G1 G2 G3 G4	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13	Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O
F5 F6 F7 G1 G2	PO.07 PO.06 SWDIO PO.20 TRACECLK PO.17	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O
F5 F6 F7 G1 G2 G3 G4	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13	Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O
F5 F6 F7 G1 G2 G3 G4	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2	Digital I/O NFC input	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection
F5 F6 F7 G1 G2 G3 G4 G5	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10	Digital I/O NFC input Digital I/O NFC input	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴
F5 F6 F7 G1 G2 G3 G4 G5	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O NFC input Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection
F5 F6 F7 G1 G2 G3 G4 G5	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09	Digital I/O NFC input Digital I/O NFC input Digital I/O NFC input Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O ⁴
F5 F6 F7 G1 G2 G3 G4 G5 G6	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O ⁴ General purpose I/O General purpose I/O General purpose I/O General purpose I/O
F5 F6 F7 G1 G2 G3 G4 G5 G6	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O NFC input Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O General purpose I/O NFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O ⁴ OF Configurable as pin reset
F5 F6 F7 G1 G2 G3 G4 G5 G6	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O OFF antenna connection General purpose I/O NFC antenna connection General purpose I/O General purpose I/O General purpose I/O Configurable as pin reset General purpose I/O
F5 F6 F7 G1 G2 G3 G4 G5 G6 G7 H1	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18 TRACEDATA[0]	Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O OFF antenna connection General purpose I/O NFC antenna connection General purpose I/O OFF antenna connection General purpose I/O Ceneral purpose I/O General purpose I/O General purpose I/O Trace port output
F5 F6 F7 G1 G2 G3 G4 G5 G6 G7 H1	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18	Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O NFC input Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O OFF antenna connection General purpose I/O NFC antenna connection General purpose I/O General purpose I/O General purpose I/O Configurable as pin reset General purpose I/O
F5 F6 F7 G1 G2 G3 G4 G5 G6 G7 H1	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18 TRACEDATA[0]	Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O OFF antenna connection General purpose I/O NFC antenna connection General purpose I/O OFF antenna connection General purpose I/O Ceneral purpose I/O General purpose I/O General purpose I/O Trace port output
F5 F6 F7 G1 G2 G3 G4 G5 G6 G7 H1	VSS P0.07 P0.06 SWDIO P0.20 TRACECLK P0.17 P0.13 NFC2 P0.10 NFC1 P0.09 P0.08 P0.21 nRESET P0.18 TRACEDATA[0] P0.16	Digital I/O NFC input Digital I/O NFC input Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O Digital I/O	General purpose I/O General purpose I/O Serial wire debug I/O for debug and programming General purpose I/O Trace port clock output General purpose I/O MFC antenna connection General purpose I/O ⁴ NFC antenna connection General purpose I/O General purpose I/O Configurable as pin reset General purpose I/O Trace port output General purpose I/O



Ball	Name		Description
	TRACEDATA[2]		Trace port output
H5	P0.14	Digital I/O	General purpose I/O
	TRACEDATA[3]		Trace port output
H6	P0.12	Digital I/O	General purpose I/O
H7	VDD	Power	Power supply

4.3 GPIO usage restrictions

4.3.1 GPIO located near the radio

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the Radio power supply and antenna pins.

Table 5: GPIO recommended usage for QFN48 package on page 17 and Table 6: GPIO recommended usage for WLCSP package on page 17 identify some GPIO that have recommended usage guidelines to maximize radio performance in an application.

Table 5: GPIO recommended usage for QFN48 package

Pin	GPIO	Recommended usage
27	P0.22	Low drive, low frequency I/O only.
28	P0.23	
29	P0.24	
37	P0.25	
38	P0.26	
39	P0.27	
40	P0.28	
41	P0.29	
42	P0.30	
43	P0.31	

Table 6: GPIO recommended usage for WLCSP package

Pin	GPIO	Recommended usage
F2	P0.22	Low drive, low frequency I/O only.
E2	P0.23	
E1	P0.24	
B3	P0.25	
D3	P0.26	
B4	P0.27	
A3	P0.28	
A4	P0.29	
A5	P0.30	
B5	P0.31	

4.3.2 NFC antenna pins

Two physical pins can be configured either as NFC antenna pins (factory default), or as GPIOs, as shown below.

Table 7: GPIO pins used by NFC

NFC pad name	GPIO
NFC1	P0.09
NFC2	P0.10

When configured as NFC antenna pins, the GPIOs on those pins will automatically be set to DISABLE state and a protection circuit will be enabled preventing the chip from being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2 V.

³ See *GPIO located near the radio* on page 17 for more information.

⁴ See *NFC antenna pins* on page 17 for more information.



For information on how to configure these pins as normal GPIOs, see *NFCT* — *Near field communication tag* on page 416 and *UICR* — *User information configuration registers* on page 54. Note that the device will not be protected against strong NFC field damage if the pins are configured as GPIO and an NFC antenna is connected to the device. The pins will always be configured as NFC pins during power-on reset until the configuration is set according to the UICR register.

These two pins will have some limitations when configured as GPIO. The pin capacitance will be higher on these pins, and there is some current leakage between the two pins if they are driven to different logical values. To avoid leakage between the pins when configured as GPIO, these GPIOs should always be at the same logical value whenever entering one of the device power saving modes. See *Electrical specification*.



5 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Table 8: Absolute maximum ratings

	Min.	Max.	Unit
Supply voltages			
VDD	-0.3	+3.9	V
VSS		0	V
I/O pin voltage			
V _{I/O} , VDD ≤3.6 V	-0.3	VDD + 0.3 V	V
V _{I/O} , VDD >3.6 V	-0.3	3.9 V	V
NFC antenna pin current			
I _{NFC1/2}		80	mA
Radio			
RF input level		10	dBm
Environmental QFN48, 6×6 mm package			
Storage temperature	-40	+125	°C
MSL (moisture sensitivity level)		2	
ESD HBM (human body model)		4	kV
ESD CDM (charged device model)		1000	V
Environmental WLCSP, 3.0×3.2 mm package			
Storage temperature	-40	+125	°C
MSL		1	
ESD HBM		2	kV
ESD CDM		500	V
Flash memory			
Endurance	10 000		Write/erase cycles
Retention	10 years at 40°C		





6 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Table 9: Recommended operating conditions

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Supply voltage, independent of DCDC enable		1.7	3.0	3.6	V
t_{R_VDD}	Supply rise time (0 V to 1.7 V)				60	ms
TĀ	Operating temperature		-40	25	85	°C

Important: The on-chip power-on reset circuitry may not function properly for rise times longer than the specified maximum.

6.1 WLCSP light sensitivity

All WLCSP package variants are sensitive to visible and close-range infrared light. This means that a final product design must shield the chip properly, either by final product encapsulation or by shielding/coating of the WLCSP device.



7 CPU

The ARM® Cortex®-M4 processor with floating-point unit (FPU) has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- · Hardware divide
- 8 and 16-bit single instruction multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex processor series is implemented and available for the M4 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the Nested Vectored Interrupt Controller (NVIC).

Executing code from flash will have a wait state penalty on the nRF52 Series. An instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see *Cache* on page 30. The section *Electrical specification* on page 21 shows CPU performance parameters including wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

7.1 Floating point interrupt

The floating point unit (FPU) may generate exceptions when used due to e.g. overflow or underflow. These exceptions will trigger the FPU interrupt (see *Instantiation* on page 24). To clear the IRQ line when an exception has occurred, the relevant exception bit within the FPSCR register needs to be cleared. For more information about the FPSCR or other FPU registers, see *Cortex-M4 Devices Generic User Guide*.

7.2 Electrical specification

7.2.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark[™] benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Тур.	Max.	Units
W_{FLASH}	CPU wait states, running from flash, cache disabled	0		2	
$W_{FLASHCACHE}$	CPU wait states, running from flash, cache enabled	0		3	
W_{RAM}	CPU wait states, running from RAM			0	
I _{DDFLASHCACHE}	CPU current, running from flash, cache enabled, LDO		7.4		mA
I _{DDFLASHCACHEDCDC}	CPU current, running from flash, cache enabled, DCDC 3V		3.7		mA
I _{DDFLASH}	CPU current, running from flash, cache disabled, LDO		8.0		mA
I _{DDFLASHDCDC}	CPU current, running from flash, cache disabled, DCDC 3V		3.9		mA
I _{DDRAM}	CPU current, running from RAM, LDO		6.7		mA
I _{DDRAMDCDC}	CPU current, running from RAM, DCDC 3V		3.3		mA
I _{DDFLASH/MHz}	CPU efficiency, running from flash, cache enabled, LDO		125		μΑ/
					MHz
I _{DDFLASHDCDC/MHz}	CPU efficiency, running from flash, cache enabled, DCDC 3V		58		μΑ/
					MHz



Symbol	Description	Min.	Тур.	Max.	Units
CM_{FLASH}	CoreMark ⁵ , running from flash, cache enabled		215		CoreN
$CM_{FLASH/MHz}$	CoreMark per MHz, running from flash, cache enabled		3.36		CoreN
					MHz
CM _{FLASH/mA}	CoreMark per mA, running from flash, cache enabled, DCDC 3V		58		CoreN
					mA

7.3 CPU and support module configuration

The ARM® Cortex®-M4 processor has a number of CPU options and support modules implemented on the device.

Option / Module	Description	Implemented
Core options		
NVIC	Nested Vector Interrupt Controller	37 vectors
PRIORITIES	Priority bits	3
WIC	Wakeup Interrupt Controller	NO
Endianness	Memory system endianness	Little endian
Bit Banding	Bit banded memory	NO
DWT	Data Watchpoint and Trace	YES
SysTick	System tick timer	YES
Modules		
MPU	Memory protection unit	YES
FPU	Floating point unit	YES
DAP	Debug Access Port	YES
ETM	Embedded Trace Macrocell	YES
ITM	Instrumentation Trace Macrocell	YES
TPIU	Trace Port Interface Unit	YES
ETB	Embedded Trace Buffer	NO
FPB	Flash Patch and Breakpoint Unit	YES
HTM	AHB Trace Macrocell	NO

⁵ Using IAR v6.50.1.4452 with flags --endian=little --cpu=Cortex-M4 -e --fpu=VFPv4_sp -Ohs --no_size_constraints



8 Memory

The nRF52832 contains flash and RAM that can be used for code and data storage.

The amount of RAM and flash will vary depending on variant, see *Table 10: Memory variants* on page 23.

Table 10: Memory variants

Device name	RAM	Flash	Comments
nRF52832-QFAA	64 kB	512 kB	
nRF52832-QFAB	32 kB	256 kB	
nRF52832-CIAA	64 kB	512 kB	

The CPU and the EasyDMA can access memory via the AHB multilayer interconnect. The CPU is also able to access peripherals via the AHB multilayer interconnect, as illustrated in *Figure 4: Memory layout* on page 23.

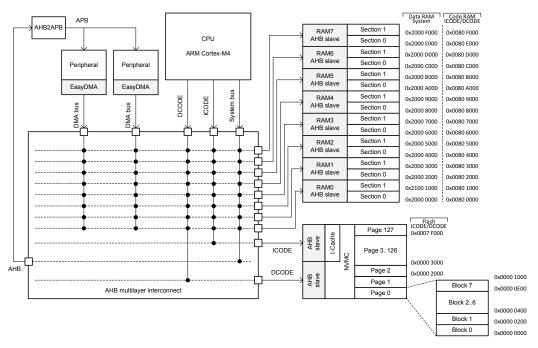


Figure 4: Memory layout

See *AHB multilayer* on page 26 and *EasyDMA* on page 27 for more information about the AHB multilayer interconnect and the EasyDMA.

The same physical RAM is mapped to both the Data RAM region and the Code RAM region. It is up to the application to partition the RAM within these regions so that one does not corrupt the other.

8.1 RAM - Random access memory

The RAM interface is divided into multiple RAM AHB slaves.

Each RAM AHB slave is connected to two 4-kilobyte RAM sections, see Section 0 and Section 1 in *Figure 4: Memory layout* on page 23.

Each of the RAM sections have separate power control for System ON and System OFF mode operation, which is configured via RAM register (see the *POWER — Power supply* on page 78).



8.2 Flash - Non-volatile memory

The Flash can be read an unlimited number of times by the CPU, but it has restrictions on the number of times it can be written and erased and also on how it can be written.

Writing to Flash is managed by the Non-volatile memory controller (NVMC), see *NVMC — Non-volatile memory controller* on page 29.

The Flash is divided into multiple pages that can be accessed by the CPU via both the ICODE and DCODE buses as shown in, *Figure 4: Memory layout* on page 23. Each page is divided into 8 blocks.

8.3 Memory map

The complete memory map is shown in *Figure 5: Memory map* on page 24. As described in *Memory* on page 23, Code RAM and the Data RAM are the same physical RAM.

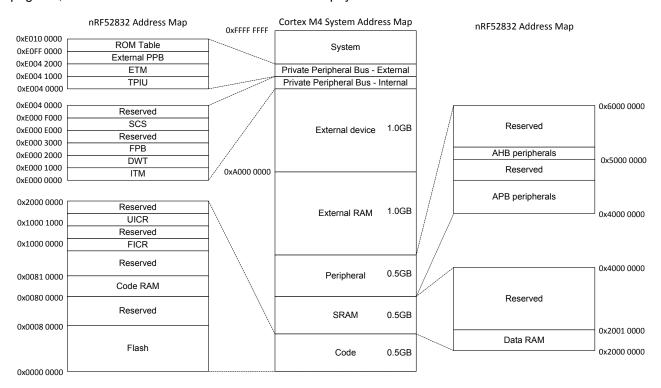


Figure 5: Memory map

8.4 Instantiation

Table 11: Instantiation table

ID	Base Address	Peripheral	Instance	Description	
0	0x40000000	CLOCK	CLOCK	Clock control	
0	0x40000000	POWER	POWER	Power control	
0	0x40000000	BPROT	BPROT	Block Protect	
1	0x40001000	RADIO	RADIO	2.4 GHz radio	
2	0x40002000	UARTE	UARTE0	Universal Asynchronous Receiver/Transmitter with EasyDM	IA
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/Transmitter	Deprecated
3	0x40003000	SPIM	SPIM0	SPI master 0	
3	0x40003000	SPIS	SPIS0	SPI slave 0	
3	0x40003000	TWIM	TWIM0	Two-wire interface master 0	
3	0x40003000	TWI	TWI0	Two-wire interface master 0	Deprecated
3	0x40003000	SPI	SPI0	SPI master 0	Deprecated



ID	Base Address	Peripheral	Instance	Description	
3	0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
4	0x40004000	SPIM	SPIM1	SPI master 1	
1	0x40004000	TWI	TWI1	Two-wire interface master 1	Deprecated
1	0x40004000	SPIS	SPIS1	SPI slave 1	
4	0x40004000	TWIS	TWIS1	Two-wire interface slave 1	
4	0x40004000	TWIM	TWIM1	Two-wire interface master 1	
4	0x40004000	SPI	SPI1	SPI master 1	Deprecated
5	0x40005000	NFCT	NFCT	Near Field Communication Tag	
6	0x40006000	GPIOTE	GPIOTE	GPIO Tasks and Events	
7	0x40007000	SAADC	SAADC	Analog to digital converter	
8	0x40008000	TIMER	TIMERO	Timer 0	
9	0x40009000	TIMER	TIMER1	Timer 1	
10	0x4000A000	TIMER	TIMER2	Timer 2	
11	0x4000B000	RTC	RTC0	Real-time counter 0	
12	0x4000C000	TEMP	TEMP	Temperature sensor	
13	0x4000D000	RNG	RNG	Random number generator	
14	0x4000E000	ECB	ECB	AES Electronic Code Book (ECB) mode block encryption	
15	0x4000F000	CCM	CCM	AES CCM Mode Encryption	
15	0x4000F000	AAR	AAR	Acelerated Address Resolver	
16	0x4001000	WDT	WDT	Watchdog timer	
17	0x40010000	RTC	RTC1	Real-time counter 1	
18	0x40011000 0x40012000	QDEC	QDEC	Quadrature decoder	
19			-	4	
	0x40013000	LPCOMP	LPCOMP	Low power comparator	
19	0x40013000	COMP	COMP	General purpose comparator	
20	0x40014000	SWI	SWI0	Software interrupt 0	
20	0x40014000	EGU	EGU0	Event Generator Unit 0	
21	0x40015000	EGU	EGU1	Event Generator Unit 1	
21	0x40015000	SWI	SWI1	Software interrupt 1	
22	0x40016000	SWI	SWI2	Software interrupt 2	
22	0x40016000	EGU	EGU2	Event Generator Unit 2	
23	0x40017000	SWI	SWI3	Software interrupt 3	
23	0x40017000	EGU	EGU3	Event Generator Unit 3	
24	0x40018000	EGU	EGU4	Event Generator Unit 4	
24	0x40018000	SWI	SWI4	Software interrupt 4	
25	0x40019000	SWI	SWI5	Software interrupt 5	
25	0x40019000	EGU	EGU5	Event Generator Unit 5	
26	0x4001A000	TIMER	TIMER3	Timer 3	
27	0x4001B000	TIMER	TIMER4	Timer 4	
28	0x4001C000	PWM	PWM0	Pulse Width Modulation Unit 0	
29	0x4001D000	PDM	PDM	Pulse Density Modulation (Digital Microphone Interface)	
30	0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller	
31	0x4001F000	PPI	PPI	Programmable Peripheral Interconnect	
32	0x40020000	MWU	MWU	Memory Watch Unit	
33	0x40021000	PWM	PWM1	Pulse Width Modulation Unit 1	
34	0x40022000	PWM	PWM2	Pulse Width Modulation Unit 2	
35	0x40023000	SPI	SPI2	SPI master 2	Deprecated
35	0x40023000	SPIS	SPIS2	SPI slave 2	
35	0x40023000	SPIM	SPIM2	SPI master 2	
36	0x40024000	RTC	RTC2	Real-time counter 2	
37	0x40025000	I2S	I2S	Inter-IC Sound Interface	
38	0x40025000	FPU	FPU	FPU interrupt	
		GPIO	GPIO	General purpose input and output	Deprecated
		JI 10	J1 10	General purpose input and output	pepretate:
)	0x50000000		PΩ	General nurnose input and output	
0 0 N/A	0x50000000 0x50000000 0x10000000	GPIO FICR	PO FICR	General purpose input and output Factory Information Configuration	



9 AHB multilayer

The CPU and all of the EasyDMAs are AHB bus masters on the AHB multilayer, while the RAM and various other modules are AHB slaves.

See *Block diagram* on page 12 for an overview of which peripherals implement EasyDMA.

The CPU has exclusive access to all AHB slaves except for the RAM that can also be accessed by the EasyDMA.

Access rights to each of the RAM AHB slaves are resolved using the priority of the different bus masters in the system

See AHB multilayer priorities on page 26 for information about the priority of the different AHB bus masters in the system. It is possible for two or more bus masters to have the same priority in cases where it is guaranteed by design that the related masters will never be able to access the same slave at the same time.

9.1 AHB multilayer priorities

Each master connected to the AHB multilayer is assigned a priority.

Table 12: AHB bus masters

Bus master name	Priority	Description
CPU	Highest priority	
SPIS1		Applies to SPIM1, SPIS1, TWIM1, TWIS1
RADIO		
CCM/ECB/AAR		
SAADC		
UARTE		
SERIALO SERIALO		Applies to SPIMO, SPISO, TWIMO, TWISO
SERIAL2		Applies to SPIM2, SPIS2
NFCT		
12S		I2S
PDM		PDM
PWM	Lowest priority	Applies to PWM0, PWM1, PWM2



10 EasyDMA

EasyDMA is an easy-to-use direct memory access module that some peripherals implement to gain direct access to Data RAM.

The EasyDMA is an AHB bus master similar to the CPU and it is connected to the AHB multilayer interconnect for direct access to the Data RAM. The EasyDMA is not able to access the Flash.

A peripheral can implement multiple EasyDMA instances, for example to provide a dedicated channel for reading data from RAM into the peripheral at the same time as a second channel is dedicated for writing data to the RAM from the peripheral. This concept is illustrated in *Figure 6: EasyDMA example* on page 27

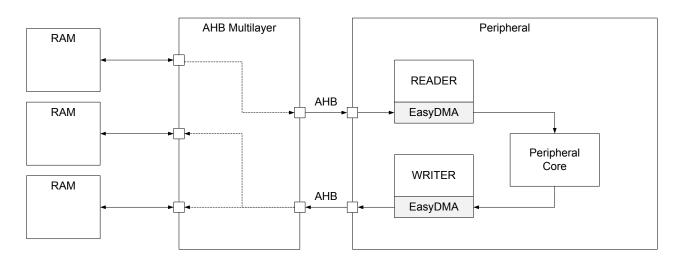


Figure 6: EasyDMA example

An EasyDMA channel is usually exposed to the user in the form illustrated below, but some variations may occur:

```
READERBUFFER_SIZE 5
WRITERBUFFER_SIZE 6

uint8_t readerBuffer[READERBUFFER_SIZE] __at__ 0x20000000;
uint8_t writerBuffer[WRITERBUFFER_SIZE] __at__ 0x20000005;

// Configuring the READER channel
MYPERIPHERAL->READER.MAXCNT = READERBUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &readerBuffer;

// Configure the WRITER channel
MYPERIPHERAL->WRITER.MAXCNT = WRITEERBUFFER_SIZE;
MYPERIPHERAL->WRITER.PTR = &writerBuffer;
```

This example shows a peripheral called MYPERIPHERAL that implements two EasyDMA channels, one for reading, called READER, and one for writing, called WRITER. When the peripheral is started, it is here assumed that the peripheral will read 5 bytes from the readerBuffer located in RAM at address 0x20000000, process the data and then write no more than 6 bytes back to the writerBuffer located in RAM at address 0x20000005. The memory layout of these buffers is illustrated in *Figure 7: EasyDMA memory layout* on page 28.



0x20000000	readerBuffer[0]	readerBuffer[1]	readerBuffer[2]	readerBuffer[3]
0x20000004	readerBuffer[4]	writerBuffer[0]	writerBuffer[1]	writerBuffer[2]
0x20000008	writerBuffer[3]	writerBuffer[4]	writerBuffer[5]	

Figure 7: EasyDMA memory layout

The EasyDMA channel's MAXCNT register cannot be specified larger than the actual size of the buffer. If, for example, the WRITER.MAXCNT register is specified larger than the size of the writerBuffer, the WRITER EasyDMA channel may overflow the writerBuffer.

After the peripheral has completed the EasyDMA transfer, the CPU can read the EasyDMA channel's AMOUNT register to see how many bytes that were transferred, e.g. it is possible for the CPU to read the MYPERIPHERAL->WRITER.AMOUNT register to see how many bytes the WRITER wrote to RAM.

10.1 EasyDMA array list

The EasyDMA is able to operate in a mode called array list.

The EasyDMA array list can be represented by the data structure ArrayList_type illustrated in the code example below.

This data structure includes only a buffer with size equal to READER.MAXCNT. EasyDMA will use the READER.MAXCNT register to determine when the buffer is full.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
   uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3];

READER.MAXCNT = BUFFER_SIZE;
READER.PTR = &ReaderList;
```

READER.PTR = &ReaderList

Ţ				
0x20000000 : ReaderList[0]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000004 : ReaderList[1]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000008 : ReaderList[2]	buffer[0]	buffer[1]	buffer[2]	buffer[3]

Figure 8: EasyDMA array list



11 NVMC — Non-volatile memory controller

The Non-volatile memory controller (NVMC) is used for writing and erasing the internal Flash memory and the UICR.

Before a write can be performed, the NVMC must be enabled for writing in CONFIG.WEN. Similarly, before an erase can be performed, the NVMC must be enabled for erasing in CONFIG.EEN, see *CONFIG* on page 31. The user must make sure that writing and erasing are not enabled at the same time. Failing to do so may result in unpredictable behavior.

11.1 Writing to Flash

When writing is enabled, the Flash is written by writing a full 32-bit word to a word-aligned address in the Flash

The NVMC is only able to write '0' to bits in the Flash that are erased, that is, set to '1'. It cannot write back a bit to '1'.

As illustrated in *Memory* on page 23, the Flash is divided into multiple pages that are further divided into multiple blocks. The same block in the Flash can only be written n_{WRITE} number of times before an erase must be performed using *ERASEPAGE* or *ERASEALL*. See the memory size and organization in *Memory* on page 23 for block size.

Only full 32-bit words can be written to Flash using the NVMC interface. To write less than 32 bits to Flash, write the data as a word, and set all the bits that should remain unchanged in the word to '1'. Note that the restriction about the number of writes (see above) still applies in this case.

The time it takes to write a word to the Flash is specified by t_{WRITE} . The CPU is halted while the NVMC is writing to the Flash.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a hard fault.

11.2 Erasing a page in Flash

When erase is enabled, the Flash can be erased page by page using the ERASEPAGE register.

After erasing a Flash page, all bits in the page are set to '1'. The time it takes to erase a page is specified by $t_{ERASEPAGE}$. The CPU is halted while the NVMC performs the erase operation.

11.3 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as Flash. After UICR has been written, the new UICR configuration will only take effect after a reset.

UICR can only be written n_{WRITE} number of times before an erase must be performed using ERASEUICR or ERASEALL.

The time it takes to write a word to the UICR is specified by t_{WRITE} . The CPU is halted while the NVMC is writing to the UICR.

11.4 Erasing user information configuration registers (UICR)

When erase is enabled, UICR can be erased using the ERASEUICR register.

After erasing UICR all bits in UICR are set to '1'. The time it takes to erase UICR is specified by $t_{ERASEPAGE}$. The CPU is halted while the NVMC performs the erase operation.



11.5 Erase all

When erase is enabled, the whole Flash and UICR can be erased in one operation by using the ERASEALL register. ERASEALL will not erase the factory information configuration registers (FICR).

The time it takes to perform an ERASEALL command is specified by $t_{ERASEALL}$ The CPU is halted while the NVMC performs the erase operation.

11.6 Cache

An instruction cache (I-Cache) can be enabled for the ICODE bus in the NVMC.

See the Memory map in *Memory map* on page 24 for the location of Flash.

A cache hit is an instruction fetch from the cache, and it has a 0 wait-state delay. The number of wait-states for a cache miss, where the instruction is not available in the cache and needs to be fetched from Flash, depends on the processor frequency and is shown in *CPU* on page 21

Enabling the cache can increase CPU performance and reduce power consumption by reducing the number of wait cycles and the number of flash accesses. This will depend on the cache hit rate. Cache will use some current when enabled. If the reduction in average current due to reduced flash accesses is larger than the cache power requirement, the average current to execute the program code will reduce.

When disabled, the cache does not use current and does not retain its content.

It is possible to enable cache profiling to analyze the performance of the cache for your program using the *ICACHECNF* register. When profiling is enabled, the *IHIT* and *IMISS* registers are incremented for every instruction cache hit or miss respectively. The hit and miss profiling registers do not wrap around after reaching the maximum value. If the maximum value is reached, consider profiling for a shorter duration to get correct numbers.

11.7 Registers

Table 13: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller	

Table 14: Register Overview

Register	Offset	Description	
READY	0x400	Ready flag	
CONFIG	0x504	Configuration register	
ERASEPAGE	0x508	Register for erasing a page in Code area	
ERASEPCR1	0x508	Register for erasing a page in Code area. Equivalent to ERASEPAGE.	Deprecated
ERASEALL	0x50C	Register for erasing all non-volatile user memory	
ERASEPCR0	0x510	Register for erasing a page in Code area. Equivalent to ERASEPAGE.	Deprecated
ERASEUICR	0x514	Register for erasing User Information Configuration Registers	
ICACHECNF	0x540	I-Code cache configuration register.	
IHIT	0x548	I-Code cache hit counter.	
IMISS	0x54C	I-Code cache miss counter.	

11.7.1 READY

Address offset: 0x400

Ready flag



Bit	Bit number					9 28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	.1 1	0 9	8	7	6	5	4	3	2	1 0
Id																																А
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe						De	scri	ipti	on																		
Α	R	READY									N۷	'MC	C is	read	dy c	r bı	ısy															
			Busy	0					N۷	'MC	C is	bus	y (o	n-g	oing	g w	rite	or	era	se c	per	atio	n)									
			Ready	1					NVMC is ready																							

11.7.2 **CONFIG**

Address offset: 0x504 Configuration register

Bit r	numbe		31	30	29	28	27	26	25	24	23	22	21 2	0 :	L9 1	18 2	17 :	16 :	15 :	14	13	12 :	11 1	.0 9	9	8	7	6	5	4	3 2	2 1	0	
Id	Id																															A	A A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (0	0	0	0	0) (0 0
Id	RW	Field	Value Id	Va	lue							Des	scrip	otio	n																			
Α	RW	WEN										Pro	gra	m m	en	nory	ac	ces	s m	od	e. I	is	stro	ngl	y re	coı	mm	en	ded					
										to only activate erase and write modes when they are actively																								
											used. Enabling write or erase will invalidate											the	e ca	che	e ar	nd k	ee	р						
												it ir	nval	idat	ed.																			
			Ren	0								Rea	ad o	nly	acc	ess																		
			Wen	1								Wr	ite E	Enab	oled	ł																		
			Een	2						Erase enabled																								

11.7.3 ERASEPAGE

Address offset: 0x508

Register for erasing a page in Code area

Bit number 31 30 29 28 27 26									5 25	5 24	23	22 2	21 2	0 1	.9 18	3 17	16	15	14 1	13 1	2 11	10	9	8	7	6 5	5 4	3	2	1 0	
Id A A A A A A A A									Α	Α	Α	A A	A A	Д А	Α.	Α	Α	Α	A A	A A	Α	Α	A	Δ,	Α Α	4 Α	A	Α	A A		
Res	et 0x0	et 0x000000000 0 0 0 0 0 0 0 0 0 0									0	0	0 () (0 0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0 0	
Id	RW	Field	Value Id	Va	lue						De	scrip	ptior	1																	
Α	RW	ERASEPAGE			Register for starting erase of a page in Code area																										
					The value is the address to the page to be erased. (Addresses of																										
											firs	st wo	ord i	n pa	age)	. No	te t	hat	cod	e er	ase	nas i	to b	e en	abl	ed l	by				
				CONFIG.EEN before the page can be erased. Attempts to erase																											
											pag	ges t	that	are	out	side	the	coo	de a	rea	may	res	ult i	n un	des	iral	ble				
											bel	havi	our,	e.g	the	wr	ong	pag	e m	nay b	e e	ase	d.								

11.7.4 ERASEPCR1 (Deprecated)

Address offset: 0x508

Register for erasing a page in Code area. Equivalent to ERASEPAGE.

Bit	numb	er		31	1 30	29	9 28	3 2	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	.0 9	9 ;	8 7	6	5	4	3	2	1	0
Id				Α	Α	Д	A	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	A /	۱ ۸	4 <i>A</i>	. 4	. A	Α	Α	Α	Α.	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0) (0 0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																			
Α	RW	ERASEPCR1										Re	gist	er f	or e	eras	ing	ар	age	in	Coc	le a	rea	. Eq	uiva	aler	nt to							

ERASEPAGE.

11.7.5 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory



Bit	numbe	er		31	L 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																				
Α	RW	ERASEALL										Era	ise a	all n	on-	-vol	atil	e m	em	ory	in	lud	ling	UIC	CR r	egi	iste	rs.	Not	e					
												tha	it co	ode	era	ise l	has	to	be (ena	ble	d by	y CC	ONF	IG.	EEN	N be	efo	re t	he					
												UIC	CR c	an l	be e	eras	sed.																		
			NoOperation	0								No	оре	erat	tion	1																			
			Erase	1								Sta	rt c	hip	era	ise																			

11.7.6 ERASEPCR0 (Deprecated)

Address offset: 0x510

Register for erasing a page in Code area. Equivalent to ERASEPAGE.

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 :	20 1	9 1	.8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	4 /	ДД	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	ı
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (į
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			l
Α	RW	ERASEPCR0										Reg	giste	r fo	or st	arti	ng e	ras	e of	ар	age	in (Cod	e a	rea.	. Eq	uiv	alei	nt t	О				
												ER/	ASEF	PAG	iΕ.																			

11.7.7 ERASEUICR

Address offset: 0x514

Register for erasing User Information Configuration Registers

Bit r	iumbe	r		31	1 30	29	28	3 27	7 20	6 25	5 24	4 2	3 2	2 2	21 2	20 2	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																				Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0) () () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							D	esc	rip	tio	n																				
Α	RW	ERASEUICR										R	egi	ste	r st	art	ing	era	ase	of	all	Use	r Ir	for	ma	tior	Co	nfig	gura	atio	n					
												R	egi	ste	rs.	Not	te t	ha	t co	ode	era	ise	has	to	be	ena	ble	d by	/							
												C	ON	FIG	i.EE	Νŀ	oef	ore	th	e U	ICF	ca	n b	e er	ase	ed.										
			NoOperation	0								N	0 0	pei	rati	on																				
			Erase	1								S	tart	t er	ase	of	UI	CR																		

11.7.8 ICACHECNF

Address offset: 0x540

I-Code cache configuration register.

Bit	numbe	r		31	1 30	29	28	3 27	7 2	6 2	5 2	24 2	23 2	22 :	21	20	19	18	17	7 16	5 15	5 14	1 13	3 12	2 11	. 10	9	8	7	6	5	4	3	2 :	1 0
Id																												В							Α
Res	et 0x0	0000000		0	0	0	0	0	(0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	alue								Des	crip	otic	n																			
Α	RW	CACHEEN										(Cac	he	ena	ble	9																		
			Disabled	0								[Disa	ble	e ca	che	e. li	nva	lid	ate	s al	l ca	che	en	trie	s.									
			Enabled	1								E	Ena	ble	cad	che	!																		
В	RW	CACHEPROFEN										(Cac	he	pro	filir	ng (ena	able	9															
			Disabled	0								[Disa	ble	e ca	che	e pi	rofi	ilin	g															
			Enabled	1								E	Ena	ble	cad	che	pr	ofi	ling	3															

11.7.9 IHIT

Address offset: 0x548 I-Code cache hit counter.



Bit r	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 :	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																			
Α	RW	HITS										Nur	nbe	er o	f ca	iche	hit	ts																

11.7.10 IMISS

Address offset: 0x54C

I-Code cache miss counter.

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α	RW	MISSES										Nu	mb	er c	of c	ach	e m	isse	es																7

11.8 Electrical specification

11.8.1 Flash programming

Symbol	Description	Min.	Тур.	Max.	Units
n _{WRITE,BLOCK}	Amount of writes allowed in a block between erase			181	
t _{WRITE}	Time to write one word	67.5		338	μs
t _{ERASEPAGE}	Time to erase one page	2.05		89.7	ms
teraseall	Time to erase all flash	6.72		295.3	ms

11.8.2 Cache size

Symbol	Description	Min.	Тур.	Max.	Units
Size _{ICODE}	I-Code cache size		2048		Bytes



12 BPROT — Block protection

The mechanism for protecting non-volatile memory can be used to prevent application code from erasing or writing to protected blocks.

Non-volatile memory can be protected from erases and writes depending on the settings in the CONFIG registers. One bit in a CONFIG register represents one protected block of 4 kB. There are four CONFIG registers of 32 bits, which means there are 128 protectable blocks in total.

Important: If an erase or write to a protected block is detected, the CPU will hard fault. If an ERASEALL operation is attempted from the CPU while any block is protected, it will be blocked and the CPU will hard fault.

On reset, all the protection bits are cleared. To ensure safe operation, the first task after reset must be to set the protection bits. The only way of clearing protection bits is by resetting the device from any reset source.

The protection mechanism is turned off when in debug interface mode (a debugger is connected) and the DISABLEINDEBUG register is set to disable. For more information, see *Debug and trace* on page 72.

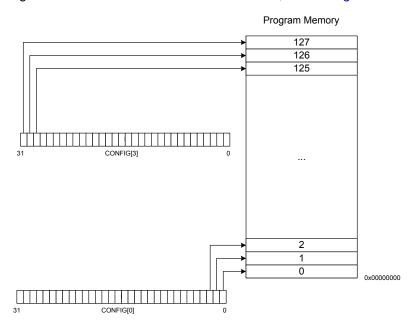


Figure 9: Protected regions of program memory

12.1 Registers

Table 15: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40000000	BPROT	BPROT	Block Protect		

Table 16: Register Overview

Register	Offset	Description	
CONFIG0	0x600	Block protect configuration register 0	
CONFIG1	0x604	Block protect configuration register 1	
DISABLEINDEBUG	0x608	Disable protection mechanism in debug interface mode	
	0x60C		Reserved
CONFIG2	0x610	Block protect configuration register 2	
CONFIG3	0x614	Block protect configuration register 3	



12.1.1 CONFIG0

Address offset: 0x600

Block protect configuration register 0

	numb	er						23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	at 0(0000000						X W V U T S R Q P O N M L K J I H G F E D C B A 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	0 0 Value	0 0	U	0 0	Description
A		REGIONO	value lu	Value				Enable protection for region 0. Write '0' has no effect.
^	11.00	REGIONO	Disabled	0				Protection disabled
			Enabled	1				Protection disabled
D	D\A/	REGION1	Ellabled	1				
В	KVV	REGIONI	Disabled	0				Enable protection for region 1. Write '0' has no effect.
			Disabled	0				Protection disabled Protection enable
_	DIA	DECIONA	Enabled	1				
С	KVV	REGION2	Disabled	0				Enable protection for region 2. Write '0' has no effect.
			Disabled	0				Protection disabled
_			Enabled	1				Protection enable
D	RW	REGION3						Enable protection for region 3. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
E	RW	REGION4						Enable protection for region 4. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
F	RW	REGION5						Enable protection for region 5. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
G	RW	REGION6						Enable protection for region 6. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
Н	RW	REGION7						Enable protection for region 7. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
I	RW	REGION8						Enable protection for region 8. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
J	RW	REGION9						Enable protection for region 9. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
K	RW	REGION10						Enable protection for region 10. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
L	RW	REGION11						Enable protection for region 11. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
М	RW	REGION12						Enable protection for region 12. Write '0' has no effect.
•••			Disabled	0				Protection disabled
			Enabled	1				Protection enable
N	D\A/	REGION13	Lilabica	-				Enable protection for region 13. Write '0' has no effect.
IN	11.00	KEGIONIS	Disabled	0				Protection disabled
			Enabled	1				Protection disabled Protection enable
_	DIA	DECIONA A	Ellabled	1				
0	L/ A/A	REGION14	Disabled	0				Enable protection for region 14. Write '0' has no effect.
			Disabled	0				Protection disabled
D	D111	DECIONAT	Enabled	1				Protection enable
Р	RW	REGION15	6: 11.1	0				Enable protection for region 15. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
Q	RW	REGION16						Enable protection for region 16. Write '0' has no effect.
			Disabled	0				Protection disabled



Bit number					29 28	27 2	6 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			f e	d c	b a	a Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A	
Rese	t 0x0	0000000		0 0	0 0	0 (0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Enabled	1				Protection enable
R	RW	REGION17						Enable protection for region 17. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
S	RW	REGION18						Enable protection for region 18. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
T	RW	REGION19						Enable protection for region 19. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
U	RW	REGION20						Enable protection for region 20. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
V	RW	REGION21						Enable protection for region 21. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
W	RW	REGION22						Enable protection for region 22. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
Χ	RW	REGION23						Enable protection for region 23. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
Υ	RW	REGION24						Enable protection for region 24. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
Z	RW	REGION25						Enable protection for region 25. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
а	RW	REGION26						Enable protection for region 26. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable
b	RW	REGION27	5					Enable protection for region 27. Write '0' has no effect.
			Disabled	0				Protection disabled
	DIA	DECIONAL	Enabled	1				Protection enable
С	RW	REGION28	D' III I	•				Enable protection for region 28. Write '0' has no effect.
			Disabled	0				Protection disabled
	DIA	DECIONAG	Enabled	1				Protection enable
d	KVV	REGION29	Disabled	0				Enable protection for region 29. Write '0' has no effect. Protection disabled
6	D\A/	PEGIONI20	Enabled	1				Protection enable Enable protection for region 20. Write '0' has no effect
е	KVV	REGION30	Disabled	0				Enable protection for region 30. Write '0' has no effect.
			Disabled	0				Protection disabled
f	DIA	DECION31	Enabled	1				Protection enable
	KW	REGION31	Disabled	0				Enable protection for region 31. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enable

12.1.2 CONFIG1

Address offset: 0x604

Block protect configuration register 1



Bit r	iumbe	r		31 30	29 28	3 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b	a :	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000		0 0	0 0	0	0	0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value					Description
Α	RW	REGION32							Enable protection for region 32. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
В	RW	REGION33							Enable protection for region 33. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
С	RW	REGION34							Enable protection for region 34. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
D	RW	REGION35							Enable protection for region 35. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Е	RW	REGION36							Enable protection for region 36. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
F	RW	REGION37							Enable protection for region 37. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
G	RW	REGION38							Enable protection for region 38. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Н	RW	REGION39							Enable protection for region 39. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
I	RW	REGION40							Enable protection for region 40. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
J	RW	REGION41							Enable protection for region 41. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
K	RW	REGION42							Enable protection for region 42. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
L	RW	REGION43							Enable protection for region 43. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
М	RW	REGION44							Enable protection for region 44. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
N	RW	REGION45							Enable protection for region 45. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
0	RW	REGION46							Enable protection for region 46. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Р	RW	REGION47							Enable protection for region 47. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Q	RW	REGION48							Enable protection for region 48. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
R	RW	REGION49							Enable protection for region 49. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
S	RW	REGION50							Enable protection for region 50. Write '0' has no effect.



Bit r	numbe	er		31 30	29	28	27 26	25	24	23 22 21	20 19	18	3 17	16	5 15	14	13	3 12	2 11	10	9	8	7	6	5	4	3	2	1	0
Id				f e	d	С	b a	Z	Υ	x w v	U T	S	R	Q	P	О	N	М	L	K	J	ī	Н	G	F	Ε	D	С	В	Α
Res	et 0x0	0000000		0 0	0	0	0 0	0	0	0 0 0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Value						Descripti																				
			Disabled	0						Protectio	n disal	ble	d																	
			Enabled	1						Protectio	n enab	ole	t																	
Т	RW	REGION51								Enable pr	otectio	on	for i	reg	ion	51	. W	rite	'0'	has	no	effe	ct.							
			Disabled	0						Protectio	n disal	ble	d																	
			Enabled	1						Protectio	n enab	ole	t																	
U	RW	REGION52								Enable pr	otectio	on	for	reg	ion	52	. W	rite	'0'	has	no	effe	ct.							
			Disabled	0						Protectio	n disal	ole	d																	
			Enabled	1						Protectio	n enab	ole	t																	
٧	RW	REGION53								Enable pr	otectio	on	for i	reg	ion	53	. W	rite	'0'	has	no	effe	ct.							
			Disabled	0						Protectio	n disal	ble	d																	
			Enabled	1						Protectio	n enab	ole	t																	
W	RW	REGION54								Enable pr	otectio	on	for i	reg	ion	54	. W	rite	'0'	has	no	effe	ct.							
			Disabled	0						Protectio	n disal	ble	d																	
			Enabled	1						Protectio	n enab	ole	t																	
Х	RW	REGION55								Enable pr	otectio	on	for	reg	ion	55	. W	rite	'0'	has	no	effe	ct.							
			Disabled	0						Protectio	n disal	ble	d																	
			Enabled	1						Protectio	n enab	ole	t																	
Υ	RW	REGION56								Enable pr	otectio	on	for	reg	ion	56	. W	rite	'0'	has	no	effe	ct.							
			Disabled	0						Protectio	n disal	ble	d																	
			Enabled	1						Protectio																				
Z	RW	REGION57								Enable pr				reg	ion	57	. W	rite	'0'	has	no	effe	ct.							
			Disabled	0						Protectio																				
			Enabled	1						Protectio																				
а	RW	REGION58	5							Enable pr				reg	ion	58	. W	rite	.0.	has	no	ette	ct.							
			Disabled	0						Protectio																				
	DVA	DECIONES	Enabled	1						Protectio									101											
b	KW	REGION59	Disabled	0						Enable pr				reg	ion	59	. vv	rite	0	nas	no	етте	ct.							
			Disabled Enabled	1						Protectio Protectio																				
С	D\A/	REGION60	спаріец	1						Enable pr				-00	ion	60	١٨.	rito	יחי.	hac	no	offo	ct							
C	NVV	REGIONOU	Disabled	0						Protectio				eg	1011	00	. vv	me	U	IIas	110	ene	CL.							
			Enabled	1						Protectio																				
d	RW	REGION61	Lilabica	_						Enable pr				reg	ion	61	۱۸/	rite	'n'	has	nο	effe	ct							
_			Disabled	0						Protectio						-														
			Enabled	1						Protectio																				
e	RW	REGION62								Enable pr				reg	ion	62	. W	rite	'0'	has	no	effe	ct.							
			Disabled	0						Protectio																				
			Enabled	1						Protectio																				
f	RW	REGION63								Enable pr				reg	ion	63	. W	rite	'0'	has	no	effe	ct.							
			Disabled	0						Protectio																				
			Enabled	1						Protectio	n enab	ole	t																	

12.1.3 DISABLEINDEBUG

Address offset: 0x608

Disable protection mechanism in debug interface mode

Bitı	numbe	er		31	. 30	29	28	27	26	5 25	5 24	23	22	21	20	19	18	17	16	15	14 :	13 :	L2 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id																																	А
Res	et 0x0	000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 1
Id	RW	Field	Value Id	Va	lue	:						De	scri	pti	on																		
Α	RW	DISABLEINDEBUG										Dis	sabl	e th	ne p	rot	ecti	on	me	cha	nisr	n fo	r N	VM	reg	ons	wh	ile					
												in	deb	ug	inte	rfa	ce r	nod	le. 1	Γhis	reg	giste	er w	ill c	nly	disa	ble	the	!				
												pro	otec	tio	n m	ech	ani	sm	if th	ne c	levi	ce i	s in	del	oug	nte	rfac	e m	node	э.			
			Disabled	1								Dis	sabl	e in	de	bug	5																



Bit number		31 30 29 28 27 20	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A
Reset 0x00000001		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Enabled	0	Enable in debug

12.1.4 CONFIG2

Address offset: 0x610

Block protect configuration register 2

BIO	CK P	protect configurati	ion register 2			
Bit n	numbe	er		31 30 29 28 27	26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e d c b	a Z \	/XWVUTSRQPONMLKJIHGFEDCBA
Rese	et OxO	0000000		0 0 0 0 0	0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value		Description
Α	RW	REGION64				Enable protection for region 64. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
В	RW	REGION65				Enable protection for region 65. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
С	RW	REGION66				Enable protection for region 66. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
D	RW	REGION67				Enable protection for region 67. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
E	RW	REGION68				Enable protection for region 68. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
F	RW	REGION69				Enable protection for region 69. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
G	RW	REGION70				Enable protection for region 70. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
Н	RW	REGION71				Enable protection for region 71. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
I	RW	REGION72				Enable protection for region 72. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
J	RW	REGION73				Enable protection for region 73. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
K	RW	REGION74				Enable protection for region 74. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
L	RW	REGION75				Enable protection for region 75. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
М	RW	REGION76				Enable protection for region 76. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
N	RW	REGION77				Enable protection for region 77. Write '0' has no effect.
			Disabled	0		Protection disabled
			Enabled	1		Protection enabled
0	RW	REGION78				Enable protection for region 78. Write '0' has no effect.
			Disabled	0		Protection disabled



Rit r	numbe	r		31 30	29 28	3 27	26.2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0	000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Enabled	1					Protection enabled
Р	RW	REGION79							Enable protection for region 79. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Q	RW	REGION80							Enable protection for region 80. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
R	RW	REGION81							Enable protection for region 81. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
S	RW	REGION82							Enable protection for region 82. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Т	RW	REGION83							Enable protection for region 83. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
U	RW	REGION84							Enable protection for region 84. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
٧	RW	REGION85							Enable protection for region 85. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
W	RW	REGION86							Enable protection for region 86. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Χ	RW	REGION87							Enable protection for region 87. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Υ	RW	REGION88							Enable protection for region 88. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
Z	RW	REGION89							Enable protection for region 89. Write '0' has no effect.
			Disabled	0					Protection disabled
			Enabled	1					Protection enabled
а	RW	REGION90		_					Enable protection for region 90. Write '0' has no effect.
			Disabled	0					Protection disabled
L	Direc	DECIONO1	Enabled	1					Protection enabled
b	KW	REGION91	Disabled	0					Enable protection for region 91. Write '0' has no effect.
			Disabled	0					Protection disabled
	DVA	PECIONO3	Enabled	1					Protection enabled
С	κW	REGION92	Disabled	0					Enable protection for region 92. Write '0' has no effect.
			Disabled	0					Protection disabled Protection enabled
d	DVA	DECIONO3	Enabled	1					
d	KW	REGION93	Disabled	0					Enable protection for region 93. Write '0' has no effect.
			Disabled	0					Protection disabled
	DVA	PECIONO4	Enabled	1					Protection enabled Enable protection for region 04. Write '0' has no effect.
е	ΚW	REGION94	Disabled	0					Enable protection for region 94. Write '0' has no effect.
			Disabled	1					Protection disabled Protection enabled
f	D\A/	PEGIONOS	Enabled	1					
	KVV	REGION95	Disabled	0					Enable protection for region 95. Write '0' has no effect.
			Disabled Enabled	1					Protection disabled
			Liidbieu	1					Protection enabled



12.1.5 CONFIG3

Address offset: 0x614

Block protect configuration register 3

	numb	er 						23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld Bas	a+ 0(0000000						X W V U T S R Q P O N M L K J I H G F E D C B A 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
res Id		Field	Value Id	0 0 Value	, 0	U	0 0	Description
A		REGION96	value lu	Value				Enable protection for region 96. Write '0' has no effect.
^	11.00	REGIONSO	Disabled	0				Protection disabled
			Enabled	1				Protection disabled
D	D\A/	REGION97	Enabled	1				
В	KVV	REGION97	Disabled	0				Enable protection for region 97. Write '0' has no effect. Protection disabled
			Disabled	0				
_	D) 4 /	DECIONOS	Enabled	1				Protection enabled
С	RW	REGION98	5	_				Enable protection for region 98. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
D	RW	REGION99						Enable protection for region 99. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
E	RW	REGION100						Enable protection for region 100. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
F	RW	REGION101						Enable protection for region 101. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
G	RW	REGION102						Enable protection for region 102. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
Н	RW	REGION103						Enable protection for region 103. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
ı	RW	REGION104						Enable protection for region 104. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
J	RW	REGION105						Enable protection for region 105. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
K	RW	REGION106						Enable protection for region 106. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
L	RW	REGION107						Enable protection for region 107. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
М	RW	REGION108						Enable protection for region 108. Write '0' has no effect.
		REGIONIO	Disabled	0				Protection disabled
			Enabled	1				Protection enabled
N	R\M	REGION109	Lilabica	•				Enable protection for region 109. Write '0' has no effect.
IN	11.00	KEGION103	Disabled	0				Protection disabled
			Enabled	1				Protection disabled
^	D\A/	DECION110	Ellableu	1				
0	r vv	REGION110	Disabled	0				Enable protection for region 110. Write '0' has no effect.
			Disabled	0				Protection disabled
D	511	DECIONAL	Enabled	1				Protection enabled
P	RW	REGION111						Enable protection for region 111. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
Q	RW	REGION112						Enable protection for region 112. Write '0' has no effect.
			Disabled	0				Protection disabled



Bitı	number			31 30 2	29 28 2	7 26 2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c k	b a Z	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x000	000000		0 0	0 0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW F		Value Id	Value				Description
			Enabled	1				Protection enabled
R	RW R	REGION113						Enable protection for region 113. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
S	RW R	REGION114						Enable protection for region 114. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
Т	RW R	REGION115		_				Enable protection for region 115. Write '0' has no effect.
-			Disabled	0				Protection disabled
			Enabled	1				Protection enabled
U	RW/ R	REGION116	Litablea	-				Enable protection for region 116. Write '0' has no effect.
Ū		.20.0.1120	Disabled	0				Protection disabled
			Enabled	1				Protection enabled
V	RW/ R	REGION117	Enablea	•				Enable protection for region 117. Write '0' has no effect.
•		(LOIONII)	Disabled	0				Protection disabled
			Enabled	1				Protection enabled
W	RW/ R	REGION118	Litablea	-				Enable protection for region 118. Write '0' has no effect.
••		(EGIONIII)	Disabled	0				Protection disabled
			Enabled	1				Protection enabled
Х	RW/ R	REGION119	Enablea	•				Enable protection for region 119. Write '0' has no effect.
^		(LOIONII)	Disabled	0				Protection disabled
			Enabled	1				Protection disabled
Υ	R\M/ R	REGION120	Lilabica	-				Enable protection for region 120. Write '0' has no effect.
	11.00	KEGIOWIZO	Disabled	0				Protection disabled
			Enabled	1				Protection disabled
Z	R\M/ R	REGION121	Lilabica	-				Enable protection for region 121. Write '0' has no effect.
_		(LOIONIZI	Disabled	0				Protection disabled
			Enabled	1				Protection enabled
а	RW/ R	REGION122	Litablea	-				Enable protection for region 122. Write '0' has no effect.
u		1201011122	Disabled	0				Protection disabled
			Enabled	1				Protection disabled
b	D\A/ D	REGION123	Lilabled	1				Enable protection for region 123. Write '0' has no effect.
D	11.00	(LGION123	Disabled	0				Protection disabled
			Enabled	1				Protection disabled Protection enabled
С	D\A/ D	REGION124	Lilabica	-				Enable protection for region 124. Write '0' has no effect.
·	11.00 11	(LOIOIVIZ4	Disabled	0				Protection disabled
			Enabled	1				Protection disabled Protection enabled
d	D\A/ D	REGION125	Ellableu	1				Enable protection for region 125. Write '0' has no effect.
u	NVV P	NEGION125	Disabled	0				Protection disabled
			Enabled	1				Protection disabled Protection enabled
Δ.	R\\\	REGION126	LIIGUICU	1				
е	LAN H	REGION126	Disabled	0				Enable protection for region 126. Write '0' has no effect. Protection disabled
			Disabled Enabled	1				Protection disabled Protection enabled
£	DIA/ 5	PEGION137	Lilableu	1				
1	KVV H	REGION127	Disabled	0				Enable protection for region 127. Write '0' has no effect.
			Disabled	0				Protection disabled
			Enabled	1				Protection enabled



13 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

13.1 Registers

Table 17: Instances

Base address	Peripheral	Instance	Description	Configuration
0x10000000	FICR	FICR	Factory Information Configuration	

Table 18: Register Overview

Register	Offset	Description	
CODEPAGESIZE	0x010	Code memory page size	
CODESIZE	0x014	Code memory size	
DEVICEID[0]	0x060	Device identifier	
DEVICEID[1]	0x064	Device identifier	
ER[0]	0x080	Encryption Root, word 0	
ER[1]	0x084	Encryption Root, word 1	
ER[2]	0x088	Encryption Root, word 2	
ER[3]	0x08C	Encryption Root, word 3	
IR[0]	0x090	Identity Root, word 0	
IR[1]	0x094	Identity Root, word 1	
IR[2]	0x098	Identity Root, word 2	
IR[3]	0x09C	Identity Root, word 3	
DEVICEADDRTYPE	0x0A0	Device address type	
DEVICEADDR[0]	0x0A4	Device address 0	
DEVICEADDR[1]	0x0A8	Device address 1	
INFO.PART	0x100	Part code	
INFO.VARIANT	0x104	Part Variant, Hardware version and Production configuration	
INFO.PACKAGE	0x108	Package option	
INFO.RAM	0x10C	RAM variant	
INFO.FLASH	0x110	Flash variant	
	0x114		Reserved
	0x118		Reserved
	0x11C		Reserved
TEMP.A0	0x404	Slope definition A0.	
TEMP.A1	0x408	Slope definition A1.	
TEMP.A2	0x40C	Slope definition A2.	
TEMP.A3	0x410	Slope definition A3.	
TEMP.A4	0x414	Slope definition A4.	
TEMP.A5	0x418	Slope definition A5.	
TEMP.B0	0x41C	y-intercept BO.	
TEMP.B1	0x420	y-intercept B1.	
TEMP.B2	0x424	y-intercept B2.	
TEMP.B3	0x428	y-intercept B3.	
TEMP.B4	0x42C	y-intercept B4.	
TEMP.B5	0x430	y-intercept B5.	
TEMP.TO	0x434	Segment end TO.	
TEMP.T1	0x438	Segment end T1.	
TEMP.T2	0x43C	Segment end T2.	
TEMP.T3	0x440	Segment end T3.	
TEMP.T4	0x444	Segment end T4.	



Register	Offset	Description
NFC.TAGHEADER0	0x450	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER1	0x454	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER2	0x458	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.
NFC.TAGHEADER3	0x45C	Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST,
		NFCID1_2ND_LAST and NFCID1_LAST.

13.1.1 CODEPAGESIZE

Address offset: 0x010 Code memory page size

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	R	CODEPAGESIZE		Code memory page size

13.1.2 CODESIZE

Address offset: 0x014 Code memory size

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A R CODESIZE		Code memory size in number of pages

Total code space is: CODEPAGESIZE * CODESIZE

13.1.3 DEVICEID[0]

Address offset: 0x060

Device identifier

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	L8 1	7 16	5 15	14	13 3	12 13	. 10	9	8	7 6	5 5	5 4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	ΑД	A	A	Α	Α	A A	Α	Α	Α	A A	A A	A A	Α	Α	А А
Re	set OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1	1	1	1 1	1	1	1	1 :	1	l 1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																
Α	R	DEVICEID										64	bit ι	ıniq	que	dev	ice i	der	ntifie	er											
												DE	VICE	ID[0] c	ont	ains	the	lea	st si	ignif	icant	bits	of t	he (devi	ce				
												ide	ntifi	er.	DE۱	VICE	EID[1	l] co	onta	ins	the i	nost	sign	ifica	nt l	oits	of t	he			
												dev	/ice	ide	ntif	ier.															

13.1.4 DEVICEID[1]

Address offset: 0x064

Device identifier

Bit number	31 30 29 28 2	27 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id	A A A A	A A A A A A A A A .	A A A A A A A A	A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1	1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description		

A R DEVICEID 64 bit unique device identifier



Reset 0xFFFFFFFF 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	. A A A A A A A A A A A A
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15	5 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.

13.1.5 ER[0]

Address offset: 0x080 Encryption Root, word 0

Bit number		31 30 29	28 2	7 26	25	24 2	3 22	21	20 1	9 18	17	16 3	15 1	4 13	12	11 10	9	8	7	6	5 -	4 3	3 2	1	0
Id		A A A	A	A A	Α	Α ,	A А	Α	A A	A	Α	Α	A A	Α Α	Α	A A	Α	Α	Α	Α	Α .	A A	A A	Α	Α
Reset 0xFFFFFFF		1 1 1	1 :	l 1	1	1	1 1	1	1 1	1	1	1	1 1	l 1	1	1 1	1	1	1	1	1	1 1	l 1	1	1
Id RW Field	Value Id	Value					escr	iptic	n																
A R FR						F	ncrvi	ntio	n Roc	ot w	ord	n													_

13.1.6 ER[1]

Address offset: 0x084 Encryption Root, word 1

Bit r	numbe	er		31	1 30	29	9 28	3 2	7 26	5 25	24	23	22	21	20	19	18	17 :	16	15 1	14 :	13 1	12 1	.1 1	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	. A	. 4	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	4 Δ	. A	Α	Α	Α	Α	Α	Α .	A A	A A
Res	et OxF	FFFFFF		1	1	1	. 1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1 1	l 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																		
Α	R	ER										En	cryp	otio	n R	oot,	wc	ord	n														

13.1.7 ER[2]

Address offset: 0x088 Encryption Root, word 2

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A R ER		Encryption Root, word n

13.1.8 ER[3]

Address offset: 0x08C Encryption Root, word 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A R ER		Encryption Root, word n

13.1.9 IR[0]

Address offset: 0x090 Identity Root, word 0



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A R IR	Identity Root, word n

13.1.10 IR[1]

Address offset: 0x094 Identity Root, word 1

Bit num	nber		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	LO	9	8	7	6	5	4	3 2	2 1	L 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α	Α.	Д	Α	Α	Α	A A	Α Α	AA
Reset 0	xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	1
Id R\	W Field	Value Id	Va	lue							De	scri	pti	on																			
A R	IR										Ide	nti	ty R	001	t, w	ord	l n																

13.1.11 IR[2]

Address offset: 0x098 Identity Root, word 2

Bitı	numbe	er		31 30	29	9 28	3 27	7 26	25	24	23	22	21	20 1	L9 1	18 1	.7 1	16 1	.5 1	4 1	3 1	2 1	1 1	9	8 (7	6	5	4	3	2	1 (
Id				A A	. 4	A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Α,	A A	Δ ,	۱ ۸	A A	Δ ,	\ <i>A</i>	. Α		A	Α	Α	Α	Α	Α	A A	Ĺ
Res	et OxF	FFFFFF		1 1	1	. 1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 :	L :	1 :	1	L 1	. 1	. 1	. 1	1	1	1	1	1	1 1	
Id	RW	Field	Value Id	Valu	9						De	scri	ptic	n																			ı
Α	R	IR									Ide	ntit	y R	oot,	wo	ord i	า																1

13.1.12 IR[3]

Address offset: 0x09C Identity Root, word 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A R IR		Identity Root, word n

13.1.13 DEVICEADDRTYPE

Address offset: 0x0A0

Device address type

Bitı	numbe	er		31 3	0 29	28	27	26	25	24	23 :	22 2	21 2	0 1	9 1	3 17	' 16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																															Α
Res	et OxF	FFFFFF		1 1	. 1	1	1	1	1	1	1	1	1 :	L 1	1	. 1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Valu	е						Des	crip	tio	1																	
Α	R	DEVICEADDRTYPE									Dev	ice	add	res	s ty	эe															
			Public	0							Pub	lic a	addr	ess																	
			Random	1							Ran	dor	n ac	ldre	SS																

13.1.14 **DEVICEADDR**[0]

Address offset: 0x0A4

Device address 0



Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	R	DEVICEADDR		48 bit device address

DEVICEADDR[0] contains the least significant bits of the device address. DEVICEADDR[1] contains the most significant bits of the device address. Only bits [15:0] of DEVICEADDR[1] are used.

13.1.15 **DEVICEADDR**[1]

Address offset: 0x0A8

Device address 1

Е	it num	nbei	r		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	7 16	15	14	13 1	.2 1	1 10	9	8	7	6 !	5 4	1 3	2	1	0
Ь	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	A A	A A	4 A	Α	Α	Α	Α	4 А	Α	Α	Α	A ,	Α ,	A A	A	Α	Α	Α
F	eset 0	xFF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	1 1	1	1	1	1	1 1	1	1	1	1	1 :	1 1	. 1	1	1	1
b	d RV	w	Field	Value Id	Va	lue							Des	crip	tio	n																	
A	Reset 0xFFFFFFF 1 1 1 1 1 1 1												48 I	bit d	levi	ice a	ddr	ress															
													add	lress	s. D	EVIC	CEA	onta DDF ss. O	R[1]	con	tain	s th	e mo	st s	igni	ficar	ıt bi	ts c	of	-			

13.1.16 INFO.PART

Address offset: 0x100

Part code

Bitı	numbe	er		31	L 30	29	28	27	26	25	24	23	22	21 2	20 1	L9 1	8 1	7 16	15	14	13	12 :	11 1	0 9	8 (7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	Δ Δ	A	Α	Α	Α	Α	A A	A 4	Δ Δ	. A	Α	Α	Α	Α	A .	4 А
Res	et 0x0	0052832		0	0	0	0	0	0	0	0	0	0	0	0	0 :	L O	1	0	0	1	0	1 () (0	0	0	1	1	0	0	1 0
Id	RW	Field	Value Id	Va	alue	•						De	scrip	otio	n																	
Α	R	PART										Par	t co	de																		
			N52832	0х	(528	332						nRl	528	332																		
			Unspecified	0х	FFF	FFF	FF					Un	spe	cifie	d																	

13.1.17 INFO.VARIANT

Address offset: 0x104

Part Variant, Hardware version and Production configuration

Bit number		31	L 30	29	2	8 2	7 2	26 2	25 2	4 2	2 2	2 21	1 20) 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Id		Α	Д	A	A	Δ Δ	۱ ۱	A A	A A	۸ ۸	Α Α	A A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	A A
Reset 0x41414142		0	1	. 0	(0) (0 (0 1	L (0 1	. 0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0 () :	1 0
Id RW Field	Value Id	Va	alu	е						C	esc	ript	ion																			
A R VARIANT										Р	art	Vari	iant	, На	ardv	vare	e ve	rsi	on	and	Pro	odu	ctio	n c	onfi	gur	atio	on,				,
										е	nco	ded	l as	ASC	II																	
	AAAA	0x	41	414	14	1				Δ	AAA	4																				
	AAAB	0x	41	414	14	2				Δ	AAI	3																				
	AABA	0x	41	414	24	1				Δ	ABA	4																				
	AABB	0x	41	414	24	2				Δ	ABI	3																				
	AAB0	0x	41	414	23	0				Δ	AB()																				
	AAE0	0x	41	414	53	0				Δ	AEC)																				
	Unspecified	0x	(FFI	FFFF	FF	:				ι	Jnsp	ecit	fied																			

13.1.18 INFO.PACKAGE

Address offset: 0x108

Package option



Bit	numb	er		31	30	29	28 2	27 2	6 25	5 2	4 23	3 22	21	20	19	18	17 1	6 1	15 1	4 13	12	11 1	0 9	8	7	6	5	4 3	2	1 0
Id				Α	Α	Α	Α .	A A	4 Α	A A	Δ Δ	А	Α	Α	Α	Α	Α /	Δ.	A A	A A	Α	Α ,	A A	Α	Α	Α	Α .	A A	A	АА
Res	et 0x0	0002000		0	0	0	0	0 (0 0) (0	0	0	0	0	0	0 (0	0 () 1	0	0 (0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue						D	escri	ptic	on																
Α	R	PACKAGE									Pa	acka	ge o	ptio	on															
			QF	0x	200	0					Q	Fxx -	48-	pin	QF	N														
			СН	0x	200	1					CI	Hxx -	7x8	3 W	LCS	P 5	6 ba	lls												
			CI	0x	200	2					CI	xx -	7x8	WL	CSP	56	bal	ls												
			CK	0x	200	5					CI	Kxx -	7x8	8 W	LCS	P 5	6 ba	lls v	with	bac	ksid	e coa	ting	for	ligh	t				
											рі	roted	ction	ı																
			Unspecified	0x	FFFF	FFF	F				U	nspe	cifie	ed																

13.1.19 INFO.RAM

Address offset: 0x10C

RAM variant

Bit	numl	per		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 :	16 :	15 :	14 1	.3 1	L2 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Д	A A	Δ Α	A A	A	Α	Α	Α	Α	Α	Α	А А
Re	set 0x	00000040		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	1	0	0	0	0	0 0
Id	RW	/ Field	Value Id	Va	lue							De	scri	otic	n																		
Α	R	RAM										RA	Μv	aria	nt																		
			K16	0x	10							16	kBy	te F	RAN	1																	
			K32	0x	20							32	kBy	te F	RAN	1																	
			K64	0x	40							64	kBy	te F	RAN	1																	
			Unspecified	0x	FFF	FFF	FF					Un	spe	cifie	d																		

13.1.20 INFO.FLASH

Address offset: 0x110

Flash variant

Bit r	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 1	L9 1	.8 1	7 16	5 15	14	13	12 1	.1 1	.0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	A A	Δ	A	Α	Α	Α	A	Δ,	4 4		A	Α	Α	Α	Α	Α.	А А
Res	et OxO	0000200		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 1	. 0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	R	FLASH										Flas	h va	aria	nt																	
			K128	0x	80							128	kBy	yte	FLA	SH																
			K256	0x	100							256	kBy	yte	FLA	SH																
			K512	0x	200							512	kBy	yte	FLA	SH																
			Unspecified	0x	FFFI	FFF	FF					Uns	pec	ifie	d																	

13.1.21 TEMP.A0

Address offset: 0x404 Slope definition A0.

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																							A	A	Α	Α	Α	Α	Α	Α	Α .	Δ.	А А
Res	et OxC	0000320		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	1	1	0	0	1	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue	•						De	cri	ptic	on																		
Α	R	Α										Α (lop	e d	efi	nitio	on)	reg	iste	r.													

13.1.22 TEMP.A1

Address offset: 0x408 Slope definition A1.



Bit	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	1 2	0 1	9 1	8 1	7 1	6 15	5 14	1 13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id																							Α	Α	Α	Α	Α	Α	Α	Α	A	A A	4 А
Res	et 0x0	0000343		0	0	0	0	0	0	0	0	0	0)	0 () (0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0 :	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	Α										A (s	lope	de	fini	tior	n) re	gis	ter.														

13.1.23 TEMP.A2

Address offset: 0x40C Slope definition A2.

Bit	numb	er		31	30 :	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	.8 1	.7 1	6 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Id																							Α	Α	Α	Α	Α	Α	Α	Α	A	A A	4 А
Res	et 0x0	000035D		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (0 () (0 0	0	0	0	1	1	0	1	0	1	1 :	L (0 1
Id	RW	Field	Value Id	Val	lue							Des	crip	tio	n																		
Α	R	Α										A (s	lope	e de	efin	tio	n) r	egis	ster														

13.1.24 TEMP.A3

Address offset: 0x410 Slope definition A3.

Bit r	numbe	er		31	30 2	9 :	28 2	7 26	25	24	23	22	21	20	19 :	18 :	17 :	16 :	15 :	L4 1	.3 1	2 11	. 10	9	8	7	6	5	4	3	2 :	1 0
Id																						Α	Α	Α	Α	Α	Α	Α	Α	A	A A	4 А
Res	et OxC	0000400		0	0 ()	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	1	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						De	scr	iptio	on																		
Α	R	Α									Α (slo	pe d	efir	itio	n) r	egi	ste	r.													

13.1.25 TEMP.A4

Address offset: 0x414 Slope definition A4.

Bit n	umb	er		31	30 2	9 2	8 27	26	25 2	4 2	3 22	2 21	20	19	18 :	17 1	16 1	15 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id																					Α	Α	Α	Α	Α	Α	Α	A	А А	Α	Α
Rese	t OxC	0000452		0	0	0 0	0 0	0	0 (0 0	0	0	0	0	0	0	0	0 (0 0	0	0	1	0	0	0	1	0	1	0 0	1	0
Id	RW	Field	Value Id	Va	lue					D	esc	ripti	on																		
Α	R	A								Α	(slc	pe o	defi	nitic	n) ı	regi	stei	٠.													

13.1.26 TEMP.A5

Address offset: 0x418 Slope definition A5.

Bit	numbe	er		31	30	29 2	28 2	27 2	6 2	5 2	4 2	3 2	2 2	1 2	0 1	9 18	8 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id																							Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α.	A A	Ą
Res	et 0x0	000037В		0	0	0	0	0 (0 (0 () () (0) (0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	0	1 1	L
Id	RW	Field	Value Id	Va	lue						C	esc	ript	tior	1																			
Α	R	Α									Δ	(sl	ope	de	fini	tion	ı) re	gist	er.															7

13.1.27 TEMP.B0

Address offset: 0x41C y-intercept B0.



																								_	_	_	_	_				_
Bit	numb	er		31	. 30	29	28 2	/ 26	5 25	24	23	22	21.	20 :	19 1	18 1	./ 1	6 1	5 1	4 1.	3 12	2 11	. 10	9	8	/	6	5	4 .	3 2	1	O
Id																				Δ	A	A	Α	Α	Α	Α	Α	Α	Α /	Α Α	A	Α
Re	et 0x	00003FCC		0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0 (0 () () 1	. 1	. 1	1	1	1	1	1	0	0 :	l 1	. 0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	n																		
Α	R	В									В (v-in	tero	ent	.)																	

13.1.28 TEMP.B1

Address offset: 0x420

y-intercept B1.

Bitı	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 :	19 1	18 :	17 1	16 1	15 1	4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3	2	1 0
Id																					A	A A	. A	. A	Α	Α	Α	Α	Α	Α	A	Α ,	4 А
Res	et 0x0	0003F98		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 1	1	. 1	1	1	1	1	0	0	1	1	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	В										3 (y	-int	erc	ept)																	

13.1.29 TEMP.B2

Address offset: 0x424

y-intercept B2.

E	3it n	umb	er		31 30 29 28 2	27 26	25	24 2	23 22	2 21	20 :	19 18	8 17	16	15	14 1	3 12	2 11	10	9	8	7	6	5 4	3	2	1 ()
1	d															A	Α Α	А	Α	Α	Α	Α	Α	A A	A A	Α	A	
F	Rese	t OxC	0003F98		0 0 0 0	0 0	0	0	0 0	0	0	0 0	0	0	0	0 1	1	. 1	1	1	1	1	0	0 1	1	0	0 ()
ı	d	RW	Field	Value Id	Value			1	Desc	riptio	on																	
		R	_							nter		١.																٠.

13.1.30 TEMP.B3

Address offset: 0x428

y-intercept B3.

Id A A A A A A A A A A A A A A A A A A A	_
Id A A A A A A A A A A A A A A A A A A A	
	1 0
51 50 25 20 27 20 25 24 25 22 21 20 15 10 17 10 15 14 15 12 11 10 5 0 7 0 5 4 5 2	A A
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0

13.1.31 TEMP.B4

Address offset: 0x42C

y-intercept B4.

Bit numb	per		31	30 2	9 28	27 2	26 2	5 24	1 23	22	21	20 1	9 18	3 17	16	15 1	4 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1)
Id																	A	A	Α	Α	Α	Α	Α	Α	A A	A A	Α	Α	Δ
Reset 0x	0000004D		0	0 0	0	0	0 (0 0	0	0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0	1	0 0) 1	1	0	1
Id RW	/ Field	Value Id	Val	ue					De	scri	ptic	n																	
A R	В								В (y-in	terc	ept)																	7

13.1.32 TEMP.B5

Address offset: 0x430

y-intercept B5.



Bit	numb	er		31 3	30 29	28	27	26 2	25 2	24 2	3 2	2 21	L 20	19	18	17	16	15 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																			A	Α Α	A	Α	Α	Α	Α	Α	Α	A	4 A	Α.	Α
Res	et 0x	00003E10		0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 1	. 1	. 1	1	1	0	0	0	0	1	0 0	0	0
Id	RW	Field	Value Id	Valu	ıe						esc	ript	ion																		
Α	R	В								Е	3 (v-	inte	rcer	ot)																	

13.1.33 TEMP.T0

Address offset: 0x434 Segment end T0.

Bit	numbe	er		31	30	29	28 2	27 2	6 2	25 2	4 2	23 2	22 2	1 2	0 1	9 1	8 17	16	15	14	13	12 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	A	Δ.	А А
Res	et 0x0	00000E2		0	0	0	0	0 (0 (0 (0	0	0 () (0 () (0	0	0	0	0	0	0 (0	0	1	1	1	0	0 (0	1 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	R	Т									7	- (se	egm	en	t en	d)re	gist	er.														

13.1.34 TEMP.T1

Address offset: 0x438 Segment end T1.

Bit r	numbe	er		31	30 2	9 :	28 2	7 26	5 25	24	23	22	21	20 :	19 1	.8 1	7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3 :	2 1	. 0
Id																										Α	Α	Α	Α	A A	4 A	A
Res	et OxO	0000000		0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	n																		
Α	R	Т									T (seg	ner	t ei	nd)r	egis	ter															

13.1.35 TEMP.T2

Address offset: 0x43C Segment end T2.

Bit r	numbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 1	9 1	8 1	7 1	6 1	5 14	1 13	12	11	10	9 :	8 7	6	5	4	3	2	1 0
Id																										A	. A	Α	Α	Α	Α	А А
Res	et OxC	0000014		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0) (0	0	0	0	0	0 (0 0	0	0	1	0	1	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	R	Т										T (s	egn	nen	t er	ıd)r	egis	ter.														

13.1.36 TEMP.T3

Address offset: 0x440 Segment end T3.

Bit	numb	er		31 3	30 29	28	8 27	26	25	24	23	22 2	21 2	0 1	9 1	8 17	7 16	15	14	13 1	2 1	10	9	8	7	6	5 4	4 3	2	1	0
Id																									Α	Α	A	ДД	Α.	Α	Α
Re	set 0x0	0000019		0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	1 1	0	0	1
Id	RW	Field	Value Id	Valu	ıe						Des	crip	tio	n																	
Α	R	Т									T (s	egn	nent	t en	d)re	gist	er.														

13.1.37 TEMP.T4

Address offset: 0x444 Segment end T4.



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9	9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A
Reset 0x00000050	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 0 1 0 0 0 0
Id RW Field Value Id	Value Description	
Δ R T	T (segment end)register	

13.1.38 NFC.TAGHEADER0

Address offset: 0x450

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 :	19 :	18 :	17 1	16 1	5 14	1 13	12	11 :	.0 9	8	7	6	5	4	3	2	1 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	C I	3 B	В	В	В	ВЕ	3 B	Α	Α	Α	Α	Α .	Α .	А А
Res	et OxF	FFFF5F		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1 :	l 1	0	1	0	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue)						Des	crip	otio	n																	
Α	R	MFGID										Def	ault	M	anu	ıfac	tur	er II): N	ord	c Se	mico	nd	ucto	r AS	A h	as I	CM				
												0x5	F																			
В	R	UD1										Uni	que	ide	enti	ifier	by	te 1														
С	R	UD2										Uni	que	ide	enti	ifier	by	te 2														
D	R	UD3										Uni	que	ide	enti	ifier	by	te 3														

13.1.39 NFC.TAGHEADER1

Address offset: 0x454

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 1	L9 1	.8 1	7 1	6 1	5 14	13	12	11 :	10	9	8	7	6 5	5 4	1 3	2	1	0
Id				D	D	D	D	D	D	D	D	С	С	С	С	C (C (c c	: B	В	В	В	В	В	В	В	١.	A A	4 4	A A	Α	Α	Α
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	. 1	1	1	1	1	1	1	1 :	L	1 :	1 1	l 1	1	1	1
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																		
Α	R	UD4										Uni	ique	ide	enti	fier	byt	e 4															_
В	R	UD5										Uni	ique	ide	enti	fier	byt	e 5															
С	R	UD6										Uni	ique	ide	enti	fier	byt	e 6															
D	R	UD7										Uni	ique	ide	enti	fier	byt	e 7															

13.1.40 NFC.TAGHEADER2

Address offset: 0x458

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	.3 1	2 1	1 1	0 9	8	7	6	5	4	3	2 :	1 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	ВІ	3 E	3 E	3 E	8 B	Α	Α	Α	Α	Α	A A	4 А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	. 1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	otic	on																		
Α	R	UD8										Un	ique	id	enti	ifie	r by	rte 8	3														
В	R	UD9										Un	ique	id	enti	ifie	r by	te 9	9														
С	R	UD10										Un	ique	id	enti	ifie	r by	te 1	10														
D	R	UD11		Unique identifier byte 11																													

13.1.41 NFC.TAGHEADER3

Address offset: 0x45C

Default header for NFC Tag. Software can read these values to populate NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST.



Bit r	iumbe	er		31	1 30	29	28	3 27	26	25	24 :	23 2	2 21	20	19	18	17	16	15 1	4 1	3 12	11	10	9 8	3 7	' 6	5	4	3	2	1 0
Id				D	D	D	D	D	D	D	D	C (С	С	С	С	С	С	В	ВВ	В	В	В	В	3 A	A	Α	Α	Α	Α	А А
Rese	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1 1	1	1	1	1 :	L 1	. 1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue	:					- 1	Des	ript	ion																	
Α	R	UD12									ı	Unic	jue i	den	tifie	r by	yte :	L2													
В	R	UD13									ı	Unic	jue i	den	tifie	r by	yte :	L3													
С	R	UD14									-	Unic	jue i	den	tifie	r by	yte :	L4													
D	R	UD15									ı	Unic	jue i	den	tifie	r by	yte :	L5													



14 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user specific settings.

For information on writing UICR registers, see the *NVMC — Non-volatile memory controller* on page 29 and *Memory* on page 23 chapters.

14.1 Registers

Table 19: Instances

Base address	Peripheral	Instance	Description	Configuration		
0x10001000	UICR	UICR	User Information Configuration			

Table 20: Register Overview

Register	Offset	Description	
	0x000		Reserved
	0x004		Reserved
	0x008		Reserved
	0x010		Reserved
NRFFW[0]	0x014	Reserved for Nordic firmware design	
NRFFW[1]	0x018	Reserved for Nordic firmware design	
NRFFW[2]	0x01C	Reserved for Nordic firmware design	
NRFFW[3]	0x020	Reserved for Nordic firmware design	
NRFFW[4]	0x024	Reserved for Nordic firmware design	
NRFFW[5]	0x028	Reserved for Nordic firmware design	
NRFFW[6]	0x02C	Reserved for Nordic firmware design	
NRFFW[7]	0x030	Reserved for Nordic firmware design	
NRFFW[8]	0x034	Reserved for Nordic firmware design	
NRFFW[9]	0x038	Reserved for Nordic firmware design	
NRFFW[10]	0x03C	Reserved for Nordic firmware design	
NRFFW[11]	0x040	Reserved for Nordic firmware design	
NRFFW[12]	0x044	Reserved for Nordic firmware design	
NRFFW[13]	0x048	Reserved for Nordic firmware design	
NRFFW[14]	0x04C	Reserved for Nordic firmware design	
NRFHW[0]	0x050	Reserved for Nordic hardware design	
NRFHW[1]	0x054	Reserved for Nordic hardware design	
NRFHW[2]	0x058	Reserved for Nordic hardware design	
NRFHW[3]	0x05C	Reserved for Nordic hardware design	
NRFHW[4]	0x060	Reserved for Nordic hardware design	
NRFHW[5]	0x064	Reserved for Nordic hardware design	
NRFHW[6]	0x068	Reserved for Nordic hardware design	
NRFHW[7]	0x06C	Reserved for Nordic hardware design	
NRFHW[8]	0x070	Reserved for Nordic hardware design	
NRFHW[9]	0x074	Reserved for Nordic hardware design	
NRFHW[10]	0x078	Reserved for Nordic hardware design	
NRFHW[11]	0x07C	Reserved for Nordic hardware design	
CUSTOMER[0]	0x080	Reserved for customer	
CUSTOMER[1]	0x084	Reserved for customer	
CUSTOMER[2]	0x088	Reserved for customer	
CUSTOMER[3]	0x08C	Reserved for customer	
CUSTOMER[4]	0x090	Reserved for customer	
CUSTOMER[5]	0x094	Reserved for customer	
CUSTOMER[6]	0x098	Reserved for customer	



Register	Offset	Description
CUSTOMER[7]	0x09C	Reserved for customer
CUSTOMER[8]	0x0A0	Reserved for customer
CUSTOMER[9]	0x0A4	Reserved for customer
CUSTOMER[10]	0x0A8	Reserved for customer
CUSTOMER[11]	0x0AC	Reserved for customer
CUSTOMER[12]	0x0B0	Reserved for customer
CUSTOMER[13]	0x0B4	Reserved for customer
CUSTOMER[14]	0x0B8	Reserved for customer
CUSTOMER[15]	0x0BC	Reserved for customer
CUSTOMER[16]	0x0C0	Reserved for customer
CUSTOMER[17]	0x0C4	Reserved for customer
CUSTOMER[18]	0x0C8	Reserved for customer
CUSTOMER[19]	0x0CC	Reserved for customer
CUSTOMER[20]	0x0D0	Reserved for customer
CUSTOMER[21]	0x0D4	Reserved for customer
CUSTOMER[22]	0x0D8	Reserved for customer
CUSTOMER[23]	0x0DC	Reserved for customer
CUSTOMER[24]	0x0E0	Reserved for customer
CUSTOMER[25]	0x0E4	Reserved for customer
CUSTOMER[26]	0x0E8	Reserved for customer
CUSTOMER[27]	0x0EC	Reserved for customer
CUSTOMER[28]	0x0F0	Reserved for customer
CUSTOMER[29]	0x0F4	Reserved for customer
CUSTOMER[30]	0x0F8	Reserved for customer
CUSTOMER[31]	0x0FC	Reserved for customer
PSELRESET[0]	0x200	Mapping of the nRESET function (see POWER chapter for details)
PSELRESET[1]	0x204	Mapping of the nRESET function (see POWER chapter for details)
APPROTECT	0x208	Access Port protection
NFCPINS	0x20C	Setting of pins dedicated to NFC functionality: NFC antenna or GPIO

14.1.1 NRFFW[0]

Address offset: 0x014

Reserved for Nordic firmware design

Bit nu	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	L3 1	12 1	111	.0 9	9 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	A A	A /	A A	A	Α	Α	Α	Α	Α	А А
Reset	0xFl	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	. 1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	cri	ptic	on																		
Α	RW	NRFFW		Reserved for Nordic firmware design																													

14.1.2 NRFFW[1]

Address offset: 0x018

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0							
Id	A A A A A A A A A A A A A A A A A A A							
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1							
Id RW Field Value Id	Value Description							
A RW NRFFW	Reserved for Nordic firmware design							

14.1.3 NRFFW[2]

Address offset: 0x01C

Reserved for Nordic firmware design



14.1.4 NRFFW[3]

Address offset: 0x020

Reserved for Nordic firmware design

14.1.5 NRFFW[4]

Address offset: 0x024

Reserved for Nordic firmware design

14.1.6 NRFFW[5]

Address offset: 0x028

Reserved for Nordic firmware design

RW NRFFW Reserved for Nordic firmware design

14.1.7 NRFFW[6]

Address offset: 0x02C

Reserved for Nordic firmware design

14.1.8 NRFFW[7]

Address offset: 0x030

Reserved for Nordic firmware design

RW NRFFW Reserved for Nordic firmware design



14.1.9 NRFFW[8]

Address offset: 0x034

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0						
Id		A A A A A A A A A A A A A A A A A A A						
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1						
Id RW Field	Value Id	Value Description						
A RW NRFFW		Reserved for Nordic firmware design						

Reserved for Nordic firmware design

14.1.10 NRFFW[9]

Address offset: 0x038

Reserved for Nordic firmware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0							
Id									
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1							
ld RW Field	Value Id	Value Description							
A RW NRFFW		Reserved for Nordic firmware design							

14.1.11 NRFFW[10]

Address offset: 0x03C

Reserved for Nordic firmware design

Bit r	numbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16 :	15 :	14	13 :	12 :	11 1	0 9	8	7	6	5	4	3	2	1 (D
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	. Δ	. A	Α	Α	Α	Α	Α	Α	A	4
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	. 1	1	1	1	1	1	1	1	1	ı
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	NRFFW										Re	serv	ved	for	No	rdic	fir	nw	are	de	sign												_

14.1.12 NRFFW[11]

Address offset: 0x040

Reserved for Nordic firmware design

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 1	15 1	.4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	A A	A A	. A	Α	Α	Α	Α	Α	Α	Α	A A	λ Α	A A
Rese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1	1	1	1	1	1	1	1	1	1 :	L 1	l 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	NRFFW										Res	erv	ed	for	Noi	dic	firr	nw	are	des	gn											

14.1.13 NRFFW[12]

Address offset: 0x044

Reserved for Nordic firmware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW NRFFW Reserved for Nordic firmware design

14.1.14 NRFFW[13]

Address offset: 0x048

Reserved for Nordic firmware design



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFFW		Reserved for Nordic firmware design

14.1.15 NRFFW[14]

Address offset: 0x04C

Reserved for Nordic firmware design

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α.	4 Α	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	l 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	NRFFW										Res	serv	/ed	for	Noi	rdic	fir	mw	are	de	sigr	1											

14.1.16 NRFHW[0]

Address offset: 0x050

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

14.1.17 NRFHW[1]

Address offset: 0x054

Reserved for Nordic hardware design

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α.	Α .	
Rese	t OxFI	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																				ı
Α	RW	NRFHW										Re	erv	ed	for	Noi	dic	ha	rdw	vare	de	sig	n												

14.1.18 NRFHW[2]

Address offset: 0x058

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

14.1.19 NRFHW[3]

Address offset: 0x05C

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description

RW NRFHW Reserved for Nordic hardware design



14.1.20 NRFHW[4]

Address offset: 0x060

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

Reserved for Nordic hardware design

14.1.21 NRFHW[5]

Address offset: 0x064

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

14.1.22 NRFHW[6]

Address offset: 0x068

Reserved for Nordic hardware design

Bit	numb	er		31	30	29	28 :	27 :	26	25 :	24	23 :	22	21 2	20 :	19 1	8 1	7 1	6 1	.5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α /	Δ ,	Δ Α	Δ ,	Δ	λ Δ	. Δ	A	Α	Α	Α	Α	Α	Α	A A	A A	Α
Res	et 0xl	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	1 :	1 1	L 1	. 1	. 1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																		
	D) 4 /	NIDELINA										_					10																

Reserved for Nordic hardware design

14.1.23 NRFHW[7]

Address offset: 0x06C

Reserved for Nordic hardware design

Bit r	iumbe	r		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	NRFHW		Reserved for Nordic hardware design

14.1.24 NRFHW[8]

Address offset: 0x070

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18	3 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A	A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW NRFHW Reserved for Nordic hardware design

14.1.25 NRFHW[9]

Address offset: 0x074

Reserved for Nordic hardware design



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

14.1.26 NRFHW[10]

Address offset: 0x078

Reserved for Nordic hardware design

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW NRFHW		Reserved for Nordic hardware design

14.1.27 NRFHW[11]

Address offset: 0x07C

Reserved for Nordic hardware design

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW NRFHW	Reserved for Nordic hardware design

14.1.28 CUSTOMER[0]

Address offset: 0x080 Reserved for customer

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.29 CUSTOMER[1]

Address offset: 0x084 Reserved for customer

Е	Bit nu	mbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 :	15 1	L4 1	13 1	12 1	.1 1	0 9	9 8	3 7	6	5	4	3	2	1	0
10	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	4 Α	۸ ۸	۸ 4	A A	. A	Α	Α	Α	Α	Α	Α
F	leset	0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	ι :	L 1	l 1	1	1	1	1	1	1	1
1	d i	RW	Field	Value Id	Va	alue							De	scri	ptic	n																			
A	4	RW	CUSTOMER										Res	erv	ed	for	cus	ton	ner																

14.1.30 CUSTOMER[2]

Address offset: 0x088 Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description	

A RW CUSTOMER Reserved for customer



14.1.31 CUSTOMER[3]

Address offset: 0x08C Reserved for customer

Bit nur	mber		31	L 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 A	A	А
Reset	0xFFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	. 1
ld F	RW Field	Value Id	Va	alue							De	scri	ptic	on																			
A F	RW CUSTOMER										Re	serv	ed	for	cus	ton	ner																

14.1.32 CUSTOMER[4]

Address offset: 0x090 Reserved for customer

Bit	: nı	umbe	er		31	30	29	28	27	26	25	5 24	1 2	3 22	2 21	L 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	. 4	. Α	. A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	
Re	set	t OxF	FFFFFF		1	1	1	1	1	1	1	1	. 1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	
Id		RW	Field	Value Id	Va	lue							D	esc	ript	ion																				l
Α		RW	CUSTOMER										R	ese	rve	d fo	r cu	sto	me	r																-

14.1.33 CUSTOMER[5]

Address offset: 0x094 Reserved for customer

Bit	numbe	r		33	1 30	29	28	3 2	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	12 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	Α	АА
Res	et 0xF	FFFFFF		1	1	1	1	1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	l 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	V	alue	•						De	scr	iptio	on																		
Α	RW	CUSTOMER										Re	ser	ved	for	cus	tor	ner															

14.1.34 CUSTOMER[6]

Address offset: 0x098 Reserved for customer

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 :	20 1	19 1	18 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5 4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	A ,	4 Α	Α.	Α	Α .	Α
Re	set 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	۱ 1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	CUSTOMER										Res	erv	ed 1	for o	cust	tom	er															_

14.1.35 CUSTOMER[7]

Address offset: 0x09C Reserved for customer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

14.1.36 CUSTOMER[8]

Address offset: 0x0A0 Reserved for customer



Bitı	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	l 1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	n																			
Α	RW	CUSTOMER										Res	erv	ed '	for	cust	tom	ner																

14.1.37 CUSTOMER[9]

Address offset: 0x0A4
Reserved for customer

Bit	numb	er		31	1 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13 :	12	11 1	.0 9	9 8	3 7	6	5	4	3	2	1 0	ı
Id				Α	Α	Α	Α	Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α Α	Α Α	Δ Δ	A	Α	Α	Α	Α	A A	
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	ι :	L 1	. 1	1	1	1	1	1 1	
Id	RW	Field	Value Id	Va	alue	:						De	scri	ptic	on																			ı
Α	RW	CUSTOMER										Res	serv	/ed	for	cus	ton	ner																1

14.1.38 CUSTOMER[10]

Address offset: 0x0A8
Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description
A RW CUSTOMER	Reserved for customer

14.1.39 CUSTOMER[11]

Address offset: 0x0AC Reserved for customer

Bitı	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.40 CUSTOMER[12]

Address offset: 0x0B0 Reserved for customer

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue							De	scr	ipti	on																			
Α	RW	CUSTOMER										Re	ser	ved	foi	r cus	stoi	mer	r															

14.1.41 CUSTOMER[13]

Address offset: 0x0B4 Reserved for customer

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value Description

A RW CUSTOMER Reserved for customer



14.1.42 CUSTOMER[14]

Address offset: 0x0B8 Reserved for customer

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13 :	12 :	11 1	10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	A A	\ A	А А
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	n																			
^	DIA	CLICTOMACD										n -			c																			

A RW CUSTOMER Reserved for customer

14.1.43 CUSTOMER[15]

Address offset: 0x0BC Reserved for customer

Bi	t n	umbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4
R	ese	t OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L
Id	ı	RW	Field	Value Id	Va	lue							De	scr	ipti	on																				ı
Δ		R\//	CUSTOMER										R۵	cor	hav	for	CHI	tor	nor																	П

A RW CUSTOMER Reserved for customer

14.1.44 CUSTOMER[16]

Address offset: 0x0C0 Reserved for customer

Bit	numbe	er		31	L 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	CUSTOMER										Re	serv	ed	for	cus	ton	ner																

14.1.45 CUSTOMER[17]

Address offset: 0x0C4 Reserved for customer

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 :	20 1	19 1	18 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5 4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	A ,	4 Α	Α.	Α	Α .	Α
Re	set 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	۱ 1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	CUSTOMER										Res	erv	ed 1	for o	cust	tom	er															_

14.1.46 CUSTOMER[18]

Address offset: 0x0C8 Reserved for customer

Bit number	31 30	0 29 28 27 26	6 25 24 23 2	2 21 20 19	18 17 16	5 15 14 13	12 11 10 9	8 7 6	5 4 3 2	1 0
Id	A A	A A A A	AAAA	АААА	A A A	A A A	A A A A	A A A	A A A A A	АА
Reset 0xFFFFFFF	1 1	11111	. 1 1 1 1	1 1 1 1	1 1 1	1 1 1	1 1 1 1	1 1 1	1 1 1 1 :	1 1
ld RW Field Va	lue Id Value	е	Desc	ription						

A RW CUSTOMER Reserved for customer

14.1.47 CUSTOMER[19]

Address offset: 0x0CC Reserved for customer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ld RW Field	Value Id	Value Description
A RW CUSTOMER		Reserved for customer

14.1.48 CUSTOMER[20]

Address offset: 0x0D0 Reserved for customer

Bit	numbe	er		31	1 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18 3	17 :	16 1	15 1	4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α,	Δ ,	A	A	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 :	1	. 1	1	1	1	1	1	1	1	1 1	l 1	. 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	n																		
Α	RW	CUSTOMER										Res	erv	ed	for	cus	tom	ner															

14.1.49 CUSTOMER[21]

Address offset: 0x0D4 Reserved for customer

Bit r	number		31 30 29 28 2	7 26 25 24	1 23 22	21 20	19 1	8 17	16 15	14 1	3 12	11 1	9	8	7	6	5 4	3	2	1 0
Id			A A A A A	4 A A A	. A A	A A	A A	A A	А А	A A	A	A A	A	Α	Α	Α .	ДД	А	A	А А
Res	et OxFFFFFF		1 1 1 1 1	1 1 1 1	1 1	1 1	1 1	l 1	1 1	1 1	1	1 1	. 1	1	1	1	1 1	. 1	1	1 1
Id	RW Field	Value Id	Value		Descri	ption														
Α	RW CUST	MER			Reserv	ed fo	r cust	omer												

14.1.50 CUSTOMER[22]

Address offset: 0x0D8 Reserved for customer

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.51 CUSTOMER[23]

Address offset: 0x0DC Reserved for customer

Bit nu	ımbe	r		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Reset	0xFl	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CUSTOMER		Reserved for customer

14.1.52 CUSTOMER[24]

Address offset: 0x0E0 Reserved for customer

Bit number	31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A
Reset 0xFFFFFFF	1 1 1 1 :	1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id RW Field Value Id	Value	Description	

A RW CUSTOMER Reserved for customer



14.1.53 CUSTOMER[25]

Address offset: 0x0E4 Reserved for customer

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13 :	12 :	11 1	10	9	8	7	6	5	4	3 2	2 2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	A A	A A	А А
Res	et 0xl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	1 1
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	n																			
^	DIA	CLICTOMACD										n -			c																			

A RW CUSTOMER Reserved for customer

14.1.54 CUSTOMER[26]

Address offset: 0x0E8
Reserved for customer

E	Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1	ld	A A A A A A A A A A A A A A A A A A A
ı	Reset 0xFFFFFFF	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
ı	ld RW Field Value Id	Value Description
-	Δ RW CUSTOMER	Reserved for customer

A RW CUSTOMER Reserved for customer

14.1.55 CUSTOMER[27]

Address offset: 0x0EC Reserved for customer

Bit	numbe	r		33	1 30	29	28	3 2	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	12 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	. 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	l 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	V	alue	•						De	scr	iptio	on																		
Α	RW	CUSTOMER										Re	ser	ved	for	cus	tor	ner															

14.1.56 CUSTOMER[28]

Address offset: 0x0F0
Reserved for customer

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 :	20 1	19 1	18 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5 4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	A ,	4 Α	Α.	Α	Α .	Α
Re	set 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	۱ 1	1	1	1	1	1	1	1	1	1	1 1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	CUSTOMER										Res	erv	ed 1	for o	cust	tom	er															_

14.1.57 CUSTOMER[29]

Address offset: 0x0F4
Reserved for customer

Bit nu	mbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 A	A A
Reset	0xFF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1 1
ld F	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Δ [R/V/	CUSTOMER										Re	ser.	/ed	for	CHIS	tor	nor																

A RW CUSTOMER Reserved for custome

14.1.58 CUSTOMER[30]

Address offset: 0x0F8
Reserved for customer



Bit r	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 1	L4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A ,	Δ ,	۱ ۸	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	ι :	L 1	. 1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	CUSTOMER										Re	serv	ed	for	cus	ton	ner															

14.1.59 CUSTOMER[31]

Address offset: 0x0FC Reserved for customer

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	13	12	11 :	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Δ,	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	CUSTOMER										Res	erv	ed	for	cus	ton	ner																

14.1.60 PSELRESET[0]

Address offset: 0x200

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they don't, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bit	numbe	er		31 30 29 28 27 26	6 25 2	4 23 2	2 21	20 2	19 18	8 17	16	15 1	4 13	12 1	11 10	9	8	7	6	5 4	3	2	1	0
Id				В																A A	A	Α	Α	Α
Res	et 0xF	FFFFFF		1 1 1 1 1 1	. 1 1	1 1	l 1	1	1 1	. 1	1	1 1	. 1	1	1 1	1	1	1	1	1 1	. 1	1	1	1
Id	RW	Field	Value Id	Value		Desc	riptio	on																
Α	RW	PIN		21		GPIC) num	nber	P0.r	n ont	o wl	hich	Rese	t is e	expos	ed								_
В	RW	CONNECT				Conr	nectio	on																
			Disconnected	1		Disco	onne	ct																
			Connected	0		Conr	nect																	

14.1.61 PSELRESET[1]

Address offset: 0x204

Mapping of the nRESET function (see POWER chapter for details)

All PSELRESET registers have to contain the same value for a pin mapping to be valid. If they don't, there will be no nRESET function exposed on a GPIO, and the device will always start independently of the levels present on any of the GPIOs.

Bit r	iumbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		21	GPIO number P0.n onto which Reset is exposed
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

14.1.62 APPROTECT

Address offset: 0x208
Access Port protection



Bitı	numbe	r		31 30	29	28	27	26	25 2	24 2	23 2	2 21	1 20	19	18	17	16	15 :	14 1	13 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																									Α	A	Α.	A A	4 A	. A	Α
Res	et 0xF	FFFFFF		1 1	1	1	1	1	1 :	1	1 1	1 1	. 1	1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 :	1 1	1	1
Id	RW	Field	Value Id	Value						0	Desc	ript	tion																		
Α	RW	PALL								E	nat	ole o	or di	sabl	e A	cces	ss P	ort	pro	tecti	on.	٩ny	oth	er v	alu	e th	nan				
										C)xFF	bei	ng v	vritt	en	to t	his	field	l wi	ll en	able	pro	tec	tion							
										S	ee l	Deb	ug d	ind	trac	e 0	n pa	age	72 f	or n	ore	info	orm	atio	n.						
			Disabled	0xFF							Disa	ble																			
			Enabled	0x00						E	nat	ole																			

14.1.63 NFCPINS

Address offset: 0x20C

Setting of pins dedicated to NFC functionality: NFC antenna or GPIO

Bit	numbe	r		31 30 29 28	27 26 2	25 24	23 22	2 21	20 1	19 18	3 17	16 1	5 14	13 12	11	10 9	8	7	6 5	4	3	2	1 0
Id																							Α
Res	et OxF	FFFFFF		1 1 1 1	1 1	1 1	1 1	. 1	1	1 1	. 1	1 1	l 1	1 1	1	1 1	1	1	1 1	1	1	1 :	1 1
Id	RW	Field	Value Id	Value			Desc	riptio	on														
Α	RW	PROTECT					Settii	ng of	pins	s dec	dicate	d to	NFC	funct	ional	ty							
			Disabled	0			Oper	atior	n as	GPIC) pins	. Sar	ne pi	otect	ion a	nor	mal	GPIC) pin	S			
			NFC	1			Oper	atior	n as	NFC	anter	nna p	oins.	Confi	gures	the	orote	ectio	n fo	r			
							NFC	oper	atior	n													



15 Peripheral interface

Peripherals are controlled by the CPU by writing to configuration registers and task registers. Peripheral events are indicated to the CPU by event registers and interrupts if they are configured for a given event.

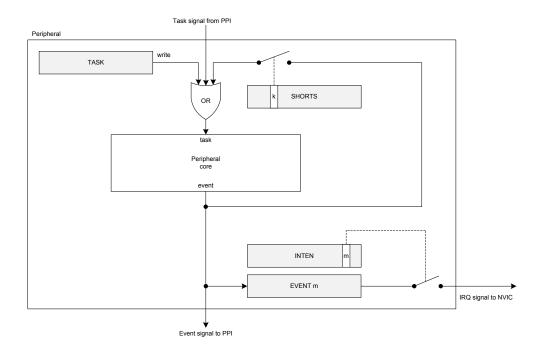


Figure 10: Tasks, events, shortcuts, and interrupts

15.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32 bit registers.

See *Instantiation* on page 24 for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between the peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Some peripherals share some registers or other common resources.
- Operation is mutually exclusive. Only one of the peripherals can be used at a time.
- Switching from one peripheral to another must follow a specific pattern (disable the first, then enable the second peripheral).

15.2 Peripherals with shared ID

In general, and with the exception of ID 0, peripherals sharing an ID and base address may not be used simultaneously. The user can only enable one at the time on this specific ID.

When switching between two peripherals that share an ID, the user should do the following to prevent unwanted behavior:

Disable the previously used peripheral



- · Remove any PPI connections set up for the peripheral that is being disabled
- Clear all bits in the INTEN register, i.e. INTENCLR = 0xFFFFFFFF.
- Explicitly configure the peripheral that you enable and do not rely on configuration values that may be inherited from the peripheral that was disabled.
- Enable the now configured peripheral.

For each of the rows in the following table, the instance ID listed is shared by the peripherals in the same row.

Table 21: Peripherals sharing an ID

Instance						
ID 2 (0x40002000)	UARTE	UART				
-						
ID 3 (0x40003000)	SPIM	SPIS	SPI	TWIM	TWIS	TWI
ID 4 (0x40004000)	SPIM	SPIS	SPI	TWIM	TWIS	TWI
ID 35 (0x40023000)	SPIM	SPIS	SPI			
-						
ID 15 (0x4000F000)	AAR	CCM				
-						
ID 19 (0x40013000)	COMP	LPCOMP				
-						
ID 20 (0x40014000)	SWI	EGU				
ID 21 (0x40015000)	SWI	EGU				
ID 22 (0x40016000)	SWI	EGU				
ID 23 (0x40017000)	SWI	EGU				
ID 24 (0x40018000)	SWI	EGU				
ID 25 (0x40019000)	SWI	EGU				

15.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified in the relevant chapter, the peripheral registers (in particular the PSEL registers) must be configured before enabling the peripheral.

Note that the peripheral must be enabled before tasks and events can be used.

15.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the "set-and-clear" pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map where the main register is followed by a dedicated SET and CLR register in that order.

The SET register is used to set individual bits in the main register while the CLR register is used to clear individual bits in the main register. Writing a '1' to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing a '0' to a bit in the SET or CLR register has no effect. Reading the SET or CLR registers returns the value of the main register.

Restriction: The main register may not be visible and hence not directly accessible in all cases.

15.5 Tasks

Tasks are used to trigger actions in a peripheral, for example, to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes a '1' to the task register or when the peripheral itself or another peripheral toggles the corresponding task signal. See *Figure 10: Tasks, events, shortcuts, and interrupts* on page 68.



15.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example, a state change in a peripheral. A peripheral may generate multiple events with each event having a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated. See *Figure 10: Tasks, events, shortcuts, and interrupts* on page 68. An event register is only cleared when firmware writes a '0' to it.

Events can be generated by the peripheral even when the event register is set to '1'.

15.7 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, its associated task is automatically triggered when its associated event is generated.

Using a shortcut is the equivalent to making the same connection outside the peripheral and through the PPI. However, the propagation delay through the shortcut is usually shorter than the propagation delay through the PPI.

Shortcuts are predefined, which means their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

15.8 Interrupts

All peripherals support interrupts. Interrupts are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the Nested Vectored Interrupt Controller (NVIC).

Using the INTEN, INTENSET and INTENCLR registers, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR, and the INTEN register is not available on those peripherals. Refer to the individual chapters for details. In all cases, however, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is shown in *Figure 10: Tasks, events, shortcuts, and interrupts* on page 68.

15.8.1 Interrupt clearing

When clearing an interrupt by writing "0" to an event register, or disabling an interrupt using the INTENCLR register, it can take up to four CPU clock cycles to take effect. This means that an interrupt may reoccur immediatelly even if a new event has not come, if the program exits an interrupt handler after the interrupt is cleared or disabled, but before four clock cycles have passed.

Important: To avoid an interrupt reoccurring before a new event has come, the program should perform a read from one of the peripheral registers, for example, the event register that has been cleared, or the INTENCLR register that has been used to disable the interrupt.

This will cause a one to three-cycle delay and ensure the interrupt is cleared before exiting the interrupt handler. Care should be taken to ensure the compiler does not remove the read operation as an optimization. If the program can guarantee a four-cycle delay after event clear or interrupt disable another way, then a read of a register is not required.





16 Debug and trace

The debug and trace system offers a flexible and powerful mechanism for non-intrusive debugging.

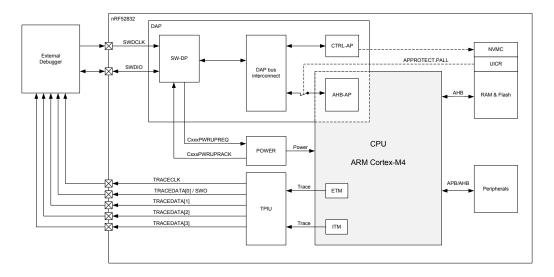


Figure 11: Debug and trace overview

The main features of the debug and trace system are:

- Two-pin Serial Wire Debug (SWD) interface
- Flash Patch and Breakpoint Unit (FPB) supports:
 - Two literal comparators
 - Six instruction comparators
- Data Watchpoint and Trace Unit (DWT)
 - Four comparators
- Instrumentation Trace Macrocell (ITM)
- Embedded Trace Macrocell (ETM)
- Trace Port Interface Unit (TPIU)
 - · 4-bit parallel trace of ITM and ETM trace data
 - · Serial Wire Output (SWO) trace of ITM data

16.1 DAP - Debug Access Port

An external debugger can access the device via the DAP.

The DAP implements a standard ARM® CoreSight™ Serial Wire Debug Port (SW-DP).

The SW-DP implements the Serial Wire Debug protocol (SWD) that is a two-pin serial interface, see SWDCLK and SWDIO in *Figure 11: Debug and trace overview* on page 72.

In addition to the default access port in the CPU (AHB-AP), the DAP includes a custom Control Access Port (CTRL-AP). The CTRL-AP is described in more detail in CTRL-AP - Control Access Port on page 73.

Important:

- The SWDIO line has an internal pull-up resistor.
- The SWDCLK line has an internal pull-down resistor.



16.2 CTRL-AP - Control Access Port

The Control Access Port (CTRL-AP) is a custom access port that enables control of the device even if the other access ports in the DAP are being disabled by the access port protection.

Access port protection blocks the debugger from read and write access to all CPU registers and memory-mapped addresses. See the UICR register *APPROTECT* on page 66 for more information about enabling access port protection.

This access port enables the following features:

- Soft reset, see Reset on page 82 for more information
- Disable access port protection

Access port protection can only be disabled by issuing an ERASEALL command via CTRL-AP. This command will erase the Flash, UICR, and RAM.

16.2.1 Registers

Table 22: Register Overview

Register	Offset	Description
RESET	0x000	Soft reset triggered through CTRL-AP
ERASEALL	0x004	Erase all
ERASEALLSTATUS	0x008	Status register for the ERASEALL operation
APPROTECTSTATUS	0x00C	Status register for access port protection
IDR	0x0FC	CTRL-AP Identification Register, IDR

RESET

Address offset: 0x000

Soft reset triggered through CTRL-AP

Bit r	umber		31 3	29	28	27	26	25	24	23	22	21 2	20 1	9 1	8 1	l7 1	6 1	.5 1	.4 1	3 12	2 1:	1 10	9	8	7	6	5	4	3 2	2 1	. 0
Id																															Α
Rese	et 0x00000000		0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0 (0 (0 (0 (0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW Field	Value Id	Valu	9						De	scrip	otio	n																		
Α	RW RESET									Sof	t re	set	trig	gere	ed t	thro	ugl	h C	ΓRL	AP.	See	e Re	set	Beh	avi	our	in				
										РО	WE	R ch	apt	er f	or i	mor	e d	eta	ils.												
		NoReset	0							Res	set i	s no	t ac	ctive	е																
		Reset	1							Res	set i	s ac	tive	. De	evic	e is	he	ld i	n re	set											

ERASEALL

Address offset: 0x004

Erase all

Bit	numbe	er		3	1 30	29	9 28	3 27	7 26	5 2	5 24	4 2	3 2	2 2	1 2	20 2	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0 0) (0 (0 (כ	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	9						D	eso	crip	tio	n																			
Α	W	ERASEALL										Ε	ras	e al	ΙFΙ	LAS	На	nd	RA	M															
			NoOperation	0								N	lo c	pei	rati	ion																			
			Erase	1								Ε	ras	e al	ΙFΙ	LAS	На	nd	RA	М															

ERASEALLSTATUS

Address offset: 0x008

Status register for the ERASEALL operation



Bitı	numbe	er		31 30	29	28	27	26	25	24	23	22	21	20	19	18 1	.7 1	.6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id																																Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Valu	е						Des	scri	ptic	on																		
Α	R	ERASEALLSTATUS									Sta	tus	reg	iste	r fo	r th	e E	RAS	EAL	L op	era	tior	1									
			Ready	0							ER/	ASE	ALL	is r	ead	ly																
			Busy	1							ER/	ASE	ALL	is b	usy	(or	n-gc	oing)													

APPROTECTSTATUS

Address offset: 0x00C

Status register for access port protection

Bit	numl	per		31 30 29 28	27 26	5 25 2	24 2	3 22 2	21 20	19	18	17 :	16 1	5 14	13	12 1	1 10	9	8	7	6	5 4	4 3	2	1 0
Id																									Α
Res	et 0	00000000		0 0 0 0	0 0	0	0 0	0	0 0	0	0	0	0 0	0	0	0	0 0	0	0	0	0	0	0 0	0	0 0
Id	RV	/ Field	Value Id	Value			D	escrip	otion																
Α	R	APPROTECTS	STATUS				St	atus	regis	ter f	or a	cces	ss po	rt p	rote	ctio	า								
			Enabled	0			Α	ccess	port	pro	tecti	on	enab	led											
			Disabled	1			Α	ccess	port	pro	tecti	on	not e	nat	oled										

IDR

Address offset: 0x0FC

CTRL-AP Identification Register, IDR

Bit r	iumbe	er		31	30	29	28 2	7 2	6 25	24	1 23	3 22 :	21 2	20 1	L9 1	8 1	7 16	5 15	14	13 3	2 1	1 10	9	8 7	6	5	4	3	2 :	1 0
Id				Ε	Ε	Ε	Е [) (D D	D	С	С	С	С	C (2 (СВ	В	В	В				Α	Α	Α	Α	Α	A A	4 А
Res	et 0x0	2880000		0	0	0	0 () (0 1	0	1	0	0	0	1 (0 (0 0	0	0	0	0 0	0	0	0 0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						De	escrip	otio	n																
Α	R	APID									AF	lde:	ntifi	cati	ion															
В	R	CLASS									Ac	cess	Por	t (A	AP) c	las	S													
			NotDefined	0x	0						No	o def	ined	d cla	ass															
			MEMAP	0x	8						М	emo	ry A	cce	ss P	ort														
С	R	JEP106ID									JE	DEC.	JEP1	106	ide	ntit	у со	de												
D	R	JEP106CONT									JE	DEC.	JEP1	106	con	tin	uatio	on c	ode											
Ε	R	REVISION									Re	visio	n																	

16.3 Debug interface mode

Before the external debugger can access the CPU's access port (AHB-AP) or the Control Access Port (CTRL-AP), the debugger must first request the device to power up via CxxxPWRUPREQ in the SWJ-DP.

As long as the debugger is requesting power via CxxxPWRUPREQ, the device will be in debug interface mode. If the debugger is not requesting power via CxxxPWRUPREQ, the device will be in normal mode.

Some peripherals will behave differently in debug interface mode compared to normal mode. These differences are described in more detail in the chapters of the peripherals that are affected.

When a debug session is over, the external debugger must make sure to put the device back into normal mode since the overall power consumption will be higher in debug interface mode compared to normal mode.

For details on how to use the debug capabilities please read the debug documentation of your IDE.

If the device is in System OFF when power is requested via CxxxPWRUPREQ, the system will wake up and the DIF flag in *RESETREAS* on page 85 will be set.

16.4 Real-time debug

The nRF52832 supports real-time debugging.



Real-time debugging will allow interrupts to execute to completion in real time when breakpoints are set in Thread mode or lower priority interrupts. This enables the developer to set a breakpoint and single-step through their code without a failure of the real-time event-driven threads running at higher priority. For example, this enables the device to continue to service the high-priority interrupts of an external controller or sensor without failure or loss of state synchronization while the developer steps through code in a low-priority thread.

16.5 Trace

The device supports ETM and ITM trace.

Trace data from the ETM and the ITM is sent to an external debugger via a 4-bit wide parallel trace port (TPIU), see TRACEDATA[0] through TRACEDATA[3] and TRACECLK in *Figure 11: Debug and trace overview* on page 72.

In addition to parallel trace, the TPIU supports serial trace via the Serial Wire Output (SWO) trace protocol.

Parallel and serial trace cannot be used at the same time.

ETM trace is only supported in parallel trace mode while ITM trace is supported in both parallel and serial trace modes.

For details on how to use the trace capabilities, please read the debug documentation of your IDE.

TPIU's trace pins are multiplexed with GPIOs, and SWO and TRACEDATA[0] use the same GPIO, see *Pin assignments* on page 13 for more information.

Trace speed is configured in the *TRACECONFIG* on page 108 register.

The speed of the trace pins depends on the DRIVE setting of the GPIOs that the trace pins are multiplexed with, see *PIN_CNF[14]* on page 142, *PIN_CNF[15]* on page 143, *PIN_CNF[16]* on page 144, *PIN_CNF[18]* on page 145 and *PIN_CNF[20]* on page 146. Only S0S1 and H0H1 drives are suitable for debugging. S0S1 is the default DRIVE at reset. If parallel or serial trace port signals are not fast enough in the debugging conditions, all GPIOs in use for tracing should be set to high drive (H0H1). The user shall make sure that these GPIOs' DRIVE is not overwritten by software during the debugging session.

16.5.1 Electrical specification

Trace port

Symbol	Description	Min.	Тур.	Max.	Units
T_{cyc}	Clock period, as defined by ARM (See ARM Infocenter,	62.5		500	ns
	Embedded Trace Macrocell Architecture Specification, Trace				
	Port Physical Interface, Timing specifications)				



17 Power and clock management

Power and clock management in nRF52832 is optimized for ultra-low power applications.

The core of the power and clock management system is the Power Management Unit (PMU) illustrated in *Figure 12: Power Management Unit* on page 76.

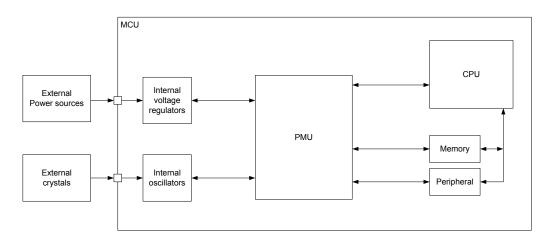


Figure 12: Power Management Unit

The user application is not required to actively control power and clock, since the PMU is able to automatically detect which resources are required by the different components in the system at any given time. The PMU will continuously optimize the system based on this information to achieve the lowest power consumption possible without user interaction.

17.1 Current consumption scenarios

As the system is being constantly tuned by the PMU, estimating the energy consumption of an application can be challenging if the designer is not able to do measurements on the hardware directly. See *Electrical specification* on page 76 for application scenarios showing average current drawn from the VDD supply.

Each scenario specifies a set of active operations and conditions applying to the given scenario. *Table 23: Current consumption scenarios, common conditions* on page 76 shows the conditions used for a scenario unless otherwise is stated in the scenario description.

Table 23: Current consumption scenarios, common conditions

Condition	Value
VDD	3 V
Temperature	25°C
CPU	WFI/WFE sleep
Peripherals	All idle
Clock	Not running
Clock Regulator	DCDC

17.1.1 Electrical specification

Current consumption: Radio

			_			
Symbol	Description	Min.	Тур.	Max.	Units	
I _{RADIO_TX0}	0 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		7.1		mA	
I _{RADIO_TX1}	-40 dBm TX @ 1 Mb/s Bluetooth Low Energy mode, Clock =		4.1		mA	
	HFXO					
I _{RADIO RX0}	Radio RX @ 1 Mb/s Bluetooth Low Energy mode, Clock = HFXO		6.5		mA	



Current consumption: Radio protocol configurations

Symbol	Description	Min.	Тур.	Max.	Units
I _{SO}	CPU running CoreMark from Flash, Radio 0 dBm TX @ 1 Mb/s		9.2		mA
	Bluetooth Low Energy mode, Clock = HFXO, Cache enabled				
I _{S1}	CPU running CoreMark from Flash, Radio RX @ 1 Mb/s		9.2		mA
	Bluetooth Low Energy mode, Clock = HFXO, Cache enabled				

Current consumption: Ultra-low power

Symbol	Description	Min.	Тур.	Max.	Units
I _{ON_RAMOFF_EVENT}	System ON, No RAM retention, Wake on any event		1.2		μΑ
I _{ON_RAMON_EVENT}	System ON, Full RAM retention, Wake on any event		1.5		μΑ
I _{ON_RAMOFF_RTC}	System ON, No RAM retention, Wake on RTC		1.9		μΑ
I _{OFF_RAMOFF_RESET}	System OFF, No RAM retention, Wake on reset		0.3		μΑ
I _{OFF_RAMOFF_GPIO}	System OFF, No RAM retention, Wake on GPIO		0.3		μΑ
I _{OFF_RAMOFF_LPCOMP}	System OFF, No RAM retention, Wake on LPCOMP		1.9		μΑ
I _{OFF_RAMOFF_NFC}	System OFF, No RAM retention, Wake on NFC field		0.7		μΑ
I _{OFF_RAMON_RESET}	System OFF, Full 64 kB RAM retention, Wake on reset		0.7		μΑ



18 POWER — Power supply

This device has the following power supply features:

- On-chip LDO and DC/DC regulators
- Global System ON/OFF modes
- Individual RAM section power control for all system modes
- Analog or digital pin wakeup from System OFF
- · Supervisor HW to manage power on reset, brownout, and power fail
- Auto-controlled refresh modes for LDO and DC/DC regulators to maximize efficiency
- Automatic switching between LDO and DC/DC regulator based on load to maximize efficiency

Note: Two additional external passive components are required to use the DC/DC regulator.

18.1 Regulators

The following internal power regulator alternatives are supported:

- Internal LDO regulator
- Internal DC/DC regulator

The LDO is the default regulator.

The DC/DC regulator can be used as an alternative to the LDO regulator and is enabled through the DCDCEN on page 88 register. Using the DC/DC regulator will reduce current consumption compared to when using the LDO regulator, but the DC/DC regulator requires an external LC filter to be connected, as shown in *Figure 14: DC/DC regulator setup* on page 79.

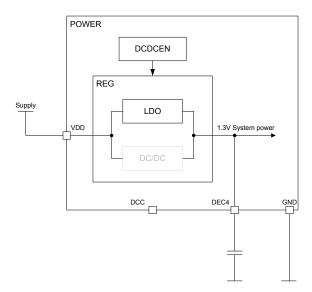


Figure 13: LDO regulator setup



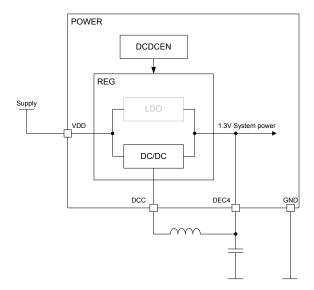


Figure 14: DC/DC regulator setup

18.2 System OFF mode

System OFF is the deepest power saving mode the system can enter. In this mode, the system's core functionality is powered down and all ongoing tasks are terminated.

The device can be put into System OFF mode using the POWER register interface. When in System OFF mode, the device can be woken up through one of the following signals:

- 1. The DETECT signal, optionally generated by the GPIO peripheral
- 2. The ANADETECT signal, optionally generated by the LPCOMP module
- 3. The SENSE signal, optionally generated by the NFC module to "wake-on-field"
- 4. A reset

When the system wakes up from System OFF mode, it gets reset. For more details, see *Reset behavior* on page 83.

One or more RAM sections can be retained in System OFF mode depending on the settings in the RAM[n].POWER registers.

RAM[n].POWER are retained registers, see *Reset behavior*. Note that these registers are usually overwritten by the startup code provided with the nRF application examples.

Before entering System OFF mode, the user must make sure that all on-going EasyDMA transactions have been completed. This is usually accomplished by making sure that the EasyDMA enabled peripheral is not active when entering System OFF.

18.2.1 Emulated System OFF mode

If the device is in debug interface mode, System OFF will be emulated to secure that all required resources needed for debugging are available during System OFF.

See *Debug and trace* on page 72 for more information. Required resources needed for debugging include the following key components: *Debug and trace* on page 72, *CLOCK* — *Clock control* on page 101, *POWER* — *Power supply* on page 78, *NVMC* — *Non-volatile memory controller* on page 29, CPU, Flash, and RAM. Since the CPU is kept on in an emulated System OFF mode, it is recommended to add an infinite loop directly after entering System OFF, to prevent the CPU from executing code that normally should not be executed.



18.3 System ON mode

System ON is the default state after power-on reset. In System ON, all functional blocks such as the CPU or peripherals, can be in IDLE or RUN mode, depending on the configuration set by the software and the state of the application executing.

Register *RESETREAS* on page 85 provides information about the source that caused the wakeup or reset.

The system can switch on and off the appropriate internal power sources, depending on how much power is needed at any given time. The power requirement of a peripheral is directly related to its activity level, and the activity level of a peripheral is usually raised and lowered when specific tasks are triggered or events are generated.

18.3.1 Sub power modes

In System ON mode, when both the CPU and all the peripherals are in IDLE mode, the system can reside in one of the two sub power modes.

The sub power modes are:

- Constant latency
- · Low power

In constant latency mode the CPU wakeup latency and the PPI task response will be constant and kept at a minimum. This is secured by forcing a set of base resources on while in sleep. The advantage of having a constant and predictable latency will be at the cost of having increased power consumption. The constant latency mode is selected by triggering the CONSTLAT task.

In low power mode the automatic power management system, described in *System ON mode* on page 80, ensures the most efficient supply option is chosen to save the most power. The advantage of having the lowest power possible will be at the cost of having varying CPU wakeup latency and PPI task response. The low power mode is selected by triggering the LOWPWR task.

When the system enters System ON mode, it will, by default, reside in the low power sub-power mode.

18.4 Power supply supervisor

The power supply supervisor initializes the system at power-on and provides an early warning of impending power failure.

In addition, the power supply supervisor puts the system in a reset state if the supply voltage is too low for safe operation (brownout). The power supply supervisor is illustrated in *Figure 15: Power supply supervisor* on page 81.



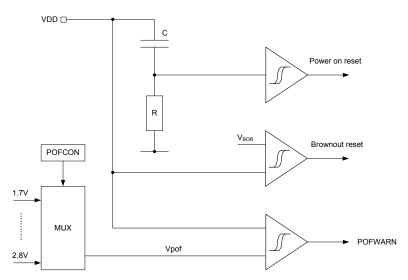


Figure 15: Power supply supervisor

18.4.1 Power-fail comparator

The power-fail comparator (POF) can provide the CPU with an early warning of impending power failure. It will not reset the system, but give the CPU time to prepare for an orderly power-down.

The comparator features a hysteresis of V_{HYST} , as illustrated in *Figure 16: Power-fail comparator (BOR = Brownout reset)* on page 81. The threshold V_{POF} is set in register *POFCON* on page 86. If the POF is enabled and the supply voltage falls below V_{POF} , the POFWARN event will be generated. This event will also be generated if the supply voltage is already below V_{POF} at the time the POF is enabled, or if V_{POF} is reconfigured to a level above the supply voltage.

If power-fail warning is enabled and the supply voltage is below V_{POF} the power-fail comparator will prevent the NVMC from performing write operations to the NVM. See NVMC - Non-volatile memory controller on page 29 for more information about the NVMC.

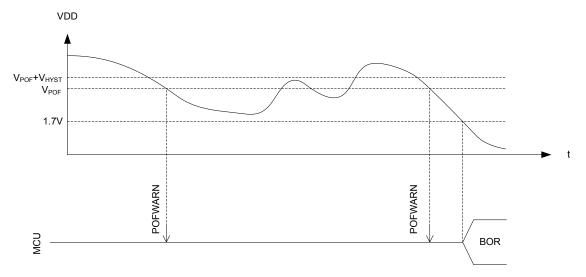


Figure 16: Power-fail comparator (BOR = Brownout reset)

To save power, the power-fail comparator is not active in System OFF or in System ON when HFCLK is not running.



18.5 RAM sections

RAM section power control is used for retention in System OFF mode and for powering down unused sections in System ON mode.

Each RAM section can power up and down independently in both System ON and System OFF mode. See chapter *Memory* on page 23 for more information on RAM sections.

18.6 Reset

There are multiple sources that may trigger a reset.

After a reset has occurred, register *RESETREAS* can be read to determine which source generated the reset.

18.6.1 Power-on reset

The power-on reset generator initializes the system at power-on.

The system is held in reset state until the supply has reached the minimum operating voltage and the internal voltage regulators have started.

A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

18.6.2 Pin reset

A pin reset is generated when the physical reset pin on the device is asserted.

Pin reset is configured via the *PSELRESET[0]* and *PSELRESET[1]* registers.

Note: Pin reset is not available on all pins.

18.6.3 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

The DAP is not reset following a wake up from System OFF mode if the device is in debug interface mode. Refer to chapter *Debug and trace* on page 72 for more information.

18.6.4 Soft reset

A soft reset is generated when the SYSRESETREQ bit of the Application Interrupt and Reset Control Register (AIRCR register) in the ARM® core is set.

Refer to ARM documentation for more details.

A soft reset can also be generated via the RESET on page 73 register in the CTRL-AP.

18.6.5 Watchdog reset

A Watchdog reset is generated when the watchdog times out.

Refer to chapter WDT — Watchdog timer on page 409 for more information.

18.6.6 Brown-out reset

The brown-out reset generator puts the system in reset state if the supply voltage drops below the brownout reset (BOR) threshold.

Refer to section *Power fail comparator* on page 99 for more information.



18.7 Retained registers

A retained register is a register that will retain its value in System OFF mode and through a reset, depending on reset source. See individual peripheral chapters for information of which registers are retained for the various peripherals.

18.8 Reset behavior

Reset source	Reset target CPU	Peripherals	GPIO	Debug ^a	SWJ-DP	RAM	WDT	Retained registers	RESETREAS
CPU lockup ⁶	x	х	x						
Soft reset	x	Х	x						
Wakeup from System OFF mode reset	х	x		x ⁷		x ⁸			
Watchdog reset ⁹	X	X	X	х		х	x	x	
Pin reset	x	x	x	x		x	x	x	
Brownout reset	x	x	x	x	x	x	x	x	x
Power on reset	х	х	х	х	х	х	X	х	х

Note: The RAM is never reset, but depending on reset source, RAM content may be corrupted.

18.9 Registers

Table 24: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40000000	POWER	POWER	Power control		

Table 25: Register Overview

Register	Offset	Description	
TASKS_CONSTLAT	0x078	Enable constant latency mode	
TASKS_LOWPWR	0x07C	Enable low power mode (variable latency)	
EVENTS_POFWARN	0x108	Power failure warning	
EVENTS_SLEEPENTER	0x114	CPU entered WFI/WFE sleep	
EVENTS_SLEEPEXIT	0x118	CPU exited WFI/WFE sleep	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
RESETREAS	0x400	Reset reason	
RAMSTATUS	0x428	RAM status register	Deprecated
SYSTEMOFF	0x500	System OFF register	
POFCON	0x510	Power failure comparator configuration	
GPREGRET	0x51C	General purpose retention register	
GPREGRET2	0x520	General purpose retention register	
RAMON	0x524	RAM on/off register (this register is retained)	Deprecated
RAMONB	0x554	RAM on/off register (this register is retained)	Deprecated
DCDCEN	0x578	DC/DC enable register	
RAM[0].POWER	0x900	RAM0 power control register	

^a All debug components excluding SWJ-DP. See *Debug and trace* on page 72 chapter for more information about the different debug components in the system.

⁶ Reset from CPU lockup is disabled if the device is in debug interface mode. CPU lockup is not possible in System OFF.

⁷ The Debug components will not be reset if the device is in debug interface mode.

RAM is not reset on wakeup from OFF mode, but depending on settings in the RAM register parts, or the whole RAM, may not be retained after the device has entered System OFF mode.

⁹ Watchdog reset is not available in System OFF.



Register	Offset	Description
RAM[0].POWERSET	0x904	RAM0 power control set register
RAM[0].POWERCLR	0x908	RAM0 power control clear register
RAM[1].POWER	0x910	RAM1 power control register
RAM[1].POWERSET	0x914	RAM1 power control set register
RAM[1].POWERCLR	0x918	RAM1 power control clear register
RAM[2].POWER	0x920	RAM2 power control register
RAM[2].POWERSET	0x924	RAM2 power control set register
RAM[2].POWERCLR	0x928	RAM2 power control clear register
RAM[3].POWER	0x930	RAM3 power control register
RAM[3].POWERSET	0x934	RAM3 power control set register
RAM[3].POWERCLR	0x938	RAM3 power control clear register
RAM[4].POWER	0x940	RAM4 power control register
RAM[4].POWERSET	0x944	RAM4 power control set register
RAM[4].POWERCLR	0x948	RAM4 power control clear register
RAM[5].POWER	0x950	RAM5 power control register
RAM[5].POWERSET	0x954	RAM5 power control set register
RAM[5].POWERCLR	0x958	RAM5 power control clear register
RAM[6].POWER	0x960	RAM6 power control register
RAM[6].POWERSET	0x964	RAM6 power control set register
RAM[6].POWERCLR	0x968	RAM6 power control clear register
RAM[7].POWER	0x970	RAM7 power control register
RAM[7].POWERSET	0x974	RAM7 power control set register
RAM[7].POWERCLR	0x978	RAM7 power control clear register

18.9.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW POFWARN		Write '1' to Enable interrupt for POFWARN event
		See EVENTS_POFWARN
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
B RW SLEEPENTER		Write '1' to Enable interrupt for SLEEPENTER event
		See EVENTS_SLEEPENTER
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
C RW SLEEPEXIT		Write '1' to Enable interrupt for SLEEPEXIT event
		See EVENTS_SLEEPEXIT
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled

18.9.2 INTENCLR

Address offset: 0x308 Disable interrupt



Bit number			31 3	30 29	9 28	27 2	26 25	5 24	23 2	2 21	1 20	19	18	17 1	6 1	5 14	1 13	12	11 1	0 9	8	7	6 5	4	3	2 1	. 0
Id																							СВ		,	Д	
Reset 0x00	000000		0	0 0	0	0	0 0	0	0 (0	0	0	0	0 (0 (0	0	0	0 (0	0	0	0 0	0	0 (0 0	0
Id RW	Field	Value Id	Valu	ıe					Desc	ript	ion																
A RW	POFWARN								Writ	e '1'	to [Disab	ble	intei	rrup	t fo	r PO	FW.	ARN	evei	nt						
									See	EVE	NTS_	POF	FW/	ARN													
		Clear	1						Disal	ble																	
		Disabled	0						Read	l: Di	sabl	ed															
		Enabled	1						Read	l: En	nable	ed															
B RW	SLEEPENTER								Writ	e '1'	to [Disal	ble i	intei	rrup	t fo	r SLE	EPE	NTE	R ev	ent						
									See	EVE	NTS_	SLE	EPE	NTE	R												
		Clear	1						Disal	ble																	
		Disabled	0						Read	l: Di	sabl	ed															
		Enabled	1						Read	l: En	nable	ed															
C RW	SLEEPEXIT								Writ	e '1'	to [Disab	ble i	intei	rrup	t fo	r SLE	EPE	XIT	ever	t						
									See	EVEI	NTS_	SLE	EPE	XIT													
		Clear	1						Disal	ble																	
		Disabled	0						Read	l: Di	sabl	ed															
		Enabled	1						Read	l: En	nable	ed															

18.9.3 RESETREAS

Address offset: 0x400

Reset reason

Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing '1' to it. If none of the reset sources are flagged, this indicates that the chip was reset from the on-chip reset generator, which will indicate a power-on-reset or a brownout reset.

Bit r	numbe	er		31 3	0 29	28 2	27 2	6 2	5 24	4 23	3 22	21 2	20 19	18	3 17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5 4	1 3	2	1 ()
Id													Н	G	F	Ε											D	С	В	1
Res	et 0x0	0000000		0 0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0 ()
Id	RW	Field	Value Id	Valu	e					De	escri	iptio	n																	ı
Α	RW	RESETPIN								Re	eset	fron	n pin-	res	et c	lete	cted													
			NotDetected	0						No	ot de	etect	ted																	
			Detected	1						De	etec	ted																		
В	RW	DOG								Re	eset	fron	n wat	cho	gob	det	ecte	d												
			NotDetected	0						No	ot de	etect	ted																	
			Detected	1						De	etec	ted																		
С	RW	SREQ								Re	eset	fron	n soft	re	set	dete	ecte	b												
			NotDetected	0						No	ot de	etect	ted																	
			Detected	1						De	etec	ted																		
D	RW	LOCKUP								Re	eset	fron	n CPU	J lo	ck-ι	ıp d	etec	ted												
			NotDetected	0						No	ot de	etect	ted																	
			Detected	1						De	etec	ted																		
Ε	RW	OFF								Re	eset	due	to wa	ake	up	froi	n Sy	ste	m C	FF n	nod	e wh	nen	wal	eup	is				
										tri	igge	red f	rom	DE.	TEC	T sig	nal	fror	n G	PIO										
			NotDetected	0						No	ot de	etect	ted																	
			Detected	1						De	etec	ted																		
F	RW	LPCOMP								Re	eset	due	to wa	ake	up	froi	n Sy	ste	m C	FF n	nod	e wh	nen	wal	eup	is				
										tri	igge	red f	rom	AN.	ADE	TEC	T sig	gnal	l fro	m L	PCO	MP								
			NotDetected	0						No	ot de	etect	ted																	
			Detected	1						De	etec	ted																		
G	RW	DIF								Re	eset	due	to wa	ake	up	froi	n Sy	ste	m C	FF n	nod	e wh	nen	wal	eup	is				
										tri	igge	red f	rom	ent	erir	ng ir	to d	lebu	ug ir	nterf	ace	mod	de							
			NotDetected	0						No	ot de	etect	ted																	
			Detected	1						De	etec	ted																		



Bit r	numbe	r		33	1 30	29	28	3 27	7 26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id																Н	G	F	Ε													D C	С Е	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	V	alue	:						De	escri	ptic	on																			
Н	RW	NFC										Re	set	due	to	wa	ke	up	fro	m S	yste	em	OFF	mo	ode	by	NF	C fie	eld					
												de	tect																					
			NotDetected	0								No	ot de	etec	tec	t																		
			Detected	1								De	etec	ted																				

18.9.4 RAMSTATUS (Deprecated)

Address offset: 0x428 RAM status register

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM1.S0, RAM block 1 is equivalent to a block comprising RAM2.S0 and RAM3.S0, RAM block 2 is equivalent to a block comprising RAM4.S0 and RAM5.S0 and RAM block 3 is equivalent to a block comprising RAM6.S0 and RAM7.S0. A RAM block field will indicate ON as long as any of the RAM sections associated with a block are on.

Bit r	numbe	er		31	30 2	9 28	3 27	26	25	24	23 2	2 2	21 20	0 1	9 18	3 17	7 16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																												ı	ОС	В	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0 (0	0 0	•	0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 0	0	0
Id	RW	Field	Value Id	Va	lue						Desc	crip	tion																		
Α	R	RAMBLOCK0									RAN	1 bl	ock (0 is	on	or	off/	pow	/erii	ng u)										
			Off	0							Off																				
			On	1							On																				
В	R	RAMBLOCK1									RAN	1 bl	ock :	1 is	on	or	off/	pow	/erii	ng u)										
			Off	0							Off																				
			On	1							On																				
С	R	RAMBLOCK2									RAN	1 bl	ock :	2 is	on	or	off/	pow	/erii	ng u)										
			Off	0							Off																				
			On	1							On																				
D	R	RAMBLOCK3									RAN	1 bl	ock :	3 is	on	or	off/	pow	/erii	ng u)										
			Off	0							Off																				
			On	1							On																				

18.9.5 SYSTEMOFF

Address offset: 0x500 System OFF register

Bit	numb	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A
Re	set 0x(00000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	D\A/	Field	Value Id	Malica	Description
·u	17.00	rieid	value iu	Value	Description
A	W	SYSTEMOFF	value id	value	Enable System OFF mode

18.9.6 POFCON

Address offset: 0x510

Power failure comparator configuration

Bit r	umb	er		31 30 29 28 27	26	25 24	23 :	22 2	1 20	19	18 17	7 16	5 15	14	L3 1	2 11	10	9	8 7	' 6	5	4	3	2 1	0
Id																						В	В	в в	Α
Rese	et OxC	0000000		0 0 0 0 0	0	0 0	0	0 (0 0	0	0 0	0	0	0	0	0 0	0	0	0 0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Value			Des	crip	tion																
Α	RW	POF					Ena	ble	or di	sable	pov	ver	failu	re c	omp	arat	or								
			Disabled	0			Disa	able																	



Bit	numbe	er		31 30 29 28 27 26 25 24	\$\frac{1}{2}\$ 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					вввва
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
			Enabled	1	Enable
В	RW	THRESHOLD			Power failure comparator threshold setting
			V17	4	Set threshold to 1.7 V
			V18	5	Set threshold to 1.8 V
			V19	6	Set threshold to 1.9 V
			V20	7	Set threshold to 2.0 V
			V21	8	Set threshold to 2.1 V
			V22	9	Set threshold to 2.2 V
			V23	10	Set threshold to 2.3 V
			V24	11	Set threshold to 2.4 V
			V25	12	Set threshold to 2.5 V
			V26	13	Set threshold to 2.6 V
			V27	14	Set threshold to 2.7 V
			V28	15	Set threshold to 2.8 V

18.9.7 GPREGRET

Address offset: 0x51C

General purpose retention register

Bit	numbe	er		31	30	29	28	27 2	6 2	25 2	4 2	3 2	2 21	20	19	18	17	16	15 1	4 1	3 12	11	10 9	9 8	7	6	5	4	3 2	1	. 0
Id																									Α	Α	Α	Α	A A	. Δ	A A
Res	et 0x0	0000000		0	0	0	0	0 (0 (0 (0 (0 (0	0	0	0	0	0	0 (0 0	0	0	0 (0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						C	esc	ript	ion																	
Α	RW	GPREGRET									G	ien	eral	pur	pos	e re	tent	tion	reg	iste											

This register is a retained register

18.9.8 GPREGRET2

Address offset: 0x520

General purpose retention register

Bit r	numbe	r		31	30 2	29 2	28 2	7 26	25	24	23	22	21 :	20 :	19 1	18 :	17 :	16	15 1	.4 1	3 12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id																										Α	Α	Α	Α	A A	. A	A A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	lue						Des	cri	ptio	n																		
Α	RW	GPREGRET									Ger	nera	al pi	urp	ose	ret	ent	ion	reg	iste	r											

This register is a retained register

18.9.9 RAMON (Deprecated)

Address offset: 0x524

RAM on/off register (this register is retained)

Since this register is deprecated the following substitutions have been made: RAM block 0 is equivalent to a block comprising RAM0.S0 and RAM0.S1 and RAM block 1 is equivalent to a block comprising RAM1.S0 and RAM1.S1. For new designs it is recommended to use the POWER.RAM-0.POWER and its sibling registers instead.

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C
Reset 0x00000003		0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW ONRAMO			Keep RAM block 0 on or off in system ON Mode
	RAMOOff	0	Off



9876543210
7670343210
ВА
0 0 0 0 0 0 0 1 1
2
ck is switched off
ck is switched off

18.9.10 RAMONB (Deprecated)

Address offset: 0x554

RAM on/off register (this register is retained)

Since this register is deprecated the following substitutions have been made: RAM block 2 is equivalent to a block comprising RAM2.S0 and RAM2.S1 and RAM block 3 is equivalent to a block comprising RAM3.S0 and RAM3.S1. For new designs it is recommended to use the POWER.RAM-0.POWER and its sibling registers instead.

Bit r	numbe	er		31	30 29	9 2	8 27	7 26	5 25	24	23 2	22	21 20	0 1	.9 18	3 17	7 16	15	14	13	12 :	11 1	.0 9	9 8	7	6	5	4	3 2	1	0
Id																D	С													В	Α
Res	et 0x0	0000003		0	0 0	(0 0	0	0	0	0	0	0 0) (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 0	1	1
Id	RW	Field	Value Id	Va	lue						Des	cri	ption	,																	
Α	RW	ONRAM2									Kee	p R	AM I	blo	ck 2	on	or o	off i	n sy	ster	n O	N M	lode	è							
			RAM2Off	0							Off																				
			RAM2On	1							On																				
В	RW	ONRAM3									Kee	p R	AM I	blo	ck 3	on	or o	off i	n sy	ster	n O	N M	lode	9							
			RAM3Off	0							Off																				
			RAM3On	1							On																				
С	RW	OFFRAM2									Kee	p r	etent	tio	n on	RA	Μb	loc	k 2 v	whe	n R	MΑ	blo	k is	swi	tche	ed o	ff			
			RAM2Off	0							Off																				
			RAM2On	1							On																				
D	RW	OFFRAM3									Kee	p r	etent	tio	n on	RA	M b	loc	k 3 v	whe	n R	MΑ	blo	k is	swi	tche	ed o	ff			
			RAM3Off	0							Off																				
			RAM3On	1							On																				

18.9.11 DCDCEN

Address offset: 0x578 DC/DC enable register

Bitı	numbe	er		3	1 30	29	9 28	8 2	7 2	26	25 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	٧	alu	е							Des	scri	pti	on																			
Α	RW	DCDCEN											Ena	ble	or	dis	abl	e D)C/E	OC o	onv	/ert	er												
			Disabled	0									Disa	able	е																				
			Enabled	1									Ena	ble	•																				

18.9.12 RAM[0].POWER

Address offset: 0x900

RAM0 power control register



Bit n	umbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Rese	t 0x0	000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	SOPOWER			Keep RAM section S0 ON or OFF in System ON mode.
					RAM sections are always retained when ON, but can also be
					retained when OFF dependent on the settings in SORETENTION.
					All RAM sections will be OFF in System OFF mode.
			Off	0	Off
			On	1	On
В	RW	S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
					RAM sections are always retained when ON, but can also be
					retained when OFF dependent on the settings in S1RETENTION.
					All RAM sections will be OFF in System OFF mode.
			Off	0	Off
			On	1	On
С	RW	SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
			Off	0	Off
			On	1	On
D	RW	S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
			Off	0	Off
			On	1	On

18.9.13 RAM[0].POWERSET

Address offset: 0x904

RAM0 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	1 23	22	21 2	20	19	18	17	16	15	14	13 1	2 1	1 1	o 9	8	7	6	5	4	3	2 1	. 0
Id																	D	С													В	3 A
Res	et 0x0	000FFFF		0	0	0	0 0) (0 0	0	0	0	0	0	0	0	0	0	1	1	1	1 1	. 1	. 1	1	1	1	1	1	1	l 1	1
Id	RW	Field	Value Id	Va	lue						De	scri	iptio	n																		
Α	W	SOPOWER									Kee	ер І	RAM	se	ctio	n S	о 0	f R	٩M	0 or	or	off i	n S	yste	m (NC	mod	e				
			On	1							On																					
В	W	S1POWER									Kee	ер І	RAM	se	ctio	n S	1 o	f R	٩M	0 or	or	off i	n S	yste	m (NC	mod	e				
			On	1							On																					
С	W	SORETENTION									Kee	ері	reter	itic	n o	n R	RΑN	1 se	ctic	on S	0 w	hen	RA	M s	ecti	on i	S					
											swi	itch	ned c	ff																		
			On	1							On																					
D	W	S1RETENTION									Kee	ері	reter	itic	n o	n R	RAN	1 se	ctic	on S	1 w	hen	RA	M s	ecti	on i	S					
											swi	itch	ned c	ff																		
			On	1							On																					

18.9.14 RAM[0].POWERCLR

Address offset: 0x908

RAM0 power control clear register

Bit r	numbe	er		31 3	0 29	9 28	3 27	26	25 2	24 2	23 2	2 21	1 20	19	18	17	16	15	14	13 :	L2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																D	С													В	Α
Res	et OxC	0000FFFF		0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	1	1	1	1 1	l 1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Valu	e						Desc	ript	ion																		
Α	W	SOPOWER								k	Keep	RA	M s	ecti	on	SO d	f R	ΑM	0 o	n or	off	in Sy	/ste	m C	N n	nod	le				
			Off	1						(Off																				
В	W	S1POWER								k	Keep	RA	M s	ecti	on	S1 (of R	ΑM	0 o	n or	off	in Sy	/ste	m C	N n	nod	le				



Bit r	numbe	er		31	30	29	28	8 27	7 2	5 25	5 2	24 2	23	22	21	20	19	18	3 1	7 1	6 1	5 1	4 1	3 1	2 1	1 1	.0 9	9 8	8 7	7 (5 5	5 .	4	3 2	1	L 0	
Id																			D	(В	3 A	
Res	et 0x0	000FFFF		0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0) 1	L 1	L 1	. 1	1 1	1	1 :	1 :	1 1	L 1	L 1	1	1	1 1	. 1	. 1	
Id	RW	Field	Value Id	Va	lue							0	Des	scri	ptio	on																					
			Off	1								C	Off																								
С	W	SORETENTION										k	(ee	p r	ete	enti	on	on	RA	M:	sec	tior	S0	wł	nen	RΑ	M	sect	tion	is							
												S	wi	tch	ed	off																					
			Off	1								C	Off																								
D	W	S1RETENTION										K	(ee	ep r	ete	enti	on	on	RA	M:	sec	tior	S1	wł	nen	RA	Ms	sect	tion	is							
												S	wi	tch	ed	off																					
			Off	1								C	Off																								

18.9.15 RAM[1].POWER

Address offset: 0x910

RAM1 power control register

			•																												
Bit	numbe	er		31	30	29	28	27	26 2	25 2	24 2	3 22	21	20	19	18	17	16	15 :	14 1	13 1	2 11	10	9	8	7	5 5	5 4	3	2	1 0
Id																	D	С												1	ВА
Res	et 0x0	0000FFFF		0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	1	1	1 1	. 1	1	1	1	1	1 :	l 1	1	1	1 1
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																	
Α	RW	SOPOWER									K	еер	RAN	vI se	ectio	on S	50 C)N c	or O	FF i	n Sy	sten	1 O N	l m	ode						
											R	AM	sect	ion	s ar	e al	lwa	vs r	etai	nec	l wh	en (N. I	out	can	alsc	be				
																					the										
																					ster		_								
			Off	0							0	ff								·											
			On	1							0	n																			
В	RW	S1POWER									K	еер	RAN	vi se	ectio	on S	51 C)N c	or O	FF i	n Sy	sten	101	l m	ode.						
											R	ΔΝΛ	cart	ion	car	اد م	lw/a	vc r	otai	nec	l wh	on (NI F	out.	can	also	he				
																					the										
																					ster		_				• • • •	014.			
			Off	0								ff		, , ,			~			,	500.			-							
			On	1							0	n																			
С	RW	SORETENTION									K	еер	rete	entic	on c	on F	RAN	1 se	ctio	n Si) wh	en l	RAIV	l se	ctio	n is	n C	FF			
			Off	0							0	ff																			
			On	1							0	n																			
D	RW	S1RETENTION									K	еер	rete	entic	on c	on F	RAN	1 se	ctio	n S	1 wh	ien l	RAIV	l se	ctio	n is	n C	FF			
			Off	0							0	ff																			
			On	1							0	n																			

18.9.16 RAM[1].POWERSET

Address offset: 0x914

RAM1 power control set register

Bit r	numbe	er		31	30	29	28	27	26 2	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 :	1 0
Id																		D	С														E	ВА
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	1 1
Id	RW	Field	Value Id	Va	lue							Des	scri	ptic	n																			
Α	W	SOPOWER										Kee	ep F	RAIV	se	ctio	n S	50 c	f R	AΜ	1 o	n o	r of	f in	Sys	ten	10 r	۱m	node	е				
			On	1								On																						
В	W	S1POWER										Kee	ep F	RAN	se	ctio	n S	51 c	f R	ΑM	1 o	n o	r of	f in	Sys	ten	10	N m	node	е				
			On	1								On																						
С	W	SORETENTION										Kee	ep r	ete	ntic	n o	n F	RAN	/I se	ctio	on S	50 v	vhe	n R	ΑM	sec	ction	ı is						
												swi	itch	ed o	off																			
			On	1								On																						



Bit	numbe	r		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id																		D	С														ı	ВА
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1
Id	RW	Field	Value Id	Va	alue							Des	scri	pti	on																			
D	W	S1RETENTION										Kee	ep r	ete	nti	on (on I	RAI	VI s	ecti	on	S1 ۱	whe	en F	ΑN	l se	ctic	n is	;					
												swi	tch	ed	off																			
			On	1								On																						

18.9.17 RAM[1].POWERCLR

Address offset: 0x918

RAM1 power control clear register

When read, this register will return the value of the POWER register.

Bitı	numbe	er		31	30	29	28 :	27 :	26 2	25 2	24 2	23 2	2 2	21 2	0 1	.9 1	8 1	7 1	16 1	15 :	L4 1	3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																	[)	С													В	Α
Res	et 0x0	0000FFFF		0	0	0	0	0	0	0	0	0 (0	0 (0	0 (0 ()	0	1	1 1	1	1	1	1	1	1	1	1	1	1	1	1
ld	RW	Field	Value Id	Va	lue							Desc	crip	tio	n																		
Α	W	SOPOWER									k	(eep	o R	AΜ	sec	tior	n SC	of	RA	M1	. on	or c	ff ir	Sy:	sten	n Ol	N m	node	e				
			Off	1							(Off																					
В	W	S1POWER									k	(eep	o R	ΑM	sec	tior	ո S1	. of	RA	M1	. on	or c	ff ir	Sy:	sten	n O	N m	node	е				
			Off	1							(Off																					
С	W	SORETENTION									k	(eep	o re	ten	tio	n or	n RA	M	sec	ctio	n SC	wh	en l	RAN	1 se	ctio	n is						
											S	wit	che	ed o	ff																		
			Off	1							(Off																					
D	W	S1RETENTION									k	(eep	o re	ten	tio	n or	n RA	M	sec	ctio	n S1	wh	en I	RAN	1 se	ctio	n is						
											S	wit	che	ed o	ff																		
			Off	1							(Off																					

18.9.18 RAM[2].POWER

Address offset: 0x920

RAM2 power control register

Reset 0x0000FFFF Id RW Field Value Id Value Description Keep RAM section S0 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System ON mode. Off On 1 On RAM section S1 ON or OFF in System ON mode. RAM sections will be OFF in System ON mode. RAM sections will be OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off O Off	Bit n	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id RW Field Value Id Value Description A RW SOPOWER Keep RAM section SO ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off On Off B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off O Off	Id				D C B A
A RW SOPOWER Keep RAM section SO ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off Off Off Off	Rese	et 0x0000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1
RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off	Id	RW Field	Value Id	Value	Description
retained when OFF dependent on the settings in SORETENTION. All RAM sections will be OFF in System OFF mode. Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off Off Off	Α	RW SOPOWER			Keep RAM section S0 ON or OFF in System ON mode.
All RAM sections will be OFF in System OFF mode. Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off Off Off					RAM sections are always retained when ON, but can also be
Off 0 Off On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off					retained when OFF dependent on the settings in SORETENTION.
On 1 On B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off					All RAM sections will be OFF in System OFF mode.
B RW S1POWER Keep RAM section S1 ON or OFF in System ON mode. RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off			Off	0	Off
RAM sections are always retained when ON, but can also be retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off			On	1	On
retained when OFF dependent on the settings in S1RETENTION. All RAM sections will be OFF in System OFF mode. Off 0 Off	В	RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
All RAM sections will be OFF in System OFF mode. Off 0 Off					RAM sections are always retained when ON, but can also be
Off 0 Off					retained when OFF dependent on the settings in S1RETENTION.
					All RAM sections will be OFF in System OFF mode.
On 1 On			Off	0	Off
011			On	1	On
C RW SORETENTION Keep retention on RAM section S0 when RAM section is in OFF	С	RW SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
Off 0 Off			Off	0	Off
On 1 On			On	1	On
D RW S1RETENTION Keep retention on RAM section S1 when RAM section is in OFF	D	RW S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
Off 0 Off			Off	0	Off
On 1 On			On	1	On



18.9.19 RAM[2].POWERSET

Address offset: 0x924

RAM2 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30	29	28 2	27 2	26 2	5 2	4 2	23 2	2 2	1 20	1	9 1	8 1	.7 1	16 :	15 :	L4 1	3 1	2 13	10	9	8	7	6	5	4	3	2 1	L 0
Id																		D (С													Е	3 A
Res	et OxO	000FFFF		0	0	0	0	0	0	0 0)	0 (0	0	0) (0	0	0	1	1 :	L 1	1	1	1	1	1	1	1	1	1	L 1	1
Id	RW	Field	Value Id	Va	lue							Desc	ript	ion																			
Α	W	SOPOWER									k	(eep	RA	M s	ect	tior	n S(of	R/	M2	on	or o	off i	n Sy	ster	n O	Νn	nod	e				
			On	1							(On																					
В	W	S1POWER									k	(eep	RA	M s	ect	tior	n S:	L of	R/	M2	on	or o	off i	n Sy	ster	n O	N n	nod	e				
			On	1							(On																					
С	W	SORETENTION									k	(eep	ret	ent	ion	on	n R	٩M	se	tio	n SC) wh	nen	RAN	1 se	ctic	n is	;					
											S	wite	che	d of	f																		
			On	1							(On																					
D	W	S1RETENTION									k	(eep	ret	ent	ion	n on	n R	٩M	se	tio	n S1	wh	nen	RAN	1 se	ctic	n is	;					
											S	wit	che	d of	f																		
			On	1							(On																					

18.9.20 RAM[2].POWERCLR

Address offset: 0x928

RAM2 power control clear register

When read, this register will return the value of the POWER register.

Bit r	umbe	er		31	30 2	9 2	28 2	7 2	26 25	5 2	4 2	3 22	21	20	19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3	2 1	0
Id																	D	С													В	Α
Res	et 0x0	000FFFF		0	0)	0 ()	0 0	(0 0	0	0	0	0	0	0	0	1	1	1 :	1 1	. 1	1	1	1	1	1	1	1	1 1	1
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	n																		
Α	W	SOPOWER									K	еер	RAN	1 se	ecti	ion	S0 d	of R	ΑM	2 or	or	off i	n Sy	ste	n O	Νn	nod	e				
			Off	1							0	ff																				
В	W	S1POWER									K	еер	RAN	1 se	ecti	ion	S1 (of R	AM	2 or	or	off i	n Sy	ste	m O	N n	nod	е				
			Off	1							0	ff																				
С	W	SORETENTION									K	еер	rete	ntio	on	on	RAN	∕l se	ctio	on S	0 wl	hen	RAN	∕l se	ctic	n is	5					
											S۱	witcl	hed	off																		
			Off	1							0	ff																				
D	W	S1RETENTION									K	еер	rete	ntio	on	on	RAN	∕l se	ectio	on S	1 wl	hen	RAN	∕l se	ctic	n is	6					
											S١	witcl	hed	off																		
			Off	1							0	ff																				

18.9.21 RAM[3].POWER

Address offset: 0x930

RAM3 power control register

Bit r	numbe	er		3	1 30	29	9 28	8 27	7 26	5 25	5 2	24 2	3 2	22	21	20	19	18	17	16	15	14	13	12	2 13	1 10) 9	8	7	6	5	4	3	2	1	0
Id																			D	С															В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	(0 (0	0	0	0	0	0	0	0	1	1	1	1	1	1	. 1	. 1	. 1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	V	alue)						D)es	cri	ptio	n																				
Α	RW	SOPOWER										K	ee	рF	RAM	se	ctio	n!	SO C	N	or (OFF	in	Sys	ter	n O	N r	noc	le.							
															ecti ed w					•						,						ON.				
												Α	dl F	RAI	M se	ecti	ions	s w	ill b	e C	FF	in S	Syst	tem	0 O	FF r	no	de.								
			Off	0								C	Off																							
			On	1								C	n																							
В	RW	S1POWER										K	ee	рF	RAM	se	ctio	on S	S1 C	N	or (OFF	in	Sys	ter	n O	N r	noc	le.							



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		D C B A
Reset 0x0000FFFF		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value Description
		RAM sections are always retained when ON, but can also be
		retained when OFF dependent on the settings in S1RETENTION.
		All RAM sections will be OFF in System OFF mode.
	Off	0 Off
	On	1 On
C RW SORETENTION		Keep retention on RAM section S0 when RAM section is in OFF
	Off	0 Off
	On	1 On
D RW S1RETENTION		Keep retention on RAM section S1 when RAM section is in OFF
	Off	0 Off
	On	1 On

18.9.22 RAM[3].POWERSET

Address offset: 0x934

RAM3 power control set register

When read, this register will return the value of the POWER register.

Bit	numbe	er		31	30 2	29	28 2	27 2	26 2	5 2	4 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	! 1	L 0
Id																	D	С														В	3 A
Res	et 0x0	000FFFF		0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Va	lue						De	escri	iptic	on																			
Α	W	SOPOWER									Ke	eep l	RAN	1 se	ctio	on S	60 c	f R	ΑM	3 o	1 0	r of	f in	Sys	ten	n O	Νn	nod	e				
			On	1							Oı	n																					
В	W	S1POWER									Ke	ep I	RAN	1 se	ctio	on S	51 c	f R	ΑM	3 o	10	r of	f in	Sys	ten	n O	N n	nod	e				
			On	1							Oı	n																					
С	W	SORETENTION									Ke	ері	rete	ntic	on c	on F	RAN	1 se	ctio	on S	0 v	vhe	n R	ΑM	se	ctio	n is						
											SV	vitch	ned (off																			
			On	1							Oı	n																					
D	W	S1RETENTION									Ke	ері	rete	ntic	on c	on F	RAN	1 se	ctio	on S	1 v	vhe	n R	ΑM	se	ctio	n is						
											SV	vitch	ned (off																			
			On	1							Oı	n																					

18.9.23 RAM[3].POWERCLR

Address offset: 0x938

RAM3 power control clear register

Bit r	iumbe	er		31	30	29	28 2	7 2	26 2	5 2	4 2	3 22	21	20	19	18	3 17	' 16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																	D	С													В	Α
Rese	et 0x0	000FFFF		0	0	0	0	0	0 (0) (0 0	0	0	0	0	0	0	1	1	1	1 1	L 1	. 1	1	1	1	1	1	1 :	l 1	. 1
Id	RW	Field	Value Id	Va	lue						C)esci	ipti	on																		
Α	W	SOPOWER									K	Сеер	RAN	VI se	ecti	ion	S0	of R	RAIV	10 8	or	off	in S	yste	m C	ı NC	nod	e				
			Off	1							C	Off																				
В	W	S1POWER									K	Сеер	RAN	VI se	ecti	ion	S1	of R	RAIV	10 8	or	off	in S	yste	m C	ı NC	nod	e				
			Off	1							C	Off																				
С	W	SORETENTION									K	Сеер	rete	enti	on	on	RA	M s	ecti	on S	0 w	hen	RA	M s	ectio	on i	S					
											S	witc	hed	off																		
			Off	1							C	Off																				
D	W	S1RETENTION									K	Сеер	rete	enti	on	on	RA	M s	ecti	on S	1 w	hen	RA	M s	ectio	on i	S					
											S	witc	hed	off																		
			Off	1							C	Off																				



18.9.24 RAM[4].POWER

Address offset: 0x940

RAM4 power control register

Bit r	number		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Res	et 0x0000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW Field	Value Id	Value	Description
Α	RW SOPOWER			Keep RAM section S0 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in SORETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
В	RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in S1RETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
С	RW SORETENTION			Keep retention on RAM section S0 when RAM section is in OFF
		Off	0	Off
		On	1	On
D	RW S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
		Off	0	Off
		On	1	On

18.9.25 RAM[4].POWERSET

Address offset: 0x944

RAM4 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30	29	28 2	27 :	26 2	25 2	24 2	23 2	22 2	21 2	0 1	19 1	18	17	16	15	14	13 1	2 1	1 1	0 9	8	3 7	6	5	4	3	2	1 0
Id																		D	С													1	ВА
Res	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0 ()	0	0	0	0	1	1	1	1 :	L 1	. 1	1	L 1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue						ı	Des	crip	tior	1																		
Α	W	SOPOWER									ŀ	(ee	p R	AΜ	sec	tio	n S	0 о	f RA	M	4 or	or	off	in S	yste	m	ON	mo	de				
			On	1							(Эn																					
В	W	S1POWER									ı	(ee	p R	ΑM	sec	tio	n S	1 o	f RA	M	4 or	or	off	in S	yste	m	ON	mo	de				
			On	1							(On																					
С	W	SORETENTION									ı	(ee	p re	ten	tio	n o	n R	ΑN	1 se	ctic	on S	0 w	hen	RA	M s	ect	ion	is					
											9	wit	che	d o	ff																		
			On	1							(Эn																					
D	W	S1RETENTION									ŀ	(ee	p re	ten	tio	n o	n R	ΑN	1 se	ctic	on S	1 w	hen	RA	M s	ect	ion	is					
											9	wit	che	d o	ff																		
			On	1							(On																					

18.9.26 RAM[4].POWERCLR

Address offset: 0x948

RAM4 power control clear register



Bit r	numbe	er		31	30	29	28 2	27 2	26 2	5 2	4 2	23 2	22 2	1 2	0 1	9 1	8 :	17 :	16	15	14 1	3 1	2 11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																		D	С													В	Α
Res	et OxO	0000FFFF		0	0	0	0	0	0	0 0)	0 (0 (0 0) (0 (0	0	0	1	1 :	L 1	. 1	1	1	1	1	1	1	1	1 1	l 1	. 1
Id	RW	Field	Value Id	Va	lue							Desc	crip	tion	1																		
Α	W	SOPOWER									k	(eep	p RA	AM :	sec	tior	n S	0 of	f RA	M	lon	or (off in	ı Sys	ten	n Ol	N m	nod	e				
			Off	1							(Off																					
В	W	S1POWER									k	(eep	p RA	AM :	sec	tior	n S	1 o	f RA	M	on	or o	off in	Sys	ten	n Ol	N m	nod	e				
			Off	1							(Off																					
С	W	SORETENTION									k	(eep	p re	ten	tio	n or	n R	ΑM	se	ctic	n SC) wh	en l	RAIV	l se	ctio	n is						
											S	wit	che	d of	ff																		
			Off	1							(Off																					
D	W	S1RETENTION									k	Keep	p re	ten	tio	n or	n R	AM	se	ctic	n S1	wh	en l	RAIV	l se	ctio	n is						
											S	wit	che	d of	ff																		
			Off	1							(Off																					

18.9.27 RAM[5].POWER

Address offset: 0x950

RAM5 power control register

Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Res	et 0x0000FFFF		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1 \ $
Id	RW Field	Value Id	Value	Description
Α	RW SOPOWER			Keep RAM section S0 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in SORETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
В	RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in S1RETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
С	RW SORETENTION			Keep retention on RAM section SO when RAM section is in OFF
		Off	0	Off
		On	1	On
D	RW S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
		Off	0	Off
		On	1	On

18.9.28 RAM[5].POWERSET

Address offset: 0x954

RAM5 power control set register

Bitı	numbe	er		31 30	29	28 2	27 2	26 2	5 24	4 2	3 22	2 21	. 20	19	18	17	16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id																D	С													В	Α
Res	et 0x0	000FFFF		0 0	0	0	0	0 (0	0	0	0	0	0	0	0	0	1	1	1	1 1	. 1	1	1	1	1	1	1	1 1	. 1	. 1
Id	RW	Field	Value Id	Value						D	escr	ripti	ion																		
Α	W	SOPOWER								K	еер	RAI	M se	ecti	on S	50 c	f R	٩M.	5 or	or	off i	n Sy	/stei	n O	Νm	node	е				
			On	1						0	n																				
В	W	S1POWER								K	еер	RAI	M se	ecti	on S	51 c	f R	٩M.	5 or	or	off i	n Sy	/stei	n O	Νm	node	е				
			On	1						0	n																				



Bit	numbe	er		31	1 30	29	28	8 27	7 2	6 2	5 2	4 2	23 2	22	21	20	19	18	3 1	7 1	6 1	15 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																			0) (2															В	Α
Res	et 0x0	0000FFFF		0	0	0	0	0	(0) (0	0	0	0	0	0	0	C) ()	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	alue								Des	cri	ptic	n																					
С	W	SORETENTION										k	(ee	рr	ete	ntio	on	on	RΑ	М	sec	tio	n S	0 w	he	n R	ΑM	se	ctic	n i	S						
												S	wit	tch	ed (off																					
			On	1								(Ͻn																								
D	W	S1RETENTION										k	(ee	рr	ete	ntio	on	on	RΑ	M	sec	tio	n S	1 w	he	n R	ΑM	se	ctic	n is	S						
												S	wit	tch	ed (off																					
			On	1								(On																								

18.9.29 RAM[5].POWERCLR

Address offset: 0x958

RAM5 power control clear register

When read, this register will return the value of the POWER register.

Bitı	numbe	er		31	30 2	29 2	28 2	7 2	6 25	5 24	23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																	D	С														В	3 A
Res	et 0x0	0000FFFF		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1 :	l 1	1
Id	RW	Field	Value Id	Va	lue						De	escr	iptio	on																			
Α	W	SOPOWER									Ke	еер	RAN	1 se	ectio	on S	SO 0	of R	ΑM	5 o	n o	r of	f in	Sys	ten	10 n	۱n	nod	e				
			Off	1							Of	ff																					
В	W	S1POWER									Ke	еер	RAN	1 se	ectio	on S	S1 (of R	ΑM	5 o	n o	r of	f in	Sys	ten	10 n	۱n	nod	e				
			Off	1							Of	ff																					
С	W	SORETENTION									Ke	еер	rete	ntic	on d	on f	RAN	√l se	ecti	on S	50 v	vhe	n R	ΑM	se	ctio	n is						
											SV	vitcl	ned	off																			
			Off	1							Of	ff																					
D	W	S1RETENTION									Ke	еер	rete	ntic	on d	on f	RAN	√l se	ecti	on S	51 v	vhe	n R	AM	se	ctio	n is						
											SV	vitcl	ned	off																			
			Off	1							Of	ff																					

18.9.30 RAM[6].POWER

Address offset: 0x960

RAM6 power control register

Bitı	number		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D C B A
Res	et 0x0000FFFF		0 0 0 0 0 0	footnotemark
Id	RW Field	Value Id	Value	Description
Α	RW SOPOWER			Keep RAM section SO ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in SORETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
В	RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
				RAM sections are always retained when ON, but can also be
				retained when OFF dependent on the settings in S1RETENTION.
				All RAM sections will be OFF in System OFF mode.
		Off	0	Off
		On	1	On
С	RW SORETENTION	Oli	-	Keep retention on RAM section SO when RAM section is in OFF
Č	JONETER TON	Off	0	Off
		On	1	On
D	RW S1RETENTION	J.,		Keep retention on RAM section S1 when RAM section is in OFF
	52	Off	0	Off
		•	5	5



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			D C B
Reset 0x0000FFFF		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1
Id RW Field	Value Id	Value	Description
	On	1	On

18.9.31 RAM[6].POWERSET

Address offset: 0x964

RAM6 power control set register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30	29	28	27 2	26 2	25 2	4 2	23 2	2 2	1 20) 1:	9 18	8 1	7 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id																	[) (2													В	Α
Res	et 0x0	000FFFF		0	0	0	0	0	0	0 (0	0 (0 0	0	0	0) (0) 1	. 1	. 1	1	1	1	1	1	1	1	1	1 :	l 1	1	1
Id	RW	Field	Value Id	Va	lue							Desc	cript	tion																			
Α	W	SOPOWER									k	Keep	o RA	M s	ect	tion	SC	of	RAI	M 6	on (or o	ff in	Sys	ten	10 r	l m	ode	9				
			On	1							(Эn																					
В	W	S1POWER									k	Keep	o RA	M s	ect	tion	S1	of	RAI	И6	on (or o	ff in	Sys	ten	10 r	l m	ode	9				
			On	1							(Эn																					
С	W	SORETENTION									k	Keep	o ret	tent	ion	on	R/	MA	sec	tior	S0	wh	en R	AM	sec	tion	ı is						
											S	wit	che	d of	f																		
			On	1							(On																					
D	W	S1RETENTION									k	Keep	o ret	tent	ion	on	R/	MA	sec	tior	S1	wh	en R	AM	sec	ction	ı is						
											S	wit	che	d of	f																		
			On	1							(Эn																					

18.9.32 RAM[6].POWERCLR

Address offset: 0x968

RAM6 power control clear register

When read, this register will return the value of the POWER register.

Bit r	numbe	er		31	30 2	9 2	28 2	7 2	6 2	5 2	4 2	3 2	2 2	1 20	0 1	19 1	8 1	.7 1	16	15 :	14 1	3 1	2 11	10	9	8	7	6	5	4	3	2	1 0
Id																	1	D	С														ВА
Res	et 0x0	0000FFFF		0	0	0	0 0) (0 0) () (0) (0 0) (0 (0	0	0	1	1	1 1	. 1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue						D	esc	rip	tion	ı																		
Α	W	SOPOWER									K	eep	R/	AM s	sec	tior	n S(of	f RA	M	on	or (off i	n Sy	stei	n O	N r	nod	le				
			Off	1							C	ff																					
В	W	S1POWER									K	eep	R/	AM s	sec	tior	1 S:	L of	f RA	M	on	or (off i	n Sy	stei	n O	N r	nod	le				
			Off	1							C	ff																					
С	W	SORETENTION									K	eep	re	tent	tio	n or	ı R	٩M	se	ctio	n S() wh	en	RAN	/l se	ctic	n i	S					
											S	wite	che	d of	ff																		
			Off	1							C	ff																					
D	W	S1RETENTION									K	eep	re	tent	tio	n or	n R	٩M	se	ctio	n S:	wh	en	RAN	∕l se	ctic	n i	S					
											S	wite	che	d of	ff																		
			Off	1							C	ff																					

18.9.33 RAM[7].POWER

Address offset: 0x970

RAM7 power control register

Bit r	number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Id			D C	Α
Res	et 0x0000FFFF	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1	1
Id	RW Field Value Id	Value	Description	
Α	RW SOPOWER		Keep RAM section S0 ON or OFF in System ON mode.	



number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
			D C B A
et 0x0000FFFF		0 0 0 0 0 0 0	footnotemark
RW Field	Value Id	Value	Description
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in SORETENTION.
			All RAM sections will be OFF in System OFF mode.
	Off	0	Off
	On	1	On
RW S1POWER			Keep RAM section S1 ON or OFF in System ON mode.
			RAM sections are always retained when ON, but can also be
			retained when OFF dependent on the settings in S1RETENTION.
			All RAM sections will be OFF in System OFF mode.
	Off	0	Off
	On	1	On
RW SORETENTION			Keep retention on RAM section SO when RAM section is in OFF
	Off	0	Off
	On	1	On
RW S1RETENTION			Keep retention on RAM section S1 when RAM section is in OFF
	Off	0	Off
	On	1	On
	RW S1POWER RW SORETENTION	eet 0x00000FFFF RW Field Value Id Off On RW S1POWER Off On RW S0RETENTION Off On RW S1RETENTION Off On Off	Off On 1 RW SORETENTION Off On 1 RW S1RETENTION Off On 1 RW S1RETENTION Off On 1

18.9.34 RAM[7].POWERSET

Address offset: 0x974

RAM7 power control set register

When read, this register will return the value of the POWER register.

	ВА
1 1 1 1 1	1 1 1
ON mode	
ON mode	
on is	
on is	
	1 1 1 1 1 1 1 CON mode ON mode on is

18.9.35 RAM[7].POWERCLR

Address offset: 0x978

RAM7 power control clear register

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8 7	6	5	4	3	2	1	0
Id																		D	С														В	Α
Rese	et 0x0	000FFFF		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	crip	tic	on																			
Α	W	SOPOWER										Kee	p R	ΑN	1 se	ecti	on:	S0 (of F	RAN	17 c	on c	r of	f in	Syst	em	ON	mo	de					
			Off	1								Off																						
В	W	S1POWER										Kee	p R	ΑN	1 se	ecti	on :	S1 (of F	RAN	17 c	on c	r of	f in	Syst	em	ON	mo	de					
			Off	1								Off																						



Bitı	numbe	er		31	1 30	29	28	8 27	7 2	26 :	25	24	23	22	21	20	0 1	9 1	8	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																				D	С															В	Α
Res	et 0x0	000FFFF		0	0	0	0	0)	0	0	0	0	0	0	0	C)	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Id	RW	Field	Value Id	Va	alue								De	scr	ipti	on																					
С	W	SORETENTION											Κe	ер	ret	ent	ior	1 0	n R	ΑN	1 se	ecti	on	S0 ۱	whe	en F	RAN	1 se	ctic	n i	5						
													sv	itc	hed	of	f																				
			Off	1									Of	f																							
D	W	S1RETENTION											Ke	ер	ret	ent	ior	1 0	n R	ΑN	1 se	cti	on:	S1 ۱	whe	en F	RAN	1 se	ctic	n i	S						
													sv	itc	hed	of	f																				
			Off	1									Of	f																							

18.10 Electrical specification

18.10.1 Current consumption, sleep

Symbol	Description	Min.	Тур.	Max.	Units
I _{OFF}	System OFF current, no RAM retention		0.3		μΑ
I _{ON}	System ON base current, no RAM retention		1.2		μΑ
I _{RAM}	Additional RAM retention current per 4 KB RAM section		20		nA

18.10.2 Device startup times

Symbol	Description	Min.	Тур.	Max.	Units
t _{POR}	Time in Power on Reset after VDD reaches 1.7 V for all supply				
	voltages and temperatures. Dependent on supply rise time. 10				
t _{POR,10us}	VDD rise time 10us		1		ms
t _{POR,10ms}	VDD rise time 10ms		9		ms
t _{POR,60ms}	VDD rise time 60ms		23		ms
t_{PINR}	If a GPIO pin is configured as reset, the maximum time taken				
	to pull up the pin and release reset after power on reset.				
	Dependent on the pin capacitive load (C) ¹¹ : t=5RC, R = 13kOhm				
t _{PINR,500nF}	C = 500nF			32.5	ms
t _{PINR,10uF}	C = 10uF			650	ms
t _{R2ON}	Time from reset to ON (CPU execute)				
t _{R2ON,NOTCONF}	If reset pin not configured	tPOR			ms
t _{R2ON,CONF}	If reset pin configured	tPOR +			ms
		tPINR			
t _{OFF2ON}	Time from OFF to CPU execute		16.5		μs
t _{IDLE2CPU}	Time from IDLE to CPU execute		3.0		μs
t _{EVTSET,CL1}	Time from HW event to PPI event in Constant Latency System		0.0625		μs
	ON mode				
t _{EVTSET,CLO}	Time from HW event to PPI event in Low Power System ON		0.0625		μs
	mode				

18.10.3 Power fail comparator

Symbol	Description	Min.	Тур.	Max.	Units
I _{POF}	Current consumption when enabled ¹²		<4		μΑ
V_{POF}	Nominal power level warning thresholds (falling supply voltage).	1.7		2.8	V
	Levels are configurable between Min. and Max. in 100mV				
	increments.				
V_{POFTOL}	Threshold voltage tolerance		±1	±5	%

A step increase in supply voltage of 300 mV or more, with rise time of 300 ms or less, within the valid supply range, may result in a system reset.

To decrease maximum time a device could hold in reset, a strong external pullup resistor can be used.

To save power, POF will not operate nor consume in System OFF, or while HFCLK is not running, even if left enabled by software



Symbol	Description	Min.	Тур.	Max.	Units
$V_{POFHYST}$	Threshold voltage hysteresis		50		mV
V _{BOR,OFF}	Brown out reset voltage range SYSTEM OFF mode	1.2		1.7	V
V _{BOR,ON}	Brown out reset voltage range SYSTEM ON mode	1.5		1.7	V



19 CLOCK — Clock control

The clock control system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. Clock distribution is automated and grouped independently by module to limit current consumption in unused branches of the clock tree.

Listed here are the main features for CLOCK:

- 64 MHz on-chip oscillator
- 64 MHz crystal oscillator, using external 32 MHz crystal
- 32.768 kHz +/-250 ppm RC oscillator
- 32.768 kHz crystal oscillator, using external 32.768 kHz crystal
- 32.768 kHz oscillator synthesized from 64 MHz oscillator
- Firmware (FW) override control of oscillator activity for low latency start up
- Automatic oscillator and clock control, and distribution for ultra-low power

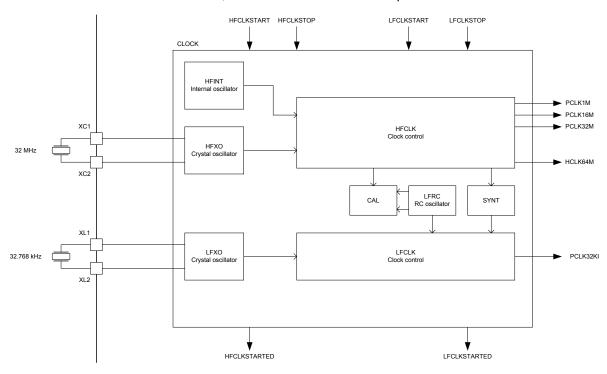


Figure 17: Clock control

19.1 HFCLK clock controller

The HFCLK clock controller provides the following clocks to the system.

- HCLK64M: 64 MHz CPU clock
- PCLK1M: 1 MHz peripheral clock
- PCLK16M: 16 MHz peripheral clock
- PCLK32M: 32 MHz peripheral clock

The HFCLK controller supports the following high frequency clock (HFCLK) sources:

- 64 MHz internal oscillator (HFINT)
- 64 MHz crystal oscillator (HFXO)

For illustration, see Figure 17: Clock control on page 101.



When the system requests one or more clocks from the HFCLK controller, the HFCLK controller will automatically provide them. If the system does not request any clocks provided by the HFCLK controller, the controller will enter a power saving mode.

These clocks are only available when the system is in ON mode. When the system enters ON mode, the internal oscillator (HFINT) clock source will automatically start to be able to provide the required HFCLK clock(s) for the system.

The HFINT will be used when HFCLK is requested and HFXO has not been started. The HFXO is started by triggering the HFCLKSTART task and stopped using the HFCLKSTOP task. A HFCLKSTARTED event will be generated when the HFXO has started and its frequency is stable.

The HFXO must be running to use the RADIO, NFC module or the calibration mechanism associated with the 32.768 kHz RC oscillator.

19.1.1 64 MHz crystal oscillator (HFXO)

The 64 MHz crystal oscillator (HFXO) is controlled by a 32 MHz external crystal

The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet.

Figure 18: Circuit diagram of the 64 MHz crystal oscillator on page 102 shows how the 32 MHz crystal is connected to the 64 MHz crystal oscillator.

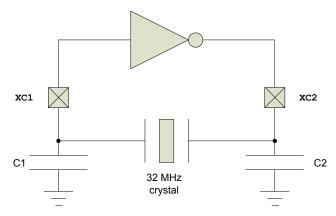


Figure 18: Circuit diagram of the 64 MHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

 $C2' = C2 + C_{pcb2} + C_{pin}$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. For more information, see *Reference circuitry* on page 545. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the xc1 and xc2 pins. See table *64 MHz crystal oscillator (HFXO)* on page 109. The load capacitors C1 and C2 should have the same value.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance, and drive level must comply with the specifications in table 64 MHz crystal oscillator (HFXO) on page 109. It is recommended to use a crystal with lower than maximum load capacitance and/or shunt capacitance. A low load capacitance will reduce both start up time and current consumption.



19.2 LFCLK clock controller

The system supports several low frequency clock sources.

As illustrated in *Figure 17: Clock control* on page 101, the system supports the following low frequency clock sources:

- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz crystal oscillator (LFXO)
- 32.768 kHz synthesized from HFCLK (LFSYNT)

The LFCLK clock is started by first selecting the preferred clock source in register *LFCLKSRC* on page 108 and then triggering the LFCLKSTART task. If the LFXO is selected as the clock source, the LFCLK will initially start running from the 32.768 kHz LFRC while the LFXO is starting up and automatically switch to using the LFXO once this oscillator is running. The LFCLKSTARTED event will be generated when the LFXO has been started.

The LFCLK clock is stopped by triggering the LFCLKSTOP task.

It is not allowed to write to register LFCLKSRC on page 108 when the LFCLK is running.

A LFCLKSTOP task will stop the LFCLK oscillator. However, the LFCLKSTOP task can only be triggered after the STATE field in register *LFCLKSTAT* on page 107 indicates a 'LFCLK running' state.

The LFCLK clock controller and all of the LFCLK clock sources are always switched off when in OFF mode.

19.2.1 32.768 kHz RC oscillator (LFRC)

The default source of the low frequency clock (LFCLK) is the 32.768 kHz RC oscillator (LFRC).

The LFRC frequency will be affected by variation in temperature. The LFRC oscillator can be calibrated to improve accuracy by using the HFXO as a reference oscillator during calibration. See Table 32.768 kHz RC oscillator (LFRC) on page 109 for details on the default and calibrated accuracy of the LFRC oscillator. The LFRC oscillator does not require additional external components.

19.2.2 Calibrating the 32.768 kHz RC oscillator

After the 32.768 kHz RC oscillator is started and running, it can be calibrated by triggering the CAL task. In this case, the HFCLK will be temporarily switched on and used as a reference.

A DONE event will be generated when calibration has finished. The calibration mechanism will only work as long as HFCLK is generated from the HFCLK crystal oscillator, it is therefore necessary to explicitly start this crystal oscillator before calibration can be started, see HFCLKSTART task.

19.2.3 Calibration timer

The calibration timer can be used to time the calibration interval of the 32.768 kHz RC oscillator.

The calibration timer is started by triggering the CTSTART task and stopped by triggering the CTSTOP task. The calibration timer will always start counting down from the value specified in CTIV and generate a CTTO timeout event when it reaches 0. The Calibration timer will stop by itself when it reaches 0.

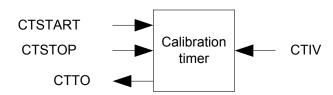


Figure 19: Calibration timer

Due to limitations in the calibration timer, only one task related to calibration, that is, CAL, CTSTART and CTSTOP, can be triggered for every period of LFCLK.



19.2.4 32.768 kHz crystal oscillator (LFXO)

For higher LFCLK accuracy (when better than +/- 250 ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used.

The following external clock sources are supported:

- Low swing clock signal applied to the XL1 pin. The XL2 pin shall then be grounded.
- Rail-to-rail clock signal applied to the XL1 pin. The XL2 pin shall then be grounded or left unconnected.

The *LFCLKSRC* on page 108 register controls the clock source, and its allowed swing. The truth table for various situations is as follows:

Table 26: LFCLKSRC configuration depending on clock source

SRC	EXTERNAL	BYPASS	Comment
0	0	0	Normal operation, RC is source
0	0	1	DO NOT USE
0	1	Χ	DO NOT USE
1	0	0	Normal XTAL operation
1	1	0	Apply external low swing signal to XL1, ground XL2
1	1	1	Apply external full swing signal to XL1, leave XL2 grounded or unconnected
1	0	1	DO NOT USE
2	0	0	Normal operation, synth is source
2	0	1	DO NOT USE
2	1	Χ	DO NOT USE

To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. *Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator* on page 104 shows the LFXO circuitry.

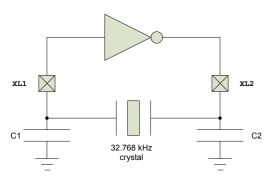


Figure 20: Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{\left(C1' \cdot C2'\right)}{\left(C1' + C2'\right)}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

 $C2' = C2 + C_{pcb2} + C_{pin}$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_{pcb1} and C_{pcb2} are stray capacitances on the PCB. C_{pin} is the pin input capacitance on the XC1 and XC2 pins (see 32.768 kHz crystal oscillator (LFXO) on page 109). The load capacitors C1 and C2 should have the same value.

For more information, see *Reference circuitry* on page 545.



19.2.5 32.768 kHz synthesized from HFCLK (LFSYNT)

LFCLK can also be synthesized from the HFCLK clock source. The accuracy of LFCLK will then be the accuracy of the HFCLK.

Using the LFSYNT clock avoids the requirement for a 32.768 kHz crystal, but increases average power consumption as the HFCLK will need to be requested in the system.

19.3 Registers

Table 27: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40000000	CLOCK	CLOCK	Clock control	

Table 28: Register Overview

Register	Offset	Description	
TASKS_HFCLKSTART	0x000	Start HFCLK crystal oscillator	
TASKS_HFCLKSTOP	0x004	Stop HFCLK crystal oscillator	
TASKS_LFCLKSTART	0x008	Start LFCLK source	
TASKS_LFCLKSTOP	0x00C	Stop LFCLK source	
TASKS_CAL	0x010	Start calibration of LFRC oscillator	
TASKS_CTSTART	0x014	Start calibration timer	
TASKS_CTSTOP	0x018	Stop calibration timer	
EVENTS_HFCLKSTARTED	0x100	HFCLK oscillator started	
EVENTS_LFCLKSTARTED	0x104	LFCLK started	
EVENTS_DONE	0x10C	Calibration of LFCLK RC oscillator complete event	
EVENTS_CTTO	0x110	Calibration timer timeout	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
HFCLKRUN	0x408	Status indicating that HFCLKSTART task has been triggered	
HFCLKSTAT	0x40C	HFCLK status	
LFCLKRUN	0x414	Status indicating that LFCLKSTART task has been triggered	
LFCLKSTAT	0x418	LFCLK status	
LFCLKSRCCOPY	0x41C	Copy of LFCLKSRC register, set when LFCLKSTART task was triggered	
LFCLKSRC	0x518	Clock source for the LFCLK	
CTIV	0x538	Calibration timer interval	Retained
TRACECONFIG	0x55C	Clocking options for the Trace Port debug interface	

19.3.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	number			31 3	30 2	9 28	8 27	26	25 24	1 23	22 2	21 20	0 19	9 18	3 17	16	15	14 13	3 12	11	10 !	9	8 7	' 6	5	4	3 2	1	0
Id																										D	С	В	Α
Res	et 0x000	00000		0	0 0	0	0	0	0 0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0 (0	0	0	0 0	0	0
Id	RW Fi	eld	Value Id	Valu	ue					De	scrip	otion	ı																
Α	RW H	FCLKSTARTED								Wr	rite '	1' to	Ena	able	int	erru	pt f	or HF	CLK	STAI	RTE) e	vent						
										Se	e <i>EV</i>	ENTS	_H	FCLI	KST	4RT	ED												
			Set	1						En	able																		
			Disabled	0						Re	ad: [Disab	led																
			Enabled	1						Re	ad: E	nabl	led																
В	RW LF	FCLKSTARTED								Wr	rite '	1' to	Ena	able	int	erru	pt f	or LF	CLKS	TAF	RTEC	ev	/ent						
										Se	e <i>EV</i>	ENTS	_ <i>LF</i>	CLK	(STA	RTE	D												
			Set	1						En	able																		
			Disabled	0						Re	ad: [Disab	led																
			Enabled	1						Re	ad: E	nabl	led																



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
C RW DONE		Write '1' to Enable interrupt for DONE event
		See EVENTS_DONE
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
D RW CTTO		Write '1' to Enable interrupt for CTTO event
		See EVENTS_CTTO
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled

19.3.2 INTENCLR

Address offset: 0x308

Disable interrupt

		•			
Bit nu	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Rese	t 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	HFCLKSTARTED			Write '1' to Disable interrupt for HFCLKSTARTED event
					See EVENTS_HFCLKSTARTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	LFCLKSTARTED			Write '1' to Disable interrupt for LFCLKSTARTED event
					See EVENTS_LFCLKSTARTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	DONE			Write '1' to Disable interrupt for DONE event
					See EVENTS_DONE
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	СТТО			Write '1' to Disable interrupt for CTTO event
					See EVENTS_CTTO
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

19.3.3 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

Bit	numbe	r		3:	1 30	29	9 2	8 2	7 2	26	25	5 24	1 2	3 2	2 2	1:	20	19	18	17	10	5 1	5 1	.4	13	12	1:	l 1	0 9	9	8	7	6	5	4	3	2	1	0
Id																																							Α
Re	et 0x0	0000000		0	0	0) () (0	0	0	0	0) ()	0	0	0	0	0	0	C)	0	0	0	0	C) (0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	alue	2							D	esc	rip	tio	n																						
Α	R	STATUS											Н	FCI	_KS	TΑ	RT	tas	k t	rigg	ger	ed	or	no	t														
			NotTriggered	0									Ta	ask	no	t tı	rigg	ger	ed																				
			Triggered	1									Т	ask	tri	gge	ere	d																					



19.3.4 HFCLKSTAT

Address offset: 0x40C

HFCLK status

Bit	numbe	er		31	30 2	29	28	27	26	25	24	23	22	21	20	19	9 18	3 1	7 1	5 1	5 1	4 1	.3 1	.2 1	1 1	0 9) 8	7	6	5	4	3	2	1	0
Id																			В																Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	C	0	() () (0	0 () () () (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																				
Α	R	SRC										So	urc	e of	f HF	FCL	.K																		
			RC	0								64	MI	Hz iı	nte	rna	al o	scil	lato	r (HFI	NT)													
			Xtal	1								64	MI	Hz c	rys	tal	oso	illa	itor	(H	FXC))													
В	R	STATE										HF	CLF	< sta	ate																				
			NotRunning	0								HF	CLF	(no	ot ru	unr	ning	5																	
			Running	1								HF	CLF	< ru	nni	ng																			

19.3.5 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

Bit r	numbe	er		31 30	29	28	27 :	26 2	25 2	24 2	3 2	2 2	1 20) 19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	6 !	5 4	1 3	2	1	0
Id																															Α
Res	et OxC	0000000		0 0	0	0	0	0	0 (0 (0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 (0 0	0	0	0
Id	RW	Field	Value Id	Value	•					C	esc	cript	tion																		
Α	R	STATUS								L	FCL	.KST	ART	tas	k tr	igge	ered	lor	not												
			NotTriggered	0						Т	ask	not	t trig	gger	ed																
			Triggered	1						Т	ask	trig	ger	ed																	

19.3.6 LFCLKSTAT

Address offset: 0x418

LFCLK status

Bit	numbe	er		31	30	29	28 2	7 2	26 25	5 24	1 23	22	21 2	0 1	9 1	8 17	16	15	14	13 1	12 1	1 10	9	8	7	6	5 4	4 3	2	1 0
Id																	В													A A
Res	et 0x0	0000000		0	0	0	0 (0	0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0 (0 0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	escri	ptio	n																
Α	R	SRC									So	urce	e of I	.FCI	_K															
			RC	0							32	.768	3 kHz	RC	osc	illat	or													
			Xtal	1							32	.768	3 kHz	cry	/sta	osc	illat	or												
			Synth	2							32	.768	3 kHz	syı	nthe	size	d fr	om	HF	CLK										
В	R	STATE									LF	CLK	state	9																
			NotRunning	0							LF	CLK	not	runi	ning															
			Running	1							LF	CLK	runr	ing																

19.3.7 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set when LFCLKSTART task was triggered

Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A R SRC			Clock source
	RC	0	32.768 kHz RC oscillator
	Xtal	1	32.768 kHz crystal oscillator
	Synth	2	32.768 kHz synthesized from HFCLK



19.3.8 LFCLKSRC

Address offset: 0x518

Clock source for the LFCLK

Bit r	iumbe	r		31	30 2	9 2	28 2	7 2	26 2	5 2	4 23	22	21 2	0 :	19 1	8 :	17	16	15	14	13	12 :	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id																	С	В														A	A A
Rese	et 0x0	0000000		0	0 ()	0 (0	0 0) (0 0	0	0	0	0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Va	lue						De	scr	iptio	n																			
Α	RW	SRC									Clo	ock	sour	ce																			
			RC	0							32	.76	8 kHz	R	os	cilla	ato	r															
			Xtal	1							32	.76	8 kHz	cr	ysta	Ιo	scil	lat	or														
			Synth	2							32	.76	8 kHz	sy	nth	esi	zec	l fro	om	HF	CLK												
В	RW	BYPASS									En	able	e or o	lisa	ble	by	pas	ss c	of L	FCL	K cr	ysta	al o	scill	ato	r w	ith	ext	ern	al			
											clo	ck:	sour	e																			
			Disabled	0							Dis	abl	le (us	e v	vith	Xt	al c	r lo	ow-	swi	ng e	exte	rna	al sc	uro	ce)							
			Enabled	1							En	able	e (us	e w	ith	rail	-to	-ra	il e	xte	nal	sou	ırce	2)									
С	RW	EXTERNAL									En	able	e or o	lisa	ble	ex	ter	nal	so	urce	e foi	r LF	CLK	(
			Disabled	0							Dis	abl	le ext	eri	nal s	ou	rce	e (u	se	with	n Xta	al)											
			Enabled	1							En	able	e use	of	ext	err	al:	sou	ırce	ins	tea	d of	f Xt	al (SRC	ne	eds	to	be				
											set	to	Xtal)																				

19.3.9 CTIV (Retained)

Address offset: 0x538

This register is a retained register

Calibration timer interval

Bitı	numbe	er		31 30	29	28 2	7 26	25	24	23	22	21 2	0 19	18	17	16	15	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id																									Α	Α	Α	ΑА	A	А
Res	et 0x0	0000000		0 0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value						De	scri	otio	n																	
Α	RW	CTIV								Cal	ibra	tion	tim	er ir	nter	val i	n m	ulti	ple	of 0	.25	seco	ond	s. R	ang	e:				
										0.2	5 se	con	ds to	31	.75	sec	ond	s.												

19.3.10 TRACECONFIG

Address offset: 0x55C

Clocking options for the Trace Port debug interface

This register is a retained register. Reset behavior is the same as debug components.

1 0
A A
0 0



19.4 Electrical specification

19.4.1 64 MHz internal oscillator (HFINT)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFINT}	Nominal output frequency		64		MHz
f _{TOL_HFINT}	Frequency tolerance		<±1.5	<±6	%
I _{HFINT}	Run current		60		μΑ
I _{START_HFINT}	Average startup current		I_HFINT		μΑ
t _{START_HFINT}	Startup time		3		us

19.4.2 64 MHz crystal oscillator (HFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_HFXO}	Nominal output frequency		64		MHz
f _{XTAL_HFXO}	External crystal frequency		32		MHz
f _{TOL_HFXO}	Frequency tolerance requirement for 2.4 GHz proprietary radio			±60	ppm
	applications				
f _{TOL_HFXO_BLE}	Frequency tolerance requirement, Bluetooth low energy			±40	ppm
	applications				
C _{L_HFXO}	Load capacitance			12	pF
C _{0_HFXO}	Shunt capacitance			7	pF
R _{S_HFXO_7PF}	Equivalent series resistance C0 = 7 pF			60	ohm
R _{S_HFXO_5PF}	Equivalent series resistance C0 = 5 pF			80	ohm
R _{S_HFXO_3PF}	Equivalent series resistance C0 = 3 pF			100	ohm
P _{D_HFXO}	Drive level			100	uW
C _{PIN_HFXO}	Input capacitance XC1 and XC2		4		pF
I _{STBY_X32M}	Core standby current ¹³		50		μΑ
I _{HFXO}	Run current		250		μΑ
I _{START_HFXO}	Average startup current, first 1 ms		0.4		mA
t _{START_HFXO}	Startup time		0.36		ms

19.4.3 32.768 kHz RC oscillator (LFRC)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFRC}	Nominal frequency		32.768		kHz
f _{TOL_LFRC}	Frequency tolerance			±2	%
f _{TOL_CAL_LFRC}	Frequency tolerance for LFRC after calibration ¹⁴			±250	ppm
I _{LFRC}	Run current for 32.768 kHz RC oscillator		0.6	1	μΑ
t _{START_LFRC}	Startup time for 32.768 kHz RC oscillator		600		us

19.4.4 32.768 kHz crystal oscillator (LFXO)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFXO}	Crystal frequency		32.768		kHz
f _{TOL_LFXO_BLE}	Frequency tolerance requirement for BLE stack			±250	ppm
f _{TOL_LFXO_ANT}	Frequency tolerance requirement for ANT stack			±50	ppm
C _{L_LFXO}	Load capacitance			12.5	pF
C _{0_LFXO}	Shunt capacitance			2	pF
R _{S_LFXO}	Equivalent series resistance			100	kohm
P _{D_LFXO}	Drive level			1	uW
C _{pin}	Input capacitance on XL1 and XL2 pads		4		pF
I _{LFXO}	Run current for 32.768 kHz crystal oscillator		0.25		μΑ

Current drawn if HFXO is forced on through for instance using the low latency power mode. Constant temperature within ± 0.5 °C and calibration performed at least every 8 seconds



Symbol	Description	Min.	Тур.	Max.	Units
t _{START_LFXO}	Startup time for 32.768 kHz crystal oscillator		0.25		S
$V_{AMP_IN_XO_LOW}$	Peak to peak amplitude for external low swing clock. Input	200		1000	mV
	signal must not swing outside supply rails.				

19.4.5 32.768 kHz synthesized from HFCLK (LFSYNT)

Symbol	Description	Min.	Тур.	Max.	Units
f _{NOM_LFSYNT}	Nominal frequency		32.768		kHz
f _{TOL_LFSYNT}	Frequency tolerance in addition to HFLCK tolerance ¹⁵		8		ppm
I _{LFSYNT}	Run current for synthesized 32.768 kHz		100		μΑ
t _{START_LFSYNT}	Startup time for synthesized 32.768 kHz		100		us

¹⁵ Frequency tolerance will be derived from the HFCLK source clock plus the LFSYNT tolerance



20 GPIO — General purpose input/output

The general purpose input/output (GPIO) is organized as one port with up to 32 I/Os (dependent on package) enabling access and control of up to 32 pins through one port. Each GPIO can be accessed individually.

GPIO has the following user-configurable features:

- Up to 32 GPIO
- 8 GPIO with Analog channels for SAADC, COMP or LPCOMP inputs
- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- · All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register

The GPIO Port peripheral implements up to 32 pins, PIN0 through PIN31. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- · Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- Analog input (for selected pins)

The PIN_CNF registers are retained registers. See *POWER — Power supply* on page 78 chapter for more information about retained registers.

20.1 Pin configuration

Pins can be individually configured, through the SENSE field in the PIN_CNF[n] register, to detect either a high level or a low level on their input.

When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal, and the default behaviour, as defined by the DETECTMODE register, is that the DETECT signal from all pins in the GPIO Port are combined into a common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals, see *Figure 21: GPIO Port and the GPIO pin details* on page 112. This mechanism is functional in both ON and OFF mode.



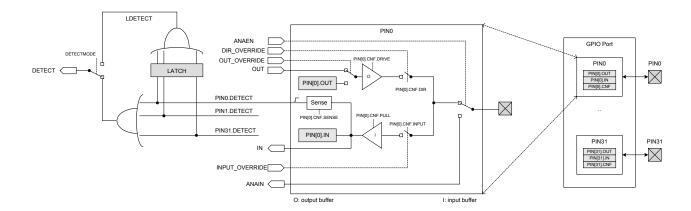


Figure 21: GPIO Port and the GPIO pin details

Figure 21: GPIO Port and the GPIO pin details on page 112 illustrates the GPIO port containing 32 individual pins, where PINO is illustrated in more detail as a reference. All the signals on the left side of the illustration are used by other peripherals in the system, and therefore, are not directly available to the CPU.

Make sure that a pin is in a level that cannot trigger the sense mechanism before enabling it. Detect will go high immediately if the sense condition configured in the PIN_CNF registers is met when the sense mechanism is enabled. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism. See *GPIOTE* — *GPIO tasks and events* on page 157.

See the following peripherals for more information about how the DETECT signal is used:

- POWER: uses the DETECT signal to exit from System OFF.
- GPIOTE: uses the DETECT signal to generate the PORT event.

When a pin's PINx.DETECT signal goes high, a flag will be set in the LATCH register, e.g. when the PIN0.DETECT signal goes high, bit 0 in the LATCH register will be set to '1'.

The LATCH register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the LATCH register will not be affected by a PINx.DETECT signal being set low.

If the CPU performs a clear operation on a bit in the LATCH register when the associated PINx.DETECT signal is high, the bit in the LATCH register will not be cleared.

The LDETECT signal will be set high when one or more bits in the LATCH register are '1'. The LDETECT signal will be set low when all bits in the LATCH register are successfully cleared to '0'.

If one or more bits in the LATCH register are '1' after the CPU has performed a clear operation on the LATCH registers, a rising edge will be generated on the LDETECT signal, this is illustrated in *Figure 22: DETECT signal behavior* on page 113.

Important: The CPU can read the LATCH register at any time to check if a SENSE condition has been met on one or more of the the GPIO pins even if that condition is no longer met at the time the CPU queries the LATCH register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change the behaviour of the GPIO port's DETECT signal from the default behaviour described above to instead be derived directly from the LDETECT signal, see *Figure 21: GPIO Port and the GPIO pin details* on page 112. *Figure 22: DETECT signal behavior* on page 113 illustrates the DETECT signals behaviour for these two alternatives.



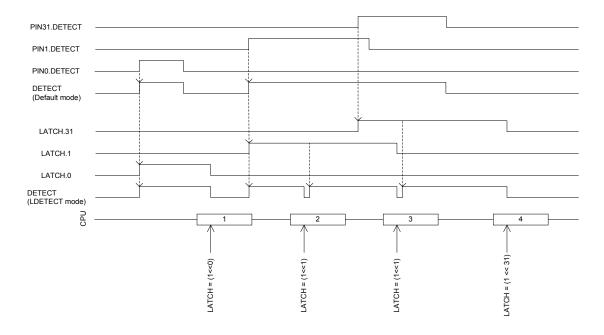


Figure 22: DETECT signal behavior

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see *Figure 21: GPIO Port and the GPIO pin details* on page 112. Inputs must be connected in order to get a valid input value in the IN register and for the sense mechanism to get access to the pin.

Other peripherals in the system can attach themselves to GPIO pins and override their output value and configuration, or read their analog or digital input value, see *Figure 21: GPIO Port and the GPIO pin details* on page 112.

Selected pins also support analog input signals, see ANAIN in *Figure 21: GPIO Port and the GPIO pin details* on page 112. The assignment of the analog pins can be found in *Pin assignments* on page 13.

Important: When a pin is configured as digital input, care has been taken in the nRF52832 design to minimize increased current consumption when the input voltage is between V_{IL} and V_{IH} . However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between V_{IL} and V_{IH} for a long period of time.

20.2 GPIO located near the RADIO

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the radio power supply and antenna pins.

Refer to *Pin assignments* on page 13 for recommended usage guidelines to maximize radio performance in an application.

20.3 Registers

Table 29: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x50000000	GPIO	GPIO	General purpose input and output		Deprecated
0x50000000	GPIO	P0	General purpose input and output		



Table 30: Register Overview

Danista.	04	Paradiation .
Register	Offset	Description Write CRIO part
OUT	0x504	Write GPIO port
OUTSET	0x508	Set individual bits in GPIO port
OUTCLR	0x50C	Clear individual bits in GPIO port
IN	0x510	Read GPIO port
DIR	0x514	Direction of GPIO pins
DIRSET	0x518	DIR set register
DIRCLR	0x51C	DIR clear register
LATCH	0x520	Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE
		registers
DETECTMODE	0x524	Select between default DETECT signal behaviour and LDETECT mode
PIN_CNF[0]	0x700	Configuration of GPIO pins
PIN_CNF[1]	0x704	Configuration of GPIO pins
PIN_CNF[2]	0x708	Configuration of GPIO pins
PIN_CNF[3]	0x70C	Configuration of GPIO pins
PIN_CNF[4]	0x710	Configuration of GPIO pins
PIN_CNF[5]	0x714	Configuration of GPIO pins
PIN_CNF[6]	0x718	Configuration of GPIO pins
PIN_CNF[7]	0x71C	Configuration of GPIO pins
PIN_CNF[8]	0x720	Configuration of GPIO pins
PIN_CNF[9]	0x724	Configuration of GPIO pins
PIN_CNF[10]	0x728	Configuration of GPIO pins
PIN_CNF[11]	0x72C	Configuration of GPIO pins
PIN_CNF[12]	0x730	Configuration of GPIO pins
PIN_CNF[13]	0x734	Configuration of GPIO pins
PIN_CNF[14]	0x738	Configuration of GPIO pins
PIN_CNF[15]	0x73C	Configuration of GPIO pins
PIN_CNF[16]	0x740	Configuration of GPIO pins
PIN_CNF[17]	0x744	Configuration of GPIO pins
PIN_CNF[18]	0x748	Configuration of GPIO pins
PIN_CNF[19]	0x74C	Configuration of GPIO pins
PIN_CNF[20]	0x750	Configuration of GPIO pins
PIN_CNF[21]	0x754	Configuration of GPIO pins
PIN_CNF[22]	0x758	Configuration of GPIO pins
PIN_CNF[23]	0x75C	Configuration of GPIO pins
PIN_CNF[24]	0x760	Configuration of GPIO pins
PIN_CNF[25]	0x764	Configuration of GPIO pins
PIN_CNF[26]	0x768	Configuration of GPIO pins
PIN_CNF[27]	0x76C	Configuration of GPIO pins
PIN_CNF[28]	0x770	Configuration of GPIO pins
PIN_CNF[29]	0x774	Configuration of GPIO pins
PIN_CNF[30]	0x778	Configuration of GPIO pins
PIN_CNF[31]	0x77C	Configuration of GPIO pins

20.3.1 OUT

Address offset: 0x504 Write GPIO port

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	L9 1	L8 1	17 :	16	15	14	13	12 1	1 1) 9	8	7	6	5	4	3	2 1	1 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	V	U .	Т	S	R	Q	Р	О	N	M	L k	J	-1	Н	G	F	Ε	D	C E	3 A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value							De	scrip	tio	n																			
Α	RW	PIN0									Pin	0																					
			Low	0								Pin	driv	⁄er i	is lo	w																	
			High	1							Pin	driv	⁄er i	is hi	igh																		
В	RW	PIN1										Pin	1																				



Bit r	numbe	er		31 30	29 28	27	26 2	5 24	23	22 21	20	19	18	17 1	16 1	.5 1	4 13	12	11	10	9 8	3 7	6	5	4	3 2	! 1	0
Id				f e	d c	b	a 2	<u> </u>	Χ	w v	U	Т	S	R (Q I	P C	N	М	L	K	J I	Н	G	F	Ε	D C	В	Α
Res	et 0x0	0000000		0 0	0 0	0	0 (0	0	0 0	0	0	0	0	0 (0 (0	0	0	0	0 (0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value						escripti																		
			Low	0						n drive																		
			High	1						n drive	r is	high	1															
С	RW	PIN2	Low	0						n 2 n drive	- :-	law																
			High	1						n drive n drive																		
D	RW	PIN3	111611	-						n 3	1 13	iiigii	•															
			Low	0						n drive	r is	low																
			High	1					Pin	n drive	r is	high	1															
E	RW	PIN4							Pir	n 4																		
			Low	0					Pin	n drive	r is	low																
			High	1					Pin	n drive	r is	high	1															
F	RW	PIN5								n 5																		
			Low	0						n drive																		
			High	1						n drive	r is	high	1															
G	RW	PIN6	Laur	0						n 6																		
			Low	0						n drive n drive																		
Н	RW	PIN7	High	1						n 7	1 15	iligii																
	11.44	11117	Low	0						n drive	r is	low																
			High	1						n drive																		
ı	RW	PIN8								n 8		J																
			Low	0					Pin	n drive	r is	low																
			High	1					Pir	n drive	r is	high	1															
J	RW	PIN9							Pin	n 9																		
			Low	0					Pin	n drive	r is	low																
			High	1						n drive	r is	high	1															
K	RW	PIN10	Laur	0						n 10																		
			Low	0						n drive n drive																		
L	RW	PIN11	High	1						n 11	1 15	iligii																
_			Low	0						n drive	r is	low																
			High	1					Pir	n drive	r is	high	ı															
М	RW	PIN12							Pir	n 12																		
			Low	0					Pir	n drive	r is	low																
			High	1					Pin	n drive	r is	high	1															
N	RW	PIN13								n 13																		
			Low	0						n drive																		
	DIA	DINIA	High	1						n drive	r is	high	1															
0	KW	PIN14	Low	0						n 14 n drive	ric	low																
			High	1						n drive																		
Р	RW	PIN15	111611	-						n 15	5																	
			Low	0					Pin	n drive	r is	low																
			High	1					Pin	n drive	r is	high	1															
Q	RW	PIN16							Pir	n 16																		
			Low	0					Pin	n drive	r is	low																
			High	1					Pir	n drive	r is	high	1															
R	RW	PIN17								n 17																		
			Low	0						n drive																		
_	D	DINIAO	High	1						n drive	r is	high	1															
S	RW	PIN18	Low	0						n 18 o drivo	-: س	lev																
			Low High	0						n drive n drive																		
Т	RW	PIN19	5!!							n arive n 19	113	mgn																
			Low	0						n drive	r is	low																



Bitı	numbe	er		31 30	29 :	28 2	27 26	25 2	4 2	23 22 2	1 20	19	18	17	16	15 :	14 1	3 12	11	10	9	8	7	6 5	5 4	3	2	1 0
Id				f e	d	c l	b a	ΖY	Y	x w \	/ U	Т	S	R	Q	Р	0 1	۱ M	L	K	J	L	Н	G I	= E	D	С	ВА
Res	et 0x0	0000000		0 0	0	0 (0 0	0 ()	0 0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Value	•					Descrip	tion																	
			High	1					F	Pin driv	er is	higl	h															
U	RW	PIN20							F	Pin 20																		
			Low	0					F	in driv	er is	low	,															
			High	1					F	in driv	er is	higl	h															
٧	RW	PIN21							F	Pin 21																		
			Low	0					F	Pin driv	er is	low	,															
			High	1					F	Pin driv	er is	higl	h															
W	RW	PIN22							F	Pin 22																		
			Low	0					F	Pin driv	er is	low	,															
			High	1					F	Pin driv	er is	higl	h															
Χ	RW	PIN23							F	Pin 23																		
			Low	0					F	Pin driv	er is	low	,															
			High	1					F	Pin driv	er is	higl	h															
Υ	RW	PIN24							F	Pin 24																		
			Low	0					F	Pin driv	er is	low	,															
			High	1					F	Pin driv	er is	higl	h															
Z	RW	PIN25							F	Pin 25																		
			Low	0					F	Pin driv	er is	low	,															
			High	1					F	Pin driv	er is	higl	h															
а	RW	PIN26							F	Pin 26																		
			Low	0					F	Pin driv	er is	low	1															
			High	1					F	Pin driv	er is	higl	h															
b	RW	PIN27							F	Pin 27																		
			Low	0					F	Pin driv	er is	low	1															
			High	1					F	Pin driv	er is	higl	h															
C	RW	PIN28							F	Pin 28																		
			Low	0					F	Pin driv	er is	low	1															
			High	1					F	Pin driv	er is	higl	h															
d	RW	PIN29							F	Pin 29																		
			Low	0					F	Pin driv	er is	low	1															
			High	1					F	Pin driv	er is	higl	h															
e	RW	PIN30							F	Pin 30																		
			Low	0					F	Pin driv	er is	low	'															
			High	1					F	Pin driv	er is	higl	h															
f	RW	PIN31							F	Pin 31																		
			Low	0					F	Pin driv	er is	low	,															
			High	1					F	Pin driv	er is	higl	h															

20.3.2 OUTSET

Address offset: 0x508

Set individual bits in GPIO port

Read: reads value of OUT register.

Bit number		31	30	29	28 :	27 :	26 2	5 2	24 2	3 2	2 2:	1 20	19	18	17	16	15	14	13 1	12 1	1 10	9	8	7	6	5 4	1 3	2	1 0
Id		f	е	d	С	b	a :	Z	Υ :	x v	V V	/ U	Т	S	R	Q	Р	О	N I	Μl	. K	J	1	Н	G	F E	D	С	В А
Reset 0x00000000		0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0 0
ld RW Field	Value Id	Va	lue						C	esc	ript	tion																	
A RW PINO									Р	in C)																		
	Low	0							R	lead	l: pi	n dr	ive	r is l	ow														
	High	0 1				R	lead	l: pi	n dr	ive	r is l	high	1																
	Set	1							٧	Vrit	e: w	/ritii	ng a	1'1	set	s th	e pi	n h	gh;	writ	ing	a '0'	has	no	effe	ct			
B RW PIN1									P	in 1	L																		
	Low	0						R	lead	l: pi	n dr	ive	r is l	ow															



Bitı	numbe	er		31 30	29 28	27 26	25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value				Description
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
С	RW	PIN2	Loui	0				Pin 2
			Low	0				Read: pin driver is low Read: pin driver is high
			High Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
D	RW	PIN3	361	_				Pin 3
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Ε	RW	PIN4						Pin 4
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
F	RW	PIN5						Pin 5
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
_	DIA	DINIC	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
G	KVV	PIN6	Low	0				Pin 6 Read: pin driver is low
			High	1				Read: pin driver is low
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Н	RW	PIN7						Pin 7
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
I	RW	PIN8						Pin 8
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
J	RW	PIN9						Pin 9
			Low	0				Read: pin driver is low
			High Set	1				Read: pin driver is high Write: writing a '1' sets the pin high; writing a '0' has no effect
K	RW	PIN10	Set	1				Pin 10
		111120	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
L	RW	PIN11						Pin 11
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
M	RW	PIN12						Pin 12
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
N.	Ditt	DINI12	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
N	KW	PIN13	Low	0				Pin 13 Read: pin driver is low
			High	1				Read: pin driver is low Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
0	RW	PIN14						Pin 14
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Р	RW	PIN15						Pin 15



Bit n	umbe	r		31 30	29 28	27 26	6 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	t 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Q	RW	PIN16						Pin 16
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
	D\4/	DINIA 7	Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
R	KVV	PIN17	Low	0				Pin 17
			High	1				Read: pin driver is low Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
S	R\M/	PIN18	Set	1				Pin 18
5	11.00	TINIO	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Т	RW	PIN19		-				Pin 19
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
U	RW	PIN20						Pin 20
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
٧	RW	PIN21						Pin 21
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
W	RW	PIN22						Pin 22
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Х	RW	PIN23						Pin 23
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
.,			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
Υ	RW	PIN24		•				Pin 24
			Low	0				Read: pin driver is low
			High Set	1				Read: pin driver is high Write: writing a '1' sets the pin high; writing a '0' has no effect
Z	R\M/	PIN25	Set	1				Pin 25
_	1.00	1 11423	Low	0				Read: pin driver is low
			High	1				Read: pin driver is low
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
а	RW	PIN26		_				Pin 26
-	•		Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
b	RW	PIN27						Pin 27
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect
С	RW	PIN28						Pin 28
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Set	1				Write: writing a '1' sets the pin high; writing a '0' has no effect



Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20	19	18	17	16	15	14	13 1	12 1	1 10	9	8	7	6	5	4	3	2 1	. 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	V	U	Т	S	R	Q	Р	О	N I	M	L K	J	-1	Н	G	F	Ε	D	C E	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0
ld	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
d	RW	PIN29										Pin	29																				
			Low	0								Rea	ıd: p	in (driv	/er	is lo	ow															
			High	1								Rea	ıd: p	in (driv	/er	is h	igh															
			Set	1							,	Wri	te:	wri	ting	g a ˈ	1' :	sets	th	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				
е	RW	PIN30										Pin	30																				
			Low	0								Rea	d: p	in (driv	/er	is lo	wc															
			High	1								Rea	ıd: p	in (driv	/er	is h	igh															
			Set	1							,	Wri	te:	wri	ting	g a '	1' :	sets	th	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				
f	RW	PIN31										Pin	31																				
			Low	0								Rea	ıd: p	in (driv	/er	is lo	ow															
			High	1								Rea	d: p	in (driv	/er	is h	igh															
			Set	1								Wri	te:	wri	ting	g a '	1' :	sets	th	e pi	n h	igh;	wri	ting	a '0	' ha	s no	eff	ect				

20.3.3 OUTCLR

Address offset: 0x50C

Clear individual bits in GPIO port Read: reads value of OUT register.

Bit r	numb	er		3	31 30	29	28	27	26	25	24	2	23 22 21	. 20	19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4 3	2	1	C
Id				f	е	d	С	b	а	Z	Υ	>	x w v	U	Т	S	R	Q	Р	0	Ν	М	L	K	J	1	н	G	F	E C) C	В	1
Rese	et OxC	0000000		C	0	0	0	0	0	0	0	(0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	-
ld	RW	Field	Value Id	١	/alue	•						D	escript	ion																			
Α	RW	PIN0										Р	in 0																				
			Low	C)							R	Read: pir	n dr	ive	r is	low																
			High	1								R	Read: pir	n dr	ive	r is	hig	า															
			Clear	1								٧	Vrite: w	ritii	ng a	1'	set	s th	ie p	in l	ow;	wr	itin	g a	'0' ł	nas	no e	effe	ct				
В	RW	PIN1										Р	in 1																				
			Low	C)							R	Read: pir	n dr	ive	r is	low																
			High	1								R	Read: pir	n dr	ive	r is	hig	า															
			Clear	1								٧	Vrite: w	ritii	ng a	1' a	set	s th	ie p	in l	ow;	wr	itin	g a	'0' ł	nas	no (effe	ct				
С	RW	PIN2										Р	in 2																				
			Low	C)							R	Read: pir	n dr	ive	r is	low																
			High	1								R	Read: pir	n dr	ive	r is	hig	า															
			Clear	1								٧	Vrite: w	ritii	ng a	1' a	set	s th	ie p	in I	ow;	wr	itin	g a	'0' ł	nas	no e	effe	ct				
D	RW	PIN3										Р	in 3																				
			Low	C)							R	Read: pir	n dr	ive	r is	low																
			High	1								R	Read: pir	n dr	ive	r is	hig	า															
			Clear	1								٧	Vrite: w	ritii	ng a	1'1	set	s th	ie p	in l	ow;	wr	itin	g a	'0' ŀ	nas	no e	effe	ct				
E	RW	PIN4										Р	in 4																				
			Low	C)							R	Read: pir	n dr	ive	r is	low																
			High	1								R	Read: pir	n dr	ive	r is	hig	า															
			Clear	1								٧	Vrite: w	ritii	ng a	1'	set	s th	ie p	in l	ow;	wr	itin	g a	'0' ł	nas	no (effe	ct				
F	RW	PIN5										Р	in 5																				
			Low	()							R	Read: pir	n dr	ive	r is	low																
			High	1								R	Read: pir	n dr	ive	r is	hig	า															
			Clear	1								٧	Vrite: w	ritii	ng a	1' a	set	s th	ie p	in l	ow;	wr	itin	g a	'0' ł	nas	no (effe	ct				
G	RW	PIN6										Р	in 6																				
			Low	C)							R	Read: pir	n dr	ive	r is	low																
			High	1								R	Read: pir	n dr	ive	r is	hig	า															
			Clear	1								٧	Vrite: w	ritii	ng a	1' a	set	s tł	ie p	in l	ow;	wr	itin	g a	'0' ł	nas	no (effe	ct				
Н	RW	PIN7										Р	in 7																				
			Low	()							R	Read: pir	n dr	ive	r is	low																
			High	1								R	Read: pir	n dr	ive	r is	hig	า															



Bit n	umbe	er		31 30	29 28	27 20	6 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z	Y X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000		0 0	0 0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
I	RW	PIN8		_				Pin 8
			Low	0				Read: pin driver is low
			High Clear	1				Read: pin driver is high Write: writing a '1' sets the pin low; writing a '0' has no effect
	RW	PIN9	Clear	1				Pin 9
,		11145	Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
K	RW	PIN10						Pin 10
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
L	RW	PIN11						Pin 11
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
	DVA	DINI4 2	Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
M	KVV	PIN12	Low	0				Pin 12 Read: pin driver is low
			High	1				Read: pin driver is low
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
N	RW	PIN13						Pin 13
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
0	RW	PIN14						Pin 14
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
-	DIA	DINIAE	Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
Р	KW	PIN15	Low	0				Pin 15
			Low High	1				Read: pin driver is low Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
Q	RW	PIN16		_				Pin 16
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
R	RW	PIN17						Pin 17
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
S	кW	PIN18	Low	0				Pin 18
			Low High	0				Read: pin driver is low Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
т	RW	PIN19	Cicui	•				Pin 19
·			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
U	RW	PIN20						Pin 20
			Low	0				Read: pin driver is low
			High	1				Read: pin driver is high
			Clear	1				Write: writing a '1' sets the pin low; writing a '0' has no effect
V	RW	PIN21						Pin 21
			Low	0				Read: pin driver is low



Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				fedcbaZY	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
W	RW	PIN22			Pin 22
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Χ	RW	PIN23			Pin 23
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
Υ	RW	PIN24			Pin 24
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
Z	D\A/	PIN25	Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect Pin 25
_	I VV	PINZO	Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
а	RW	PIN26	oleu.		Pin 26
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
b	RW	PIN27			Pin 27
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
С	RW	PIN28			Pin 28
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
d	RW	PIN29			Pin 29
			Low	0	Read: pin driver is low
			High	1	Read: pin driver is high
	Dist	DINIO	Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
е	кW	PIN30	Low	0	Pin 30
			Low	0	Read: pin driver is low
			High Clear	1	Read: pin driver is high Write: writing a '1' sets the pin low; writing a '0' has no effect
f	R\M/	PIN31	Cical	_	Pin 31
	11.00	11131	Low	0	Read: pin driver is low
			High	1	Read: pin driver is low
			Clear	1	Write: writing a '1' sets the pin low; writing a '0' has no effect
			2.20.	-	

20.3.4 IN

Address offset: 0x510 Read GPIO port

Bitı	numbe	er		31	1 30	29	28	27	7 26	5 25	5 2	4 2	3 2	2 2	1 2	0 19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				f	е	d	С	b	а	Z	. Y	<i>(</i>)	(V	v v	/ L	ı T	S	R	Q	Р	0	Ν	М	L	K	J	1	Н	G	F	Ε	D	С	ВА
Res	et 0x0	0000000		0	0	0	0	0	0	0) () () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue	:						D	esc	ript	tion																			
Α	R	PIN0										Р	in C)																				
			Low	0								Р	in i	npu	t is	low																		
			High	1								D	in i	าทเเ	t ic	hig	1																	



Bit r	numbe	er		31 30	29 2	8 27	26 2	25 24	1 23	22 21	20	19 1	8 17	7 16	15	14 1	3 12	11	10 !	9 8	7	6	5 4	4 3	2	1 (
Id										W V																
Rese	et 0x0	0000000		0 0	0 0	0	0	0 0	0	0 0	0	0	0 0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0 (
Id	RW	Field	Value Id	Value					De	escripti	ion															
В	R	PIN1							Pin																	
			Low	0						n input																
			High	1						n input	is h	nigh														
С	R	PIN2								n 2 																
			Low	0						n input n input																
D	R	PIN3	High	1						n 3	15 1	ııgıı														
		11145	Low	0						n input	is le	οw														
			High	1						n input																
E	R	PIN4	-						Pir			-														
			Low	0					Pir	n input	is l	ow														
			High	1					Pin	n input	is h	nigh														
F	R	PIN5							Pin	n 5																
			Low	0					Pin	n input	is l	ow														
			High	1						n input	is h	nigh														
G	R	PIN6							Pin																	
			Low	0						n input																
		DINIZ	High	1						n input	is h	nigh														
Н	R	PIN7	Low	0					Pin	n / n input	ic l	014														
			High	1						n input																
1	R	PIN8	111611	-					Pin		131	''B''														
	•••		Low	0						n input	is l	ow														
			High	1						n input																
J	R	PIN9							Pin	n 9																
			Low	0					Pin	n input	is l	ow														
			High	1					Pin	n input	is h	nigh														
K	R	PIN10							Pin	n 10																
			Low	0					Pin	n input	is l	ow														
			High	1						n input	is h	nigh														
L	R	PIN11								n 11																
			Low	0						n input																
М	R	PIN12	High	1						n input n 12	IS I	ııgn														
IVI	IX.	FINIZ	Low	0						n input	is le	οw														
			High	1						n input																
N	R	PIN13	· ·							n 13																
			Low	0						n input	is l	ow														
			High	1						n input																
0	R	PIN14							Pir	n 14																
			Low	0						n input																
			High	1						n input	is h	nigh														
Р	R	PIN15								n 15																
			Low	0						n input																
_	D	DINI16	High	1						n input	is h	nigh														
Q	R	PIN16	Low	0						n 16 n input	ic I	014														
			Low High	1						n input n input																
R	R	PIN17	6!!							n 117	101	ıığı I														
.,			Low	0						n input	is le	ow														
			High	1						n input																
S	R	PIN18	-							n 18		,														
			Low	0						n input	is l	ow														
			High	1					Pin	n input	is h	nigh														
Т	R	PIN19							Pir	n 19																



Bit r	numbe	er		31 30	29	28 2	27 26	25 2	24	23 22	21	20 1	9 1	18 1	7 1	16 1	15 :	L4 1	3 12	2 1:	10	9	8	7	6	5	4	3 2	1	0
Id				f e	d	С	b a	Z	Υ	x w	V	U T	Г	S F	۲ ا	Q	Р	1 0	N N	1 L	K	J	T	Н	G	F	Ε	D C	В	Δ
Res	et 0x0	0000000								0 0																				
Id		Field	Value Id	Value						Descri																				
			Low	0						Pin inp			v																	
			High	1						Pin inp																				
U	R	PIN20	3							Pin 20																				
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
٧	R	PIN21								Pin 21																				
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
W	R	PIN22	3							Pin 22																				
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
Χ	R	PIN23	5							Pin 23			,																	
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
Υ	R	PIN24		_						Pin 24			,																	
•	•••		Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
Z	R	PIN25								Pin 25			•••																	
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
a	R	PIN26	5							Pin 26		. 0	,																	
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
b	R	PIN27	<u> </u>							Pin 27																				
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp	ut i	s hig	gh																	
С	R	PIN28	-							Pin 28		_																		
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp	ut i	s hig	gh																	
d	R	PIN29								Pin 29																				
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
e	R	PIN30								Pin 30																				
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
f	R	PIN31								Pin 31																				
			Low	0						Pin inp	ut i	s lov	v																	
			High	1						Pin inp																				
			-																											

20.3.5 DIR

Address offset: 0x514 Direction of GPIO pins

Bit r	numbe	er		31	30	29	28	27	26 2	25	24 2	23 2	22 2	21 2	0 1	9 1	8 1	7 1	5 1	5 14	4 13	3 12	2 11	10	9	8	7	6	5	4	3	2 :	1 0
Id				f	е	d	С	b	a :	Z	Υ	X١	٧V	νι	. ر	Т 9	S F	2 C) P	C	N	M	l L	K	J	1	н	G	F	Ε	D	C E	ВА
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0 (0 ()	0 () () (0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	ı																		
Α	RW	PIN0									F	Pin (0																				
			Input	0							F	Pin :	set	as ii	าрเ	ıt																	
			Output	1							F	Pin :	set	as c	utp	out																	
В	RW	PIN1									F	Pin	1																				
			Input	0							F	Pin :	set	as ii	าрเ	ıt																	
			Output	1							F	Pin :	set	as c	utp	out																	
С	RW	PIN2									F	Pin :	2																				



D:+				21.20	. 20	20.25	7 20 1	DE 24	22.2	22.21	20.10	2 10	17	10 1	г 1	4 12	12.1	1 10	0	0 .	7 ,	· -	4	2 2	1	0
Bit r	umbe	er ·		31 30 f e																						
	t 0x0	000000		0 0																						
		Field	Value Id	Value						criptio																
			Input	0						set as		t														
			Output	1					Pin s	set as	outp	ut														
D	RW	PIN3							Pin 3	3																
			Input	0					Pin s	set as	input	t														
			Output	1					Pin s	set as	outp	ut														
Ε	RW	PIN4							Pin 4	4																
			Input	0					Pin s	set as	input	t														
			Output	1					Pin	set as	outp	ut														
F	RW	PIN5							Pin 5	5																
			Input	0					Pin s	set as	input	t														
			Output	1					Pin s	set as	outp	ut														
G	RW	PIN6							Pin 6	6																
			Input	0					Pin s	set as	input	t														
			Output	1						set as	outp	ut														
Н	RW	PIN7							Pin 7																	
			Input	0						set as																
			Output	1						set as	outp	ut														
I	RW	PIN8							Pin 8																	
			Input	0						set as																
	5111		Output	1						set as	outp	ut														
J	RW	PIN9							Pin 9																	
			Input	0						set as																
K	D\A/	PIN10	Output	1					Pin S	set as	outp	ut														
K	NVV	PINIO	Input	0						set as	innut															
			Output	1						set as																
L	RW	PIN11	Cutput	•					Pin :		outp	ut														
-			Input	0						set as	input	t														
			Output	1						set as																
М	RW	PIN12							Pin :		·															
			Input	0					Pin s	set as	input	t														
			Output	1					Pin s	set as	outp	ut														
N	RW	PIN13							Pin :	13																
			Input	0					Pin s	set as	input	t														
			Output	1					Pin	set as	outp	ut														
0	RW	PIN14							Pin :	14																
			Input	0					Pin	set as	input	t														
			Output	1					Pin s	set as	outp	ut														
Р	RW	PIN15							Pin :																	
			Input	0						set as																
			Output	1						set as	outp	ut														
Q	RW	PIN16							Pin :																	
			Input	0						set as																
_	5111		Output	1						set as	outp	ut														
R	KW	PIN17	lanut	0					Pin :		lm															
			Input	0						set as																
ç	DIA	DINI19	Output	1						set as	outp	ut														
S	πVV	PIN18	Innut	0					Pin :	18 set as	inner															
			Input Output	1						set as set as																
Т	B/W	PIN19	σαιραί						Pin :		outp	ut														
	IVV	1 11473	Input	0						set as	innut															
			Output	1						set as set as																
U	B/W	PIN20	Catput	1					Pin 2		outp	ut														
5			Input	0						set as	innut	t														
				-					3	: us	pui	-														



Bitı	numbe	er		31 30	29	28 2	27 26	25 2	24 :	23 2:	2 21	20 19	9 18	3 17	16	15 3	14 1	3 12	11	10 9	9 8	3 7	6	5	4	3 2	1	0
Id				f e	d	С	b a	Z	Υ	x v	N V	U T	S	R	Q	Р	0 1	I M	L	Κ.	JI	Н	G	F	Е	D C	В	Α
Res	et 0x0	0000000		0 0	0	0	0 0	0	0	0 0	0 0	0 0	0	0	0	0	0 0	0	0	0 (0 (0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value					1	Desc	criptio	on																
			Output	1						Pin s	et as	outp	ut															
٧	RW	PIN21							-	Pin 2	21																	
			Input	0					ı	Pin s	et as	input																
			Output	1					ı	Pin s	et as	outp	ut															
W	RW	PIN22							-	Pin 2	22																	
			Input	0					-	Pin s	et as	input	:															
			Output	1					-	Pin s	et as	outp	ut															
Χ	RW	PIN23							- 1	Pin 2	23																	
			Input	0					-	Pin s	et as	input																
			Output	1					-	Pin s	et as	outp	ut															
Υ	RW	PIN24							- 1	Pin 2	24																	
			Input	0					-	Pin s	et as	input	:															
			Output	1					-	Pin s	et as	outp	ut															
Z	RW	PIN25							-	Pin 2	25																	
			Input	0					-	Pin s	et as	input	:															
			Output	1					-	Pin s	et as	outp	ut															
а	RW	PIN26							-	Pin 2	26																	
			Input	0					-	Pin s	et as	input	:															
			Output	1					-	Pin s	et as	outp	ut															
b	RW	PIN27							- 1	Pin 2	27																	
			Input	0					- 1	Pin s	et as	input	:															
			Output	1					- 1	Pin s	et as	outp	ut															
С	RW	PIN28							1	Pin 2	28																	
			Input	0					1	Pin s	et as	input	:															
			Output	1					١	Pin s	et as	outp	ut															
d	RW	PIN29							-	Pin 2	29																	
			Input	0					- 1	Pin s	et as	input																
			Output	1					- 1	Pin s	et as	outp	ut															
е	RW	PIN30							1	Pin 3	30																	
			Input	0					١	Pin s	et as	input																
			Output	1					١	Pin s	et as	outp	ut															
f	RW	PIN31							-	Pin 3	31																	
			Input	0					-	Pin s	et as	input																
			Output	1					- 1	Pin s	et as	outp	ut															

20.3.6 DIRSET

Address offset: 0x518

DIR set register

Read: reads value of DIR register.

Bit number		31	30	29 2	28 2	27 2	6 2	5 2	4 2	23 2	22 2	1 2	0 1	9 18	3 17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	1	0
Id		f	e	d	С	b a	a Z	Z \	Υ :	X١	W١	/ L	J 1	S	R	Q	Р	0	Ν	М	L	K	J	I	Н	G	F	Ε) C	В	Α
Reset 0x00000000		0	0	0	0	0 (0 (0 ()	0 (0 (0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id RW Field	Value Id	Val	lue						0	Des	crip	tior	1																		
A RW PINO									S	Set a	as o	utp	ut p	oin ()																
1	Input	0							F	Read	d: p	in s	et a	s in	put																
	Output	1							F	Read	d: p	in s	et a	s o	ıtpı	t															
!	Set	1							٧	Nrit	te: v	vrit	ing	a '1	set	s pi	n to	ou	tpu	t; w	riti	ng a	o '0	' ha	s n	o ef	ffec	t			
B RW PIN1									S	Set a	as o	utp	ut p	oin :	L																
1	Input	0							F	Read	d: p	in s	et a	s in	put																
	Output	1							F	Read	d: p	in s	et a	s o	ıtpı	t															
:	Set	1							٧	Nrit	te: v	vrit	ing	a '1	set	s pi	n to	ou	tpu	t; w	riti	ng a	o '0	' ha	s n	o ef	ffec	t			
C RW PIN2									S	et a	as o	utp	ut p	oin 2	2																



Bit n	umbe	er		31 30	29 28	27 26	5 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	ΖV	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	t 0x0	0000000		0 0	0 0	0 0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
_	5111		Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
D	RW	PIN3		•				Set as output pin 3
			Input	0				Read: pin set as input
			Output Set	1				Read: pin set as output Write: writing a '1' sets pin to output; writing a '0' has no effect
E	RW	PIN4	Set	-				Set as output pin 4
-		11144	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
F	RW	PIN5						Set as output pin 5
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
G	RW	PIN6						Set as output pin 6
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Н	RW	PIN7						Set as output pin 7
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
I	RW	PIN8						Set as output pin 8
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
	DIA	DINIO	Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
J	RW	PIN9	la acat	0				Set as output pin 9
			Input	0				Read: pin set as input
			Output Set	1				Read: pin set as output Write: writing a '1' sets pin to output; writing a '0' has no effect
K	R\M	PIN10	Jet	1				Set as output pin 10
K	11.00	11110	Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
L	RW	PIN11						Set as output pin 11
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
М	RW	PIN12						Set as output pin 12
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
N	RW	PIN13						Set as output pin 13
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
0	RW	PIN14						Set as output pin 14
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect
Р	RW	PIN15						Set as output pin 15
			Input	0				Read: pin set as input
			Output	1				Read: pin set as output
			Set	1				Write: writing a '1' sets pin to output; writing a '0' has no effect



Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Res	set 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Q	RW PIN16		Set as output pin 16
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
_	5111 51114 5	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
R	RW PIN17		Set as output pin 17
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
_	DIA DINIA	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
S	RW PIN18	la acce	Set as output pin 18
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
_	DW DINIAO	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
Т	RW PIN19	lanut	Set as output pin 19
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
	RW PIN20	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
U	RW PINZU	la acat	Set as output pin 20
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
.,	DIA/ DINI24	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
V	RW PIN21	la acce	Set as output pin 21
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
	DIA DINIZZ	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
W	RW PIN22	la acat	Set as output pin 22
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
V	DW DIN22	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
Х	RW PIN23	la acce	Set as output pin 23
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
Υ	DW DINGA	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
T	RW PIN24	lanut	Set as output pin 24
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
7	DW DINIZE	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
Z	RW PIN25	lanut	Set as output pin 25
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output 1 Write: writing a '1' sets pin to output; writing a '0' has no effect
2	RW PIN26	Set	
а	NVV PIINZO	Innut	Set as output pin 26 O Read: pin set as input
		Input Output	· · · · · · · · · · · · · · · · · · ·
		·	1 Read: pin set as output
h	DW/ DINI27	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
b	RW PIN27	Innut	Set as output pin 27
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output Write: writing a '1' sets pin to output: writing a '0' has no offect
_	DW/ DINI20	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
С	RW PIN28	loout	Set as output pin 28
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
	DIM DINIO	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
d	RW PIN29	lanet	Set as output pin 29
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
e RW PIN30		Set as output pin 30
	Input	0 Read: pin set as input
	Output	1 Read: pin set as output
	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect
f RW PIN31		Set as output pin 31
	Input	0 Read: pin set as input
	Output	1 Read: pin set as output
	Set	1 Write: writing a '1' sets pin to output; writing a '0' has no effect

20.3.7 DIRCLR

Address offset: 0x51C

DIR clear register

Read: reads value of DIR register.

Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZY	Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	
ld	RW Field	Value Id	Value	Description
Α	RW PINO			Set as input pin 0
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
В	RW PIN1			Set as input pin 1
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
С	RW PIN2			Set as input pin 2
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
D	RW PIN3			Set as input pin 3
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
E	RW PIN4			Set as input pin 4
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
F	RW PIN5			Set as input pin 5
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
G	RW PIN6			Set as input pin 6
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
Н	RW PIN7			Set as input pin 7
		Input	0	Read: pin set as input
		Output	1	Read: pin set as output
		Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect
I	RW PIN8			Set as input pin 8
		Input	0	Read: pin set as input



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW Field	Value Id	Value Description
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
J	RW PIN9		Set as input pin 9
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
K	RW PIN10		Set as input pin 10
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
L	RW PIN11		Set as input pin 11
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
М	RW PIN12		Set as input pin 12
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
	B	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
N	RW PIN13		Set as input pin 13
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
_	DIA DINA	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
0	RW PIN14		Set as input pin 14
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
Р	DIA DINIE	Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Р	RW PIN15	lanut	Set as input pin 15
		Input	0 Read: pin set as input 1 Read: pin set as output
		Output Clear	1 Read: pin set as output 1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Q	RW PIN16	Cledi	Set as input pin 16
Q	KW FINIO	Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
R	RW PIN17	Cicui	Set as input pin 17
	111127	Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
S	RW PIN18		Set as input pin 18
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
Т	RW PIN19		Set as input pin 19
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
U	RW PIN20		Set as input pin 20
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
٧	RW PIN21		Set as input pin 21
		Input	0 Read: pin set as input
		Output	1 Read: pin set as output
		Clear	1 Write: writing a '1' sets pin to input; writing a '0' has no effect
W	RW PIN22		Set as input pin 22
••			mpac p ==



Bit r	number			31 30	29 2	8 2	7 26	25 2	4 :	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id				f e	d d	c l	о а	Z '	Y	X W V U T S R Q P O N M L K J I H G F E D C B /
Res	et 0x0000	0000		0 0	0 () (0 0	0 (ס	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Fie	ld	Value Id	Value					1	Description
			Input	0						Read: pin set as input
			Output	1					ı	Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect
Χ	RW PIN	N23							:	Set as input pin 23
			Input	0					ı	Read: pin set as input
			Output	1					1	Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect
Υ	RW PIN	N24							:	Set as input pin 24
			Input	0					١	Read: pin set as input
			Output	1					١	Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect
Z	RW PIN	N25							:	Set as input pin 25
			Input	0					ı	Read: pin set as input
			Output	1					ı	Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect
а	RW PIN	126							:	Set as input pin 26
			Input	0					١	Read: pin set as input
			Output	1					ı	Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect
b	RW PIN	N27							:	Set as input pin 27
			Input	0					1	Read: pin set as input
			Output	1					1	Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect
С	RW PIN	N28							:	Set as input pin 28
			Input	0					١	Read: pin set as input
			Output	1					١	Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect
d	RW PIN	129							:	Set as input pin 29
			Input	0					١	Read: pin set as input
			Output	1					١	Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect
е	RW PIN	130							:	Set as input pin 30
			Input	0						Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect
f	RW PIN	N31								Set as input pin 31
			Input	0					- 1	Read: pin set as input
			Output	1						Read: pin set as output
			Clear	1					١	Nrite: writing a '1' sets pin to input; writing a '0' has no effect

20.3.8 LATCH

Address offset: 0x520

Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers

Bit n	umbe	er		31	. 30	29	28	27	26 2	25	24 :	23 :	22 2	21 2	0 1	19 1	8 1	7 1	5 15	5 14	13	12	11	10	9	8	7 (5 5	4	3	2	1 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	V	J	Т :	5 1	R C	Į P	0	Ν	М	L	K	J	I I	1 (G F	Е	D	С	ВА
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0 () (0 0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0 0
Id	RW	Field	Value Id	Va	llue						ı	Des	crip	otio	n																	
Α	RW	PIN0									:	Stat	tus	on v	vhe	ethe	r Pl	N0	nas	me	t cr	iteri	a se	t in	PII	N_CN	IF0	.SEN	ISE			
											-	regi	iste	r. W	rite	e '1'	to	clea	r.													
			NotLatched	0							(Crit	eria	ha:	s no	ot b	eer	me	t													
			Latched	1							(Crit	eria	ha:	s be	een	me	t														
В	RW	PIN1									:	Stat	tus	on v	vhe	ethe	r Pl	N1	nas	me	t cr	iteri	a se	t in	PIN	N_CN	IF1	.SEN	ISE			
												regi	iste	r. W	rite	e '1'	to	clea	r.													



Bitı	numbe	er		31 30	29 28	27 26	5 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								XWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	:			Description
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
С	RW	PIN2						Status on whether PIN2 has met criteria set in PIN_CNF2.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
D	RW	PIN3						Status on whether PIN3 has met criteria set in PIN_CNF3.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
_	DIA	DINIA	Latched	1				Criteria has been met
E	KW	PIN4						Status on whether PIN4 has met criteria set in PIN_CNF4.SENSE
			NotLatched	0				register. Write '1' to clear. Criteria has not been met
			Latched	1				Criteria has been met
F	RW	PIN5	Latericu	-				Status on whether PIN5 has met criteria set in PIN_CNF5.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
G	RW	PIN6						Status on whether PIN6 has met criteria set in PIN_CNF6.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
Н	RW	PIN7						Status on whether PIN7 has met criteria set in PIN_CNF7.SENSE
								register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
I	RW	PIN8						Status on whether PIN8 has met criteria set in PIN_CNF8.SENSE
				_				register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
	DIA	DINO	Latched	1				Criteria has been met
J	KVV	PIN9						Status on whether PIN9 has met criteria set in PIN_CNF9.SENSE
			NotLatched	0				register. Write '1' to clear. Criteria has not been met
			Latched	1				Criteria has been met
K	RW	PIN10	Laterica	-				Status on whether PIN10 has met criteria set in
		20						PIN_CNF10.SENSE register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
L	RW	PIN11						Status on whether PIN11 has met criteria set in
								PIN_CNF11.SENSE register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
М	RW	PIN12						Status on whether PIN12 has met criteria set in
								PIN_CNF12.SENSE register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
N	RW	PIN13						Status on whether PIN13 has met criteria set in
								PIN_CNF13.SENSE register. Write '1' to clear.
			NotLatched	0				Criteria has not been met
			Latched	1				Criteria has been met
0	RW	PIN14						Status on whether PIN14 has met criteria set in
			Not atched	0				PIN_CNF14.SENSE register. Write '1' to clear.
			NotLatched Latched	0				Criteria has not been met Criteria has been met
			Latched	1				Criteria nas Deen met



Bitı	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				Y X W V U T S R Q P O N M L K J I H G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Р	RW PIN15			Status on whether PIN15 has met criteria set in
				PIN_CNF15.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
Q	RW PIN16			Status on whether PIN16 has met criteria set in
		NI-41-4-bd	0	PIN_CNF16.SENSE register. Write '1' to clear.
		NotLatched Latched	0 1	Criteria has not been met Criteria has been met
R	RW PIN17	Laterieu	1	Status on whether PIN17 has met criteria set in
				PIN_CNF17.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
S	RW PIN18			Status on whether PIN18 has met criteria set in
				PIN_CNF18.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
Т	RW PIN19			Status on whether PIN19 has met criteria set in
				PIN_CNF19.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
U	RW PIN20			Status on whether PIN20 has met criteria set in
			_	PIN_CNF20.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
.,	DIA DIAI24	Latched	1	Criteria has been met
V	RW PIN21			Status on whether PIN21 has met criteria set in
		NotLatched	0	PIN_CNF21.SENSE register. Write '1' to clear. Criteria has not been met
		Latched	1	Criteria has been met
W	RW PIN22			Status on whether PIN22 has met criteria set in
				PIN_CNF22.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
Χ	RW PIN23			Status on whether PIN23 has met criteria set in
				PIN_CNF23.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
Υ	RW PIN24			Status on whether PIN24 has met criteria set in
				PIN_CNF24.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
7	RW PIN25	Latched	1	Criteria has been met
Z	IVAN LINGS			Status on whether PIN25 has met criteria set in PIN_CNF25.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
a	RW PIN26	-		Status on whether PIN26 has met criteria set in
				PIN_CNF26.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
b	RW PIN27			Status on whether PIN27 has met criteria set in
				PIN_CNF27.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met
		Latched	1	Criteria has been met
С	RW PIN28			Status on whether PIN28 has met criteria set in
				PIN_CNF28.SENSE register. Write '1' to clear.
		NotLatched	0	Criteria has not been met



Bit number			31	30 2	29 2	8 27	7 26	25	24	23 2	22 23	L 20	19	18	17 1	16	15 1	L4 1	.3 12	2 11	10	9	8	7 6	5 5	4	3	2	1 0
Id			f	e	d d	b b	а	Z	Υ	X '	w v	U	Т	S	R	Q	Р	0 1	N M	l L	K	J	I I	1 (6 F	Ε	D	С	ВА
Reset 0x0000	00000		0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0 () (0	0	0	0	0 0
Id RW Fie	eld V	/alue Id	Val	ue						Des	cript	ion																	
	L	atched	1							Crit	eria l	nas	bee	n m	et														
d RW PI	N29									Stat	tus o	n wl	heth	er f	PIN2	9 h	as r	net	crite	eria	set i	n							
										PIN _.	_CNF	29.	SEN	SE r	egis	ter	. Wı	rite	'1' to	o cle	ar.								
	N	lotLatched	0							Crit	eria l	nas	not	bee	n m	et													
	L	atched	1							Crit	eria l	nas	bee	n m	et														
e RW PI	N30									Stat	tus o	n wl	heth	er f	PIN3	0 h	as r	net	crite	eria	set i	n							
										PIN _.	_CNF	30.	SEN	SE r	egis	ter	. W	rite	'1' to	o cle	ar.								
	N	lotLatched	0							Crit	eria l	nas	not	bee	n m	et													
	L	atched	1							Crit	eria l	nas	bee	n m	et														
f RW PI	N31									Stat	tus o	n wl	heth	er f	PIN3	1 h	as r	net	crite	eria	set i	n							
										PIN _.	_CNF	31.	SEN	SE r	egis	ter	. W	rite	'1' to	o cle	ar.								
	N	NotLatched	0							Crit	eria l	nas	not	bee	n m	et													
	L	atched	1							Crit	eria l	nas	bee	n m	et														

20.3.9 DETECTMODE

Address offset: 0x524

Select between default DETECT signal behaviour and LDETECT mode

Bitı	numbe	r		31	1 30	29	28	27	26	25	24	23	22	21	20	19 1	18 :	17 1	.6 1	L5 1	4 1	3 12	2 11	. 10	9	8	7	6	5	4	3	2 :	1 ()
Id																																	A	Ą
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0 (0 0)
Id	RW	Field	Value Id	Va	alue	:						De	scri	ptio	n																			
Α	RW	DETECTMODE										Sel	ect	bet	we	en d	lefa	ult	DE	TEC	Γsi	gnal	bel	navi	our	and	d LC	ETE	CT					
												mo	de																					
			Default	0								DE	TEC	T di	rec	tly c	on	nec	ted	to	PIN	DET	EC1	sig	nal	S								
			LDETECT	1								Use	e th	e la	tch	ed L	DE.	TEC	Тb	eha	vio	ır												

20.3.10 PIN_CNF[0]

Address offset: 0x700

Rit r	numb	er e		31	30	29	28 :	27 :	26.2	25 :	24	23 2	2 2	1 20) 10	18	17	' 16	15	14	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id				-	. 50						- '				, 10	, 10		E			10.			D	_		Ŭ	_	•	. C	В	-
	et Oxí	00000002		0	٥	0	0	n	0	0	n	0 (n 0	0	0	0	0	n	0	0	0	0 0		0	0	n	0	n	0 0		1	
Id		Field	Value Id	_	lue	Ŭ	Ť	•		•	Ť	Desc	rint	ion	ŭ	ŭ	ŭ	ŭ	Ŭ	Ŭ				Ŭ		Ť		•			-	
A		DIR	value lu	• •	iiuc							Pin c				ami	a ni	avci.	ر اد-	rogi	ctor	ac D	ID ra	orict	or							
Α.	11.00	DIK	Innut	0																_	stei	as D	11111	gisi	.Cı							
			Input	0								Conf	-																			
			Output	1								Conf	figur	e p	in a	s ar	า ดเ	ıtpu	t pi	n												
В	RW	INPUT										Conr	nect	or	disc	oni	nec	t inp	ut	buf	fer											
			Connect	0								Conr	nect	inp	ut l	buft	fer															
			Disconnect	1								Disc	onn	ect i	inpı	ut b	uff	er														
С	RW	PULL										Pull	conf	figu	rati	on																
			Disabled	0								No p	ull																			
			Pulldown	1								Pull	dow	n o	n pi	in																
			Pullup	3								Pull	up c	n p	in																	
D	RW	DRIVE										Drive	е со	nfig	ura	tio	า															
			S0S1	0								Stan	dar	'0' b	, st	and	ard	'1'														
			H0S1	1								High	driv	/e '()', s	tan	dar	d '1	'													
			S0H1	2								Stan	dar	'0' b	, hi	gh (driv	e '1														
			H0H1	3								High	driv	/e '()', h	nigh	'dr	ive	1''													
			DOS1	4								Disc	onn	ect	'0' s	tan	daı	d '1	' (n	orn	nally	use	d for	wii	ed-	or						
												conr	necti	ions	5)																	



Bit number		31 3	30 29	28	3 27	26	25	24	23 2	22 21	L 20	19	18	17	16	15 :	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Ε	Ε					D	D	D				C	. C	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	cript	ion																		
	D0H1	5							Disc	onne	ect '	0', h	nigh	dri	ve '	1' (r	norn	nally	use	d fo	r w	ired	-or	•					
									conr	necti	ons)																	
	SOD1	6							Stan	ndard	'0' t	. dis	con	nec	t '1	' (n	orm	ally ı	used	for	wii	red-	and	d					
									conr	necti	ons)																	
	H0D1	7							High	n driv	/e '0)', di	sco	nne	ct '	1' (r	norn	nally	use	d fo	r w	ired	-ar	nd					
									conr	necti	ons)																	
E RW SENSE									Pin s	sensi	ing r	mec	han	ism	1														
	Disabled	0							Disa	bled																			
	High	2							Sens	se fo	r hig	gh le	evel																
	Low	3							Sens	se fo	r lov	w le	vel																

20.3.11 PIN_CNF[1]

Address offset: 0x704

Configuration of GPIO pins

ld RW Field Value Id Value Description	
Reset 0x000000002 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical ph	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0
A RW DIR Pin direction. Same phys	
. ,	
Input 0 Configure nin as an input	sical register as DIR register
input 0 Configure pin as an input	t pin
Output 1 Configure pin as an outp	out pin
B RW INPUT Connect or disconnect in	nput buffer
Connect 0 Connect input buffer	
Disconnect 1 Disconnect input buffer	
C RW PULL Pull configuration	
Disabled 0 No pull	
Pulldown 1 Pull down on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	1
HOS1 1 High drive '0', standard '2	1'
SOH1 2 Standard '0', high drive '2	1'
H0H1 3 High drive '0', high 'drive	'1"
D0S1 4 Disconnect '0' standard '	1' (normally used for wired-or
connections)	
D0H1 5 Disconnect '0', high drive	e '1' (normally used for wired-or
connections)	
SOD1 6 Standard '0'. disconnect	'1' (normally used for wired-and
connections)	
H0D1 7 High drive '0', disconnect	t '1' (normally used for wired-and
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	
Low 3 Sense for low level	

20.3.12 PIN_CNF[2]

Address offset: 0x708



Reset 0x00000002 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	B A 1 0
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin Connect or disconnect input buffer Connect of disconnect input buffer Connect pinct buffer Disconnect input buffer Pull configuration Pull configuration No pull	1 0
A RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
Output 1 Configure pin as an output pin B RW INPUT Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
B RW INPUT Connect or disconnect input buffer Connect Disconnect Disconnect Disconnect input buffer Disconnect input buffer Disconnect input buffer Pull configuration No pull	
Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
C RW PULL Pull configuration Disabled 0 No pull	
Disabled 0 No pull	
·	
0.11.	
Pulldown 1 Pull down on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	
H0S1 1 High drive '0', standard '1'	
SOH1 2 Standard '0', high drive '1'	
H0H1 3 High drive '0', high 'drive '1"	
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or	
connections)	
D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or	
connections)	
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and	
connections)	
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and	
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	
Low 3 Sense for low level	

20.3.13 PIN_CNF[3]

Address offset: 0x70C Configuration of GPIO pins

В А 10
1 0



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E E DDD CCBA
Reset 0x00000002	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value Description
D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
	connections)
S0D1	6 Standard '0'. disconnect '1' (normally used for wired-and
	connections)
H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
	connections)
E RW SENSE	Pin sensing mechanism
Disabled	0 Disabled
High	2 Sense for high level
Low	3 Sense for low level

20.3.14 PIN_CNF[4]

Address offset: 0x710

Configuration of GPIO pins

Bit n	umbe	er		31 30	29 2	8 27	26 25	5 24 2	23 2	22 21 2	20	19 1	8 17	16	15	14 1	.3 12	2 11	10	9	3 7	6	5	4	3 2	2 1	. 0
Id													Е	Ε					D	D I)				C	В	Α
Rese	t 0x0	0000002		0 0	0 (0 0	0 0	0	0	0 0	0	0 (0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 () 1	0
Id	RW	Field	Value Id	Value					Des	criptio	n																
Α	RW	DIR						F	Pin d	directi	on	. San	ie pł	nysi	cal r	egis	ter a	s DI	R re	giste	r						
			Input	0				(Con	figure	pir	n as a	n in	put	pin												
			Output	1				(Con	figure	pir	n as a	n oı	ıtpu	ıt pi	n											
В	RW	INPUT						(Con	nect o	r d	liscor	nec	t inp	out l	ouffe	er										
			Connect	0				(Con	nect ir	ηpι	ut bu	fer														
			Disconnect	1				[Disc	onnec	t ir	nput	buff	er													
С	RW	PULL						F	Pull	config	ur	ation															
			Disabled	0				1	No p	oull																	
			Pulldown	1				F	Pull	down	on	pin															
			Pullup	3				F	Pull	up on	piı	n															
D	RW	DRIVE						[Driv	e conf	igu	uratio	n														
			S0S1	0				9	Stan	dard '	0',	stan	dard	'1'													
			H0S1	1				H	High	n drive	'0	', sta	ndar	d '1	1												
			S0H1	2				9	Stan	dard '	0',	high	driv	e '1	1												
			H0H1	3				H	High	n drive	'0	', hig	ı 'dr	ive	'1''												
			DOS1	4				[Disc	onnec	t '(O' sta	ndar	'd '1	.' (n	orma	ally u	ısed	for	wire	d-or						
								(conr	nectio	ns))															
			D0H1	5						onnec			gh dr	rive	'1' (norr	nally	use	d fo	r wi	red-	or					
			SOD1	6						dard '	,		nne	ct '	1' (n	orm	ally	usec	l for	wir	ed-a	nd					
								(conr	nectio	ns))															
			H0D1	7				ŀ	High	n drive	'0	', disc	onn	ect	'1' (norr	nally	use	d fo	r wi	red-	and					
								(conr	nectio	ns))															
E	RW	SENSE						F	Pin s	sensin	g n	nech	nisr	m													
			Disabled	0				[Disa	bled																	
			High	2				9	Sens	se for I	hig	h lev	el														
			Low	3				9	Sens	se for I	lov	v leve	el														

20.3.15 PIN_CNF[5]

Address offset: 0x714



Bit	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x000000	002	0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPU	т		Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIV	E		Drive configuration
		S0S1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENS	SE .		Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

20.3.16 PIN_CNF[6]

Address offset: 0x718
Configuration of GPIO pins

Bit	numb	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Res	et 0x0	00000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			SOS1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	E E DDD CCBA
Reset 0x00000002	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value Description
D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
	connections)
S0D1	6 Standard '0'. disconnect '1' (normally used for wired-and
	connections)
H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
	connections)
E RW SENSE	Pin sensing mechanism
Disabled	0 Disabled
High	2 Sense for high level
Low	3 Sense for low level

20.3.17 PIN_CNF[7]

Address offset: 0x71C

Configuration of GPIO pins

Bit n	umbe	er		31 30	29 2	8 27	26 25	5 24 2	23 2	22 21 2	20	19 1	8 17	16	15	14 1	.3 12	2 11	10	9	3 7	6	5	4	3 2	2 1	. 0
Id													Е	Ε					D	D I)				C	В	Α
Rese	t 0x0	0000002		0 0	0 (0 0	0 0	0	0	0 0	0	0 (0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 () 1	0
Id	RW	Field	Value Id	Value					Des	criptio	n																
Α	RW	DIR						F	Pin d	directi	on	. San	ie pł	nysi	cal r	egis	ter a	s DI	R re	giste	r						
			Input	0				(Con	figure	pir	n as a	n in	put	pin												
			Output	1				(Con	figure	pir	n as a	n oı	ıtpu	ıt pi	n											
В	RW	INPUT						(Con	nect o	r d	liscor	nec	t inp	out l	ouffe	er										
			Connect	0				(Con	nect ir	ηpι	ut bu	fer														
			Disconnect	1				[Disc	onnec	t ir	nput	buff	er													
С	RW	PULL						F	Pull	config	ur	ation															
			Disabled	0				1	No p	oull																	
			Pulldown	1				F	Pull	down	on	pin															
			Pullup	3				F	Pull	up on	piı	n															
D	RW	DRIVE						[Driv	e conf	igu	uratio	n														
			S0S1	0				9	Stan	dard '	0',	stan	dard	'1'													
			H0S1	1				H	High	n drive	'0	', sta	ndar	d '1	1												
			S0H1	2				9	Stan	dard '	0',	high	driv	e '1	1												
			H0H1	3				H	High	n drive	'0	', hig	ı 'dr	ive	'1''												
			DOS1	4				[Disc	onnec	t '(O' sta	ndar	'd '1	.' (n	orma	ally u	ısed	for	wire	d-or						
								(conr	nectio	ns))															
			D0H1	5						onnec			gh dr	rive	'1' (norr	nally	use	d fo	r wi	red-	or					
			SOD1	6						dard '	,		nne	ct '	1' (n	orm	ally	usec	l for	wir	ed-a	nd					
								(conr	nectio	ns))															
			H0D1	7				ŀ	High	n drive	'0	', disc	onn	ect	'1' (norr	nally	use	d fo	r wi	red-	and					
								(conr	nectio	ns))															
E	RW	SENSE						F	Pin s	sensin	g n	nech	nisr	m													
			Disabled	0				[Disa	bled																	
			High	2				9	Sens	se for I	hig	h lev	el														
			Low	3				9	Sens	se for I	lov	v leve	el														

20.3.18 PIN_CNF[8]

Address offset: 0x720



Reset 0x00000002 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	B A 1 0
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin Connect or disconnect input buffer Connect of disconnect input buffer Connect pinct buffer Disconnect input buffer Pull configuration Pull configuration No pull	1 0
A RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect 0 Connect input buffer Connect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
Output 1 Configure pin as an output pin B RW INPUT Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
B RW INPUT Connect or disconnect input buffer Connect Disconnect Disconnect Disconnect input buffer Disconnect input buffer Disconnect input buffer Pull configuration No pull	
Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
C RW PULL Pull configuration Disabled 0 No pull	
Disabled 0 No pull	
·	
0.11.	
Pulldown 1 Pull down on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	
H0S1 1 High drive '0', standard '1'	
SOH1 2 Standard '0', high drive '1'	
H0H1 3 High drive '0', high 'drive '1"	
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or	
connections)	
D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or	
connections)	
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and	
connections)	
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and	
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	
Low 3 Sense for low level	

20.3.19 PIN_CNF[9]

Address offset: 0x724

С В А
1 0



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.20 PIN_CNF[10]

Address offset: 0x728

Configuration of GPIO pins

	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d .	E E DDD CCBA
leset 0x00000002	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
d RW Field Value Id	Value Description
RW DIR	Pin direction. Same physical register as DIR register
Input	0 Configure pin as an input pin
Output	1 Configure pin as an output pin
RW INPUT	Connect or disconnect input buffer
Connect	0 Connect input buffer
Disconnect	1 Disconnect input buffer
RW PULL	Pull configuration
Disabled	0 No pull
Pulldown	1 Pull down on pin
Pullup	3 Pull up on pin
RW DRIVE	Drive configuration
S0S1	0 Standard '0', standard '1'
H0S1	1 High drive '0', standard '1'
S0H1	2 Standard '0', high drive '1'
H0H1	3 High drive '0', high 'drive '1"
DOS1	4 Disconnect '0' standard '1' (normally used for wired-or
	connections)
D0H1	5 Disconnect '0', high drive '1' (normally used for wired-or
	connections)
SOD1	6 Standard '0'. disconnect '1' (normally used for wired-and
	connections)
H0D1	7 High drive '0', disconnect '1' (normally used for wired-and
	connections)
	Pin sensing mechanism
RW SENSE	0 0: 11.1
Disabled	0 Disabled
	2 Sense for high level 3 Sense for low level

20.3.21 PIN_CNF[11]

Address offset: 0x72C



Reset 0x00000002 Id RW Field	B A 0 1 0
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin Connect or disconnect input buffer Connect or disconnect input buffer Connect Disconnect 0 Connect input buffer Disconnect 1 Disconnect input buffer Pull configuration Pull configuration No pull	1 0
A RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer RW PULL RW PULL Disabled O No pull	
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer C RW PULL Pull configuration Disabled 0 No pull	
Output 1 Configure pin as an output pin B RW INPUT Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
B RW INPUT Connect or disconnect input buffer Connect of Disconnect input buffer Disconnect input buffer Disconnect input buffer Disconnect input buffer Pull configuration No pull	
Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
Disconnect 1 Disconnect input buffer C RW PULL Pull configuration Disabled 0 No pull	
C RW PULL Pull configuration Disabled 0 No pull	
Disabled 0 No pull	
·	
Pulldown 1 Pull down on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	
H0S1 1 High drive '0', standard '1'	
SOH1 2 Standard '0', high drive '1'	
H0H1 3 High drive '0', high 'drive '1"	
D0S1 4 Disconnect '0' standard '1' (normally used for wired-or	
connections)	
D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or	
connections)	
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and	
connections)	
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and	
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	
Low 3 Sense for low level	

20.3.22 PIN_CNF[12]

Address offset: 0x730 Configuration of GPIO pins

С В А
1 0



Bit number		31 3	30 29	28	3 27	26	25	24	23 2	22 21	L 20	19	18	17	16	15 :	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Ε	Ε					D	D	D				C	. C	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	cript	ion																		
	D0H1	5							Disc	onne	ect '	0', h	nigh	dri	ve '	1' (r	norn	nally	use	d fo	r w	ired	-or	•					
									conr	necti	ons)																	
	SOD1	6							Stan	ndard	'0' t	. dis	con	nec	t '1	' (n	orm	ally ı	used	l for	wii	red-	and	d					
									conr	necti	ons)																	
	H0D1	7							High	n driv	/e '0)', di	sco	nne	ct '	1' (r	norn	nally	use	d fo	r w	ired	-ar	nd					
									conr	necti	ons)																	
E RW SENSE									Pin s	sensi	ing r	mec	han	ism	1														
	Disabled	0							Disa	bled																			
	High	2							Sens	se fo	r hig	gh le	evel																
	Low	3							Sens	se fo	r lov	w le	vel																

20.3.23 PIN_CNF[13]

Address offset: 0x734

Configuration of GPIO pins

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.24 PIN_CNF[14]

Address offset: 0x738



Reset 0x00000002 Id RW Field	B A 0 1 0
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin Connect or disconnect input buffer Connect or disconnect input buffer Connect Disconnect 0 Connect input buffer Disconnect 1 Disconnect input buffer Pull configuration Pull configuration No pull	1 0
A RW DIR Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer RW PULL RW PULL Disabled O No pull	
Input 0 Configure pin as an input pin Output 1 Configure pin as an output pin B RW INPUT Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer C RW PULL Pull configuration Disabled 0 No pull	
Output 1 Configure pin as an output pin B RW INPUT Connect or disconnect input buffer Connect Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
B RW INPUT Connect or disconnect input buffer Connect of Disconnect input buffer Disconnect input buffer Disconnect input buffer Disconnect input buffer Pull configuration No pull	
Connect 0 Connect input buffer Disconnect 1 Disconnect input buffer C RW PULL Disabled 0 No pull	
Disconnect 1 Disconnect input buffer C RW PULL Pull configuration Disabled 0 No pull	
C RW PULL Pull configuration Disabled 0 No pull	
Disabled 0 No pull	
·	
Pulldown 1 Pull down on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	
H0S1 1 High drive '0', standard '1'	
SOH1 2 Standard '0', high drive '1'	
H0H1 3 High drive '0', high 'drive '1"	
D0S1 4 Disconnect '0' standard '1' (normally used for wired-or	
connections)	
D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or	
connections)	
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and	
connections)	
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and	
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	
Low 3 Sense for low level	

20.3.25 PIN_CNF[15]

Address offset: 0x73C Configuration of GPIO pins

Bit r	numb	er		31	30	29 :	28 2	27 2	26 2	5 2	4 23	22	2 21	20	19	18	17	16	15	14	13	12 1	1 1	9	8	7	6	5	4 3	2	1	0
Id																	Ε	Ε					0	D	D				C	С	В	Α
Rese	et OxC	00000002		0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	1	0
Id	RW	Field	Value Id	Va	lue						De	escr	ripti	on																		
Α	RW	DIR									Pir	n di	irect	tion	ı. Sa	me	ph	ysi	al r	egis	ter	as I	DIR i	egis	ter							
			Input	0							Co	nfi	gure	e pi	n as	an	inp	out	pin													
			Output	1							Co	nfi	gure	e pi	n as	an	ou	tpu	t pi	า												
В	RW	INPUT									Co	nn	ect	or c	disco	onn	ect	inp	ut l	ouff	er											
			Connect	0							Co	nn	ect i	inpı	ut b	uff	er															
			Disconnect	1							Di	sco	nne	ct i	npu	t b	uffe	er														
С	RW	PULL									Pu	ıll c	onfi	gur	atic	n																
			Disabled	0							No	рι	ıll																			
			Pulldown	1							Pu	ıll d	lowi	n or	n pii	n																
			Pullup	3							Pu	ıll u	ір оі	n pi	n																	
D	RW	DRIVE									Dr	ive	cor	nfigu	urat	ion	ı															
			S0S1	0							Sta	and	lard	'0',	, sta	nda	ard	'1'														
			H0S1	1							Hi	gh	driv	e '0	', st	and	dar	d '1														
			S0H1	2							Sta	and	lard	'0',	, hig	h d	lrive	e '1														
			H0H1	3							Hi	gh	driv	e '0)', hi	igh	'dri	ve '	1''													
			DOS1	4							Di	sco	nne	ct '	0' st	tan	dar	d '1	' (n	orm	ally	use	d fo	r wi	red-	or						
											со	nne	ectio	ons)																	



Bit number		31 3	30 29	28	3 27	26	25	24	23 2	22 21	L 20	19	18	17	16	15 :	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Ε	Ε					D	D	D				C	. C	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	cript	ion																		
	D0H1	5							Disc	onne	ect '	0', h	nigh	dri	ve '	1' (r	norn	nally	use	d fo	r w	ired	-or	•					
									conr	necti	ons)																	
	SOD1	6							Stan	ndard	'0' t	. dis	con	nec	t '1	' (n	orm	ally ı	used	l for	wii	red-	and	d					
									conr	necti	ons)																	
	H0D1	7							High	n driv	/e '0)', di	sco	nne	ct '	1' (r	norn	nally	use	d fo	r w	ired	-ar	nd					
									conr	necti	ons)																	
E RW SENSE									Pin s	sensi	ing r	mec	han	ism	1														
	Disabled	0							Disa	bled																			
	High	2							Sens	se fo	r hig	gh le	evel																
	Low	3							Sens	se fo	r lov	w le	vel																

20.3.26 PIN_CNF[16]

Address offset: 0x740

Configuration of GPIO pins

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.27 PIN_CNF[17]

Address offset: 0x744



Bit	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x000000	002	0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPU	т		Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIV	E		Drive configuration
		S0S1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENS	SE .		Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

20.3.28 PIN_CNF[18]

Address offset: 0x748
Configuration of GPIO pins

Bit r	numb	er		31	. 30	29	28 :	27 :	26 2	5 2	24 23	3 22	2 21	20	19	18	17	16	15	14	13 :	12 1	1 1	0 9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					0	D	D					C C	В	Α
Res	et Ox(00000002		0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	1	0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
Α	RW	DIR									Pi	in d	irec	tion	ı. Sa	me	ph	ysic	al r	egi	ter	as [)IR ı	egis	ter							
			Input	0							C	onfi	igur	e pii	n as	an	inp	ut	pin													
			Output	1							C	onfi	igur	e pii	n as	an	ou	tpu	t pi	n												
В	RW	INPUT									C	onn	ect	or d	disco	nn	ect	inp	ut l	ouff	er											
			Connect	0							C	onn	ect	inpı	ut b	uffe	er															
			Disconnect	1							D	isco	nne	ct i	npu	t bı	uffe	r														
С	RW	PULL									Pı	ull c	confi	gur	atio	n																
			Disabled	0							N	о р	ull																			
			Pulldown	1							Pi	ull c	dow	n or	n pir	1																
			Pullup	3							Pi	ull t	ıp o	n pi	n																	
D	RW	DRIVE									D	rive	cor	nfigu	urat	ion																
			S0S1	0							St	and	dard	'0',	, sta	nda	ard	'1'														
			H0S1	1							Н	igh	driv	e '0	', st	and	lard	d '1'														
			S0H1	2							St	tand	dard	'0',	, hig	h d	rive	e '1'														
			H0H1	3							Н	igh	driv	e '0	', hi	gh	'dri	ve '	1''													
			DOS1	4							D	isco	nne	ct '	0' st	and	dar	d '1	no	orm	ally	use	d fo	r wi	ired	-or						
											cc	onn	ecti	ons))																	



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.29 PIN_CNF[19]

Address offset: 0x74C

Configuration of GPIO pins

Bit n	umbe	er		31 30	29 2	8 27	26 25	5 24 2	23 2	22 21 2	20	19 1	8 17	16	15	14 1	.3 12	2 11	10	9	3 7	6	5	4	3 2	2 1	. 0
Id													Е	Ε					D	D I)				C	В	Α
Rese	t 0x0	0000002		0 0	0 (0 0	0 0	0	0	0 0	0	0 (0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 () 1	0
Id	RW	Field	Value Id	Value					Des	criptio	n																
Α	RW	DIR						F	Pin d	directi	on	. San	ie pł	nysi	cal r	egis	ter a	s DI	R re	giste	r						
			Input	0				(Con	figure	pir	n as a	n in	put	pin												
			Output	1				(Con	figure	pir	n as a	n oı	ıtpu	ıt pi	n											
В	RW	INPUT						(Con	nect o	r d	liscor	nec	t inp	out l	ouffe	er										
			Connect	0				(Con	nect ir	ηpι	ut bu	fer														
			Disconnect	1				[Disc	onnec	t ir	nput	buff	er													
С	RW	PULL						F	Pull	config	ur	ation															
			Disabled	0				1	No p	oull																	
			Pulldown	1				F	Pull	down	on	pin															
			Pullup	3				F	Pull	up on	piı	n															
D	RW	DRIVE						[Driv	e conf	igu	uratio	n														
			S0S1	0				9	Stan	dard '	0',	stan	dard	'1'													
			H0S1	1				H	High	n drive	'0	', sta	ndar	d '1	1												
			S0H1	2				9	Stan	dard '	0',	high	driv	e '1	1												
			H0H1	3				H	High	n drive	'0	', hig	ı 'dr	ive	'1''												
			DOS1	4				[Disc	onnec	t '(O' sta	ndar	'd '1	.' (n	orma	ally u	ısed	for	wire	d-or						
								(conr	nectio	ns))															
			D0H1	5						onnec			gh dr	rive	'1' (norr	nally	use	d fo	r wi	red-	or					
			SOD1	6						dard '	,		nne	ct '	1' (n	orm	ally	usec	l for	wir	ed-a	nd					
								(conr	nectio	ns))															
			H0D1	7				ŀ	High	n drive	'0	', disc	onn	ect	'1' (norr	nally	use	d fo	r wi	red-	and					
								(conr	nectio	ns))															
E	RW	SENSE						F	Pin s	sensin	g n	nech	nisr	m													
			Disabled	0				[Disa	bled																	
			High	2				9	Sens	se for I	hig	h lev	el														
			Low	3				9	Sens	se for I	lov	v leve	el														

20.3.30 PIN_CNF[20]

Address offset: 0x750 Configuration of GPIO pins



Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Е	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.31 PIN_CNF[21]

Address offset: 0x754 Configuration of GPIO pins

B A 1 0
1 0



Bit number		31 3	30 29	28	3 27	26	25	24	23 2	22 21	L 20	19	18	17	16	15 :	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Ε	Ε					D	D	D				C	. C	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	cript	ion																		
	D0H1	5							Disc	onne	ect '	0', h	nigh	dri	ve '	1' (r	norn	nally	use	d fo	r w	ired	-or	•					
									conr	necti	ons)																	
	SOD1	6							Stan	ndard	'0' t	. dis	con	nec	t '1	' (n	orm	ally ı	used	for	wii	red-	and	d					
									conr	necti	ons)																	
	H0D1	7							High	n driv	/e '0)', di	sco	nne	ct '	1' (r	norn	nally	use	d fo	r w	ired	-ar	nd					
									conr	necti	ons)																	
E RW SENSE									Pin s	sensi	ing r	mec	han	ism	1														
	Disabled	0							Disa	bled																			
	High	2							Sens	se fo	r hig	gh le	evel																
	Low	3							Sens	se fo	r lov	w le	vel																

20.3.32 PIN_CNF[22]

Address offset: 0x758

Configuration of GPIO pins

ld RW Field Value Id Value Description	
Reset 0x000000002 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical ph	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0
A RW DIR Pin direction. Same phys	
. ,	
Input 0 Configure nin as an input	sical register as DIR register
input 0 Configure pin as an input	t pin
Output 1 Configure pin as an outp	out pin
B RW INPUT Connect or disconnect in	nput buffer
Connect 0 Connect input buffer	
Disconnect 1 Disconnect input buffer	
C RW PULL Pull configuration	
Disabled 0 No pull	
Pulldown 1 Pull down on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	1
HOS1 1 High drive '0', standard '2	1'
SOH1 2 Standard '0', high drive '2	1'
H0H1 3 High drive '0', high 'drive	'1"
D0S1 4 Disconnect '0' standard '	1' (normally used for wired-or
connections)	
D0H1 5 Disconnect '0', high drive	e '1' (normally used for wired-or
connections)	
SOD1 6 Standard '0'. disconnect	'1' (normally used for wired-and
connections)	
H0D1 7 High drive '0', disconnect	t '1' (normally used for wired-and
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	
Low 3 Sense for low level	

20.3.33 PIN_CNF[23]

Address offset: 0x75C

Configuration of GPIO pins



Bit r	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Res	et 0x0	0000002		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Е	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.34 PIN_CNF[24]

Address offset: 0x760 Configuration of GPIO pins

Bit r	numb	er		31	. 30	29	28 :	27 :	26 2	5 2	24 23	3 22	2 21	20	19	18	17	16	15	14	13 :	12 1	1 1	0 9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					0	D	D					C C	В	Α
Res	et Ox(00000002		0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	1	0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
Α	RW	DIR									Pi	in d	irec	tion	ı. Sa	me	ph	ysic	al r	egi	ter	as [)IR ı	egis	ter							
			Input	0							C	onfi	igur	e pii	n as	an	inp	ut	pin													
			Output	1							C	onfi	igur	e pii	n as	an	ou	tpu	t pi	n												
В	RW	INPUT									C	onn	ect	or d	disco	nn	ect	inp	ut l	ouff	er											
			Connect	0							C	onn	ect	inpı	ut b	uffe	er															
			Disconnect	1							D	isco	nne	ct i	npu	t bı	uffe	r														
С	RW	PULL									Pı	ull c	confi	gur	atio	n																
			Disabled	0							N	о р	ull																			
			Pulldown	1							Pi	ull c	dow	n or	n pir	1																
			Pullup	3							Pi	ull t	ир о	n pi	n																	
D	RW	DRIVE									D	rive	cor	nfigu	urat	ion																
			S0S1	0							St	and	dard	'0',	, sta	nda	ard	'1'														
			H0S1	1							Н	igh	driv	e '0	', st	and	lard	d '1'														
			S0H1	2							St	tand	dard	'0',	, hig	h d	rive	e '1'														
			H0H1	3							Н	igh	driv	e '0	', hi	gh	'dri	ve '	1''													
			DOS1	4							D	isco	nne	ct '	0' st	and	dar	d '1	no	orm	ally	use	d fo	r wi	ired	-or						
											cc	onn	ecti	ons))																	



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.35 PIN_CNF[25]

Address offset: 0x764

Configuration of GPIO pins

Bit n	umbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Rese	t 0x0	0000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
					connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
					connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
					connections)
Ε	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level

20.3.36 PIN_CNF[26]

Address offset: 0x768

Configuration of GPIO pins



Reset 0x000000002 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	C C B A 0 0 0 0 1 0
Id RW Field Value Id Value Description A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin	0 0 0 0 1 0
A RW DIR Pin direction. Same physical register as DIR register Input 0 Configure pin as an input pin	
Input 0 Configure pin as an input pin	
Output 1 Configure pin as an output pin	
Surper 1 Compare pin as an output pin	
B RW INPUT Connect or disconnect input buffer	
Connect 0 Connect input buffer	
Disconnect 1 Disconnect input buffer	
C RW PULL Pull configuration	
Disabled 0 No pull	
Pulldown 1 Pull down on pin	
Pullup 3 Pull up on pin	
D RW DRIVE Drive configuration	
SOS1 0 Standard '0', standard '1'	
H0S1 1 High drive '0', standard '1'	
SOH1 2 Standard '0', high drive '1'	
H0H1 3 High drive '0', high 'drive '1"	
DOS1 4 Disconnect '0' standard '1' (normally used for wired-or	
connections)	
D0H1 5 Disconnect '0', high drive '1' (normally used for wired-or	
connections)	
SOD1 6 Standard '0'. disconnect '1' (normally used for wired-and	
connections)	
H0D1 7 High drive '0', disconnect '1' (normally used for wired-and	
connections)	
E RW SENSE Pin sensing mechanism	
Disabled 0 Disabled	
High 2 Sense for high level	
Low 3 Sense for low level	

20.3.37 PIN_CNF[27]

Address offset: 0x76C Configuration of GPIO pins

Bit r	numb	er		31	. 30	29	28	27 :	26 2	5 2	24 23	3 22	2 21	20	19	18	17	16	15	14	13 :	12 1	1 1	0 9	8	7	6	5	4	3 2	1	0
Id																	Ε	Ε					0	D	D					C C	В	Α
Res	et Ox(00000002		0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	1	0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																		
Α	RW	DIR									Pi	in d	irec	tion	ı. Sa	me	ph	ysic	al r	egi	ter	as [)IR ı	egis	ter							
			Input	0							C	onfi	igur	e pii	n as	an	inp	ut	pin													
			Output	1							C	onfi	igur	e pii	n as	an	ou	tpu	t pi	n												
В	RW	INPUT									C	onn	ect	or d	disco	nn	ect	inp	ut l	ouff	er											
			Connect	0							C	onn	ect	inpı	ut b	uffe	er															
			Disconnect	1							D	isco	nne	ct i	npu	t bı	uffe	r														
С	RW	PULL									Pı	ull c	confi	gur	atio	n																
			Disabled	0							N	о р	ull																			
			Pulldown	1							Pi	ull c	dow	n or	n pir	1																
			Pullup	3							Pi	ull t	ир о	n pi	n																	
D	RW	DRIVE									D	rive	cor	nfigu	urat	ion																
			S0S1	0							St	and	dard	'0',	, sta	nda	ard	'1'														
			H0S1	1							Н	igh	driv	e '0	', st	and	lard	d '1'														
			S0H1	2							St	tand	dard	'0',	, hig	h d	rive	e '1'														
			H0H1	3							Н	igh	driv	e '0	', hi	gh	'dri	ve '	1''													
			DOS1	4							D	isco	nne	ct '	0' st	and	dar	d '1	no	orm	ally	use	d fo	r wi	ired	-or						
											cc	onn	ecti	ons))																	



Bit number	31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E E DDD CCBA
Reset 0x00000002	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
		connections)
SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and
		connections)
H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
		connections)
E RW SENSE		Pin sensing mechanism
Disabled	0	Disabled
High	2	Sense for high level
Low	3	Sense for low level

20.3.38 PIN_CNF[28]

Address offset: 0x770

Configuration of GPIO pins

Bit n	umbe	er		31 30	29 2	8 27	26 25	5 24 2	23 2	22 21 2	20	19 1	8 17	16	15	14 1	.3 12	2 11	10	9	3 7	6	5	4	3 2	2 1	. 0
Id													Е	Ε					D	D I)				C	В	Α
Rese	t 0x0	0000002		0 0	0 (0 0	0 0	0	0	0 0	0	0 (0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 () 1	0
Id	RW	Field	Value Id	Value					Des	criptio	n																
Α	RW	DIR						F	Pin d	directi	on	. San	ie pł	nysi	cal r	egis	ter a	s DI	R re	giste	r						
			Input	0				(Con	figure	pir	n as a	n in	put	pin												
			Output	1				(Con	figure	pir	n as a	n oı	ıtpu	ıt pi	n											
В	RW	INPUT						(Con	nect o	r d	liscor	nec	t inp	out l	ouffe	er										
			Connect	0				(Con	nect ir	ηpι	ut bu	fer														
			Disconnect	1				[Disc	onnec	t ir	nput	buff	er													
С	RW	PULL						F	Pull	config	ur	ation															
			Disabled	0				1	No p	oull																	
			Pulldown	1				F	Pull	down	on	pin															
			Pullup	3				F	Pull	up on	piı	n															
D	RW	DRIVE						[Driv	e conf	igu	uratio	n														
			S0S1	0				9	Stan	dard '	0',	stan	dard	'1'													
			H0S1	1				H	High	n drive	'0	', sta	ndar	d '1	1												
			S0H1	2				9	Stan	dard '	0',	high	driv	e '1	1												
			H0H1	3				H	High	n drive	'0	', hig	ı 'dr	ive	'1''												
			DOS1	4				[Disc	onnec	t '(O' sta	ndar	'd '1	.' (n	orma	ally u	ısed	for	wire	d-or						
								(conr	nectio	ns))															
			D0H1	5						onnec			gh dr	rive	'1' (norr	nally	use	d fo	r wi	red-	or					
			SOD1	6						dard '	,		nne	ct '	1' (n	orm	ally	usec	l for	wir	ed-a	nd					
								(conr	nectio	ns))															
			H0D1	7				ŀ	High	n drive	'0	', disc	onn	ect	'1' (norr	nally	use	d fo	r wi	red-	and					
								(conr	nectio	ns))															
E	RW	SENSE						F	Pin s	sensin	g n	nech	nisr	m													
			Disabled	0				[Disa	bled																	
			High	2				9	Sens	se for I	hig	h lev	el														
			Low	3				9	Sens	se for I	lov	v leve	el														

20.3.39 PIN_CNF[29]

Address offset: 0x774

Configuration of GPIO pins



Bit	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E E DDD CCBA
Res	et 0x000000	002	0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW DIR			Pin direction. Same physical register as DIR register
		Input	0	Configure pin as an input pin
		Output	1	Configure pin as an output pin
В	RW INPU	т		Connect or disconnect input buffer
		Connect	0	Connect input buffer
		Disconnect	1	Disconnect input buffer
С	RW PULL			Pull configuration
		Disabled	0	No pull
		Pulldown	1	Pull down on pin
		Pullup	3	Pull up on pin
D	RW DRIV	E		Drive configuration
		S0S1	0	Standard '0', standard '1'
		H0S1	1	High drive '0', standard '1'
		S0H1	2	Standard '0', high drive '1'
		H0H1	3	High drive '0', high 'drive '1"
		D0S1	4	Disconnect '0' standard '1' (normally used for wired-or
				connections)
		D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or
				connections)
		S0D1	6	Standard '0'. disconnect '1' (normally used for wired-and
				connections)
		H0D1	7	High drive '0', disconnect '1' (normally used for wired-and
				connections)
Ε	RW SENS	SE .		Pin sensing mechanism
		Disabled	0	Disabled
		High	2	Sense for high level
		Low	3	Sense for low level

20.3.40 PIN_CNF[30]

Address offset: 0x778 Configuration of GPIO pins

В А 10
1 0



Bit number		31 3	30 29	28	3 27	26	25	24	23 2	22 21	L 20	19	18	17	16	15 :	14 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id														Ε	Ε					D	D	D				C	. C	В	Α
Reset 0x00000002		0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	1	0
ld RW Field	Value Id	Valu	ıe						Desc	cript	ion																		
	D0H1	5							Disc	onne	ect '	0', h	nigh	dri	ve '	1' (r	norn	nally	use	d fo	r w	ired	-or	•					
									conr	necti	ons)																	
	SOD1	6							Stan	ndard	'0' t	. dis	con	nec	t '1	' (n	orm	ally ı	used	for	wii	red-	and	d					
									conr	necti	ons)																	
	H0D1	7							High	n driv	/e '0)', di	sco	nne	ct '	1' (r	norn	nally	use	d fo	r w	ired	-ar	nd					
									conr	necti	ons)																	
E RW SENSE									Pin s	sensi	ing r	mec	han	ism	1														
	Disabled	0							Disa	bled																			
	High	2							Sens	se fo	r hig	gh le	evel																
	Low	3							Sens	se fo	r lov	w le	vel																

20.3.41 PIN_CNF[31]

Address offset: 0x77C

Configuration of GPIO pins

	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					E E DDD CCBA
Res		0000002			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
Α	RW	DIR			Pin direction. Same physical register as DIR register
			Input	0	Configure pin as an input pin
			Output	1	Configure pin as an output pin
В	RW	INPUT			Connect or disconnect input buffer
			Connect	0	Connect input buffer
			Disconnect	1	Disconnect input buffer
С	RW	PULL			Pull configuration
			Disabled	0	No pull
			Pulldown	1	Pull down on pin
			Pullup	3	Pull up on pin
D	RW	DRIVE			Drive configuration
			S0S1	0	Standard '0', standard '1'
			H0S1	1	High drive '0', standard '1'
			S0H1	2	Standard '0', high drive '1'
			H0H1	3	High drive '0', high 'drive '1"
			DOS1	4	Disconnect '0' standard '1' (normally used for wired-or
					connections)
			D0H1	5	Disconnect '0', high drive '1' (normally used for wired-or connections)
			SOD1	6	Standard '0'. disconnect '1' (normally used for wired-and connections)
			H0D1	7	High drive '0', disconnect '1' (normally used for wired-and connections)
E	RW	SENSE			Pin sensing mechanism
			Disabled	0	Disabled
			High	2	Sense for high level
			Low	3	Sense for low level
			20	<u> </u>	50.50.10.10.10.10.10.10.10.10.10.10.10.10.10

20.4 Electrical specification

20.4.1 GPIO Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
V _{IH}	Input high voltage	0.7 x VD	D	VDD	V



Symbol	Description	Min.	Тур.	Max.	Units
V _{IL}	Input low voltage	VSS		0.3 x VDI	O V
V _{OH,SD}	Output high voltage, standard drive, 0.5 mA, VDD ≥1.7	VDD-0.4		VDD	V
V _{OH,HDH}	Output high voltage, high drive, 5 mA, VDD >= 2.7 V	VDD-0.4		VDD	V
V _{OH,HDL}	Output high voltage, high drive, 3 mA, VDD >= 1.7 V	VDD-0.4		VDD	V
V _{OL,SD}	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS		VSS+0.4	V
V _{OL,HDH}	Output low voltage, high drive, 5 mA, VDD >= 2.7 V	VSS		VSS+0.4	V
V _{OL,HDL}	Output low voltage, high drive, 3 mA, VDD >= 1.7 V	VSS		VSS+0.4	V
I _{OL,SD}	Current at VSS+0.4 V, output set low, standard drive, VDD ≥1.7	1	2	4	mA
I _{OL,HDH}	Current at VSS+0.4 V, output set low, high drive, VDD >= 2.7 V	6	10	15	mA
I _{OL,HDL}	Current at VSS+0.4 V, output set low, high drive, VDD >= 1.7 V	3			mA
I _{OH,SD}	Current at VDD-0.4 V, output set high, standard drive, VDD ≥1.7	1	2	4	mA
I _{OH,HDH}	Current at VDD-0.4 V, output set high, high drive, VDD >= 2.7 V	6	9	14	mA
I _{OH,HDL}	Current at VDD-0.4 V, output set high, high drive, VDD >= 1.7 V	3			mA
t _{RF,15pF}	Rise/fall time, low drive mode, 10-90%, 15 pF load ¹		9		ns
t _{RF,25pF}	Rise/fall time, low drive mode, 10-90%, 25 pF load ¹		13		ns
t _{RF,50pF}	Rise/fall time, low drive mode, 10-90%, 50 pF load ¹		25		ns
t _{HRF,15pF}	Rise/Fall time, high drive mode, 10-90%, 15 pF load ¹		4		ns
t _{HRF,25pF}	Rise/Fall time, high drive mode, 10-90%, 25 pF load ¹		5		ns
t _{HRF,50pF}	Rise/Fall time, high drive mode, 10-90%, 50 pF load ¹		8		ns
R _{PU}	Pull-up resistance	11	13	16	kΩ
R _{PD}	Pull-down resistance	11	13	16	kΩ
C _{PAD}	Pad capacitance		3		pF
C _{PAD_NFC}	Pad capacitance on NFC pads		4		pF
I _{NFC_LEAK}	Leakage current between NFC pads when driven to different		2	10	μΑ
	ctates				

The current drawn from the battery when GPIO is active as an output is calculated as follows:

 I_{GPIO} = V_{DD} C_{load} f

 C_{load} being the load capacitance and "f" is the switching frequency.

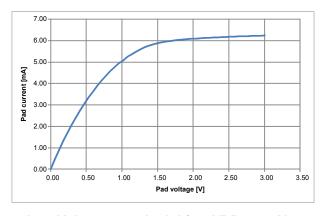


Figure 23: GPIO drive strength vs Voltage, standard drive, VDD = 3.0 V

¹ Rise and fall times based on simulations



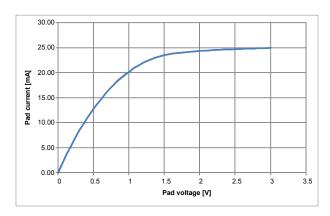


Figure 24: GPIO drive strength vs Voltage, high drive, VDD = 3.0 V

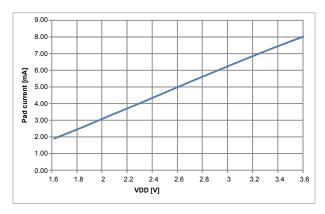


Figure 25: Max sink current vs Voltage, standard drive

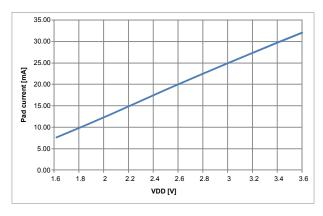


Figure 26: Max sink current vs Voltage, high drive

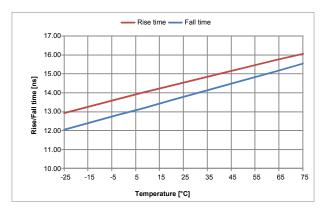


Figure 27: Rise and fall time vs Temperature, 10%-90%, 25pF load capacitance, VDD = 3.0 V



21 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Low power detection of pin state changes is possible when in System ON or System OFF.

Table 31: GPIOTE properties

Instance	Number of GPIOTE channels
GPIOTE	8

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one (OUT) is configurable to perform following operations:

- Set
- Clear
- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- Rising edge
- Falling edge
- · Any change

21.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The tasks (SET[n], CLR[n] and OUT[n]) can be used for writing to individual pins, and the events (IN[n]) can be generated from changes occurring at the inputs of individual pins.

The SET task will set the pin selected in CONFIG[n].PSEL to high.

The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in CONFIG[n].POLARITY, and can either set the pin high, set it low, or toggle it.

The tasks and events are configured using the CONFIG[n] registers. Every set of SET, CLR and OUT[n] tasks and IN[n] events has one CONFIG[n] register associated with it.

As long as a SET[n], CLR[n] and OUT[n] task or an IN[n] event is configured to control a pin **n**, the pin's output value will only be updated by the GPIOTE module. The pin's output value as specified in the GPIO will therefore be ignored as long as the pin is controlled by GPIOTE. Attempting to write a pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, see MODE field in CONFIG[n] register, the associated pin will get the output and configuration values specified in the GPIO module.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, the precedence of the tasks will be as described in *Table 32: Task priorities* on page 157.

Table 32: Task priorities

Priority	Task
1	OUT
2	CLR
3	SET



When setting the CONFIG[n] registers, MODE=Disabled does not have the same effect as MODE=Task and POLARITY=None. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, according to the priorities described in the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the OUTINIT field of CONFIG[n].

21.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See *GPIO* — *General purpose input/output* on page 111 for more information about the DETECT signal.

Putting the system into System ON IDLE while DETECT is high will not cause DETECT to wake the system up again. Make sure to clear all DETECT sources before entering sleep. If the LATCH register is used as a source, if any bit in LATCH is still high after clearing all or part of the register (for instance due to one of the PINx.DETECT signal still high), a new rising edge will be generated on DETECT, see *Pin configuration* on page 111.

Trying to put the system to System OFF while DETECT is high will cause a wakeup from System OFF reset.

This feature is always enabled although the peripheral itself appears to be IDLE, that is, no clocks or other power intensive infrastructure have to be requested to keep this feature enabled. This feature can therefore be used to wake up the CPU from a WFI or WFE type sleep in System ON with all peripherals and the CPU idle, that is, lowest power consumption in System ON mode.

In order to prevent spurious interrupts from the PORT event while configuring the sources, the user shall first disable interrupts on the PORT event (through INTENCLR.PORT), then configure the sources (PIN_CNF[n].SENSE), clear any potential event that could have occurred during configuration (write '1' to EVENTS_PORT), and finally enable interrupts (through INTENSET.PORT).

21.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO.

Only one GPIOTE channel can be assigned to one physical pin. Failing to do so may result in unpredictable behavior.

21.4 Registers

Table 33: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40006000	GPIOTE	GPIOTE	GPIO Tasks and Events	

Table 34: Register Overview

Register	Offset	Description
TASKS_OUT[0]	0x000	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is configured in
		CONFIG[0].POLARITY.
TASKS_OUT[1]	0x004	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is configured in
		CONFIG[1].POLARITY.



TASKS_OUT[4] 0x010 Task for writing to pin specified in CONFIG[4].PSEL Action on pin is configured in CONFIG[4].POLARITY. TASKS_OUT[5] 0x014 Task for writing to pin specified in CONFIG[5].PSEL Action on pin is configured in CONFIG[5].POLARITY. TASKS_OUT[6] 0x018 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[6].POLARITY. TASKS_OUT[7] 0x01C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].POLARITY. TASKS_SET[0] 0x030 Task for writing to pin specified in CONFIG[0].PSEL Action on pin is to set it high. TASKS_SET[1] 0x034 Task for writing to pin specified in CONFIG[0].PSEL Action on pin is to set it high. TASKS_SET[2] 0x038 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[3] 0x03C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[4] 0x040 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it high. TASKS_SET[5] 0x044 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[6] 0x044 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[6] 0x044 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[6] 0x044 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLR[0] 0x04C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLR[0] 0x04C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_CLR[1] 0x04C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x06C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is	Register	Offset	Description
TASKS_OUT[3] 0.000C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is configured in CONFIG[3].POLARITY. TASKS_OUT[6] 0.0010 Task for writing to pin specified in CONFIG[5].PSEL Action on pin is configured in CONFIG[6].POLARITY. TASKS_OUT[6] 0.0014 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].POLARITY. TASKS_OUT[7] 0.001C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].POLARITY. TASKS_SET[0] 0.0030 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is configured in CONFIG[7].POLARITY. TASKS_SET[1] 0.0034 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[2] 0.0038 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[3] 0.0032 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[3] 0.0040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[1] 0.0041 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0.0042 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0.0048 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0.0040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0.0040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0.0040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it high. TASKS_SET[8] 0.0040 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[8] 0.0050 Task for writing to pin specified in CONFIG[8].PSEL Action on pin is to set it low. TASKS_CLR[8] 0.005	TASKS_OUT[2]	0x008	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is configured in
TASKS_OUT[6] 0x010 Task for writing to pin specified in CONFIG[6] PSEL Action on pin is configured in CONFIG[6] POLARITY. TASKS_OUT[6] 0x014 Task for writing to pin specified in CONFIG[6] PSEL Action on pin is configured in CONFIG[6] POLARITY. TASKS_OUT[7] 0x012 Task for writing to pin specified in CONFIG[6] PSEL Action on pin is configured in CONFIG[6] POLARITY. TASKS_OUT[7] 0x012 Task for writing to pin specified in CONFIG[6] PSEL Action on pin is configured in CONFIG[7] PSEL Action on pin is configured in CONFIG[7] PSEL Action on pin is configured in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[7] 0x010 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[7] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL Action on pin is to set it high. TASKS_SET[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL Action on pin is to set it low. TASKS_CER[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL Action on pin is to set it low. TASKS_CER[8] 0x020 Task for writing to pin specified in CONFIG[8] PSEL			CONFIG[2].POLARITY.
TASKS_OUT[4] 0x010 Task for writing to pin specified in CONFIG[4].PSEL Action on pin is configured in CONFIG[4] POLARITY. TASKS_OUT[6] 0x018 Task for writing to pin specified in CONFIG[5].PSEL Action on pin is configured in CONFIG[6] POLARITY. TASKS_OUT[7] 0x01C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is configured in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[1] 0x030 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[8] 0x034 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[8] 0x032 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[8] 0x032 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CON	TASKS_OUT[3]	0x00C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is configured in
TASKS_OUT[6] 0x014 Task for writing to pin specified in CONFIG[6]. PSEL Action on pin is configured in CONFIG[6] POLARITY. TASKS_OUT[7] 0x012 Task for writing to pin specified in CONFIG[6]. PSEL Action on pin is configured in CONFIG[6]. PSEL Action on pin is configured in CONFIG[7]. PSEL Action on pin is constitution. TASKS_SET[7] 0x038 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it high. TASKS_SET[8] 0x043 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it high. TASKS_SET[8] 0x044 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it high. TASKS_SET[7] 0x044 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it high. TASKS_SET[8] 0x048 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it high. TASKS_SET[8] 0x048 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it high. TASKS_SET[8] 0x040 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it high. TASKS_CURIO 0x060 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it how. TASKS_CURIO 0x060 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it how. TASKS_CURIO 0x060 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it how. TASKS_CURIO 0x060 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it how. TASKS_CURIO 0x060 Task for writing to pin specified in CONFIG[7]. PSEL Action on pin is to set it how. TASKS_CURIO 0x070 Task for writing to p			CONFIG[3].POLARITY.
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TASKS_SET[5] 0x044 Task for writing to pin specified in CONFIG[5].PSEL Action on pin is to set it high. TASKS_SET[7] 0x04C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it high. TASKS_SET[7] 0x04C Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it high. TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x068 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x060 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x070 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x070 Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[1] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x070 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[6].PSEL Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[1] 0x105 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[1] 0x106 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[1] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[1] 0x116 Event generate	TASKS_SET[3]	0x03C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it high.
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TASKS_CER[7] 0x04C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it high. TASKS_CLR[1] 0x06A Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low. TASKS_CLR[1] 0x06A Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low. TASKS_CLR[2] 0x06C Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[8] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[9] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[9] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[0] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[0] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[0] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[0] 0x116 Event generated from multiple input GPIO pins with SENSE mechanism enabled EVENTS_IN[0] 0x116 Event generated from multiple input GPIO pins with SENSE mechanism enabled EVENTS_IN[0] 0x510 Configuration for OUT[n]. SET[n] and CLR[n] tasks and IN[n] event EVENTS[0] 0x521 Configuration for OUT[n]. SET[n] and CLR[n] tasks and IN[n] event EVENTS[0] 0	TASKS_SET[5]	0x044	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it high.
TASKS_CLR[0] 0x060 Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low. TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low. TASKS_CLR[2] 0x066 Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x074 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[7].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[7].PSEL. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[3] 0x100 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[8] 0x110 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[8] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[9] 0x116 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[9] 0x116 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[9] 0x110 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[9] 0x110 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[9] 0x110 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[9] 0x110 Event generated from pin specified in CONFIG[9].PSEL EVENTS_IN[9] 0x110 Event generated from pin specified in CONFIG[9].PSEL EVENTS_IN[9] 0x110 Event generated from pin specified in CONFIG[9].PSEL EVENTS_IN[9] 0x110 Event generated from pin specified in CONFIG[9].PSEL EVEN	TASKS_SET[6]	0x048	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it high.
TASKS_CLR[1] 0x064 Task for writing to pin specified in CONFIG[1].PSEL Action on pin is to set it low. TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[2].PSEL Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[4].PSEL Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[7].PSEL Action on pin is to set it low. TASKS_CLR[7] 0x100 Event generated from pin specified in CONFIG[7].PSEL Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[8] 0x304 Enable interrupt INTENCER 0x308 Disable interrupt CONFIG[8] 0x510 Configuration for OUT[1]. SET[1] and CLR[1] tasks and IN[1] event CONFIG[9] 0x510 Configuration for OUT[1]. SET[1] and CLR[1] tasks and IN[1] event CONFIG[8] 0x520 Configuration for OUT[1]. SET[1] and CLR[1] tasks and IN[1] event CONFIG[8] 0x528 Configuration for OUT[1]. SET[1] and CLR[1	TASKS_SET[7]	0x04C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it high.
TASKS_CLR[2] 0x068 Task for writing to pin specified in CONFIG[2]. PSEL. Action on pin is to set it low. TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3]. PSEL. Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[4]. PSEL. Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[6]. PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6]. PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6]. PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[6]. PSEL. Action on pin is to set it low. EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7]. PSEL EVENTS_IN[7] 0x11C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENSET 0x304 Configuration for OUT[n]. SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x518 Configuration for OUT[n]. SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x518 Configuration for OUT[n]. SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x524 Configuration for OUT[n]. SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[0]	0x060	Task for writing to pin specified in CONFIG[0].PSEL. Action on pin is to set it low.
TASKS_CLR[3] 0x06C Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low. TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[4].PSEL. Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7].PSEL Action on pin is to set it low. EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[1] 0x108 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENSET 0x304 Enable interrupt CONFIG[6] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[7] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[8] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[8] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[8] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[1]	0x064	Task for writing to pin specified in CONFIG[1].PSEL. Action on pin is to set it low.
TASKS_CLR[4] 0x070 Task for writing to pin specified in CONFIG[4], PSEL. Action on pin is to set it low. TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5]. PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6]. PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[6]. PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7]. PSEL. Action on pin is to set it low. EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[7]. PSEL EVENTS_IN[1] 0x108 Event generated from pin specified in CONFIG[7]. PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[7]. PSEL EVENTS_IN[8] 0x110 Event generated from pin specified in CONFIG[8]. PSEL EVENTS_IN[9] 0x114 Event generated from pin specified in CONFIG[8]. PSEL EVENTS_IN[9] 0x114 Event generated from pin specified in CONFIG[8]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[8]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[8]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[8]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[8]. PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[8]. PSEL EVENTS_IN[8] 0x304 Enable interrupt INTENCER 0x308 Disable interrupt CONFIG[8] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[8] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[8] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[8] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[8] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[2]	0x068	Task for writing to pin specified in CONFIG[2].PSEL. Action on pin is to set it low.
TASKS_CLR[5] 0x074 Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low. TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[6] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled interrupt intervent	TASKS_CLR[3]	0x06C	Task for writing to pin specified in CONFIG[3].PSEL. Action on pin is to set it low.
TASKS_CLR[6] 0x078 Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low. TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[4]	0x070	Task for writing to pin specified in CONFIG[4]. PSEL. Action on pin is to set it low.
TASKS_CLR[7] 0x07C Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low. EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x304 Enable interrupt INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[5]	0x074	Task for writing to pin specified in CONFIG[5].PSEL. Action on pin is to set it low.
EVENTS_IN[0] 0x100 Event generated from pin specified in CONFIG[0].PSEL EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[6].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCIA 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[6]	0x078	Task for writing to pin specified in CONFIG[6].PSEL. Action on pin is to set it low.
EVENTS_IN[1] 0x104 Event generated from pin specified in CONFIG[1].PSEL EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENCER 0x304 Enable interrupt INTENCER 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	TASKS_CLR[7]	0x07C	Task for writing to pin specified in CONFIG[7].PSEL. Action on pin is to set it low.
EVENTS_IN[2] 0x108 Event generated from pin specified in CONFIG[2].PSEL EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[0]	0x100	Event generated from pin specified in CONFIG[0].PSEL
EVENTS_IN[3] 0x10C Event generated from pin specified in CONFIG[3].PSEL EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[7].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] eve	EVENTS_IN[1]	0x104	
EVENTS_IN[4] 0x110 Event generated from pin specified in CONFIG[4].PSEL EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[2]	0x108	Event generated from pin specified in CONFIG[2].PSEL
EVENTS_IN[5] 0x114 Event generated from pin specified in CONFIG[5].PSEL EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[3]	0x10C	Event generated from pin specified in CONFIG[3].PSEL
EVENTS_IN[6] 0x118 Event generated from pin specified in CONFIG[6].PSEL EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[4]	0x110	Event generated from pin specified in CONFIG[4].PSEL
EVENTS_IN[7] 0x11C Event generated from pin specified in CONFIG[7].PSEL EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	EVENTS_IN[5]	0x114	
EVENTS_PORT 0x17C Event generated from multiple input GPIO pins with SENSE mechanism enabled INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	_		Event generated from pin specified in CONFIG[6].PSEL
INTENSET 0x304 Enable interrupt INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	_		
INTENCLR 0x308 Disable interrupt CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	_		
CONFIG[0] 0x510 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event			·
CONFIG[1] 0x514 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event			·
CONFIG[2] 0x518 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event			
CONFIG[3] 0x51C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event			
CONFIG[4] 0x520 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event			
CONFIG[5] 0x524 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event			
CONFIG[6] 0x528 Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event			
CONFIG[7] 0x52C Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event	• •		-
	CONFIG[7]	0x52C	Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

21.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31	30 2	9 2	28 2	7 26	25	24	23	22 2	21 2	0 19	9 18	17	16	15 :	L4 1	3 12	11	10	9	8	7	6 !	5 4	1 3	2	1	0
Id				L																					Н	G I	F E	E D	С	В	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						De	crip	tio	n																	
Α	RW	IN0									Wr	ite '1	l' to	Ena	ble	inte	rru	pt f	or IN	[0]	ever	nt									



Bit r	number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			T	H G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_IN[0]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW IN1			Write '1' to Enable interrupt for IN[1] event
				See EVENTS_IN[1]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW IN2			Write '1' to Enable interrupt for IN[2] event
				See EVENTS_IN[2]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW IN3			Write '1' to Enable interrupt for IN[3] event
				See EVENTS_IN[3]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW IN4			Write '1' to Enable interrupt for IN[4] event
		Cat	1	See EVENTS_IN[4] Enable
		Set Disabled	1 0	enable Read: Disabled
		Enabled	1	Read: Enabled
_	RW IN5	Ellableu	1	Write '1' to Enable interrupt for IN[5] event
•	IVVV IIVS			
				See EVENTS_IN[5]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW IN6			Write '1' to Enable interrupt for IN[6] event
				See EVENTS_IN[6]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW IN7			Write '1' to Enable interrupt for IN[7] event
				See EVENTS_IN[7]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
I	RW PORT			Write '1' to Enable interrupt for PORT event
				See EVENTS_PORT
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

21.4.2 INTENCLR

Address offset: 0x308 Disable interrupt



Bit n	iumbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L	H G F E D C B A
Rese	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	IN0			Write '1' to Disable interrupt for IN[0] event
					See EVENTS_IN[0]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	IN1			Write '1' to Disable interrupt for IN[1] event
					See EVENTS_IN[1]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	IN2			Write '1' to Disable interrupt for IN[2] event
					See EVENTS_IN[2]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	IN3			Write '1' to Disable interrupt for IN[3] event
					See EVENTS_IN[3]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	IN4			Write '1' to Disable interrupt for IN[4] event
					See EVENTS_IN[4]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	IN5			Write '1' to Disable interrupt for IN[5] event
					See EVENTS_IN[5]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
G	RW	IN6			Write '1' to Disable interrupt for IN[6] event
					See EVENTS_IN[6]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	IN7			Write '1' to Disable interrupt for IN[7] event
					See EVENTS_IN[7]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
I	RW	PORT			Write '1' to Disable interrupt for PORT event
					See EVENTS_PORT
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

21.4.3 CONFIG[0]

Address offset: 0x510



Bit num	nber		31 30	29 28	27 26	6 25	24	23 22 2	21 20	0 19	18 17	7 1	6 15	14	13 1	12 1	1 10	9	8	7 6	5 5	4	3	2	1 0
Id									D)	С	C C				ВЕ	3 B	В	В						А А
Reset 0)x00000000		0 0	0 0	0 0	0	0	0 0	0 0	0	0 0	0	0	0	0	0 (0	0	0	0 (0	0	0	0	0 0
Id R	W Field	Value Id	Value					Descrip	tion	ı															
A R	W MODE							Mode																	
		Disabled	0					Disable	d. Pi	n spe	cifie	d b	y PS	EL w	ill n	ot b	e acc	quire	d b	y th	e				
								GPIOTE	mo	dule.															
		Event	1					Event n	node	9															
								The pin	spe	cified	l by P	SEI	L wil	l be	conf	figuı	red a	s an	inp	ut a	nd t	he			
								IN[n] e	vent	will b	e ge	ner	ated	d if c	pera	atio	n spe	cifie	d in	РО	LARI	ΤY			
								occurs	on tl	ne pir	١.														
		Task	3					Task m	ode																
								The GP	IO sp	oecifi	ed by	/ PS	EL v	vill b	e co	nfig	ured	lasa	an o	utp	ut ar	nd			
								triggeri	ng tl	ne SE	T[n],	CLF	R[n]	or C	UT[n] ta	ask w	/ill p	erfo	rm	the				
								operati	on s	pecif	ed b	y P	OLA	RITY	on t	the	pin. ۱		n er	nabl	ed a	s a			
								task the	e GP	IOTE	mod	ule	will	acq	uire	the	pin a	and 1	he į	oin	can r	10			
								longer	be w	ritte	n as a	re	gula	r ou	tput	pin	fron	n the	e GP	10 ו	nod	ule.			
B R\	W PSEL		[031]					GPIO n	umb	er as	socia	ted	wit	h SE	T[n]	, CLI	R[n]	and	OUT	[n]	task	S			
								and IN[n] e	vent															
C R\	W POLARITY							When I	n tas	sk mo	de: 0	Эре	erati	on t	o be	per	form	ed o	n o	utp	ut				
								when C	TUC	n] tas	k is t	rigg	gere	d. W	/hen	ı In e	even	t mc	de:	Ope	erati	on			
								on inpu	it th	at sha	all trig	gge	r IN	[n] e	ven	t.									
		None	0					Task m	ode:	No e	ffect	on	pin	fror	n Ol	JT[n] tas	k. Ev	ent	mo	de: r	10			
								IN[n] e	vent	gene	rated	d or	n pir	act	ivity										
		LoToHi	1					Task m	ode:	Set p	in fr	om	OU.	T[n]	task	. Ev	ent r	node	e: G	ene	rate				
								IN[n] e				_	-												
		HiToLo	2					Task m			•			_	-		ven	mo	de:	Ger	erat	e			
								IN[n] e				-	_												
		Toggle	3					Task m		-	•				[n].	Eve	nt m	ode:	Gei	nera	ite				
D 51	AL OLITIBUT							IN[n] w				_	-		-6,1					. I	CDIC	\ T F			
D R\	W OUTINIT							When i													GPIC	JΙĒ			
		Low	0					channe																	
		Low	0					Task m											-						
		High	1					Task m	oue:	mitia	ıı vall	ue (oi bi	11 DE	TOTE	: tas	K (FIE	ger	ırıg I	s ni	RII				

21.4.4 CONFIG[1]

Address offset: 0x514

Bit r	numbe	er		31	1 30	29	28	27	26 2	5 2	24 2	23 2	2 2	21 2	0 1	L9 1	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id														ı	D			С	С				В	В	В	В	В						Α	A
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0	0 (0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue						ı	Desc	crip	tio	n																			
Α	RW	MODE									ı	Mod	le																					
			Disabled	0							[Disa	ble	d. P	in:	spe	cifi	ed	by	PSE	Lν	will	not	be	acc	uir	ed b	y t	he					
											(GPIC	DTE	mo	odu	le.																		
			Event	1							E	Ever	nt n	nod	e																			
											1	The	pin	spe	ecif	ied	by	PS	EL،	will	be	e co	nfig	gure	d a	s ar	inp	out	and	d th	e			
											ı	IN[n] ev	/ent	t w	ill b	e g	en	era	ted	if	оре	erat	ion	spe	cifi	ed i	n P	OLA	ARIT	Υ			
											(occu	ırs	on t	he	pin	١.																	
			Task	3							1	Task	m	ode																				
											1	The	GΡ	IO s	pe	cifie	ed I	by I	PSE	Lw	rill I	be	con	figu	red	as	an d	out	put	and	d			
											t	trigg	eri	ng t	he	SET	Γ[n], C	LR[n] (or (OU.	T[n]	tas	k w	ill p	erf	orn	n th	e				
											(oper	rati	on s	spe	cifi	ed	by	РΟ	LAF	RITY	Y oı	n th	e pi	n. \	Vhe	n e	nal	oled	l as	a			
											t	task	the	e GF	910	TE i	mo	du	e w	/ill a	acc	quir	e th	ne p	in a	nd	the	pir	ı caı	n n	0			
											ı	long	er l	oe v	vrit	ter	ı as	a	regi	ular	r oı	utp	ut p	in f	ron	n th	e G	PIO	mc	odu	le.			



Bit n	umbe	r		31 3	0 29	28	27	26 2	25 2	4 23	3 22	21	20	19 1	.8 1	17 1	6 1	5 14	13	12 :	11 1	0 9	8	7	6	5 4	4 3	2	1	0
Id													D		(C C				В	ВЕ	В	В						Α	Α
Rese	t 0x0	0000000		0 0	0	0	0	0 (0 (0 0	0	0	0	0 (0 (0 0	0	0	0	0	0 (0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Valu	е					D	escr	iptio	on																	
В	RW	PSEL		[03	1]					GI	PIO	num	ber	ass	ocia	ated	l wi	th S	ET[n], Cl	.R[n]	and	OU	T[n] tas	sks				
										ar	nd II	N[n]	eve	nt																
С	RW	POLARITY								W	/hen	ı In t	ask	mod	de:	Оре	erat	ion	to b	e pe	rfor	ned	on	out	ut					
										W	hen	OU.	T[n]	task	k is	trig	ger	ed. \	Whe	n In	eve	nt m	ode	: Op	era	tior	1			
										or	n inp	out t	hat	shal	ll tr	igge	er IN	l[n]	ever	nt.										
			None	0						Ta	sk r	mod	e: N	o ef	fec	t on	pir	fro	m O	UT[ı	n] ta	sk. E	ven	t m	ode	: no				
										IN	l[n]	evei	nt g	ener	ate	ed o	n pi	n ac	tivit	у.										
			LoToHi	1						Ta	sk r	mod	e: S	et pi	in f	rom	OU	IT[n] tas	k. Ev	ent	mod	de: 0	Sen	erat	e				
										IN	l[n]	evei	nt w	hen	ris	ing	edg	e or	pin											
			HiToLo	2						Ta	sk r	nod	e: C	lear	pin	fro	m (DUT	[n] t	ask.	Eve	nt m	ode	: Ge	ner	ate				
										IN	l[n]	evei	nt w	hen	fal	ling	edg	ge o	n pir	١.										
			Toggle	3						Ta	sk r	nod	e: T	oggl	e p	in fr	om	OU	T[n]	. Eve	nt r	node	e: G	ene	ate					
										IN	l[n]	whe	n aı	ny cł	han	ige o	on p	in.												
D	RW	OUTINIT								W	hen	in t	ask	mod	de:	Initi	ial v	alue	e of	the o	outp	ut w	hen	the	GP	TOI	E			
										ch	nanr	nel is	coı	nfigu	ıred	d. W	/her	n in	ever	nt m	ode	No	effe	ct.						
			Low	0						Ta	sk r	nod	e: Ir	itial	l va	lue	of p	in b	efor	e ta	sk tr	igge	ring	is l	w					
			High	1						Ta	sk r	nod	e: Ir	itial	l va	lue	of p	in b	efor	e ta	sk tr	igge	ring	is h	igh					

21.4.5 CONFIG[2]

Address offset: 0x518

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				D CC BBBBB AA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	RW	MODE		Mode
			Disabled	O Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.
			Event	1 Event mode
				The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.
			Task	3 Task mode
				The GPIO specified by PSEL will be configured as an output and
				triggering the SET[n], CLR[n] or OUT[n] task will perform the
				operation specified by POLARITY on the pin. When enabled as a
				task the GPIOTE module will acquire the pin and the pin can no
_				longer be written as a regular output pin from the GPIO module.
В	RW	PSEL		[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks and IN[n] event
С	RW	POLARITY		When In task mode: Operation to be performed on output
				when OUT[n] task is triggered. When In event mode: Operation
				on input that shall trigger IN[n] event.
			None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
				IN[n] event generated on pin activity.
			LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
				IN[n] event when rising edge on pin.
			HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
				IN[n] event when falling edge on pin.
			Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
				IN[n] when any change on pin.



Bit numb	er		31	1 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	3 7	7 6	5	4	3	2	1	0
Id														D			С	С				В	В	В	В	3						Α	Α
Reset 0x	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0
ld RW	Field	Value Id	Va	alue							De	scr	iptio	on																			
D RW	OUTINIT										Wh	nen	in t	tasl	k m	ode	e: In	itia	l va	lue	of	the	out	put	wh	en t	he (SPIC	OTE				
											cha	ann	el is	s cc	onfi	gur	ed.	Wh	nen	in e	evei	nt m	ode	: N	o e	fec	t.						
		Low	0								Tas	sk r	nod	le: I	Initi	al v	alu	e o	f pi	n b	efor	e ta	sk t	rigg	geri	ng i	lov	v					
		High	1								Tas	sk r	nod	le: I	Initi	al v	alu	e o	f pi	n b	efor	e ta	sk t	rigg	geri	ng i	hig	gh					

21.4.6 CONFIG[3]

Address offset: 0x51C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit	numb	er		3	1 30	29	28	27	26	25	24	23	22 2	1 20	19	9 18	17	16	15	14	13	12	11	10	9	8	7 (5 5	5 4	3	2	1
Id														D	1		С	С				В	В	В	В	В						Α
Res	et 0x(00000000		0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0
Id	RW	Field	Value Id	٧	/alue	9						De	escrip	tion																		
Α	RW	MODE										М	ode																			
			Disabled	0)							Di	sable	d. Pi	n s	peci	fiec	l by	PS	EL v	vill ı	not	be a	icqu	iire	d by	y th	e				
												GF	PIOTE	mod	dul	e.																
			Event	1								Ev	ent n	ode	•																	
												Th	ie pin	spe	cifi	ed b	y P	SEL	wil	l be	coı	nfig	ure	d as	an	inpı	ut a	nd	the			
												IN	[n] ev	ent	wil	l be	ger	nera	iteo	d if	pe	rati	on s	pec	ifie	d in	РС	LAF	RITY			
												oc	curs	on th	ne p	oin.																
			Task	3								Та	sk mo	ode																		
												Th	ie GPI	O sn	eci	ified	bv	PSI	EL v	vill l	ne c	onf	igur	ed a	as a	n o	utn	ut a	ınd			
													ggeri										-									
													erati	-		-									•							
													sk the										•									
												loi	nger l	oe w	ritt	en a	is a	reg	ula	r oı	ıtpı	ıt p	in fr	om	the	GP	10	noc	dule			
В	RW	PSEL		[031	L]						GF	PIO nu	ımb	er a	asso	ciat	ed	wit	h Si	T[n], C	LR[r	n] ar	nd (TUC	[n]	tas	ks			
												an	d IN[n] ev	/en	t																
С	RW	POLARITY										W	hen I	n tas	k n	nod	e: C	pei	ati	on t	o b	ер	erfo	rme	d o	n o	utp	ut				
												wl	hen O	ı]TU	n] t	ask	is tı	igg	ere	d. V	Vhe	n Ir	eve	ent	mo	de:	Ор	erat	ion			
												or	inpu	t tha	at s	hall	trig	ger	IN	[n] (evei	nt.										
			None	0)							Ta	sk mo	ode:	No	eff	ect	on	pin	fro	n O	UT	n] t	ask.	Ev	ent	mo	de:	no			
												IN	[n] ev	ent	ger	nera	ted	on	pir	ac	ivit	у.										
			LoToHi	1								Ta	sk mo	ode:	Set	t pir	fro	m	DU.	Γ[n]	tas	k. E	ven	t mo	ode	: G	ene	rate	9			
												IN	[n] ev	ent	wh	en i	isin	g e	dge	on	pin											
			HiToLo	2								Ta	sk mo	ode:	Cle	ear p	in f	ror	n O	UT[n] t	ask	Eve	ent i	mo	de:	Ger	nera	ite			
													[n] ev					-	_		•											
			Toggle	3									isk mo				•				[[n]	. Ev	ent	mo	de:	Ger	nera	ate				
													[n] w				_		-													
D	RW	OUTINIT											hen ii															GPI	OTI			
													anne			-																
			Low	0									isk mo											-		_						
			High	1								Ta	sk mo	ode:	Ini	tial	valι	ie o	t pi	n b	efor	e t	isk t	rigg	geri	ng i	s hi	gh				

21.4.7 CONFIG[4]

Address offset: 0x520



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	D CC BBBBB AA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW MODE	Mode
Disabled	O Disabled. Pin specified by PSEL will not be acquired by the
	GPIOTE module.
Event	1 Event mode
	The pin specified by PSEL will be configured as an input and the
	IN[n] event will be generated if operation specified in POLARITY
	occurs on the pin.
Task	3 Task mode
	The GPIO specified by PSEL will be configured as an output and
	triggering the SET[n], CLR[n] or OUT[n] task will perform the
	operation specified by POLARITY on the pin. When enabled as a
	task the GPIOTE module will acquire the pin and the pin can no
	longer be written as a regular output pin from the GPIO module.
B RW PSEL	[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
	and IN[n] event
C RW POLARITY	When In task mode: Operation to be performed on output
	when OUT[n] task is triggered. When In event mode: Operation
	on input that shall trigger IN[n] event.
None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
	IN[n] event generated on pin activity.
LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
	IN[n] event when rising edge on pin.
HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
	IN[n] event when falling edge on pin.
Toggle	3 Task mode: Toggle pin from OUT[n]. Event mode: Generate
	IN[n] when any change on pin.
D RW OUTINIT	When in task mode: Initial value of the output when the GPIOTE
	channel is configured. When in event mode: No effect.
Low	0 Task mode: Initial value of pin before task triggering is low
High	1 Task mode: Initial value of pin before task triggering is high

21.4.8 CONFIG[5]

Address offset: 0x524

	·	_		-							-	-																						
Bit r	numbe	er		31	. 30	29	28 2	27 :	26 2	5 2	4 2	23 22	2 21	L 20	19	18	3 1	7 1	6 1	15	14	13	12	11 :	LO	9	8	7	6 !	5 4	1 3	2	1	0
Id														D			C	. (2				В	В	В	В	В						Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0) (0 0	0	0	0	0	0) () (0	0	0	0	0	0	0	0 (0	0 (0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						0	Desc	ript	ion																				
Α	RW	MODE									N	√lod•	е																					
			Disabled	0							0	Disab	led	. Pir	ı sp	eci	ifie	d b	y P	SE	Lw	ill n	ot	oe a	cqı	uire	d b	y th	ne					
											C	SPIO	TE	mod	lule	2.																		
			Event	1							Е	ven	t m	ode																				
											Т	he p	oin s	spec	ifie	ed b	oy F	PSE	Lw	/ill	be (con	ıfigı	ired	l as	an	inp	ut a	and	the				
											П	N[n]	eve	ent v	will	be	ge	ne	rate	ed	if o	per	atio	n s	pec	ifie	d in	PC	DLA	RITY	,			
											c	occui	rs o	n th	ер	in.																		
			Task	3							Т	ask	mo	de																				
											Т	he (SPIC) sp	eci	fied	d by	y P	SEL	wi	ll b	e co	onfi	gur	ed	as a	n o	utp	out a	and				
											t	rigge	erin	g th	e S	ET[[n],	CL	R[n	n] o	r O	UT	[n]	task	wi	ll p	erfo	rm	the					
											c	per	atio	n sp	eci	ifie	d b	у Р	OL	AR	ITY	on	the	pir	. W	/he	n er	ab	led	as a	ı			
											t	ask 1	the	GPI	ОТІ	E m	od	ule	wi	II a	cqı	iire	the	e pii	n ar	nd t	he p	oin	can	no				
											le	onge	er b	e wi	ritte	en a	as a	a re	gu	lar	out	pu	t pi	n fr	om	the	e GP	10	mo	dule	è.			



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	D CC BBBBB AA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
B RW PSEL	[031] GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
	and IN[n] event
C RW POLARITY	When In task mode: Operation to be performed on output
	when OUT[n] task is triggered. When In event mode: Operation
	on input that shall trigger IN[n] event.
None	0 Task mode: No effect on pin from OUT[n] task. Event mode: no
	IN[n] event generated on pin activity.
LoToHi	1 Task mode: Set pin from OUT[n] task. Event mode: Generate
	IN[n] event when rising edge on pin.
HiToLo	2 Task mode: Clear pin from OUT[n] task. Event mode: Generate
	IN[n] event when falling edge on pin.
Toggle	Task mode: Toggle pin from OUT[n]. Event mode: Generate
	IN[n] when any change on pin.
D RW OUTINIT	When in task mode: Initial value of the output when the GPIOTE
	channel is configured. When in event mode: No effect.
Low	0 Task mode: Initial value of pin before task triggering is low
High	1 Task mode: Initial value of pin before task triggering is high

21.4.9 CONFIG[6]

Address offset: 0x528

Bit nur	mbe	r		31 30 29 28 27 26 25	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id					D C C B B B B B A
Reset	0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld F	RW	Field	Value Id	Value	Description
A F	RW	MODE			Mode
			Disabled	0	Disabled. Pin specified by PSEL will not be acquired by the
					GPIOTE module.
			Event	1	Event mode
					The pin specified by PSEL will be configured as an input and the
					IN[n] event will be generated if operation specified in POLARITY
					occurs on the pin.
			Task	3	Task mode
					The GPIO specified by PSEL will be configured as an output and
					triggering the SET[n], CLR[n] or OUT[n] task will perform the
					operation specified by POLARITY on the pin. When enabled as a
					task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.
B F	D\A/	PSEL		[031]	GPIO number associated with SET[n], CLR[n] and OUT[n] tasks
ь г	I V V	FJLL		[031]	and IN[n] event
C F	R\M	POLARITY			When In task mode: Operation to be performed on output
		1 OLJ MATT			when OUT[n] task is triggered. When In event mode: Operation
					on input that shall trigger IN[n] event.
			None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no
					IN[n] event generated on pin activity.
			LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate
					IN[n] event when rising edge on pin.
			HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate
					IN[n] event when falling edge on pin.
			Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate
					IN[n] when any change on pin.



Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id													D			С	С				ВЕ	В	В	В						Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0
ld RW Field	Value Id	Va	lue							De	scr	ipti	on																		
D RW OUTINIT										W	hen	in	tasl	c mo	ode	: In	itia	l va	lue	of tl	ne o	utpı	ıt w	her	th	e GF	2101	Έ			
										ch	ann	el i	s cc	nfig	gur	ed.	Wh	en	in e	ven	mc	de:	No	effe	ct.						
	Low	0								Ta	sk r	noc	le: I	niti	al v	alu	e o	f piı	n be	fore	tas	k tri	gge	ring	is I	ow					
	High	1								Та	sk r	noc	le: I	niti	al v	alu	e o	f piı	n be	fore	tas	k tri	gge	ring	is l	nigh					

21.4.10 CONFIG[7]

Address offset: 0x52C

Configuration for OUT[n], SET[n] and CLR[n] tasks and IN[n] event

Bit	numb	er		3	1 30	29	28	27	26	25	24	23	22 2	1 20	19	9 18	17	16	15	14	13	12	11	10	9	8	7 (5 5	5 4	3	2	1
Id														D	1		С	С				В	В	В	В	В						Α
Res	et 0x(00000000		0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0
Id	RW	Field	Value Id	٧	/alue	9						De	escrip	tion																		
Α	RW	MODE										М	ode																			
			Disabled	0)							Di	sable	d. Pi	n s	peci	fiec	l by	PS	EL v	vill ı	not	be a	icqu	iire	d by	y th	e				
												GF	PIOTE	mod	dul	e.																
			Event	1								Ev	ent n	ode	•																	
												Th	ie pin	spe	cifi	ed b	y P	SEL	wil	l be	coı	nfig	ure	d as	an	inpı	ut a	nd	the			
												IN	[n] ev	ent	wil	l be	ger	nera	iteo	d if	pe	rati	on s	pec	ifie	d in	РС	LAF	RITY			
												oc	curs	on th	ne p	oin.																
			Task	3								Та	sk mo	ode																		
												Th	ie GPI	O sn	eci	ified	bv	PSI	EL v	vill l	ne c	onf	igur	ed a	as a	n o	utn	ut a	ınd			
													ggeri										-									
													erati	-		-									•							
													sk the										•									
												loi	nger l	oe w	ritt	en a	is a	reg	ula	r oı	ıtpı	ıt p	in fr	om	the	GP	10	noc	dule			
В	RW	PSEL		[031	L]						GF	PIO nu	ımb	er a	asso	ciat	ed	wit	h Si	T[n], C	LR[r	n] ar	nd (TUC	[n]	tas	ks			
												an	d IN[n] ev	/en	t																
С	RW	POLARITY										W	hen I	n tas	k n	nod	e: C	pei	ati	on t	o b	ер	erfo	rme	d o	n o	utp	ut				
												wl	hen O	ı]TU	n] t	ask	is tı	igg	ere	d. V	Vhe	n Ir	eve	ent	mo	de:	Ор	erat	ion			
												or	inpu	t tha	at s	hall	trig	ger	IN	[n] (evei	nt.										
			None	0)							Ta	sk mo	ode:	No	eff	ect	on	pin	fro	n O	UT	n] t	ask.	Ev	ent	mo	de:	no			
												IN	[n] ev	ent	ger	nera	ted	on	pir	ac	ivit	у.										
			LoToHi	1								Ta	sk mo	ode:	Set	t pir	fro	m	DU.	Γ[n]	tas	k. E	ven	t mo	ode	: G	ene	rate	9			
												IN	[n] ev	ent	wh	en i	isin	g e	dge	on	pin											
			HiToLo	2								Ta	sk mo	ode:	Cle	ear p	in f	ror	n O	UT[n] t	ask	Eve	ent i	mo	de:	Ger	nera	ite			
													[n] ev					-	_		•											
			Toggle	3									isk mo				•				[[n]	. Ev	ent	mo	de:	Ger	nera	ate				
													[n] w				_		-													
D	RW	OUTINIT											hen ii															GPI	OTI			
													anne			-																
			Low	0									isk mo											-		_						
			High	1								Ta	sk mo	ode:	Ini	tial	valι	ie o	t pi	n b	efor	e t	isk t	rigg	geri	ng i	s hi	gh				

21.5 Electrical specification

21.5.1 GPIOTE Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{GPIOTE,IN}	Run current with 1 or more GPIOTE active channels in Input		0.1	0.5	μΑ
	mode				



22 PPI — Programmable peripheral interconnect

The Programmable peripheral interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

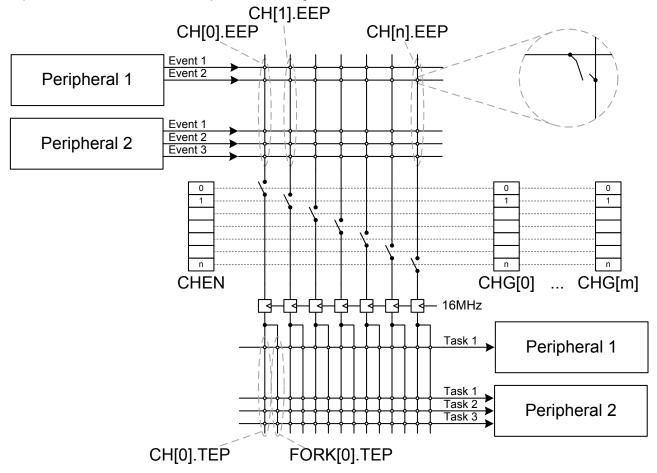


Figure 28: PPI block diagram

The PPI system has, in addition to the fully programmable peripheral interconnections, a set of channels where the event end point (EEP) and task end points (TEP) are fixed in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels.

Table 35: Configurable and fixed PPI channels

Instance	Channel	Number of channels	Number of groups
PPI	0-19	20	6
PPI (fixed)	20-31	12	

The PPI provides a mechanism to automatically trigger a task in one peripheral as a result of an event occurring in another peripheral. A task is connected to an event through a PPI channel. The PPI channel is composed of three end point registers, one EEP and two TEPs. A peripheral task is connected to a TEP using the address of the task register associated with the task. Similarly, a peripheral event is connected to an EEP using the address of the event register associated with the event.

On each PPI channel, the signals are synchronized to the 16 MHz clock, to avoid any internal violation of setup and hold timings. As a consequence, events that are synchronous to the 16 MHz clock will be delayed by one clock period, while other asynchronous events will be delayed by up to one 16 MHz clock period.



Note that shortcuts (as defined in the SHORTS register in each peripheral) are not affected by this 16 MHz synchronization, and are therefore not delayed.

Each TEP implements a fork mechanism that enables a second task to be triggered at the same time as the task specified in the TEP is triggered. This second task is configured in the task end point register in the FORK registers groups, e.g. FORK.TEP[0] is associated with PPI channel CH[0].

There are two ways of enabling and disabling PPI channels:

- Enable or disable PPI channels individually using the CHEN, CHENSET, and CHENCLR registers.
- Enable or disable PPI channels in PPI channel groups through the groups' ENABLE and DISABLE tasks.
 Prior to these tasks being triggered, the PPI channel group must be configured to define which PPI channels belongs to which groups.

Note that when a channel belongs to two groups m and n, and CHG[m].EN and CHG[n].DIS occur simultaneously (m and n can be equal or different), EN on that channel has priority.

PPI tasks (for example, CHG[0].EN) can be triggered through the PPI like any other task, which means they can be hooked up to a PPI channel as a TEP. One event can trigger multiple tasks by using multiple channels and one task can be triggered by multiple events in the same way.

22.1 Pre-programmed channels

Some of the PPI channels are pre-programmed. These channels cannot be configured by the CPU, but can be added to groups and enabled and disabled like the general purpose PPI channels. The FORK TEP for these channels are still programmable and can be used by the application.

For a list of pre-programmed PPI channels, see the table below.

Table 36: Pre-programmed channels

Channel	EEP	TEP
20	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
21	TIMERO->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
22	TIMERO->EVENTS_COMPARE[1]	RADIO->TASKS_DISABLE
23	RADIO->EVENTS_BCMATCH	AAR->TASKS_START
24	RADIO->EVENTS_READY	CCM->TASKS_KSGEN
25	RADIO->EVENTS_ADDRESS	CCM->TASKS_CRYPT
26	RADIO->EVENTS_ADDRESS	TIMERO->TASKS_CAPTURE[1]
27	RADIO->EVENTS_END	TIMERO->TASKS_CAPTURE[2]
28	RTCO->EVENTS_COMPARE[0]	RADIO->TASKS_TXEN
29	RTCO->EVENTS_COMPARE[0]	RADIO->TASKS_RXEN
30	RTCO->EVENTS_COMPARE[0]	TIMERO->TASKS_CLEAR
31	RTCO->EVENTS_COMPARE[0]	TIMERO->TASKS_START

22.2 Registers

Table 37: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001F000	PPI	PPI	Programmable Peripheral Interconnect	

Table 38: Register Overview

Register	Offset	Description
TASKS_CHG[0].EN	0x000	Enable channel group 0
TASKS_CHG[0].DIS	0x004	Disable channel group 0
TASKS_CHG[1].EN	0x008	Enable channel group 1
TASKS_CHG[1].DIS	0x00C	Disable channel group 1
TASKS_CHG[2].EN	0x010	Enable channel group 2
TASKS_CHG[2].DIS	0x014	Disable channel group 2
TASKS_CHG[3].EN	0x018	Enable channel group 3
TASKS_CHG[3].DIS	0x01C	Disable channel group 3
TASKS_CHG[4].EN	0x020	Enable channel group 4



Register	Offset	Description
TASKS_CHG[4].DIS	0x024	Disable channel group 4
TASKS_CHG[5].EN	0x028	Enable channel group 5
TASKS_CHG[5].DIS	0x02C	Disable channel group 5
CHEN	0x500	Channel enable register
CHENSET	0x504	Channel enable set register
CHENCLR	0x508	Channel enable clear register
CH[0].EEP	0x510	Channel 0 event end-point
CH[0].TEP	0x514	Channel 0 task end-point
CH[1].EEP	0x518	Channel 1 event end-point
CH[1].TEP	0x51C	Channel 1 task end-point
CH[2].EEP	0x520	Channel 2 event end-point
CH[2].TEP	0x524	Channel 2 task end-point
CH[3].EEP	0x528	Channel 3 event end-point
CH[3].TEP	0x52C	Channel 3 task end-point
CH[4].EEP	0x530	Channel 4 event end-point
CH[4].TEP	0x534	Channel 4 task end-point
CH[5].EEP	0x538	Channel 5 event end-point
CH[5].TEP	0x53C	Channel 5 task end-point
CH[6].EEP	0x540	Channel 6 event end-point
CH[6].TEP	0x544	Channel 6 task end-point
CH[7].EEP	0x548	Channel 7 event end-point
CH[7].TEP	0x54C	Channel 7 task end-point
CH[8].EEP	0x550	Channel 8 event end-point
CH[8].TEP	0x554	Channel 8 task end-point
CH[9].EEP	0x558	Channel 9 event end-point
CH[9].TEP	0x55C	Channel 9 task end-point
CH[10].EEP	0x560	Channel 10 event end-point
CH[10].TEP	0x564	Channel 10 task end-point
CH[11].EEP	0x568	Channel 11 event end-point
CH[11].TEP	0x56C	Channel 11 task end-point
CH[12].EEP	0x570	Channel 12 event end-point
CH[12].TEP	0x570	Channel 12 task end-point
CH[13].EEP	0x578	Channel 13 event end-point
CH[13].TEP	0x57C	Channel 13 task end-point
CH[14].EEP	0x580	Channel 14 event end-point
CH[14].TEP	0x584	Channel 14 task end-point
CH[15].EEP	0x588	Channel 15 event end-point
CH[15].TEP	0x58C	Channel 15 task end-point
CH[16].EEP	0x590	Channel 16 event end-point
CH[16].TEP	0x594	Channel 16 task end-point
CH[17].EEP	0x594 0x598	Channel 17 event end-point
CH[17].TEP	0x59C	Channel 17 task end-point Channel 17 task end-point
CH[18].EEP	0x5A0	Channel 18 event end-point
CH[18].TEP	0x5A4	Channel 18 task end-point
CH[19].EEP	0x5A4 0x5A8	Channel 19 event end-point
CH[19].TEP	0x5A6 0x5AC	Channel 19 task end-point
CHG[0]	0x800	Channel group 0
CHG[1]	0x800	Channel group 1
CHG[2]	0x804 0x808	Channel group 2
CHG[2]	0x80C	Channel group 3
CHG[4]	0x80C 0x810	Channel group 4
CHG[5]	0x810 0x814	Channel group 5
FORK[0].TEP	0x910	Channel 1 task and point
FORK[1].TEP	0x914	Channel 1 task end-point
FORK[2].TEP	0x918	Channel 2 task end-point
FORK[3].TEP	0x91C	Channel 3 task end-point
FORK[4].TEP	0x920	Channel 4 task end-point
FORK[5].TEP	0x924	Channel 5 task end-point



Register	Offset	Description	
FORK[6].TEP	0x928	Channel 6 task end-point	
FORK[7].TEP	0x92C	Channel 7 task end-point	
FORK[8].TEP	0x930	Channel 8 task end-point	
FORK[9].TEP	0x934	Channel 9 task end-point	
FORK[10].TEP	0x938	Channel 10 task end-point	
FORK[11].TEP	0x93C	Channel 11 task end-point	
FORK[12].TEP	0x940	Channel 12 task end-point	
FORK[13].TEP	0x944	Channel 13 task end-point	
FORK[14].TEP	0x948	Channel 14 task end-point	
FORK[15].TEP	0x94C	Channel 15 task end-point	
FORK[16].TEP	0x950	Channel 16 task end-point	
FORK[17].TEP	0x954	Channel 17 task end-point	
FORK[18].TEP	0x958	Channel 18 task end-point	
FORK[19].TEP	0x95C	Channel 19 task end-point	
FORK[20].TEP	0x960	Channel 20 task end-point	
FORK[21].TEP	0x964	Channel 21 task end-point	
FORK[22].TEP	0x968	Channel 22 task end-point	
FORK[23].TEP	0x96C	Channel 23 task end-point	
FORK[24].TEP	0x970	Channel 24 task end-point	
FORK[25].TEP	0x974	Channel 25 task end-point	
FORK[26].TEP	0x978	Channel 26 task end-point	
FORK[27].TEP	0x97C	Channel 27 task end-point	
FORK[28].TEP	0x980	Channel 28 task end-point	
FORK[29].TEP	0x984	Channel 29 task end-point	
FORK[30].TEP	0x988	Channel 30 task end-point	
FORK[31].TEP	0x98C	Channel 31 task end-point	

22.2.1 CHEN

Address offset: 0x500 Channel enable register

		<u> </u>																												
Bit	numb	er		31 3	30 2	29 2	8 27	26 2	25 2	24 2	23 :	22 2	21 2	20 1	9 18	3 17	16	15	14	13 1	2 11	10	9	8	7	6 5	5 4	3	2	1 0
Id				f	e	d (c b	а	Z	Υ)	X '	W '	V	U T	S	R	Q	Р	0	N N	1 L	K	J	1	Н	G I	E	D	С	ВА
Res	et 0x0	0000000		0	0	0 (0 0	0	0	0 (0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe					D	Des	scrip	otio	n																
Α	RW	CH0								E	na	ble	or (disal	ole d	char	nel	0												
			Disabled	0						D	Disa	able	cha	anne	el															
			Enabled	1						Е	na	able	cha	nne	I															
В	RW	CH1								Е	na	able	or (disal	ole o	har	nel	1												
			Disabled	0						D	Disa	able	cha	anne	el															
			Enabled	1						Е	na	able	cha	nne	I															
С	RW	CH2								Е	na	ble	or (disal	ole o	har	nel	2												
			Disabled	0							Disa	able	cha	anne	el															
			Enabled	0 1							na	ble	cha	nne	I															
D	RW	CH3								Е	na	able	or (disal	ole o	har	nel	3												
			Disabled	0							Disa	able	cha	anne	el															
			Enabled	1						Е	na	able	cha	nne	I															
Ε	RW	CH4								Е	na	ble	or (disal	ole o	har	nel	4												
			Disabled	0						D	Disa	able	cha	anne	el															
			Enabled	1						Е	na	ble	cha	nne	I															
F	RW	CH5								Е	na	able	or (disal	ole o	har	nel	5												
			Disabled	0						D	Disa	able	cha	anne	el															
			Enabled	1						Е	na	ble	cha	nne	I															
G	RW	CH6								E	na	ble	or (disal	ole o	har	nel	6												
			Disabled	0						D	Disa	able	ch	anne	el															
			Enabled	1						Е	na	ble	cha	nne	I															
Н	RW	CH7								Е	na	ble	or (disal	ole d	har	nel	7												



DILI	iumbe	er		31 30	29 28	27 20	6 25 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				f e	d c	b a	ΖY	X W V U T S R Q P O N M L K J I H G F E D C B
Res	et 0x0	0000000		0 0	0 0	0 0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value				Description
			Disabled	0				Disable channel
			Enabled	1				Enable channel
I	RW	CH8						Enable or disable channel 8
			Disabled	Enable or disable channel 8 bibled 1 Enable channel 1 Enable or disable channel 9 bibled 1 Enable or disable channel 9 bibled 1 Enable or disable channel 9 bibled 1 Enable or disable channel 10 bibled 1 Enable or disable channel 10 bibled 1 Enable or disable channel 11 bibled 1 Enable or disable channel 11 bibled 1 Enable or disable channel 11 bibled 1 Enable or disable channel 12 bibled 1 Enable or disable channel 12 bibled 1 Enable or disable channel 13 bibled 1 Enable or disable channel 13 bibled 1 Enable or disable channel 14 bibled 1 Enable or disable channel 14 bibled 1 Enable or disable channel 14 bibled 1 Enable or disable channel 15 bibled 1 Enable or disable channel 15 bibled 1 Enable or disable channel 15 bibled 1 Enable or disable channel 16 bibled 1 Enable or disable channel 16 bibled 1 Enable or disable channel 18 bibled 1 Enable or disable channel 18 bibled 1 Enable or disable channel 19 bibled 1 Enable or disable channel 19 bibled 1 Enable channel 10 bi				
			Enabled	1				Enable channel
J	RW	CH9		Enable or disable channel Enable or disable channel Enable or disable channel				
			Disabled	Enable or disable channel				
			Enabled	Disable channel Enable or disable channel 8 Disable channel Enable or disable channel 8 Disable channel Enable or disable channel 9 Disable channel Enable or disable channel 10 Disable channel Enable or disable channel 10 Disable channel Enable or disable channel 11 Disable channel Enable or disable channel 11 Disable channel Enable or disable channel 12 Disable channel Enable or disable channel 12 Disable channel Enable or disable channel 13 Disable channel Enable or disable channel 14 Disable channel Enable or disable channel 15 Disable channel Enable or disable channel 14 Disable channel Enable or disable channel 14 Disable channel Enable or disable channel 17 Disable channel Enable or disable channel 14 Disable channel Enable or disable channel 16 Disable channel Enable or disable channel 17 Disable channel Enable or disable channel 18 Disable channel Enable or disable channel 19 Disable channel Enable or disable channel 16 Disable channel Enable or disable channel 16 Disable channel Enable or disable channel 16 Disable channel Enable or disable channel 17 Disable channel Enable or disable channel 17 Disable channel Enable or disable channel 19 Disable channel Enable or disable channel 20 Disable channel Enable or disable channel 21 Disable channel Enable or disable channel 22 Disable channel Enable or disable channel 23 Disable channel Enable or disable channel 23 Disable channel Enable or disable channel 24				
K	RW	CH10	Disabled 0 Disable channel Enabled 1 Enable channel Disabled 0 Disable channel Enabled 1 Enable channel Disabled 0 Disable channel Disabled 0 Disable channel Enable Channel 1 Enable channel Disabled 0 Disable channel Enabled 1 Enable channel Disabled 0 Disable channel Enabled 1 Enable channel Enabled 1 Enable channel Enabled 0 Disable channel Enabled 1 Enable channel Enabled 0 Disable channel Enabled 0 Disable channel Enable					
			Disabled	0				Disable channel
			Enabled	1				Enable channel
L	RW	CH11						Enable or disable channel 11
			Disabled	0				Disable channel
			Enabled	1				Enable channel
М	RW	CH12						
			Enabled	1				Enable channel
N	RW	CH13						Enable or disable channel 13
			Disabled	0				Disable channel
			Enabled	1				
0	RW	CH14		Disable channel Enable or disable channel				
			Disabled	Quality Description Disable channel Disa				
			Enabled	1				Enable channel
Р	RW	CH15		Value Description 0 Disable channel 1 Enable channel 6 Disable channel 1 Enable or disable channel 1 Enable channel 6 Disable channel 1 Enable or disable channel 1 Enable channel 1 Enable channel 2 Disable channel 3 Enable channel 4 Enable channel 5 Enable channel 6 Disable channel 1 Enable channel 6 Disable channel 1 Enable channel 1 Enable channel 1 Enable channel 2 Disable channel 3 Disable channel 4 Disable channel 5 Enable channel 6 Disable channel 1 Enable channel 6 Disable channel 1 Enable channel 6 Disable ch				
			Disabled	0	Value			
			Enabled	1				
Q	RW	CH16		Value Disable channel Enable or disable channel Enable channel Enable channel Enable channel Enable or disable channel 15 O Disable channel Enable or disable channel 16 Disable channel Enable or disable channel 17 O Disable channel Enable or disable channel 17 D Disable channel Enable or disable channel 18 Disable channel Enable or disable channel 19 Disable channel Enable or disable channel 20 Disable channel Enable or disable channel 20 Disable channel Enable or disable channel 21 Disable channel Enable or disable channel 22 Disable channel Enable or disable channel 23 Disable channel Enable or disable channel 24 Disable channel Enable or disable channel 24 Disable channel Enable or disable channel 25				
				Value Description 0 Disable channel 1 Enable channel 6 Disable channel 1 Enable or disable channel 1 Enable channel Enable or disable channel Enable channel 1 Enable channel 1 Enable or disable channel 10 0 Disable channel 1 Enable or disable channel 11 0 Disable channel 1 Enable or disable channel 12 0 Disable channel 1 Enable or disable channel 12 0 Disable channel 1 Enable or disable channel 13 0 Disable channel 1 Enable or disable channel 14 0 Disable channel 1 Enable or disable channel 15 0 Disable channel 1 Enable or disable channel 15 0 Disable channel 1 Enable or disable channel 16 0 Disable channel 1 Enable or d				
			Enabled	1				
R	RW	CH17		Value Description 0 Disable channel 1 Enable condisable channel 0 Disable channel 1 Enable condisable channel 1 Enable condisable channel 1 Enable condisable channel 2 Disable channel 3 Enable condisable channel 4 Enable condisable channel 5 Enable condisable channel 6 Disable channel 1 Enable condisable channel				
			Enabled	1				
S	RW	CH18		_				
_			Enabled	1				
Т	RW	CH19	S. 11.1					
	DVA	CU20	Enabled	1				
U	KVV	CH20	Disabled	Enable or disable channel 16 Disable channel Enable channel Enable or disable channel 17 Died 0 Disable channel Enable or disable channel 18 Died 1 Enable channel Enable or disable channel 18 Died 0 Disable channel Enable channel Enable or disable channel Enable or disable channel 19 Died 0 Disable channel Enable or disable channel Enable or disable channel 20 Died 0 Disable channel Enable or disable channel Enable channel Enable channel				
				Enable or disable channel 17 ed 0 Disable channel ed 1 Enable channel Enable or disable channel 18 ed 0 Disable channel ed 1 Enable channel Enable or disable channel Enable or disable channel 19 ed 0 Disable channel ed 1 Enable or disable channel Enable or disable channel Enable or disable channel Enable or disable channel 20 Disable channel				
.,	DVA	CU24	Enabled	1				
V	KW	CH21	Disabled	Enable or disable channel 12 0 Disable channel 1 Enable or disable channel 13 0 Disable channel 1 Enable or disable channel 14 0 Disable channel 1 Enable or disable channel 14 0 Disable channel 1 Enable or disable channel 15 0 Disable channel 1 Enable or disable channel 15 0 Disable channel 1 Enable or disable channel 16 0 Disable channel 1 Enable or disable channel 17 0 Disable channel 1 Enable or disable channel 17 0 Disable channel 1 Enable or disable channel 18 0 Disable channel 1 Enable or disable channel 18 0 Disable channel 1 Enable or disable channel 18 0 Disable channel 1 Enable or disable channel 19 0 Disable channel 1 Enable or disable channel 19 0 Disable channel 1 Enable or disable channel 20 0 Disable channel 1 Enable or disable channel 20 0 Disable channel 1 Enable or disable channel 21 0 Disable channel 1 Enable or disable channel 21 0 Disable channel 1 Enable or disable channel 21 0 Disable channel 1 Enable or disable channel 22 0 Disable channel 1 Enable or disable channel 23 0 Disable channel 1 Enable or disable channel 23 0 Disable channel 1 Enable or disable channel 24 0 Disable channel Enable or disable channel 24 0 Disable channel Enable or disable channel 24 0 Disable channel Enable or disable channel 24				
	DIA	CU22	Enabled	1				
W	ĸW	CH22	Disabled	0				
v	DV	CH22	Enabled	1				
Х	KW	CH23	Disabled	0				
.,	F	CUDA	Enabled	1				
Υ	кW	CH24	8:-11-1					
			Disabled	Enable or disable channel Enable channel Enable or disable channel Enabl				
				Disable channel				
			Enabled	1				
Z	RW	CH25	Enabled Disabled					Enable or disable channel 25



Bitı	number			31 30	29 28	27 20	5 25 2	24 2	3 22 2	21 2	20 19	9 18	3 17	16	15	14 1	3 12	11	10	9 8	3 7	6	5	4 3	2	1	0
Id				f e	d c	b a	Z	Υ)	x w	V	U T	S	R	Q	Р	0 N	I M	L	K	J	ΙН	G	F	Е [) С	В	Α
Res	et 0x000	000000		0 0	0 0	0 0	0	0 (0 0	0	0 0	0	0	0	0	0 0	0	0	0	0 (0 0	0	0	0 (0	0	0
Id	RW F	Field	Value Id	Value				D	escrip	otio	n																
			Enabled	1				Ε	nable	cha	annel	I															
а	RW C	CH26						Ε	nable	or (disab	ole (chan	nel	26												
			Disabled	0				D	Disable	ch	anne	el															
			Enabled	1				Е	nable	cha	annel	I															
b	RW C	CH27						Е	nable	or (disab	ole (chan	nel	27												
			Disabled	0				D	Disable	ch	anne	el															
			Enabled	1				Ε	nable	cha	annel	I															
С	RW C	CH28						Ε	nable	or (disab	ole (han	nel	28												
			Disabled	0				D	Disable	ch	anne	el															
			Enabled	1				Ε	nable	cha	annel	I															
d	RW C	CH29						Ε	nable	or (disab	ole (chan	nel	29												
			Disabled	0				D	Disable	ch	anne	el															
			Enabled	1				Ε	nable	cha	annel	I															
е	RW C	CH30						Ε	nable	or	disab	ole (han	nel	30												
			Disabled	0				D	Disable	ch	anne	el															
			Enabled	1				Е	nable	cha	annel	I															
f	RW C	CH31						Е	nable	or (disab	ole (han	nel	31												
			Disabled	0				D	isable	ch	anne	el															
			Enabled	1				Е	nable	cha	annel	I															

22.2.2 CHENSET

Address offset: 0x504

Channel enable set register

Read: reads value of CH{i} field in CHEN register.

BILL	numbe	er		31 3	30 2	9 28	27	26	25 2	4 2	23 22	21	20 1	9 1	8 17	16	15	14	13	12 1	11 1	0 9	8	7	6	5 -	4 3	2	1 0
Id				f	e d	d c	b	а	ΖY	/ :	x w	V	U -	Г :	S R	Q	Р	О	N	М	L k	(J	1	н	G	F	E D	С	ВА
Res	et 0x0	0000000		0	0 (0 0	0	0	0 () (0 0	0	0 (0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0 0
Id	RW	Field	Value Id	Valu	ıe					0	Desci	iptio	on																
Α	RW	CH0								C	Chan	nel C) ena	ble	set	regi	ster	. W	ritir	ng '0	' ha	s no	effe	ct					
			Disabled	0						F	Read	cha	nnel	dis	able	d													
			Enabled	1						F	Read	cha	nnel	en	able	d													
			Set	1						٧	Vrite	: En	able	cha	nne	I													
В	RW	CH1								C	Chan	nel 1	ena	ble	set	regi	ster	. W	ritir	ng '0	ha:	s no	effe	ct					
			Disabled	0						F	Read	cha	nnel	dis	able	d													
			Enabled	1						F	Read	cha	nnel	en	able	d													
			Set	1						٧	Vrite	: En	able	cha	nne	I													
С	RW	CH2								C	Chan	nel 2	ena	ble	set	regi	ster	. W	ritir	ng '0	ha:	s no	effe	ct					
			Disabled	0						F	Read	cha	nnel	dis	able	d													
			Enabled	1						F	Read	cha	nnel	en	able	d													
			Set	1						٧	Vrite	: En	able	cha	nne	I													
D	RW	CH3								C	Chan	nel 3	ena	ble	set	regi	ster	. W	ritir	ng '0	' ha	s no	effe	ct					
			Disabled	0						F	Read	cha	nnel	dis	able	d													
			Enabled	1						F	Read	cha	nnel	en	able	d													
			Set	1						٧	Vrite	: En	able	cha	nne	I													
Ε	RW	CH4								C	Chan	nel 4	l ena	ble	set	regi	ster	. W	ritir	ng '0	ha:	s no	effe	ct					
			Disabled	0						F	Read	cha	nnel	dis	able	d													
			Enabled	1						F	Read	cha	nnel	en	able	d													
			Set	1						٧	Vrite	: En	able	cha	nne	I													
F	RW	CH5								C	Chan	nel 5	ena	ble	set	regi	ster	. W	ritir	ng '0	ha:	s no	effe	ct					
			Disabled	0						F	Read	cha	nnel	dis	able	d													
			Enabled	1						F	Read	cha	nnel	en	able	d													
			Set	1						٧	Vrite	: En	able	cha	nne	I													



Bitı	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	set 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
G	RW CH6		Channel 6 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Н	RW CH7	S. 11.1	Channel 7 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
	DIM CHO	Set	1 Write: Enable channel
I	RW CH8	Disabled	Channel 8 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
	DW CHO	Set	1 Write: Enable channel
J	RW CH9	Disabled	Channel 9 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
	DW CHIO	Set	1 Write: Enable channel
K	RW CH10	Disabled	Channel 10 enable set register. Writing '0' has no effect O Read: channel disabled
		Disabled	
		Enabled	1 Read: channel enabled 1 Write: Enable channel
L	RW CH11	Set	
_	KW CHII	Disabled	Channel 11 enable set register. Writing '0' has no effect O Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
М	RW CH12	Set	Channel 12 enable set register. Writing '0' has no effect
IVI	NVV CITIZ	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
N	RW CH13	Jei	Channel 13 enable set register. Writing '0' has no effect
	NW CHIS	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
0	RW CH14	300	Channel 14 enable set register. Writing '0' has no effect
•	NW CHIT	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Р	RW CH15	300	Channel 15 enable set register. Writing '0' has no effect
•	6.125	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Q	RW CH16		Channel 16 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
R	RW CH17		Channel 17 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
S	RW CH18		Channel 18 enable set register. Writing '0' has no effect
-		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Т	RW CH19	JCC	Channel 19 enable set register. Writing '0' has no effect
'	WAA CLITA	Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Lilabica	1 Nead. Charmer Chabled



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCB
Rese	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		Set	1 Write: Enable channel
U	RW CH20		Channel 20 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
٧	RW CH21		Channel 21 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
W	RW CH22		Channel 22 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Χ	RW CH23		Channel 23 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Υ	RW CH24		Channel 24 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
Z	RW CH25		Channel 25 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
а	RW CH26		Channel 26 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
b	RW CH27		Channel 27 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
C	RW CH28		Channel 28 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
d	RW CH29		Channel 29 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
е	RW CH30		Channel 30 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel
f	RW CH31		Channel 31 enable set register. Writing '0' has no effect
		Disabled	0 Read: channel disabled
		Enabled	1 Read: channel enabled
		Set	1 Write: Enable channel

22.2.3 CHENCLR

Address offset: 0x508

Channel enable clear register



Read: reads value of CH(i) field in CHEN register.

Bit r	numbe	er		31 30	29 2	8 27	7 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 (0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
Α	RW	CH0							Channel 0 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
В	RW	CH1							Channel 1 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
С	RW	CH2							Channel 2 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
D	RW	CH3							Channel 3 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
E	R\M/	CH4	Cicui	•					Channel 4 enable clear register. Writing '0' has no effect
-	11.00	CH	Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
									Write: disable channel
_	D\A/	CHE	Clear	1					
F	KVV	CH5	Disabled	0					Channel 5 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
G	RW	CH6		_					Channel 6 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
Н	RW	CH7							Channel 7 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
I	RW	CH8							Channel 8 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
J	RW	CH9							Channel 9 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
K	RW	CH10							Channel 10 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
L	RW	CH11							Channel 11 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
N/A	D\A/	CH12	Cicai	1					
М	rvv	CH12	Disabled	0					Channel 12 enable clear register. Writing '0' has no effect
			Disabled	0					Read: channel disabled
			Enabled	1					Read: channel enabled
			Clear	1					Write: disable channel
N	RW	CH13							Channel 13 enable clear register. Writing '0' has no effect



Bit r	numbe	er		31 30	29 28	27 26	5 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	ΖY	X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
0	RW	CH14						Channel 14 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Р	RW	CH15						Channel 15 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Q	RW	CH16						Channel 16 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
R	RW	CH17						Channel 17 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
S	RW	CH18						Channel 18 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Т	RW	CH19		_				Channel 19 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
	DIA	CU20	Clear	1				Write: disable channel
U	RW	CH20	D' III I	•				Channel 20 enable clear register. Writing '0' has no effect
			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
V	D\A/	CH21	Clear	1				Write: disable channel Channel 21 enable clear register. Writing '0' has no effect
V	KVV	CHZI	Disabled	0				Read: channel disabled
			Disabled Enabled	0				
			Clear	1				Read: channel enabled Write: disable channel
W	R\M/	CH22	Cicai	1				Channel 22 enable clear register. Writing '0' has no effect
vv	IVVV	CHZZ	Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Х	RW	CH23	Cicui	-				Channel 23 enable clear register. Writing '0' has no effect
^		C1123	Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Υ	R\M	CH24	oleu.	-				Channel 24 enable clear register. Writing '0' has no effect
•			Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
Z	RW	CH25	2.50	-				Channel 25 enable clear register. Writing '0' has no effect
		<u>-</u> 5	Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
а	R/M/	CH26	e.eui	-				Channel 26 enable clear register. Writing '0' has no effect
u		J. 120	Disabled	0				Read: channel disabled
			Enabled	1				Read: channel enabled
			Clear	1				Write: disable channel
			Cical	1				WITEC. GISADIC CHAINCI



Bit nun	nber		31 30	29 2	8 27	26	25 24	1 23	3 22 2	21 2	20 19	18	17	16	15 1	4 13	12	11 1	0 9	8	7	6	5	4 3	2	1	0
Id			f e	d d	c b	а	Z Y	Χ	W '	Vι	U T	S	R	Q	Р (O N	М	L	〈 J	-1	Н	G	F	ΕС	С	В	Α
Reset 0)x00000000		0 0	0 0	0 0	0	0 0	0	0	0 (0 0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0
Id R	W Field	Value Id	Value					De	escrip	tio	n																
b R	W CH27							Ch	nanne	el 27	7 ena	ble	clea	ır re	gist	er. W	/ritir	ıg '0	has	no	effe	ct					
		Disabled	0					Re	ad: c	han	nel	disa	bled														
		Enabled	1					Re	ad: c	han	nel e	enal	bled														
		Clear	1					W	rite: o	disa	ble o	har	nnel														
c R	W CH28							Ch	nanne	1 28	3 ena	ble	clea	ır re	gist	er. V	/ritir	ıg '0	has	no	effe	ct					
		Disabled	0					Re	ad: c	han	nel	disa	bled														
		Enabled	1					Re	ad: c	han	nel e	enal	bled														
		Clear	1					W	rite: o	disa	ble o	har	nnel														
d R	W CH29							Ch	nanne	1 29	ena	ble	clea	ır re	gist	er. W	/ritir	ıg '0	has	no	effe	ct					
		Disabled	0					Re	ad: c	han	nel	disa	bled	l													
		Enabled	1					Re	ad: c	han	nel	enal	bled														
		Clear	1					W	rite: o	disa	ble o	har	nel														
e R	W CH30							Ch	nanne	130) ena	ble	clea	ır re	gist	er. W	/ritir	ıg '0	has	no	effe	ct					
		Disabled	0					Re	ad: c	han	nel	disa	bled														
		Enabled	1					Re	ad: c	han	nel e	enal	bled														
		Clear	1					W	rite: o	disa	ble o	har	nel														
f R	W CH31							Ch	nanne	l 31	l ena	ble	clea	ır re	gist	er. W	/ritir	ıg '0	has	no	effe	ct					
		Disabled	0					Re	ad: c	han	nel	disa	bled														
		Enabled	1					Re	ad: c	han	nel	enal	bled														
		Clear	1					W	rite: d	disa	ble o	har	nel														
f R	W CH31	Disabled Enabled	0					Ch Re	nanne ead: c ead: c	l 31 han han	L ena	ible disa enal	clea blea bled	l	gist	er. W	/ritir	ıg '0	' has	s no	effe	ct					

22.2.4 CH[0].EEP

Address offset: 0x510

Channel 0 event end-point

Bit ı	numbe	er	:	31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	16	15	14	13	12 :	11 1	0 9	9 8	3 7	6	5	4	3	2	1 ()
Id			,	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	A A	Α	Α	Α	Α	Α	A A	Δ Α	Α Α	Δ Δ	A	Α	Α	Α /	Δ.	A A	A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 () () (0	0	0	0	0 (0	0 ()
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0																													
Α	RW	EEP		Pointer to event register. Accepts only addresses to registers												_																	

from the Event group.

22.2.5 CH[0].TEP

Address offset: 0x514 Channel 0 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20	19 1	18 2	17 :	16 :	15 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	ı
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	ı
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	ı
Id	RW	Field	Value Id	0 0 0 0 0 0 0 0 Value											n																				l
Α	RW	TEP		Pointer to task register. Accepts only addresses to registers												1																			

from the Task group.

22.2.6 CH[1].EEP

Address offset: 0x518 Channel 1 event end-point



Bit r	umber		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A A A A A A A A A A A A
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Α	RW EEP		Pointer to event register. Accepts only addresses to registers
			from the Event group.

22.2.7 CH[1].TEP

Address offset: 0x51C Channel 1 task end-point

Bit r	iumbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 1	18 1	7 1	.6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α /	Δ ,	Δ /	Α Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ Α	A A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egist	er.	Acc	ept	s or	ıly a	ddr	ess	es t	o re	egis	ters	5				
												fro	m tl	he 1	Task	gro	oup.																

22.2.8 CH[2].EEP

Address offset: 0x520

Channel 2 event end-point

Bit	numbe	er		31	1 30	29	28	3 2	7 26	25	24	23	22	21	20	19	18	17	16 1	15 :	14 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	. A	. 4	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ Α	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α .	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0) (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptio	on																		
Α	RW	EEP										Ро	inte	r to	ev	ent	reg	iste	er. A	Acce	pts	onl	y ac	ddre	sse	s to	reg	giste	ers				
												fro	m t	he I	Eve	nt g	grou	ıp.															

22.2.9 CH[2].TEP

Address offset: 0x524 Channel 2 task end-point

Bit r	iumbe	er		3:	1 30	29	28	8 2	7 2	6 2	25 2	24 2	23 :	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id				Α	Α	Α	. 4	\ <i>A</i>	۸ ۸	Δ.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	4 А
Res	et OxC	0000000		0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	V	alue	•						ı	Des	crip	otic	n																			
Α	RW	TEP										F	Poir	nter	r to	tas	k re	egis	ter	. Ac	cep	ots	onl	y ad	ldre	sse	s to	o re	gis	ters					
												f	fror	n th	ne 1	asl	gr	oup).																

22.2.10 CH[3].EEP

Address offset: 0x528

Channel 3 event end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value Description
A RW EEP		Pointer to event register. Accepts only addresses to registers

from the Event group.

22.2.11 CH[3].TEP

Address offset: 0x52C Channel 3 task end-point



Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19 :	18 :	17 1	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	A A	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	А
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egis	ter.	Aco	cept	10 2	nly a	ddr	esse	es t	o re	gis	ters	;				
												fro	m tl	he 1	Tasl	c gr	oup																

22.2.12 CH[4].EEP

Address offset: 0x530

Channel 4 event end-point

Bitı	number		31	30	29	28	27	7 26	25	24	23	22	21	20 1	19	18 1	.7 :	16 1	15 :	14	13	12 :	11 :	10	9	8	7	6	5	4	3	2	1 0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ.	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Δ,	4 А
Res	et 0x00000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	
1.1											_																						
Ia	RW Field	Value Id	Va	llue							Des	scri	otic	n																			
A	RW Field RW EEP								ent	regi	ste	r. A	Acce	ept	s or	ıly a	dd	res	ses	to	reg	iste	ers										

22.2.13 CH[4].TEP

Address offset: 0x534 Channel 4 task end-point

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 18	8 17	16	15	14	13	12 1	11 1	.0 9	9 8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		A	Α	Α	Α	Α	Α.	Α ,	Α Α	A A	A	Α	Α	Α	Α	A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	RW	TEP										Poi	ntei	r to	task	reg	giste	r. A	cce	pts	only	ad a	dre	sses	to	regi	ster	'S				
														-	ask																	

22.2.14 CH[5].EEP

Address offset: 0x538

Channel 5 event end-point

Bit r	numb	er		3:	1 30	29	28	3 2	7 26	25	5 24	23	22	21 2	20 1	9 1	8 17	7 16	15	14	13	12 1	1 1	0 9	8 (7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	. 4	A	Α	Α	Α	Α	Α	A A	Δ Δ	A	Α	Α	Α	Α	A	A A	Α Δ	. Δ	A	. A	A	Α	Α	Α	А А
Res	et Ox(00000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	•						De	scri	ptio	n																	
Α	RW/	EEP										Poi	inte	r to	eve	nt r	egis	ter.	Acc	ept	s or	ılv a	ddr	esse	es to	o re	gist	ers				
																	-0					, .					_					

22.2.15 CH[5].TEP

Address offset: 0x53C Channel 5 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 1	16	15 :	14	13	12	11 1	0 9	9 8	7	6	5	4	3	2	1	C
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α Α	A A	A	Α	Α	Α	Α	Α	A	Δ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	D
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Poi	nte	r to	tas	k re	egis	ter.	Ac	сер	ts	only	ad	dre	sses	to	regi	ste	rs					

from the Task group.

22.2.16 CH[6].EEP

Address offset: 0x540

Channel 6 event end-point



Bit r	umb	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 1	.9 1	8 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	4 A	Α	Α	Α	Α	A .	Δ Δ	Α	Α	Α	Α	Α	Α	Α .	Δ ,	A A
Res	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																	
Α	RW	EEP										Poi	nte	r to	eve	nt r	egis	ter.	Acc	ept	s or	ly a	ddre	sse	s to	reg	iste	ers				
												fro	m tl	he E	ven	t gr	oup															

22.2.17 CH[6].TEP

Address offset: 0x544 Channel 6 task end-point

D.:				24	20	. 20			7 20		·	4 2		2 2	4 2	0.11			10	4.5	4.4	42	4.2	4.4	10	^	^	7	_	_		2	2	4	0
BIT	numbe	er		31	. 30	25) ZE	3 2	/ 26	5 2:	5 24	4 2	23 2	2 2	1 2	0 19) TS	3 1/	16	15	14	13	12	11	10	9	8	/	6	5	4	3	2	1	U
Id				Α	Α	Α	. A		A A	. 4	Д Д	۱ ۸	Δ ,	4 4	۱ ۸	4 A	Α	А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et Ox0	0000000		0	0	0	0	C	0	0	0 0) (0 (0 () (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							D	eso	rip	tio	n																			
Α	RW	TEP										Р	oin	ter	to '	task	reg	iste	r. A	cce	pts	onl	y ac	ldre	esse	es to	o re	egis	ter	s					
												fı	rom	the	е Та	ask g	grou	up.																	

22.2.18 CH[7].EEP

Address offset: 0x548

Channel 7 event end-point

Bitı	numbe	er		31	1 30) 29	9 28	3 2	7 26	5 25	24	23	22	21	20	19 :	18 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3	2 1	L 0
Id				Α	Α	Α	A	. 4	A A	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	4 <i>A</i>	A A
Res	et OxO	0000000		0	0	0	0	C	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																		
Α	RW	EEP										Ро	inte	r to	eve	ent	regi	ster	. Ac	сер	ts o	nly	add	res	ses	to	reg	iste	rs				
												fro	m t	he I	Evei	nt g	roup	ο.															

22.2.19 CH[7].TEP

Address offset: 0x54C Channel 7 task end-point

Bitı	numbe	er		33	1 30	29	28	8 2	7 26	5 25	5 24	4 23	3 22	21	20	19	18	17	16	15 1	L4 1	.3 1	2 1:	l 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	. A	\ A	A A	. A	A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α /	A	Α	Α	Α	Α	Α	Α	Α	Α ,	4 /	A A
Res	et 0x0	0000000		0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	V	alue	•						D	escr	ipti	on																		
Α	RW	TEP										Po	ointe	er to	tas	sk re	egis	ter.	Ac	сер	ts c	nly	add	ress	es t	o r	egis	ter	S				

22.2.20 CH[8].EEP

Address offset: 0x550

Channel 8 event end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW EEP		Pointer to event register. Accepts only addresses to registers

from the Event group.

22.2.21 CH[8].TEP

Address offset: 0x554 Channel 8 task end-point



Bit r	nur	nbe	r		31	30	29	28	27	7 26	25	24	23	22	21	20 1	.9 1	8 17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id					Α	Α	Α	Α	А	Α	Α	Α	Α	Α	Α	Α.	Δ ,	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A
Res	et (0x0(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0 0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	R	W	TEP										Poi	inte	r to	tas	k re	giste	er. A	Acce	pts	onl	y ac	ldre	sse	es to	o re	gist	ters					
													fro	m tl	he 1	ask	gro	up.																

22.2.22 CH[9].EEP

Address offset: 0x558

Channel 9 event end-point

Bitı	numb	er		31	30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 2	1 0
Id				А	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ A	A A
Res	et 0x	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	EEP										Poi	nter	to	even	t re	gist	er.	Acc	ept	s or	ıly a	add	res	ses	to	reg	iste	rs				
												froi	n th	e E	vent	gro	up.																

22.2.23 CH[9].TEP

Address offset: 0x55C Channel 9 task end-point

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	.8 1	7 1	6 15	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ,	4 Δ		\ A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
Α	RW	TEP										Poi	ntei	r to	tas	k re	gist	er.	Acc	ept	on	ly a	ddr	ess	es t	o re	gis	ters	5				
														_			up.																

22.2.24 CH[10].EEP

Address offset: 0x560

Channel 10 event end-point

Bit r	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16 1	15 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A А	Α	Α	Α .	A A	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	D\A/	Field	Value Id	Va	lue							Des	crip	tio	,																	
	IVVV	rieiu	value la									-	,cp	,	•																	
Α		EEP	variac la										•		• even	t reg	giste	er. A	cce	pts (only	add	ress	es	to r	regi	iste	ers				

22.2.25 CH[10].TEP

Address offset: 0x564

Channel 10 task end-point

Bit	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20 1	L9 1	8 1	7 1	.6 1	.5 1	4 1	13 1	12	11 1	0	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 /	Δ ,	Δ ,	Δ	A.	Α	A	Δ.	Α	Α	Α	Α	Α	Α	Α .	Α.	A A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0 (0	0	0	0)	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	lue							De	cri	otic	n																				ı
Α	RW	TEP										Poi	nte	r to	tas	k re	gist	er.	Acc	ept	ts c	nly	ad	dre	sse	s to	re	gist	ters						١

from the Task group.

22.2.26 CH[11].EEP

Address offset: 0x568

Channel 11 event end-point



Bit r	umb	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 1	.9 1	8 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	4 A	Α	Α	Α	Α	A .	Δ Δ	Α	Α	Α	Α	Α	Α	Α .	Δ ,	A A
Res	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																	
Α	RW	EEP										Poi	nte	r to	eve	nt r	egis	ter.	Acc	ept	s or	ly a	ddre	sse	s to	reg	iste	ers				
												fro	m tl	he E	ven	t gr	oup															

22.2.27 CH[11].TEP

Address offset: 0x56C

Channel 11 task end-point

Bit r	iumbe	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	18 1	7 1	.6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ ,	Δ /	Α Α	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							Des	scri	ptio	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	gist	er.	Acc	ept	10 2:	nly a	ddr	ess	es t	o re	gis	ters	;				
												froi	m tl	he T	Task	gro	oup.																

22.2.28 CH[12].EEP

Address offset: 0x570

Channel 12 event end-point

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 1	.9 1	8 1	7 1	5 15	14	13	12	11 3	10	9	8	7	6 5	5 4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ,	A A	Α Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Α,	Α Α	4 Δ	A	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 (0	0 (0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																		
Α	RW	EEP										Poi	ntei	r to	eve	nt i	regis	ter	. Ac	cept	S OI	nly a	addı	ress	es	to r	egis	ter	s				
												fro	m th	ne F	ven	tσι	nur	,															

22.2.29 CH[12].TEP

Address offset: 0x574

Channel 12 task end-point

Bit r	umbe	r		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	' 16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Δ.	А А
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R\//	TEP										Poi	nter	to	task	res	iste	r. A	cce	nts	onl	v ad	dre	sse	s to	o re	gis	ters	5				
	1100	101															,					,					_						

22.2.30 CH[13].EEP

Address offset: 0x578

Channel 13 event end-point

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW EEP	Pointer to event register. Accepts only addresses to registers

from the Event group.

22.2.31 CH[13].TEP

Address offset: 0x57C

Channel 13 task end-point



Bit r	num	ber			31	30	29	28	27	7 26	5 2	5 24	4 2	3 2	2 2:	L 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id					Α	Α	Α	Α	А	A	A	Α	. /	A A	A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α ,	А А
Res	et Ox	x00	000000		0	0	0	0	0	0	C	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RV	N	Field	Value Id	Va	lue	:						C	esc	ript	ion																			
Α	RV	V ·	TEP										Р	oin	ter 1	o t	skı	regi	ste	r. A	cce	pts	onl	y a	ddr	esse	es t	o re	gis	ters	s				
													f	rom	the	Та	sk g	rou	p.																

22.2.32 CH[14].EEP

Address offset: 0x580

Channel 14 event end-point

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16 1	15 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A A	Α	Α	Α .	A A	Α Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	4 Α	А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tion																		
		Ticiu		-								-	,cp	,	•																	
Α	RW	EEP	74.40.14												• even	t re	giste	er. A	ссе	pts (only	add	ress	ses	to r	regi	iste	ers				

22.2.33 CH[14].TEP

Address offset: 0x584

Channel 14 task end-point

Bit r	numb	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 1	9 1	8 17	7 16	15	14	13	12	11 :	.0	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ ,	4 A	Α	Α	Α	Α	Α	Α	Δ.	Α	Α	Α	Α	Α	Α	ΑА	. 4	A A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scrip	otio	n																		
Α	RW	TEP										Poi	ntei	r to	tasl	k re	giste	er. A	ссе	pts	onl	y ad	ldre	sse	s to	re	gist	ers					
												fro	m th	ne T	ask	gro	up.																

22.2.34 CH[15].EEP

Address offset: 0x588

Channel 15 event end-point

Bit r	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16 1	15 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A А	Α	Α	Α .	A A	Α Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	D\A/	Field	Value Id	Va	lue							Des	crip	tio	,																	
	IVVV	rieiu	value la									-	,cp	,	•																	
Α		EEP	variac la										•		• even	t reg	giste	er. A	cce	pts (only	add	ress	es	to r	regi	iste	ers				

22.2.35 CH[15].TEP

Address offset: 0x58C

Channel 15 task end-point

Bit	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20 1	L9 1	8 1	7 1	.6 1	.5 1	4 1	13 1	12	11 1	0	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 /	Δ ,	Δ ,	Δ	A.	Α	A	Δ.	Α	Α	Α	Α	Α	Α	Α .	Α.	A A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0 (0	0	0	0)	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	lue							De	cri	otic	n																				ı
Α	RW	TEP										Poi	nte	r to	tas	k re	gist	er.	Acc	ept	ts c	nly	ad	dre	sse	s to	re	gist	ters						١

from the Task group.

22.2.36 CH[16].EEP

Address offset: 0x590

Channel 16 event end-point



Bit r	umb	er		31	. 30	29	28	27	26	25	24	23	22	21 :	20 1	.9 1	8 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	4 A	Α	Α	Α	Α	A .	Δ Δ	Α	Α	Α	Α	Α	Α	Α .	Δ ,	A A
Res	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptio	n																	
Α	RW	EEP										Poi	nte	r to	eve	nt r	egis	ter.	Acc	ept	s or	ly a	ddre	sse	s to	reg	iste	ers				
												fro	m tl	he E	ven	t gr	oup															

22.2.37 CH[16].TEP

Address offset: 0x594

Channel 16 task end-point

Bit r	nur	nbe	r		31	30	29	28	27	7 26	25	24	23	22	21	20 1	.9 1	8 17	7 16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id					Α	Α	Α	Α	А	Α	Α	Α	Α	Α	Α	Α.	Δ ,	4 A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A
Res	et (0x0(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0 0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	R	W	TEP										Poi	inte	r to	tas	k re	giste	er. A	Acce	pts	onl	y ac	ldre	sse	es to	o re	gist	ters					
													fro	m tl	he 1	ask	gro	up.																

22.2.38 CH[17].EEP

Address offset: 0x598

Channel 17 event end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	.8 1	7 16	15	14	13	12	11 1	0 9	9 8	3 7	6	5	4	3	2	1 0	l
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α	A A	۸ ۸	4 А	. A	Α	Α	Α	Α	A	Δ Α	A /	A	A	A	Α	Α	Α	A A	ı
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0 () (0 0	0	0	0	0	0	0) () (0	0	0	0	0	0	0 0	l
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		l
Α	RW	EEP										Poi	nter	to	eve	nt r	egis	ter.	Acc	ept	s or	nly a	ddr	ess	es t	o re	gist	ers					
												froi	n th	e F	ven	t ør	้ดนถ																

22.2.39 CH[17].TEP

Address offset: 0x59C

Channel 17 task end-point

Bit r	umbe	er		31	1 30	29	28	27	7 26	25	24	23	22	21 2	20 1	9 1	8 17	7 16	15	14	13	12 1	1 1	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α.	A A	Δ Δ	A	Α	Α	Α	Α	Α.	A A	A	. A	Α	Α	Α	Α	Α	Α.	А А
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scrip	otio	n																	
Α	D\A/	TEP										Poi	intei	r to	task	res	iste	r. A	cce	nts	only	/ ad	dres	ses	to i	egi	ster	·s				
	1100	1-1															5.000				,					- 0						

22.2.40 CH[18].EEP

Address offset: 0x5A0

Channel 18 event end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW EEP		Pointer to event register. Accepts only addresses to registers

from the Event group.

22.2.41 CH[18].TEP

Address offset: 0x5A4 Channel 18 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW TEP	Pointer to task register. Accepts only addresses to registers

22.2.42 CH[19].EEP

Address offset: 0x5A8

Channel 19 event end-point

Bit n	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																			
Α	RW	EEP										Ро	inte	er to	o ev	/ent	re	gist	er.	Acc	ept	S O	nly	ado	dres	ses	to	reg	iste	ers				

Pointer to event register. Accepts only addresses to registe

from the Event group.

from the Task group.

22.2.43 CH[19].TEP

Address offset: 0x5AC Channel 19 task end-point

Bit r	iumbe	er		31	. 30	29	28	27	7 26	25	24	23	22	21	20	19	18 :	17 1	16 1	15 1	14 :	13 :	12 1	11 :	LO	9	8	7	6	5 -	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Α.	Α	Α	Α.	Д	Α.	Α	Α	Α	Α	A .	Α	A A	A A	A A
Res	et OxO	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	gis	ter.	Ac	сер	ts c	nly	ad	dre	sse	s to	re	gist	ers					
																	guc																	

22.2.44 CHG[0]

Address offset: 0x800 Channel group 0

Dia -	numbe			21.2	0 20	9 28 2	77.20	2 2 5	- 24	22	22.2	1 20	2 10	10	17 .	10	1 - 1	4 1.	112	11	0	9 8	7	6	5	4	3 2	1	0
	iumbe	:1																				9 0			Ŭ		_	1	Ŭ
Id				f e	e d	С	b a	Z	Υ	Х	W۱	V U	T	S	R	Q	PC) N	M	L	Κ.	JI	Н	G	F	E) C	В	Α
Res	et 0x0	0000000		0 (0 0	0	0 0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0 (0 0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Valu	ie					De	scrip	tion	ı																
Α	RW	CH0								Inc	lude	or e	xclu	ıde	chan	nel	0												
			Excluded	0						Exc	clude																		
			Included	1						Inc	lude																		
В	RW	CH1								Inc	lude	or e	xclu	ıde	chan	nel	1												
			Excluded	0						Exc	clude																		
			Included	1						Inc	lude																		
С	RW	CH2								Inc	lude	or e	xclu	ıde	chan	nel	2												
			Excluded	0						Exc	clude																		
			Included	1						Inc	lude																		
D	RW	CH3								Inc	lude	or e	xclu	ıde	chan	nel	3												
			Excluded	0						Exc	clude																		
			Included	1						Inc	lude																		
E	RW	CH4								Inc	lude	or e	xclu	ıde	chan	nel	4												
			Excluded	0						Exc	clude																		
			Included	1						Inc	lude																		
F	RW	CH5								Inc	lude	or e	xclu	ıde	chan	nel	5												
			Excluded	0						Exc	clude																		
			Included	1						Inc	lude																		
G	RW	CH6								Inc	lude	or e	xclu	ıde	chan	nel	6												



Bit n	umbe	er		31 30	29 28	27 2	26 25	24	22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6	5 5	4 3	2 1 0
Id									WVUTSRQPONMLKJI				
Rese	t Ox0	0000000		0 0	0 0	0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 (0 0	0 0	0 0 0
Id	RW	Field	Value Id	Value					scription				
			Excluded	0					clude				
			Included	1					lude				
Н	RW	CH7							clude or exclude channel 7				
			Excluded	0					clude				
	DIA	CUO	Included	1					clude				
ı	RW	CH8	Findings	0					clude or exclude channel 8				
			Excluded Included	0					clude clude				
J	RW	СН9	included	1					clude or exclude channel 9				
,			Excluded	0					clude				
			Included	1					clude				
K	RW	CH10							clude or exclude channel 10				
			Excluded	0					clude				
			Included	1					clude				
L	RW	CH11							clude or exclude channel 11				
			Excluded	0					clude				
			Included	1					clude				
М	RW	CH12							clude or exclude channel 12				
			Excluded	0					clude				
			Included	1					clude				
N	RW	CH13		_					clude or exclude channel 13				
			Excluded	0					clude				
0	D\A/	CH14	Included	1					clude clude or exclude channel 14				
U	KVV	Cn14	Excluded	0					clude				
			Included	1					clude				
Р	RW	CH15	meladed	-					clude or exclude channel 15				
			Excluded	0					clude				
			Included	1					clude				
Q	RW	CH16							clude or exclude channel 16				
			Excluded	0					clude				
			Included	1					clude				
R	RW	CH17							clude or exclude channel 17				
			Excluded	0					clude				
			Included	1					lude				
S	RW	CH18							clude or exclude channel 18				
			Excluded	0					clude				
т.	D\A/	CU10	Included	1					clude				
Т	KVV	CH19	Excluded	0					clude or exclude channel 19 Clude				
			Included	1					clude				
U	RW	CH20	meladed	-					clude or exclude channel 20				
_			Excluded	0					clude				
			Included	1					clude				
V	RW	CH21							clude or exclude channel 21				
			Excluded	0					clude				
			Included	1					clude				
W	RW	CH22							clude or exclude channel 22				
			Excluded	0					clude				
			Included	1					lude				
Х	RW	CH23							clude or exclude channel 23				
			Excluded	0					clude				
			Included	1					clude				
Υ	RW	CH24							clude or exclude channel 24				
			Excluded	0					clude				



Bitı	numbe	er		31	30 2	29 28	8 27	7 26	25 2	4 23	3 22	21	20 1	9 18	3 17	16	15	14 1	.3 1	2 11	10	9	8 7	6	5	4	3 2	1	0
Id				f	е	d c	b	а	ΖY	′ X	W	٧	U T	S	R	Q	Р	0	N N	1 L	K	J	ΙН	G	F	Ε	D C	В	Α
Res	et 0x0	0000000		0	0	0 0	0	0	0 (0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0 0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	ue					De	escri	ptic	n																
			Included	1						In	clude	e																	
Z	RW	CH25								In	clude	e or	excl	ude	cha	nne	el 25	5											
			Excluded	0						Ex	clud	e																	
			Included	1						In	clude	е																	
а	RW	CH26								In	clude	e or	excl	ude	cha	nne	el 26	5											
			Excluded	0						Ex	clud	e																	
			Included	1						In	clude	е																	
b	RW	CH27								In	clude	e or	excl	ude	cha	nne	el 27	,											
			Excluded	0						Ex	clud	e																	
			Included	1						In	clude	e																	
С	RW	CH28								In	clude	e or	excl	ude	cha	nne	el 28	3											
			Excluded	0						Ex	clud	e																	
			Included	1						In	clude	е																	
d	RW	CH29								In	clude	e or	excl	ude	cha	nne	29)											
			Excluded	0						Ex	clud	e																	
			Included	1						In	clude	е																	
е	RW	CH30								In	clude	e or	excl	ude	cha	nne	130)											
			Excluded	0						Ex	clud	e																	
			Included	1						In	clude	е																	
f	RW	CH31								In	clude	e or	excl	ude	cha	nne	el 31												
			Excluded	0						Ex	clud	e																	
			Included	1						In	clude	е																	

22.2.45 CHG[1]

Address offset: 0x804

Channel group 1

Bit	numbe	er		31	30	29	28	27 :	6.2	25.2	4 2	3	22 2	1.2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	3 13) 11	10	9	8	7	6	5	4 3	2	1	0
Id				f	e	d	С	b	а	ΖY	()	Χ	w v	/	U T		S F	2 (Q F	· ())	N N	1 L	K	J	ī	Н	G	F	E C	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0 () (0	0 0)	0 0) (0 0) () (. () (0 0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						C	Des	script	tio	n																		
Α	RW	CH0									li	ncl	lude	or	excl	ud	e ch	anı	nel	0													
			Excluded	0							Е	xc	lude																				
			Included	1							li	ncl	lude																				
В	RW	CH1									li	ncl	lude	or	excl	ud	e ch	anı	nel	1													
			Excluded	0							Е	xc	lude																				
			Included	1							h	ncl	lude																				
С	RW	CH2									li	ncl	lude	or	excl	ud	e ch	anı	nel	2													
			Excluded	0							Е	xc	lude																				
			Included	1							h	ncl	lude																				
D	RW	CH3									li	ncl	lude	or	excl	ud	e ch	anı	nel	3													
			Excluded	0							Е	xc	lude																				
			Included	1							li	ncl	lude																				
Ε	RW	CH4									li	ncl	lude	or	excl	ud	e ch	anı	nel	4													
			Excluded	0							Е	xc	lude																				
			Included	1							li	ncl	lude																				
F	RW	CH5									li	ncl	lude	or	excl	ud	e ch	anı	nel	5													
			Excluded	0							Е	xc	lude																				
			Included	1							li	ncl	lude																				
G	RW	CH6									li	ncl	lude	or	excl	ud	e ch	anı	nel	6													
			Excluded	0							Е	xc	lude																				
			Included	1							li	ncl	lude																				
Н	RW	CH7									h	ncl	lude	or	excl	ud	e ch	anı	nel	7													
			Excluded	0							E	xc	lude																				



Bit n	iumbe	er		31 30	29 2	28 27	' 26 2	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id				f e	d	c b	a i	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et OxO	0000000		0 0	0	0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			Included	1					Include
I	RW	CH8							Include or exclude channel 8
			Excluded	0					Exclude
			Included	1					Include
J	RW	CH9							Include or exclude channel 9
			Excluded	0					Exclude
			Included	1					Include
K	RW	CH10							Include or exclude channel 10
			Excluded	0					Exclude
			Included	1					Include
L	RW	CH11							Include or exclude channel 11
			Excluded	0					Exclude
			Included	1					Include
М	RW	CH12							Include or exclude channel 12
			Excluded	0					Exclude
			Included	1					Include
N	RW	CH13							Include or exclude channel 13
			Excluded	0					Exclude
			Included	1					Include
0	RW	CH14							Include or exclude channel 14
			Excluded	0					Exclude
			Included	1					Include
Р	RW	CH15							Include or exclude channel 15
			Excluded	0					Exclude
			Included	1					Include
Q	RW	CH16							Include or exclude channel 16
			Excluded	0					Exclude
_			Included	1					Include
R	RW	CH17		_					Include or exclude channel 17
			Excluded	0					Exclude
			Included	1					Include
S	RW	CH18							Include or exclude channel 18
			Excluded	0					Exclude
_		01140	Included	1					Include
Т	RW	CH19							Include or exclude channel 19
			Excluded	0					Exclude
	D	CU20	Included	1					Include
U	кW	CH20	Evaludad	0					Include or exclude channel 20
			Excluded	0					Exclude
V	DIA	CH21	Included	1					Include
V	KVV	CH21	Evaludad	0					Include or exclude channel 21
			Excluded	0					Exclude
١٨,	DIA	CH22	Included	1					Include
W	кW	CH22	Evoludad	0					Include or exclude channel 22
			Excluded	0					Exclude
v	DIA	CH33	Included	1					Include
X	KW	CH23	Evoluded	0					Include or exclude channel 23
			Excluded	0					Exclude
v	D	CUDA	Included	1					Include
Υ	кW	CH24							Include or exclude channel 24
			Excluded	0					Exclude
_			Included	1					Include
Z	RW	CH25							Include or exclude channel 25
			Excluded	0					Exclude
			Included	1					Include



Bit n	umbe	er		31	30	29	28 2	27 2	26 2	25 2	24 2	23	22	21 2	20 1	L9 1	8 1	7 16	5 15	14	13	12 1	11 10	9	8	7	6	5	4	3 2	1	0
Id				f	е	d	С	b	a .	Z	Υ	Χ	W	٧	U .	Т 9	S F	Q	P	0	N	М	L K	J	-1	Н	G	F	E) C	В	Α
Rese	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	scrip	ptio	n																	
а	RW	CH26									I	Incl	lude	e or	exc	lude	e ch	ann	el 2	6												
			Excluded	0							E	Exc	lude	e																		
			Included	1							I	Incl	lude	9																		
b	RW	CH27									- 1	Incl	lude	e or	exc	lude	e ch	ann	el 2	7												
			Excluded	0							E	Exc	lude	e																		
			Included	1							I	Incl	lude	9																		
C	RW	CH28									I	Incl	lude	e or	exc	lude	e ch	ann	el 2	8												
			Excluded	0							E	Exc	lude	e																		
			Included	1							I	Incl	lude	e																		
d	RW	CH29									I	Incl	lude	e or	exc	lude	e ch	ann	el 2	9												
			Excluded	0							E	Exc	lud	e																		
			Included	1							I	Incl	lude	9																		
е	RW	CH30									I	Incl	lude	e or	exc	lude	e ch	ann	el 3	0												
			Excluded	0							E	Exc	lude	e																		
			Included	1							I	Incl	lude	e																		
f	RW	CH31									I	Incl	lude	e or	exc	lude	e ch	ann	el 3	1												
			Excluded	0							E	Exc	lude	e																		
			Included	1							ı	Incl	lude	9																		

22.2.46 CHG[2]

Address offset: 0x808 Channel group 2

Bit	numbe	er		3	1 30	29	9 28	3 27	7 26	5 25	5 24	1 2	23	22 2	21 2	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Id														W																					
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	(0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	٧	alu	е						D)es	scrip	tio	n																			
Α	RW	СНО										Ir	ncl	lude	or	ex	clu	de	cha	nn	el C														
			Excluded	0								Ε	xc	lude	•																				
			Included	1								Ir	ncl	lude																					
В	RW	CH1										Ir	ncl	lude	or	ex	clu	de	cha	nn	el 1														
			Excluded	0								Е	xc	lude	•																				
			Included	1								Ir	ncl	lude																					
С	RW	CH2										Ir	ncl	lude	or	ex	clu	de	cha	nn	el 2														
			Excluded	0								Ε	xc	lude	•																				
			Included	1								Ir	ncl	lude																					
D	RW	CH3										Ir	ncl	lude	or	ex	clu	de	cha	nn	el 3														
			Excluded	0								Ε	xc	lude	•																				
			Included	1								Ir	ncl	lude																					
Е	RW	CH4										Ir	ncl	lude	or	ex	clu	de	cha	nn	el 4														
			Excluded	0								Ε	xc	clude	•																				
			Included	1								Ir	ncl	lude																					
F	RW	CH5										Ir	ncl	lude	or	ex	clu	de	cha	nn	el 5														
			Excluded	0								Ε	xc	lude	9																				
			Included	1								Ir	ncl	lude																					
G	RW	CH6										Ir	ncl	lude	or	ex	clu	de	cha	nn	el 6														
			Excluded	0								Ε	xc	lude	è																				
			Included	1										lude																					
Н	RW	CH7										Ir	ncl	lude	or	ex	clu	de	cha	nn	el 7														
			Excluded	0								Ε	xc	clude	2																				
			Included	1										lude																					
I	RW	CH8												lude		ex	clu	de	cha	nn	el 8														
			Excluded	0										lude																					
			Included	1								Ir	ncl	lude																					



Bit r	numbe	er		31 30	29 28	27 2	26 25	24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0	0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
J	RW	СН9							Include or exclude channel 9
			Excluded	0					Exclude
			Included	1					Include
K	RW	CH10							Include or exclude channel 10
			Excluded	0					Exclude
			Included	1					Include
L	RW	CH11							Include or exclude channel 11
			Excluded	0					Exclude
			Included	1					Include
M	RW	CH12							Include or exclude channel 12
			Excluded	0					Exclude
			Included	1					Include
N	RW	CH13							Include or exclude channel 13
			Excluded	0					Exclude
_			Included	1					Include
0	RW	CH14							Include or exclude channel 14
			Excluded	0					Exclude
	DVA	CUAF	Included	1					Include
Р	KVV	CH15	Evaluded	0					Include or exclude channel 15
			Excluded	0					Exclude
0	D\A/	CU16	Included	1					Include Include or exclude channel 16
Q	KVV	CH16	Excluded	0					Exclude Exclude
			Included	1					Include
R	R\M	CH17	included	1					Include or exclude channel 17
IX.	11.44	CHI	Excluded	0					Exclude
			Included	1					Include
S	RW	CH18	meiadea	-					Include or exclude channel 18
		0.110	Excluded	0					Exclude
			Included	1					Include
Т	RW	CH19							Include or exclude channel 19
			Excluded	0					Exclude
			Included	1					Include
U	RW	CH20							Include or exclude channel 20
			Excluded	0					Exclude
			Included	1					Include
٧	RW	CH21							Include or exclude channel 21
			Excluded	0					Exclude
			Included	1					Include
W	RW	CH22							Include or exclude channel 22
			Excluded	0					Exclude
			Included	1					Include
Х	RW	CH23							Include or exclude channel 23
			Excluded	0					Exclude
			Included	1					Include
Υ	RW	CH24							Include or exclude channel 24
			Excluded	0					Exclude
			Included	1					Include
Z	RW	CH25							Include or exclude channel 25
			Excluded	0					Exclude
			Included	1					Include
a	RW	CH26							Include or exclude channel 26
			Excluded	0					Exclude
			Included	1					Include
b	RW	CH27							Include or exclude channel 27



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcbaZY	'XWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Excluded	0	Exclude
	Included	1	Include
c RW CH28			Include or exclude channel 28
	Excluded	0	Exclude
	Included	1	Include
d RW CH29			Include or exclude channel 29
	Excluded	0	Exclude
	Included	1	Include
e RW CH30			Include or exclude channel 30
	Excluded	0	Exclude
	Included	1	Include
f RW CH31			Include or exclude channel 31
	Excluded	0	Exclude
	Included	1	Include

22.2.47 CHG[3]

Address offset: 0x80C

Channel group 3

		ici group 5									 																	_				
	numb	er										22 2																				
Id												W V																				
Res		0000000				0	0	0	0	0		0 0			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id		/ Field	Value Id	Va	lue							escript																				
Α	RW	CH0										clude		excl	ude	cha	ınn	el 0														
			Excluded	0								clude																				
			Included	1								clude																				
В	RW	CH1										clude	or e	excl	ude	cha	ınn	el 1														
			Excluded	0								clude																				
			Included	1								clude																				
С	RW	CH2										clude	or e	excl	ude	cha	ınn	el 2														
			Excluded	0								clude																				
			Included	1								clude																				
D	RW	CH3										clude	or e	excl	ude	cha	ınn	el 3														
			Excluded	0								clude																				
			Included	1								clude																				
E	RW	CH4										clude	or e	excl	ude	cha	ınn	el 4														
			Excluded	0								clude																				
			Included	1								clude																				
F	RW	CH5										clude	or e	excl	ude	cha	ınn	el 5														
			Excluded	0								clude																				
			Included	1								clude																				
G	RW	CH6									Inc	clude	or e	excl	ude	cha	ınn	el 6														
			Excluded	0								clude																				
			Included	1								clude																				
Н	RW	CH7									Inc	clude	or e	excl	ude	cha	ınn	el 7														
			Excluded	0							Exc	clude																				
			Included	1								clude																				
I	RW	CH8									Inc	clude	or e	excl	ude	cha	ınn	el 8														
			Excluded	0							Exc	clude																				
			Included	1								clude																				
J	RW	CH9										clude	or e	excl	ude	cha	nn	el 9														
			Excluded	0							Exc	clude																				
			Included	1							Inc	clude																				
K	RW	CH10									Inc	clude	or e	excl	ude	cha	nn	el 1	0													



Dit				21.20	20.20.1	7.26	25.24	22 22 24 3	20.10.1	0.17	16 15	14.12	12.11	10.0	0	7 /	 4	2 2	1 0
Bit r	ıumber							23 22 21 : X W V											
	et 0x00	000000						0 0 0											
	RW		Value Id	Value				Descriptio											
			Excluded	0				Exclude											
			Included	1				Include											
L	RW	CH11						Include or	exclud	e cha	nnel 1	1							
			Excluded	0				Exclude											
			Included	1				Include											
M	RW	CH12						Include or	exclud	e cha	nnel 1	2							
			Excluded	0				Exclude											
			Included	1				Include											
N	RW	CH13						Include or	exclud	e cha	nnel 1	3							
			Excluded	0				Exclude											
			Included	1				Include											
0	RW	CH14						Include or	exclud	e cha	nnel 1	4							
			Excluded	0				Exclude											
			Included	1				Include											
Р	RW	CH15						Include or	exclud	e cha	nnel 1	5							
			Excluded	0				Exclude											
_	Divi	CHAC	Included	1				Include			, ,	_							
Q	RW	CH16	Evaluded	0				Include or	exclud	e cha	nnel 1	b							
			Excluded	0				Exclude											
R	D\A/	CU17	Included	1				Include Include or	avalud	o obo	anal 1	7							
ĸ	KVV	CH17	Excluded	0				Exclude	excluu	e cria	inei 1	,							
			Included	1				Include											
S	RW	CH18	ilicidded	1				Include or	exclud	e cha	nnel 1	8							
,		C1110	Excluded	0				Exclude	СХСІЦЦ	c cria		o							
			Included	1				Include											
Т	RW	CH19	o.uucu	-				Include or	exclud	e cha	nnel 1	9							
			Excluded	0				Exclude											
			Included	1				Include											
U	RW	CH20						Include or	exclud	e cha	nnel 2	0							
			Excluded	0				Exclude											
			Included	1				Include											
V	RW	CH21						Include or	exclud	e cha	nnel 2	1							
			Excluded	0				Exclude											
			Included	1				Include											
W	RW	CH22						Include or	exclud	e cha	nnel 2	2							
			Excluded	0				Exclude											
			Included	1				Include											
Χ	RW	CH23						Include or	exclud	e cha	nnel 2	3							
			Excluded	0				Exclude											
			Included	1				Include											
Υ	RW	CH24						Include or	exclud	e cha	nnel 2	4							
			Excluded	0				Exclude											
_	D: 1	CUAS	Included	1				Include			, .	_							
Z	KW	CH25	Frielinded	0				Include or	exclud	e cha	nnel 2	5							
			Excluded	0				Exclude											
2	D\A/	CH26	Included	1				Include or	ovel	o che	anel 2	c							
a	K VV	CH26	Eveluded	0				Include or	exclud	e cna	mei Z	U							
			Excluded Included	0				Exclude Include											
b	R\M/	CH27	moluucu	_				Include or	eyclud	e cha	nnel 2	7							
b	IVV	CHZ/	Excluded	0				Exclude or	caciuu	e ciidi	mer Z	,							
			Included	1				Include											
С	R\M/	CH28	moducu	1				Include or	exclud	e cha	nnel ?	8							
-			Excluded	0				Exclude	zciuu	_ 0110	2	_							
				-															



Bit	numbe	er		31	30	29 2	28 2	7 2	26 2	5 2	4 23	3 22	21	20	19	18	17	16	15 :	14 1	.3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id				f	e	d	c I	b	a Z	<u> </u>	ΥX	W	٧	U	Т	S	R	Q	Р	0 1	N M	L	K	J	1	Н	G	F E	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Val	lue						D	escri	ptic	on																		
			Included	1							In	clud	e																			
d	RW	CH29									In	clud	e oı	ex	cluc	de c	har	ine	1 29													
			Excluded	0							Ex	kclud	le																			
			Included	1							In	clud	e																			
e	RW	CH30		1									e oı	ex	cluc	de c	har	ne	I 30													
			Excluded	0							Ex	clud	le																			
			Included	1							In	clud	e																			
f	RW	CH31									In	clud	e oı	exc	cluc	de c	har	ne	l 31													
			Excluded	0							E	clud	le																			
			Included	1							In	clud	e																			

22.2.48 CHG[4]

Address offset: 0x810 Channel group 4

011	aiii	iei gioup 4																									
Bit	numb	er		31 30	29 28	3 27	26	25 24	4 2	3 22 21	20 1	9 1	3 17	16	15	14	13	12 13	l 10	9	8	7 6	5	4	3	2 :	1 0
Id				f e	d c	b	а	Z Y	′)	x w v	U .	T S	R	Q	Р	0	N	M L	K	J	I I	H G	F	Ε	D	C I	3 A
Res	et 0x0	00000000		0 0	0 0	0	0	0 0) (0 0 0	0 (0 0	0	0	0	0	0	0 0	0	0	0 (0	0	0	0	0 (0
Id	RW	Field	Value Id	Value	:				D	escript	ion																
Α	RW	CH0							lr	nclude c	r exc	lude	cha	nne	0 اء												
			Excluded	0					Е	xclude																	
			Included	1					Ir	nclude																	
В	RW	CH1							lr	nclude c	r exc	lude	cha	nne	1 ا												
			Excluded	0					Ε	xclude																	
			Included	1					lr	nclude																	
С	RW	CH2							lr	nclude c	r exc	lude	cha	nne	el 2												
			Excluded	0					Ε	xclude																	
			Included	1					lr	nclude																	
D	RW	CH3							lr	nclude c	r exc	lude	cha	nne	el 3												
			Excluded	0					Ε	xclude																	
			Included	1					lr	nclude																	
Ε	RW	CH4							lr	nclude c	r exc	lude	cha	nne	el 4												
			Excluded	0					Ε	xclude																	
			Included	1					lr	nclude																	
F	RW	CH5							lr	nclude c	r exc	lude	cha	nne	el 5												
			Excluded	0					Ε	xclude																	
			Included	1					lr	nclude																	
G	RW	CH6							lr	nclude c	r exc	lude	cha	nne	el 6												
			Excluded	0					Ε	xclude																	
			Included	1						nclude																	
Н	RW	CH7								nclude c	r exc	lude	cha	nne	el 7												
			Excluded	0						xclude																	
			Included	1						nclude																	
I	RW	CH8								nclude c	r exc	lude	cha	nne	el 8												
			Excluded	0						xclude																	
			Included	1						nclude																	
J	RW	CH9								nclude c	r exc	Iude	cha	nne	9												
			Excluded	0						xclude																	
		0.110	Included	1						nclude																	
K	RW	CH10	5 1 1 1	•						nclude c	r exc	lude	cha	nne	21 10)											
			Excluded	0						xclude																	
	B	CUAA	Included	1						nclude																	
L	KW	CH11	5 1 1 1	_						nclude c	r exc	iude	cha	nne	21 11	L											
			Excluded	0					E	xclude																	



Bit r	numb	er		31 30	29	28 2	7 26 :	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d	c b	а	Z Y	X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et OxC	0000000		0 0	0	0 0	0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	!				Description
			Included	1					Include
М	RW	CH12		_					Include or exclude channel 12
			Excluded	0					Exclude
	DIA	CUAD	Included	1					Include
N	RW	CH13	Fuelude d	0					Include or exclude channel 13
			Excluded	0					Exclude Include
0	D\A/	CH14	Included	1					Include or exclude channel 14
U	11.00	CITI4	Excluded	0					Exclude
			Included	1					Include
Р	RW	CH15		_					Include or exclude channel 15
			Excluded	0					Exclude
			Included	1					Include
Q	RW	CH16							Include or exclude channel 16
			Excluded	0					Exclude
			Included	1					Include
R	RW	CH17							Include or exclude channel 17
			Excluded	0					Exclude
			Included	1					Include
S	RW	CH18							Include or exclude channel 18
			Excluded	0					Exclude
			Included	1					Include
Т	RW	CH19							Include or exclude channel 19
			Excluded	0					Exclude
			Included	1					Include
U	RW	CH20							Include or exclude channel 20
			Excluded	0					Exclude
.,	DVA	CU24	Included	1					Include Include or exclude channel 21
V	KW	CH21	Evaludad	0					
			Excluded Included	1					Exclude Include
W	RW	CH22	meidaed	_					Include or exclude channel 22
••		3.122	Excluded	0					Exclude
			Included	1					Include
Х	RW	CH23							Include or exclude channel 23
			Excluded	0					Exclude
			Included	1					Include
Υ	RW	CH24							Include or exclude channel 24
			Excluded	0					Exclude
			Included	1					Include
Z	RW	CH25							Include or exclude channel 25
			Excluded	0					Exclude
			Included	1					Include
а	RW	CH26							Include or exclude channel 26
			Excluded	0					Exclude
			Included	1					Include
b	RW	CH27	5 1 1 1						Include or exclude channel 27
			Excluded	0					Exclude
	DVA	CUDE	Included	1					Include
С	ĸW	CH28	Evoluded	0					Include or exclude channel 28
			Excluded Included	0					Exclude Include
d	R\M/	CH29	meraucu						Include or exclude channel 29
ŭ	1.00	525	Excluded	0					Exclude
			Included	1					Include



Bitı	numbe	er		31	30 2	9 :	28 2	27 :	26 2	5 2	24 23	3 22	21	20	19	18	17	16	15 1	.4 1	3 12	2 11	10	9	8	7	6	5	4	3	2	1 0
Id				f	е	d	С	b	a Z	, ' -	Y X	W	V	U	Т	S	R	Q	Р (1 C	N N	1 L	K	J	1	Н	G	F	Е	D	C I	ВА
Res	et 0x0	0000000		0	0	0	0	0	0 0) (0 0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																		
е	RW	CH30		0								clud	de o	r ex	clu	de (har	ne	I 30													
			Excluded	-						E>	clu	de																				
			Included	0 1						In	clud	de																				
f	RW	CH31		1							In	clud	de o	r ex	clu	de (har	ne	l 31													
			Excluded	0						E>	clu	de																				
			Included	0 1							In	clud	de																			

22.2.49 CHG[5]

Address offset: 0x814 Channel group 5

Bit number	E D C B .
Reset 0x00000000000000000000000000000000000	
Id RW Field Value Id Value Description A RW CH0 Include or exclude channel 0 Excluded 0 Exclude Include 1 Include B RW CH1 Include or exclude channel 1 Excluded 0 Exclude Include 1 Include C RW CH2 Include or exclude channel 2 Excluded 0 Exclude	0 0 0 0 0
A RW CH0 Include or exclude channel 0 Excluded 0 Exclude Included 1 Include B RW CH1 Include or exclude channel 1 Excluded 0 Exclude Include 1 Include C RW CH2 Include or exclude channel 2 Excluded 0 Exclude	
B RW CH1 Excluded 0 Exclude B RW CH1 Include or exclude channel 1 Excluded 0 Exclude Include 1 Include C RW CH2 Include or exclude channel 2 Excluded 0 Exclude	
B RW CH1 Included 1 Include Excluded 0 Exclude Include Include RW CH2 Excluded 0 Exclude Included 1 Include Include Include or exclude channel 1 Include Include Exclude Excluded 0 Exclude	
B RW CH1 Include or exclude channel 1 Excluded 0 Exclude Included 1 Include C RW CH2 Include or exclude channel 2 Excluded 0 Exclude	
Excluded 0 Exclude Included 1 Include C RW CH2 Included 0 Exclude channel 2 Excluded 0 Exclude	
Included 1 Include C RW CH2 Include or exclude channel 2 Excluded 0 Exclude	
C RW CH2 Include or exclude channel 2 Excluded 0 Exclude	
Excluded 0 Exclude	
Included 1 Include	
D RW CH3 Include or exclude channel 3	
Excluded 0 Exclude	
Included 1 Include	
E RW CH4 Include or exclude channel 4	
Excluded 0 Exclude	
Included 1 Include	
F RW CH5 Include or exclude channel 5	
Excluded 0 Exclude	
Included 1 Include	
G RW CH6 Include or exclude channel 6	
Excluded 0 Exclude	
Included 1 Include	
H RW CH7 Include or exclude channel 7	
Excluded 0 Exclude	
Included 1 Include	
I RW CH8 Include or exclude channel 8	
Excluded 0 Exclude	
Included 1 Include	
J RW CH9 Include or exclude channel 9	
Excluded 0 Exclude	
Included 1 Include	
K RW CH10 Include or exclude channel 10	
Excluded 0 Exclude	
Included 1 Include	
L RW CH11 Include or exclude channel 11	
Excluded 0 Exclude	
Included 1 Include	
M RW CH12 Include or exclude channel 12	
Excluded 0 Exclude	
Included 1 Include	



Bit n	numbe	er		31 30	29 28	27 2	6 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id								Y X W V U T S R Q P O N M L K J I H G F E D C B
Rese	et OxO	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
N	RW	CH13						Include or exclude channel 13
			Excluded	0				Exclude
			Included	1				Include
0	RW	CH14						Include or exclude channel 14
			Excluded	0				Exclude
Р	D\A/	CH15	Included	1				Include Include or exclude channel 15
-	IVV	CHIS	Excluded	0				Exclude Exclude
			Included	1				Include
Q	RW	CH16						Include or exclude channel 16
-			Excluded	0				Exclude
			Included	1				Include
R	RW	CH17						Include or exclude channel 17
			Excluded	0				Exclude
			Included	1				Include
S	RW	CH18						Include or exclude channel 18
			Excluded	0				Exclude
			Included	1				Include
Т	RW	CH19						Include or exclude channel 19
			Excluded	0				Exclude
			Included	1				Include
U	RW	CH20	Fresholde d	0				Include or exclude channel 20
			Excluded	0				Exclude Include
V	R\M	CH21	Included	1				Include or exclude channel 21
•	11.00	CHZI	Excluded	0				Exclude
			Included	1				Include
W	RW	CH22						Include or exclude channel 22
			Excluded	0				Exclude
			Included	1				Include
Χ	RW	CH23						Include or exclude channel 23
			Excluded	0				Exclude
			Included	1				Include
Υ	RW	CH24						Include or exclude channel 24
			Excluded	0				Exclude
			Included	1				Include
Z	RW	CH25	5 1 1 1	•				Include or exclude channel 25
			Excluded	0				Exclude
а	D\A/	CH26	Included	1				Include Include or exclude channel 26
u	11.44	G120	Excluded	0				Exclude
			Included	1				Include
b	RW	CH27						Include or exclude channel 27
			Excluded	0				Exclude
			Included	1				Include
С	RW	CH28						Include or exclude channel 28
			Excluded	0				Exclude
			Included	1				Include
d	RW	CH29						Include or exclude channel 29
			Excluded	0				Exclude
			Included	1				Include
е	RW	CH30						Include or exclude channel 30
			Excluded	0				Exclude
	D	CUDA	Included	1				Include
f	KW	CH31						Include or exclude channel 31



Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17	7 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		fedcba	Z Y X W V U T S R	Q P O N M L K J I H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description	
	Excluded	0	Exclude	
	Included	1	Include	

22.2.50 FORK[0].TEP

Address offset: 0x910 Channel 0 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TFP		Pointer to task register

22.2.51 FORK[1].TEP

Address offset: 0x914 Channel 1 task end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 <i>A</i>	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																

22.2.52 FORK[2].TEP

Address offset: 0x918 Channel 2 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14 :	13 1	.2 1	.1 10	9	8	7	6	5	4	3 2	2 1	L 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Δ.	ДД	Α	Α	Α	Α	Α	Α	A A	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	Va	lue							De	cri	otic	n																		
Α	RW	TEP										Poi	nte	r to	tas	k re	egis	ter															

22.2.53 FORK[3].TEP

Address offset: 0x91C Channel 3 task end-point

Bit	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Id				A A A A A A A A A A A A A A A A A A A	Α
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
Id	RW	Field	Value Id	Value Description	
Α	RW	TEP		Pointer to task register	

22.2.54 FORK[4].TEP

Address offset: 0x920 Channel 4 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$
ld RW Field Value Id	Value Description
A RW TEP	Pointer to task register

22.2.55 FORK[5].TEP

Address offset: 0x924 Channel 5 task end-point

Bit number		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	А А
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id RW Field	Value Id	Val	lue							De	scri	ptic	on																			
A RW TEP										Poi	nte	r to	tas	sk re	egis	ter																

22.2.56 FORK[6].TEP

Address offset: 0x928 Channel 6 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 :	21	20 :	19 :	18 :	17 :	16 1	.5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0	j
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ /	Α Α	Α Α	A A	A A	Α	Α	Α	Α	Α	Α	Α .	A A	A A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0) () (0	0	0	0	0	0	0	0	0 (0 0	,
Id	RW	Field	Value Id	Va	lue							De	crip	otic	n																			ı
Α	RW	TEP										Poi	ntei	r to	tas	k re	gis	ter																7

22.2.57 FORK[7].TEP

Address offset: 0x92C Channel 7 task end-point

Bit num	ber		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	9 8	3 7	6	5	4	3	2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۸ ۸	4 <i>A</i>	A A	A	. A	Α	Α	Α	Α	Α
Reset 0	x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0	0
Id RV	<i>N</i> Field	Value Id	Va	lue							De	scri	ptic	on																			
A RV	W TEP										Poi	nte	r to	ta	sk r	egis	ter																_

22.2.58 FORK[8].TEP

Address offset: 0x930 Channel 8 task end-point

Bit nun	nber			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13 1	12 :	11 1	0 9	8	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ <i>A</i>	A	Α	Α	Α	Α	Α	Α	Α	АА
Reset (0x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0 0
ld R	w i	ield	Value Id	Va	lue							Des	scri	ptic	on																			
A R	W 7	ГЕР										Poi	nte	r to	tas	sk r	egis	ter																

22.2.59 FORK[9].TEP

Address offset: 0x934 Channel 9 task end-point

Bit	nui	mbe	r			31	30	29	28	27	26	25	24	23 :	22 :	21 :	20 :	19 1	l8 1	7 1	6 1	5 14	4 13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id						Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ Α	A A	Δ Δ	A	Α	Α	Α	A	Α.	Α.	Α	Α.	Α.	А А	Α	Α
Re	set	0x0	000000)		0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	F	w	Field		Value Id	Va	lue							Des	cri	otio	n																		

A RW TEP Pointer to task register



22.2.60 FORK[10].TEP

Address offset: 0x938

Channel 10 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 :	19 1	18 :	17 1	l6 1	15 1	4 1	L3 1	12 :	11 1	.0 9	9 ;	8 7	7	6 !	5 4	4 3	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	A	Α ,	Α.	Α	Α	A A	Δ ,	۸ ۸	Δ ,	Δ.	Α,	Α ,	Δ ,	A	Α	Α
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0 () () (0 ()	0	0 (0 (0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																			
Α	RW	TEP										Poi	ntei	to	tas	k re	gis	ter																

22.2.61 FORK[11].TEP

Address offset: 0x93C

Channel 11 task end-point

Bit	าเ	ımb	er				31	30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	L8 1	17 1	16	15 :	14	13 1	2 :	11 1	0 9) 8	3 7	6	5	4	3	2	1	0
Id							Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α.	Α	Α	Α	Α	Α.	Α	A A	A A		A	. 4	A	Α	Α	Α	Α	Α
Re	set	Ox(00000	00			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0
Id		RW	Field		,	Value Id	Va	lue							Des	cri	otio	n																			
Α		RW	TEP												Poi	nte	r to	tas	k re	gist	ter																

22.2.62 FORK[12].TEP

Address offset: 0x940

Channel 12 task end-point

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α ,	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	pti	on																			
Α	RW	TEP										Ро	inte	er to	ta	sk r	egis	ster																

22.2.63 FORK[13].TEP

Address offset: 0x944

Channel 13 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.64 FORK[14].TEP

Address offset: 0x948

Channel 14 task end-point

Bit number		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0	ı
ld		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ /	А А	
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	ı
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																				l
A RW TFP										Pο	inte	r to	ta	sk n	egiq	ter																	

22.2.65 FORK[15].TEP

Address offset: 0x94C

Channel 15 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$
Id RW Field Value Id	Value Description
A RW TEP	Pointer to task register

22.2.66 FORK[16].TEP

Address offset: 0x950

Channel 16 task end-point

Bit number		31 30 29	28 27 26	5 25 24 23 22	21 20 19 18	3 17 16 15 14 13	3 12 11 10 9 8	7 6 5 4 3	3 2 1 0
Id		A A A	A A A	. A A A A	A A A A	. A A A A A	. A A A A A	AAAA	A A A A
Reset 0x000000	0	0 0 0	0 0 0	0 0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0 0	0 0 0 0	0 0 0 0
ld RW Field	Value Id	Value		Descri	ption				
A RW TEP				Pointe	r to task reg	ister			

22.2.67 FORK[17].TEP

Address offset: 0x954

Channel 17 task end-point

Bit	numbe	er		31	30	29	28	27	7 26	5 25	5 24	1 23	3 22	2 21	20	19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	. A	Α	Α	Α	Δ	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	esc	ripti	on																			
Α	RW	TEP										Po	int	er t	o ta	ask ı	eg	iste	r															

22.2.68 FORK[18].TEP

Address offset: 0x958

Channel 18 task end-point

Bit num	ber		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	9 8	3 7	6	5	4	3	2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۸ ۸	4 <i>A</i>	A A	. A	. A	Α	Α	Α	Α	Α
Reset 0	x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0	0
Id RV	<i>N</i> Field	Value Id	Va	lue							De	scri	ptic	on																			
A RV	W TEP										Poi	nte	r to	ta	sk r	egis	ter																_

22.2.69 FORK[19].TEP

Address offset: 0x95C

Channel 19 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.70 FORK[20].TEP

Address offset: 0x960

Channel 20 task end-point

Bit number	31	30 29	28	27 :	26 2	25 2	4 2	3 22	21	20 1	.9 18	3 17	16	15 1	L4 1	3 12	11	10	9 8	3 7	6	5	4	3	2 1	0
Id	А	A A	Α	Α	Α.	A A	Δ Δ	A	Α	A	4 A	Α	Α	Α.	A A	A	Α	Α	A A	A A	A	Α	Α	Α	A A	Α
Reset 0x00000000	0	0 0	0	0	0	0 (0	0	0	0 (0 0	0	0	0	0 0	0	0	0	0 (0	0	0	0	0	0 0	0
Id RW Field Va	alue Id Va	lue					D	escri	ptio	n																

A RW TEP Pointer to task register



22.2.71 FORK[21].TEP

Address offset: 0x964

Channel 21 task end-point

Bit	numb	er		31	30	29	28	27	26	25	24	23	22 :	21 :	20 :	19 1	18 :	17 1	l6 1	15 1	4 1	L3 1	12 :	11 1	.0 9	9 ;	8 7	7	6 !	5 4	4 3	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	A	Α,	Α.	Α	Α	A A	Δ ,	۸ ۸	Δ ,	Δ.	Δ,	Α,	Δ ,	A	Α	Α
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0 () () (0 ()	0	0 (0 (0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	otio	n																			
Α	RW	TEP										Poi	ntei	to	tas	k re	gis	ter																

22.2.72 FORK[22].TEP

Address offset: 0x968

Channel 22 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.73 FORK[23].TEP

Address offset: 0x96C

Channel 23 task end-point

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13 :	12 :	11 1	0 9) ;	3 7	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α Α	۱ ۸	Δ Α	Α	Α	Α	Α	Α	A A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () (0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																

22.2.74 FORK[24].TEP

Address offset: 0x970

Channel 24 task end-point

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 :	10	9	8	7	6	5	4	3 2	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۱	А А
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Poi	nte	r to	tas	sk re	egis	ter																

22.2.75 FORK[25].TEP

Address offset: 0x974

Channel 25 task end-point

Bit number		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2 :	1 0	ı
ld		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ /	А А	
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	ı
ld RW Field	Value Id	Va	lue							De	scri	ptic	on																				l
A RW TFP										Pο	inte	r to	ta	sk n	egiq	ter																	

22.2.76 FORK[26].TEP

Address offset: 0x978

Channel 26 task end-point



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0									
Id	A A A A A A A A A A A A A A A A A A A									
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$									
Id RW Field Value Id	Value Description									
A RW TEP	Pointer to task register									

22.2.77 FORK[27].TEP

Address offset: 0x97C

Channel 27 task end-point

Bitı	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17 1	16 :	15 1	14 :	13 :	12	11 1	0 9	9 1	3 .	7 (5 5	5 4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α	Α	Α	A A	\ <i>A</i>	۱ ۸	Δ ,	۱ ۸	Δ ,	A /	A	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () () () (0 (0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	TEP										Poi	inte	r to	ta	sk re	gis	ter																_

22.2.78 FORK[28].TEP

Address offset: 0x980

Channel 28 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.79 FORK[29].TEP

Address offset: 0x984

Channel 29 task end-point

Bit num	ber		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	9 8	3 7	6	5	4	3	2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۸ ۸	4 <i>A</i>	A A	. A	. A	Α	Α	Α	Α	Α
Reset 0	x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0	0
Id RV	<i>N</i> Field	Value Id	Va	lue							De	scri	ptic	on																			
A RV	W TEP		Pointer							Pointer to task register											_												

22.2.80 FORK[30].TEP

Address offset: 0x988

Channel 30 task end-point

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW TEP		Pointer to task register

22.2.81 FORK[31].TEP

Address offset: 0x98C

Channel 31 task end-point

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description	

A RW TEP Pointer to task register





23 RADIO — 2.4 GHz Radio

The RADIO contains a 2.4 GHz radio receiver and a 2.4 GHz radio transmitter that is compatible with Nordic's proprietary 1 Mbps and 2 Mbps radio modes in addition to 1 Mbps and 2 Mbps *Bluetooth*® low energy mode.

EasyDMA in combination with an automated packet assembler and packet disassembler, and an automated CRC generator and CRC checker, makes it very easy to configure and use the RADIO. See *Figure 29: RADIO block diagram* on page 205 for details.

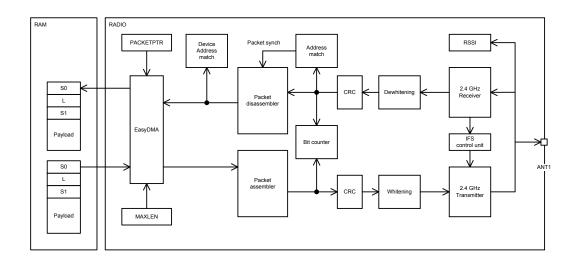


Figure 29: RADIO block diagram

The RADIO includes a Device Address Match unit and an interframe spacing control unit that can be utilized to simplify address white listing and interframe spacing respectively, in *Bluetooth* Smart and similar applications.

The RADIO also includes a Received Signal Strength Indicator (RSSI) and a bit counter. The bit counter generates events when a preconfigured number of bits have been sent or received by the RADIO.

23.1 EasyDMA

The RADIO use EasyDMA for reading and writing of data packets from and to the RAM without CPU involvement.

As illustrated in *Figure 29: RADIO block diagram* on page 205, the RADIO's EasyDMA utilizes the same PACKETPTR for receiving and transmitting packets. The CPU should reconfigure this pointer every time before the RADIO is started via the START task.

The structure of a radio packet is described in detail in *Packet configuration* on page 206. The data that is stored in Data RAM and transported by EasyDMA consists of S0, LENGTH, S1, the payload itself, and a static add-on sent immediately after the payload.

The size of each of the above elements in the frame is configurable (see *Packet configuration* on page 206), and the space occupied in RAM depends on these settings. A size of zero is possible for any of the fields, it is up to the user to make sure that the resulting frame complies with the RF protocol chosen.

For the field sizes defined in bits, the occupation in RAM will always be rounded up to the next full byte size (for instance 3 bit length will allocate 1 byte in RAM, 9 bit length will allocate 2 bytes, etc.).



In addition, the S0INCL field in PCNF0 determines if S0 is present in RAM at all if its length is zero. If present, one byte is allocated in RAM.

The size of S0 is configured through the S0LEN field in PCNF0. The size of LENGTH is configured through the LFLEN field in PCNF0. The size of S1 is configured through the S1LEN field in PCNF0. The size of the payload is configured through the value in RAM corresponding to the LENGTH field. The size of the static add-on to the payload is configured through the STATLEN field in PCNF1.

The MAXLEN field in the PCNF1 register configures the maximum packet payload plus add-on size in number of bytes that can be transmitted or received by the RADIO. This feature can be used to ensure that the RADIO does not overwrite, or read beyond, the RAM assigned to the packet payload. This means that if the packet payload length defined by PCNF1.STATLEN and the LENGTH field in the packet specifies a packet larger than MAXLEN, the payload will be truncated at MAXLEN.

Note that MAXLEN includes the payload and the add-on, but excludes the size occupied by the S0, LENGTH and S1 fields. This has to be taken into account when allocating RAM.

If the payload plus add-on length is specified larger than MAXLEN, the RADIO will still transmit or receive in the same way as before except the payload is now truncated to MAXLEN. The packet's LENGTH field will not be altered when the payload is truncated. The RADIO will calculate CRC as if the packet length is equal to MAXLEN.

If the PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The DISABLED event indicates that the EasyDMA has finished accessing the RAM.

23.2 Packet configuration

A Radio packet contains the following fields: PREAMBLE, ADDRESS, S0, LENGTH, S1, PAYLOAD and CRC.

See *Figure 30: On-air packet layout* on page 206. Not shown in the figure is the static payload add-on (the length of which is defined in STATLEN, and which is 0 bytes long in a standard BLE packet), and would be sent between PAYLOAD and CRC. The Radio sends the different fields in the packet in the order they are illustrated below, from left to right. The preamble will be sent least significant bit first on-air.

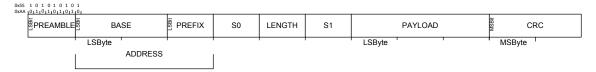


Figure 30: On-air packet layout

For all modes, except for 2 Mbit/s Bluetooth Low Energy mode, the preamble is one byte long. For 2 Mbit/s Bluetooth Low Energy mode the preamble is 2 bytes long. If the first bit of the ADDRESS is 0 the preamble will be set to 0xAA otherwise the PREAMBLE will be set to 0x55.

Radio packets are stored in memory inside instances of a radio packet data structure as illustrated in *Figure 31: In-RAM representation of radio packet, S0, LENGTH and S1 are optional* on page 206. The PREAMBLE, ADDRESS and CRC fields are omitted in this data structure.



Figure 31: In-RAM representation of radio packet, S0, LENGTH and S1 are optional



The byte ordering on air is always Least Significant Byte First for the ADDRESS and PAYLOAD fields and Most Significant Byte First for the CRC field. The ADDRESS fields are always transmitted and received least significant bit first on-air. The CRC field is always transmitted and received Most Significant Bit first. The bit-endian, i.e. which order the bits are sent and received in, of the S0, LENGTH, S1 and PAYLOAD fields can be configured via the ENDIAN in PCNF1.

The S0INCL field in PCNF0 determines if S0 is present in RAM at all if its length is zero. If present, one byte is allocated in RAM.

The sizes of the S0, LENGTH and S1 fields can be individually configured via S0LEN, LFLEN and S1LEN in PCNF0 respectively. If any of these fields are configured to be less than 8 bit long the, the least significant bits of the fields, as seen from the RAM representation, are used.

If S0, LENGTH or S1 are specified with zero length their fields will be omitted in memory, otherwise each field will be represented as a separate byte, regardless of the number of bits in their on-air counterpart.

23.3 Maximum packet length

Independent of the configuration of MAXLEN, the combined length of S0, LENGTH, S1 and PAYLOAD cannot exceed 258 bytes.

23.4 Address configuration

The on-air radio ADDRESS field is composed of two parts, the base address field and the address prefix field.

The size of the base address field is configurable via BALEN in PCNF1. The base address is truncated from LSByte if the BALEN is less than 4. See *Table 39: Definition of logical addresses* on page 207.

The on-air addresses are defined in the BASEn and PREFIXn registers, and it is only when writing these registers the user will have to relate to actual on-air addresses. For other radio address registers such as the TXADDRESS, RXADDRESSES and RXMATCH registers, logical radio addresses ranging from 0 to 7 are being used. The relationship between the on-air radio addresses and the logical addresses is described in *Table 39: Definition of logical addresses* on page 207.

Table 39: Definition of logical addresses

Logical address	Base address	Prefix byte
0	BASE0	PREFIXO.APO
1	BASE1	PREFIXO.AP1
2	BASE1	PREFIXO.AP2
3	BASE1	PREFIXO.AP3
4	BASE1	PREFIX1.AP4
5	BASE1	PREFIX1.AP5
6	BASE1	PREFIX1.AP6
7	BASE1	PREFIX1.AP7

23.5 Data whitening

The RADIO is able to do packet whitening and de-whitening.

See WHITEEN in PCNF1 register for how to enable whitening. When enabled, whitening and de-whitening will be handled by the RADIO automatically as packets are sent and received.

The whitening word is generated using polynomial $g(D) = D^7 + D^4 + 1$, which then is XORed with the data packet that is to be whitened, or de-whitened. See the figure below.



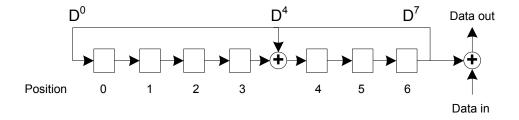


Figure 32: Data whitening and de-whitening

Whitening and de-whitening will be performed over the whole packet (except for the preamble and the address field).

The linear feedback shift register, illustrated in *Figure 32: Data whitening and de-whitening* on page 208 can be initialised via the DATAWHITEIV register.

23.6 CRC

The CRC generator in the RADIO calculates the CRC over the whole packet excluding the preamble. If desirable, the address field can be excluded from the CRC calculation as well

See CRCCNF register for more information.

The CRC polynomial is configurable as illustrated in *Figure 33: CRC generation of an n bit CRC* on page 208 where bit 0 in the CRCPOLY register corresponds to X⁰ and bit 1 corresponds to X¹ etc. See CRCPOLY for more information.

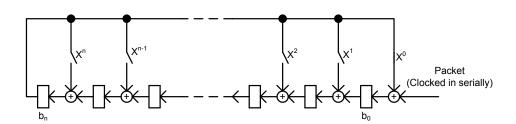


Figure 33: CRC generation of an n bit CRC

As illustrated in *Figure 33: CRC generation of an n bit CRC* on page 208, the CRC is calculated by feeding the packet serially through the CRC generator. Before the packet is clocked through the CRC generator, the CRC generator's latches b_0 through b_n will be initialized with a predefined value specified in the CRCINIT register. When the whole packet is clocked through the CRC generator, latches b_0 through b_n will hold the resulting CRC. This value will be used by the RADIO during both transmission and reception but it is not available to be read by the CPU at any time. A received CRC can however be read by the CPU via the RXCRC register independent of whether or not it has passed the CRC check.

The length (n) of the CRC is configurable, see CRCCNF for more information.

After the whole packet including the CRC has been received, the RADIO will generate a CRCOK event if no CRC errors were detected, or alternatively generate a CRCERROR event if CRC errors were detected.



The status of the CRC check can be read from the CRCSTATUS register after a packet has been received.

23.7 Radio states

The RADIO can enter a number of states.

The RADIO can enter the states described the table below. An overview state diagram for the RADIO is illustrated in *Figure 34: Radio states* on page 209. This figure shows how the tasks and events relate to the RADIO's operation. The RADIO does not prevent a task from being triggered from the wrong state. If a task is triggered from the wrong state, for example if the RXEN task is triggered from the RXDISABLE state, this may lead to incorrect behaviour. As illustrated in *Figure 34: Radio states* on page 209, the PAYLOAD event is always generated even if the payload is zero.

Table 40: RADIO state diagram

State	Description
DISABLED	No operations are going on inside the radio and the power consumption is at a minimum
RXRU	The radio is ramping up and preparing for reception
RXIDLE	The radio is ready for reception to start
RX	Reception has been started and the addresses enabled in the RXADDRESSES register are being monitored
TXRU	The radio is ramping up and preparing for transmission
TXIDLE	The radio is ready for transmission to start
TX	The radio is transmitting a packet
RXDISABLE	The radio is disabling the receiver
TXDISABLE	The radio is disabling the transmitter

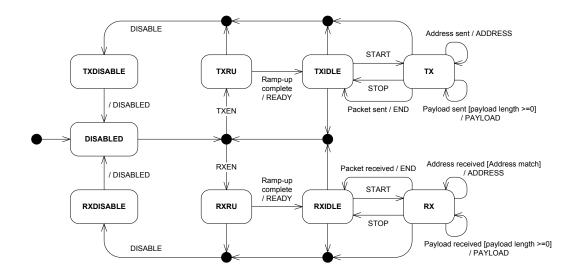


Figure 34: Radio states

23.8 Transmit sequence

Before the RADIO is able to transmit a packet, it must first ramp-up in TX mode.

See TXRU in *Figure 34: Radio states* on page 209 and *Figure 35: Transmit sequence* on page 210. A TXRU ramp-up sequence is initiated when the TXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet transmission can be initiate. A packet transmission is initiated by triggering the START task. As illustrated in *Figure 34: Radio states* on page 209 the START task can first be triggered after the RADIO has entered into the TXIDLE state.

Figure 35: Transmit sequence on page 210 illustrates a single packet transmission where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay caused by CPU execution is expected between READY and START, and between END and DISABLE. As illustrated in Figure 35: Transmit sequence on page 210



the RADIO will by default transmit '1's between READY and START, and between END and DISABLED. What is transmitted can be programmed through the DTX field in the MODECNF0 register.

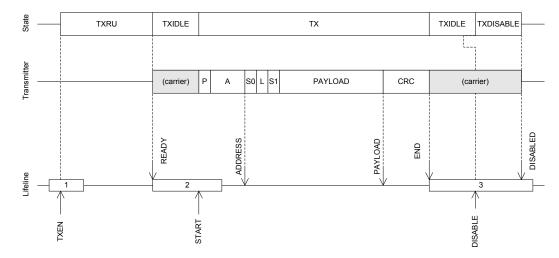


Figure 35: Transmit sequence

A slightly modified version of the transmit sequence from *Figure 35: Transmit sequence* on page 210 is illustrated in *Figure 36: Transmit sequence using shortcuts to avoid delays* on page 210 where the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.

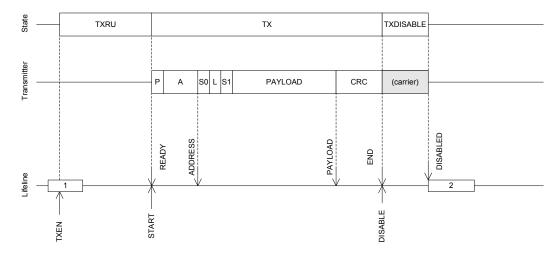


Figure 36: Transmit sequence using shortcuts to avoid delays

The RADIO is able to send multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated in *Figure 37: Transmission of multiple packets* on page 211.



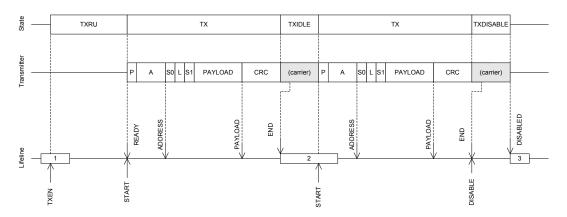


Figure 37: Transmission of multiple packets

23.9 Receive sequence

Before the RADIO is able to receive a packet, it must first ramp up in RX mode

See RXRU in *Figure 34: Radio states* on page 209 and *Figure 38: Receive sequence* on page 211. An RXRU ramp-up sequence is initiated when the RXEN task is triggered. After the radio has successfully ramped up it will generate the READY event indicating that a packet reception can be initiated. A packet reception is initiated by triggering the START task. As illustrated in *Figure 34: Radio states* on page 209 the START task can, first be triggered after the RADIO has entered into the RXIDLE state.

Figure 38: Receive sequence on page 211 illustrates a single packet reception where the CPU manually triggers the different tasks needed to control the flow of the RADIO, i.e. no shortcuts are used. If shortcuts are not used, a certain amount of delay, caused by CPU execution, is expected between READY and START, and between END and DISABLE. As illustrated Figure 38: Receive sequence on page 211 the RADIO will be listening and possibly receiving undefined data, illustrated with an 'X', from START and until a packet with valid preamble (P) is received.

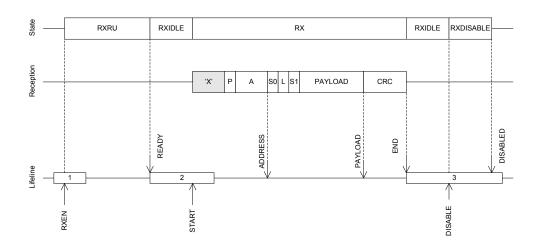


Figure 38: Receive sequence

A slightly modified version of the receive sequence from *Figure 38: Receive sequence* on page 211 is illustrated in *Figure 39: Receive sequence using shortcuts to avoid delays* on page 212 where the the RADIO is configured to use shortcuts between READY and START, and between END and DISABLE, which means that no delay is introduced.



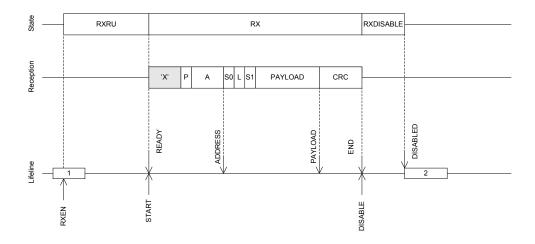


Figure 39: Receive sequence using shortcuts to avoid delays

The RADIO is able to receive multiple packets one after the other without having to disable and re-enable the RADIO between packets, this is illustrated *Figure 40: Reception of multiple packets* on page 212.

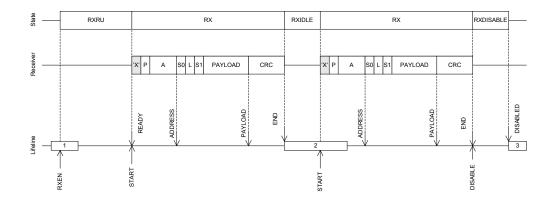


Figure 40: Reception of multiple packets

23.10 Received Signal Strength Indicator (RSSI)

The radio implements a mechanism for measuring the power in the received radio signal. This feature is called Received Signal Strength Indicator (RSSI).

Sampling of the received signal strength is started by using the RSSISTART task. The sample can be read from the RSSISAMPLE register.

The sample period of the RSSI is defined by RSSI_{PERIOD}, see the device product specification for details. The RSSI sample will hold the average received signal strength during this sample period.

For the RSSI sample to be valid the radio has to be enabled in receive mode (RXEN task) and the reception has to be started (READY event followed by START task).

23.11 Interframe spacing

Interframe spacing is the time interval between two consecutive packets.

It is defined as the time, in micro seconds, from the end of the last bit of the previous packet received and to the start of the first bit of the subsequent packet that is transmitted. The RADIO is able to enforce this



interval as specified in the TIFS register as long as TIFS is not specified to be shorter than the RADIO's turnaround time, i.e. the time needed to switch off the receiver, and switch back on the transmitter.

TIFS is only enforced if END_DISABLE and DISABLED_TXEN or END_DISABLE and DISABLED_RXEN shortcuts are enabled. TIFS is only qualified for use in BLE_1MBIT mode, and default ramp-up mode.

23.12 Device address match

The device address match feature is tailored for address white listing in a Bluetooth Smart and similar implementations.

This feature enables on-the-fly device address matching while receiving a packet on air. This feature only works in receive mode and as long as RADIO is configured for little endian, see PCNF1.ENDIAN.

The Device Address match unit assumes that the 48 first bits of the payload is the device address and that bit number 6 in S0 is the TxAdd bit. See the Bluetooth Core Specification for more information about device addresses, TxAdd and whitelisting.

The RADIO is able to listen for eight different device addresses at the same time. These addresses are specified in a DAB/DAP register pair, one pair per address, in addition to a TxAdd bit configured in the DACNF register. The DAB register specifies the 32 least significant bits of the device address, while the DAP register specifies the 16 most significant bits of the device address.

Each of the device addresses can be individually included or excluded from the matching mechanism. This is configured in the DACNF register.

23.13 Bit counter

The RADIO implements a simple counter that can be configured to generate an event after a specific number of bits have been transmitted or received.

By using shortcuts, this counter can be started from different events generated by the RADIO and hence count relative to these.

The bit counter is started by triggering the BCSTART task, and stopped by triggering the BCSTOP task. A BCMATCH event will be generated when the bit counter has counted the number of bits specified in the BCC register. The bit counter will continue to count bits until the DISABLED event is generated or until the BCSTOP task is triggered. The CPU can therefore, after a BCMATCH event, reconfigure the BCC value for new BCMATCH events within the same packet.

The bit counter can only be started after the RADIO has received the ADDRESS event.

The bit counter will stop and reset on BCSTOP, STOP, END and DISABLE tasks.

The figure below illustrates how the bit counter can be used to generate a BCMATCH event in the beginning of the packet payload, and again generate a second BCMATCH event after sending 2 bytes (16 bits) of the payload.



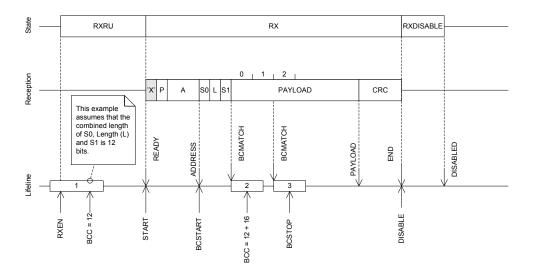


Figure 41: Bit counter example

23.14 Registers

Table 41: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40001000	RADIO	RADIO	2.4 GHz radio		

Table 42: Register Overview

Register	Offset	Description
TASKS_TXEN	0x000	Enable RADIO in TX mode
TASKS RXEN	0x000	Enable RADIO in RX mode
_		
TASKS_START	0x008	Start RADIO
TASKS_STOP	0x00C	Stop RADIO
TASKS_DISABLE	0x010	Disable RADIO
TASKS_RSSISTART	0x014	Start the RSSI and take one single sample of the receive signal strength.
TASKS_RSSISTOP	0x018	Stop the RSSI measurement
TASKS_BCSTART	0x01C	Start the bit counter
TASKS_BCSTOP	0x020	Stop the bit counter
EVENTS_READY	0x100	RADIO has ramped up and is ready to be started
EVENTS_ADDRESS	0x104	Address sent or received
EVENTS_PAYLOAD	0x108	Packet payload sent or received
EVENTS_END	0x10C	Packet sent or received
EVENTS_DISABLED	0x110	RADIO has been disabled
EVENTS_DEVMATCH	0x114	A device address match occurred on the last received packet
EVENTS_DEVMISS	0x118	No device address match occurred on the last received packet
EVENTS_RSSIEND	0x11C	Sampling of receive signal strength complete.
EVENTS_BCMATCH	0x128	Bit counter reached bit count value.
EVENTS_CRCOK	0x130	Packet received with CRC ok
EVENTS_CRCERROR	0x134	Packet received with CRC error
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CRCSTATUS	0x400	CRC status
RXMATCH	0x408	Received address
RXCRC	0x40C	CRC field of previously received packet



Register	Offset	Description	
DAI	0x410	Device address match index	
PACKETPTR	0x504	Packet pointer	
FREQUENCY	0x508	Frequency	
TXPOWER	0x50C	Output power	
MODE	0x510	Data rate and modulation	
PCNF0	0x514	Packet configuration register 0	
PCNF1	0x518	Packet configuration register 1	
BASE0	0x51C	Base address 0	
BASE1	0x520	Base address 1	
PREFIXO	0x524	Prefixes bytes for logical addresses 0-3	
PREFIX1	0x528	Prefixes bytes for logical addresses 4-7	
TXADDRESS	0x52C	Transmit address select	
RXADDRESSES	0x530	Receive address select	
CRCCNF	0x534	CRC configuration	
CRCPOLY	0x538	CRC polynomial	
CRCINIT	0x53C	CRC initial value	
	0x540		Reserved
TIFS	0x544	Inter Frame Spacing in us	
RSSISAMPLE	0x548	RSSI sample	
STATE	0x550	Current radio state	
DATAWHITEIV	0x554	Data whitening initial value	
BCC	0x560	Bit counter compare	
DAB[0]	0x600	Device address base segment 0	
DAB[1]	0x604	Device address base segment 1	
DAB[2]	0x608	Device address base segment 2	
DAB[3]	0x60C	Device address base segment 3	
DAB[4]	0x610	Device address base segment 4	
DAB[5]	0x614	Device address base segment 5	
DAB[6]	0x618	Device address base segment 6	
DAB[7]	0x61C	Device address base segment 7	
DAP[0]	0x620	Device address prefix 0	
DAP[1]	0x624	Device address prefix 1	
DAP[2]	0x628	Device address prefix 2	
DAP[3]	0x62C	Device address prefix 3	
DAP[4]	0x630	Device address prefix 4	
DAP[5]	0x634	Device address prefix 5	
DAP[6]	0x638	Device address prefix 6	
DAP[7]	0x63C	Device address prefix 7	
DACNF	0x640	Device address match configuration	
MODECNF0	0x650	Radio mode configuration register 0	
POWER	0xFFC	Peripheral power control	

23.14.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	er		31	. 30	29	28	27 2	26 2	25 2	24 2	3 22	2 21	20	19	18 :	17 1	6 1	5 14	4 13	3 12	11	10	9	8 7	6	5	4	3	2	1 0
Id																									Н	G	F	Ε	D	C I	В А
Res	et 0x0	0000000		0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																	
Α	RW	READY_START									S	hort	cut	bet	wee	n R	EAD	Y ev	/ent	an	d ST	ART	tas	k							
											S	ee E	VEN	ITS_	REA	DΥ	and	TA.	SKS_	_ST/	4RT										
			Disabled	0							D	isat	ole s	hor	tcut																
			Enabled	1							Ε	nab	le sh	ort	cut																
В	RW	END_DISABLE									S	hort	cut	bet	wee	n El	ND (evei	nt a	nd [DISA	BLE	tasl	(
											S	ee E	VEN	ITS_	ENL	ar	ıd <i>T</i>	4 <i>5K</i> .	S_D	ISA	BLE										



Bit number 31 30 29 2				4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
С	RW DISABLED_TXEN			Shortcut between DISABLED event and TXEN task
				See EVENTS_DISABLED and TASKS_TXEN
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
D	RW DISABLED_RXEN			Shortcut between DISABLED event and RXEN task
				See EVENTS_DISABLED and TASKS_RXEN
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
E	RW ADDRESS_RSSISTART		_	Shortcut between ADDRESS event and RSSISTART task
	_			C. SUSHIES ADDRESS. LITASUS DOSISTADE
		Disabled	0	See EVENTS_ADDRESS and TASKS_RSSISTART
		Disabled	0	Disable shortcut
F	RW END START	Enabled	1	Enable shortcut Shortcut between END event and START task
Г	KW END_STAKT			Shortcut between END event and START task
				See EVENTS_END and TASKS_START
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
G	RW ADDRESS_BCSTART			Shortcut between ADDRESS event and BCSTART task
				See EVENTS_ADDRESS and TASKS_BCSTART
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut
Н	RW DISABLED_RSSISTOP			Shortcut between DISABLED event and RSSISTOP task
				See EVENTS_DISABLED and TASKS_RSSISTOP
		Disabled	0	Disable shortcut
		Enabled	1	Enable shortcut

23.14.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			LK I HGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW READY			Write '1' to Enable interrupt for READY event
			See EVENTS_READY
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW ADDRESS			Write '1' to Enable interrupt for ADDRESS event
			See EVENTS_ADDRESS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW PAYLOAD			Write '1' to Enable interrupt for PAYLOAD event
			See EVENTS_PAYLOAD
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW END			Write '1' to Enable interrupt for END event



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			LK I HGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_END
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW DISABLED			Write '1' to Enable interrupt for DISABLED event
			See EVENTS_DISABLED
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW DEVMATCH		_	Write '1' to Enable interrupt for DEVMATCH event
			See EVENTS_DEVMATCH
	Set	1	Enable
	Disabled	0	Read: Disabled
C DIA DEVANCE	Enabled	1	Read: Enabled
G RW DEVMISS			Write '1' to Enable interrupt for DEVMISS event
			See EVENTS_DEVMISS
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
H RW RSSIEND			Write '1' to Enable interrupt for RSSIEND event
			See EVENTS_RSSIEND
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
I RW BCMATCH			Write '1' to Enable interrupt for BCMATCH event
			See EVENTS_BCMATCH
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
K RW CRCOK			Write '1' to Enable interrupt for CRCOK event
			See EVENTS_CRCOK
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
L RW CRCERROR			Write '1' to Enable interrupt for CRCERROR event
	C-+	4	See EVENTS_CRCERROR
	Set	1	Enable Read: Disabled
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

23.14.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit no	umbe	r		31	30	29	28	27	26	25	24	23 2	22 2	21 2	0 1	19 1	8 1	7 1	6 1	5 14	4 1	3 1	2 1:	1 10	9	8	7	6	5	4	3	2 1	0
Id																					L	. k		-1			Н	G	F	Е	D (СВ	Α
Rese	t 0x0(0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0 (0 (0) (0	0) (0	0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW	READY										Wri	te '1	L' to	Di	sab	le ir	nter	rup	t fo	r R	EAI	DY e	ven	t								
												See	EVE	NT	S_F	REA	DΥ																
			Clear	1								Disa	ble																				
	ld Rese Id	ld Reset 0x00 Id RW	Reset 0x00000000 Id RW Field	Reset 0x000000000 Id RW Field Value Id A RW READY	Reset 0x00000000	Reset 0x00000000	Reset 0x00000000 0 0 0 0 Id RW Field Value Id Value A RW READY	Reset 0x00000000	Reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Reset 0x00000000	Id Reset 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Id Reset 0x000000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	L K Reset 0x00000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0	L K I Reset 0x00000000	Reset 0x00000000	Reset 0x000000000																	



Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					LK I HGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ADDRESS			Write '1' to Disable interrupt for ADDRESS event
					See EVENTS_ADDRESS
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	PAYLOAD			Write '1' to Disable interrupt for PAYLOAD event
					See EVENTS_PAYLOAD
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	END			Write '1' to Disable interrupt for END event
					See EVENTS_END
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Ε	RW	DISABLED			Write '1' to Disable interrupt for DISABLED event
					See EVENTS_DISABLED
			Clear	1	Disable
			Disabled	0	Read: Disabled
-	DVA	DEMAATCH	Enabled	1	Read: Enabled
F	KVV	DEVMATCH			Write '1' to Disable interrupt for DEVMATCH event
					See EVENTS_DEVMATCH
			Clear	1	Disable
			Disabled Enabled	0	Read: Disabled Read: Enabled
G	RW/	DEVMISS	Ellabled	1	Write '1' to Disable interrupt for DEVMISS event
Ü	11.00	DE VIVII 33			·
			Class	1	See EVENTS_DEVMISS
			Clear Disabled	0	Disable Read: Disabled
			Enabled	1	Read: Disabled Read: Enabled
Н	RW	RSSIEND	2.nabica	-	Write '1' to Disable interrupt for RSSIEND event
					·
			Clear	1	See EVENTS_RSSIEND Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
ī	RW	ВСМАТСН			Write '1' to Disable interrupt for BCMATCH event
					See EVENTS_BCMATCH
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
K	RW	CRCOK			Write '1' to Disable interrupt for CRCOK event
					See EVENTS_CRCOK
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
L	RW	CRCERROR			Write '1' to Disable interrupt for CRCERROR event
					See EVENTS_CRCERROR
			Clear	1	Disable
			Disabled	0	Read: Disabled



Bit number		31 30 29 28 27 20	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 L K I H G F E D C B
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description

23.14.4 CRCSTATUS

Address offset: 0x400

CRC status

Bit	numbe	er		31 30	29	28	27 :	26 2	25 2	24 2	23 2	22 2	1 20	19	18	17	16	15	14 :	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0 (0	0 (0 (0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	9					C	Desc	crip	tion																		
Α	R	CRCSTATUS								C	CRC	sta	tus	of p	acke	et re	cei	ved													
			CRCError	0						P	ack	cet r	rece	ivec	l wi	th C	RC	erro	or												
			CRCOk	1						P	ack	cet r	rece	ivec	l wi	th C	RC	ok													

23.14.5 RXMATCH

Address offset: 0x408 Received address

Bit	numbe	er		31	30	29	28 2	27 2	26 2	25 2	24 2	23 2	2 2	1 2	0 1	9 1	8 17	7 16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	2 1	1 0
Id																														A	λ Α	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						1	Des	crip	tio	n																	
Α	R	RXMATCH									F	Rec	eive	d a	ddr	ess																

Logical address of which previous packet was received

23.14.6 RXCRC

Address offset: 0x40C

CRC field of previously received packet

Bit r	numb	er		31	1 30	29	28	3 27	26	5 2	5 24	1 23	3 2:	2 21	1 2	0 19	9 18	8 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Id												Α	Δ	A A	. 4	A	. 4	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A
Res	et OxC	0000000		0	0	0	0	0	0	C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (
Id	RW	Field	Value Id	Va	alue							D	esc	ript	ion	1																		
												-		c: _ ı _				1.			- 1													
Α	R	RXCRC										CI	(C)	rieid	1 01	pre	evic	ousi	/ re	ceiv	ea	pac	ket											

23.14.7 DAI

Address offset: 0x410

Device address match index

Bitı	numbe	r		31	30	29	28 2	27 26	5 25	5 24	1 23	22	21	20 1	19 1	.8 1	7 16	15	14	13 1	2 1:	1 10	9	8	7	6	5	4	3	2	1 0
Id																													,	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	n																	
Α	R	DAI									De	vice	ad	dres	s m	atch	n inc	lex													

Index (n) of device address, see $\mathsf{DAB}[n]$ and $\mathsf{DAP}[n]$, that got an address match.

23.14.8 PACKETPTR

Address offset: 0x504



Packet pointer

Bit	numbe	er		31	L 30	29	28	3 27	26	25	24	23	22	21 :	20	19	18	17	16	15	14	13 :	12 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	\ <i>A</i>	Α Α	Α	Α	Α	Α	Α	Α .	Δ.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							Des	scri	ptio	n																		
Α	RW	PACKETPTR										Pac	ket	poi	inte	er																	
																		e u											:-				
													•					ansı ısmi		Ŭ		•		•				•					
																									·								
												pac	ket	WII	II be	ıw e	ritte	en t	o t	his a	idd	ress	s. Ir	ıs a	ddr	ess	ıs a	byt	e				
												alig	nec	d ra	m a	addı	res	s.															

23.14.9 FREQUENCY

Address offset: 0x508

Frequency

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A A A A A A
Reset 0x00000002		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW FREQUENCY		[0100]	Radio channel frequency
			Frequency = 2400 + FREQUENCY (MHz).
B RW MAP			Channel map selection.
	Default	0	Channel map between 2400 MHZ 2500 MHz
			Frequency = 2400 + FREQUENCY (MHz)
	Low	1	Channel map between 2360 MHZ 2460 MHz
			Frequency = 2360 + FREQUENCY (MHz)

23.14.10 TXPOWER

Address offset: 0x50C

Output power

		24.20	20	20.25	7.26	25.2		- 22	24.2	0.44	2 40		1.0	4.5		12.41		10	^	0	, .	· ·		2	2	1 0
		31 30	29 .	28 27	/ 26	25 2	24 23	22	21 2	0 19	€ 18	3 1/	16	15	14 1	L3 1 ₂	2 11	10	9							
																					Δ /	4 Α	A	Α	Α	A A
000000		0 0	0	0 0	0	0 (0 0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0) (0 (0	0	0	0 0
Field	Value Id	Value					De	escri	ption	1																
TXPOWER							RA	DIO	outp	out _l	pow	er.														
							Οι	ıtpu	t pov	ver	in n	uml	oer (of d	Bm,	i.e.	if th	e va	lue	-20	is s	peci	fied			
							the	e ou	tput	pov	ver v	will	be s	set t	io -2	:0dBi	m.									
	Pos4dBm	0x04					+4	dBr	n																	
	Pos3dBm	0x03					+3	dBr	n																	
	0dBm	0x00					0 0	dBm	1																	
	Neg4dBm	0xFC					-4	dBn	n																	
	Neg8dBm	0xF8					-8	dBn	n																	
	Neg12dBm	0xF4					-12	2 dB	m																	
	Neg16dBm	0xF0					-16	6 dB	m																	
	Neg20dBm	0xEC					-20	0 dB	m																	
	Neg30dBm	0xD8					-40	0 dB	m															De	orec	ated
	Neg40dBm	0xD8					-40	0 dB	m																	
	000000 Field TXPOWER	Pos4dBm Pos3dBm OdBm Neg4dBm Neg8dBm Neg12dBm Neg16dBm Neg20dBm Neg30dBm	Pos4dBm 0x04 Pos3dBm 0x03 0dBm 0x00 Neg4dBm 0xFC Neg8dBm 0xF8 Neg12dBm 0xF4 Neg16dBm 0xF0 Neg20dBm 0xEC Neg30dBm 0xEC Neg30dBm 0xD8	Pos4dBm 0x03 Pos3dBm 0x00 Neg4dBm 0x00 Neg4dBm 0xFC Neg8dBm 0xF8 Neg12dBm 0xF4 Neg16dBm 0xF0 Neg20dBm 0xEC Neg30dBm 0xD8	Pos4dBm Ox04 Pos3dBm Ox03 OdBm Ox00 Neg4dBm OxFC Neg8dBm OxF8 Neg12dBm OxF4 Neg16dBm OxF0 Neg20dBm OxEC Neg30dBm OxEC Neg30dBm OxD8	Pos4dBm	Pos4dBm Ox04 Value Value <t< td=""><td>OOOOOOO O O O O O O O O O O O O O O O O O O O</td><td>Pos4dBm Ox00 Ox00</td><td>OOO0000 O O O O O O O O O O O O O O O O O O O</td><td>OOO0000 Value Id Value Description TXPOWER RADIO output power the output power the</td><td>OOO0000 Value Id Value Description TXPOWER RADIO output power in n the output power in n output power in n the output power in n output power i</td><td>OOO0000 Value Id Value Description TXPOWER RADIO output power in number the output power will Pos4dBm 0x04 +4 dBm Pos3dBm 0x03 +3 dBm 0dBm 0x00 0 dBm Neg4dBm 0xFC -4 dBm Neg8dBm 0xF8 -8 dBm Neg12dBm 0xF4 -12 dBm Neg16dBm 0xF0 -16 dBm Neg20dBm 0xEC -20 dBm Neg30dBm 0xD8 -40 dBm</td><td>OOO0000 Value Id Value Description TXPOWER RADIO output power in number of the output power will be standard and the output power wil</td><td>OOO0000 Value Id Value Description TXPOWER RADIO output power in number of d the output power will be set to the output power w</td><td>OOO0000 Value Id Value Description TXPOWER RADIO output power in number of dBm, the output power will be set to -2 Pos4dBm 0x04 +4 dBm Pos3dBm 0x03 +3 dBm 0dBm 0x00 0 dBm Neg4dBm 0xFC -4 dBm Neg8dBm 0xF8 -8 dBm Neg12dBm 0xF4 -12 dBm Neg16dBm 0xF0 -16 dBm Neg20dBm 0xEC -20 dBm Neg30dBm 0xD8 -40 dBm</td><td>OOO0000 Value Id Value Description TXPOWER RADIO output power in number of dBm, i.e. the output power will be set to -20dB. Pos4dBm 0x04 +4 dBm Pos3dBm 0x03 +3 dBm 0dBm 0x00 0 dBm Neg4dBm 0xFC -4 dBm Neg8dBm 0xF8 -8 dBm Neg12dBm 0xF4 -12 dBm Neg20dBm 0xEC -20 dBm Neg30dBm 0xD8 -40 dBm</td><td>OOODOOO Value Id Value Description TXPOWER RADIO output power in number of dBm, i.e. if the output power will be set to -20dBm. Pos4dBm 0x04 +4 dBm Pos3dBm 0x03 +3 dBm 0dBm 0xFC -4 dBm Neg4dBm 0xFE -8 dBm Neg12dBm 0xF4 -12 dBm Neg16dBm 0xFO -16 dBm Neg20dBm 0xEC -20 dBm Neg30dBm 0xD8 -40 dBm</td><td>000000</td><td>000000</td><td>000000</td><td>000000</td><td>0000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td><td> Company Comp</td><td>0000000</td><td>0000000 O O O O O O O O O </td></t<>	OOOOOOO O O O O O O O O O O O O O O O O O O O	Pos4dBm Ox00 Ox00	OOO0000 O O O O O O O O O O O O O O O O O O O	OOO0000 Value Id Value Description TXPOWER RADIO output power the	OOO0000 Value Id Value Description TXPOWER RADIO output power in n the output power in n output power in n the output power in n output power i	OOO0000 Value Id Value Description TXPOWER RADIO output power in number the output power will Pos4dBm 0x04 +4 dBm Pos3dBm 0x03 +3 dBm 0dBm 0x00 0 dBm Neg4dBm 0xFC -4 dBm Neg8dBm 0xF8 -8 dBm Neg12dBm 0xF4 -12 dBm Neg16dBm 0xF0 -16 dBm Neg20dBm 0xEC -20 dBm Neg30dBm 0xD8 -40 dBm	OOO0000 Value Id Value Description TXPOWER RADIO output power in number of the output power will be standard and the output power wil	OOO0000 Value Id Value Description TXPOWER RADIO output power in number of d the output power will be set to the output power w	OOO0000 Value Id Value Description TXPOWER RADIO output power in number of dBm, the output power will be set to -2 Pos4dBm 0x04 +4 dBm Pos3dBm 0x03 +3 dBm 0dBm 0x00 0 dBm Neg4dBm 0xFC -4 dBm Neg8dBm 0xF8 -8 dBm Neg12dBm 0xF4 -12 dBm Neg16dBm 0xF0 -16 dBm Neg20dBm 0xEC -20 dBm Neg30dBm 0xD8 -40 dBm	OOO0000 Value Id Value Description TXPOWER RADIO output power in number of dBm, i.e. the output power will be set to -20dB. Pos4dBm 0x04 +4 dBm Pos3dBm 0x03 +3 dBm 0dBm 0x00 0 dBm Neg4dBm 0xFC -4 dBm Neg8dBm 0xF8 -8 dBm Neg12dBm 0xF4 -12 dBm Neg20dBm 0xEC -20 dBm Neg30dBm 0xD8 -40 dBm	OOODOOO Value Id Value Description TXPOWER RADIO output power in number of dBm, i.e. if the output power will be set to -20dBm. Pos4dBm 0x04 +4 dBm Pos3dBm 0x03 +3 dBm 0dBm 0xFC -4 dBm Neg4dBm 0xFE -8 dBm Neg12dBm 0xF4 -12 dBm Neg16dBm 0xFO -16 dBm Neg20dBm 0xEC -20 dBm Neg30dBm 0xD8 -40 dBm	000000	000000	000000	000000	0000000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Company Comp	0000000	0000000 O O O O O O O O O

23.14.11 MODE

Address offset: 0x510

Data rate and modulation



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	2 1 0
Id		A	. A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0
Id RW Field	Value Id	Value Description	
A RW MODE		Radio data rate and modulation setting. The radio supports	
		Frequency-shift Keying (FSK) modulation.	
	Nrf_1Mbit	0 1 Mbit/s Nordic proprietary radio mode	
	Nrf_2Mbit	1 2 Mbit/s Nordic proprietary radio mode	
	Nrf_250Kbit	2 250 kbit/s Nordic proprietary radio mode De	eprecated
	Ble_1Mbit	3 1 Mbit/s Bluetooth Low Energy	
	Ble_2Mbit	4 2 Mbit/s Bluetooth Low Energy	

23.14.12 PCNF0

Address offset: 0x514

Packet configuration register 0

Bit r	numbe	er		31	30 2	9 :	28 2	7 2	6 2	5 24	1 23	3 22	21	20	19	18	17	16 1	15 1	4 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1 0
Id										G	i			F	Ε	Ε	Ε	E							С				Α	Α	A A
Res	et 0x0	0000000		0	0	0	0 () (0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						De	escri	ptic	n																	
Α	RW	LFLEN									Le	ngth	n on	air	of	LEN	IGT	l fie	eld i	n nı	ımb	er o	f bit	s.							
С	RW	SOLEN									Le	ngth	n on	air	of	SO 1	ielo	in	nun	nber	of l	yte	s.								
Ε	RW	S1LEN									Le	ngth	n on	air	of	S1 1	ielo	in	nun	nber	of l	its.									
F	RW	S1INCL									In	clud	e or	ex	cluc	le S	1 fi	eld	in R	AM											
			Automatic	0							In	clud	e S1	fie	ld i	n R	ΑM	onl	y if	S1L	N >	0									
			Include	1							Αl	way	s ind	luc	le S	1 fi	eld	in R	ΑM	ind	epe	nde	nt o	f S1	LLEN	l					
G	RW	PLEN									Le	ngth	n of	pre	am	ble	on	air.	Dec	isio	n pc	int:	TAS	SKS	_STA	ART	tas	sk			
			8bit	0							8-	bit p	rea	mb	le																
			16bit	1							16	-bit	pre	am	ble																

23.14.13 PCNF1

Address offset: 0x518

Packet configuration register 1

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D	C C C B B B B B B B A A A A A A A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	MAXLEN		[0255]	Maximum length of packet payload. If the packet payload is
					larger than MAXLEN, the radio will truncate the payload to
					MAXLEN.
В	RW	STATLEN		[0255]	Static length in number of bytes
					The static length parameter is added to the total length of the
					payload when sending and receiving packets, e.g. if the static
					length is set to N the radio will receive or send N bytes more
					than what is defined in the LENGTH field of the packet.
С	RW	BALEN		[24]	Base address length in number of bytes
					The address field is composed of the base address and the one
					byte long address prefix, e.g. set BALEN=2 to get a total address
					of 3 bytes.
D	RW	ENDIAN			On air endianness of packet, this applies to the SO, LENGTH, S1
					and the PAYLOAD fields.
			Little	0	Least Significant bit on air first
			Big	1	Most significant bit on air first
Е	RW	WHITEEN			Enable or disable packet whitening
			Disabled	0	Disable



Id RW Field	Value Id	Value	Description						
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0 0	0 0
Id			E D C	СССВ	в в в	В В В	В А А	A A A A	A A
Bit number		31 30 29 28 27 26	5 24 23 22 21 20 19 18	8 17 16 15	5 14 13 12	11 10 9	8 7 6	5 4 3 2	1 0

23.14.14 BASE0

Address offset: 0x51C

Base address 0

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW BASEO		Base address 0

Radio base address 0.

23.14.15 BASE1

Address offset: 0x520

Base address 1

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	.0	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Д	Α	Α	Α	Α	Α	Α	Α	Α.	A	A
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α	RW	BASE1										Bas	se a	ddr	ess	1																			7

Radio base address 1.

23.14.16 PREFIX0

Address offset: 0x524

Prefixes bytes for logical addresses 0-3

Bit r	umbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	1	L 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	ВВ	В	В	В	В	В	Α	Α	Α	Α	A A	. A	A A
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue	:						Des	scri	ptic	on																		
Α	RW	AP0										Add	dres	ss p	refi	x 0.																	
В	RW	AP1										Add	dres	ss p	refi	x 1.																	
С	RW	AP2										Add	dres	ss p	refi	x 2.																	
D	RW	AP3										Add	dres	ss p	refi	х 3.																	

23.14.17 PREFIX1

Address offset: 0x528

Prefixes bytes for logical addresses 4-7

Bit r	umbe	r		31	. 30	29	28	27	26	25	24	23	22 :	21 :	20	19	18	17	16	15 :	14 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				D	D	D	D	D	D	D	D	С	С	С	С	С	С	С	С	В	В	ВІ	B E	В	В	В	Α	Α	Α	Α	Α	Α.	А А
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue	!						Des	crip	otio	n																		
Α	RW	AP4										Add	dres	s p	refi	x 4.																	
В	RW	AP5										Add	dres	s p	refi	x 5.																	
С	RW	AP6										Ado	dres	s p	refi	x 6.																	
D	RW	AP7										Add	dres	s p	refi	x 7.																	



23.14.18 TXADDRESS

Address offset: 0x52C

Transmit address select

Bit r	numbe	er		31 30 29 28 27	7 26 25 24	1 23 22 2	1 20 19	18 17	7 16	15 14	13 1	2 11 1	.0 9	8	7	6	5	4	3 2	1 0
Id																			Д	. A A
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	0 0 0	0 0	0 0	0	0 0	0 (0	0 0	0	0	0	0	0	0 0	0 0
Id	RW	Field	Value Id	Value		Descrip	tion													
Α	RW	TXADDRESS				Transmi	t addre	ss sele	ct											

Logical address to be used when transmitting a packet.

23.14.19 RXADDRESSES

Address offset: 0x530 Receive address select

	numbe	er -		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					HGFEDCBA
Res		0000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
Α	RW	ADDR0			Enable or disable reception on logical address 0.
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	ADDR1			Enable or disable reception on logical address 1.
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	ADDR2			Enable or disable reception on logical address 2.
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	ADDR3			Enable or disable reception on logical address 3.
			Disabled	0	Disable
			Enabled	1	Enable
Е	RW	ADDR4			Enable or disable reception on logical address 4.
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	ADDR5			Enable or disable reception on logical address 5.
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	ADDR6			Enable or disable reception on logical address 6.
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	ADDR7			Enable or disable reception on logical address 7.
			Disabled	0	Disable
			Enabled	1	Enable

23.14.20 CRCCNF

Address offset: 0x534 CRC configuration

	31 30	29	28 2	7 26	5 25	24	23 2	22 2	1 20	19	18	17 1	16 1	5 14	1 13	12	11 10	9	8	7	6	5 4	4 3	2	1	0
																			В						Α	Α
0	0 0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0 (0	0	0	0 0	0	0	0	0	0	0 0	0	0	0
Value Id	Value						Des	cript	tion																	
	[13]						CRC	len	gth i	in nu	ımb	er o	f by	tes.												
Disabled	0						CRC	len	gth i	is zei	ro a	nd C	CRC	calc	ulati	on i	s disa	bled	ł							
One	1						CRC	len	gth i	is on	e by	/te a	and	CRC	calc	ulat	ion is	ena	ble	d						
Two	2						CRC	len	gth i	is tw	o b	ytes	and	l CR	C cal	cula	tion i	s en	able	ed						
0	Disabled One	00 0 0 Value Id Value [13] Disabled 0 One 1	00	00	00	00	00	00	Value Id Value Descript [13] CRC leng Disabled 0 CRC leng One 1 CRC leng	Value Id Value Description [13] CRC length Disabled 0 CRC length One 1 CRC length	Value Id Value Description [13] CRC length in nu. Disabled 0 CRC length is zerone One 1 CRC length is on	Value Id Value Description [13] CRC length in numb Disabled 0 CRC length is zero a One 1 CRC length is one by	Value Id Value Description [13] CRC length in number of CRC length is zero and CRC length is zero and CRC length is one byte at the case of the c	Value Id Value Description [13] CRC length in number of by Disabled 0 CRC length is zero and CRC One 1 CRC length is one byte and	Value Id Value Description [13] CRC length in number of bytes. Disabled 0 CRC length is zero and CRC calc One 1 CRC length is one byte and CRC	Value Id Value Description [13] CRC length in number of bytes. Disabled 0 CRC length is zero and CRC calculations. One 1 CRC length is one byte and CRC calculations.	00	Value Id Value Description [13] CRC length in number of bytes. Disabled One 1 CRC length is one byte and CRC calculation is disa	Value Id Value Description [13] CRC length in number of bytes. Disabled 0 CRC length is zero and CRC calculation is disabled. One 1 CRC length is one byte and CRC calculation is enabled.	No 1 1 1 1 1 1 1 1 1	No 1	No 1	No 1 1 1 1 1 1 1 1 1	No 1 1 1 1 1 1 1 1 1	00	00



Bit number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A A
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Three	3	CRC length is three bytes and CRC calculation is enabled
B RW SKIPADDR			Include or exclude packet address field out of CRC calculation.
	Include	0	CRC calculation includes address field
	Skip	1	CRC calculation does not include address field. The CRC
			calculation will start at the first byte after the address.

23.14.21 CRCPOLY

Address offset: 0x538

CRC polynomial

Bit r	umbe	er		31	. 30	29	28	27	26 2	25 2	24 2	3 22	2 21	20	19	18	17	16	15 :	14 1	3 12	2 11	10	9	8	7	6 5	5 4	3	2	1 0
Id											A	4 A	Α	Α	Α	Α	Α	Α	Α	A A	A A	Α.	Α	Α	Α ,	۸ ,	Α Α	A A	Α	Α	A A
Res	t 0x0	0000000		0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0 ()	0 0	0	0	0	0 0
Id	RW	Field	Value Id	Va	llue						D	esc	ripti	ion																	
Α	RW	CRCPOLY									C	RC p	ooly	nor	nial																
											Е	ach	terr	m in	the	e CF	RC p	olyr	non	nial i	s ma	арре	d to	al	oit ir	th	is				
											r	egist	ter v	whi	ch ir	nde	х со	rre	spo	nds	to th	ne te	rm'	s ex	pon	ent	t. Th	е			
											le	east	sign	nific	ant	ter	m/b	it is	ha	rd-w	irec	int	erna	lly	to 1,	an	d bi	t			
											n	uml	oer (0 of	the	re	giste	er c	ont	ent i	s igi	nore	d by	th:	e ha	rdv	vare				
											Т	he f	ollo	win	g ex	kam	ple	is f	or a	n 8	bit C	RC	oly	non	nial:	х8	+ x7	7 +			
											х	3 + 3	(2 +	1 =	11	000	110	01.													

23.14.22 CRCINIT

Address offset: 0x53C

CRC initial value

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :	11 1	.0 9	9 .	8 7	7 (5 5	4	3	2	1)
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ Α	Δ,	A A	۱ ۸	λ Α	Α	Α	Α	Α.	Δ
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 () (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	on																			
Α	RW	CRCINIT										CRO	C in	itia	l va	lue																		7

Initial value for CRC calculation.

23.14.23 TIFS

Address offset: 0x544
Inter Frame Spacing in us

Bit r	numbe	r		31	. 30	29	28	3 27	' 26	25	24	1 23	3 22	2 2:	1 2	0 1	19 :	18	17	16	15	5 1	4 1	3 1	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																														Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0) ()	0	0	0	0	0	() (0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							D	esc	ript	tior	1																					
Α	RW	TIFS										In	ter	Fra	me	e Sį	pac	ing	g in	us																	
														fra																			/e				
												pa	acke	ets.	. It i	is c	lefi	ne	d a	s th	ne '	tim	e, i	in r	mic	ro s	eco	ond	s, fr	ron	n th	ie					
												er	nd c	of th	he	las	t bi	t o	f th	ne p	ore	vic	us	pa	cke	t to	th	e st	art	of	the	fir	st				
												bi	t of	fthe	e si	ubs	seq	ue	nt i	oac	ke	t.															

23.14.24 RSSISAMPLE

Address offset: 0x548

RSSI sample



Bitı	numbe	er		31 3	0 29	28 2	27 2	6 25	5 24	23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id																										Α	Α	Α	A A	Δ Α	A A
Res	et 0x0	0000000		0 0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 (0 0
Id	RW	Field	Value Id	Valu	е					De	scr	ipti	on																		
Α	R	RSSISAMPLE		[01	27]					RS:	SI s	am	ple																		
																					·	ster engt				•		ve			
										val	ue.	. Ac	tua	l red	ceiv	ed	sign	nal s	tre	ngth	ı is t	here	for	e as	fol	low	s:				
										rec	eiv	/ed	sigr	nal s	stre	ngt	h =	-A (dBn	1											

23.14.25 STATE

Address offset: 0x550 Current radio state

Bit number		31	30	29 :	28 2	27 2	6 2	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id																													4 A	. A	А
Reset 0x00000000		0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
ld RW Field	Value Id	Va	lue						De	escri	ptic	on																			
A R STATE									Cι	ırrer	nt ra	adic	sta	ite																	
	Disabled	0							R/	ADIO	is i	n th	ne D	isa	ble	d st	ate	!													
	RxRu	1							R/	ADIO	is i	n th	ne R	XR	U st	ate	•														
	RxIdle	2							R/	ADIO	is i	n th	ne R	XIE	LE	sta	te														
	Rx	3							R/	ADIO	is i	n th	ne R	X s	tate	•															
	RxDisable	4							R/	ADIO	is i	n th	ne R	XD	ISA	BLE	D s	tat	e												
	TxRu	9							R/	ADIO	is i	n th	ne T	XRI	J st	ate															
	TxIdle	10							R/	ADIO	is i	n tł	ne T	XID	LE :	stat	te														
	Tx	11							R/	ADIO	is i	n tł	ne T	X s	tate	:															
	TxDisable	12							R/	ADIO	is i	n tł	ne T	XD	ISAI	3LE	D s	tat	е												

23.14.26 DATAWHITEIV

Address offset: 0x554

Data whitening initial value

Bit r	umbe	r		31	L 30	29	28	27	26	25	24 2	23 :	22	21	20	19	18	3 17	7 16	5 15	5 14	1 13	3 12	2 13	1 10	9	8	7	6	5	4	3	2	1	0
Id																													Α	Α	Α	Α	Α	Α	Α
Rese	t 0x0	0000040		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue						ı	Des	scri	iptio	on																				
Α	RW	DATAWHITEIV									ı	Dat	a v	vhit	teni	ing	ini	tial	val	ue.	Bit	6 i	s ha	ırd-	wir	ed t	o '1	', w	ritii	ng '	0'				
											t	to i	t ha	as r	no e	effe	ct,	an	d it	wil	l alv	way	/s b	e re	ead	bac	k ar	nd u	ised	l by	/				
											t	the	de	vic	e as	s '1	١.																		
												Bit (0 с	orr	esp	on	ds t	o F	osi	tio	n 6	of t	he	LSF	R. F	it 1	to I	Posi	itioı	n 5.					
												etc.													, -					,					
											•		•																						

23.14.27 BCC

Address offset: 0x560 Bit counter compare

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19	18 1	17 1	.6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Δ ,	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	ВСС										Bit	cou	ınte	r cc	omp	oare	:															

Bit counter compare register



23.14.28 DAB[0]

Address offset: 0x600

Device address base segment 0

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α,	4 Α	A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	DAB										De	vice	ad	dre	ss b	ase	seg	mei	nt 0													

23.14.29 DAB[1]

Address offset: 0x604

Device address base segment 1

E	Bit n	umb	er			31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	7 10	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	L 0
1	d					А	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A A	A	. Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4 Δ	A A
F	lese	t Ox	000000	0		0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0
ı	d	RW	Field		Value Id	Va	lue							Des	crip	otio	n																		
1	١	RW	DAB											Dev	ice	ado	lres	s ba	se s	egi	nen	t 1													

23.14.30 DAB[2]

Address offset: 0x608

Device address base segment 2

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	17 1	16 1	L5 1	14 :	13 :	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α.	Α.	Α	Α	Α	A A	. Δ	. A	Α	Α	Α	Α	Α	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	DAB										De	vice	ad	dre	ss b	ase	seg	gme	ent	2												

23.14.31 DAB[3]

Address offset: 0x60C

Device address base segment 3

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19 :	18	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	٨
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	lue							De	cri	ptic	n																				
Α	RW	DAB										Dev	/ice	ad	dre	ss b	ase	se	gm	ent	3														7

23.14.32 DAB[4]

Address offset: 0x610

Device address base segment 4

Bit number		31	30	29	28	27	26	25	24	23	22	21 :	20 :	19 1	18 1	7 1	6 15	5 14	13	12	11 1	.0 9	8	7	6	5	4	3 2	2 1	. 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ Α	A	. A	Α	Α	A	Α /	A	. A	Α	Α	Α	A A	λ Α	A A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0
ld RW Field	Value Id	Va	lue							Des	cri	otio	n																	

A RW DAB Device address base segment 4

23.14.33 DAB[5]

Address offset: 0x614

Device address base segment 5



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id	A A A A A A A A A A A A A A A A A A A	A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id RW Field Value Id	Value Description	
A RW DAB	Device address base segment 5	

23.14.34 DAB[6]

Address offset: 0x618

Device address base segment 6

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	DAB										De	vice	ad	dre	ss b	ase	e se	gm	ent	6													

23.14.35 DAB[7]

Address offset: 0x61C

Device address base segment 7

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	DAB										De	vice	ad	dre	ss b	ase	e se	gm	ent	7													

23.14.36 DAP[0]

Address offset: 0x620 Device address prefix 0

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18	17 16 15 14 1	13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id				A A .	AAAAA	A A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0	0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW DAP			Device address pref	fix 0		

23.14.37 DAP[1]

Address offset: 0x624 Device address prefix 1

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11	1 10 9 8 7 6 5 4 3	2 1 0
Id				AAAAA	A A A A A A A A	A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	00000000	0 0 0
Id RW Field	Value Id	Value	Description			
A RW DAP			Device address prefix 1			

23.14.38 DAP[2]

Address offset: 0x628 Device address prefix 2

Bitı	numbe	er		31	30 2	29	28 2	27 2	6 2	5 2	24 2	3 2	2 21	L 20	19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id																			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 А
Res	et 0x0	0000000		0	0	0	0	0 () () (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						C	esc	ript	ion																			
Α	RW	DAP									С	evi	ce a	ddr	ess	pre	fix	2															



23.14.39 DAP[3]

Address offset: 0x62C Device address prefix 3

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 1	10 9 8 7 6 5 4 3 2 1 0
Bit Humber		31 30 23 20 27	20 23 24 23 22 21 20 13 10 17 1		
Id				AAAAAA	A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW DAP			Device address prefix 3		

23.14.40 DAP[4]

Address offset: 0x630 Device address prefix 4

Е	Bit n	umb	er						31 3	30 2	9 2	28 27	7 26	25	24	23 :	22 2	21 2	0 1	9 1	8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	l
1	d																						Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	A A	ĺ
F	Rese	t Ox	00	000000				(0	0 ()	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	
b	d	RW	/	Field		V	alue Id	,	Valu	ıe						Des	crip	otio	n																			ı
A	Α	RW	/	DAP												Dev	ice	add	lres	s pr	efix	4																1

23.14.41 DAP[5]

Address offset: 0x634

Device address prefix 5

																																_
1	Bit nur	mbe	r			31	30 2	9 28	27	26 2	25 2	4 23	22	21 2	20 1	.9 18	3 17	16	15	14 1	3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
1	d																		Α	A A	Α Α	A	Α	Α	Α	Α	Α	Α	Α	А А	A	Α
ı	Reset	0x0	0000000			0	0 (0	0	0	0 0	0	0	0	0	0 0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0
ı	ld R	RW	Field	Va	lue Id	Va	lue					De	scri	ptio	n																	
7	A F	RW	DAP									De	vice	ado	dres	s pr	efix	5														

23.14.42 DAP[6]

Address offset: 0x638

Device address prefix 6

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3	3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A	A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0
ld RW Field	Value Id	Value Description	
A RW DAP		Device address prefix 6	

23.14.43 DAP[7]

Address offset: 0x63C

Device address prefix 7

Bit number		31 30 29 28 27 20	6 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id				A A A A A A	A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description		
A RW DAP			Device address prefix 7		

23.14.44 DACNF

Address offset: 0x640

Device address match configuration



Bit	number			31 30 29	9 28 2	27 26	25 24	23 22 21 :	20 19	18 17	16 3	15 1	L4 1	3 12	11 10	9	8	7 6	5	4 3	2	1	0
Id												Р (0 1	N M	L K	J	1 1	H G	F	E D	С	В	Α
Res	et 0x000	00000		0 0 0	0	0 0	0 0	0 0 0	0 0	0 0	0	0 (0 0	0	0 0	0	0 (0 0	0	0 0	0	0	0
Id	RW Fi	ield	Value Id	Value				Description	on														
Α	RW EI	NA0						Enable or	disable	devid	e ac	ddre	ess n	natcl	ning u	sing	devi	ce ad	dres	S			_
								0															
			Disabled	0				Disabled															
			Enabled	1				Enabled															
В	RW EI	NA1						Enable or	disable	devid	e ac	ddre	ess n	natcl	ning u	sing	devi	ce ad	dres	S			
								1															
			Disabled	0				Disabled															
			Enabled	1				Enabled															
С	RW EI	NA2						Enable or	disable	devid	e ac	ddre	ess n	natcl	ning u	sing	devi	ce ad	dres	S			
								2															
			Disabled	0				Disabled															
			Enabled	1				Enabled															
D	RW EI	NA3						Enable or	disable	devid	ce ac	ddre	ess n	natcl	ning u	sing	devi	ce ad	dres	S			
								3															
			Disabled	0				Disabled															
			Enabled	1				Enabled															
Ε	RW EI	NA4						Enable or	disable	devid	ce ac	ddre	ess n	natcl	ning u	sing	devi	ce ad	dres	S			
								4															
			Disabled	0				Disabled															
			Enabled	1				Enabled															
F	RW EI	NA5						Enable or	disable	devid	ce ac	ddre	ess n	natcl	ning u	sing	devi	ce ad	dres	S			
								5															
			Disabled	0				Disabled															
			Enabled	1				Enabled															
G	RW EI	NA6						Enable or	disable	devid	ce ac	ddre	ess n	natcl	ning u	sing	devi	ce ad	dres	S			
								6															
			Disabled	0				Disabled															
			Enabled	1				Enabled								_							
Н	RW EI	NA7						Enable or	disable	devid	ce ac	ddre	ess n	natcl	ning u	sing	devi	ce ad	dres	S			
			S					7															
			Disabled	0				Disabled															
	D)4/ =	VADDO	Enabled	1				Enabled	d *														
1	RW T							TxAdd for															
J	RW T							TxAdd for TxAdd for															
K																							
L	RW T							TxAdd for TxAdd for															
M																							
N O	RW T							TxAdd for TxAdd for															
P	RW T							TxAdd for															
-	INVV I	AAUU/						TAMUU 101	uevice	auure	-55 /												

23.14.45 MODECNF0

Address offset: 0x650

Radio mode configuration register 0

Bit	num	bei	•		31	. 30	29	28	27	26	25 :	24	23 2	22 2:	1 20	0 19	18	3 17	16	15	14	13	12	11 1	.0 9	9 (3 7	6	5	4	3	2	1	0
Id																									(. (Α
Res	et 0	x00	0000200		0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0 :	. (0	0	0	0	0	0	0	0
Id	R۱	N	Field	Value Id	Va	lue							Desc	cript	ion																			
Α	R۷	Ν	RU										Radi	io ra	mp	-up	tim	ie																
				Default	0								Defa	ult	ram	ıp-u	p ti	me	(tR	XEN	I), c	om	oati	ble	with	fir	mw	are						
												,	writ	ten	for	nRF	51																	
				Fast	1								Fast	ram	ıp-ι	ıp (t	RXI	EN,I	FAS	T), s	see	elec	tric	al s	oeci	fica	tior	for	r mo	ore				
													info	rma	tion	1																		



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		C C A
Reset 0x00000200		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
C RW DTX		Default TX value
		Specifies what the RADIO will transmit when it is not started, i.e. between:
		RADIO.EVENTS_READY and RADIO.TASKS_START
		RADIO.EVENTS_END and RADIO.TASKS_START
		RADIO.EVENTS_END and RADIO.EVENTS_DISABLED
	B1	0 Transmit '1'
	В0	1 Transmit '0'
	Center	2 Transmit center frequency
		When tuning the crystal for centre frequency, the RADIO must
		be set in DTX = Center mode to be able to achieve the expected
		accuracy.

23.14.46 POWER

Address offset: 0xFFC
Peripheral power control

Bit r	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				А
Res	et 0x00000001		0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW Field	Value Id	Value	Description
Α	RW POWER			Peripheral power control. The peripheral and its registers will be
				reset to its initial state by switching the peripheral off and then
				back on again.
		Disabled	0	Peripheral is powered off
		Enabled	1	Peripheral is powered on

23.15 Electrical specification

23.15.1 General Radio Characteristics

Symbol	Description	Min.	Тур.	Max.	Units
f_{OP}	Operating frequencies	2360		2500	MHz
f _{PLL,PROG,RES}	PLL programming resolution		2		kHz
f _{PLL,CH,SP}	PLL channel spacing		1		MHz
f _{DELTA,1M}	Frequency deviation @ 1 Msps		±170		kHz
f _{DELTA,BLE,1M}	Frequency deviation @ BLE 1Msps		±250		kHz
f _{DELTA,2M}	Frequency deviation @ 2 Msps		±320		kHz
f _{DELTA,BLE,2M}	Frequency deviation @ BLE 2 Msps		±500		kHz
fsk _{SPS}	On-the-air data rate	1		2	Msps

23.15.2 Radio current consumption (Transmitter)

Symbol	Description	Min.	Тур.	Max.	Units
I _{TX,PLUS4dBM,DCDC}	TX only run current (DCDC, 3V) P _{RF} =+4 dBm		7.5		mA
I _{TX,PLUS4dBM}	TX only run current P _{RF} = +4 dBm		16.6		mA
I _{TX,0dBM,DCDC}	TX only run current (DCDC, $3V$)P _{RF} = $0dBm$		5.3		mA
I _{TX,0dBM}	TX only run current P _{RF} = 0dBm		11.6		mA
I _{TX,MINUS4dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -4dBm		4.2		mA
I _{TX,MINUS4dBM}	TX only run current P _{RF} = -4 dBm		9.3		mA
I _{TX,MINUS8dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -8 dBm		3.8		mA



Symbol	Description	Min.	Тур.	Max.	Units
I _{TX,MINUS8dBM}	TX only run current P _{RF} = -8 dBm		8.4		mA
I _{TX,MINUS12dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -12 dBm		3.5		mA
I _{TX,MINUS12dBM}	TX only run current P _{RF} = -12 dBm		7.7		mA
I _{TX,MINUS16dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -16 dBm		3.3		mA
I _{TX,MINUS16dBM}	TX only run current P _{RF} = -16 dBm		7.3		mA
I _{TX,MINUS20dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -20 dBm		3.2		mA
I _{TX,MINUS20dBM}	TX only run current P _{RF} = -20 dBm		7.0		mA
I _{TX,MINUS40dBM,DCDC}	TX only run current DCDC, 3V P _{RF} = -40 dBm		2.7		mA
I _{TX,MINUS40dBM}	TX only run current P _{RF} = -40 dBm		5.9		mA
I _{START,TX,DCDC}	TX start-up current DCDC, 3V, P _{RF} = 4 dBm		4.0		mA
I _{START,TX}	TX start-up current, P _{RF} = 4 dBm		8.8		mA

23.15.3 Radio current consumption (Receiver)

Symbol	Description	Min.	Тур.	Max.	Units
I _{RX,1M,DCDC}	RX only run current (DCDC, 3V) 1Msps / 1Msps BLE		5.4		mA
I _{RX,1M}	RX only run current 1Msps / 1Msps BLE		11.7		mA
I _{RX,2M,DCDC}	RX only run current (DCDC, 3V) 2Msps / 2Msps BLE		5.8		mA
I _{RX,2M}	RX only run current 2Msps / 2Msps BLE		12.9		mA
I _{START,RX,DCDC}	RX start-up current (DCDC 3V)		3.5		mA
I _{START,RX,LDO}	RX start-up current (LDO 3V)		7.5		mA

23.15.4 Transmitter specification

Symbol	Description	Min.	Тур.	Max.	Units
P _{RF}	Maximum output power		4	6	dBm
P _{RFC}	RF power control range		24		dB
P _{RFCR}	RF power accuracy			±4	dB
P _{RF1,1}	1st Adjacent Channel Transmit Power 1 MHz (1 Msps Nordic		-25		dBc
	proprietary mode)				
P _{RF2,1}	2nd Adjacent Channel Transmit Power 2 MHz (1 Msps Nordic		-50		dBc
	proprietary mode)				
P _{RF1,2}	1st Adjacent Channel Transmit Power 2 MHz (2 Msps Nordic		-25		dBc
	proprietary mode)				
P _{RF2,2}	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps Nordic		-50		dBc
	proprietary mode)				
P _{RF1,2,BLE}	1st Adjacent Channel Transmit Power 2 MHz (2 Msps BLE mode)		-20		dBc
P _{RF2,2,BLE}	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps BLE		-50		dBc
	mode)				

23.15.5 Receiver operation

Symbol	Description	Min.	Тур.	Max.	Units
P _{RX,MAX}	Maximum received signal strength at < 0.1% BER		0		dBm
P _{SENS,IT,1M}	Sensitivity, 1Msps nRF mode ¹⁶		-93		dBm
P _{SENS,IT,SP,1M,BLE}	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER=1E-3 ¹⁷		-96		dBm
P _{SENS,IT,LP,1M,BLE}	Sensitivity, 1Msps BLE ideal transmitter >=128 bytes BER=1E-4 18		-95		dBm
P _{SENS,IT,2M}	Sensitivity, 2Msps nRF mode ¹⁹		-89		dBm

¹⁶ Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

¹⁸ Equivalent BER limit < 10E-04

Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.



Symbol	Description	Min.	Тур.	Max.	Units
P _{SENS,IT,SP,2M,BLE}	Sensitivity, 2Msps BLE ideal transmitter, Packet length		-93		dBm
	<=37bytes				
P _{SENS,DT,SP,2M,BLE}	Sensitivity, 2Msps BLE dirty transmitter, Packet length		-93		dBm
	<=37bytes				
P _{SENS,IT,LP,2M,BLE}	Sensitivity, 2Msps BLE ideal transmitter >= 128bytes		-92		dBm
P _{SENS,DT,LP,2M,BLE}	Sensitivity, 2Msps BLE dirty transmitter, Packet length >=		-92		dBm
	128bytes				

23.15.6 RX selectivity

RX selectivity with equal modulation on interfering signal²⁰

Symbol	Description	Min.	Тур.	Max.	Units
C/I _{1M,co-channel}	1Msps mode, Co-Channel interference		9		dB
C/I _{1M,-1MHz}	1 Msps mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1M,+1MHz}	1 Msps mode, Adjacent (+1 MHz) interference		-10		dB
C/I _{1M,-2MHz}	1 Msps mode, Adjacent (-2 MHz) interference		-19		dB
C/I _{1M,+2MHz}	1 Msps mode, Adjacent (+2 MHz) interference		-42		dB
C/I _{1M,-3MHz}	1 Msps mode, Adjacent (-3 MHz) interference		-38		dB
C/I _{1M,+3MHz}	1 Msps mode, Adjacent (+3 MHz) interference		-48		dB
C/I _{1M,±6MHz}	1 Msps mode, Adjacent (≥6 MHz) interference		-50		dB
C/I _{1MBLE,co-channel}	1 Msps BLE mode, Co-Channel interference		6		dB
C/I _{1MBLE,-1MHz}	1 Msps BLE mode, Adjacent (-1 MHz) interference		-2		dB
C/I _{1MBLE,+1MHz}	1 Msps BLE mode, Adjacent (+1 MHz) interference		-9		dB
C/I _{1MBLE,-2MHz}	1 Msps BLE mode, Adjacent (-2 MHz) interference		-22		dB
C/I _{1MBLE,+2MHz}	1 Msps BLE mode, Adjacent (+2 MHz) interference		-46		dB
C/I _{1MBLE,>3MHz}	1 Msps BLE mode, Adjacent (≥3 MHz) interference		-50		dB
C/I _{1MBLE,image}	Image frequency Interference		-22		dB
C/I _{1MBLE,image,1MHz}	Adjacent (1 MHz) interference to in-band image frequency		-35		dB
C/I _{2M,co-channel}	2Msps mode, Co-Channel interference		10		dB
C/I _{2M,-2MHz}	2 Msps mode, Adjacent (-2 MHz) interference		6		dB
C/I _{2M,+2MHz}	2 Msps mode, Adjacent (+2 MHz) interference		-14		dB
C/I _{2M,-4MHz}	2 Msps mode, Adjacent (-4 MHz) interference		-20		dB
C/I _{2M,+4MHz}	2 Msps mode, Adjacent (+4 MHz) interference		-44		dB
C/I _{2M,-6MHz}	2 Msps mode, Adjacent (-6 MHz) interference		-42		dB
C/I _{2M,+6MHz}	2 Msps mode, Adjacent (+6 MHz) interference		-47		dB
C/I _{2M,≥12MHz}	2 Msps mode, Adjacent (≥12 MHz) interference		-52		dB
C/I _{2MBLE,co-channel}	2 Msps BLE mode, Co-Channel interference		7		dB
C/I _{2MBLE,±2MHz}	2 Msps BLE mode, Adjacent (±2 MHz) interference		0		dB
C/I _{2MBLE,±4MHz}	2 Msps BLE mode, Adjacent (±4 MHz) interference		-47		dB
C/I _{2MBLE,≥6MHz}	2 Msps BLE mode, Adjacent (≥6 MHz) interference		-49		dB
C/I _{2MBLE,image}	Image frequency Interference		-21		dB
C/I _{2MBLE,image} , 2MHz	Adjacent (2 MHz) interference to in-band image frequency		-36		dB

23.15.7 RX intermodulation

RX intermodulation²¹

Symbol	Description	Min.	Тур.	Max.	Units
P _{IMD,1M}	IMD performance, 1 Msps (3 MHz, 4 MHz, and 5 MHz offset)		-33		dBm
P _{IMD,1M,BLE}	IMD performance, BLE 1 Msps (3 MHz, 4 MHz, and 5 MHz		-30		dBm
	offset)				
P _{IMD,2M}	IMD performance, 2 Msps (6 MHz, 8 MHz, and 10 MHz offset)		-33		dBm

Wanted signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented

Wanted signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.



Symbol	Description	Min.	Тур.	Max.	Units
P _{IMD,2M,BLE}	IMD performance, BLE 2 Msps (6 MHz, 8 MHz, and 10 MHz		-32		dBm
	offset)				

23.15.8 Radio timing

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXEN}	Time between TXEN task and READY event after channel		140		us
	FREQUENCY configured				
t _{TXEN,FAST}	Time between TXEN task and READY event after channel		40		us
	FREQUENCY configured (Fast Mode)				
$t_{TXDISABLE}$	Time between DISABLE task and DISABLED event when the		6		us
	radio was in TX and mode is set to 1Msps				
t _{TXDISABLE,2M}	Time between DISABLE task and DISABLED event when the		4		us
	radio was in TX and mode is set to 2Msps				
t _{RXEN}	Time between the RXEN task and READY event after channel		140		us
	FREQUENCY configured in default mode				
t _{RXEN,FAST}	Time between the RXEN task and READY event after channel		40		us
	FREQUENCY configured in fast mode				
t _{SWITCH}	The minimum time taken to switch from RX to TX or TX to RX		20		us
	(channel FREQUENCY unchanged)				
t _{RXDISABLE}	Time between DISABLE task and DISABLED event when the		0		us
	radio was in RX				
t _{TXCHAIN}	TX chain delay		0.6		us
t _{RXCHAIN}	RX chain delay		9.4		us
t _{RXCHAIN,2M}	RX chain delay in 2Msps mode		5		us

23.15.9 Received Signal Strength Indicator (RSSI) specifications

Symbol	Description	Min.	Тур.	Max.	Units
RSSI _{ACC}	RSSI Accuracy Valid range -90 to -20 dBm		±2		dB
RSSI _{RESOLUTION}	RSSI resolution		1		dB
RSSI _{PERIOD}	Sample period		0.25		us

23.15.10 Jitter

Symbol	Description	Min.	Тур.	Max.	Units	
t _{DISABLEDJITTER}	Jitter on DISABLED event relative to END event when shortcut		0.25		us	
	between END and DISABLE is enabled.					
t _{READYJITTER}	Jitter on READY event relative to TXEN and RXEN task.		0.25		us	

23.15.11 Delay when disabling the RADIO

Symbol	Description	Min.	Тур.	Max.	Units
t _{TXDISABLE,1M}	Disable delay from TX.		6		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit				
	and MODE = Ble_1Mbit				
t _{RXDISABLE,1M}	Disable delay from RX.		0		us
	Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit				
	and MODE = Ble_1Mbit				



24 TIMER — Timer/counter

The TIMER can operate in two modes: timer and counter.

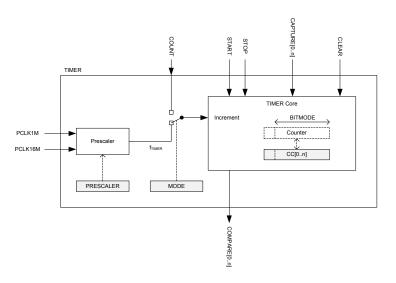


Figure 42: Block schematic for timer/counter

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a four-bit (1/2X) prescaler that can divide the timer input clock from the HFCLK controller. Clock source selection between PCLK16M and PCLK1M is automatic according to TIMER base frequency set by the prescaler. The TIMER base frequency is always given as 16 MHz divided by the prescaler value.

The PPI system allows a TIMER event to trigger a task of any other system peripheral of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

The TIMER can operate in two modes, Timer mode and Counter mode. In both modes, the TIMER is started by triggering the START task, and stopped by triggering the STOP task. After the timer is stopped the timer can resume timing/counting by triggering the START task again. When timing/counting is resumed, the timer will continue from the value it had prior to being stopped.

In Timer mode, the TIMER's internal Counter register is incremented by one for every tick of the timer frequency f_{TIMER} as illustrated in *Figure 42: Block schematic for timer/counter* on page 234. The timer frequency is derived from PCLK16M as shown below, using the values specified in the PRESCALER register:

```
f_{\text{TIMER}} = 16 \text{ MHz} / (2^{\text{PRESCALER}})
```

When $f_{TIMER} \le 1$ MHz the TIMER will use PCLK1M instead of PCLK16M for reduced power consumption.

In counter mode, the TIMER's internal Counter register is incremented by one each time the COUNT task is triggered, that is, the timer frequency and the prescaler are not utilized in counter mode. Similarly, the COUNT task has no effect in Timer mode.

The TIMER's maximum value is configured by changing the bit-width of the timer in the *BITMODE* on page 239 register.

PRESCALER on page 239 and the *BITMODE* on page 239 must only be updated when the timer is stopped. If these registers are updated while the TIMER is started then this may result in unpredictable behavior.



When the timer is incremented beyond its maximum value the Counter register will overflow and the TIMER will automatically start over from zero.

The Counter register can be cleared, that is, its internal value set to zero explicitly, by triggering the CLEAR task.

The TIMER implements multiple capture/compare registers.

Independent of prescaler setting the accuracy of the TIMER is equivalent to one tick of the timer frequency f_{TIMER} as illustrated in *Figure 42: Block schematic for timer/counter* on page 234.

24.1 Capture

The TIMER implements one capture task for every available capture/compare register.

Every time the CAPTURE[n] task is triggered, the Counter value is copied to the CC[n] register.

24.2 Compare

The TIMER implements one COMPARE event for every available capture/compare register.

A COMPARE event is generated when the Counter is incremented and then becomes equal to the value specified in one of the capture compare registers. When the Counter value becomes equal to the value specified in a capture compare register CC[n], the corresponding compare event COMPARE[n] is generated.

BITMODE on page 239 specifies how many bits of the Counter register and the capture/compare register that are used when the comparison is performed. Other bits will be ignored.

24.3 Task delays

After the TIMER is started, the CLEAR task, COUNT task and the STOP task will guarantee to take effect within one clock cycle of the PCLK16M.

24.4 Task priority

If the START task and the STOP task are triggered at the same time, that is, within the same period of PCLK16M, the STOP task will be prioritized.

24.5 Registers

Table 43: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40008000	TIMER	TIMER0	Timer 0	This timer instance has 4 CC registers
				(CC[03])
0x40009000	TIMER	TIMER1	Timer 1	This timer instance has 4 CC registers
				(CC[03])
0x4000A000	TIMER	TIMER2	Timer 2	This timer instance has 4 CC registers
				(CC[03])
0x4001A000	TIMER	TIMER3	Timer 3	This timer instance has 6 CC registers
				(CC[05])
0x4001B000	TIMER	TIMER4	Timer 4	This timer instance has 6 CC registers
				(CC[05])

Table 44: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start Timer



Register	Offset	Description	
TASKS_STOP	0x004	Stop Timer	
TASKS_COUNT	0x008	Increment Timer (Counter mode only)	
TASKS_CLEAR	0x00C	Clear time	
TASKS_SHUTDOWN	0x010	Shut down timer	Deprecated
TASKS_CAPTURE[0]	0x040	Capture Timer value to CC[0] register	
TASKS_CAPTURE[1]	0x044	Capture Timer value to CC[1] register	
TASKS_CAPTURE[2]	0x048	Capture Timer value to CC[2] register	
TASKS_CAPTURE[3]	0x04C	Capture Timer value to CC[3] register	
TASKS_CAPTURE[4]	0x050	Capture Timer value to CC[4] register	
TASKS_CAPTURE[5]	0x054	Capture Timer value to CC[5] register	
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match	
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match	
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match	
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match	
EVENTS_COMPARE[4]	0x150	Compare event on CC[4] match	
EVENTS_COMPARE[5]	0x154	Compare event on CC[5] match	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
MODE	0x504	Timer mode selection	
BITMODE	0x508	Configure the number of bits used by the TIMER	
PRESCALER	0x510	Timer prescaler register	
CC[0]	0x540	Capture/Compare register 0	
CC[1]	0x544	Capture/Compare register 1	
CC[2]	0x548	Capture/Compare register 2	
CC[3]	0x54C	Capture/Compare register 3	
CC[4]	0x550	Capture/Compare register 4	
CC[5]	0x554	Capture/Compare register 5	

24.5.1 SHORTS

Address offset: 0x200 Shortcut register

Bit number	31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		L K J I H G F E D C B A
Reset 0x00000000	0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field Value Id	Value	Description
A RW COMPAREO_CLEAR		Shortcut between COMPARE[0] event and CLEAR task
		See EVENTS_COMPARE[0] and TASKS_CLEAR
Disabled	0	Disable shortcut
Enabled	1	Enable shortcut
B RW COMPARE1_CLEAR		Shortcut between COMPARE[1] event and CLEAR task
		See EVENTS_COMPARE[1] and TASKS_CLEAR
Disabled	0	Disable shortcut
Enabled	1	Enable shortcut
C RW COMPARE2_CLEAR		Shortcut between COMPARE[2] event and CLEAR task
		See EVENTS_COMPARE[2] and TASKS_CLEAR
Disabled	0	Disable shortcut
Enabled	1	Enable shortcut
D RW COMPARE3_CLEAR		Shortcut between COMPARE[3] event and CLEAR task
		See EVENTS_COMPARE[3] and TASKS_CLEAR
Disabled	0	Disable shortcut
Enabled	1	Enable shortcut
E RW COMPARE4_CLEAR		Shortcut between COMPARE[4] event and CLEAR task
		See EVENTS_COMPARE[4] and TASKS_CLEAR



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		L K J I H G F E D C B
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Disabled	0 Disable shortcut
	Enabled	1 Enable shortcut
F RW COMPARE5_CLE	AR	Shortcut between COMPARE[5] event and CLEAR task
		See EVENTS_COMPARE[5] and TASKS_CLEAR
	Disabled	0 Disable shortcut
	Enabled	1 Enable shortcut
G RW COMPAREO_STO	P	Shortcut between COMPARE[0] event and STOP task
		See EVENTS_COMPARE[0] and TASKS_STOP
	Disabled	0 Disable shortcut
	Enabled	1 Enable shortcut
H RW COMPARE1_STO	P	Shortcut between COMPARE[1] event and STOP task
		See EVENTS_COMPARE[1] and TASKS_STOP
	Disabled	0 Disable shortcut
	Enabled	1 Enable shortcut
I RW COMPARE2_STO	P	Shortcut between COMPARE[2] event and STOP task
		See EVENTS_COMPARE[2] and TASKS_STOP
	Disabled	0 Disable shortcut
	Enabled	1 Enable shortcut
J RW COMPARE3_STC	P	Shortcut between COMPARE[3] event and STOP task
_		Con FUENTS COMMARKING and TACKS STOR
	Disabled	See EVENTS_COMPARE[3] and TASKS_STOP Disable shortcut
	Enabled	1 Enable shortcut
K RW COMPARE4_STC		Shortcut between COMPARE[4] event and STOP task
_		
	Disabled	See EVENTS_COMPARE[4] and TASKS_STOP Disable shortcut
	Enabled	1 Enable shortcut
L RW COMPARES_STO		Shortcut between COMPARE[5] event and STOP task
2 NW COMITANES_STO		
		See EVENTS_COMPARE[5] and TASKS_STOP
	Disabled	0 Disable shortcut
	Enabled	1 Enable shortcut

24.5.2 INTENSET

Address offset: 0x304

Enable interrupt

		•																																	
Bitı	numbe	er		31	30 2	9 2	28 2	27 :	26 2	25 2	24	23 :	22 2	21 2	20	19	18	17	16	15	14	1 13	3 12	2 1:	1 10	9	8	7	6	5	4	3	2	1	0
Id														F	Ε	D	С	В	Α																
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	scrip	tio	n																				
Α	RW	COMPARE0									•	Wri	ite '1	1' to	o Ei	nab	le i	inte	erru	ıpt	for	· CC	M	PAR	E[O] ev	ent								_
											:	See	EVE	EN7	rs_	coi	MP.	AR	E[0	1															
			Set	1								Ena	ble																						
			Disabled	0								Rea	ad: D	isa	ble	d																			
			Enabled	1								Rea	ad: E	nal	ble	b																			
В	RW	COMPARE1									,	Wri	ite '1	1' to	o Ei	nab	le i	inte	erru	ıpt	for	· CC	M	PAR	E[1] ev	ent								
											:	See	EVE	EN7	rs_	coi	MP.	AR	E[1	1															
			Set	1								Ena	ble																						
			Disabled	0								Rea	ad: D	isa	ble	d																			
			Enabled	1								Rea	ad: E	nal	ble	b																			
С	RW	COMPARE2										Wri	ite '1	1' to	o Ei	nab	le i	inte	erru	ıpt	for	· cc	M	PAR	E[2	l ev	ent								



Bit number			31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C B A
Reset 0x00000	000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	d	Value Id	Value	Description
				See EVENTS_COMPARE[2]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D RW COM	//PARE3			Write '1' to Enable interrupt for COMPARE[3] event
				See EVENTS_COMPARE[3]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E RW COM	//PARE4			Write '1' to Enable interrupt for COMPARE[4] event
				See EVENTS COMPARE[4]
		Set	1	See EVENTS_COMPARE[4] Enable
			1	
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F RW COM	MPARE5			Write '1' to Enable interrupt for COMPARE[5] event
				See EVENTS_COMPARE[5]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

24.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	COMPARE0			Write '1' to Disable interrupt for COMPARE[0] event
					See EVENTS_COMPARE[0]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	COMPARE1			Write '1' to Disable interrupt for COMPARE[1] event
					See EVENTS_COMPARE[1]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	COMPARE2			Write '1' to Disable interrupt for COMPARE[2] event
					See EVENTS_COMPARE[2]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	COMPARE3			Write '1' to Disable interrupt for COMPARE[3] event
					See EVENTS COMPARE[3]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
E	RW	COMPARE4			Write '1' to Disable interrupt for COMPARE[4] event
			Cloar	1	See EVENTS_COMPARE[4] Disable
			Clear	1	nisable



Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F E D C B A
Reset 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
F RW COMPARE5			Write '1' to Disable interrupt for COMPARE[5] event
			See EVENTS_COMPARE[5]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

24.5.4 MODE

Address offset: 0x504 Timer mode selection

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																		Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																				
Α	RW	MODE										Tin	ner	mo	de																				
			Timer	0								Se	lect	Tim	er	mo	de																		
			Counter	1								Se	lect	Cou	ınte	er m	nod	e														Dep	orec	cate	ed
			LowPowerCounter	2								Se	lect	Lov	v Po	we	r Co	oun	ter	mo	ode														

24.5.5 BITMODE

Address offset: 0x508

Configure the number of bits used by the TIMER

Bit	numbe	er		31	1 30	29	9 28	8 2	7 2	6 2	25 2	24	23	22	21	20	19	18	8 1	7 1	6 1	.5 :	14 :	13 :	12 :	11	10	9	8	7	6	5	4	3	2	1	0
Id																																				Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•							Des	scri	pti	on																					
Α	RW	BITMODE											Tim	ner	bit	wi	dth																				
			16Bit	0									16 I	bit	tim	ner	bit	wi	dth																		
			08Bit	1									8 bi	it ti	me	er b	it v	vid	th																		
			24Bit	2									24 I	bit	tim	ner	bit	wi	dth																		
			32Bit	3									32 I	bit	tim	ner	bit	wi	dth																		

24.5.6 PRESCALER

Address offset: 0x510
Timer prescaler register

Bit	numbe	r		31	30	29 2	28 2	7 26	25	24	23	22	21	20	19	18 :	17 1	.6 1	5 1	4 13	12	11	10	9	8	7	6	5	4	3	2 :	1 ()
Id																														A	Α Α	A A	٨
Res	et 0x0	0000004		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	L (0 0)
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	n																			
Α	RW	PRESCALER		[0.	.9]						Pre	sca	ler	valu	ıe																		-

24.5.7 CC[0]

Address offset: 0x540

Capture/Compare register 0



Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14	13 3	12 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	A	Α	Α	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	Α	A	A A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tior	1																	
Α	RW	СС										Cap	ture	e/Co	mp	are v	valu	ıe														
												Onl	y th	e nı	ımb	er o	f bit	ts in	ndic	ate	d by	BIT	МО	DE v	vill	be ι	ısed	d by	/			
												the	TIN	1ER.																		

24.5.8 CC[1]

Address offset: 0x544

Capture/Compare register 1

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	0 19	9 18	17	16	15	14	13 1	2 11	10	9	8	7	6	5	4	3	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	Δ Δ	A	Α	Α	Α	Α	A	4 A	Α	Α	Α	Α	Α	Α	Α	Α /	Δ Δ	A
Res	et 0x(0000000		0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							Des	scrip	otio	1																	
Α	RW	CC										Cap	otur	e/Co	mp	are	valı	ıe														
												Onl	ly th	ie ni	ımb	er c	f bi	ts ir	ndic	ate	d by	BITN	/OD	E w	/ill b	e u	ised	d by	,			
												the	TIN	ΛER.																		

24.5.9 CC[2]

Address offset: 0x548

Capture/Compare register 2

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 1	8 17	7 16	15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	4 A	. A	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	A A	A A	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	RW	СС										Cap	tur	e/C	om	pare	e val	ue														
												Onl	y th	ne n	um	ber	of b	its i	ndic	ate	d by	BIT	MO	DE v	vill k	oe u	ısec	d by	,			
												the	TIN	ЛER							·							·				

24.5.10 CC[3]

Address offset: 0x54C

Capture/Compare register 3

Bitı	numbe	er		31	1 30	29	9 2	8 2	27 2	26	25	24	23	22 :	21 2	20 1	19 1	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	. 4	Δ ,	Α	Α	Α	Α	Α	Α	Α	Α.	Α .	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4
Res	et 0x0	0000000		0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	כ
Id	RW	Field	Value Id	Va	alue	•							De	crip	otio	n																				
Α	RW	CC											Cap	tur	e/C	om	par	e v	alu	e																
													On the	•			ber	of	bit	s ir	ndic	ate	d b	у В	ITIV	IOD	Εw	vill b	oe u	ıse	d by	у				

24.5.11 CC[4]

Address offset: 0x550

Capture/Compare register 4

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW CC		Capture/Compare value

Capture/Compare value



Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 10 1d A A A A A A A A A A A A A A A A A A
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Bit number 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Only the number of bits indicated by BITMODE will be used by the TIMER.

24.5.12 CC[5]

Address offset: 0x554

Capture/Compare register 5

Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۸ ۸	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	pti	on																			
Α	RW	СС										Ca	otu	re/0	Con	npa	re v	/alu	e															

Only the number of bits indicated by BITMODE will be used by the TIMER.

24.6 Electrical specification

24.6.1 Timers Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{TIMER_1M}	Run current with 1 MHz clock input (PCLK1M)	3	5	8	μΑ
I _{TIMER_16M}	Run current with 16 MHz clock input (PCLK16M)	50	70	120	μΑ
t _{TIMER.START}	Time from START task is given until timer starts counting		0.25		μs



25 RTC — Real-time counter

The Real-time counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK).

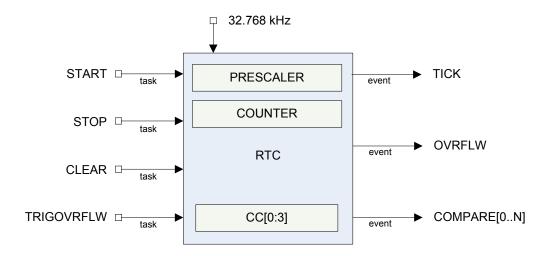


Figure 43: RTC block schematic

The RTC module features a 24-bit COUNTER, a 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

25.1 Clock source

The RTC will run off the LFCLK.

The COUNTER resolution will therefore be $30.517 \,\mu s$. Depending on the source, the RTC is able to run while the HFCLK is OFF and PCLK16M is not available.

The software has to explicitely start LFCLK before using the RTC.

See CLOCK — Clock control on page 101 for more information about clock sources.

25.2 Resolution versus overflow and the PRESCALER

Counter increment frequency:

```
f_{RTC} [kHz] = 32.768 / (PRESCALER + 1 )
```

The PRESCALER register is read/write when the RTC is stopped. The PRESCALER register is read-only once the RTC is STARTed. Writing to the PRESCALER register when the RTC is started has no effect.

The PRESCALER is restarted on START, CLEAR and TRIGOVRFLW, that is, the prescaler value is latched to an internal register (<<PRESC>>) on these tasks.

Examples:

1. Desired COUNTER frequency 100 Hz (10 ms counter period)

 $f_{RTC} = 99.9 \text{ Hz}$



10009.576 µs counter period

2. Desired COUNTER frequency 8 Hz (125 ms counter period)

PRESCALER = round(32.768 kHz / 8 Hz) - 1 = 4095

 $f_{RTC} = 8 Hz$

125 ms counter period

Table 45: RTC resolution versus overflow

Prescaler	Counter resolution	Overflow
0	30.517 μs	512 seconds
28-1	7812.5 μs	131072 seconds
2 ¹² -1	125 ms	582.542 hours

25.3 COUNTER register

The COUNTER increments on LFCLK when the internal PRESCALER register (<<PRESC>>) is 0x00. <<PRESC>> is reloaded from the PRESCALER register. If enabled, the TICK event occurs on each increment of the COUNTER. The TICK event is disabled by default.

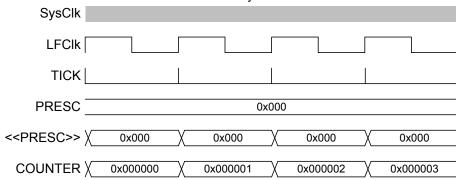


Figure 44: Timing diagram - COUNTER_PRESCALER_0

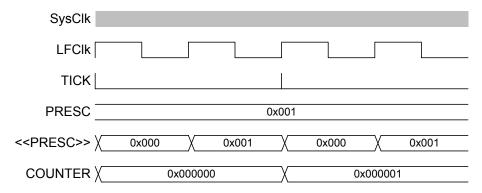


Figure 45: Timing diagram - COUNTER_PRESCALER_1

25.4 Overflow features

The TRIGOVRFLW task sets the COUNTER value to 0xFFFFF0 to allow SW test of the overflow condition.

OVRFLW occurs when COUNTER overflows from 0xFFFFFF to 0.

Important: The OVRFLW event is disabled by default.

25.5 TICK event

The TICK event enables low power "tick-less" RTOS implementation as it optionally provides a regular interrupt source for a RTOS without the need to use the ARM® SysTick feature.



Using the RTC TICK event rather than the SysTick allows the CPU to be powered down while still keeping RTOS scheduling active.

Important: The TICK event is disabled by default.

25.6 Event control feature

To optimize RTC power consumption, events in the RTC can be individually disabled to prevent PCLK16M and HFCLK being requested when those events are triggered. This is managed using the EVTEN register.

For example, if the TICK event is not required for an application, this event should be disabled as it is frequently occurring and may increase power consumption if HFCLK otherwise could be powered down for long durations.

This means that the RTC implements a slightly different task and event system compared to the standard system described in *Peripheral interface* on page 68. The RTC task and event system is illustrated in *Figure 46: Tasks, events and interrupts in the RTC* on page 244.

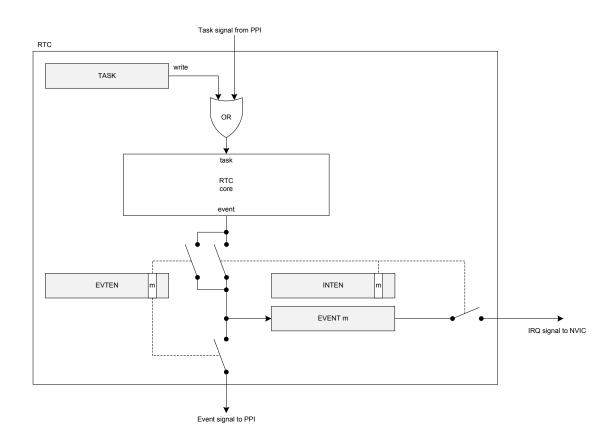


Figure 46: Tasks, events and interrupts in the RTC

25.7 Compare feature

There are a number of Compare registers.

For more information, see *Registers* on page 248.

When setting a compare register, the following behavior of the RTC compare event should be noted:

If a CC register value is 0 when a CLEAR task is set, this will not trigger a COMPARE event.



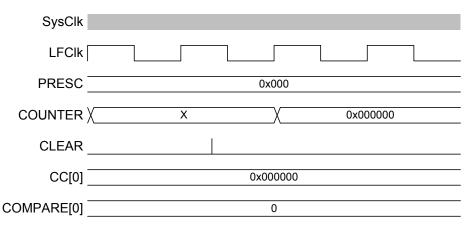


Figure 47: Timing diagram - COMPARE_CLEAR

• If a CC register is N and the COUNTER value is N when the START task is set, this will not trigger a COMPARE event.

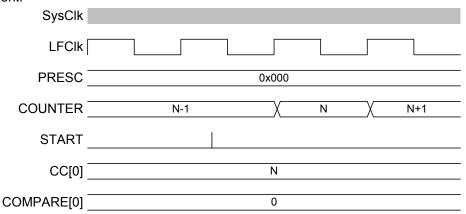


Figure 48: Timing diagram - COMPARE_START

• COMPARE occurs when a CC register is N and the COUNTER value transitions from N-1 to N.

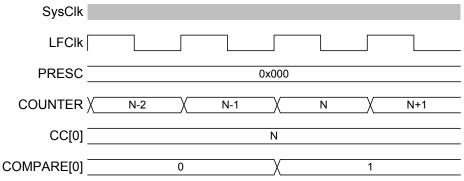


Figure 49: Timing diagram - COMPARE

• If the COUNTER is N, writing N+2 to a CC register is guaranteed to trigger a COMPARE event at N+2.



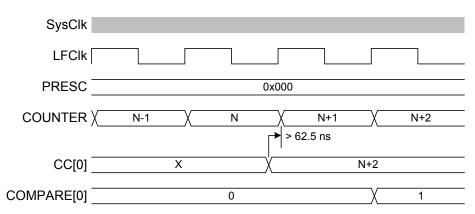


Figure 50: Timing diagram - COMPARE_N+2

• If the COUNTER is N, writing N or N+1 to a CC register may not trigger a COMPARE event.

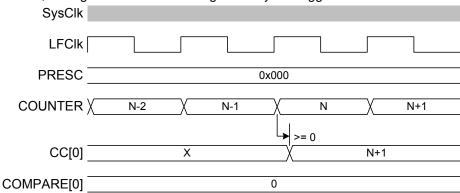


Figure 51: Timing diagram - COMPARE_N+1

• If the COUNTER is N and the current CC register value is N+1 or N+2 when a new CC value is written, a match may trigger on the previous CC value before the new value takes effect. If the current CC value greater than N+2 when the new value is written, there will be no event due to the old value.

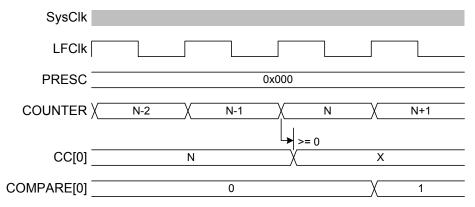


Figure 52: Timing diagram - COMPARE_N-1

25.8 TASK and EVENT jitter/delay

Jitter or delay in the RTC is due to the peripheral clock being a low frequency clock (LFCLK) which is not synchronous to the faster PCLK16M.

Registers in the peripheral interface, part of the PCLK16M domain, have a set of mirrored registers in the LFCLK domain. For example, the COUNTER value accessible from the CPU is in the PCLK16M domain and is latched on read from an internal register called COUNTER in the LFCLK domain. COUNTER is the register which is actually modified each time the RTC ticks. These registers must be synchronised between clock domains (PCLK16M and LFCLK).

The following is a summary of the jitter introduced on tasks and events. Figures illustrating jitter follow.



Table 46: RTC jitter magnitudes on tasks

 Task
 Delay

 CLEAR, STOP, START, TRIGOVRFLOW
 +15 to 46 μs

Table 47: RTC jitter magnitudes on events



1. CLEAR and STOP (and TRIGOVRFLW; not shown) will be delayed as long as it takes for the peripheral to clock a falling edge and rising of the LFCLK. This is between 15.2585 μ s and 45.7755 μ s – rounded to 15 μ s and 46 μ s for the remainder of the section.

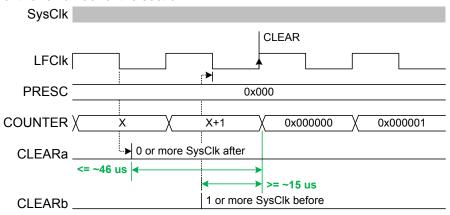


Figure 53: Timing diagram - DELAY_CLEAR

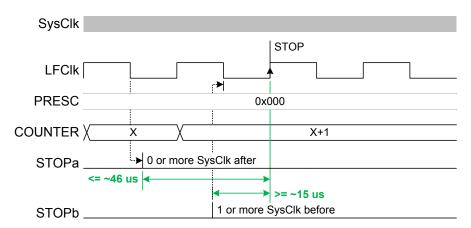


Figure 54: Timing diagram - DELAY_STOP

2. The START task will start the RTC. Assuming that the LFCLK was previously running and stable, the first increment of COUNTER (and instance of TICK event) will be typically after 30.5 μs +/-15 μs. In some cases, in particular if the RTC is STARTed before the LFCLK is running, that timing can be up to ~250 μs. The software should therefore wait for the first TICK if it has to make sure the RTC is running. Sending a TRIGOVRFLW task sets the COUNTER to a value close to overflow. However, since the update of COUNTER relies on a stable LFCLK, sending this task while LFCLK is not running will start LFCLK, but the update will then be delayed by the same amount of time of up to ~250 us. The figures show the smallest and largest delays to on the START task which appears as a +/-15 μs jitter on the first COUNTER increment.

Note: 32.768 kHz clock jitter is additional to the numbers provided above.

²² Assumes RTC runs continuously between these events.



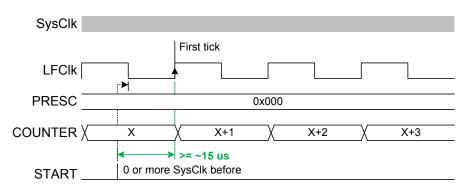


Figure 55: Timing diagram - JITTER_START-

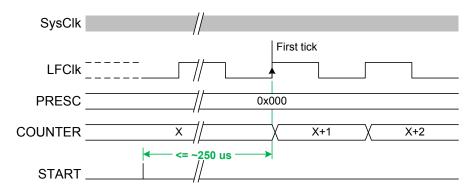


Figure 56: Timing diagram - JITTER_START+

25.9 Reading the COUNTER register

To read the COUNTER register, the internal <<COUNTER>> value is sampled.

To ensure that the <<COUNTER>> is safely sampled (considering an LFCLK transition may occur during a read), the CPU and core memory bus are halted for three cycles by lowering the core PREADY signal. The Read takes the CPU 2 cycles in addition resulting in the COUNTER register read taking a fixed five PCLK16M clock cycles.

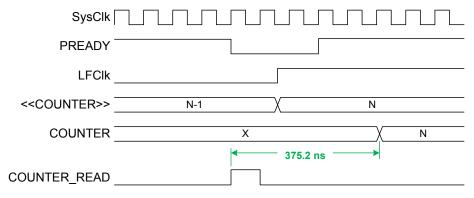


Figure 57: Timing diagram - COUNTER_READ

25.10 Registers

Table 48: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000B000	RTC	RTC0	Real-time counter 0	CC[02] implemented, CC[3] not
				implemented
0x40011000	RTC	RTC1	Real-time counter 1	CC[03] implemented



Base address	Peripheral	Instance	Description	Configuration
0x40024000	RTC	RTC2	Real-time counter 2	CC[03] implemented

Table 49: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start RTC COUNTER
TASKS_STOP	0x004	Stop RTC COUNTER
TASKS_CLEAR	0x008	Clear RTC COUNTER
TASKS_TRIGOVRFLW	0x00C	Set COUNTER to 0xFFFFF0
EVENTS_TICK	0x100	Event on COUNTER increment
EVENTS_OVRFLW	0x104	Event on COUNTER overflow
EVENTS_COMPARE[0]	0x140	Compare event on CC[0] match
EVENTS_COMPARE[1]	0x144	Compare event on CC[1] match
EVENTS_COMPARE[2]	0x148	Compare event on CC[2] match
EVENTS_COMPARE[3]	0x14C	Compare event on CC[3] match
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
EVTEN	0x340	Enable or disable event routing
EVTENSET	0x344	Enable event routing
EVTENCLR	0x348	Disable event routing
COUNTER	0x504	Current COUNTER value
PRESCALER	0x508	12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is
		stopped
CC[0]	0x540	Compare register 0
CC[1]	0x544	Compare register 1
CC[2]	0x548	Compare register 2
CC[3]	0x54C	Compare register 3

25.10.1 INTENSET

Address offset: 0x304

Enable interrupt

		•			
Bit r	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	TICK			Write '1' to Enable interrupt for TICK event
					See EVENTS_TICK
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	OVRFLW			Write '1' to Enable interrupt for OVRFLW event
					See EVENTS_OVRFLW
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	COMPARE0			Write '1' to Enable interrupt for COMPARE[0] event
					See EVENTS_COMPARE[0]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	COMPARE1			Write '1' to Enable interrupt for COMPARE[1] event
					See EVENTS_COMPARE[1]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled



Bit	numbe	r		31	30 2	9 2	28 27	7 2	6 25	24	23 2	22 2	21 20	19	18	17	16	15	14 1	.3 12	2 11	10	9	8	7	6	5	4	3 2	1	0
Id														F	Ε	D	С													В	Α
Res	et 0x0	0000000		0	0 (0 (0 0) (0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	tion																		
Ε	RW	COMPARE2									Writ	e '1	1' to	Ena	ble	inte	erru	pt f	or C	ОМІ	PARE	[2]	eve	ent							
											See	EVE	ENTS	_cc	ЭМЕ	PAR	E[2]														
			Set	1							Enal	ble																			
			Disabled	0							Read	d: D	Disab	led																	
			Enabled	1							Read	d: E	nabl	ed																	
F	RW	COMPARE3									Writ	e '1	1' to	Ena	ble	inte	erru	pt f	or C	ОМІ	PARE	[3]	eve	ent							
											See	EVE	ENTS	_cc	ЭМЕ	PAR	E[3]														
			Set	1							Enal	ble																			
			Disabled	0							Read	d: D	Disab	led																	
			Enabled	1							Read	d: E	nabl	ed																	

25.10.2 INTENCLR

Address offset: 0x308

Disable interrupt

DIS	sable interrupt			
Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F E D C
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW TICK			Write '1' to Disable interrupt for TICK event
				See EVENTS_TICK
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW OVRFLW			Write '1' to Disable interrupt for OVRFLW event
				See EVENTS_OVRFLW
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW COMPAREO			Write '1' to Disable interrupt for COMPARE[0] event
				See EVENTS_COMPARE[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW COMPARE1			Write '1' to Disable interrupt for COMPARE[1] event
				See EVENTS_COMPARE[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW COMPARE2			Write '1' to Disable interrupt for COMPARE[2] event
				See EVENTS_COMPARE[2]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW COMPARE3			Write '1' to Disable interrupt for COMPARE[3] event
				See EVENTS_COMPARE[3]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled



25.10.3 EVTEN

Address offset: 0x340

Enable or disable event routing

Rit	numbe	or .		31 30	29	28.2	7 21	5 25	24	23	22 21	20	n 19	9 18	R 17	16	: 15	14	13	12	11 1	0 0	9 8	7	6	5	4	3	2 -	1 0
Id	nambe	-1		51 50	23	20 2	, 2	, 25	1	23.	22 21			: E					13				, ,	,	Ü	J		,		3 A
	et 0x0	0000000		0 0	0	0 (0	0	0	0	0 0	0						0	0	0	0 (0	0	0	0	0	0	0		0 0
Id	RW	Field	Value Id	Value						Des	script	ion																		
Α	RW	TICK									able o				ever	nt ro	out	ing	for T	ГІСН	(eve	nt								
			Disabled	0							able	VIJ		ICK																
			Enabled	1							able																			
В	RW	OVRFLW	Lilabica	•							able o	r di	isak	ole e	ever	nt re	out	ing	for (OVE	RFIW	l eve	ent							
		· · · · · · · · · · · · · · · · · · ·															Juc	6												
											e EVEI	VTS	5_0	VRF	LW															
			Disabled	0							able																			
			Enabled	1							able																			
С	RW	COMPARE0								Ena	able o	r di	isat	ole e	ever	nt r	out	ing	for (CON	ИРΑΙ	RE[C)] ev	ent						
										See	e EVEI	VTS	_ C	ом	PAR	E[0)]													
			Disabled	0						Disa	able																			
			Enabled	1						Ena	able																			
D	RW	COMPARE1								Ena	able o	r di	isat	ole e	ever	nt re	out	ing	for (CON	ЛΡΑΙ	RE[1	.] ev	ent						
										Soo	e EVEI	VITC	: 0	ΩM	DAD	E[1	7													
			Disabled	0							able	VIJ		Olvi	ran		·J													
			Enabled	1							able																			
E	D\A/	COMPARE2	Lilabieu	1							able o	r d	icak	مام د	or	n+ r/	01.I+	ina	for (~~ N	4DAI	סבום	11 01	ont						
_	IVV	COMPAREZ								LIIa	able 0	ı u	ısar	JIE 6	vei	10.10	out	ıı ıg	101 (201	VIFAI	\L[2	.] =	CIIL						
										See	EVEI	VTS	_ C	ОМ	PAR	E[2	?]													
			Disabled	0						Disa	able																			
			Enabled	1						Ena	able																			
F	RW	COMPARE3								Ena	able o	r d	isak	ole e	ever	nt re	out	ing	for (CON	ЛРΑΙ	RE[3	8] ev	ent						
										See	e EVEI	VTS	s co	ом	PAR	E[3	31													
			Disabled	0							able																			
			Enabled	1							able																			
				•																										

25.10.4 EVTENSET

Address offset: 0x344 Enable event routing

Bit r	numbe	r		31	30 29	28	27	26 25	5 24	23 2	2 2:	1 20	19	18	17	16	15 :	14 1	.3 1	2 11	10	9	8	7	6 5	5 4	3	2	1 0
Id													F	Ε	D	С													В А
Rese	et OxO	0000000		0	0 0	0	0	0 0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0 (0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Val	ue					Desc	ript	tion																	
Α	RW	TICK								Writ	e '1'	' to I	Enal	ble	eve	nt r	out	ing	for T	ICK	evei	nt							
										See	EVE	NTS	_TIC	CK															
			Set	1						Enab	ole																		
			Disabled	0						Read	l: Di	isabl	ed																
			Enabled	1						Read	l: Er	nable	ed																
В	RW	OVRFLW								Writ	e '1'	' to I	Enal	ble	eve	nt r	out	ing	for C	OVR	LW	eve	ent						
										See	EVE	NTS_	ov	/RFL	w														
			Set	1						Enab	ole																		
			Disabled	0						Read	l: Di	isabl	ed																
			Enabled	1						Read	l: Er	nable	ed																
С	RW	COMPARE0								Writ	e '1'	' to I	Enal	ble	eve	nt r	out	ing	for C	ОМ	PAR	E[0] eve	ent					
										See	EVE	NTS_	_co	MP	ARI	[0]													
			Set	1						Enab	ole																		



Bit	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	COMPARE1			Write '1' to Enable event routing for COMPARE[1] event
					See EVENTS_COMPARE[1]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Е	RW	COMPARE2			Write '1' to Enable event routing for COMPARE[2] event
					See EVENTS_COMPARE[2]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	COMPARE3			Write '1' to Enable event routing for COMPARE[3] event
					See EVENTS COMPARE[3]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

25.10.5 EVTENCLR

Address offset: 0x348 Disable event routing

Bit	numbe	er		31 30	29	28 2	7 2	6 25	5 24	23	22	2 21	20	19	18	17	16	15	14	13	12	11 1	.0	9 8	3 7	6	5	4	3	2	1	0
Id														F	Ε	D	С														В	Α
Res	et 0x0	0000000		0 0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Value						De	esci	riptic	n																			
Α	RW	TICK										e '1' t				eve	nt	rou	ting	g fo	r TI	CK e	ver	nt								
												VEN	TS_	TIC	K																	
			Clear	1						Dis	sab	ole																				
			Disabled	0						Re	ad	: Disa	bl	ed																		
			Enabled	1						Re	ad	: Ena	ble	ed																		
В	RW	OVRFLW										e '1' t					nt	rou	ting	g fo	r O\	/RF	-W	eve	nt							
												VEN	TS_	OV	RFL	W																
			Clear	1						Dis	sab	ole																				
			Disabled	0						Re	ad	: Disa	bl	ed																		
			Enabled	1						Re	ad	: Ena	ble	ed																		
С	RW	COMPARE0								Wr	rite	e '1' t	0 [Disal	ole	eve	nt	rou	tin	g fo	r CC	MF	AR	E[0]	eve	ent						
										Se	e E	VEN	TS_	CO	MP.	ARE	[0]															
			Clear	1						Dis	sab	ole																				
			Disabled	0						Re	ad	: Disa	bl	ed																		
			Enabled	1						Re	ad	: Ena	ble	ed																		
D	RW	COMPARE1								ıW	rite	e '1' t	0 [Disal	ole	eve	nt	rou	ting	g fo	r CC	MF	AR	E[1]	eve	ent						
										Se	e E	VEN	TS_	CO	MP.	ARE	[1]															
			Clear	1						Dis	sab	ole																				
			Disabled	0						Re	ad	: Disa	bl	ed																		
			Enabled	1						Re	ad	: Ena	ble	ed																		
E	RW	COMPARE2								Wr	rite	e '1' t	0 [Disal	ole	eve	nt	rou	ting	g fo	r CC	MF	AR	E[2]	eve	ent						
										Se	e E	VEN	TS_	CO	MP.	ARE	[2]															
			Clear	1						Dis	sab	ole																				
			Disabled	0						Re	ad	: Disa	abl	ed																		
			Enabled	1						Re	ad	: Ena	ble	ed																		



Bit	numbe	er		31	1 30	29	28	3 27	7 26	25	24	23	22	21	. 20	19	9 1	8 1	.7 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																F	E	= (D	С															В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue)						De	scr	ipti	ion																					
F	RW	COMPARE3										W	rite	'1'	to	Dis	abl	e e	eve	nt ı	ou	tin	g fo	r C	ON	1PA	RE[3] 6	evei	nt						
												Se	e <i>E</i>	VEN	VTS.	_c	OM	IPA	RE	[3]																
			Clear	1								Dis	ab	le																						
			Disabled	0								Re	ad:	Dis	sab	led																				
			Enabled	1								Re	ad:	En	abl	ed																				

25.10.6 COUNTER

Address offset: 0x504

Current COUNTER value

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15	14 13 12 11 10 9 8 7 6 5 4 3 2	2 1 0
Id			A A A A A A A A	A A A A A A A A A A A A	A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0
ld RW Field	Value Id	Value	Description		
A R COUNTER			Counter value		

25.10.7 PRESCALER

Address offset: 0x508

12 bit prescaler for COUNTER frequency (32768/(PRESCALER+1)). Must be written when RTC is stopped

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id																							,	Δ Δ	Α	Α	Α	Α	Α	Α	A	Δ ,	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	RW	PRESCALER										Pre	sca	ler	val	ue																	

25.10.8 CC[0]

Address offset: 0x540 Compare register 0

Bit r	numbe	r		31	. 30	29	28	27	26	25 :	24 :	23 :	22 :	21 :	20	19	18	17 :	16	15 1	14 :	13 1	2 1	1 1	0 9	8	7	6	5	4	3	2	1 0	
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4 /	Δ Α	. Α	A	Α	Α	Α	Α	Α .	Α.	A A	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	alue	:					ı	Des	crip	otio	n																			
Α	RW	COMPARE									(Con	npa	re v	/alu	ıe																		

25.10.9 CC[1]

Address offset: 0x544 Compare register 1

Bitı	numbe	er		31	. 30	29	28	27	26 :	25 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α /	۸ ۸	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue	:						Des	cri	ptic	on																			
Α	RW	COMPARE										Cor	np	are	val	ue																		

25.10.10 CC[2]

Address offset: 0x548 Compare register 2



Bit r	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12 :	11 :	10	9	8	7	6	5 .	4	3 2	1	. 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Α Δ	. A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue	:						Des	cri	otic	n																			
Α	RW	COMPARE										Cor	npa	ire '	valı	ıe																		

25.10.11 CC[3]

Address offset: 0x54C Compare register 3

Bit r	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Δ.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																			
Α	RW	COMPARE										Coi	npa	are	val	ue																		

25.11 Electrical specification

25.11.1 RTC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
Into	Run current Real Time Counter (LECLK source)		0.1		пΑ



26 RNG — Random number generator

The Random number generator (RNG) generates true non-deterministic random numbers based on internal thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

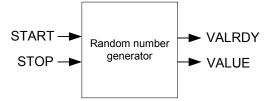


Figure 58: Random number generator

The RNG is started by triggering the START task and stopped by triggering the STOP task. When started, new random numbers are generated continuously and written to the VALUE register when ready. A VALRDY event is generated for every new random number that is written to the VALUE register. This means that after a VALRDY event is generated the CPU has the time until the next VALRDY event to read out the random number from the VALUE register before it is overwritten by a new random number.

26.1 Bias correction

A bias correction algorithm is employed on the internal bit stream to remove any bias toward '1' or '0'. The bits are then queued into an eight-bit register for parallel readout from the VALUE register.

It is possible to enable bias correction in the CONFIG register. This will result in slower value generation, but will ensure a statistically uniform distribution of the random values.

26.2 Speed

The time needed to generate one random byte of data is unpredictable, and may vary from one byte to the next. This is especially true when bias correction is enabled.

26.3 Registers

Table 50: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000D000	RNG	RNG	Random number generator	

Table 51: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the random number generator
TASKS_STOP	0x004	Task stopping the random number generator
EVENTS_VALRDY	0x100	Event being generated for every new random number written to the VALUE register
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
CONFIG	0x504	Configuration register
VALUE	0x508	Output random number

26.3.1 SHORTS

Address offset: 0x200 Shortcut register



В	t nu	ımbe	r		31	1 30	29	28	27	7 26	25	24	23	22	21	20	19	18 :	17 1	16 1	L5 1	.4 1	3 1	2 13	10	9	8	7	6	5	4	3	2 1	1 0
Id																																		Α
R	eset	0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 (0 0
Id		RW	Field	Value Id	Va	alue							De	scri	iptic	n																		
Α		RW	VALRDY_STOP										Sh	orto	cut k	etv	wee	n V	ALR	DY	eve	nt a	and	STC	P ta	sk								
													Se	e <i>E</i> \	/EN	TS_	VAL	RD	Y ar	nd 7	ASI	KS	TO	P										
				Disabled	0								Dis	abl	e sh	ort	cut																	
				Enabled	1								En	able	e sh	orto	cut																	

26.3.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31	1 30	29	2	8 2	7 :	26	25	24	23	22	2 21	L 20	19	9 1	8 :	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	C	0)	0	0	0	0	0	0	0	0	C)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	•							De	SCI	ript	ion																					
Α	RW	VALRDY											W	rite	'1'	to	Ena	able	ii e	nte	rru	pt ·	for	VA	LRE	PΥ	ver	nt									
													Se	e E	VEI	NTS.	_V	ALF	RD'	Υ																	
			Set	1									En	ab	le																						
			Disabled	0									Re	ad	: Di	sab	led																				
			Enabled	1									Re	ad	: En	abl	ed																				

26.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	iumbe	r		31	. 30	29	28	3 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																																	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	on																		
Α	RW	VALRDY										Wri	ite '	'1' t	o D	isa	ble	inte	erru	ıpt	for	VAI	.RD	ev /	ent								
												See	EV	'EN	TS_	VA	LRD	Υ															
			Clear	1								Disa	able	е																			
			Disabled	0								Rea	id: I	Disa	able	ed																	
			Enabled	1								Rea	id:	Ena	ble	d																	

26.3.4 CONFIG

Address offset: 0x504 Configuration register

Bit	numbe	r		33	1 30	29	28	3 27	26	5 25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	•						De	escr	ipti	on																			
Α	RW	DERCEN										Bia	as c	orre	ecti	on																		
			Disabled	0								Di	sab	led																				
			Enabled	1								En	abl	ed																				

26.3.5 VALUE

Address offset: 0x508

Output random number



Bit	numb	er		31	30 29	28 2	27 26	25 2	24 2	3 22	2 21	20	19 1	8 17	⁷ 16	15	14 1	3 12	11	10 9	8	7	6	5	4	3 2	1	0
Id																						Α	Α	Α	Α	А А	Α	Α
Res	et 0x	00000000		0	0 0	0	0 0	0	0 (0	0	0	0	0 0	0	0	0 (0	0	0 0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	ue				D	esc	ripti	on																
Δ	R	VΔITIE		٠ 10	2551				G	ene	rate	d ra	ndo	m nı	ımh	er												

26.4 Electrical specification

26.4.1 RNG Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{RNG}	Run current, CPU sleeping.		500		μΑ
t _{RNG,START}	Time from setting the START task to generation begins. This is		128		μs
	a one-time delay on START signal and does not apply between				
	samples.				
t _{RNG,RAW}	Run time per byte without bias correction. Uniform distribution		30		μs
	of 0 and 1 is not guaranteed.				
t _{RNG,BC}	Run time per byte with bias correction. Uniform distribution		120		μs
	of 0 and 1 is guaranteed. Time to generate a byte cannot be				
	guaranteed.				



27 TEMP — Temperature sensor

The temperature sensor measures die temperature over the temperature range of the device. Linearity compensation can be implemented if required by the application.

Listed here are the main features for TEMP:

- Temperature range is greater than or equal to operating temperature of the device
- Resolution is 0.25 degrees

TEMP is started by triggering the START task.

When the temperature measurement is completed, a DATARDY event will be generated and the result of the measurement can be read from the TEMP register.

To achieve the measurement accuracy stated in the electrical specification, the crystal oscillator must be selected as the HFCLK source, see *CLOCK* — *Clock control* on page 101 for more information.

When the temperature measurement is completed, TEMP analog electronics power down to save power.

TEMP only supports one-shot operation, meaning that every TEMP measurement has to be explicitly started using the START task.

27.1 Registers

Table 52: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000C000	TEMP	TEMP	Temperature sensor	

Table 53: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start temperature measurement
TASKS_STOP	0x004	Stop temperature measurement
EVENTS_DATARDY	0x100	Temperature measurement complete, data ready
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
TEMP	0x508	Temperature in °C (0.25° steps)
A0	0x520	Slope of 1st piece wise linear function
A1	0x524	Slope of 2nd piece wise linear function
A2	0x528	Slope of 3rd piece wise linear function
A3	0x52C	Slope of 4th piece wise linear function
A4	0x530	Slope of 5th piece wise linear function
A5	0x534	Slope of 6th piece wise linear function
ВО	0x540	y-intercept of 1st piece wise linear function
B1	0x544	y-intercept of 2nd piece wise linear function
B2	0x548	y-intercept of 3rd piece wise linear function
B3	0x54C	y-intercept of 4th piece wise linear function
B4	0x550	y-intercept of 5th piece wise linear function
B5	0x554	y-intercept of 6th piece wise linear function
то	0x560	End point of 1st piece wise linear function
T1	0x564	End point of 2nd piece wise linear function
T2	0x568	End point of 3rd piece wise linear function
T3	0x56C	End point of 4th piece wise linear function
T4	0x570	End point of 5th piece wise linear function



27.1.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	iumbe	er		31	1 30	29	28	8 2	7 2	6 2	5 2	4 2	23 2	22	21	20	19	18	1	7 1	6 1	15 :	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	0	0) () () (0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue								Des	cri	pti	on																					
Α	RW	DATARDY										١	Wri	te '	1'1	to E	na	ble	in	teri	up	t f	or I	DAT	ΓAR	DY	ev	ent									
												S	See	ΕV	ΈN	TS_	DA	ΙTΑ	RD	γ																	
			Set	1								E	Ena	ble	:																						
			Disabled	0								F	Rea	d:	Dis	able	ed																				
			Enabled	1								F	Rea	d:	Ena	ble	ed																				

27.1.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	iumbe	r		31	1 30	29	28	3 27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue	:						De	scr	ipti	ion																			
Α	RW	DATARDY										W	rite	'1'	to I	Disa	ble	int	err	upt	for	DA	TAF	RDY	eve	ent								
												Se	e <i>E</i>	VEN	VTS_	_DA	TA	RD	Y															
			Clear	1								Dis	sab	le																				
			Disabled	0								Re	ad:	Dis	sabl	ed																		
			Enabled	1								Re	ad:	En	abl	ed																		

27.1.3 TEMP

Address offset: 0x508

Temperature in °C (0.25° steps)

Bit	numbe	er		31	30	29	28	27	26	25 :	24	23	22 2	1 2	20 1	9 1	.8 1	7 1	.6 1	L5 1	14 1	3 12	2 11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	A	Δ ,	Δ ,	4 Α	۸ ۸	Α.	A A	A	Α	Α	Α	Α	Α	A	A A	Δ Α	A A	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 (0 (0 (0 (0 (0 (0 (0	0 (0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																		
Α	R	TEMP										Ten	nper	atu	ıre i	in °0	C (0	.25	° st	eps	s)												
													ult o										Die	tem	per	atu	re ii	n °C	, 2's	5			
												Dec	isio	n p	oint	:: D	ΑTΑ	(RD	Υ														

27.1.4 A0

Address offset: 0x520

Slope of 1st piece wise linear function

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 1	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id				A A A A	
Reset 0x00000320		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1	. 0 0 1 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW A0			Slope of 1st piece wise line	ar function	

27.1.5 A1

Address offset: 0x524



Slope of 2nd piece wise linear function

Е	Bit nur	mbe	r			31	30 2	9 2	28 2	7 26	25	24	23	22 2	21 2	0 1	9 18	3 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2	1 0	ı
10	d																						Þ	A	Α	Α	Α	Α	Α	Α	Α	A A	А А	ı
F	leset	0x0	0000343			0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	1	1	0	1	0	0	0	0	1 1	ı
1	d R	RW	Field	Va	alue Id	Val	lue						Des	scrip	tio	n																		l
A	A P	RW	A1										Slo	pe o	f 2r	nd p	iece	wis	e li	nea	r fu	ncti	on											

27.1.6 A2

Address offset: 0x528

Slope of 3rd piece wise linear function

Bit	numb	er			31	30 2	9 2	8 27	26	25 2	24	23 2	22 2	1 20	19	18	17	16	15 :	14 1	.3 1	2 11	. 10	9	8	7	6	5	4	3	2 1	. 0
Id																						Α	Α	Α	Α	Α	Α	Α	Α	Α	Δ Δ	A
Res	et 0x	000003	5D		0	0 (0	0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 0	0	0	1	1	0	1	0	1	1	1 0	1
Id	RW	Field		Value Id	Va	lue						Des	crip	tion																		
Α	RW	Α2										Slon	e of	f 3rc	l nie	ce v	vise	lin	ear	fun	rtior	1										

27.1.7 A3

Address offset: 0x52C

Slope of 4th piece wise linear function

Bi	t nı	ımb	er		31	30	29 :	28 2	7 26	5 25	24	23	22	21	20	19	18 :	17 :	16 :	15 :	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																							A	A	Α	Α	Α	Α	Α	Α	Α	A A	A A
R	eset	t Ox(0000400		0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	1	0	0	0	0	0	0	0	0 (0 0
Id		RW	Field	Value Id	Va	lue						De	scri	ptic	on																		
Α		RW	A3									Slo	ne	of 4	th i	oiec	e w	ise	line	ar	fun	ctio	n										

27.1.8 A4

Address offset: 0x530

Slope of 5th piece wise linear function

Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 1	1109876543210
Id			,	A A A A A A A A A A A
Reset 0x0000047F		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 0 0 0 1 1 1 1 1 1 1
Id RW Field	Value Id	Value	Description	
A RW A4			Slope of 5th piece wise linear function	

27.1.9 A5

Address offset: 0x534

Slope of 6th piece wise linear function

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id			A A A	A A A A A A A A
Reset 0x0000037B		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1 1 0 1 1 1 1 0 1 1
ld RW Field	Value Id	Value	Description	
A RW A5			Slope of 6th piece wise linear function	

27.1.10 B0

Address offset: 0x540

y-intercept of 1st piece wise linear function



Bitı	numbe	er		31	30 2	9 2	28 2	27 20	5 25	5 24	23	22	21 :	20 1	L9 1	8 1	7 1	6 15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	4 Δ	A	Α
Res	et 0x0	0003FCC		0	0 ()	0	0 0	0	0	0	0	0	0	0 (0 (0	0	0	1	1	1	1	1	1	1	1	0	0	1 1	. 0	0
Id	RW	Field	Value Id	Va	ue						De	scri	ptio	n																		
Α	RW	В0									y-i	nter	сер	t of	1st	pie	ce v	vise	line	ar f	unc	tior	1									

27.1.11 B1

Address offset: 0x544

y-intercept of 2nd piece wise linear function

Bit num	nber		31	30 2	29 2	28 2	7 26	25	24	23 2	22 2	1 20	0 19	18	17	16	15 :	14 1	3 1	2 11	10	9	8	7	6	5	4	3 2	2 1	0
Id																		1	Δ Α	A	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Reset 0	x00003F98		0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 :	L 1	. 1	1	1	1	1	0	0	1	1 (0	0
Id R	W Field	Value Id	Va	lue						Des	crip	tion	ı																	
A R	W B1								,	y-in	terc	ept	of 2	nd	piec	e w	ise	inea	ar fu	ınct	ion									

27.1.12 B2

Address offset: 0x548

y-intercept of 3rd piece wise linear function

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19	18	17	16	15	14 :	13	12 :	11	10	9	8	7	6	5	4	3	2	1 ()
Id																						Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Δ,	A	4
Res	et 0x0	0003F98		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	1	0 (0 ()
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																				
Α	RW	B2										y-ir	iter	сер	t of	f 3r	d p	iece	e wi	se l	ine	ar f	unc	tio	n										-

27.1.13 B3

Address offset: 0x54C

y-intercept of 4th piece wise linear function

Bit r	umbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id																						Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	۱ ۸	А А
Res	et 0x0	0000012		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0 ()	1 0
Id	RW	Field	Value Id	Va	alue							Des	cri	otic	n																			
Α	RW	В3										y-ir	iter	cep	t o	f 4t	h p	iece	e w	ise l	ine	ar f	uno	tio	n									

27.1.14 B4

Address offset: 0x550

y-intercept of 5th piece wise linear function

Bit	numb	er		31 3	30 29	28	3 27	26	25 2	24 2	3 22	2 21	20	19 1	8 1	7 16	5 15	14	13	12 1	.1 1) 9	8	7	6	5	4	3 2	1	0
Id																			Α	Α.	Δ Δ	A	Α	Α	Α	Α	Α	АА	A	Α
Res	et 0x0	000006A		0	0 0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0	0	0	0	0	1	1	0	1 0	1	0
Id	RW	Field	Value Id	Valu	ıe					C	esc	ripti	on																	
Α	RW	B4								У	-inte	erce	pt o	f 5th	pie	ce v	vise	line	ar f	unc	ion									

27.1.15 B5

Address offset: 0x554

y-intercept of 6th piece wise linear function

Bi	t nı	umb	er		31 30 29 28 27	26	25 2	4 23	22	21 2	0 19	18	17	16	15	14 1	.3 1	.2 1:	10	9	8	7	6	5	4	3	2	1 0
Id																,	Δ ,	4 Д	Α	Α	Α	Α	Α	Α	Α	Α	A	А А
R	ese	t Ox	0003DD0		0 0 0 0 0	0	0 (0 0	0	0 (0	0	0	0	0	0	1 :	1 1	1	0	1	1	1	0	1	0	0 (0 0
Id		RW	Field	Value Id	Value			De	escri	ptior	,																	
Α		RW	B5					y-i	inter	cept	of 6	th p	oiece	e w	ise l	inea	ır fu	ıncti	on									

y-intercept of 6th piece wise linear function



27.1.16 TO

Address offset: 0x560

End point of 1st piece wise linear function

Bit nu	ımber		31 30 29 28 27	⁷ 26 25 24 23 22 21 20 19 1	.8 17 16 15 14 13 12 1	11 10 9 8	7 6	5 4	3	2 1	0
Id							А А	A A	A	А А	Α
Reset	0x000000E2		0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0	1 1	1 (0	0 1	0
Id	RW Field	Value Id	Value	Description							
Α	RW TO			End point of 1st n	iece wise linear functio	าท					

27.1.17 T1

Address offset: 0x564

End point of 2nd piece wise linear function

Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	00000000
Id RW Field	Value Id	Value	Description		
A RW T1			End point of 2nd pie	ce wise linear function	

27.1.18 T2

Address offset: 0x568

End point of 3rd piece wise linear function

Bit	numbe	er		31	30 2	9 :	28	27 2	26 2	25 2	24	23 :	22 2	21 2	20 1	9 1	8 1	7 16	15	14	13	12 :	1 1	0 9	8	7	6	5	4	3	2 :	1 0
Id																										Α	Α	Α	Α	Α .	Δ ,	A A
Res	et 0x0	0000014		0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0	1	0	1 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	RW	T2										End	poi	int (of 3	rd p	iec	e wi	se li	nea	r fu	ncti	on									

27.1.19 T3

Address offset: 0x56C

End point of 4th piece wise linear function

Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0			
Id			A A A A A A A A			
Reset 0x00000019		0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $			
ld RW Field	Value Id	Value	Description			
A RW T3		End point of 4th piece wise linear function				

27.1.20 T4

Address offset: 0x570

End point of 5th piece wise linear function

Bit number		31 30 29 28 23	7 26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0			
Id					A A A A A A A			
Reset 0x00000050		0 0 0 0 0	0000000000	000000000	0 1 0 1 0 0 0 0			
Id RW Field	Value Id	Value	Description					
A RW T4		End point of 5th piece wise linear function						

End point of 5th piece wise linear function



27.2 Electrical specification

27.2.1 Temperature Sensor Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t_{TEMP}	Time required for temperature measurement		36		μs
T _{TEMP,RANGE}	Temperature sensor range	-40		85	°C
T _{TEMP,ACC}	Temperature sensor accuracy	-5		5	°C
T _{TEMP,RES}	Temperature sensor resolution		0.25		°C
T _{TEMP,STB}	Sample to sample stability at constant device temperature		+/-0.25		°C
T _{TEMP,OFFST}	Sample offset at 25°C	-2.5		2.5	°C



28 ECB — AES electronic codebook mode encryption

The AES electronic codebook mode encryption (ECB) can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. The ECB encryption block supports 128 bit AES encryption (encryption only, not decryption).

AES ECB operates with EasyDMA access to system Data RAM for in-place operations on cleartext and ciphertext during encryption. ECB uses the same AES core as the CCM and AAR blocks and is an asynchronous operation which may not complete if the AES core is busy.

AES ECB features:

- 128 bit AES encryption
- Supports standard AES ECB block encryption
- Memory pointer support
- · DMA data transfer

AES ECB performs a 128 bit AES block encrypt. At the STARTECB task, data and key is loaded into the algorithm by EasyDMA. When output data has been written back to memory, the ENDECB event is triggered.

AES ECB can be stopped by triggering the STOPECB task.

28.1 Shared resources

The ECB, CCM, and AAR share the same AES module. The ECB will always have lowest priority and if there is a sharing conflict during encryption, the ECB operation will be aborted and an ERRORECB event will be generated.

28.2 EasyDMA

The ECB implements an EasyDMA mechanism for reading and writing to the Data RAM. This DMA cannot access the program memory or any other parts of the memory area except RAM.

If the ECBDATAPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The EasyDMA will have finished accessing the Data RAM when the ENDECB or ERRORECB is generated.

28.3 ECB data structure

Input to the block encrypt and output from the block encrypt are stored in the same data structure. ECBDATAPTR should point to this data structure before STARTECB is initiated.

Table 54: ECB data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
CLEARTEXT	16	16 byte AES cleartext input block
CIPHERTEXT	32	16 byte AES ciphertext output block



28.4 Registers

Table 55: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000E000	ECB	ECB	AES Electronic Code Book (ECB) mode	
			block encryption	

Table 56: Register Overview

Register	Offset	Description
TASKS_STARTECB	0x000	Start ECB block encrypt
TASKS_STOPECB	0x004	Abort a possible executing ECB operation
EVENTS_ENDECB	0x100	ECB block encrypt complete
EVENTS_ERRORECB	0x104	ECB block encrypt aborted because of a STOPECB task or due to an error
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ECBDATAPTR	0x504	ECB block encrypt memory pointers

28.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	r		31	30 :	29 2	28 2	7 2	6 2	5 24	4 2	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																																В	Α
Res	et 0x0	0000000		0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Val	ue						D	escr	ipti	on																			
Α	RW	ENDECB									W	/rite	'1'	to E	nal	ole i	inte	rru	pt 1	or I	NE	EC	B e	ven	t								
											Se	ee <i>E</i>	VEN	ITS_	EN	DEC	СВ																
			Set	1							E	nabl	e																				
			Disabled	0							R	ead:	Dis	able	ed																		
			Enabled	1							R	ead:	Ena	able	ed																		
В	RW	ERRORECB									W	/rite	'1'	to E	nal	ole i	inte	rru	pt 1	or I	RR	OR	ECE	ev	ent								
											Se	ee <i>E</i> '	VEN	ITS_	ER	ROF	REC	8															
			Set	1							E	nabl	е																				
			Disabled	0							R	ead:	Dis	able	ed																		
			Enabled	1							R	ead:	Ena	able	ed																		

28.4.2 INTENCLR

Address offset: 0x308 Disable interrupt

Bit n	umbe	r		31	1 30	29	28	27	26	25	24 2	23 2:	2 21	1 20	19	18	17	16	15	14 1	3 1	2 11	10	9	8	7	6	5 4	3	2	1 ()
Id																															В	l.
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0 ()
Id	RW	Field	Value Id	Va	alue						ı	Desc	ript	ion																		
Α	RW	ENDECB									١	Write	e '1'	to [Disa	ble	int	erru	pt 1	or E	NDI	ECB	evei	nt								
											9	See E	VEI	NTS_	_EN	DE	СВ															
			Clear	1							ı	Disab	le																			
			Disabled	0							ı	Read	: Di	sabl	ed																	
			Enabled	1							ı	Read	: En	able	ed																	
В	RW	ERRORECB									١	Write	· '1'	to [Disa	ble	int	erru	pt 1	for E	RRC	OREC	CB e	ven	t							
											9	See E	VEI	NTS_	_ER	ROI	REC	В														
			Clear	1							ı	Disab	le																			
			Disabled	0							ı	Read	: Di	sabl	ed																	



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 1	.6 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id					ВА
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	Enabled	1	Read: Enabled		

28.4.3 ECBDATAPTR

Address offset: 0x504

ECB block encrypt memory pointers

Bit r	numb	er		31	. 30	29	28	27 :	26	25	24	23 :	22 2	1 20	19	18	17	16 :	15 1	14 1	3 12	2 11	. 10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α.	Α	Α	Α	Α.	Α /	4 A	. A	Α	Α	Α	Α	Α	Α	Α	A A		A A
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							Des	crip	tion																		
Α	RW	ECBDATAPTR										Poi	nter	to t	he E	СВ	data	str	uct	ure	(see	Tal	ole 1	L EC	Вd	ata						
												stru	ıctur	e ov	/ervi	iew))															

28.5 Electrical specification

28.5.1 ECB Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{ECB}	Run time per 16 byte block in all modes		6		μs



29 CCM — AES CCM mode encryption

Cipher block chaining - message authentication code (CCM) mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication. The CCM terminology "Message authentication code (MAC)" is called the "Message integrity check (MIC)" in 'Bluetooth terminology and also in this document.

The CCM block generates an encrypted keystream that is applied to input data using the XOR operation and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the Radio. All operations can complete within the packet RX or TX time. CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF *RFC3610*, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in *NIST Special Publication 800-38C*. The *Bluetooth* specification describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

The AES CCM supports three operations: key-stream generation, packet encryption, and packet decryption. All these operations are done in compliance with the *Bluetooth* specification. ²³A new key-stream must be generated before a new packet encryption or packet decryption operation can be started.

A key-stream is generated by triggering the KSGEN task. An ENDKSGEN event will be generated when the new key-stream has been generated. The key-stream will be stored in the AES CCM's temporary memory area, specified by the SCRATCHPTR, where it will be used in subsequent encryption and decryption operations.

Encryption is started by triggering the CRYPT task with the MODE register set to ENCRYPTION. Similarly, decryption is started by triggering the same task with MODE set to DECRYPTION. An ENDCRYPT event will be generated when packet encryption is completed as well as when packet decryption is completed, see *Figure 59: Key-stream generation followed by encryption or decryption. The shortcut is optional.* on page 267.

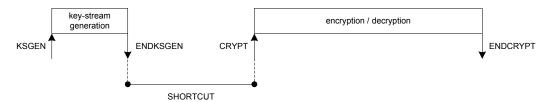


Figure 59: Key-stream generation followed by encryption or decryption. The shortcut is optional.

Key-stream generation, packet encryption, and packet decryption operations utilize the configuration specified in the data structure pointed to by the CNFPTR pointer. It is necessary to configure this pointer and its underlying data structure, and the MODE register before the KSGEN task is triggered. It is also necessary to configure the INPTR pointer and the OUTPTR pointer before the CRYPT task is triggered.

If a shortcut is used between ENDKSGEN event and CRYPT task, the INPTR pointer and the OUTPTR pointer must be configured before the KSGEN task is triggered.

The AES CCM supports different packet lengths, this is configured via the PACKETLENGTH field in the MODE register.

²³ Bluetooth AES CCM 128 bit block encryption, see Bluetooth Core specification Version 4.0.



29.1 Shared resources

The CCM shares registers and other resources with other peripherals that have the same ID as the CCM. The user must therefore disable all peripherals that have the same ID as the CCM before the CCM can be configured and used.

Disabling a peripheral that have the same ID as the CCM will not reset any of the registers that are shared with the CCM. It is therefore important to configure all relevant CCM registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

29.2 Encryption

During packet encryption, the AES CCM will read the unencrypted packet located in RAM at the address specified in the INPTR pointer, encrypt the packet and append a four byte long Message Integrity Check (MIC) field to the packet.

The AES CCM will also modify the length field of the packet to adjust for the appended MIC field, that is, add four bytes to the length, and store the resulting packet back into RAM at the address specified in the OUTPTR pointer, see *Figure 60: Encryption* on page 268.

Empty packets (length field is set to 0) will not be encrypted but instead moved unmodified through the AES CCM.

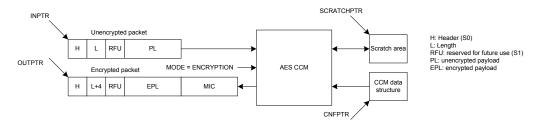


Figure 60: Encryption

29.3 Decryption

During packet decryption, the AES CCM will read the encrypted packet located in RAM at the address specified in the INPTR pointer, decrypt the packet, authenticate the packet's MIC field and generate the appropriate MIC status.

The AES CCM will also modify the length field of the packet to adjust for the MIC field, that is, subtract four bytes from the length, and then store the decrypted packet into RAM at the address pointed to by the OUTPTR pointer, see *Figure 61: Decryption* on page 269.

The CCM is only able to decrypt packets that are at least 5 bytes long, that is, 1 byte or more encrypted payload (EPL) and 4 bytes of MIC. The CCM will therefore generate a MIC error for packets where the length field is set to 1, 2, 3 or 4.

Empty packets (length field is set to 0) will not be decrypted but instead moved unmodified through the AES CCM, these packets will always pass the MIC check.



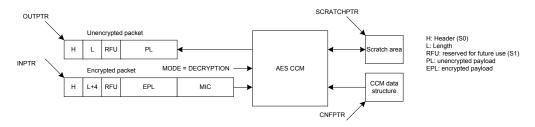


Figure 61: Decryption

29.4 AES CCM and RADIO concurrent operation

The AES CCM is designed to run in parallel with the RADIO to enable on-the-fly encryption and decryption of RADIO packets without CPU involvement. To facilitate this, the RADIO has to be configured with specific settings.

Table 57: Radio configuration settings

Dadia assessatas	Malara	Description
Radio parameter	Value	Description
PCNF0.S0LEN	1	Length of HEADER field in: Table 59: Data structure for unencrypted packet on page 271 and Table
		60: Data structure for encrypted packet on page 271.
PCNF0.LFLEN	5 or 8	Length of LENGTH field in: Table 59: Data structure for unencrypted packet on page 271 and Table
		60: Data structure for encrypted packet on page 271.
PCNF0.S1LEN	3 or 0	Length of the RFU field in: Table 59: Data structure for unencrypted packet on page 271 and Table
		60: Data structure for encrypted packet on page 271. The combined length of LENGTH and RFU
		must always be 8 bit.
PCNF0.S1	Include	Always include the S1 field (RFU field) in RAM to secure that the same data structure can be used
		for PCNF0.S1LEN = 3 and PCNF0.S1LEN = 0: Table 59: Data structure for unencrypted packet on page
		271 and Table 60: Data structure for encrypted packet on page 271.
MODE	Ble_1Mbit	Data rate. Must match CCM->MODE.DATARATE
PCNF1.BALEN	3	Length of address (32 bit)
CRCCNF.LEN	3	Length of CRC (24 bit)

29.5 Encrypting packets on-the-fly in radio transmit mode

When the AES CCM is encrypting a packet on-the-fly at the same time as the RADIO is transmitting it, the RADIO must read the encrypted packet from the same memory location as the AES CCM is writing to.

The OUTPTR pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 62: Configuration of on-the-fly encryption* on page 269.

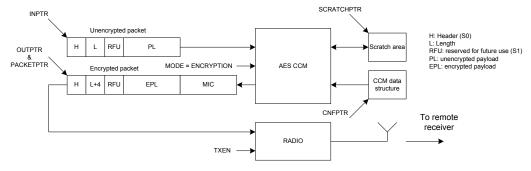


Figure 62: Configuration of on-the-fly encryption

In order to match the RADIO's timing, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered, in addition the shortcut between the ENDKSGEN event and the CRYPT task must be enabled. This use-case is illustrated in *Figure 63: On-the-fly encryption using a PPI connection* on page 270 using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM.



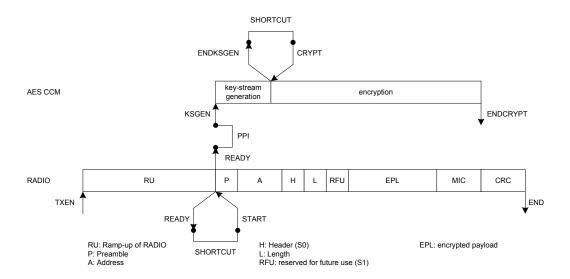


Figure 63: On-the-fly encryption using a PPI connection

29.6 Decrypting packets on-the-fly in radio receive mode

When the AES CCM is decrypting a packet on-the-fly at the same time as the RADIO is receiving it, the AES CCM must read the encrypted packet from the same memory location as the RADIO is writing to.

The INPTR pointer in the AES CCM must therefore point to the same memory location as the PACKETPTR pointer in the RADIO, see *Figure 64: Configuration of on-the-fly decryption* on page 270.

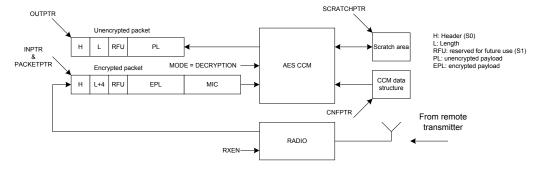


Figure 64: Configuration of on-the-fly decryption

In order to match the RADIO's timing, the KSGEN task must be triggered no later than when the START task in the RADIO is triggered. In addition, the CRYPT task must be triggered no earlier than when the ADDRESS event is generated by the RADIO.

If the CRYPT task is triggered exactly at the same time as the ADDRESS event is generated by the RADIO, the AES CCM will guarantee that the decryption is completed no later than when the END event in the RADIO is generated.

This use-case is illustrated in *Figure 65: On-the-fly decryption using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM* on page 271 using a PPI connection between the ADDRESS event in the RADIO and the CRYPT task in the AES CCM. The KSGEN task is triggered from the READY event in the RADIO through a PPI connection.



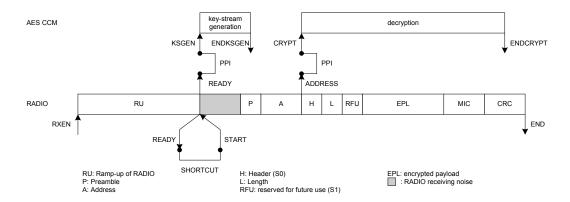


Figure 65: On-the-fly decryption using a PPI connection between the READY event in the RADIO and the KSGEN task in the AES CCM

29.7 CCM data structure

The CCM data structure is located in Data RAM at the memory location specified by the CNFPTR pointer register.

Table 58: CCM data structure overview

Property	Address offset	Description
KEY	0	16 byte AES key
PKTCTR	16	Octet0 (LSO) of packet counter
	17	Octet1 of packet counter
	18	Octet2 of packet counter
	19	Octet3 of packet counter
	20	Bit 6 – Bit 0: Octet4 (7 most significant bits of packet counter, with Bit 6 being the most significant
		bit) Bit7: Ignored
	21	Ignored
	22	Ignored
	23	Ignored
	24	Bit 0: Direction bit Bit 7 – Bit 1: Zero padded
IV	25	8 byte initialization vector (IV) Octet0 (LSO) of IV, Octet1 of IV,, Octet7 (MSO) of IV

The NONCE vector (as specified by the *Bluetooth* Core Specification) will be generated by hardware based on the information specified in the CCM data structure from *Table 58: CCM data structure overview* on page 271.

Table 59: Data structure for unencrypted packet

Property	Address offset	Description
HEADER	0	Packet Header
LENGTH	1	Number of bytes in unencrypted payload
RFU	2	Reserved Future Use
PAYLOAD	3	Unencrypted payload

Table 60: Data structure for encrypted packet

Property	Address offset	Description					
HEADER	0	Packet Header					
LENGTH	1	Number of bytes in encrypted payload including length of MIC					
		Important: LENGTH will be 0 for empty packets since the MIC is not added to empty					
		packets					
RFU	2	Reserved Future Use					
PAYLOAD	3	Encrypted payload					
MIC	3 + payload length	ENCRYPT: 4 bytes encrypted MIC					



Property	Address offset	Description
----------	----------------	-------------

Important: MIC is not added to empty packets

29.8 EasyDMA and ERROR event

The CCM implements an EasyDMA mechanism for reading and writing to the RAM.

In some scenarios where the CPU and other DMA enabled peripherals are accessing the RAM at the same time, the CCM DMA could experience some bus conflicts which may also result in an error during encryption. If this happens, the ERROR event will be generated.

The EasyDMA will have finished accessing the RAM when the ENDKSGEN and ENDCRYPT events are generated.

If the CNFPTR, SCRATCHPTR, INPTR and the OUTPTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

29.9 Registers

Table 61: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x4000F000	CCM	CCM	AES CCM Mode Encryption		

Table 62: Register Overview

Register	Offset	Description
TASKS_KSGEN	0x000	Start generation of key-stream. This operation will stop by itself when completed.
TASKS_CRYPT	0x004	Start encryption/decryption. This operation will stop by itself when completed.
TASKS_STOP	0x008	Stop encryption/decryption
EVENTS_ENDKSGEN	0x100	Key-stream generation complete
EVENTS_ENDCRYPT	0x104	Encrypt/decrypt complete
EVENTS_ERROR	0x108	CCM error event
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
MICSTATUS	0x400	MIC check result
ENABLE	0x500	Enable
MODE	0x504	Operation mode
CNFPTR	0x508	Pointer to data structure holding AES key and NONCE vector
INPTR	0x50C	Input pointer
OUTPTR	0x510	Output pointer
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

29.9.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	pti	on																				
Α	RW	ENDKSGEN_CRYPT										Sho	orto	ut l	bet	we	en I	ENE	OKS	GEI	۷e	ven	t an	d C	RYP	T ta	ask								
												See	e EN	/EN	TS_	EN	IDK.	SGE	N a	and	TA.	SKS	_CF	ΥP	г										
			Disabled	0								Dis	abl	e sł	nor	tcut	t																		
			Enabled	1								Ena	able	e sh	ort	cut																			



29.9.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31 30 29 28 27	26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id						СВА
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value		Description
Α	RW	ENDKSGEN				Write '1' to Enable interrupt for ENDKSGEN event
						See EVENTS_ENDKSGEN
			Set	1		Enable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
В	RW	ENDCRYPT				Write '1' to Enable interrupt for ENDCRYPT event
						See EVENTS_ENDCRYPT
			Set	1		Enable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled
С	RW	ERROR				Write '1' to Enable interrupt for ERROR event
						See EVENTS_ERROR
			Set	1		Enable
			Disabled	0		Read: Disabled
			Enabled	1		Read: Enabled

29.9.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Res	et 0x00000000		0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW Field	Value Id	Value	Description
Α	RW ENDKSG	EN		Write '1' to Disable interrupt for ENDKSGEN event
				See EVENTS_ENDKSGEN
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW ENDCRY	PT		Write '1' to Disable interrupt for ENDCRYPT event
				See EVENTS_ENDCRYPT
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ERROR			Write '1' to Disable interrupt for ERROR event
				See EVENTS_ERROR
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

29.9.4 MICSTATUS

Address offset: 0x400 MIC check result



Bi	t numl	per		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A
Re	set 0	(00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RV	/ Field	Value Id	Value	Description
Α	R	MICSTATUS			The result of the MIC check performed during the previous
					decryption operation
			CheckFailed	0	MIC check failed
			CheckPassed	1	MIC check passed

29.9.5 ENABLE

Address offset: 0x500

Enable

Bit	nur	mbe	r		31 30	29	28	27	26	25	24	23	22 2	21 2	20 1	19 :	18 2	17 1	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		А А
Re	set	0x00	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	F	RW	Field	Value Id	Value	:						Des	crip	otio	n																			
Α	F	RW	ENABLE									Ena	ble	or (disa	ble	CC	M																
				Disabled	0							Disa	able	:																				
				Enabled	2							Ena	ble																					

29.9.6 MODE

Address offset: 0x504

Operation mode

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		C B A
Reset 0x0000001		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW MODE		The mode of operation to be used
	Encryption	0 AES CCM packet encryption mode
	Decryption	1 AES CCM packet decryption mode
B RW DATARATE		Data rate that the CCM shall run in synch with
	1Mbit	0 In synch with 1 Mbit data rate
	2Mbit	1 In synch with 2 Mbit data rate
C RW LENGTH		Packet length configuration
	Default	0 Default length. Effective length of LENGTH field is 5-bit
	Extended	1 Extended length. Effective length of LENGTH field is 8-bit

29.9.7 CNFPTR

Address offset: 0x508

Pointer to data structure holding AES key and NONCE vector

Bit	number		31	30	29	28	27	7 26	25	24	23	22	21	20 1	L9 1	8 1	7 16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	1	0
Id			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	ДД	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	et 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
											n-			_																		
ld	RW Field	Value Id	Va	llue							Des	scri	ptic	n																		
A	RW Field RW CNFPTR	Value Id	Va	iiue											da	ta st	ruct	ture	ho	ldin	g th	e A	ES I	key	an	d tł	ne (CCN	Λ			

29.9.8 INPTR

Address offset: 0x50C

Input pointer



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field Value Id	Value Description
A RW INPTR	Input pointer

29.9.9 OUTPTR

Address offset: 0x510

Output pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW OUTPTR		Output pointer

29.9.10 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit	numbe	er		31	1 30	29	28 2	7 20	5 25	24	23	22 2	21 2	0 19	18	17	16	15	14 1	13 1	2 13	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α ,	Д Д	А	Α	Α	Α .	A A	A	Α	Α	Α	Α	Α	A A	A A	Α	Α	Α	Α	Α	Α	Α	A A	A A	Α
Res	et 0x0	0000000		0	0	0	0 (0 0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	alue						De	scrip	tion	ı																	
Α	RW	SCRATCHPTR									Ро	inter	to a	scr	atch	n da	ta a	area	use	d fo	or te	npo	rar	y sto	orag	ge					
											du	ring l	key-	stre	am	gen	era	tion	, M	IC g	ener	atio	n ar	nd e	ncr	ypti	ion	/			
											de	crypt	ion.																		
											Th	e scr	a+ah	250			4 f.			0 50	t			f da							
											1111	e scr	attn	are	d IS	use	u ic	א זכ	amp	Orai	ry St	or ag	e o	ı uaı	ld U	urn	ng				
											key	y-stre	eam	gen	era	tion	an	d er	ncry	ptio	n.										
											A s	pace	of 4	13 b	ytes	s, or	(16	î + î	MAX	(PAC	CKET	SIZE) by	rtes,	wł	nate	eve	r			
											is I	arge	st m	nust	he	rese	rve	d ir	nRΔ	М											
											15 1	arge	st, 11	iust	be	rese	i ve	eu II	IKA	IVI.											



30 AAR — Accelerated address resolver

Accelerated address resolver is a cryptographic support function for implementing the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core specification* v4.0. "Resolvable private address generation" should be achieved using ECB and is not supported by AAR.

The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address. The AAR block enables real-time address resolution on incoming packets when configured as described in this chapter. This allows real-time packet filtering (whitelisting) using a list of known shared keys (Identity Resolving Keys (IRK) in *Bluetooth*).

30.1 Shared resources

The AAR shares registers and other resources with the peripherals that have the same ID as the AAR. The user must therefore disable all peripherals that have the same ID as the AAR before the AAR can be configured and used.

Disabling a peripheral that have the same ID as the AAR will not reset any of the registers that are shared with the AAR. It is therefore important to configure all relevant AAR registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

30.2 EasyDMA

The AAR implements EasyDMA for reading and writing to the RAM. The EasyDMA will have finished accessing the RAM when the END, RESOLVED, and NOTRESOLVED events are generated.

If the IRKPTR, ADDRPTR and the SCRATCHPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

30.3 Resolving a resolvable address

As per Bluetooth specification, a private resolvable address is composed of six bytes.

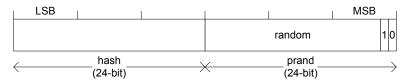


Figure 66: Resolvable address

To resolve an address the ADDRPTR register must point to the start of packet. The resolver is started by triggering the START task. A RESOLVED event is generated when the AAR manages to resolve the address using one of the Identity Resolving Keys (IRK) found in the IRK data structure. The AAR will use the IRK specified in the register IRK0 to IRK15 starting from IRK0. How many to be used is specified by the NIRK register. The AAR module will generate a NOTRESOLVED event if it is not able to resolve the address using the specified list of IRKs.

The AAR will go through the list of available IRKs in the IRK data structure and for each IRK try to resolve the address according to the Resolvable Private Address Resolution Procedure described in the *Bluetooth* Specification²⁴. The time it takes to resolve an address may vary depending on where in the list the

Bluetooth Specification Version 4.0 [Vol 3] chapter 10.8.2.3.



resolvable address is located. The resolution time will also be affected by RAM accesses performed by other peripherals and the CPU. See the *Electrical specifications* for more information about resolution time.

The AAR will only do a comparison of the received address to those programmed in the module. And not check what type of address it actually is.

The AAR will stop as soon as it has managed to resolve the address, or after trying to resolve the address using NIRK number of IRKs from the IRK data structure. The AAR will generate an END event after it has stopped.

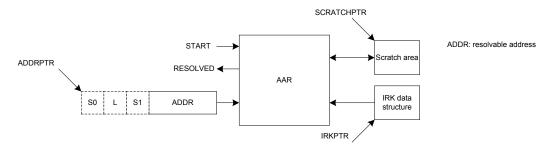


Figure 67: Address resolution with packet preloaded into RAM

30.4 Use case example for chaining RADIO packet reception with address resolution using AAR

The AAR may be started as soon as the 6 bytes required by the AAR have been received by the RADIO and stored in RAM. The ADDRPTR pointer must point to the start of packet.

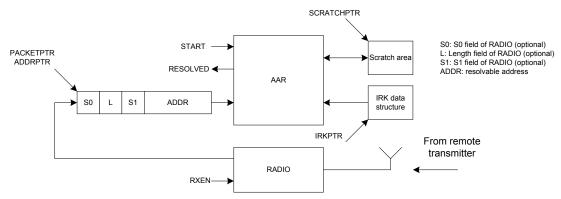


Figure 68: Address resolution with packet loaded into RAM by the RADIO

30.5 IRK data structure

The IRK data structure is located in RAM at the memory location specified by the CNFPTR pointer register.

Table 63: IRK data structure overview

Property	Address offset	Description
IRK0	0	IRK number 0 (16 - byte)
IRK1	16	IRK number 1 (16 - byte)
IRK15	240	IRK number 15 (16 - byte)



30.6 Registers

Table 64: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4000F000	AAR	AAR	Acelerated Address Resolver	

Table 65: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start resolving addresses based on IRKs specified in the IRK data structure
TASKS_STOP	0x008	Stop resolving addresses
EVENTS_END	0x100	Address resolution procedure complete
EVENTS_RESOLVED	0x104	Address resolved
EVENTS_NOTRESOLVED	0x108	Address not resolved
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Resolution status
ENABLE	0x500	Enable AAR
NIRK	0x504	Number of IRKs
IRKPTR	0x508	Pointer to IRK data structure
ADDRPTR	0x510	Pointer to the resolvable address
SCRATCHPTR	0x514	Pointer to data area used for temporary storage

30.6.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Res	et 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW RESOLVED			Write '1' to Enable interrupt for RESOLVED event
				See EVENTS_RESOLVED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW NOTRESOLVED			Write '1' to Enable interrupt for NOTRESOLVED event
				See EVENTS_NOTRESOLVED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

30.6.2 INTENCLR

Address offset: 0x308 Disable interrupt



																																_
Bitı	numbe	er		31	30	29	28	27	26 2	25 2	24 2	3 22	2 21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5 4	4 3	2	1	0
Id																														С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0 (0 0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						C	escr	ripti	on																		
Α	RW	END									٧	Vrite	'1'	to C	isal	ble	inte	erru	ıpt i	for	END	ev	ent									
											S	ee E	VEN	ITS_	ENL	D																
			Clear	1							C	Disab	le																			
			Disabled	0							R	Read	: Dis	able	ed																	
			Enabled	1							R	Read	: En	able	d																	
В	RW	RESOLVED									٧	Vrite	'1'	to D	isal	ble	inte	erru	ıpt i	for	RES	OLV	ED 6	even	t							
											S	ee E	VEN	ITS_	RES	OL	VEC)														
			Clear	1							C	Disab	le																			
			Disabled	0							R	Read:	: Dis	able	ed																	
			Enabled	1							R	Read:	: En	able	d																	
С	RW	NOTRESOLVED									٧	Vrite	'1'	to C	isal	ble	inte	erru	ıpt 1	for	NOT	RES	SOL\	/ED	ever	nt						
											S	ee E	VEN	ITS_	NO	TRE	SO	LVE	D													
			Clear	1							C	Disab	le																			
			Disabled	0							R	Read	: Dis	able	ed																	
			Enabled	1							R	Read	: En	able	d																	

30.6.3 STATUS

Address offset: 0x400

Resolution status

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААА
Reset 0x00000000		0 0 0 0 0 0	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Id RW Field	Value Id	Value	Description
A R STATUS		[015]	The IRK that was used last time an address was resolved

30.6.4 ENABLE

Address offset: 0x500

Enable AAR

Bit	numb	er			31	30	29 2	28 2	27 2	26 2	25 2	24	23	22 2	21 2	0 1	9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 1:	10	9	8	7	6	5	4	3 2	2 1	0
Id																																	Α	Α
Res	et 0x	0000	00000		0	0	0	0	0	0	0	0	0	0	0	0 () () () () () (0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	/ Fie	eld	Value Id	Val	ue							Des	crip	tio	n																		
Α	RW	/ EN	NABLE										Ena	ble	or (disa	ble	AΑ	R															
				Disabled	0								Disa	able	!																			
				Enabled	3								Ena	ble																				

30.6.5 NIRK

Address offset: 0x504

Number of IRKs

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ААААА
Reset 0x0000001		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
A RW NIRK		[116]	Number of Identity root keys available in the IRK data structure

30.6.6 IRKPTR

Address offset: 0x508



Pointer to IRK data structure

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
Id		A A A A A A A A A A A A A A A A A A A					
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0					
Id RW Field	Value Id	Value Description					
A RW IRKPTR		Pointer to the IRK data structure					

30.6.7 ADDRPTR

Address offset: 0x510

Pointer to the resolvable address

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0					
Id		A A A A A A A A A A A A A A A A A A A					
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0					
ld RW Field	Value Id	Value Description					
A RW ADDRPTR		Pointer to the resolvable address (6-bytes)					

30.6.8 SCRATCHPTR

Address offset: 0x514

Pointer to data area used for temporary storage

Bit	numb	er		3:	1 30	29	28	8 2	7 2	6 2	5 2	24 2	3 2	2 2	1 2	0 19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α Δ	Α Α	Δ /	Δ Α	Δ /	Α Α	Δ Δ	Α Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	Α	Α
Res	et 0x0	00000000		0	0	0	0	0) (0 (0 (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	V	alue	:						D	esc	ript	tion																			
Α	RW	SCRATCHPTR										Р	oin	ter	to a	scr	atc	h da	ata	area	a us	ed 1	or t	tem	noq	rary	sto	ora	ge					
												d	uriı	ng r	eso	luti	on.	A sp	ace	of	min	imu	ım :	3 by	tes	mı	ust	be						
												r	000	rve	4																			

30.7 Electrical specification

30.7.1 AAR Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{AAR,8}	Time for address resolution of 8 IRKs		48		μs



31 SPIM — Serial peripheral interface master with EasyDMA

The SPI master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus.

Listed here are the main features for the SPIM

- Three SPIM instances
- SPI mode 0-3
- EasyDMA direct transfer to/from RAM for both SPI Slave and SPI Master
- · Individual selection of IO pin for each SPI signal

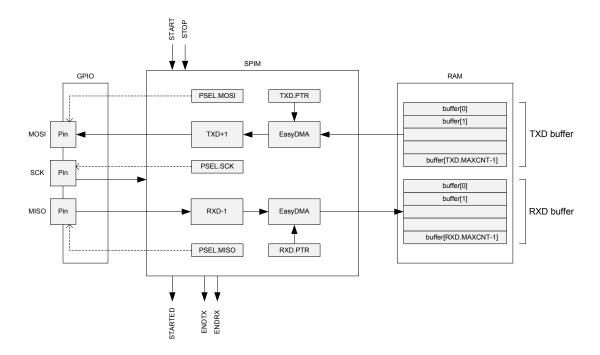


Figure 69: SPIM — SPI master with EasyDMA

The SPIM does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPIM supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 66: SPI modes

Mode	Clock polarity	Clock phase
	CPOL	СРНА
SPI_MODE	0 (Active High)	0 (Leading)
SPI_MODE	0 (Active High)	1 (Trailing)
SPI_MODE	1 (Active Low)	0 (Leading)
SPI_MODE	1 (Active Low)	1 (Trailing)

31.1 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.



Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

31.2 EasyDMA

The SPI master implements EasyDMA for reading and writing of data packets from and to the DATA RAM without CPU involvement.

The RXD.PTR and TXD.PTR point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively, see *Figure 69: SPIM* — *SPI master with EasyDMA* on page 281. RXD.MAXCNT and TXD.MAXCNT specify the maximum number of bytes allocated to the buffers.

The SPI master will automatically stop transmitting after TXD.MAXCNT bytes have been transmitted and RXD.MAXCNT bytes have been received. If TXD.MAXCNT is larger than RXD.MAXCNT, the superfluous received bytes will be ignored. If RXD.MAXCNT is larger than TXD.MAXCNT, the remaining transmitted bytes will contain the value defined in the ORC register.

If the RXD.PTR and the TXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next transmission immediately after having received the STARTED event.

The ENDRX/ENDTX event indicate that EasyDMA has finished accessing respectively the RX/TX buffer in RAM. The END event gets generated when both RX and TX are finished accessing the buffers in RAM.

31.2.1 EasyDMA list

EasyDMA supports one list type.

The supported list type is:

Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type.

For illustration, see the code example below. This data structure includes only a buffer with size equal to Channel.MAXCNT. EasyDMA will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.

The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

```
#define BUFFER_SIZE 4

typedef struct ArrayList
{
  uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type MyArrayList[3];
```



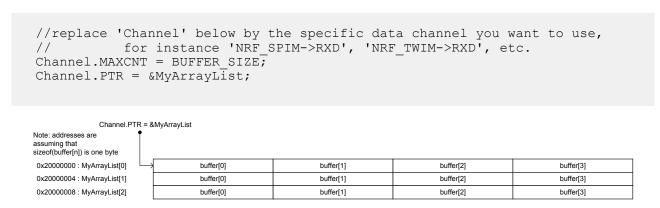


Figure 70: EasyDMA array list

31.3 SPI master transaction sequence

An SPI master transaction consists of a sequence started by the START task followed by a number of events, and finally the STOP task.

An SPI master transaction is started by triggering the START task. The ENDTX event will be generated when the transmitter has transmitted all bytes in the TXD buffer as specified in the TXD.MAXCNT register. The ENDRX event will be generated when the receiver has filled the RXD buffer, i.e. received the last possible byte as specified in the RXD.MAXCNT register.

Following a START task, the SPI master will generate an END event when both ENDRX and ENDTX have been generated.

The SPI master is stopped by triggering the STOP task. A STOPPED event is generated when the SPI master has stopped.

If the ENDRX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDRX event explicitly even though the RX buffer is not full.

If the ENDTX event has not already been generated when the SPI master has come to a stop, the SPI master will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 71: SPI master transaction* on page 284.



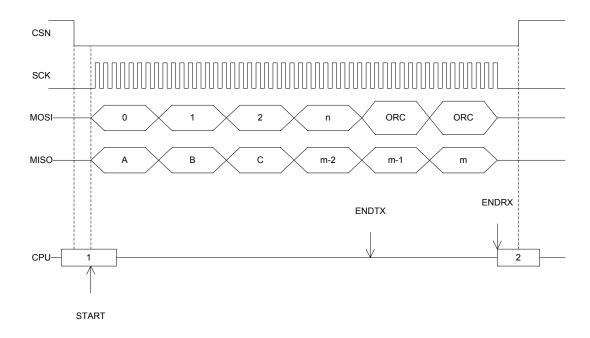


Figure 71: SPI master transaction

31.4 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

31.5 Master mode pin configuration

The SCK, MOSI, and MISO signals associated with the SPI master are mapped to physical pins according to the configuration specified in the PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively.

The PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSEL.SCK, PSEL.MOSI and PSEL.MISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 67: GPIO configuration* on page 284 prior to enabling the SPI. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 67: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value	Comments
SCK	As specified in PSEL.SCK	Output	Same as CONFIG.CPOL	
MOSI	As specified in PSEL.MOSI	Output	0	
MISO	As specified in PSEL.MISO	Input	Not applicable	



31.6 Registers

Table 68: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPIM	SPIM0	SPI master 0		
0x40004000	SPIM	SPIM1	SPI master 1		
0x40023000	SPIM	SPIM2	SPI master 2		

Table 69: Register Overview

Register	Offset	Description
TASKS_START	0x010	Start SPI transaction
TASKS_STOP	0x014	Stop SPI transaction
TASKS_SUSPEND	0x01C	Suspend SPI transaction
TASKS_RESUME	0x020	Resume SPI transaction
EVENTS_STOPPED	0x104	SPI transaction has stopped
EVENTS_ENDRX	0x110	End of RXD buffer reached
EVENTS_END	0x118	End of RXD buffer and TXD buffer reached
EVENTS_ENDTX	0x120	End of TXD buffer reached
EVENTS_STARTED	0x14C	Transaction started
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable SPIM
PSEL.SCK	0x508	Pin select for SCK
PSEL.MOSI	0x50C	Pin select for MOSI signal
PSEL.MISO	0x510	Pin select for MISO signal
FREQUENCY	0x524	SPI frequency. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type
CONFIG	0x554	Configuration register
ORC	0x5C0	Over-read character. Character clocked out in case and over-read of the TXD buffer.

31.6.1 SHORTS

Address offset: 0x200 Shortcut register

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1	0
Id																		Α																
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	END_START										Sho	ortc	ut b	etv	vee	n E	ND	ev	ent	an	T2 b	AR	tas	k									
												See	e <i>EV</i>	EN	rs_	ENL	o ar	nd i	TAS	KS_	STA	ART												
			Disabled	0								Dis	able	e sh	ort	cut																		
			Enabled	1								Ena	able	sho	orto	ut																		

31.6.2 INTENSET

Address offset: 0x304 Enable interrupt



Bit numb	er		31 30 29	28 2	7 26 2	25 24	23	22 21 2	0 19	18 1	17 1	5 15	14	13 1	12 1	1 10	9	8 7	ϵ	5	4	3	2	1 0
Id									Ε									D	C		В			A
Reset 0x	00000000		0 0 0	0 0	0	0 0	0	0 0	0 0	0	0 0	0	0	0	0 0	0	0	0 0	C	0	0	0	0	0 0
ld RW	/ Field	Value Id	Value				De	scriptio	n															
A RW	STOPPED						Wr	ite '1' to	Ena	ble ir	nteri	upt	for S	TOI	PPEC	eve	nt							
							See	e <i>EVENT</i>	S_ST	OPPE	ED													
		Set	1				Ena	able																
		Disabled	0				Rea	ad: Disa	bled															
		Enabled	1				Rea	ad: Enak	oled															
B RW	ENDRX						Wr	ite '1' to	Ena	ble ir	nteri	upt	for E	END	RX e	vent								
							See	e <i>EVENT</i>	S_EN	IDRX														
		Set	1				Ena	able																
		Disabled	0				Rea	ad: Disa	bled															
		Enabled	1				Rea	ad: Enak	oled															
C RW	END						Wr	ite '1' to	Ena	ble ir	nteri	upt	for E	END	eve	nt								
							See	e <i>EVENT</i>	S_EN	ID														
		Set	1				Ena	able																
		Disabled	0				Rea	ad: Disa	bled															
		Enabled	1				Rea	ad: Enak	oled															
D RW	ENDTX						Wr	ite '1' to	Ena	ble ir	nteri	upt	for E	END.	TX e	vent								
							See	e <i>EVENT</i>	S_EN	IDTX														
		Set	1				Ena	able																
		Disabled	0				Rea	ad: Disa	bled															
		Enabled	1				Rea	ad: Enab	oled															
E RW	STARTED						Wr	ite '1' to	Ena	ble ir	nteri	upt	for S	τΑF	RTED	ever	nt							
							See	e <i>EVENT</i>	S_ST	ARTE	D													
		Set	1				Ena	able																
		Disabled	0				Rea	ad: Disa	bled															
		Enabled	1				Rea	ad: Enak	oled															
E RW	STARTED	Disabled Enabled Set Disabled	0 1 1 0				Rea Wr See Ena	ad: Disa ad: Enak rite '1' to e <i>EVENT</i> able ad: Disa	oled o Ena S_ <i>ST</i> bled			upt	for S	STAF	RTED) ever	nt							

31.6.3 INTENCLR

Address offset: 0x308 Disable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		E D C B A
Reset 0x00000000		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value Description
A RW STOPPED		Write '1' to Disable interrupt for STOPPED event
		See EVENTS_STOPPED
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
B RW ENDRX		Write '1' to Disable interrupt for ENDRX event
		See EVENTS_ENDRX
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
C RW END		Write '1' to Disable interrupt for END event
		See EVENTS_END
	Clear	1 Disable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
D RW ENDTX		Write '1' to Disable interrupt for ENDTX event
		See EVENTS_ENDTX



Bit number	31 30 29	9 28 27 26 25 24	23 22 21 20 1	19 18 17 1	6 15 1	4 13 12	2 11 10	9	8 7	6	5	4 3	2	1 0
Id				Е					D	С		В		Α
Reset 0x00000000	0 0 0	0 0 0 0 0	0 0 0 0	0 0 0	0 0	0 0	0 0	0	0 0	0	0	0 0	0	0 0
ld RW Field Value	d Value		Description											
Clear	1		Disable											
Disable	ed 0		Read: Disable	ed										
Enable	d 1		Read: Enabled	d										
E RW STARTED			Write '1' to Di	isable inter	rrupt fo	or STAR	TED ev	ent						
			See EVENTS_S	STARTED										
Clear	1		Disable											
Disable	ed 0		Read: Disable	ed										
Enable	d 1		Read: Enabled	d										

31.6.4 ENABLE

Address offset: 0x500

Enable SPIM

Bi	t nu	ımbe	r		31 30	29	28	27	26 2	25 2	24 2	23 2	22 2	1 2	0 1	9 1	8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id																															A A	A A	Α
Re	set	t 0x0	0000000		0 0	0	0	0	0	0	0	0	0 (0 () () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id		RW	Field	Value Id	Value							Des	crip	tio	1																		
Α		RW	ENABLE								E	nal	ble	or c	lisal	ble	SPII	M															
				Disabled	0						[Disa	ble	SPI	M																		
				Enabled	7						E	nal	ole:	SPI	N																		

31.6.5 PSEL.SCK

Address offset: 0x508 Pin select for SCK

Bitı	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

31.6.6 PSEL.MOSI

Address offset: 0x50C Pin select for MOSI signal

Bitı	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

31.6.7 PSEL.MISO

Address offset: 0x510

Pin select for MISO signal



Bit	numbe	er		31 30 29 28 27 26 2	5 24	23 2	22 23	1 20	19	18	17 1	6 15	14	13 12	2 11	10	9 8	3 7	6	5	4	3 2	2 1	0
Id				С																	Α	ΑА	A A	Α
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1	. 1	1	1 1	. 1	1	1	1 1	l 1	1	1 1	1	1	1 1	. 1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value		Des	cript	tion																
Α	RW	PIN		[031]		Pin ı	num	ber																
С	RW	CONNECT				Con	nect	ion																
			Disconnected	1		Disc	onn	ect																
			Connected	0		Con	nect																	

31.6.8 FREQUENCY

Address offset: 0x524

SPI frequency. Accuracy depends on the HFCLK source selected.

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A	
Reset 0x04000000		0 0 0 0 0	$. \ \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ $
Id RW Field	Value Id	Value	Description
A RW FREQUENCY			SPI master data rate
	K125	0x02000000	125 kbps
	K250	0x04000000	250 kbps
	K500	0x0800000	500 kbps
	M1	0x10000000	1 Mbps
	M2	0x20000000	2 Mbps
	M4	0x40000000	4 Mbps
	M8	0x80000000	8 Mbps

31.6.9 RXD.PTR

Address offset: 0x534

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer

31.6.10 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 13	7 16 15 14 13 12 11 10 9 8	3 7 6 5 4	3 2 1 0
Id					A A A A	A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	000000000	0000	0 0 0 0
Id RW Field	Value Id	Value	Description			
A RW MAXCNT	Maximum number of bytes in receive buffer					

31.6.11 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 1	11 10 9 8 7 6 5 4 3 2 1 0					
Id			A A A A A A A					
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0					
Id RW Field	Value Id	Value Description						
A R AMOUNT		Number of bytes transferred in the last transaction						



31.6.12 RXD.LIST

Address offset: 0x540 EasyDMA list type

Bit r	numbe	er		31 3	0 2	9 2	8 27	7 26	5 25	24	23	22	21	20 :	L9 1	8 1	7 16	5 15	14	13	12 1	1 10	9	8	7	6	5	4	3	2 1	L 0
Id																													,	Α Δ	A A
Res	et OxC	0000000		0	0 () (0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0	0
Id	RW	Field	Value Id	Valu	e						De	scri	ptic	n																	
Α	RW	LIST									List	t typ	эe																		
			Disabled	0							Dis	able	e Ea	syD	MA	list															
			ArrayList	1							Us	e ar	ray	list																	

31.6.13 TXD.PTR

Address offset: 0x544

Data pointer

В	it nu	um	be	r		31	30	29	28	8 2	7 2	6	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Ic	d					Α	Α	Α	А	١,	Δ ,	Д	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	А А
R	lese	t 0	x00	000000		0	0	0	0) (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Ic	d	R۱	N	Field	Value Id	Va	lue	•							De	scri	ptic	on																			
Α		R۱	N	PTR											Da	a r	oin	ter																			

31.6.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	7 6	5 4	3 2	2 1 0
Id					АА	A A	. A A	A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0000000000	0 0	0 0	0 0	0 0
Id RW Field	Value Id	Value	Description					
A RW MAXCNT			Maximum number of	bytes in transmit buffer				

31.6.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit	numb	er		31	30 2	9 2	8 27	26	25 2	24 2	3 2	2 2	1 20	0 19	18	17	16	15 :	14 1	3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																									Α	Α	Α.	A	А А	Α	Α
Res	et 0x0	0000000		0	0	0 (0 0	0	0	0 (0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	ue					C	esc	ript	tion	1																	
Α	R	AMOUNT								Ν	lum	ber	of	byte	es tr	ans	ferr	ed i	n th	e la	st tr	ans	acti	on							

31.6.16 TXD.LIST

Address offset: 0x550 EasyDMA list type

В	it n	umbe	r		31	30	29	28	27	26	25	5 24	23	22	21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
lo	b																																A .	4 А
R	lese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
I	d	RW	Field	Value Id	Va	lue							De	scr	ipti	on																		
Δ	١.	RW	LIST										Lis	t ty	ре																			
				Disabled	0								Di	sab	le E	asyl)M	A lis	t															
				ArrayList	1								Us	e a	rray	list																		



31.6.17 CONFIG

Address offset: 0x554 Configuration register

Bit r	numbe	r		31	30 2	29 2	28 2	7 2	26 25	5 24	4 2	3 22	21	20	19	18	17	16	15	14	13	12 :	11:	0	9	8	7	6 !	5 4	. 3	2	1	0
Id																															С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0 0	0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	ipti	on																			
Α	RW	ORDER									В	it or	der																				
			MsbFirst	0							N	lost	sign	ific	ant	bit	shit	ftec	lοι	ıt fii	st												
			LsbFirst	1							Le	east	sign	ific	ant	bit	shi	ftec	d ou	ıt fi	rst												
В	RW	СРНА									S	erial	clo	ck (5	SCK) ph	ase	è															
			Leading	0							S	amp	le o	n le	adiı	ng e	edge	e of	clo	ck,	shi	t se	ria	da	ta	on t	rail	ing					
											е	dge																					
			Trailing	1							S	amp	le o	n tr	ailir	ng e	dge	e of	clo	ck,	shif	t se	rial	da	ta d	on le	ad	ing					
											е	dge																					
С	RW	CPOL									S	erial	clo	ck (5	SCK) pc	lari	ity															
			ActiveHigh	0							Α	ctive	hig	h																			
			ActiveLow	1							Α	ctive	lov	V																			

31.6.18 ORC

Address offset: 0x5C0

Over-read character. Character clocked out in case and over-read of the TXD buffer.

Bitı	number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Res	et 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
Α	RW ORC		Over-read character. Character clocked out in case and over-
			read of the TXD buffer.

31.7 Electrical specification

31.7.1 SPIM master interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIM}	Bit rates for SPIM ²⁵			8 ²⁶	Mbps
I _{SPIM,2Mbps}	Run current for SPIM, 2 Mbps		50		μΑ
I _{SPIM,8Mbps}	Run current for SPIM, 8 Mbps		50		μΑ
I _{SPIM,IDLE}	Idle current for SPIM (STARTed, no CSN activity)		1		μΑ
t _{SPIM.START}	Time from START task to transmission started				μs

31.7.2 Serial Peripheral Interface Master (SPIM) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIM,CSCK}	SCK period				ns
t _{SPIM,RSCK,LD}	SCK rise time, standard drive ^a			t _{RF,25pF}	
t _{SPIM,RSCK,HD}	SCK rise time, high drive ^a			t _{HRF,25pF}	
t _{SPIM,FSCK,LD}	SCK fall time, standard drive ^a			t _{RF,25pF}	
t _{SPIM,FSCK,HD}	SCK fall time, high drive ^a			t _{HRF,25pF}	
t _{SPIM,WHSCK}	SCK high time ^a	(0.5*t _{CSC}	κJ		
		- t _{RSCK}			

²⁵ High bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.

^a At 25pF load, including GPIO pin capacitance, see GPIO spec.



Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIM,WLSCK}	SCK low time ^a	(0.5*	csck)		
		- t _{FSC}	<		
t _{SPIM,SUMI}	MISO to CLK edge setup time	19			ns
t _{SPIM,HMI}	CLK edge to MISO hold time	18			ns
t _{SPIM,VMO}	CLK edge to MOSI valid			59	ns
t _{SPIM.HMO}	MOSI hold time after CLK edge	20			ns

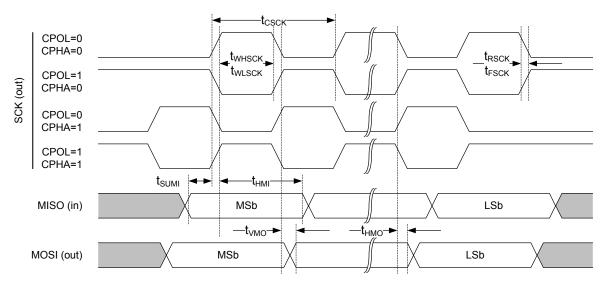


Figure 72: SPIM timing diagram



32 SPIS — Serial peripheral interface slave with EasyDMA

SPI slave (SPIS) is implemented with EasyDMA support for ultra low power serial communication from an external SPI master. EasyDMA in conjunction with hardware-based semaphore mechanisms removes all real-time requirements associated with controlling the SPI slave from a low priority CPU execution context.

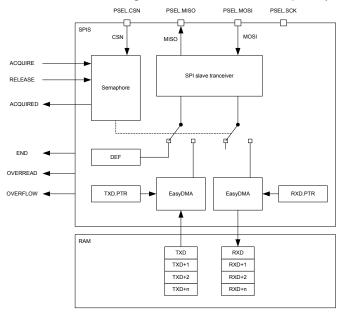


Figure 73: SPI slave

The SPIS supports SPI modes 0 through 3. The CONFIG register allows setting CPOL and CPHA appropriately.

Table 70: SPI modes

Mode	Clock polarity CPOL	Clock phase CPHA
SPI_MODE0	0 (Leading)	0 (Active High)
SPI_MODE1	0 (Leading)	1 (Active Low)
SPI_MODE2	1 (Trailing)	0 (Active High)
SPI MODE3	1 (Trailing)	1 (Active Low)

32.1 Shared resources

The SPI slave shares registers and other resources with other peripherals that have the same ID as the SPI slave. Therefore, you must disable all peripherals that have the same ID as the SPI slave before the SPI slave can be configured and used.

Disabling a peripheral that has the same ID as the SPI slave will not reset any of the registers that are shared with the SPI slave. It is important to configure all relevant SPI slave registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 24 shows which peripherals have the same ID as the SPI slave.

32.2 EasyDMA

The SPI slave implements EasyDMA for reading and writing to and from the RAM. The END event indicates that EasyDMA has finished accessing the buffer in RAM.



If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

32.3 SPI slave operation

SPI slave uses two memory pointers, RXD.PTR and TXD.PTR, that point to the RXD buffer (receive buffer) and TXD buffer (transmit buffer) respectively. Since these buffers are located in RAM, which can be accessed by both the SPI slave and the CPU, a hardware based semaphore mechanism is implemented to enable safe sharing.

See Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled on page 294.

Before the CPU can safely update the RXD.PTR and TXD.PTR pointers it must first acquire the SPI semaphore. The CPU can acquire the semaphore by triggering the ACQUIRE task and then receiving the ACQUIRED event. When the CPU has updated the RXD.PTR and TXD.PTR pointers the CPU must release the semaphore before the SPI slave will be able to acquire it. The CPU releases the semaphore by triggering the RELEASE task. This is illustrated in *Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 294. Triggering the RELEASE task when the semaphore is not granted to the CPU will have no effect.

The semaphore mechanism does not, at any time, prevent the CPU from performing read or write access to the RXD.PTR register, the TXD.PTR registers, or the RAM that these pointers are pointing to. The semaphore is only telling when these can be updated by the CPU so that safe sharing is achieved.

The semaphore is by default assigned to the CPU after the SPI slave is enabled. No ACQUIRED event will be generated for this initial semaphore handover. An ACQUIRED event will be generated immediately if the ACQUIRE task is triggered while the semaphore is assigned to the CPU.

The SPI slave will try to acquire the semaphore when CSN goes low. If the SPI slave does not manage to acquire the semaphore at this point, the transaction will be ignored. This means that all incoming data on MOSI will be discarded, and the DEF (default) character will be clocked out on the MISO line throughout the whole transaction. This will also be the case even if the semaphore is released by the CPU during the transaction. In case of a race condition where the CPU and the SPI slave try to acquire the semaphore at the same time, as illustrated in lifeline item 2 in *Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled* on page 294, the semaphore will be granted to the CPU.

If the SPI slave acquires the semaphore, the transaction will be granted. The incoming data on MOSI will be stored in the RXD buffer and the data in the TXD buffer will be clocked out on MISO.

When a granted transaction is completed and CSN goes high, the SPI slave will automatically release the semaphore and generate the END event.

As long as the semaphore is available the SPI slave can be granted multiple transactions one after the other. If the CPU is not able to reconfigure the TXD.PTR and RXD.PTR between granted transactions, the same TX data will be clocked out and the RX buffers will be overwritten. To prevent this from happening, the END_ACQUIRE shortcut can be used. With this shortcut enabled the semaphore will be handed over to the CPU automatically after the granted transaction has completed, giving the CPU the ability to update the TXPTR and RXPTR between every granted transaction.

If the CPU tries to acquire the semaphore while it is assigned to the SPI slave, an immediate handover will not be granted. However, the semaphore will be handed over to the CPU as soon as the SPI slave has released the semaphore after the granted transaction is completed. If the END_ACQUIRE shortcut is enabled and the CPU has triggered the ACQUIRE task during a granted transaction, only one ACQUIRE request will be served following the END event.

The MAXRX register specifies the maximum number of bytes the SPI slave can receive in one granted transaction. If the SPI slave receives more than MAXRX number of bytes, an OVERFLOW will be indicated in the STATUS register and the incoming bytes will be discarded.

The MAXTX parameter specifies the maximum number of bytes the SPI slave can transmit in one granted transaction. If the SPI slave is forced to transmit more than MAXTX number of bytes, an OVERREAD will be indicated in the STATUS register and the ORC character will be clocked out.



The RXD.AMOUNT and TXD.AMOUNT registers are updated when a granted transaction is completed. The TXD.AMOUNT register indicates how many bytes were read from the TX buffer in the last transaction, that is, ORC (over-read) characters are not included in this number. Similarly, the RXD.AMOUNT register indicates how many bytes were written into the RX buffer in the last transaction.

The ENDRX event is generated when the RX buffer has been filled.

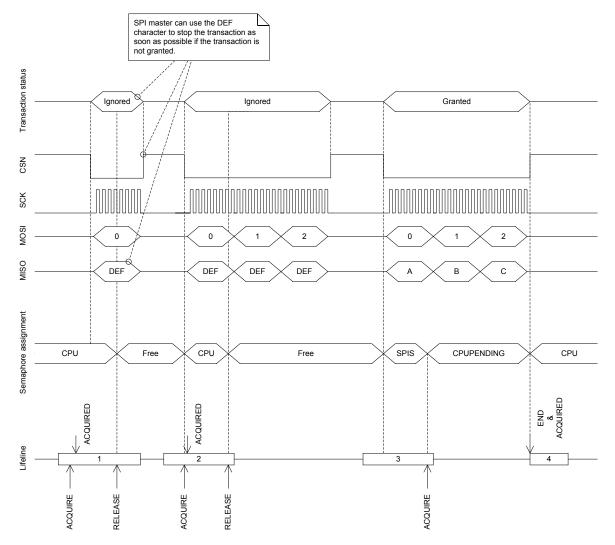


Figure 74: SPI transaction when shortcut between END and ACQUIRE is enabled

32.4 Pin configuration

The CSN, SCK, MOSI, and MISO signals associated with the SPI slave are mapped to physical pins according to the configuration specified in the PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers respectively. If the CONNECT field of any of these registers is set to Disconnected, the associated SPI slave signal will not be connected to any physical pins.

The PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO registers and their configurations are only used as long as the SPI slave is enabled, and retained only as long as the device is in System ON mode, see *POWER — Power supply* on page 78 chapter for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.CSN, PSEL.SCK, PSEL.MOSI, and PSEL.MISO must only be configured when the SPI slave is disabled.

To secure correct behavior in the SPI slave, the pins used by the SPI slave must be configured in the GPIO peripheral as described in *Table 71: GPIO configuration before enabling peripheral* on page 295 before enabling the SPI slave. This is to secure that the pins used by the SPI slave are driven correctly if the SPI



slave itself is temporarily disabled, or if the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the SPI slave is to be recognized by an external SPI master.

The MISO line is set in high impedance as long as the SPI slave is not selected with CSN.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 71: GPIO configuration before enabling peripheral

SPI signal	SPI pin	Direction	Output value	Comment
CSN	As specified in PSEL.CSN	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
MOSI	As specified in PSEL.MOSI	Input	Not applicable	
MISO	As specified in PSEL.MISO	Input	Not applicable	Emulates that the SPI slave is not selected.

32.5 Registers

Table 72: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPIS	SPIS0	SPI slave 0		
0x40004000	SPIS	SPIS1	SPI slave 1		
0x40023000	SPIS	SPIS2	SPI slave 2		

Table 73: Register Overview

Register	Offset	Description	
TASKS_ACQUIRE	0x024	Acquire SPI semaphore	
TASKS_RELEASE	0x028	Release SPI semaphore, enabling the SPI slave to acquire it	
EVENTS_END	0x104	Granted transaction completed	
EVENTS_ENDRX	0x110	End of RXD buffer reached	
EVENTS_ACQUIRED	0x128	Semaphore acquired	
SHORTS	0x200	Shortcut register	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
SEMSTAT	0x400	Semaphore status register	
STATUS	0x440	Status from last transaction	
ENABLE	0x500	Enable SPI slave	
PSELSCK	0x508	Pin select for SCK	Deprecated
PSELMISO	0x50C	Pin select for MISO	Deprecated
PSELMOSI	0x510	Pin select for MOSI	Deprecated
PSELCSN	0x514	Pin select for CSN	Deprecated
PSEL.SCK	0x508	Pin select for SCK	
PSEL.MISO	0x50C	Pin select for MISO signal	
PSEL.MOSI	0x510	Pin select for MOSI signal	
PSEL.CSN	0x514	Pin select for CSN signal	
RXDPTR	0x534	RXD data pointer	Deprecated
MAXRX	0x538	Maximum number of bytes in receive buffer	Deprecated
AMOUNTRX	0x53C	Number of bytes received in last granted transaction	Deprecated
RXD.PTR	0x534	RXD data pointer	
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer	
RXD.AMOUNT	0x53C	Number of bytes received in last granted transaction	
TXDPTR	0x544	TXD data pointer	Deprecated
MAXTX	0x548	Maximum number of bytes in transmit buffer	Deprecated
AMOUNTTX	0x54C	Number of bytes transmitted in last granted transaction	Deprecated
TXD.PTR	0x544	TXD data pointer	
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer	
TXD.AMOUNT	0x54C	Number of bytes transmitted in last granted transaction	
CONFIG	0x554	Configuration register	



Register	Offset	Description
DEF	0x55C	Default character. Character clocked out in case of an ignored transaction.
ORC	0x5C0	Over-read character

32.5.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	8 17	7 16	15	14	13 1	2 1	1 10	9	8	7	6	5 4	1 3	2	1	0
Id																														Α		
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	alue							Des	crip	otio	n																	
Α	RW	END_ACQUIRE										Sho	rtcı	ut b	etw	een	EN	D ev	ent/	and	l AC	QUI	RE ta	sk								
												See	EVI	ENT	S_E	ND	and	TAS	SKS_	AC	QUIF	RE										
			Disabled	0								Disa	able	sho	ortc	ut																
			Enabled	1								Ena	ble	sho	rtcı	ut																

32.5.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				C B A
Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW ENDRX			Write '1' to Enable interrupt for ENDRX event
				See EVENTS_ENDRX
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ACQUIRED			Write '1' to Enable interrupt for ACQUIRED event
				See EVENTS_ACQUIRED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

32.5.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		3:	1 30	29	2	8 27	7 2	6 2	5 2	4 2	3 2	2 21	L 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id																									С						В			Α	ı
Res	et 0x0	0000000		0	0	0	C	0) (0 (0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0)
ld	RW	Field	Value Id	V	alue							0	esc	ript	ion																				
Α	RW	END										٧	Vrit	e '1'	to	Disa	able	in'	terr	upt	fo	· EN	D e	ven	t										
												S	ee	VEI	NTS	_EN	ID																		
			Clear	1									isal	ole																					
			Disabled	0								F	ead	l: Di	sab	led																			
			Enabled	1								F	ead	l: En	abl	ed																			
В	RW	ENDRX										٧	Vrit	e '1'	to	Disa	able	in'	terr	upt	fo	· EN	DR:	K ev	ent	:									



Bit	numbe	er		31	30 2	29 2	28 2	27 2	26 2	5 2	4 2	3 22	2 21	20	19	18	17 :	16 :	15 :	14 1	3 12	2 11	10	9	8	7	6 5	5 4	3	2	1 0
Id																							С					В			Α
Res	et 0x0	0000000		0	0	0	0 (0	0 (0 (0 (0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0 0
Id	RW	Field	Value Id	Val	lue						D	esc	ripti	on																	
											S	ee E	VΕN	ITS_	ENL	ORX	(
			Clear	1							D	isab	ole																		
			Disabled	0							R	lead	: Dis	able	ed																
			Enabled	1							R	lead	: Ena	able	d																
С	RW	ACQUIRED									۷	Vrite	e '1'	to E	Disal	ole	inte	rru	pt f	or A	CQL	JIRE	D ev	/en	t						
											S	ee E	VEN	ITS_	ACC	วบเ	RED)													
			Clear	1							D	isab	ole																		
			Disabled	0							R	lead	: Dis	able	ed																
			Enabled	1							R	lead	: Ena	able	d																

32.5.4 SEMSTAT

Address offset: 0x400 Semaphore status register

Bitı	numbe	er		31	. 30	29	28	3 27	7 26	6 25	5 24	23	22	21	20	19	18	3 17	7 10	5 1	5 1	4 1	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α	Α
Res	et OxO	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	() (0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	Va	lue							De	escr	ipti	on																					
Α	R	SEMSTAT										Se	ma	pho	re :	sta	tus																			
			Free	0								Se	ma	pho	ore i	is fı	ree																			
			CPU	1								Se	ma	pho	ore i	is a	ssię	gne	d to	o C	PU															
			SPIS	2								Se	ma	pho	ore i	is a	ssię	gne	d to	o S	PI s	lav	e													
			CPUPending	3								Se	ma	pho	ore i	is a	ssię	gne	d to	o S	PI b	ut	a h	nan	do	ver	to 1	the	CPI	J is						
												pe	ndi	ng																						

32.5.5 STATUS

Address offset: 0x440

Status from last transaction

Individual bits are cleared by writing a '1' to the bits that shall be cleared

Bit number		31	30	29 2	28 2	27 2	6 2	!5 2	24	23	22	21	20	19	18	17 :	16	15 :	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																															В	Α
Reset 0x00000000		0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
ld RW Field	Value Id	Va	lue							De	scri	ptic	n																			
A RW OVERREAD										TX	buf	fer	ove	r-re	ad	det	ect	ed,	an	d p	rev	ent	ed									
	NotPresent	0								Rea	ad:	erro	r n	ot p	res	ent																
	Present	1								Rea	ad:	erro	r p	res	nt																	
	Clear	1							,	Wr	ite:	cle	ar e	rro	or	ıw r	itir	g '1	L'													
B RW OVERFLOW										RX	buf	fer	ove	rflo	w	lete	cte	d, a	and	pr	eve	nte	d									
	NotPresent	0								Rea	ad:	erro	r n	ot p	res	ent																
	Present	1								Rea	ad:	erro	r p	res	nt																	
	Clear	1								Wr	ite:	cle	ar e	rro	or	ıwı	itir	g '1	L'													

32.5.6 ENABLE

Address offset: 0x500 Enable SPI slave

Bit	numb	er		31	30	29 2	28 2	7 26	25	24	23	22 2	21 2	20 1	9 1	8 1	7 16	5 15	14	13	12	11 :	.0 9	8	7	6	5	4	3	2	1	0
Id																													Α	Α	Α.	Α
Re	set 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Val	lue						Des	crip	tio	n																		
Α	RW	ENABLE									Ena	ble	or (disa	ble	SPI	slav	e														7



Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17 16 1	15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					AAAA
Reset 0x00000000		0 0 0 0 0	000000000000	0 0 0 0 0 0 0	00000000
Id RW Field	Value Id	Value	Description		
	Disabled	0	Disable SPI slave		
	Enabled	2	Enable SPI slave		

32.5.7 PSELSCK (Deprecated)

Address offset: 0x508 Pin select for SCK

Bit	numb	er		31	. 30	29	28	27	' 26	25	24	23	22 2	21 2	20 1	9 1	.8 1	7 10	5 15	14	13	12	11 1	10 9	9 8	3 7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۸ ۸	ДД	. Α	A	Α	Α	Α	Α	A A	Α Α	Δ Δ	A	A	Α	Α	Α ,	A A
Res	et 0xl	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	1 1	. 1	. 1	1	1	1	1	1 :	1 1	L 1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	RW	PSELSCK		[0	31]						Pin	nur	nbe	r cc	nfi	gura	tio	n fo	r SP	I SC	K si	gnal									
			Disconnected	0x	FFF	FFF	FF					Disc	coni	nec	t																	

32.5.8 PSELMISO (Deprecated)

Address offset: 0x50C Pin select for MISO

Bit	numbe	er		31	L 30	29	28	27	26	25	24	23	22	21	20	19 :	18 1	.7 1	16 1	15 :	14 1	13 :	L2 :	11 1	LO	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	Α	Α	Α.	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	А А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	n																			
Α	RW	PSELMISO		[0	31]						Pin	nu	mb	er c	onf	igur	atio	on f	or	SPI	MIS	SO :	sign	al									
			Disconnected	0х	FFF	FFF	FF					Dis	con	nec	t																			

32.5.9 PSELMOSI (Deprecated)

Address offset: 0x510 Pin select for MOSI

Bit	numbe	er		31	1 30	29	28	3 2	7 2	6 2	25 2	24 2	23 :	22 :	21 :	20 :	19	18	17 :	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	. Α	. Δ	A /	Δ ,	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	. 4	A
Res	et 0xF	FFFFFF		1	1	1	1	. 1	L 1	1 :	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	. 1
Id	RW	Field	Value Id	Va	alue	:						ı	Des	crip	otio	n																			
Α	RW	PSELMOSI		[031]						ı	Pin	nur	nbe	er c	onf	igu	rati	on	for	SPI	MC	OSI	sign	nal											
			Disconnected	0>	ĸFFF	FFF	FFF						Disc	con	nec	t																			

32.5.10 PSELCSN (Deprecated)

Address offset: 0x514 Pin select for CSN

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 :	21 :	20 1	19 1	18 1	7 1	6 1	5 14	1 13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α ,	A A	Α Α	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L :	l 1	. 1	1	1	1	1	1	1	1	1	1	1	1 1	1	. 1
Id	RW	Field	Value Id	Va	lue							De	crip	otio	n																		
Α	RW	PSELCSN		[0	31]						Pin	nur	nbe	er co	onfi	igura	atic	n fo	or SI	PI C	SN s	igna	I									
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t:																		

32.5.11 PSEL.SCK

Address offset: 0x508 Pin select for SCK



Bit	numbe	er		31	30 2	9 2	28 27	7 26	5 25	24	23	22	21 2	20 1	9 1	8 17	16	15	14 1	13 1	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id				В																								Α	А А	A	Α
Res	et 0xF	FFFFFF		1	1 1	1 :	1 1	1	1	1	1	1	1	1 :	1 1	l 1	1	1	1	1 1	1	1	1	1	1	1	1	1	1 1	. 1	1
Id	RW	Field	Value Id	Val	ue						Des	scrip	otio	n																	
Α	RW	PIN		[0	31]						Pin	nur	nbe	r																	
В	RW	CONNECT									Cor	nne	ction	n																	
			Disconnected	1							Dis	con	nect	t																	
			Connected	0							Cor	nne	ct																		

32.5.12 PSEL.MISO

Address offset: 0x50C Pin select for MISO signal

Bit r	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

32.5.13 PSEL.MOSI

Address offset: 0x510

Pin select for MOSI signal

Bit	numbe	er		31 30 29 28 27 26 25 2	$24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id				В	A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

32.5.14 PSEL.CSN

Address offset: 0x514

Pin select for CSN signal

Bit	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

32.5.15 RXDPTR (Deprecated)

Address offset: 0x534 RXD data pointer



Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	RW	RXDPTR										RXI	O da	ata	poi	ntei	-																	

32.5.16 MAXRX (Deprecated)

Address offset: 0x538

Maximum number of bytes in receive buffer

D:4				21	20.1		20.2	7 2	C 21	- 2	1 21		21	20	10	10	17	10	1 -	11	12	12	11	10	0	0	7	_	_	4	2	2	1 0
BIT	numbe	er		31	30 2	29 .	28 2	/ 21	6 25	> 24	+ 2:	5 22	. 21	20	19	18	1/	16	15	14	13	12	11	10	9	8	/	Ь	5	4	3	2	1 0
Id																											Α	Α	Α	Α	Α	Α .	А А
Res	et 0x0	0000000		0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	esci	ipti	on																			
Α	RW	MAXRX									Μ	axi	mur	n nı	uml	oer	of b	oyte	es ir	ı re	ceiv	e b	uffe	er									

32.5.17 AMOUNTRX (Deprecated)

Address offset: 0x53C

Number of bytes received in last granted transaction

Bit number		31 30 29 28 27 26	6 25 24 23 22 21 20 19	18 17 16 15 14 13 12 11	1 10 9 8 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0000000	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A R AMOUI	TRX		Number of byte	es received in the last gran	ited transaction

32.5.18 RXD.PTR

Address offset: 0x534 RXD data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		RXD data pointer

32.5.19 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit	numb	er		31	30 2	9 2	8 2	7 26	25	24	23	22 2	21 :	20 1	L9 1	8 1	7 1	6 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0	l
Id																										Α	Α	Α	Α	Α	Α	А А	l
Re	et 0x0	0000000		0	0 0) (0	0	0	0	0	0	0	0	0	0 (0 () () () () () (0	0	0	0	0	0	0	0	0	0 0	l
Id	RW	Field	Value Id	Val	ue						De	scrip	otio	n																			l
Α	RW	MAXCNT									Ma	xim	um	nuı	mbe	er o	f by	tes	in ı	rece	eive	bu	ffer										١

32.5.20 RXD.AMOUNT

Address offset: 0x53C

Number of bytes received in last granted transaction

Id															,	Δ Δ	A	Α	Α	АА	Α
Res	et 0x0	0000000		0 0 0 0 0	0 0 0	0 0	0 0	0 (0 0	0 0	0	0 0	0 0	n	0	n 0	n	0	0	0 0	0
										•	_	~ ~		٠	•			_			
Id	RW	Field	Value Id	Value			iption														

R AMOUNT Number of bytes received in the last granted transaction



32.5.21 TXDPTR (Deprecated)

Address offset: 0x544
TXD data pointer

Bit r	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17 :	16 1	L5 1	4 1	3 12	2 1	1 10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Α	Α Α	. 4	А	Α	Α	Α	Α	Α	Α	Α .	Α.	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
Α	RW	TXDPTR										TXI) d	ata	poi	nte	r																

32.5.22 MAXTX (Deprecated)

Address offset: 0x548

Maximum number of bytes in transmit buffer

D'u		24 20 20 20 2	7 26 25 24 22 22 24 20 40 40 4	7.46.45.44.42.42.44.40.0.0	7.6.5	4 2 2 4	0
Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 1	./ 16 15 14 13 12 11 10 9 8	, / 6 5	4321	U
Id					A A A	. A A A A	Α
Reset 0x00000000		0 0 0 0 0	00000000000	0 0 0 0 0 0 0 0 0	000	0 0 0 0	0
Id RW Field	Value Id	Value	Description				
A RW MAXTX			Maximum number o	f bytes in transmit buffer			

32.5.23 AMOUNTTX (Deprecated)

Address offset: 0x54C

Number of bytes transmitted in last granted transaction

Bit r	numbe	er		31	. 30	0 29	28	3 27	26	25	24	23	22 2	21 2	20 1	9 1	.8 1	7 1	5 15	5 14	13	12	11	10	9	8	7	6 5	5 4	3	2	1	0
Id																											Δ.	A A	A 4	A	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0
Id	RW	Field	Value Id	Va	ılu	е						De	scrip	tio	n																		
Α	R	AMOUNTTX										Nu	mbe	r o	f by	tes	trar	ısm	itte	d in	las	t gra	nte	d tr	ans	act	on						_

32.5.24 TXD.PTR

Address offset: 0x544

TXD data pointer

	Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	Id		A A A A A A A A A A A A A A A A A A A
	Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	ld RW Field	Value Id	Value Description
ı	A RW PTR		TXD data pointer

32.5.25 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 13	1 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	000000000000
Id RW Field	Value Id	Value Description	
A RW MAXCNT		Maximum number of bytes in transmit by	uffer

32.5.26 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transmitted in last granted transaction



Bit r	numb	er		31	30	29	28	27 :	26	25	24	23 :	22 2	21 2	0 1	9 18	3 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3	2	1 0
Id																										Α	Α	Α	Α	Α	A	4 А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	n																	
Α	R	AMOUNT										Nur	nbe	r of	byt	es t	rans	mit	ted	in	last	gran	ted	trar	ısac	tio	n					

32.5.27 CONFIG

Address offset: 0x554 Configuration register

Bit r	iumbe	er		31	30	29	28 2	27 2	26 2	5 2	4 2	3 22	21	20	19	18 :	17 :	16 1	15	14 1	L3 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																														С	В	Α
Rese	et 0x0	0000000		0	0	0	0	0	0 (0) (0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D)escr	iptio	on																		
Α	RW	ORDER									В	it or	der																			
			MsbFirst	0							Ν	∕lost	sign	ifica	ant	bit :	shif	ted	ou	t fir	st											
			LsbFirst	1							L	east	sign	ifica	ant	bit :	shif	ted	ou	t fir	st											
В	RW	СРНА									S	erial	cloc	k (S	SCK)) ph	ase															
			Leading	0							S	amp	le o	n lea	adir	ng e	dge	of	clo	ck,	shif	t se	rial	data	on	tra	iling	S				
											е	dge																				
			Trailing	1							S	amp	le o	n tra	ailir	ıg e	dge	of	clo	ck, s	shif	t se	rial (data	on	lea	ding	S				
											е	dge																				
С	RW	CPOL									S	erial	clo	k (S	SCK) po	lari	ty														
			ActiveHigh	0							Α	ctive	e hig	h																		
			ActiveLow	1							Α	ctive	e lov	v																		

32.5.28 DEF

Address offset: 0x55C

Default character. Character clocked out in case of an ignored transaction.

Bit r	number		31	1 30	29	28	27 2	6 2	25 2	4 2	3 2	2 2	1 2	0 1	9 1	8 17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	1	. 0
Id																									Α	Α	Α	Α	ΑА	. 4	А
Res	et 0x00000000		0	0	0	0	0	0	0 () (0 (0) (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	C	0
Id	RW Field	Value Id	Vā	alue						D	esc	ript	tior	1																	
Α	RW DEF									D	efa	ult	cha	rac	ter.	Cha	arac	ter	clo	cked	d ou	t in	case	of	an i	gno	red				
										tı	ran	sact	ion	1.																	

32.5.29 ORC

Address offset: 0x5C0 Over-read character

Bit r	numbe	er		31	30 :	29 2	28 2	27 2	26 2	25 2	4 2	3 2	2 2	1 2	0 19	9 18	3 17	16	15	14	13	12 1	11 :	10 !	9	8 7	6	5	4	3	2	1 0
Id																										Δ	. Δ	A	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0 (0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						0	eso	rip	tion	1																	
Α	RW	ORC									C	vei	r-re	ad o	har	act	er. (Chai	act	er c	locl	ked	out	t aft	er a	an o	ver-	rea	d			

of the transmit buffer.



32.6 Electrical specification

32.6.1 SPIS slave interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPIS}	Bit rates for SPIS ²⁷			8 ²⁸	Mbps
I _{SPIS,2Mbps}	Run current for SPIS, 2 Mbps		45		μΑ
I _{SPIS,8Mbps}	Run current for SPIS, 8 Mbps		45		μΑ
I _{SPIS,IDLE}	Idle current for SPIS (STARTed, no CSN activity)		1		μΑ
t _{SPIS,LP,START}	Time from RELEASE task to ready to receive/transmit (CSN		t _{SPIS,CL,ST}	AR	μs
	active), Low power mode		+		
			t _{START_HF}	N	
t _{SPIS,CL,START}	Time from RELEASE task to receive/transmit (CSN active),		0.125		μs
	Constant latency mode				

32.6.2 Serial Peripheral Interface Slave (SPIS) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPIS,CSCKIN,8Mbps}	SCK input period at 8Mbps		125		ns
t _{SPIS,CSCKIN,4Mbps}	SCK input period at 4Mbps		250		ns
t _{SPIS,CSCKIN,2Mbps}	SCK input period at 2Mbps		500		ns
t _{SPIS,RFSCKIN}	SCK input rise/fall time			30	ns
t _{SPIS,WHSCKIN}	SCK input high time	30			ns
t _{SPIS,WLSCKIN}	SCK input low time	30			ns
t _{SPIS,SUCSN,LP}	CSN to CLK setup time, Low power mode	t _{SPIS,SUC}	SN,		ns
		+			
		t _{START_}	IFIN		
t _{SPIS,SUCSN,CL}	CSN to CLK setup time, Constant latency mode	1000			ns
t _{SPIS,HCSN}	CLK to CSN hold time	2000			ns
t _{SPIS,ASO}	CSN to MISO driven ^a			1000	ns
t _{SPIS,DISSO}	CSN to MISO disabled ^a			68	ns
t _{SPIS,CWH}	CSN inactive time	300			ns
t _{SPIS,VSO}	CLK edge to MISO valid			19	ns
t _{SPIS,HSO}	MISO hold time after CLK edge	18 ²⁹			ns
t _{SPIS,SUSI}	MOSI to CLK edge setup time	59			ns
t _{SPIS,HSI}	CLK edge to MOSI hold time	20			ns

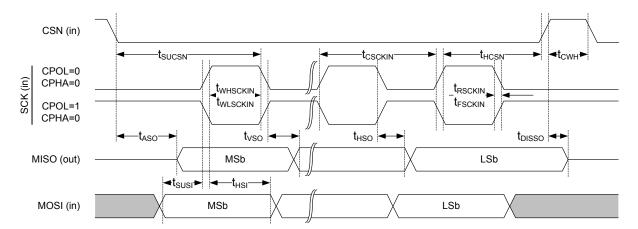


Figure 75: SPIS timing diagram

²⁷ Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

²⁸ The actual maximum data rate depends on the master's CLK to MISO and MOSI setup and hold timings.

^a At 25pF load, including GPIO capacitance, see GPIO spec.

This is to ensure compatibility to SPI masters sampling MISO on the same edge as MOSI is output



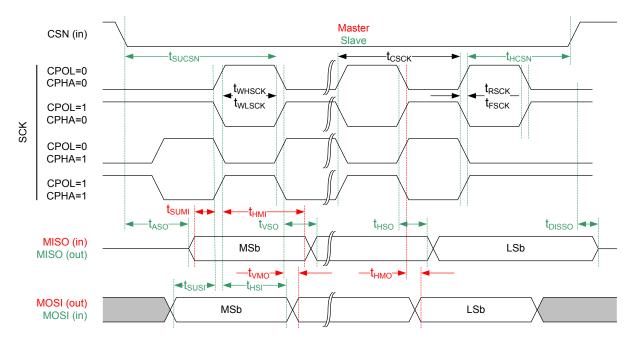


Figure 76: Common SPIM and SPIS timing diagram



33 TWIM — I²C compatible two-wire interface master with EasyDMA

TWI master with EasyDMA (TWIM) is a two-wire half-duplex master which can communicate with multiple slave devices connected to the same bus

Listed here are the main features for TWIM:

- I²C compatible
- 100 kbps, 250 kbps, or 400 kbps
- · Support for clock stretching
- EasyDMA

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. TWIM is not compatible with CBUS.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

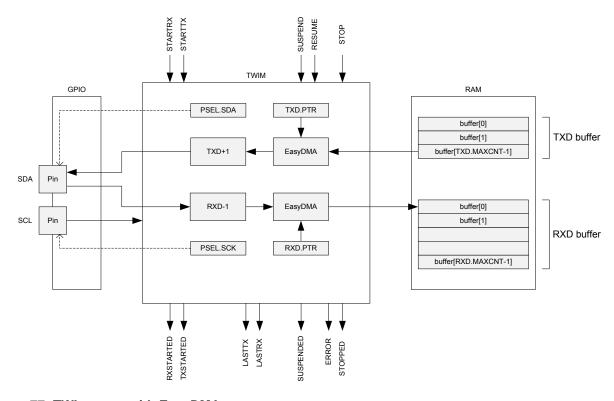


Figure 77: TWI master with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 78: A typical TWI setup comprising one master and three slaves* on page 306. This TWIM is only able to operate as a single master on the TWI bus. Multi-master bus configuration is not supported.



Figure 78: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task. The TWI master will generate a STOPPED event when it has stopped following a STOP task.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

After the TWI master is started, the STARTTX task or the STARTRX task should not be triggered again before the TWI master has stopped, i.e. following a LASTRX, LASTTX or STOPPED event.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

33.1 Shared resources

The TWI master shares registers and other resources with other peripherals that have the same ID as the TWI master. Therefore, you must disable all peripherals that have the same ID as the TWI master before the TWI master can be configured and used.

Disabling a peripheral that has the same ID as the TWI master will not reset any of the registers that are shared with the TWI master. It is therefore important to configure all relevant registers explicitly to secure that the TWI master operates correctly.

The Instantiation table in *Instantiation* on page 24 shows which peripherals have the same ID as the TWI.

33.2 EasyDMA

The TWI master implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

33.2.1 EasyDMA list

EasyDMA supports one list type.

The supported list type is:

Array list

EasyDMA array list

The EasyDMA array list can be represented by the data structure ArrayList_type.

For illustration, see the code example below. This data structure includes only a buffer with size equal to Channel.MAXCNT. EasyDMA will use the Channel.MAXCNT register to determine when the buffer is full. Replace 'Channel' by the specific data channel you want to use, for instance 'NRF_SPIM->RXD', 'NRF_SPIM->TXD', 'NRF_TWIM->RXD', etc.



The Channel.MAXCNT register cannot be specified larger than the actual size of the buffer. If Channel.MAXCNT is specified larger than the size of the buffer, the EasyDMA channel may overflow the buffer.

This array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM

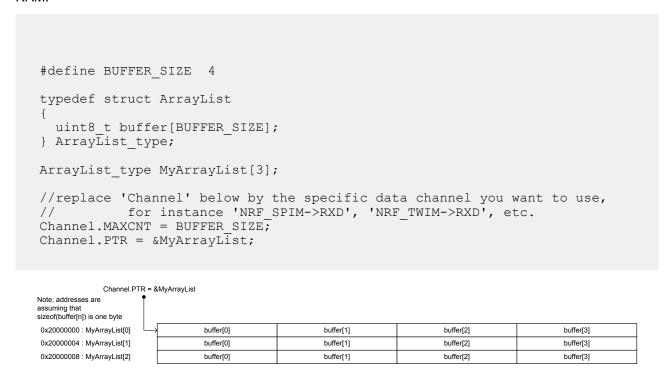


Figure 79: EasyDMA array list

33.3 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes found in the transmit buffer located in RAM at the address specified in the TXD.PTR register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave.

A typical TWI master write sequence is illustrated in *Figure 80: TWI master writing data to a slave* on page 308. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.



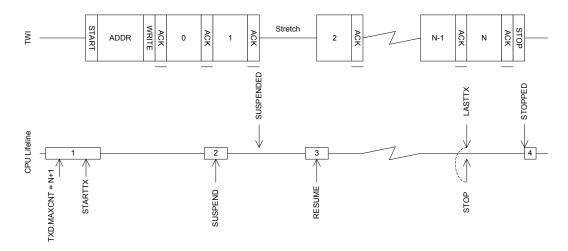


Figure 80: TWI master writing data to a slave

The TWI master will generate a LASTTX event when it starts to transmit the last byte, this is illustrated in *Figure 80: TWI master writing data to a slave* on page 308

The TWI master is stopped by triggering the STOP task, this task should be triggered during the transmission of the last byte to secure that the TWI will stop as fast as possible after sending the last byte. It is safe to use the shortcut between LASTTX and STOP to accomplish this.

Note that the TWI master does not stop by itself when the whole RAM buffer has been sent, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

33.4 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1). The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

Data received will be stored in RAM at the address specified in the RXD.PTR register. The TWI master will generate an ACK after all but the last byte received from the slave. The TWI master will generate a NACK after the last byte received to indicate that the read sequence shall stop.

A typical TWI master read sequence is illustrated in *Figure 81: The TWI master reading data from a slave* on page 309. Occurrence 2 in the figure illustrates clock stretching performed by the TWI master following a SUSPEND task.

A SUSPENDED event indicates that the SUSPEND task has taken effect; this event can be used to synchronize the software.

The TWI master will generate a LASTRX event when it is ready to receive the last byte, this is illustrated in *Figure 81: The TWI master reading data from a slave* on page 309. If RXD.MAXCNT > 1 the LASTRX event is generated after sending the ACK of the previously received byte. If RXD.MAXCNT = 1 the LASTRX event is generated after receiving the ACK following the address and READ bit.

The TWI master is stopped by triggering the STOP task, this task must be triggered before the NACK bit is supposed to be transmitted. The STOP task can be triggered at any time during the reception of the last byte. It is safe to use the shortcut between LASTRX and STOP to accomplish this.



Note that the TWI master does not stop by itself when the RAM buffer is full, or when an error occurs. The STOP task must be issued, through the use of a local or PPI shortcut, or in software as part of the error handler.

The TWI master cannot get stopped while it is suspended, so the STOP task has to be issued after the TWI master has been resumed.

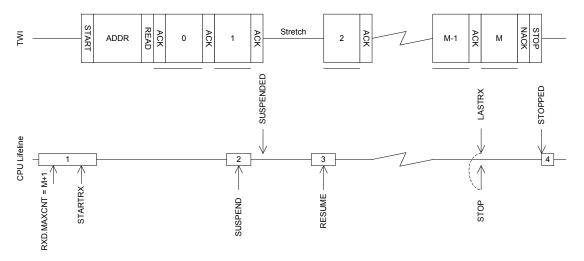


Figure 81: The TWI master reading data from a slave

33.5 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave. This example uses shortcuts to perform the simplest type of repeated start sequence, i.e. one write followed by one read. The same approach can be used to perform a repeated start sequence where the sequence is read followed by write.

The figure Figure 82: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave on page 309 illustrates this:

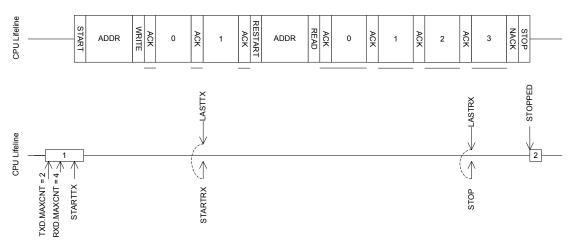


Figure 82: A repeated start sequence, where the TWI master writes two bytes followed by reading 4 bytes from the slave

If a more complex repeated start sequence is needed and the TWI firmware drive is serviced in a low priority interrupt it may be necessary to use the SUSPEND task and SUSPENDED event to guarantee that the correct tasks are generated at the correct time. This is illustrated in *Figure 83: A double repeated start* sequence using the SUSPEND task to secure safe operation in low priority interrupts on page 310.



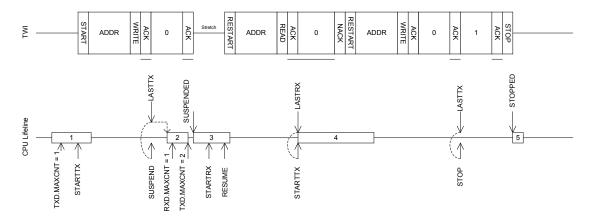


Figure 83: A double repeated start sequence using the SUSPEND task to secure safe operation in low priority interrupts

33.6 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

33.7 Master mode pin configuration

The SCL and SDA signals associated with the TWI master are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI master is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL, PSEL.SDA must only be configured when the TWI master is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 74: GPIO configuration before enabling peripheral* on page 310.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 74: GPIO configuration before enabling peripheral

TWI master signal	TWI master pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	SOD1
SDA	As specified in PSEL.SDA	Input	Not applicable	SOD1

33.8 Registers

Table 75: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	TWIM	TWIM0	Two-wire interface master 0		
0x40004000	TWIM	TWIM1	Two-wire interface master 1		



Table 76: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction. Must be issued while the TWI master is not suspended.
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_SUSPENDED	0x148	Last byte has been sent out after the SUSPEND task has been issued, TWI traffic is now suspended.
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_LASTRX	0x15C	Byte boundary, starting to receive the last byte
EVENTS_LASTTX	0x160	Byte boundary, starting to transmit the last byte
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWIM
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
FREQUENCY	0x524	TWI frequency
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
RXD.LIST	0x540	EasyDMA list type
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
TXD.LIST	0x550	EasyDMA list type

33.8.1 SHORTS

Address offset: 0x200 Shortcut register

Bit r	numbe	r		31 30	29 2	28 27	7 26	25 24	1 23	22 2	21 20) 19	18	17 :	16	15 1	4 1	3 12	2 11	10	9	8 7	' 6	5	4	3	2	1 0
Id																		F		D	С	ВА	4					
Rese	et 0x0	0000000		0 0	0	0 0	0	0 0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value					Des	scrip	tion																	
Α	RW	LASTTX_STARTRX							Sho	ortcu	ıt be	twe	en L	AST	TX	eve	nt a	nd S	TAF	RTRX	tas	k						
									See	e EVE	ENTS	_LA	STT	K an	d 7	ASK	S_S	TAR	TRX									
			Disabled	0					Dis	able	sho	rtcu	t															
			Enabled	1					Ena	able	shor	tcut																
В	RW	LASTTX_SUSPEND							Sho	ortcu	ıt be	twe	en L	AST	TX	eve	nt a	nd S	USF	PENI) tas	sk						
									See	e EVE	ENTS	_LA	STT	K an	d 7	ASK	s_s	USP	END)								
			Disabled	0					Dis	able	sho	rtcu	t															
			Enabled	1					Ena	able	shor	tcut																
С	RW	LASTTX_STOP							Sho	ortcu	ıt be	twe	en L	AST	TX	eve	nt a	nd S	TOF	tas	k							
									See	e EVE	ENTS	_LA	STT	K an	d 7	ASK	S_S	ТОР										
			Disabled	0					Dis	able	sho	rtcu	t															
			Enabled	1					Ena	able	shor	tcut																
D	RW	LASTRX_STARTTX							Sho	ortcu	ıt be	twe	en L	AST	RX	eve	nt a	nd S	TAF	RTTX	tas	k						
									See	EVE	ENTS	LA.	STR	X an	d 7	ASK	s_s	TAR	TTX									

Disable shortcut

Disabled



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			F D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Enabled	1	Enable shortcut
F RW LASTRX_STOP			Shortcut between LASTRX event and STOP task
			See EVENTS_LASTRX and TASKS_STOP
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

33.8.2 INTEN

Address offset: 0x300 Enable or disable interrupt

D.:.		or disable interre	·																						_	_	-				
	numbe	er		31	30 29	9 28	3 27	26			23 22					7 16	5 15	14	- 13	12	11	. 10		8	7	6	5	4 3	3 2		
Id -											1			G F									D							A	
		0000000				0	0	0	0		0 0			0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0
ld .		Field	Value Id	Val	ue						Descr												_								
Α	RW	STOPPED									Enabl	le or (disa	ible i	nte	erru	pt f	or S	IOF	PE	Dε	ven	t								
										:	See <i>E</i>	VENT	TS_S	TOP	PEI	D															
			Disabled	0						- 1	Disab	le																			
			Enabled	1						-	Enabl	le																			
D	RW	ERROR								ı	Enabl	le or (disa	ıble i	nte	rru	pt f	or E	RRC)R e	eve	nt									
										9	See <i>E</i>	VENT	TS E	RRC)R																
			Disabled	0							Disab		-																		
			Enabled	1							Enabl																				
F	RW	SUSPENDED								-	Enabl	le or o	disa	ıble i	nte	rru	pt f	or S	USF	EN	DE	D ev	/en	t							
											c -		.		- N	0.55															
			Disabled	0							See <i>E</i> Disab		13_3	OUSP	EIV	DEL	,														
			Enabled	1							Enabl																				
G	D\A/	RXSTARTED	Ellableu								Enabl		dica	hla i	nte	rrii	nt f	or E	VCT	۷D.	TEI) av	ont								
J	IVV	NASTANTED									LIIabi	ie oi v	uisa	ible i	1110	iiu	pι	יו וכ	1/21	ΑI	16	Jev	CIII								
										:	See <i>E</i>	VENT	TS_F	RXST	AR	TED															
			Disabled	0						ı	Disab	le																			
			Enabled	1						- 1	Enabl	le																			
Н	RW	TXSTARTED								- 1	Enabl	le or (disa	ıble i	nte	rru	pt f	or T	XST	AR	TEC) ev	ent								
										:	See <i>E</i>	VEN1	TS_1	TXST.	AR	ΓED															
			Disabled	0						-	Disab	le																			
			Enabled	1						- 1	Enabl	le																			
1	RW	LASTRX								- 1	Enabl	le or (disa	ıble i	nte	rru	pt f	or L	AST	RX	eve	ent									
										9	See <i>E</i>	VENT	TS L	AST	RX																
			Disabled	0							Disab																				
			Enabled	1							Enabl																				
J	RW	LASTTX		_							Enabl		disa	ıble i	nte	rru	pt f	or L	AST	TX	eve	ent									
	-															-						-									
				_							See <i>E</i>		15_L	.AST	ľΧ																
			Disabled	0							Disab 																				
			Enabled	1						١	Enabl	le																			

33.8.3 INTENSET

Address offset: 0x304 Enable interrupt



Bit r	numb	er		31 30	29 2	8 27	7 26	25 24	1 2	23 22 21	L 2	0 19	18	3 17	16	5 15	14	13	3 1.	2 1:	1 10) 9	8	7	6	5	4	3	2 :	1 0
Id								J	1	I .	F	l G	F									D)						A	Д
Res	et 0x0	0000000		0 0	0 (0 0	0	0 0	(0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value					D	Descripti	ion	1																		
Α	RW	STOPPED							٧	Vrite '1'	to	Ena	ble	int	err	upt	foi	ST	OP	PEC	ev	ent	t							
									S	ee <i>EVEN</i>	VTS	S_ST	OP	PEC)															
			Set	1					Ε	nable																				
			Disabled	0					R	Read: Dis	sab	oled																		
			Enabled	1					R	Read: En	ab	led																		
D	RW	ERROR							٧	Vrite '1'	to	Ena	ble	int	err	upt	foi	ER	.RO	R e	ven	t								
									S	ee <i>EVEN</i>	VTS	S_ER	RC)R																
			Set	1					Ε	nable																				
			Disabled	0					R	Read: Dis	sab	oled																		
			Enabled	1					R	Read: En	ab	led																		
F	RW	SUSPENDED							٧	Vrite '1'	to	Ena	ble	int	err	upt	foi	SU	ISPI	ENE	DED	ev	ent							
									S	ee <i>EVEN</i>	VTS	s_su	ISP	ENE	DEL)														
			Set	1					Ε	nable																				
			Disabled	0					R	Read: Dis	sab	oled																		
			Enabled	1					R	Read: En	ab	led																		
G	RW	RXSTARTED							٧	Vrite '1'	to	Ena	ble	int	err	upt	foi	RX	STA	ART	ED	eve	ent							
									S	ee <i>EVEN</i>	VTS	S_RX	ST.	ART	ED															
			Set	1					Ε	nable																				
			Disabled	0					R	Read: Dis	sab	oled																		
			Enabled	1					R	Read: En	ab	led																		
Н	RW	TXSTARTED							٧	Vrite '1'	to	Ena	ble	int	err	upt	foi	TX	ST/	٩RT	ED	eve	ent							
									S	ee <i>EVEN</i>	VTS	S_TX	ST	4RT	ED															
			Set	1					Ε	nable																				
			Disabled	0					R	Read: Dis	sab	oled																		
			Enabled	1					R	Read: En	ab	led																		
1	RW	LASTRX							٧	Vrite '1'	to	Ena	ble	int	err	upt	foi	LA	STF	₹X ∈	ever	nt								
									S	ee <i>EVEN</i>	VTS	S_LA	ST	RX																
			Set	1					Ε	nable																				
			Disabled	0					R	Read: Dis	sab	oled																		
			Enabled	1					R	Read: En	ab	led																		
J	RW	LASTTX							٧	Vrite '1'	to	Ena	ble	int	err	upt	foi	LA	ST1	ГΧ є	ver	nt								
									S	ee <i>EVEN</i>	VTS	5_ <i>LA</i>	ST	TX																
			Set	1					Ε	nable																				
			Disabled	0					R	Read: Dis	sab	oled																		
			Enabled	1					R	Read: En	ab	led																		

33.8.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bitı	numbe	er		31	30	29	28	27 2	26 2	5 2	4 2	3 22	2 21	20	19	18	17	16 :	15 1	4 1	3 12	2 11	10	9	8 7	7 6	5 5	4	3	2	1 0
Id										J				Н	G	F								D							А
Res	et 0x0	0000000		0	0	0	0	0	0 (0) (0	0	0	0	0	0	0	0 (0	0	0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	on																	
Α	RW	STOPPED									V	√rite	e '1'	to [Disa	ble	inte	rru	pt f	or S	ТОР	PED	eve	nt							
											S	ee E	VEN	ITS_	STO	OPP	ED														
			Clear	1							D	isat	ole																		
			Disabled	0							R	ead	: Dis	abl	ed																
			Enabled	1							R	ead	: Ena	able	ed																
D	RW	ERROR									W	Vrite	e '1'	to [Disa	ble	inte	rru	pt f	or E	RRC	R ev	ent								
											S	ee E	VEN	ITS_	ERI	ROR	?														



Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			J	I HGF D A
Res	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW SUSPENDED			Write '1' to Disable interrupt for SUSPENDED event
				See EVENTS_SUSPENDED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW RXSTARTED			Write '1' to Disable interrupt for RXSTARTED event
				C FVENTC DVCTADTED
		Clear	1	See EVENTS_RXSTARTED Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW TXSTARTED	Lilabled	1	Write '1' to Disable interrupt for TXSTARTED event
"	IW INSTANTED			write 1 to bisable interrupt for TASTARTED event
				See EVENTS_TXSTARTED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
1	RW LASTRX			Write '1' to Disable interrupt for LASTRX event
				See EVENTS_LASTRX
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW LASTTX			Write '1' to Disable interrupt for LASTTX event
				See EVENTS_LASTTX
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

33.8.5 ERRORSRC

Address offset: 0x4C4

Error source

Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
Α	RW OVERRUI	l	Overrun error
			A new byte was received before previous byte got transferred
			into RXD buffer. (Previous data is lost)
		NotReceived	0 Error did not occur
		Received	1 Error occurred
В	RW ANACK		NACK received after sending the address (write '1' to clear)
		NotReceived	0 Error did not occur
		Received	1 Error occurred
С	RW DNACK		NACK received after sending a data byte (write '1' to clear)
		NotReceived	0 Error did not occur
		Received	1 Error occurred

33.8.6 ENABLE

Address offset: 0x500



Enable TWIM

Bit	num	ber				31 3	30 2	29 2	28	27	26	25	24	23	3 22	2 2	1 2	0 1	9 1	18	17	16	15	14	13	12	2 11	. 10	9	8	7	6	5	4	3	2	1	0
Id																																			Α	Α	Α	Α
Res	et 0	x00	000000			0	0	0	0	0	0	0	0	0	0	C) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RV	N	Field	Value Id	,	Valu	ıe							De	esci	ript	tioi	1																				
Α	RV	N	ENABLE											En	nab	le c	or c	lisa	ble	ΤV	VIN	1																_
				Disabled		0								Di	sab	le '	TW	'IM																				
				Enabled		6								En	nab	le 1	W	IM																				

33.8.7 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

33.8.8 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

Bit r	numbe	er		31	30 2	29 2	28 2	7 20	5 25	5 24	23	22	21 :	20 :	19 1	18 1	.7 1	6 1	5 14	13	12	11 1	.0 9	9 8	3 7	6	5	4	3	2	1 0)
Id				В																								Α	Α	Α	A A	
Res	et OxF	FFFFFF		1	1	1	1 1	1	. 1	1	1	1	1	1	1	1 :	1 1	l 1	1	1	1	1	1 1	1	. 1	. 1	1	1	1	1	1 1	
Id	RW	Field	Value Id	Val	lue						De	scri	ptio	n																		l
Α	RW	PIN		[0	.31]						Pin	nu	mbe	er																		
В	RW	CONNECT									Coi	nne	ctio	n																		
			Disconnected	1							Dis	con	nec	t																		
			Connected	0							Coi	nne	ct																			

33.8.9 FREQUENCY

Address offset: 0x524

TWI frequency

Bitı	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	АА		A
Res	et 0x0	4000000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	otic	on																			
Α	RW	FREQUENCY										TW	/I m	aste	er c	loc	k fr	equ	ıen	су														
			K100	0x	019	800	000					100) kb	ps																				
			K250	0x	040	0000	000					250) kb	ps																				
			K400	0x	064	000	000					400) kb	ps																				

33.8.10 RXD.PTR

Address offset: 0x534

Data pointer



В	Bit n	umb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	LO	9	8	7	6	5	4	3	2 :	1 0
lo	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α	Α	Α	Α	Α	Α	A A	А А
R	lese	t OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
le	d	RW	Field	Value Id	Va	lue							De	scri	pti	on																			
Α	١	RW	PTR										Da	ta p	oin	ter																			

33.8.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

D.1			24 20 2	0 20 2=			22.22		20.46		47.4	C 45		12 11		40 0	_	7	_	_		2		
Bit nu	ımber		31 30 2	9 28 27	26 2	5 24	23 22	2 21 .	20 19) T8	1/1	.6 15	14	13 14	2 11	10 9	8	/	6	5 4	1 3	2	1 ()
Id																		Α	Α	A A	A A	Α	Α Α	A
Rese	0x00000000		0 0 0	0 0	0 0	0	0 0	0	0 0	0	0	0 0	0	0 0	0	0 0	0	0	0	0 (0	0	0 ()
Id	RW Field	Value Id	Value				Desc	riptio	n															
Α	RW MAXCNT		[1255]				Maxi	mum	num	ber	of by	rtes i	n re	eive	buff	er								7

33.8.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bitı	numbe	er		31	30	29	28	27 2	6 2	25 2	4 2	3 2	2 21	1 20) 19	18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1 ()
Id																										Α	Α	Α	Α	Α	Α	A A	,
Res	et 0x0	0000000		0	0	0	0	0 () (0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	į
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion																			l
Α	R	AMOUNT									N	lum	ber	of	byte	s tr	rans	fer	red	in t	he l	ast	tran	sact	tior	ı. In	cas	e of	f				7
											N	ΙΔΟΙ	(or	ror	inc	lud	oc t∣	ha I	νας	`k'^	d h	ıtα											

33.8.13 RXD.LIST

Address offset: 0x540 EasyDMA list type

E	Bit n	umbe	er		31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3	2	1 0
1	d																																Α.	А А
F	Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0
ı	d	RW	Field	Value Id	Va	lue							Des	crip	otio	n																		
A	A	RW	LIST										List	typ	e																			
				Disabled	0								Disa	able	Ea	syD	MA	A lis	t															
				ArrayList	1								Use	arr	ay l	ist																		

33.8.14 TXD.PTR

Address offset: 0x544

Data pointer

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	.6 1	5 14	4 13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ /	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	PTR										Dat	ар	oin	ter																		

33.8.15 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer



	Bit number		31 30 29 26 27 20 23 24 23 22	2 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	d			A A A A A A A
1	Reset 0x00000000		0 0 0 0 0 0 0 0 0	
				utuatuu.
	ld RW Field	Value Id	Value Descri	ription

33.8.16 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bitı	numbe	er		31	30	29	28 2	27 2	6 2	25 2	4 2	3 22	2 21	. 20	19	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3 2	2 :	1 0
Id																											Α	Α	Α	Α	A A	A A	4 А
Res	et 0x0	0000000		0	0	0	0	0 0) (0 (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						D	esc	ripti	ion																			
Α	R	AMOUNT									Ν	lum	ber	of I	oyte	s tr	ans	feri	ed	in t	he I	ast	tra	ารลด	tio	n. I	n c	ase	of				
												IVCK	ori	or	inc	uda	ac tl	h o N	ייי	K'o	d h	ıtα											

33.8.17 TXD.LIST

Address offset: 0x550 EasyDMA list type

Bitı	numbe	er		31	L 30	29	28	27	26	25	24	23	22 2	21 2	20 1	19	18 :	17	16	15	14	13 :	12 1	.1 1	0 9	8	7	6	5	4	3	2	1 0
Id																																Α	АА
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							Des	crip	otio	n																		
Α	RW	LIST										List	typ	e																			
			Disabled	Λ								Dic	able	Ea	CVD		\ lia	+															
			Disabled	U								DIS	abic	: La	Syu	IVIA	A IIS	ι															

33.8.18 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bit n	umbe	r		31	30	29 :	28 2	7 26	5 25	5 24	1 23	22	21	20	19	18	17 :	16 :	15 1	.4 1	3 1	2 11	. 10	9	8	7	6	5	4	3 2	1	L 0
Id																											Α	Α	Α	A A	. 4	АА
Rese	t 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						De	scri	ptic	on																		
Α	RW	ADDRESS									Ad	dre	ss u	sed	l in	the	TW	/I tr	ans	fer												

33.9 Electrical specification

33.9.1 TWIM interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIM}	Bit rates for TWIM ³⁰	100		400	kbps
I _{TWIM,100kbps}	Run current for TWIM, 100 kbps		50		μΑ
I _{TWIM,400kbps}	Run current for TWIM, 400 kbps		50		μΑ
t _{TWIM,START,LP}	Time from STARTRX/STARTTX task to transmission started, Low		t _{TWIM,ST}	AR1	μs
	power mode		+		
			t _{START_H}	FIN	
t _{TWIM,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1.5		μs
	Constant latency mode				

Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



33.9.2 Two Wire Interface Master (TWIM) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIM,SCL,100kbps}	SCL clock frequency, 100 kbps		100		kHz
f _{TWIM,SCL,250kbps}	SCL clock frequency, 250 kbps		250		kHz
f _{TWIM,SCL,400kbps}	SCL clock frequency, 400 kbps		400		kHz
t _{TWIM,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWIM,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
$t_{TWIM,HD_STA,100kbps}$	TWIM master hold time for START and repeated START condition, 100 kbps	10000			ns
t _{TWIM,HD_STA,250kbps}	TWIM master hold time for START and repeated START condition, 250kbps	4000			ns
$t_{TWIM,HD_STA,400kbps}$	TWIM master hold time for START and repeated START condition, 400 kbps	2500			ns
t _{TWIM} ,SU_STO,100kbps	TWIM master setup time from SCL high to STOP condition, 100 kbps	5000			ns
t _{TWIM} ,SU_STO,250kbps	TWIM master setup time from SCL high to STOP condition, 250 kbps	2000			ns
t _{TWIM} ,su_sto,400kbps	TWIM master setup time from SCL high to STOP condition, 400 kbps	1250			ns
t _{TWIM} ,BUF,100kbps	TWIM master bus free time between STOP and START conditions, 100 kbps	5800			ns
t _{TWIM,BUF,250kbps}	TWIM master bus free time between STOP and START conditions, 250 kbps	2700			ns
t _{TWIM} ,BUF,400kbps	TWIM master bus free time between STOP and START conditions, 400 kbps	2100			ns

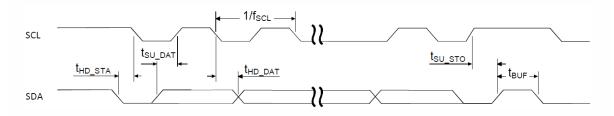


Figure 84: TWIM timing diagram, 1 byte transaction

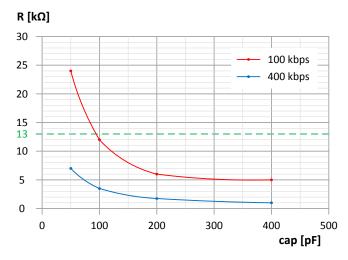


Figure 85: Recommended TWIM pullup value vs. line capacitance

- The I2C specification allows a line capacitance of 400 pF at most.
- The nRF52832 internal pullup has a fixed value of typ. 13 kOhm, see R_{PU} in the GPIO chapter.



34 TWIS — I²C compatible two-wire interface slave with EasyDMA

TWI slave with EasyDMA (TWIS) is compatible with I²C operating at 100 kHz and 400 kHz. The TWI transmitter and receiver implement EasyDMA.

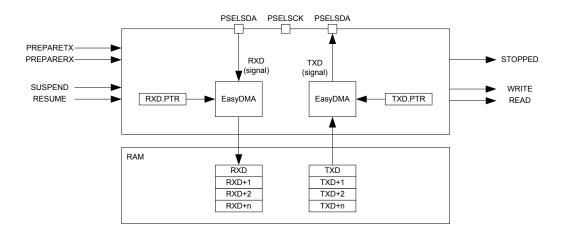


Figure 86: TWI slave with EasyDMA

A typical TWI setup consists of one master and one or more slaves. For an example, see *Figure 87: A typical TWI setup comprising one master and three slaves* on page 319. TWIS is only able to operate with a single master on the TWI bus.

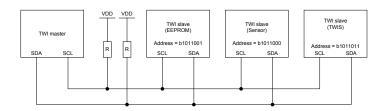


Figure 87: A typical TWI setup comprising one master and three slaves

The TWI slave state machine is illustrated in *Figure 88: TWI slave state machine* on page 320 and *Table 77: TWI slave state machine symbols* on page 320 is explaining the different symbols used in the state machine.



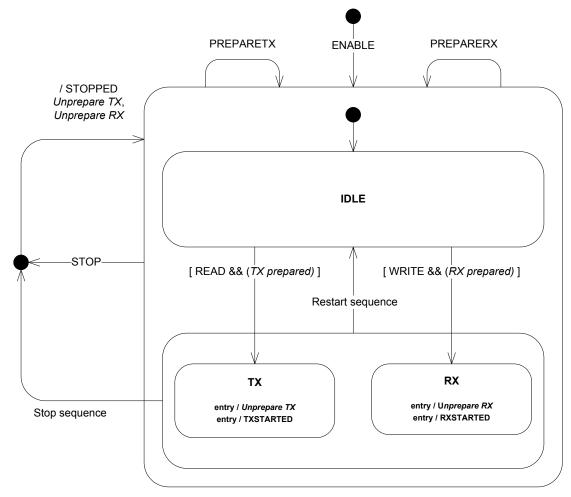


Figure 88: TWI slave state machine

Table 77: TWI slave state machine symbols

Symbol	Туре	Description
ENABLE	Register	The TWI slave has been enabled via the <i>ENABLE</i> register
PREPARETX	Task	The TASKS_PREPARETX task has been triggered
STOP	Task	The TASKS_STOP task has been triggered
PREPARERX	Task	The TASKS_PREPARERX task has been triggered
STOPPED	Event	The EVENTS_STOPPED event was generated
RXSTARTED	Event	The EVENTS_RXSTARTED event was generated
TXSTARTED	Event	The EVENTS_TXSTARTED event was generated
TX prepared	Internal	Internal flag indicating that a TASKS_PREPARETX task has been triggered. This flag is not visible to the user.
RX prepared	Internal	Internal flag indicating that a TASKS_PREPARERX task has been triggered. This flag is not visible to the user.
Unprepare TX	Internal	Clears the internal 'TX prepared' flag until next TASKS_PREPARETX task.
Unprepare RX	Internal	Clears the internal 'RX prepared' flag until next TASKS_PREPARERX task.
Stop sequence	TWI protocol	A TWI stop sequence was detected
Restart sequence	TWI protocol	A TWI restart sequence was detected

The TWI slave supports clock stretching performed by the master.

The TWI slave operates in a low power mode while waiting for a TWI master to initiate a transfer. As long as the TWI slave is not addressed, it will remain in this low power mode.

To secure correct behaviour of the TWI slave, PSEL.SCL, PSEL.SDA, CONFIG and the ADDRESS[n] registers, must be configured prior to enabling the TWI slave through the ENABLE register. Similarly, changing these settings must be performed while the TWI slave is disabled. Failing to do so may result in unpredictable behaviour.



34.1 Shared resources

The TWI slave shares registers and other resources with other peripherals that have the same ID as the TWI slave.

Therefore, you must disable all peripherals that have the same ID as the TWI slave before the TWI slave can be configured and used. Disabling a peripheral that has the same ID as the TWI slave will not reset any of the registers that are shared with the TWI slave. It is therefore important to configure all relevant registers explicitly to secure that the TWI slave operates correctly.

The Instantiation table in *Instantiation* on page 24 shows which peripherals have the same ID as the TWI slave.

34.2 EasyDMA

The TWI slave implements EasyDMA for reading and writing to and from the RAM.

The STOPPED event indicates that EasyDMA has finished accessing the buffer in RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

34.3 TWI slave responding to a read command

Before the TWI slave can respond to a read command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{\rm IDLE}$.

A read command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the TWI slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the read command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a READ event when it acknowledges the read command.

The TWI slave is only able to detect a read command from the IDLE state.

The TWI slave will set an internal 'TX prepared' flag when the PREPARETX task is triggered.

When the read command is received the TWI slave will enter the TX state if the internal 'TX prepared' flag is set.

If the internal 'TX prepared' flag is not set when the read command is received, the TWI slave will stretch the master's clock until the PREPARETX task is triggered and the internal 'TX prepared' flag is set.

The TWI slave will generate the TXSTARTED event and clear the 'TX prepared' flag ('unprepare TX') when it enters the TX state. In this state the TWI slave will send the data bytes found in the transmit buffer to the master using the master's clock. The TWI slave will consume I_{TX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the TX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the 'TX prepared' flag ('unprepare TX') and go back to the IDLE state when it has stopped.

The transmit buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to send TXD.MAXCNT bytes from the transmit buffer for each transaction. If the TWI master



forces the slave to send more than TXD.MAXCNT bytes, the slave will send the byte specified in the ORC register to the master instead. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see TXD.PTR etc., are latched when the TXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the 'TX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 324.

Each byte sent from the slave will be followed by an ACK/NACK bit sent from the master. The TWI master will generate a NACK following the last byte that it wants to receive to tell the slave to release the bus so that the TWI master can generate the stop condition. The TXD.AMOUNT register can be queried after a transaction to see how many bytes were sent.

A typical TWI slave read command response is illustrated in *Figure 89: The TWI slave responding to a read command* on page 322. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

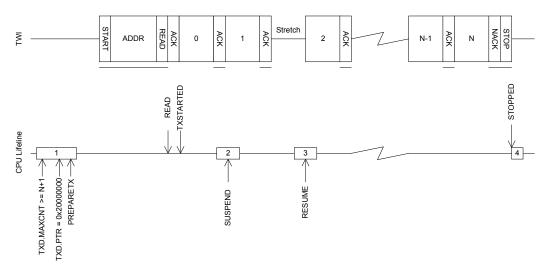


Figure 89: The TWI slave responding to a read command

34.4 TWI slave responding to a write command

Before the TWI slave can respond to a write command the TWI slave must be configured correctly and enabled via the ENABLE register. When enabled the TWI slave will be in its IDLE state where it will consume $I_{\rm IDLE}$.

A write command is started when the TWI master generates a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1). The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) response from the slave.

The TWI slave is able to listen for up to two addresses at the same time. Which addresses to listen for is configured in the ADDRESS registers and the CONFIG register.

The TWI slave will only acknowledge (ACK) the write command if the address presented by the master matches one of the addresses the slave is configured to listen for. The TWI slave will generate a WRITE event if it acknowledges the write command.

The TWI slave is only able to detect a write command from the IDLE state.

The TWI slave will set an internal 'RX prepared' flag when the PREPARERX task is triggered.

When the write command is received the TWI slave will enter the RX state if the internal 'RX prepared' flag is set.

If the internal 'RX prepared' flag is not set when the write command is received, the TWI slave will stretch the master's clock until the PREPARERX task is triggered and the internal 'RX prepared' flag is set.



The TWI slave will generate the RXSTARTED event and clear the internal 'RX prepared' flag ('unprepare RX') when it enters the RX state. In this state the TWI slave will be able to receive the bytes sent by the TWI master. The TWI slave will consume I_{RX} in this mode.

The TWI slave will go back to the IDLE state if the TWI slave receives a restart command when it is in the RX state.

The TWI slave is stopped when it receives the stop condition from the TWI master. A STOPPED event will be generated when the transaction has stopped. The TWI slave will clear the internal 'RX prepared' flag ('unprepare RX') and go back to the IDLE state when it has stopped.

The receive buffer is located in RAM at the address specified in the TXD.PTR register. The TWI slave will only be able to receive as many bytes as specified in the RXD.MAXCNT register. If the TWI master tries to send more bytes to the slave than the slave is able to receive, these bytes will be discarded and the bytes will be NACKed by the slave. If this happens, an ERROR event will be generated.

The EasyDMA configuration registers, see RXD.PTR etc., are latched when the RXSTARTED event is generated.

The TWI slave can be forced to stop by triggering the STOP task. A STOPPED event will be generated when the TWI slave has stopped. The TWI slave will clear the internal 'RX prepared' flag and go back to the IDLE state when it has stopped, see also *Terminating an ongoing TWI transaction* on page 324.

The TWI slave will generate an ACK after every byte received from the master. The RXD.AMOUNT register can be queried after a transaction to see how many bytes were received.

A typical TWI slave write command response is illustrated in *Figure 90: The TWI slave responding to a write command* on page 323. Occurrence 2 in the figure illustrates clock stretching performed by the TWI slave following a SUSPEND task.

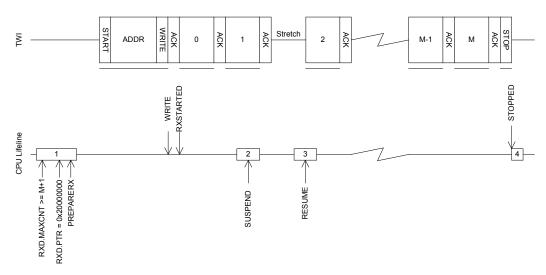


Figure 90: The TWI slave responding to a write command

34.5 Master repeated start sequence

An example of a repeated start sequence is one in which the TWI master writes two bytes to the slave followed by reading four bytes from the slave.

This is illustrated in Figure 91: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave on page 324.

It is here assumed that the receiver does not know in advance what the master wants to read, and that this information is provided in the first two bytes received in the write part of the repeated start sequence. To guarantee that the CPU is able to process the received data before the TWI slave starts to reply to the read command, the SUSPEND task is triggered via a shortcut from the READ event generated when the read command is received. When the CPU has processed the incoming data and prepared the correct data response, the CPU will resume the transaction by triggering the RESUME task.



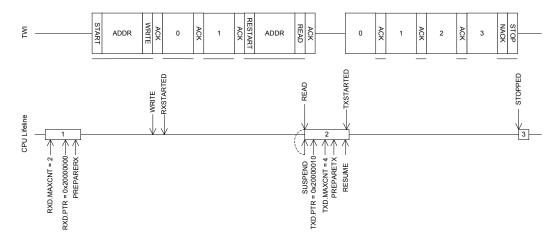


Figure 91: A repeated start sequence, where the TWI master writes two bytes followed by reading four bytes from the slave

34.6 Terminating an ongoing TWI transaction

In some situations, e.g. if the external TWI master is not responding correctly, it may be required to terminate an ongoing transaction.

This can be achieved by triggering the STOP task. In this situation a STOPPED event will be generated when the TWI has stopped independent of whether or not a STOP condition has been generated on the TWI bus. The TWI slave will release the bus when it has stopped and go back to its IDLE state.

34.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

34.8 Slave mode pin configuration

The SCL and SDA signals associated with the TWI slave are mapped to physical pins according to the configuration specified in the PSEL.SCL and PSEL.SDA registers respectively.

The PSEL.SCL and PSEL.SDA registers and their configurations are only used as long as the TWI slave is enabled, and retained only as long as the device is in ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register. PSEL.SCL and PSEL.SDA must only be configured when the TWI slave is disabled.

To secure correct signal levels on the pins used by the TWI slave when the system is in OFF mode, and when the TWI slave is disabled, these pins must be configured in the GPIO peripheral as described in *Table 78: GPIO configuration before enabling peripheral* on page 324.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 78: GPIO configuration before enabling peripheral

TWI slave signal	TWI slave pin	Direction	Output value	Drive strength
SCL	As specified in PSEL.SCL	Input	Not applicable	SOD1
SDA	As specified in PSEL.SDA	Input	Not applicable	S0D1



34.9 Registers

Table 79: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40003000	TWIS	TWIS0	Two-wire interface slave 0	
0x40004000	TWIS	TWIS1	Two-wire interface slave 1	

Table 80: Register Overview

Register	Offset	Description
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
TASKS_PREPARERX	0x030	Prepare the TWI slave to respond to a write command
TASKS_PREPARETX	0x034	Prepare the TWI slave to respond to a read command
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_ERROR	0x124	TWI error
EVENTS_RXSTARTED	0x14C	Receive sequence started
EVENTS_TXSTARTED	0x150	Transmit sequence started
EVENTS_WRITE	0x164	Write command received
EVENTS_READ	0x168	Read command received
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4D0	Error source
MATCH	0x4D4	Status register indicating which address had a match
ENABLE	0x500	Enable TWIS
PSEL.SCL	0x508	Pin select for SCL signal
PSEL.SDA	0x50C	Pin select for SDA signal
RXD.PTR	0x534	RXD Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in RXD buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last RXD transaction
TXD.PTR	0x544	TXD Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in TXD buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last TXD transaction
ADDRESS[0]	0x588	TWI slave address 0
ADDRESS[1]	0x58C	TWI slave address 1
CONFIG	0x594	Configuration register for the address match mechanism
ORC	0x5C0	Over-read character. Character sent out in case of an over-read of the transmit buffer.

34.9.1 SHORTS

Address offset: 0x200

Shortcut register

Bitı	numbe	er		3:	1 30	29	2	8 2	7 2	6 2	5 2	24 2	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																						В	Α													
Res	et 0x0	0000000		0	0	0	C	0) (0 ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	V	alue								Des	scri	iptic	n																				
Α	RW	WRITE_SUSPEND										9	Sho	orto	cut k	etv	wee	n۱	VRI	ΓΕ (eve	nt a	and	SU	SPE	ND	tas	k								
												9	See	E\	VEN	TS_	W	RITE	an	<i>T</i> ,	4 <i>SK</i>	S_5	sus	PEN	ID											
			Disabled	0								[Disa	abl	le sh	ort	cut																			
			Enabled	1								E	Ena	ble	e sh	orto	cut																			
В	RW	READ_SUSPEND										9	Sho	orto	cut k	etv	wee	n F	EAI) e	ven	t a	nd :	SUS	PEN	ND t	ask									
												9	See	e <i>E</i> \	VEN	TS_	RE	4 <i>D</i> :	and	TΑ	SKS	_S	USF	ENI	D											



Bit number		31 30 29 28 27	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			B A
Reset 0x00000000		0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id RW Field	Value Id	Value	Description
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

34.9.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit ı	numbe	r		33	1 30	29	28	27 2	26 2	25 2	24 23	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id									Н	G				F	Ε										В							A	Ą
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0) () 0
ld	RW	Field	Value Id	V	alue						D	esc	ripti	on																			
Α	RW	STOPPED									Er	nab	ole or	r di	sab	le iı	nter	rup	t fo	or S	ТОР	PEI	D e	vent	t								
											Se	ee E	EVEN	VTS	_57	OPI	PED																
			Disabled	0							Di	isat	ble																				
			Enabled	1							Er	nab	ole																				
В	RW	ERROR									Er	nab	ole or	r di	sab	le ii	nter	rup	t fo	r E	RRC)R e	eve	nt									
											Se	ee E	EVEN	VTS.	_ER	RO	R																
			Disabled	0							Di	isat	ble																				
			Enabled	1							Er	nab	ole																				
Ε	RW	RXSTARTED									Er	nab	ole or	r di	sab	le ii	nter	rup	t fo	r R	XST	AR٦	TEC	eve	ent								
											Se	ee E	EVEN	VTS.	_ <i>R x</i>	(STA	\RT	ED															
			Disabled	0							Di	isat	ble																				
			Enabled	1							Er	nab	ole																				
F	RW	TXSTARTED									Er	nab	ole or	r di	sab	le iı	nter	rup	t fo	or T	XST.	AR1	ΓED	eve	ent								
											Se	ee E	EVEN	VTS.	_ <i>T</i> x	STA	RTI	ED															
			Disabled	0							Di	isat	ble																				
			Enabled	1							Er	nab	ole																				
G	RW	WRITE									Er	nab	ole o	r di	sab	le iı	nter	rup	t fo	or W	/RIT	Еe	vei	nt									
											Se	ee E	EVEN	VTS.	_w	RIT	E																
			Disabled	0							Di	isat	ble																				
			Enabled	1							Er	nab	ole																				
Н	RW	READ									Er	nab	ole or	r di	sab	le iı	nter	rup	t fo	r R	EAC	ev	en ⁻	t									
											Se	ee E	EVEN	VTS.	RE	AD																	
			Disabled	0							Di	isak	ble																				
			Enabled	1							Er	nab	ole																				

34.9.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31 30	29	9 28	8 27	7 26	25	24	23	22	21 2	0	19 1	8 2	17 1	6 1	.5 1	4 13	3 12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id								Н	G					F	Ε									В							Α	
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0	0	0 (0 0	0	0	0
Id	RW	Field	Value Id	Valu	9						De	scri	ptio	n																		
Α	RW	STOPPED									Wr	ite	'1' to	Eı	nab	e iı	nter	rup	t fo	r ST	OPF	PED	eve	nt								
											See	e EV	ENT	S_ .	sto	PPE	ED															
			Set	1							Ena	able	•																			
			Disabled	0							Rea	ad:	Disa	ble	d																	
			Enabled	1							Rea	ad:	Enak	ole	d																	
В	RW	ERROR									Wr	ite	'1' to	Eı	nab	e ii	nter	rup	t fo	r ER	ROF	R ev	ent									



Bit number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	H G	F E B A
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
		See EVENTS_ERROR
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
E RW RXSTARTED		Write '1' to Enable interrupt for RXSTARTED event
		See EVENTS_RXSTARTED
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
F RW TXSTARTED		Write '1' to Enable interrupt for TXSTARTED event
		See EVENTS_TXSTARTED
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
G RW WRITE		Write '1' to Enable interrupt for WRITE event
		See EVENTS_WRITE
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
H RW READ	-	Write '1' to Enable interrupt for READ event
		See EVENTS_READ
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled

34.9.4 INTENCLR

Address offset: 0x308

Disable interrupt

Rit r	numbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld.				H G	F E B A
	et OxO	000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Value	Description
Α	RW	STOPPED			Write '1' to Disable interrupt for STOPPED event
					See EVENTS_STOPPED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	ERROR			Write '1' to Disable interrupt for ERROR event
					See EVENTS_ERROR
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Е	RW	RXSTARTED			Write '1' to Disable interrupt for RXSTARTED event
					See EVENTS_RXSTARTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
F	RW	TXSTARTED			Write '1' to Disable interrupt for TXSTARTED event
					See EVENTS_TXSTARTED
			Clear	1	Disable



Bit number	31 30 29 28 27 26	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	Н	IG FE B A
Reset 0x00000000	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
G RW WRITE		Write '1' to Disable interrupt for WRITE event
		See EVENTS_WRITE
Clear	1	Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled
H RW READ		Write '1' to Disable interrupt for READ event
		See EVENTS_READ
Clear	1	Disable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled

34.9.5 ERRORSRC

Address offset: 0x4D0

Error source

Bit r	numbe	er		31	30	29	28 2	7 2	26 2	5 2	24 2	3 22	21	20	19 1	18 3	17 3	16 :	15 :	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																														C E	3	Α
Res	et 0x0	0000000		0	0	0	0 (כ	0 (0	0 (0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D	escri	iptio	n																		
Α	RW	OVERFLOW									R	X bu	ffer	ove	rflo	w c	lete	cte	d, a	and	pre	ven	ted									
			NotDetected	0							Ε	ror	did r	ot	осс	ur																
			Detected	1							Ε	rror	occu	irre	d																	
В	RW	DNACK									N	ACK	sent	af	ter ı	ece	ivi	ng a	da	ta k	oyte											
			NotReceived	0							Е	ror	did r	ot	осс	ur																
			Received	1							Ε	rror	occu	irre	d																	
С	RW	OVERREAD									T	X bu	ffer	ove	r-re	ad	det	ect	ed,	and	d pr	evei	nted									
			NotDetected	0							Ε	ror	did r	ot	осс	ur																
			Detected	1							Ε	rror	occu	ırre	d																	

34.9.6 MATCH

Address offset: 0x4D4

Status register indicating which address had a match

Bitı	numbe	er		31	30	29 :	28 2	27 26	5 25	5 24	23	22	21 2	20 1	19 1	.8 1	7 16	5 15	14	13	12	11 1	.0 9	8	7	6	5	4	3	2 :	1 0
Id																															Α
Res	et 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0
ld	RW	Field	Value Id	Va	lue						De	scri	otio	n																	
Α	R	MATCH		[0.	.1]						W	nich	of t	he a	add	ress	es i	n {A	DDI	RES	s} m	atcl	ned 1	the	inco	mi	ng				
											ad	dres	s																		

34.9.7 ENABLE

Address offset: 0x500

Enable TWIS

Bit	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				АААА
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW ENABLE			Enable or disable TWIS
		Disabled	0	Disable TWIS



	Enabled	0	Enable TWIS	
Id RW Field	Value Id	Value	Description	
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id				АААА
Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13	3 12 11 10 9 8 7 6 5 4 3 2 1 0

34.9.8 PSEL.SCL

Address offset: 0x508

Pin select for SCL signal

Bit r	numbe	r		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	$1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.9.9 PSEL.SDA

Address offset: 0x50C Pin select for SDA signal

Bit r	umbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	t 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

34.9.10 RXD.PTR

Address offset: 0x534 RXD Data pointer

Bit	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	9 8	3 7	7 6	5 5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	۸ ۸	A A	Δ ,	\ <i>A</i>	Α Δ	A	Α	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () () () (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	PTR										RXI	D D	ata	poi	nte	r																	7

34.9.11 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in RXD buffer

В	it numbe	er		31	30	29 :	28 2	7 26	6 25	5 24	1 23	22	21	20	19	18	17	16	15 1	L4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Ic	1																									Α	Α	Α	A ,	4 A	. A	A
R	eset 0x0	0000000		0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Ic	l RW	Field	Value Id	Va	lue						De	escr	ipti	on																		
Α	RW	MAXCNT									М	axir	nun	า ทน	ımb	er c	of b	vte	s in	RXI) bu	ıffe										

34.9.12 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last RXD transaction



Bit r	iumbe	er		31	30 :	29	28 2	27 2	6 2	25 2	24 2	23 2	22 2	1 2	0 1	9 18	8 17	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	L 0
Id																											Α	Α	Α	Α	Α	A A	A A
Res	et 0x0	0000000		0	0	0	0	0 (0 (0	0	0	0 0) () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue						1	Des	crip	tior	1																		
Α	R	AMOUNT									ı	Nun	nber	r of	byt	es t	ran	sfei	red	in	the	last	t RX	D tr	an	sact	ior	1					

34.9.13 TXD.PTR

Address offset: 0x544
TXD Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value Description
A RW PTR		TXD Data pointer

34.9.14 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in TXD buffer

Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW MAXCNT		Maximum number of bytes in TXD buffer

34.9.15 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last TXD transaction

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	O
Id																												Α	Α	Α	Α	Α .	Δ	Α	4
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	כ
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				
Α	R	AMOUNT										Nu	mb	er c	of b	yte	s tr	ans	feri	red	in 1	he	last	TX	D tr	ans	sact	ion							7

34.9.16 ADDRESS[0]

Address offset: 0x588 TWI slave address 0

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id					A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
A RW ADDRESS			TWI slave address		

34.9.17 ADDRESS[1]

Address offset: 0x58C TWI slave address 1

Bit number	31 30 29 28 2	27 26 25 24 23 22 21 20 19 18 1	17 16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id				A A A A A A
Reset 0x00000000	0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field Value	Id Value	Description		

RW ADDRESS TWI slave address



34.9.18 CONFIG

Address offset: 0x594

Configuration register for the address match mechanism

Bit r	iumbe	er		31	L 30	29	28	8 27	7 2	6 25	5 2	4 2	3 22	2 2:	1 20	0 1	9 1	8 1	.7 1	.6 :	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			В	Α
Res	et 0x0	0000001		0	0	0	0	0	•	0	0) (0	0	0	•	0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Id	RW	Field	Value Id	Va	alue							D	esc	ript	tion																					
Α	RW	ADDRESS0										Е	nab	le c	or d	isal	ble	ad	dre	ss r	ma	:chi	ng	on	ΑD	DR	ESS	[0]								
			Disabled	0								D	isab	lec	t																					
			Enabled	1								Е	nab	led																						
В	RW	ADDRESS1										Е	nab	le c	or d	isal	ble	ad	dre	ss r	ma	chi	ng	on	ΑD	DR	ESS	[1]								
			Disabled	0								D	isab	lec	t																					
			Enabled	1								Е	nab	led																						

34.9.19 ORC

Address offset: 0x5C0

Over-read character. Character sent out in case of an over-read of the transmit buffer.

Bit	numbe	er		31 3	0 29	28	27 26	5 25	24	23	22 2	21 2	0 19	9 18	3 17	16	15	14	13 :	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																								Α	Α	Α	Α.	A A	Α	Α
Res	et 0x0	0000000		0 (0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	e					De	scrip	otio	n																	
Α	RW	ORC								Ove	er-re	ead	char	act	er. C	Chai	ract	er s	ent	out	in ca	se	of a	n o	ver-	read	d			
										of t	he t	ran	smit	hut	ffer															

34.10 Electrical specification

34.10.1 TWIS slave interface electrical specifications

Description	Min.	Тур.	Max.	Units
Bit rates for TWIS ³¹	100		400	kbps
Run current for TWIS (Average current to receive and transfer a		45		μΑ
byte to RAM), 100 kbps				
Run current for TWIS (Average current to receive and transfer a		45		μΑ
byte to RAM), 400 kbps				
Idle current for TWIS		1		μΑ
Time from PREPARERX/PREPARETX task to ready to receive/		t _{TWIS,START}	τ,	μs
transmit, Low power mode		+		
		t _{START_HFIN}	١	
Time from PREPARERX/PREPARETX task to ready to receive/		1.5		μs
transmit, Constant latency mode				
	Bit rates for TWIS ³¹ Run current for TWIS (Average current to receive and transfer a byte to RAM), 100 kbps Run current for TWIS (Average current to receive and transfer a byte to RAM), 400 kbps Idle current for TWIS Time from PREPARERX/PREPARETX task to ready to receive/ transmit, Low power mode Time from PREPARERX/PREPARETX task to ready to receive/	Bit rates for TWIS ³¹ 100 Run current for TWIS (Average current to receive and transfer a byte to RAM), 100 kbps Run current for TWIS (Average current to receive and transfer a byte to RAM), 400 kbps Idle current for TWIS Time from PREPARERX/PREPARETX task to ready to receive/ transmit, Low power mode Time from PREPARERX/PREPARETX task to ready to receive/	Bit rates for TWIS ³¹ Run current for TWIS (Average current to receive and transfer a byte to RAM), 100 kbps Run current for TWIS (Average current to receive and transfer a byte to RAM), 400 kbps Idle current for TWIS 1 Time from PREPARERX/PREPARETX task to ready to receive/transmit, Low power mode transfer a to the total receive to the t	Bit rates for TWIS ³¹ Run current for TWIS (Average current to receive and transfer a byte to RAM), 100 kbps Run current for TWIS (Average current to receive and transfer a byte to RAM), 400 kbps Idle current for TWIS Time from PREPARERX/PREPARETX task to ready to receive/ transmit, Low power mode Time from PREPARERX/PREPARETX task to ready to receive/ Time from PREPARERX/PREPARETX task to ready to receive/

34.10.2 TWIS slave timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWIS,SCL,400kbps}	SCL clock frequency, 400 kbps			400	kHz
t _{TWIS,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWIS,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWIS,HD_STA,100kbps}	TWI slave hold time from for START condition (SDA low to SCL	5200			ns
	low), 100 kbps				
t _{TWIS,HD_STA,400kbps}	TWI slave hold time from for START condition (SDA low to SCL	1300			ns
	low), 400 kbps				

Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
$t_{TWIS,SU_STO,100kbps}$	TWI slave setup time from SCL high to STOP condition, 100 kbps	5200			ns
t _{TWIS,SU_STO,400kbps}	TWI slave setup time from SCL high to STOP condition, 400 kbps	1300			ns
t _{TWIS,BUF,100kbps}	TWI slave bus free time between STOP and START conditions,		4700		ns
	100 kbps				
t _{TWIS,BUF,400kbps}	TWI slave bus free time between STOP and START conditions,		1300		ns
	400 khns				

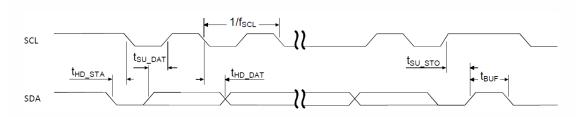


Figure 92: TWIS timing diagram, 1 byte transaction



35 UARTE — Universal asynchronous receiver/ transmitter with EasyDMA

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

Listed here are the main features for UARTE:

- Full-duplex operation
- · Automatic hardware flow control
- Parity checking and generation for the 9th data bit
- EasyDMA
- Up to 1 Mbps baudrate
- · Return to IDLE between transactions supported (when using HW flow control)
- One stop bit
- Least significant bit (LSB) first

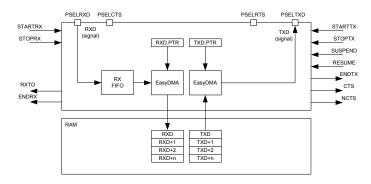


Figure 93: UARTE configuration

The GPIOs used for each UART interface can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

35.1 Shared resources

The UARTE shares registers and other resources with other peripherals that have the same ID as the UARTE.

Therefore, you must disable all peripherals that have the same ID as the UARTE before the UARTE can be configured and used. Disabling a peripheral that has the same ID as the UARTE will not reset any of the registers that are shared with the UARTE. It is therefore important to configure all relevant UARTE registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

35.2 EasyDMA

The UARTE implements EasyDMA for reading and writing to and from the RAM.

If the TXD.PTR and the RXD.PTR are not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.



The .PTR and .MAXCNT registers are double-buffered. They can be updated and prepared for the next RX/TX transmission immediately after having received the RXSTARTED/TXSTARTED event.

The ENDRX/ENDTX event indicates that EasyDMA has finished accessing respectively the RX/TX buffer in RAM.

35.3 Transmission

The first step of a DMA transmission is storing bytes in the transmit buffer and configuring EasyDMA. This is achieved by writing the initial address pointer to TXD.PTR, and the number of bytes in the RAM buffer to TXD.MAXCNT. The UARTE transmission is started by triggering the STARTTX task.

After each byte has been sent over the TXD line, a TXDRDY event will be generated.

When all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have been transmitted, the UARTE transmission will end automatically and an ENDTX event will be generated.

A UARTE transmission sequence is stopped by triggering the STOPTX task, a TXSTOPPED event will be generated when the UARTE transmitter has stopped.

If the ENDTX event has not already been generated when the UARTE transmitter has come to a stop, the UARTE will generate the ENDTX event explicitly even though all bytes in the TXD buffer, as specified in the TXD.MAXCNT register, have not been transmitted.

If flow control is enabled, a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 94: UARTE transmission* on page 334. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended.

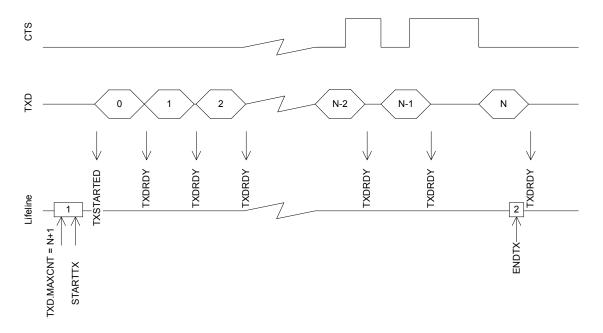


Figure 94: UARTE transmission

The UARTE transmitter will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTTX or after it has been stopped via STOPTX and the TXSTOPPED event has been generated. See *POWER* — *Power supply* on page 78 for more information about power modes.

35.4 Reception

The UARTE receiver is started by triggering the STARTRX task. The UARTE receiver is using EasyDMA to store incoming data in an RX buffer in RAM.



The RX buffer is located at the address specified in the RXD.PTR register. The RXD.PTR register is double-buffered and it can be updated and prepared for the next STARTRX task immediately after the RXSTARTED event is generated. The size of the RX buffer is specified in the RXD.MAXCNT register and the UARTE will generate an ENDRX event when it has filled up the RX buffer, see *Figure 95: UARTE reception* on page 335.

For each byte received over the RXD line, an RXDRDY event will be generated. This event is likely to occur before the corresponding data has been transferred to Data RAM.

The RXD.AMOUNT register can be queried following an ENDRX event to see how many new bytes have been transferred to the RX buffer in RAM since the previous ENDRX event.

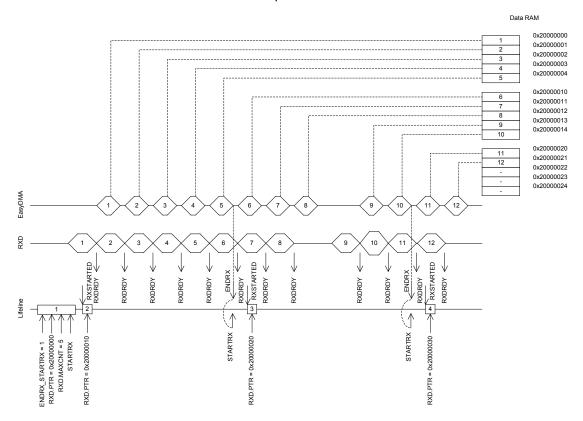


Figure 95: UARTE reception

The UARTE receiver is stopped by triggering the STOPRX task. An RXTO event is generated when the UARTE has stopped. The UARTE will make sure that an impending ENDRX event will be generated before the RXTO event is generated. This means that the UARTE will guarantee that no ENDRX event will be generated after RXTO, unless the UARTE is restarted or a FLUSHRX command is issued after the RXTO event is generated.

Important: If the ENDRX event has not already been generated when the UARTE receiver has come to a stop, which implies that all pending content in the RX FIFO has been moved to the RX buffer, the UARTE will generate the ENDRX event explicitly even though the RX buffer is not full. In this scenario the ENDRX event will be generated before the RXTO event is generated.

To be able to know how many bytes have actually been received into the RX buffer, the CPU can read the RXD.AMOUNT register following the ENDRX event or the RXTO event.

The UARTE is able to receive up to four bytes after the STOPRX task has been triggered as long as these are sent in succession immediately after the RTS signal is deactivated. This is possible because after the RTS is deactivated the UARTE is able to receive bytes for an extended period equal to the time it takes to send 4 bytes on the configured baud rate.

After the RXTO event is generated the internal RX FIFO may still contain data, and to move this data to RAM the FLUSHRX task must be triggered. To make sure that this data does not overwrite data in the RX buffer, the RX buffer should be emptied or the RXD.PTR should be updated before the FLUSHRX task is triggered.



To make sure that all data in the RX FIFO is moved to the RX buffer, the RXD.MAXCNT register must be set to RXD.MAXCNT > 4, see *Figure 96: UARTE reception with forced stop via STOPRX* on page 336. The UARTE will generate the ENDRX event after completing the FLUSHRX task even if the RX FIFO was empty or if the RX buffer does not get filled up. To be able to know how many bytes have actually been received into the RX buffer in this case, the CPU can read the RXD.AMOUNT register following the ENDRX event.

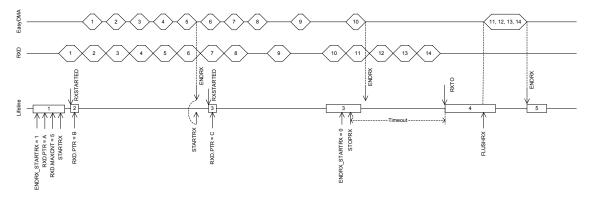


Figure 96: UARTE reception with forced stop via STOPRX

If HW flow control is enabled the RTS signal will be deactivated when the receiver is stopped via the STOPRX task or when the UARTE is only able to receive four more bytes in its internal RX FIFO.

With flow control disabled, the UARTE will function in the same way as when the flow control is enabled except that the RTS line will not be used. This means that no signal will be generated when the UARTE has reached the point where it is only able to receive four more bytes in its internal RX FIFO. Data received when the internal RX FIFO is filled up, will be lost.

The UARTE receiver will be in its lowest activity level, and consume the least amount of energy, when it is stopped, i.e. before it is started via STARTRX or after it has been stopped via STOPRX and the RXTO event has been generated. See *POWER* — *Power supply* on page 78 for more information about power modes.

35.5 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

An ERROR event will not stop reception. If the error was a parity error, the received byte will still be transferred into Data RAM, and so will following incoming bytes. If there was a framing error (wrong stop bit), that specific byte will NOT be stored into Data RAM, but following incoming bytes will.

35.6 Using the UARTE without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

35.7 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

35.8 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.



The STOPTX and STOPRX tasks may not be always needed (the peripheral might already be stopped), but if STOPTX and/or STOPRX is sent, software shall wait until the TXSTOPPED and/or RXTO event is received in response, before disabling the peripheral through the ENABLE register.

35.9 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UARTE are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.RTS, and PSEL.TXD registers respectively.

The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UARTE is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.RTS, PSEL.RTS and PSEL.TXD must only be configured when the UARTE is disabled.

To secure correct signal levels on the pins by the UARTE when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Table 81: GPIO configuration before enabling peripheral* on page 337.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 81: GPIO configuration before enabling peripheral

UARTE signal	UARTE pin	Direction	Output value
RXD	As specified in PSEL.RXD	Input	Not applicable
CTS	As specified in PSEL.CTS	Input	Not applicable
RTS	As specified in PSEL.RTS	Output	1
TXD	As specified in PSEL.TXD	Output	1

35.10 Registers

Table 82: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40002000	UARTE	UARTE0	Universal Asynchronous Receiver/	
			Transmitter with EasyDMA	

Table 83: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_FLUSHRX	0x02C	Flush RX FIFO into RX buffer
EVENTS CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x104	Data received in RXD (but potentially not yet transferred to Data RAM)
_		
EVENTS_ENDRX	0x110	Receive buffer is filled up
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ENDTX	0x120	Last TX byte transmitted
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
EVENTS_RXSTARTED	0x14C	UART receiver has started
EVENTS_TXSTARTED	0x150	UART transmitter has started
EVENTS_TXSTOPPED	0x158	Transmitter stopped
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt



Register	Offset	Description
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSEL.RTS	0x508	Pin select for RTS signal
PSEL.TXD	0x50C	Pin select for TXD signal
PSEL.CTS	0x510	Pin select for CTS signal
PSEL.RXD	0x514	Pin select for RXD signal
BAUDRATE	0x524	Baud rate. Accuracy depends on the HFCLK source selected.
RXD.PTR	0x534	Data pointer
RXD.MAXCNT	0x538	Maximum number of bytes in receive buffer
RXD.AMOUNT	0x53C	Number of bytes transferred in the last transaction
TXD.PTR	0x544	Data pointer
TXD.MAXCNT	0x548	Maximum number of bytes in transmit buffer
TXD.AMOUNT	0x54C	Number of bytes transferred in the last transaction
CONFIG	0x56C	Configuration of parity and hardware flow control

35.10.1 SHORTS

Address offset: 0x200 Shortcut register

Bit	numbe	er		31	1 30	29	28	27	26	25	24 2	23 22	2 21	20	19	18	17 1	16 1	15 1	4 1	3 1	2 11	. 10	9	8	7	6 !	5 4	3	2	1	0
Id																											D (2				
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0 0	0	0	0	0
Id	RW	Field	Value Id	Va	alue							Desc	ripti	on																		
С	RW	ENDRX_STARTRX									5	hort	cut	bet	wee	n E	NDF	RX e	ver	nt a	nd S	TAR	TRX	tas	k							
											5	See E	VEN	ITS_	ENL	ORX	and	d T /	ISK.	s_ <i>s</i> :	TAR	TRX										
			Disabled	0							[Disab	le sl	hort	cut																	
			Enabled	1							E	Enab	le sh	ort	cut																	
D	RW	ENDRX_STOPRX									S	Short	cut	bet	wee	n E	NDF	RX e	ver	nt a	nd S	TOF	PRX	task								
											S	See E	VEN	ITS_	ENL	ORX	and	d T /	ISK.	s_s:	ТОР	RX										
			Disabled	0								Disab	le sl	hort	tcut																	
			Enabled	1							E	nab	le sh	ort	cut																	

35.10.2 INTEN

Address offset: 0x300 Enable or disable interrupt

umbe	r		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
				L J I H G F E D C B A
t 0x0	0000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
RW	Field	Value Id	Value	Description
RW	CTS			Enable or disable interrupt for CTS event
				See EVENTS_CTS
		Disabled	0	Disable
		Enabled	1	Enable
RW	NCTS			Enable or disable interrupt for NCTS event
				See EVENTS_NCTS
		Disabled	0	Disable
		Enabled	1	Enable
RW	RXDRDY			Enable or disable interrupt for RXDRDY event
				See EVENTS_RXDRDY
		Disabled	0	Disable
		Enabled	1	Enable
RW	ENDRX			Enable or disable interrupt for ENDRX event
				See EVENTS_ENDRX
	RW RW	RW Field RW CTS RW NCTS RW RXDRDY RW ENDRX	RW Field Value Id RW CTS Disabled Enabled RW NCTS Disabled Enabled RW NCTS Disabled Enabled Enabled	Cox000000000



Bitı	numbe	er		31 30	29	28 2	7 26	5 25	24	23 :	22 21	1 2	0 19	18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id											L	J	-1		Н								G	F	Ε			D		C I	ВА
Res	et 0x0	0000000		0 0	0	0 (0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value						Des	cript	ion	ı																		
			Disabled	0						Disa	able																				
			Enabled	1						Ena	ble																				
Ε	RW	TXDRDY								Ena	ble o	r d	isab	le i	nter	ru	ot fo	or T	XD	RD۱	ev ev	ent	:								
										See	EVEI	NTS	_ <i>T</i> X	(DR	DΥ																
			Disabled	0						Disa	able																				
			Enabled	1						Ena	ble																				
F	RW	ENDTX								Ena	ble o	r d	isab	le i	nter	ru	ot fo	or E	ND	TX	eve	nt									
										See	EVEI	NTS	S EN	VD7	X																
			Disabled	0							able		_																		
			Enabled	1						Ena																					
G	RW	ERROR								Ena	ble o	r d	isab	le i	nter	ru	ot fo	or E	RR	OR	eve	nt									
										500	EVEI	NIT		200	ıD.																
			Disabled	0							able	VIS		inu	'n																
			Enabled	1						Ena																					
Н	RW	RXTO	Enablea	•							ible o	r d	isab	ıle i	nter	rui	ot fo	or F	XT	o e	ven	t									
																- 1															
			Disabled	0							EVEI	N I S	_ <i>K</i>)	KIO																	
			Disabled Enabled	0						Ena	able																				
1	R\M/	RXSTARTED	Ellableu	1							ible ible o	ır d	icah	i alı	nter	riii	at fo	or F	XC.	ΓΔR	TFI	۱ ۵۰	/en	+							
	11.00	MOTANTED															JC 10	,,,,	I/IJ	171		<i>,</i>	CII								
											EVEI	NTS	5_ <i>R</i>)	(ST)	4RT	ED															
			Disabled	0							able																				
	DIM	TVCTARTER	Enabled	1						Ena										- 4 0	-										
J	KW	TXSTARTED								Ena	ble o	r a	ısab	ie i	nter	ru	ot to	or i	XS	IAK	IEL) ev	/eni	τ							
										See	EVEI	NTS	_ <i>T</i> X	(ST)	4RT	ED															
			Disabled	0							able																				
			Enabled	1						Ena																					
L	RW	TXSTOPPED								Ena	ble o	r d	isab	le i	nter	ru	ot fo	or T	XS	ГОР	PEI) e	/en	t							
										See	EVEI	NTS	5_ <i>T</i> X	(ST	OPP	ED															
			Disabled	0						Disa	able																				
			Enabled	1						Ena	ble																				

35.10.3 INTENSET

Address offset: 0x304 Enable interrupt

Bit r	numbe	er		31	30 2	9 2	8 2	7 2	6 25	5 2	4 2	3 2	2 2:	1 20	19	18	3 17	7 16	15	14	13	12	11	10	9	8 7	' (5 5	4	3	2	1 0
Id												L	-	J	-1		Н	l							G	F E			D		С	ВА
Res	et 0x0	0000000		0	0	0 (0 0) (0 0	() (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						C)esc	ript	tion																		
Α	RW	CTS									٧	Vrite	e '1	' to	Ena	ble	int	terr	upt	for	CTS	ev	ent									
											S	ee E	VE	NTS	_c	rs																
			Set	1							Е	nab	le																			
			Disabled	0							R	lead	l: Di	isab	led																	
			Enabled	1							R	lead	l: Er	nabl	ed																	
В	RW	NCTS									٧	Vrite	e '1	' to	Ena	ble	int	terr	upt	for	NC	TS e	ver	it								
											S	ee E	VE	NTS	_N	CTS																
			Set	1							Е	nab	le																			
			Disabled	0							R	lead	l: Di	isab	led																	
			Enabled	1							R	lead	l: Er	nabl	ed																	
С	RW	RXDRDY									٧	Vrite	e '1	' to	Ena	ble	int	terr	upt	for	RXI	ORD	Υe	vent	t							



Bit	numbe	er		31 30	29	28 27	7 26 :	25 24	23 22 21	20 19 :	18 17	16 15	14 1	3 12	11 1	0 9	8	7	6 5	4	3	2 1	. 0
Id -										JI	Н						F			D		СВ	
		0000000	Value Id		0	0 0	0	0 0	0 0 0		0 0	0 0	0 (0 0	0 (0	0	0	0 0	0	0	0 0	0
ld	KVV	Field	Value Id	Value					See EVEN		RDV												
			Set	1					Enable	13_NAL	וטוי												
			Disabled	0					Read: Disa	abled													
			Enabled	1					Read: Ena														
D	RW	ENDRX							Write '1' t		le inte	errupt	for El	NDR)	(eve	nt							
									See <i>EVEN</i>	TS ENL	DRX												
			Set	1					Enable	_													
			Disabled	0					Read: Disa	abled													
			Enabled	1					Read: Ena	bled													
Ε	RW	TXDRDY							Write '1' t	o Enab	le inte	errupt	for T	KDRD	Y eve	ent							
									See <i>EVEN</i>	TS_TXD	RDY												
			Set	1					Enable														
			Disabled	0					Read: Disa	abled													
			Enabled	1					Read: Ena	bled													
F	RW	ENDTX							Write '1' t	o Enab	le inte	errupt	for El	NDTX	(ever	nt							
									See <i>EVEN</i>	TS_ENE	OTX												
			Set	1					Enable														
			Disabled	0					Read: Disa														
			Enabled	1					Read: Ena														
G	RW	ERROR							Write '1' t	o Enab	le inte	errupt	tor El	RROF	l ever	nt							
									See EVEN	TS_ERR	OR												
			Set	1					Enable														
			Disabled	0					Read: Disa														
Н	D\A/	RXTO	Enabled	1					Read: Ena Write '1' t		lo inte	rrunt	for P	VTO	ovent								
	11.00	IXIO										irupt	101 10		cvciii								
			Cat	1					See EVEN Enable	IS_KXI	U												
			Set Disabled	1					Read: Disa	ahlad													
			Enabled	1					Read: Ena														
ı	RW	RXSTARTED		_					Write '1' t		le inte	errupt	for R	XSTA	RTED	eve	nt						
									See <i>EVEN</i>	TS RXS	TARTI	-D											
			Set	1					Enable		.,												
			Disabled	0					Read: Disa	abled													
			Enabled	1					Read: Ena	bled													
J	RW	TXSTARTED							Write '1' t	o Enab	le inte	errupt	for T	KSTA	RTED	evei	nt						
									See <i>EVEN</i>	TS_TXS	TART	D											
			Set	1					Enable														
			Disabled	0					Read: Disa	abled													
			Enabled	1					Read: Ena	bled													
L	RW	TXSTOPPED							Write '1' t	o Enab	le inte	errupt	for T	KSTO	PPED	eve	nt						
									See <i>EVEN</i>	TS_TXS	TOPP	ED											
			Set	1					Enable														
			Disabled	0					Read: Disa														
			Enabled	1					Read: Ena	bled													

35.10.4 INTENCLR

Address offset: 0x308

Disable interrupt



Bit r	number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L J I H G F E D C B A
Res	set 0x00000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW CTS			Write '1' to Disable interrupt for CTS event
				See EVENTS_CTS
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW NCTS			Write '1' to Disable interrupt for NCTS event
				See EVENTS_NCTS
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW RXDRDY			Write '1' to Disable interrupt for RXDRDY event
				See EVENTS_RXDRDY
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW ENDRX			Write '1' to Disable interrupt for ENDRX event
				Son EVENTS ENDRY
		Clear	1	See EVENTS_ENDRX Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW TXDRDY	Enablea	-	Write '1' to Disable interrupt for TXDRDY event
-				
				See EVENTS_TXDRDY
		Clear	1	Disable
		Disabled	0	Read: Disabled
F	RW ENDTX	Enabled	1	Read: Enabled Write '1' to Disable interrupt for ENDTX event
r	KW ENDIX			write 1 to disable interrupt for ENDTA event
				See EVENTS_ENDTX
		Clear	1	Disable
		Disabled	0	Read: Disabled
	DW FDDOD	Enabled	1	Read: Enabled
G	RW ERROR			Write '1' to Disable interrupt for ERROR event
				See EVENTS_ERROR
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW RXTO			Write '1' to Disable interrupt for RXTO event
				See EVENTS_RXTO
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
I	RW RXSTARTED			Write '1' to Disable interrupt for RXSTARTED event
				See EVENTS_RXSTARTED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW TXSTARTED			Write '1' to Disable interrupt for TXSTARTED event
				See EVENTS_TXSTARTED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW TXSTOPPED			Write '1' to Disable interrupt for TXSTOPPED event



Bit number		31 30 2	9 28 2	27 26	5 25	24 2	23 2	2 21	20	19 1	18 1	7 16	5 15	14 :	13 13	2 11 :	10 9	8	7	6	5	4 3	2	1	0
Id							L	-	J	1	-	4					G	F	Ε			D	С	В	Α
Reset 0x00000000		0 0 0	0	0 0	0	0	0 0	0 (0	0	0 (0 0	0	0	0 0	0	0 0	0	0	0	0	0 0	0	0	0
Id RW Field	Value Id	Value				ı	Desc	ripti	on																
						9	See L	EVEN	ITS_	TXS	TOP	PED													
C	Clear	1				[Disal	ble																	
С	Disabled	0				F	Read	l: Dis	able	ed															
E	Enabled	1				F	Read	l: Ena	able	d															

35.10.5 ERRORSRC

Address offset: 0x480

Error source

D.1				24	20	20	20.2	- -	<i>c</i> 2		4.0		22.	24 2		2 4	0 4-	7 4	. 45		4.0	4.3		40	_	0	7	_	_		· ·		1 0
	numbe	er		31	30	29	28 2	1 2	.6 2	5 2	4 2	.3 4	22 2	21 2	0 19	9 I	81.	/ T() 15	14	- 13	12	. 11	1 10	9	8	/	6	5			2 1	1 0
Id _																															D (ВА
		0000000	Value Id	0	_	0	0 (, (0 0	, (0) (0	0	0	0	U	0	0	0	U	U	U	0	0	0	0 () (0 0
ld		Field	value Id	Va	lue								scrip																				
Α	RW	OVERRUN									С)ve	erru	n er	ror																		
											Α	st	tart	bit	is re	cei	ved	wh	ile t	he	pre	vio	us c	data	sti	II lie	s in	RXI	D.				
											(1	Pre	evio	us c	lata	is I	ost.)															
			NotPresent	0							R	lea	ad: e	rro	r no	t pr	ese	nt															
			Present	1							R	lea	ad: e	rro	r pre	ese	nt																
В	RW	PARITY									Р	ari	ity e	erro	r																		
											Α	\ ch	hara	cte	r wit	th b	ad	par	ity i	s re	cei	ved	l, if	HW	pa	rity	che	ck i	S				
											е	na	able	d.																			
			NotPresent	0							R	lea	ad: e	rro	r no	t pı	ese	nt															
			Present	1							R	lea	ad: e	rro	r pre	ese	nt																
С	RW	FRAMING									F	rar	min	g er	ror	occ	urre	ed															
											Α	\ va	alid	sto	p bit	is	not	det	ect	ed o	on t	he:	ser	ial c	lata	inp	ut a	fte	r al	ı			
															arac																		
			NotPresent	0							R	lea	ad: e	rro	r no	t pr	ese	nt															
			Present	1							R	lea	ad: e	rro	r pre	ese	nt																
D	RW	BREAK									В	Brea	ak c	onc	litio	n																	
											_	·ho		ial	data	inr	+	ic 'C	' fo	r lo	200	r +h		th o	lon	ath	of.	- d-	+-				
															uata e da						-					-							
															e ua h pa				eng	LI I 13	, 10	י טונ	LS VI	VICIII	Jut	μαι	icy i	лс, с	ailu				
			NotPresent	0											r no			•															
			Present	1											r pre			111															
			TICSCIIC	1							11	ıca	u. c	0	, bic	.JC	110																

35.10.6 ENABLE

Address offset: 0x500

Enable UART

Bit	numb	er		31	30	29	28	27	26	5 2	5 2	24	23	22	21	20	19	9 1	8 1	17	16	15	14	13	12	2 1	1 1) 9	8	7	6	5	4	3	2	1 0
Id																																		Α	Α	ΑА
Res	et 0x(00000000		0	0	0	0	0	0	(0	0	0	0	0	0	0	()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Val	ue								De	scr	ipt	on																				
Α	RW	ENABLE											Ena	abl	e o	di.	sak	le	UA	RT	E															
			Disabled	0									Dis	ab	le l	IAR	TE																			
			Enabled	8									Ena	abl	e U	AR'	TE																			

35.10.7 PSEL.RTS

Address offset: 0x508

Pin select for RTS signal



Bit	numbe	er		3:	1 30	29	28	27	26	25	24	23 2	22 2	21 2	0 19	18	3 17	16	15	14 1	3 1	2 11	. 10	9	8	7	6	5 4	3	2	1	0
Id				В																								Þ	A	Α	Α	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1 1	l 1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1 1	. 1	1	1	1
Id	RW	Field	Value Id	V	alue							Des	crip	tior	1																	
Α	RW	PIN		[0)31]						Pin	nun	nbe	r																	
В	RW	CONNECT										Con	nec	tior	1																	
			Disconnected	1						Disc	conr	nect																				
			Connected	0								Con	nec	t																		

35.10.8 PSEL.TXD

Address offset: 0x50C Pin select for TXD signal

Bit r	numbe	er		31 30	29	28	27	26	25	24	23 2	22 2	1 20	0 19	18	17 1	.6 15	5 14	13 1	2 1:	l 10	9	8	7	6	5	4	3 2	1	0
Id				В																							A	4 A	Α	Α
Res	et OxF	FFFFFF		1 1	1	1	1	1	1	1	1	1 :	1 1	. 1	1	1	1 1	1	1 :	l 1	1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value	:						Des	crip	tion	1																
Α	RW	PIN		[031	.]						Pin	nun	ber																	
В	RW	CONNECT									Con	nec	tion																	
			Disconnected	1							Disc	conn	ect																	
			Connected	0							Con	nec	t																	

35.10.9 PSEL.CTS

Address offset: 0x510

Pin select for CTS signal

Bit	numbe	er		31 30 29 28 27 26 25 2	$24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id				В	A A A A
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.10.10 PSEL.RXD

Address offset: 0x514

Pin select for RXD signal

Bit	numbe	er		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Re	set 0xF	FFFFFF		1 1 1 1 1 1 1 :	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

35.10.11 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.



Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		AAAAAAAA	A A A A A A A A A A A A A A A A A A A
Reset 0x04000000		0 0 0 0 0 1 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
ld RW Field	Value Id	Value	Description
A RW BAUDRATE			Baud rate
	Baud1200	0x0004F000	1200 baud (actual rate: 1205)
	Baud2400	0x0009D000	2400 baud (actual rate: 2396)
	Baud4800	0x0013B000	4800 baud (actual rate: 4808)
	Baud9600	0x00275000	9600 baud (actual rate: 9598)
	Baud14400	0x003AF000	14400 baud (actual rate: 14401)
	Baud19200	0x004EA000	19200 baud (actual rate: 19208)
	Baud28800	0x0075C000	28800 baud (actual rate: 28777)
	Baud38400	0x009D0000	38400 baud (actual rate: 38369)
	Baud57600	0x00EB0000	57600 baud (actual rate: 57554)
	Baud76800	0x013A9000	76800 baud (actual rate: 76923)
	Baud115200	0x01D60000	115200 baud (actual rate: 115108)
	Baud230400	0x03B00000	230400 baud (actual rate: 231884)
	Baud250000	0x04000000	250000 baud
	Baud460800	0x07400000	460800 baud (actual rate: 457143)
	Baud921600	0x0F000000	921600 baud (actual rate: 941176)
	Baud1M	0x10000000	1Mega baud

35.10.12 RXD.PTR

Address offset: 0x534

Data pointer

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer

35.10.13 RXD.MAXCNT

Address offset: 0x538

Maximum number of bytes in receive buffer

Bit r	umb	er		31 30	29 2	28 27	7 26	25	24 2	3 22	2 21	20	19 1	.8 1	7 16	15	14 :	L3 1	2 11	. 10	9	8	7	6	5 4	1 3	2	1	0
Id																							Α	A	4 Α	A A	Α	Α	Α
Res	et OxC	0000000		0 0	0	0 0	0	0	0	0 0	0	0	0	0 (0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Value)esc	ripti	on																	
Α	RW	MAXCNT							N	Лахі	mun	n nu	ımbe	er of	f byt	es ir	ı rec	eive	buf	fer									7

35.10.14 RXD.AMOUNT

Address offset: 0x53C

Number of bytes transferred in the last transaction

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10 9 8	3 7 6 5 4 3	2 1 0
Id					A A A A A	A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	000000000	00000	0 0 0
Id RW Field	Value Id	Value	Description			
A R AMOUNT			Number of bytes tran	nsferred in the last transaction		

35.10.15 TXD.PTR

Address offset: 0x544

Data pointer



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Data pointer

35.10.16 TXD.MAXCNT

Address offset: 0x548

Maximum number of bytes in transmit buffer

Bit	numb	er		31 3	30 29	9 28	8 27	26	25	24	23	22	21	20	19	18	17	16	15 :	14	13	12 :	11	10	9	8	7	6	5	4	3 2	! 1	1 0
Id																											Α	Α	Α.	Α	A A		A A
Re	et 0x	00000000		0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Valu	ıe						Des	cri	ptic	n																			
Δ	R\M	MAXCNT									Mα	vim	um	nu	mh	or 1	of h	νtο	c in	tra	ncr	nit l	nuf	for									

35.10.17 TXD.AMOUNT

Address offset: 0x54C

Number of bytes transferred in the last transaction

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A R AMOUNT			Number of bytes transferred in the last transaction

35.10.18 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit	numbe	er		31	30 2	29 :	28 2	27 2	26 2	25 2	24 2	23 2	2 2	1 20	0 19	9 18	3 1	7 16	5 15	14	13	12	11 1	.0 9	8 (7	6	5	4	3	2 :	1 0
Id																														В	ВЕ	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Va	lue							Desc	ript	tion	ı																	
Α	RW	HWFC									H	Harc	lwa	re f	low	coı	ntro	ol														
			Disabled	0								Disa	bled	t																		
			Enabled	1							E	nat	oled																			
В	RW	PARITY									F	Parit	y																			
			Excluded	0x0	0						E	Excl	ude	par	ity	bit																
			Included	0x	7						- 1	nclu	ıde	pari	ity Ł	bit																

35.11 Electrical specification

35.11.1 UARTE electrical specification

Symbol	Description	Min.	Тур.	Max.	Units
f _{UARTE}	Baud rate for UARTE ³² .		. , , , .	1000	kbps
I _{UARTE1M}	Run current at max baud rate.		55		μΑ
I _{UARTE115k}	Run current at 115200 bps.		55		μΑ
I _{UARTE1k2}	Run current at 1200 bps.		55		μΑ
I _{UARTE,IDLE}	Idle current for UARTE (STARTed, no XXX activity)		1		μΑ
t _{UARTE,CTSH}	CTS high time	1			μs

Higher baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{UARTE,START,LP}	Time from STARTRX/STARTTX task to transmission started, low		t _{UARTE,ST}	AR	μs
	power mode		+		
			t _{START_HF}	IN	
t _{UARTE,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1		μs
	constant latency mode				



36 QDEC — Quadrature decoder

The Quadrature decoder (QDEC) provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors.

The sample period and accumulation are configurable to match application requirements. The QDEC provides the following:

- Decoding of digital waveform from off-chip quadrature encoder.
- · Sample accumulation eliminating hard real-time requirements to be enforced on application.
- Optional input de-bounce filters.
- Optional LED output signal for optical encoders.

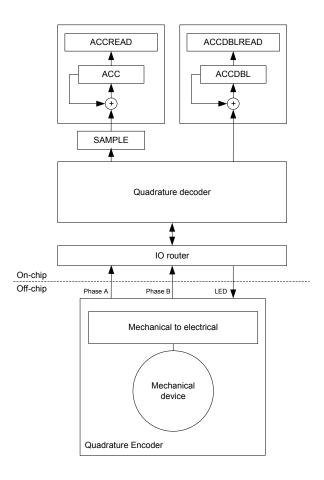


Figure 97: Quadrature decoder configuration

36.1 Sampling and decoding

The QDEC decodes the output from an incremental motion encoder by sampling the QDEC phase input pins (A and B).

The off-chip quadrature encoder is an incremental motion encoder outputting two waveforms, phase A and phase B. The two output waveforms are always 90 degrees out of phase, meaning that one always changes level before the other. The direction of movement is indicated by which of these two waveforms that changes level first. Invalid transitions may occur, that is when the two waveforms switch simultaneously. This may occur if the wheel rotates too fast relative to the sample rate set for the decoder.



The QDEC decodes the output from the off-chip encoder by sampling the QDEC phase input pins (A and B) at a fixed rate as specified in the SAMPLEPER register.

If the SAMPLEPER value needs to be changed, the QDEC shall be stopped using the STOP task. SAMPLEPER can be then changed upon receiving the STOPPED event, and QDEC can be restarted using the START task. Failing to do so may result in unpredictable behaviour.

It is good practice to change other registers (LEDPOL, REPORTPER, DBFEN and LEDPRE) only when the QDEC is stopped.

When started, the decoder continuously samples the two input waveforms and decodes these by comparing the current sample pair (n) with the previous sample pair (n-1).

The decoding of the sample pairs is described in the table below.

Table 84: Sampled value encoding

Previous sample - 1)	e pair(n	·	les pair(n)	SAMPLE register	ACC operation	ACCDBL operation	Description
Α	В	Α	В				
0	0	0	0	0	No change	No change	No movement
0	0	0	1	1	Increment	No change	Movement in positive direction
0	0	1	0	-1	Decrement	No change	Movement in negative direction
0	0	1	1	2	No change	Increment	Error: Double transition
0	1	0	0	-1	Decrement	No change	Movement in negative direction
0	1	0	1	0	No change	No change	No movement
0	1	1	0	2	No change	Increment	Error: Double transition
0	1	1	1	1	Increment	No change	Movement in positive direction
1	0	0	0	1	Increment	No change	Movement in positive direction
1	0	0	1	2	No change	Increment	Error: Double transition
1	0	1	0	0	No change	No change	No movement
1	0	1	1	-1	Decrement	No change	Movement in negative direction
1	1	0	0	2	No change	Increment	Error: Double transition
1	1	0	1	-1	Decrement	No change	Movement in negative direction
1	1	1	0	1	Increment	No change	Movement in positive direction
1	1	1	1	0	No change	No change	No movement

36.2 LED output

The LED output follows the sample period, and the LED is switched on a given period before sampling and switched off immediately after the inputs are sampled. The period the LED is switched on before sampling is given in the LEDPRE register.

The LED output pin polarity is specified in the LEDPOL register.

For using off-chip mechanical encoders not requiring a LED, the LED output can be disabled by writing value 'Disconnected' to the CONNECT field of the PSEL.LED register. In this case the QDEC will not acquire access to a LED output pin and the pin can be used for other purposes by the CPU.

36.3 Debounce filters

Each of the two-phase inputs have digital debounce filters.

When enabled through the DBFEN register, the filter inputs are sampled at a fixed 1 MHz frequency during the entire sample period (which is specified in the SAMPLEPER register), and the filters require all of the samples within this sample period to equal before the input signal is accepted and transferred to the output of the filter.

As a result, only input signal with a steady state longer than twice the period specified in SAMPLEPER are guaranteed to pass through the filter, and any signal with a steady state shorter than SAMPLEPER will always be suppressed by the filter. (This is assumed that the frequency during the debounce period never exceeds 500 kHz (as required by the Nyquist theorem when using a 1 MHz sample frequency).

The LED will always be ON when the debounce filters are enabled, as the inputs in this case will be sampled continuously.



Note that when when the debounce filters are enabled, displacements reported by the QDEC peripheral are delayed by one SAMPLEPER period.

36.4 Accumulators

The quadrature decoder contains two accumulator registers, ACC and ACCDBL, that accumulate respectively valid motion sample values and the number of detected invalid samples (double transitions).

The ACC register will accumulate all valid values (1/-1) written to the SAMPLE register. This can be useful for preventing hard real-time requirements from being enforced on the application. When using the ACC register the application does not need to read every single sample from the SAMPLE register, but can instead fetch the ACC register whenever it fits the application. The ACC register will always hold the relative movement of the external mechanical device since the previous clearing of the ACC register. Sample values indicating a double transition (2) will not be accumulated in the ACC register.

An ACCOF event will be generated if the ACC receives a SAMPLE value that would cause the register to overflow or underflow. Any SAMPLE value that would cause an ACC overflow or underflow will be discarded, but any samples not causing the ACC to overflow or underflow will still be accepted.

The accumulator ACCDBL accumulates the number of detected double transitions since the previous clearing of the ACCDBL register.

The ACC and ACCDBL registers can be cleared by the READCLRACC and subsequently read using the ACCREAD and ACCDBLREAD registers.

The ACC register can be separately cleared by the RDCLRACC and subsequently read using the ACCREAD registers.

The ACCDBL register can be separately cleared by the RDCLRDBL and subsequently read using the ACCDBLREAD registers.

The REPORTPER register allows automating the capture of several samples before it can send out a REPORTRDY event in case a non-null displacement has been captured and accumulated, and a DBLRDY event in case one or more double-displacements have been captured and accumulated. The REPORTPER field in this register selects after how many samples the accumulators contents are evaluated to send (or not) REPORTRDY and DBLRDY events.

Using the RDCLRACC task (manually sent upon receiving the event, or using the DBLRDY_RDCLRACC shortcut), ACCREAD can then be read.

In case at least one double transition has been captured and accumulated, a DBLRDY event is sent. Using the RDCLRDBL task (manually sent upon receiving the event, or using the DBLRDY_RDCLRDBL shortcut), ACCDBLREAD can then be read.

36.5 Output/input pins

The QDEC uses a three-pin interface to the off-chip quadrature encoder.

These pins will be acquired when the QDEC is enabled in the ENABLE register. The pins acquired by the QDEC cannot be written by the CPU, but they can still be read by the CPU.

The pin numbers to be used for the QDEC are selected using the PSEL.n registers.

36.6 Pin configuration

The Phase A, Phase B, and LED signals are mapped to physical pins according to the configuration specified in the PSEL.A, PSEL.B, and PSEL.LED registers respectively.

If the CONNECT field value 'Disconnected' is specified in any of these registers, the associated signal will not be connected to any physical pin. The PSEL.A, PSEL.B, and PSEL.LED registers and their configurations are only used as long as the QDEC is enabled, and retained only as long as the device is in



ON mode. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To secure correct behavior in the QDEC, the pins used by the QDEC must be configured in the GPIO peripheral as described in *Table 85: GPIO configuration before enabling peripheral* on page 350 before enabling the QDEC. This configuration must be retained in the GPIO for the selected IOs as long as the QDEC is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 85: GPIO configuration before enabling peripheral

QDEC signal	QDEC pin	Direction	Output value	Comment	
Phase A	As specified in PSEL.A	Input	Not applicable		
Phase B	As specified in PSEL.B	Input	Not applicable		
LED	As specified in PSEL.LED	Input	Not applicable		

36.7 Registers

Table 86: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40012000	QDEC	QDEC	Quadrature decoder	

Table 87: Register Overview

Register	Offset	Description
TASKS_START	0x000	Task starting the quadrature decoder
TASKS_STOP	0x004	Task stopping the quadrature decoder
TASKS_READCLRACC	0x008	Read and clear ACC and ACCDBL
TASKS_RDCLRACC	0x00C	Read and clear ACC
TASKS_RDCLRDBL	0x010	Read and clear ACCDBL
EVENTS_SAMPLERDY	0x100	Event being generated for every new sample value written to the SAMPLE register
EVENTS_REPORTRDY	0x104	Non-null report ready
EVENTS_ACCOF	0x108	ACC or ACCDBL register overflow
EVENTS_DBLRDY	0x10C	Double displacement(s) detected
EVENTS_STOPPED	0x110	QDEC has been stopped
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable the quadrature decoder
LEDPOL	0x504	LED output pin polarity
SAMPLEPER	0x508	Sample period
SAMPLE	0x50C	Motion sample value
REPORTPER	0x510	Number of samples to be taken before REPORTRDY and DBLRDY events can be generated
ACC	0x514	Register accumulating the valid transitions
ACCREAD	0x518	Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task
PSEL.LED	0x51C	Pin select for LED signal
PSEL.A	0x520	Pin select for A signal
PSEL.B	0x524	Pin select for B signal
DBFEN	0x528	Enable input debounce filters
LEDPRE	0x540	Time period the LED is switched ON prior to sampling
ACCDBL	0x544	Register accumulating the number of detected double transitions
ACCDBLREAD	0x548	Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

36.7.1 SHORTS

Address offset: 0x200 Shortcut register



Bit	number	•		31 30	29 28	3 27 20	5 25 2	4 23 22	22 21	20 19	18 1	7 16	15	14 13	3 12	11 1	0 9	8	7	6 5	5 4	1 3	2	1	0
Id																				G F	= E	E D	С	В	Α
Res	et 0x00	0000000		0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0	0	0 0	0	0 () 0	0	0	0 () () 0	0	0	0
Id	RW	Field	Value Id	Value				Desc	criptic	on															
Α	RW	REPORTRDY_READCLRACG						Short	rtcut k	betwe	en RE	POR	TRD	eve	ent a	nd RF	EADO	CLRA	.CC 1	task					
								See E	EVEN	TS_RE	PORT	RDY	and	TASI	KS_R	EADO	CLRA	СС							
			Disabled	0				Disab	ble sh	nortcu	t														
			Enabled	1				Enab	ble sh	ortcut															
В	RW	SAMPLERDY_STOP						Short	rtcut k	betwe	en SA	MPL	.ERD	Y eve	ent a	nd S7	ГОР	task							
								See E	EVEN	TS_SA	MPLE	RDY	and	TAS	KS_S	TOP									
			Disabled	0				Disab	ble sh	nortcu	t														
			Enabled	1				Enab	ble sh	ortcut															
С	RW	REPORTRDY_RDCLRACC						Short	rtcut k	betwe	en RE	POR	TRD	eve	ent a	nd RI	CLF	RACC	tas	k					
								See E	EVEN	TS_RE	PORT	RDY	and	TASI	KS_R	DCLR	ACC	:							
			Disabled	0				Disab	ble sh	nortcu	t														
			Enabled	1				Enab	ble sh	ortcut															
D	RW	REPORTRDY_STOP						Short	rtcut b	betwe	en RE	POR	TRD	eve	nt a	nd ST	OP 1	task							
								See E	EVEN	TS_RE	PORT	RDY	and	TASI	<s_s< td=""><td>ТОР</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></s_s<>	ТОР									
			Disabled	0				Disab	ble sh	nortcu	t														
			Enabled	1				Enab	ble sh	ortcut															
Ε	RW	DBLRDY_RDCLRDBL						Short	rtcut k	betwe	en DB	BLRD	Y ev	ent a	nd R	DCLF	≀DBL	. task	(
								See E	EVEN	TS_DE	LRDY	and	TAS	KS_R	≀DCL	RDBL									
			Disabled	0				Disab	ble sh	nortcu	t														
			Enabled	1				Enab	ble sh	ortcut															
F	RW	DBLRDY_STOP						Short	rtcut b	betwe	en DB	BLRD	Y ev	ent a	nd S	TOP 1	task								
								See E	EVEN	TS_DE	LRDY	and	TAS	KS_S	TOP										
			Disabled	0				Disab	ble sh	nortcu	t														
			Enabled	1				Enab	ble sh	ortcut															
G	RW	SAMPLERDY_READCLRAC	C					Short	rtcut k	betwe	en SA	MPL	.ERD	Y eve	ent a	nd RI	EAD	CLRA	CC	task					
								See E	EVEN	TS_SA	MPLE	RDY	and	TAS	KS_R	EAD	CLRA	ICC							
			Disabled	0				Disab	ble sh	nortcu	t														
			Enabled	1				Enab	ble sh	ortcut															

36.7.2 INTENSET

Address offset: 0x304 Enable interrupt

Bit r	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				E D C B A
Res	et 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW SAMPLERDY			Write '1' to Enable interrupt for SAMPLERDY event
				See EVENTS_SAMPLERDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REPORTRDY			Write '1' to Enable interrupt for REPORTRDY event
				See EVENTS_REPORTRDY
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW ACCOF			Write '1' to Enable interrupt for ACCOF event
				See EVENTS_ACCOF
		Set	1	Enable



Bit number			31 30	29 2	8 27	26 25	24 2	23 22	21 20	0 19	18 1	17 16	15 1	14 13	3 12	11 10	9	8 7	6	5 4	1 3	2	1 0
Id																				- 1	D	С	В А
Reset 0x0000	0000		0 0	0 (0 0	0 0	0	0 0	0 0	0	0 (0 0	0	0 0	0	0 0	0	0 0	0	0 (0	0	0 0
Id RW Fie	eld V	/alue Id	Value					Descri	iption	1													
	С	Disabled	0				F	Read:	Disab	led													
	E	Enabled	1				F	Read:	Enabl	led													
D RW DB	LRDY						١	Write	'1' to	Enab	le in	nterru	upt fo	or DE	BLRD	Y eve	nt						
							5	See E	VENTS	_DBL	LRDY	Y											
	S	Set	1				E	Enable	е														
	С	Disabled	0				F	Read:	Disab	led													
	E	Enabled	1				F	Read:	Enabl	led													
E RW ST	OPPED						١	Write	'1' to	Enab	le ir	nterru	upt fo	or ST	OPPI	ED ev	ent						
							5	See E	VENTS	S_STC	OPPE	D											
	S	Set	1				E	Enable	е														
	D	Disabled	0				F	Read:	Disab	led													
	E	Enabled	1				F	Read:	Enabl	led													

36.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numb	er		31	30 2	9 28	3 27	26	25	24 2	23	22 21	1 20) 19	9 18	17	16	15	14	13	12 :	11 1	0 9	8	7	6	5	4	3 2	2 1	0
Id																												Е	D (В	Α
Res	et 0x	00000000		0	0 (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Val	ıe					ı	Des	script	ion																		
Α	RW	SAMPLERDY								١	Wri	ite '1'	' to	Dis	able	int	errı	upt	for	SAN	ИPL	ERD	Y ev	ent							
										9	See	e EVEI	NTS	_S/	AMF	PLER	DΥ														
			Clear	1						ı	Disa	able																			
			Disabled	0						ı	Rea	ad: Dis	sab	led																	
			Enabled	1						ı	Rea	ad: En	nabl	ed																	
В	RW	REPORTRDY								١	Wri	ite '1'	' to	Disa	able	int	errı	upt	for	REF	OR	TRD	Y ev	ent							
										9	See	e EVEI	NTS	RE	EPO	RTR	DY														
			Clear	1						ı	Disa	able																			
			Disabled	0						ı	Rea	ad: Dis	sab	led																	
			Enabled	1						ı	Rea	ad: En	nabl	ed																	
С	RW	ACCOF								١	Wri	ite '1'	' to	Disa	able	int	errı	upt	for	AC	COF	eve	nt								
										9	See	e EVEI	NTS	_A	ссо	F															
			Clear	1						ı	Disa	able																			
			Disabled	0						1	Rea	ad: Dis	sab	led																	
			Enabled	1						1	Rea	ad: En	nabl	ed																	
D	RW	DBLRDY								١	Wri	ite '1'	' to	Disa	able	int	errı	upt	for	DBI	_RD	Y ev	ent								
										9	See	e EVEI	NTS	_DI	BLR	DY															
			Clear	1						ı	Disa	able																			
			Disabled	0						ı	Rea	ad: Dis	sab	led																	
			Enabled	1						ı	Rea	ad: En	nabl	ed																	
Ε	RW	STOPPED								١	Wri	ite '1'	'to	Disa	able	int	errı	upt	for	STC	PPI	D e	ven	t							
										9	See	e EVEI	NTS	_57	ГОР	PED															
			Clear	1						I	Disa	able																			
			Disabled	0						ı	Rea	ad: Dis	sab	led																	
			Enabled	1						ı	Rea	ad: En	nabl	ed																	

36.7.4 ENABLE

Address offset: 0x500

Enable the quadrature decoder



Bit	numl	er		31	30	29	28	27	26	25	24 :	23 2	22 :	21 2	0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																																			Α
Re	set 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	/ Field	Value Id	Va	lue						ı	Des	crip	ptio	n																				
Α	RW	ENABLE									ı	Enal	ble	or o	lisa	ble	th	e q	uac	dra	ure	e de	eco	der											
											,	Whe	en (enal	ole	d th	ie (dec	ode	er p	ins	wi	ll be	e ac	tive	e. W	/he	n d	isat	oled	ł				
											1	the	qua	adra	itui	re d	ec	ode	r p	ins	are	nc	ot a	ctiv	e a	nd o	an	be	use	ed a	IS				
											(GPI	Ο.																						
			Disabled	0							ı	Disa	able	9																					
			Enabled	1							١	Enal	ble																						

36.7.5 LEDPOL

Address offset: 0x504 LED output pin polarity

Bit	numb	er		31 30	29	28 2	27 2	26 2	5 24	1 23	3 22	21	20 :	19 1	8 1	7 1	6 15	5 14	13	12	11 1	0 9	8	7	6	5	4	3	2 :	1 0
Id																														Α
Res	et Ox	0000000		0 0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value						D	escri	ptic	n																	
Α	RW	LEDPOL								LE	Ο οι	ıtpı	ıt pi	n po	olari	ity														
			ActiveLow	0						Le	d ac	tive	on	out	put	pin	low	,												
			ActiveHigh	1						Le	ed ac	tive	on	out	put	pin	hig	h												

36.7.6 SAMPLEPER

Address offset: 0x508

Sample period

Bit r	numbe	er		31	30 2	9 2	28 2	7 2	6 25	24	4 23	22	21 20	19	18	17	16	15	14 1	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																													Α Δ	A	Α
Res	et 0x0	0000000		0	0 () (0 0) (0 0	0	0 (0	0 0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0
ld	RW	Field	Value Id	Va	lue						Des	scrip	otion																		
Α	RW	SAMPLEPER									Sar	nple	e peri	od.	The	SA	MΡ	LE r	egis	ter	will	be ι	ıpda	itec	l fo	r ev	ery				
											nev	w sa	mple																		
			128us	0							128	B us																			
			256us	1							256	6 us																			
			512us	2							512	2 us																			
			1024us	3							102	24 u	S																		
			2048us	4							204	48 u	S																		
			4096us	5							409	96 u	S																		
			8192us	6							819	92 u	S																		
			16384us	7							163	384	us																		
			32ms	8							327	768	us																		
			65ms	9							655	536	us																		
			131ms	10							131	1072	2 us																		

36.7.7 SAMPLE

Address offset: 0x50C Motion sample value

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A R SAMPLE		[-12] Last motion sample



Id RW Field Va	alue Id Vali					_	cript																
Reset 0x00000000	0	0 0 0	0 0	0	0 0	0	0 0	0	0	0 0	0	0	0 0	0	0	0 0	0	0	0	0	0 0	0	0 0
Id	А	A A A	А А	Α .	А А	Α	A A	Α	Α ,	4 A	Α	Α	А А	Α	A	A A	A A	Α	Α	Α ,	4 A	Α	A A
Bit number	31 :	30 29 2	28 27	26 2	25 24	23	22 21	20	19 1	.8 17	16	15 1	14 13	12	11 1	10 9	8	7	6	5 4	4 3	2	1 0

The value is a 2's complement value, and the sign gives the direction of the motion. The value '2' indicates a double transition.

36.7.8 REPORTPER

Address offset: 0x510

Number of samples to be taken before REPORTRDY and DBLRDY events can be generated

Bit number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Reset 0x00000000		0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
A RW REPORTPER			Specifies the number of samples to be accumulated in the ACC
			register before the REPORTRDY and DBLRDY events can be
			generated
			The report period in [us] is given as: RPUS = SP * RP Where
			RPUS is the report period in [us/report], SP is the sample period
			in [us/sample] specified in SAMPLEPER, and RP is the report
			period in [samples/report] specified in REPORTPER .
	10Smpl	0	10 samples / report
	40Smpl	1	40 samples / report
	80Smpl	2	80 samples / report
	120Smpl	3	120 samples / report
	160Smpl	4	160 samples / report
	200Smpl	5	200 samples / report
	240Smpl	6	240 samples / report
	280Smpl	7	280 samples / report
	1Smpl	8	1 sample / report

36.7.9 ACC

Address offset: 0x514

Register accumulating the valid transitions

Bit number	31 30 29 28	3 27 26 25 24	23 22 21 20 1	9 18 17	16 15 :	14 13 1	2 11 1	9	8	7 6	5	4	3 2	1	0
Id	АААА	. A A A A	A A A A	A A A	А А	AAA	A A A	A	Α .	A A	Α	Α /	A A	Α	Α
Reset 0x00000000	0 0 0 0	0 0 0 0	0 0 0 0 0	0 0	0 0	0 0 (0 0	0	0	0 0	0	0 (0 0	0	0
ld RW Field Va	alue Id Value		Description												
A R ACC	[-10241023	3]	Register accum	nulating	all valid	l sampl	es (not	dou	ble t	ansi	tion)			_
			read from the	SAMPLE	registe	r									
			Double transit	ions (SA	MDIF -	- 2 \ wil	not he	arr	ıımıı	later	lin				
			Double transit	10113 (3A	VIFEL -	- 2) WII	יוטנ טפ	acc	uiiiu	atet					
			this register. T	he value	is a 32	bit 2's	comple	men	t val	ue. I	a				
			sample that we	ould cau	se this	register	to ove	rflov	v or	unde	rflo	w			
			is received, the	e sample	will be	ignore	d and a	n ov	erflo	w ev	ent				
			(ACCOF) will b	oe gener	ated. T	he ACC	registe	r is o	lear	ed by	,				

36.7.10 ACCREAD

Address offset: 0x518

Snapshot of the ACC register, updated by the READCLRACC or RDCLRACC task



Re	 	0000000	V.I		0	0	0	0				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	 lue	N23					scri	ptic																				

The ACCREAD register is updated when the READCLRACC or RDCLRACC task is triggered

36.7.11 PSEL.LED

Address offset: 0x51C Pin select for LED signal

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

36.7.12 PSEL.A

Address offset: 0x520 Pin select for A signal

Bit	numbe	er		31 30	29	28	27	26	25	24	23 2	2 2	1 20	19	18	17 1	6 15	5 14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id				В																							A	A A	. A	Α
Res	et 0xF	FFFFFF		1 1	1	1	1	1	1	1	1 :	1 1	l 1	1	1	1 :	1 1	1	1 :	l 1	. 1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value	•						Desc	crip	tion																	
Α	RW	PIN		[031	L]						Pin r	num	ber																	
В	RW	CONNECT									Coni	nect	tion																	
			Disconnected	1							Disc	onn	ect																	
			Connected	0							Coni	nect	t																	

36.7.13 PSEL.B

Address offset: 0x524 Pin select for B signal

Bit r	iumbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

36.7.14 DBFEN

Address offset: 0x528

Enable input debounce filters



Bit	num	nber			31 30	29	28	27	26	25	24	23	22 2	21 2	0 1	9 1	8 17	16	15	14	13	12	11 :	10	9 1	3	7 6	5 5	5 4	3	2	1 0
Id																																Α
Res	et 0)x00	000000		0 0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0 0
Id	R۱	w	Field	Value Id	Value	•						Des	crip	otio	n																	
Α	R۱	W	DBFEN	DBFEN								Ena	ble	inp	ut d	ebo	unc	e fi	lter	S												
				Disabled	O Debounce input filters disabled																											
				Enabled	1			Debounce input filters enabled																								

36.7.15 LEDPRE

Address offset: 0x540

Time period the LED is switched ON prior to sampling

Bit r	numbe	er		31	30 2	9 2	8 27	7 26	25	24	23	22 2	1 2	0 19	18	17	16	15	14 :	l3 1	2 11	. 10	9	8	7	6	5	4	3	2 1	. 0
Id																								Α	Α	Α	Α	Α	A	4 A	A
Res	et OxO	0000010		0	0 0) (0 0	0	0	0	0	0 () (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	1	0 (0 0	0
Id	RW	Field	Value Id	Val	ue						Des	crip	tior	1																	
Α	RW	LEDPRE		[1511] Period in us the LED is switched on prior to sampling																											

36.7.16 ACCDBL

Address offset: 0x544

Register accumulating the number of detected double transitions

Bit nu	umbe	r		31	. 30 :	29	28 2	27 :	26 2	25 2	24 2	23 22	2 21	20	19	18 :	17 1	16 1	.5 1	.4 13	3 12	11	10 !	9	8 7	΄ 6	5	4	Ŭ	2 A	1 A	0 A
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 (· c	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							Desc	riptio	on																		
A	R	ACCDBL		[0.	15]						t V a c il	rans Whenccun overf Ilega	ter a ition n this nula low I tran ned.	s re tior eve nsit This	SAN gisten of nt (ions	APL dou ACC	E = nas r uble COF e de	2). eac /ill) w	hed lega vill b	d its al tra be ge afte	max ansit ener	imu ions ateo e ma	m va will I if a axim	alu I sto ny num	e the	e an ble ue	or was					

36.7.17 ACCDBLREAD

Address offset: 0x548

Snapshot of the ACCDBL, updated by the READCLRACC or RDCLRDBL task

Bit	numb	er		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					АААА
Res	et 0x0	0000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	D\A/	er 1.1	Value Id	Value	Description
iu	IVVV	Field	value id	value	Description
A	R	ACCDBLREAD	value id	[015]	Snapshot of the ACCDBL register. This field is updated when the

36.8 Electrical specification

36.8.1 QDEC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{QDEC}	Run current		5		μΑ
t _{SAMPLE}	Time between sampling signals from quadrature decoder	128		131072	μs
t_{LFD}	Time from LED is turned on to signals are sampled	0		511	μs



37 SAADC — Successive approximation analog-todigital converter

The ADC is a differential successive approximation register (SAR) analog-to-digital converter.

Listed here are the main features of SAADC:

- 8/10/12-bit resolution, 14-bit resolution with oversampling
- Up to eight input channels
 - One channel per single-ended input and two channels per differential input
 - Scan mode can be configured with both single-ended channels and differential channels.
- Full scale input range (0 to VDD)
- Sampling triggered via a task from software or a PPI channel for full flexibility on sample frequency source from low power 32.768kHz RTC or more accurate 1/16MHz Timers
- One-shot conversion mode to sample a single channel
- Scan mode to sample a series of channels in sequence. Sample delay between channels is t_{ack} + t_{conv} which may vary between channels according to user configuration of t_{ack}.
- Support for direct sample transfer to RAM using EasyDMA
- · Interrupts on single sample and full buffer events
- Samples stored as 16-bit 2's complement values for differential and single-ended sampling
- Continuous sampling without the need of an external timer
- Internal resistor string
- · Limit checking on the fly

37.1 Shared resources

The ADC can coexist with COMP and other peripherals using one of AIN0-AIN7, provided these are assigned to different pins.

It is not recommended to select the same analog input pin for both modules.

37.2 Overview

The ADC supports up to eight external analog input channels, depending on package variant. It can be operated in a one-shot mode with sampling under software control, or a continuous conversion mode with a programmable sampling rate.

The analog inputs can be configured as eight single-ended inputs, four differential inputs or a combination of these. Each channel can be configured to select AIN0 to AIN7 pins, or the VDD pin. Channels can be sampled individually in one-shot or continuous sampling modes, or, using scan mode, multiple channels can be sampled in sequence. Channels can also be oversampled to improve noise performance.



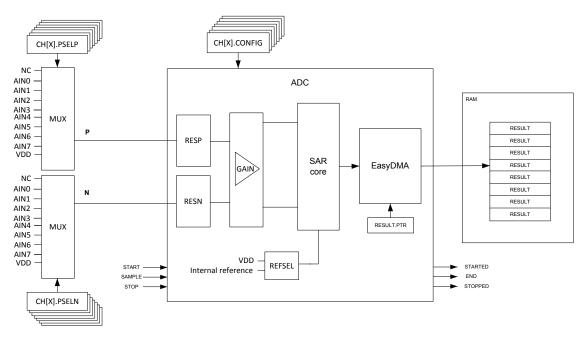


Figure 98: Simplified ADC block diagram

Internally, the ADC is always a differential analog-to-digital converter, but by default it is configured with single-ended input in the MODE field of the CH[n].CONFIG register. In single-ended mode, the negative input will be shorted to ground internally.

The assumption in single-ended mode is that the internal ground of the ADC is the same as the external ground that the measured voltage is referred to. The ADC is thus sensitive to ground bounce on the PCB in single-ended mode. If this is a concern we recommend using differential measurement.

37.3 Digital output

The output result of the ADC depends on the settings in the CH[n].CONFIG and RESOLUTION registers as follows:

```
RESULT = [V(P) - V(N)] * GAIN/REFERENCE * 2 (RESOLUTION - m)
```

where

V(P)

is the voltage at input P

V(N)

is the voltage at input N

GAIN

is the selected gain setting

REFERENCE

is the selected reference voltage

and m=0 if CONFIG.MODE=SE, or m=1 if CONFIG.MODE=Diff.

The result generated by the ADC will deviate from the expected due DC errors like offset, gain, differential non-linearity (DNL), and integral non-linearity (INL). See *Electrical specification* for details on these parameters. The result can also vary due to AC errors like non-linearities in the GAIN block, settling errors due to high source impedance and sampling jitter. For battery measurement the DC errors are most noticeable.



The ADC has a wide selection of gains controlled in the GAIN field of the CH[n].CONFIG register. If CH[n].CONFIG.REFSEL=0, the input range of the ADC core is nominally ± 0.6 V differential and the input must be scaled accordingly.

The ADC has a temperature dependent offset. If the ADC is to operate over a large temperature range, we recommend running CALIBRATEOFFSET at regular intervals, a CALIBRATEDONE event will be fired when the calibration is complete

37.4 Analog inputs and channels

Up to eight analog input channels, CH[n](n=0..7), can be configured.

See Shared resources on page 357 for shared input with comparators.

Any one of the available channels can be enabled for the ADC to operate in one-shot mode. If more than one CH[n] is configured, the ADC enters scan mode.

An analog input is selected as a positive converter input if CH[n].PSELP is set, setting CH[n].PSELP also enables the particular channel.

An analog input is selected as a negative converter input if CH[n].PSELN is set. The CH[n].PSELN register will have no effect unless differential mode is enabled, see MODE field in CH[n].CONFIG register.

If more than one of the CH[n].PSELP registers is set, the device enters scan mode. Input selections in scan mode are controlled by the CH[n].PSELP and CH[n].PSELN registers, where CH[n].PSELN is only used if the particular scan channel is specified as differential, see MODE field in CH[n].CONFIG register.

Important: Channels selected for COMP cannot be used at the same time for ADC sampling, though channels not selected for use by these blocks can be used by the ADC.

Table 88: Legal connectivity CH[n] vs. analog input

Channel input	Source	Connectivity
CH[n].PSELP	AINOAIN7	Yes(any)
CH[n].PSELP	VDD	Yes
CH[n].PSELN	AINOAIN7	Yes(any)
CH[n].PSELN	VDD	Yes

37.5 Operation modes

The ADC input configuration supports one-shot mode, continuous mode and scan mode.

Scan mode and oversampling cannot be combined.

37.5.1 One-shot mode

One-shot operation is configured by enabling only one of the available channels defined by CH[n].PSELP, CH[n].PSELN, and CH[n].CONFIG registers.

Upon a SAMPLE task, the ADC starts to sample the input voltage. The CH[n].CONFIG.TACQ controls the acquisition time.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA. For more information, see *EasyDMA* on page 361.

37.5.2 Continuous mode

Continuous sampling can be achieved by using the internal timer in the ADC, or triggering the SAMPLE task from one of the general purpose timers through the PPI.

Care shall be taken to ensure that the sample rate fulfils the following criteria, depending on how many channels are active:

 $f_{SAMPLE} < 1/[t_{ACQ} + t_{conv}]$



The SAMPLERATE register can be used as a local timer instead of triggering individual SAMPLE tasks. When SAMPLERATE.MODE is set to Timers, it is sufficient to trigger SAMPLE task only once in order to start the SAADC and triggering the STOP task will stop sampling. The SAMPLERATE.CC field controls the sample rate.

The SAMPLERATE timer mode cannot be combined with SCAN mode, and only one channel can be enabled in this mode.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

37.5.3 Oversampling

An accumulator in the ADC can be used to average noise on the analog input. In general, oversampling improves the signal-to-noise ratio (SNR). Oversampling, however, does not improve the integral non-linearity (INL), or differential non-linearity (DNL).

Oversampling and scan should not be combined, since oversampling and scan will average over input channels.

The accumulator is controlled in the OVERSAMPLE register. The SAMPLE task must be set 2^{OVERSAMPLE} number of times before the result is written to RAM. This can be achieved by:

- Configuring a fixed sampling rate using the local timer or a general purpose timer and PPI to trigger a SAMPLE task
- Triggering SAMPLE 2^{OVERSAMPLE} times from software
- · Enabling BURST mode

CH[n].CONFIG.BURST can be enabled to avoid setting SAMPLE task $2^{\text{OVERSAMPLE}}$ times. With BURST = 1 the ADC will sample the input $2^{\text{OVERSAMPLE}}$ times as fast as it can (actual timing: $<(t_{\text{ACQ}}+t_{\text{CONV}})\times2^{\text{OVERSAMPLE}})$. Thus, for the user it will just appear like the conversion took a bit longer time, but other than that, it is similar to one-shot mode. Scan mode can be combined with BURST=1, if burst is enabled on all channels.

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals that enough conversions have taken place for an oversampled result to get transferred into RAM. Note that both events may occur before the actual value has been transferred into RAM by EasyDMA.

37.5.4 Scan mode

A channel is considered enabled if CH[n].PSELP is set. If more than one channel, CH[n], is enabled, the ADC enters scan mode.

In scan mode, one SAMPLE task will trigger one conversion per enabled channel. The time it takes to sample all channels is:

```
Total time < Sum (CH[x].t<sub>ACO</sub>+t<sub>CONV</sub>), x=0..enabled channels
```

A DONE event signals that one sample has been taken.

In this mode, the RESULTDONE event signals has the same meaning as DONE when no oversampling takes place. Note that both events may occur before the actual values have been transferred into RAM by EasyDMA.

Figure 99: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 361 provides an example of results placement in Data RAM, with an even RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled.



	31 16	15 0
RESULT.PTR	CH[2] 1 st result	CH[1] 1 st result
RESULT.PTR + 4	CH[1] 2 nd result	CH[5] 1 st result
RESULT.PTR + 8	CH[5] 2 nd result	CH[2] 2 nd result
	(.)
RESULT.PTR + 2*(RESULT.MAXCNT – 2)	CH[5] last result	CH[2] last result

Figure 99: Example of RAM placement (even RESULT.MAXCNT), channels 1, 2 and 5 enabled

Figure 100: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled on page 361 provides an example of results placement in Data RAM, with an odd RESULT.MAXCNT. In this example, channels 1, 2 and 5 are enabled, all others are disabled. The last 32-bit word is populated only with one 16-bit result.

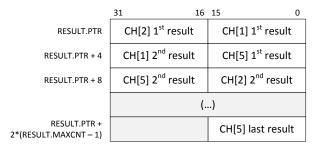


Figure 100: Example of RAM placement (odd RESULT.MAXCNT), channels 1, 2 and 5 enabled

37.6 EasyDMA

After configuring RESULT.PTR and RESULT.MAXCNT, the ADC resources are started by triggering the START task. The ADC is using EasyDMA to store results in a Result buffer in RAM.

The Result buffer is located at the address specified in the RESULT.PTR register. The RESULT.PTR register is double-buffered and it can be updated and prepared for the next START task immediately after the STARTED event is generated. The size of the Result buffer is specified in the RESULT.MAXCNT register and the ADC will generate an END event when it has filled up the Result buffer, see *Figure 101: ADC* on page 362. Results are stored in little-endian byte order in Data RAM. Every sample will be sign extended to 16 bit before stored in the Result buffer.

The ADC is stopped by triggering the STOP task. The STOP task will terminate an ongoing sampling. The ADC will generate a STOPPED event when it has stopped. If the ADC is already stopped when the STOP task is triggered, the STOPPED event will still be generated.



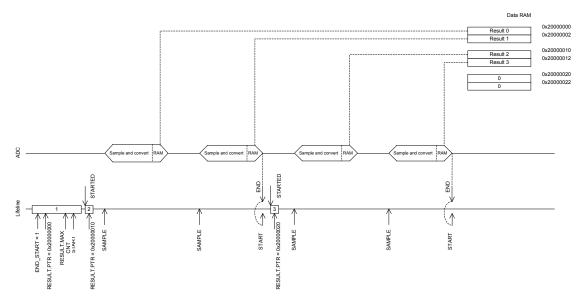


Figure 101: ADC

If the RESULT.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

The EasyDMA will have finished accessing the RAM when the END or STOPPED event has been generated.

The RESULT.AMOUNT register can be read following an END event or a STOPPED event to see how many results have been transferred to the Result buffer in RAM since the START task was triggered.

In Scan mode, the size of the Result buffer must be large enough to have room for a minimum one result from each of the enabled channels. To secure this, RESULT.MAXCNT must be specified to RESULT.MAXCNT >= "number of channels enabled". See *Scan mode* on page 360 for more information about Scan mode.

37.7 Resistor ladder

The ADC has an internal resistor string for positive and negative input.

See Figure 102: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP) on page 363. The resistors are controlled in the CH[n].CONFIG.RESP and CH[n].CONFIG.RESN registers.



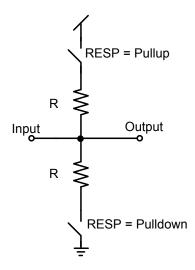


Figure 102: Resistor ladder for positive input (negative input is equivalent, using RESN instead of RESP)

37.8 Reference

The ADC can use two different references, controlled in the REFSEL field of the CH[n].CONFIG register.

These are:

- · Internal reference
- VDD as reference

The internal reference results in an input range of ± 0.6 V on the ADC core. VDD as reference results in an input range of $\pm VDD/4$ on the ADC core. The gain block can be used to change the effective input range of the ADC.

```
Input range = (+- 0.6 \text{ V or } +-\text{VDD}/4)/\text{Gain}
```

For example, choosing VDD as reference, single ended input (grounded negative input), and a gain of 1/4 the input range will be:

```
Input range = (VDD/4)/(1/4) = VDD
```

With internal reference, single ended input (grounded negative input), and a gain of 1/6 the input range will be:

```
Input range = (0.6 \text{ V})/(1/6) = 3.6 \text{ V}
```

The AIN0-AIN7 inputs cannot exceed VDD, or be lower than VSS.

37.9 Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see *Figure 103: Simplified ADC sample network* on page 364. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source (R_{source}) resistance. For high source resistance the acquisition time should be increased, see *Table 89: Acquisition time* on page 364.



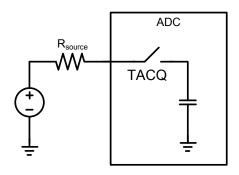


Figure 103: Simplified ADC sample network

Table 89: Acquisition time

TACQ [µs]	Maximum source resistance [kOhm]
3	10
5	40
10	100
15	200
20	400
40	800

37.10 Limits event monitoring

A channel can be event monitored by configuring limit register CH[n].LIMIT.

If the conversion result is higher than the defined high limit, or lower than the defined low limit, the appropriate event will get fired.

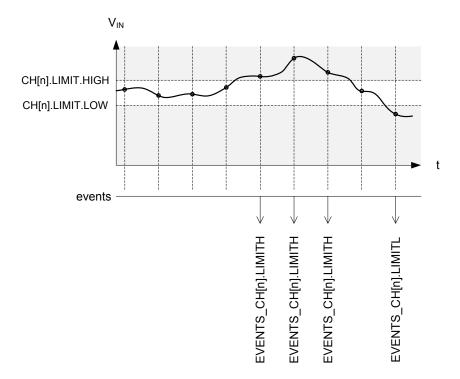


Figure 104: Example of limits monitoring on channel 'n'

Note that when setting the limits, CH[n].LIMIT.HIGH shall always be higher than or equal to CH[n].LIMIT.LOW . In other words, an event can be fired only when the input signal has been sampled



outside of the defined limits. It is not possible to fire an event when the input signal is inside a defined range by swapping high and low limits.

The comparison to limits always takes place, there is no need to enable it. If comparison is not required on a channel, the software shall simply ignore the related events. In that situation, the value of the limits registers is irrelevant, so it does not matter if CH[n].LIMIT.LOW is lower than CH[n].LIMIT.HIGH or not.

37.11 Registers

Table 90: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40007000	SAADC	SAADC	Analog to digital converter	

Table 91: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the ADC and prepare the result buffer in RAM
TASKS_SAMPLE	0x004	Take one ADC sample, if scan is enabled all channels are sampled
TASKS_STOP	0x008	Stop the ADC and terminate any on-going conversion
TASKS_CALIBRATEOFFSE	0x00C	Starts offset auto-calibration
EVENTS_STARTED	0x100	The ADC has started
EVENTS_END	0x104	The ADC has filled up the Result buffer
EVENTS_DONE	0x108	A conversion task has been completed. Depending on the mode, multiple conversions might be
		needed for a result to be transferred to RAM.
EVENTS_RESULTDONE	0x10C	A result is ready to get transferred to RAM.
EVENTS_CALIBRATEDON	0x110	Calibration is complete
EVENTS_STOPPED	0x114	The ADC has stopped
EVENTS_CH[0].LIMITH	0x118	Last results is equal or above CH[0].LIMIT.HIGH
EVENTS_CH[0].LIMITL	0x11C	Last results is equal or below CH[0].LIMIT.LOW
EVENTS_CH[1].LIMITH	0x120	Last results is equal or above CH[1].LIMIT.HIGH
EVENTS_CH[1].LIMITL	0x124	Last results is equal or below CH[1].LIMIT.LOW
EVENTS_CH[2].LIMITH	0x128	Last results is equal or above CH[2].LIMIT.HIGH
EVENTS_CH[2].LIMITL	0x12C	Last results is equal or below CH[2].LIMIT.LOW
EVENTS_CH[3].LIMITH	0x130	Last results is equal or above CH[3].LIMIT.HIGH
EVENTS_CH[3].LIMITL	0x134	Last results is equal or below CH[3].LIMIT.LOW
EVENTS_CH[4].LIMITH	0x138	Last results is equal or above CH[4].LIMIT.HIGH
EVENTS_CH[4].LIMITL	0x13C	Last results is equal or below CH[4].LIMIT.LOW
EVENTS_CH[5].LIMITH	0x140	Last results is equal or above CH[5].LIMIT.HIGH
EVENTS_CH[5].LIMITL	0x144	Last results is equal or below CH[5].LIMIT.LOW
EVENTS_CH[6].LIMITH	0x148	Last results is equal or above CH[6].LIMIT.HIGH
EVENTS_CH[6].LIMITL	0x14C	Last results is equal or below CH[6].LIMIT.LOW
EVENTS_CH[7].LIMITH	0x150	Last results is equal or above CH[7].LIMIT.HIGH
EVENTS_CH[7].LIMITL	0x154	Last results is equal or below CH[7].LIMIT.LOW
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
STATUS	0x400	Status
ENABLE	0x500	Enable or disable ADC
CH[0].PSELP	0x510	Input positive pin selection for CH[0]
CH[0].PSELN	0x514	Input negative pin selection for CH[0]
CH[0].CONFIG	0x518	Input configuration for CH[0]
CH[0].LIMIT	0x51C	High/low limits for event monitoring a channel
CH[1].PSELP	0x520	Input positive pin selection for CH[1]
CH[1].PSELN	0x524	Input negative pin selection for CH[1]
CH[1].CONFIG	0x528	Input configuration for CH[1]
CH[1].LIMIT	0x52C	High/low limits for event monitoring a channel
CH[2].PSELP	0x530	Input positive pin selection for CH[2]



Register	Offset	Description
CH[2].PSELN	0x534	Input negative pin selection for CH[2]
CH[2].CONFIG	0x538	Input configuration for CH[2]
CH[2].LIMIT	0x53C	High/low limits for event monitoring a channel
CH[3].PSELP	0x540	Input positive pin selection for CH[3]
CH[3].PSELN	0x544	Input negative pin selection for CH[3]
CH[3].CONFIG	0x548	Input configuration for CH[3]
CH[3].LIMIT	0x54C	High/low limits for event monitoring a channel
CH[4].PSELP	0x550	Input positive pin selection for CH[4]
CH[4].PSELN	0x554	Input negative pin selection for CH[4]
CH[4].CONFIG	0x558	Input configuration for CH[4]
CH[4].LIMIT	0x55C	High/low limits for event monitoring a channel
CH[5].PSELP	0x560	Input positive pin selection for CH[5]
CH[5].PSELN	0x564	Input negative pin selection for CH[5]
CH[5].CONFIG	0x568	Input configuration for CH[5]
CH[5].LIMIT	0x56C	High/low limits for event monitoring a channel
CH[6].PSELP	0x570	Input positive pin selection for CH[6]
CH[6].PSELN	0x574	Input negative pin selection for CH[6]
CH[6].CONFIG	0x578	Input configuration for CH[6]
CH[6].LIMIT	0x57C	High/low limits for event monitoring a channel
CH[7].PSELP	0x580	Input positive pin selection for CH[7]
CH[7].PSELN	0x584	Input negative pin selection for CH[7]
CH[7].CONFIG	0x588	Input configuration for CH[7]
CH[7].LIMIT	0x58C	High/low limits for event monitoring a channel
RESOLUTION	0x5F0	Resolution configuration
OVERSAMPLE	0x5F4	Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is
		applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.
SAMPLERATE	0x5F8	Controls normal or continuous sample rate
RESULT.PTR	0x62C	Data pointer
RESULT.MAXCNT	0x630	Maximum number of buffer words to transfer
RESULT.AMOUNT	0x634	Number of buffer words transferred since last START

37.11.1 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit r	number	•		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	STARTED			Enable or disable interrupt for STARTED event
					See EVENTS_STARTED
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	END			Enable or disable interrupt for END event
					See EVENTS_END
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	DONE			Enable or disable interrupt for DONE event
					See EVENTS_DONE
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	RESULTDONE			Enable or disable interrupt for RESULTDONE event
					See EVENTS_RESULTDONE
			Disabled	0	Disable
			Enabled	1	Enable



Bit r	numbe	er		31 30	29	28 2	7 26	25 24	V U T S R Q P O N M L K J I H G F E D C B A
	et 0x0	0000000		0 0	0	0 (0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
Ε	RW	CALIBRATEDONE							Enable or disable interrupt for CALIBRATEDONE event
									See EVENTS_CALIBRATEDONE
			Disabled	0					Disable
			Enabled	1					Enable
F	RW	STOPPED							Enable or disable interrupt for STOPPED event
				_					See EVENTS_STOPPED
			Disabled Enabled	0					Disable Enable
G	RW	CHOLIMITH	Ellabled	1					Enable or disable interrupt for CH[0].LIMITH event
Ū		C.102.11							
			Disabled	0					See EVENTS_CH[0].LIMITH Disable
			Enabled	1					Enable
Н	RW	CHOLIMITL							Enable or disable interrupt for CH[0].LIMITL event
									See EVENTS_CH[0].LIMITL
			Disabled	0					Disable
			Enabled	1					Enable
I	RW	CH1LIMITH							Enable or disable interrupt for CH[1].LIMITH event
									See EVENTS_CH[1].LIMITH
			Disabled	0					Disable
	D\A/	CH1LIMITL	Enabled	1					Enable Enable or disable interrupt for CH[1] LIMITL event
J	KVV	CHILIMITE							Enable or disable interrupt for CH[1].LIMITL event
			Disabled	0					See EVENTS_CH[1].LIMITL Disable
			Enabled	1					Enable
K	RW	CH2LIMITH		_					Enable or disable interrupt for CH[2].LIMITH event
									See EVENTS_CH[2].LIMITH
			Disabled	0					Disable
			Enabled	1					Enable
L	RW	CH2LIMITL							Enable or disable interrupt for CH[2].LIMITL event
									See EVENTS_CH[2].LIMITL
			Disabled	0					Disable
	DIA	CURLINATE	Enabled	1					Enable
М	RW	CH3LIMITH							Enable or disable interrupt for CH[3].LIMITH event
			S. 11.1						See EVENTS_CH[3].LIMITH
			Disabled Enabled	0 1					Disable Enable
N	RW	CH3LIMITL	Litabica	1					Enable or disable interrupt for CH[3].LIMITL event
									See EVENTS CH[3].LIMITL
			Disabled	0					Disable
			Enabled	1					Enable
0	RW	CH4LIMITH							Enable or disable interrupt for CH[4].LIMITH event
									See EVENTS_CH[4].LIMITH
			Disabled	0					Disable
			Enabled	1					Enable
Р	RW	CH4LIMITL							Enable or disable interrupt for CH[4].LIMITL event
									See EVENTS_CH[4].LIMITL
			Disabled	0					Disable
Q	R/v/	CH5LIMITH	Enabled	1					Enable Enable or disable interrupt for CH[5].LIMITH event
٧		S. ISERTITI							
									See EVENTS_CH[5].LIMITH



Bitı	numbe	er		31	30 2	9 28	27	26 2	25 2	24 2	23 2	22 2	1 20	0 19	18	3 17	16	15	14	13	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id												٧	/ L	ΙT	S	R	Q	Р	0	N	М	L K	J	-1	Н	G	F	Е	D (В	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0 (0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Val	ue					D	Des	script	tion																		
			Disabled	0						D	Disa	able																			
			Enabled	1						E	na	able																			
R	RW	CH5LIMITL								Е	na	able o	or d	isab	le i	ntei	rup	t fo	or Cl	1[5]].LIN	IITL	eve	nt							
										S	ee	EVE	NTS	C C	1[5]	.LIN	ΛΙΤΙ														
			Disabled	0						D	Disa	able		_																	
			Enabled	1						Ε	na	able																			
S	RW	CH6LIMITH								Ε	na	able o	or d	isab	le i	ntei	rrup	t fo	r Cl	1[6]].LIN	IITH	eve	ent							
										ς	مم	EVE	NITS	: CI	4[6]		літі	,													
			Disabled	0								able	1415		iloj	·LIII		•													
			Enabled	1								able																			
Т	RW	CH6LIMITL	Z. I. G. Z.	-								able o	or d	isab	ıle i	ntei	rur	t fo	or Cl	1[6]	l.LIN	1ITL	eve	nt							
																	·			-[-]	,										
												EVE	NTS	_CF	1[6]	.LIN	ΛΙΤΙ														
			Disabled	0								able																			
			Enabled	1								ble																			
U	RW	CH7LIMITH								E	na	able o	or d	isab	ile i	ntei	rrup	t fo	or Cl	1[7]	J.LIIV	IITH	eve	ent							
										S	ee	EVE	NTS	_CF	1[7]	.LIN	1ITI	1													
			Disabled	0						D	Disa	able																			
			Enabled	1						Е	na	able																			
٧	RW	CH7LIMITL								Е	na	able o	or d	isab	le i	ntei	rup	t fo	r Cl	1[7]].LIN	IITL	eve	nt							
										S	iee	EVE	NTS	CF	1[7]	.LIN	ΛΙΤΙ														
			Disabled	0						D	Disa	able																			
			Enabled	1						Е	na	able																			

37.11.2 INTENSET

Address offset: 0x304

Enable interrupt

	number	3	31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0														
Id				V U T S R Q P O N M L K J I H G F E D C B A														
Res	set 0x00000000	C	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0														
Id	RW Field Val	lue Id \	/alue	Description														
Α	RW STARTED			Write '1' to Enable interrupt for STARTED event														
				See EVENTS_STARTED														
	Set	t 1	1	Enable														
	Disa	sabled ()	Read: Disabled														
	Ena	abled 1	1	Read: Enabled														
В	RW END			Write '1' to Enable interrupt for END event														
				See EVENTS_END														
	Set	t 1	1	Enable														
	Disa	sabled ()	Read: Disabled														
	Ena	abled 1	1	Read: Enabled														
С	RW DONE			Write '1' to Enable interrupt for DONE event														
				See EVENTS_DONE														
	Set	t 1	1	Enable														
	Disa	sabled ()	Read: Disabled														
	Ena	abled 1	1	Read: Enabled														
D	RW RESULTDONE			Write '1' to Enable interrupt for RESULTDONE event														
				See EVENTS_RESULTDONE														
	Set	t 1	1	Enable														
	Disa	sabled ()	Read: Disabled														
	Ena	abled 1	1	Read: Enabled														



Bit r	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Ε	RW CALIBRATEDONE			Write '1' to Enable interrupt for CALIBRATEDONE event
				See EVENTS_CALIBRATEDONE
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS STORRED
		C-1	4	See EVENTS_STOPPED
		Set	1	Enable Control of Cont
		Disabled Enabled	0	Read: Disabled Read: Enabled
_	DW CHOUNITH	Enabled	1	
G	RW CHOLIMITH			Write '1' to Enable interrupt for CH[0].LIMITH event
				See EVENTS_CH[0].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW CHOLIMITL			Write '1' to Enable interrupt for CH[0].LIMITL event
				See EVENTS_CH[0].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
T	RW CH1LIMITH			Write '1' to Enable interrupt for CH[1].LIMITH event
				See EVENTS_CH[1].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW CH1LIMITL			Write '1' to Enable interrupt for CH[1].LIMITL event
		6.1		See EVENTS_CH[1].LIMITL
		Set	1	Enable
		Disabled Enabled	0	Read: Disabled Read: Enabled
K	RW CH2LIMITH	Enabled	1	
K	RW CHZLIIVIITH			Write '1' to Enable interrupt for CH[2].LIMITH event
				See EVENTS_CH[2].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW CH2LIMITL			Write '1' to Enable interrupt for CH[2].LIMITL event
				See EVENTS_CH[2].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
М	RW CH3LIMITH			Write '1' to Enable interrupt for CH[3].LIMITH event
				See EVENTS_CH[3].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
N	RW CH3LIMITL			Write '1' to Enable interrupt for CH[3].LIMITL event
		Sot	1	See EVENTS_CH[3].LIMITL
		Set	1	Enable Read: Disabled
		Disabled Enabled	0	Read: Disabled Read: Enabled
0	RW CH4LIMITH	LIIANICU	1	Write '1' to Enable interrupt for CH[4].LIMITH event
0	NW CH4LIIVIII II			write 1 to chable interrupt for Cri[4].Livilin event



Bit r	number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
				See EVENTS_CH[4].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Р	RW CH4LIMITL			Write '1' to Enable interrupt for CH[4].LIMITL event
				See EVENTS_CH[4].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Q	RW CH5LIMITH			Write '1' to Enable interrupt for CH[5].LIMITH event
				See EVENTS_CH[5].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
R	RW CH5LIMITL			Write '1' to Enable interrupt for CH[5].LIMITL event
				See EVENTS_CH[5].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
S	RW CH6LIMITH			Write '1' to Enable interrupt for CH[6].LIMITH event
				See EVENTS_CH[6].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Т	RW CH6LIMITL			Write '1' to Enable interrupt for CH[6].LIMITL event
				See EVENTS_CH[6].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
U	RW CH7LIMITH			Write '1' to Enable interrupt for CH[7].LIMITH event
				See EVENTS_CH[7].LIMITH
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
V	RW CH7LIMITL			Write '1' to Enable interrupt for CH[7].LIMITL event
				See EVENTS CH[7].LIMITL
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
		Litabica	-	neua: Enableu

37.11.3 INTENCLR

Address offset: 0x308 Disable interrupt

	Bit number 31 30 29 28 27 26 25 24									23	22	21	20 :	19 1	L8 1	.7 1	6 1	5 14	1 13	12	11	10	9	8 7	7 6	5 5	5 4	3	2	1	0			
	Id														٧	U	Т	S	R C	Q P	0	N	М	L	K	J	I E	1 (6 F	E	D	С	В	Α
	Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () () (0	0	0	0	0
	Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
ı	Α	RW	STARTED										Wr	rite '	'1' t	o D	isab	le i	nter	rup	t fo	r ST	ART	ED 6	ver	nt								_
														See EVENTS_STARTED																				
				Clear	1								Dis	able	е																			



See EVENTS, DOME		numbe	er		3:	1 30	29	28 2	27 2	6 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
March Marc		o+ 0v0	000000		٥	۰	۸	٥	۰ ،		
Disabled				Malica Id				U	0 (ט כ	
Frable	Ia	KW	rieia								*
Sec Ward Sec Ward Sec Ward Sec Ward Sec											
Clear	D	D\A/	END	Enabled	1						
Clear 1	ь	KVV	END								write 1 to disable interrupt for END event
Disabled Final											See EVENTS_END
Enabled 1				Clear	1						Disable
Company				Disabled	0						
Clear				Enabled	1						
Clear	С	RW	DONE								Write '1' to Disable interrupt for DONE event
Disabled Centrolled Centr											See EVENTS_DONE
Read				Clear	1						Disable
D RW RESULTONE				Disabled	0						Read: Disabled
Clear				Enabled	1						Read: Enabled
Clear	D	RW	RESULTDONE								Write '1' to Disable interrupt for RESULTDONE event
Clear											See EVENTS RESULTDONE
E RW CALIBRATEDONE				Clear	1						
RW CALIBRATEDONE				Disabled	0						
Clear				Enabled	1						Read: Enabled
Clear	E	RW	CALIBRATEDONE								Write '1' to Disable interrupt for CALIBRATEDONE event
Clear											SOO EVENTS CALIBRATEDONE
Disabled Enabled Read: Disabled Read: Chabled Read: Disabled Read: Disabled Read: Disabled Read: Disabled Read: Disabled Read: Disabled Read: Chabled				Cloar	1						
RW STOPPED											
F RW STOPPED See EVENTS_STOPPED											
Clear	F	RW	STOPPED	Lilabica	_						
Clear	•		31011125								
Disabled Disabled Enabled Disabled											
Enabled 1 Read: Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[0].LIMITH event See EVENTS_CH[0].LIMITH See EVENTS_CH[0].LIMITH Disable Clear 1 Disabled Dis											
G RW CHOLIMITH Clear											
See EVENTS_CH[0].LIMITH Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled H RW CHOLIMITL Clear 1 Disable Disabled 0 Read: Disable interrupt for CH[0].LIMITL event See EVENTS_CH[0].LIMITL Clear 1 Disable Enabled 1 Read: Enabled Frabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITH event See EVENTS_CH[1].LIMITH Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITH event See EVENTS_CH[1].LIMITH Clear 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear 1 Disable Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear 1 Disable Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Clear 1 Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Clear 1 Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Clear 1 Disable	_	DIA	CHOLINAITH	Enabled	1						
Clear 1 Disable	G	KVV	CHULIMITH								Write 1 to Disable Interrupt for Ch[U].LIMITH event
Disabled											See EVENTS_CH[0].LIMITH
H RW CHOLIMITL Clear Disabled Disabled Clear Disabled Disabled Enabled Clear Disabled Disabled Enabled Clear Disabled Enabled Disabled Enabled Disabled Enabled Disabled Enabled Disabled Enabled Disabled Enabled Disabled Disabled Disabled Disabled Enabled Disabled Disabled Disabled Enabled Disabled Enabled Disabled Disabled Enabled Disabled Enabled Write '1' to Disable interrupt for CH[1].LIMITH event See EVENTS_CH[1].LIMITL Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear Disabled Disabled Write '1' to Disabled Enabled Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH See EVENTS_CH[2].LIMITH Disable				Clear	1						Disable
H RW CHOLIMITL Clear Disabled Disabled Enabled Disabled				Disabled	0						Read: Disabled
See EVENTS_CH[0].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITH event See EVENTS_CH[1].LIMITH Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Finabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITH Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear 1 Disable Read: Disabled Read: Disabled Write '1' to Disable interrupt for CH[2].LIMITL Clear 1 Disable Write '1' to Disable interrupt for CH[2].LIMITH Clear 1 Read: Enabled Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Clear 1 Disable				Enabled	1						
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Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITH event See EVENTS_CH[1].LIMITH Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITH Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[2].LIMITH Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Clear 1 Disable											See EVENTS_CH[0].LIMITL
RW CHILIMITH Clear 1 Rwite '1' to Disable interrupt for CH[1].LIMITH event				Clear	1						Disable
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See EVENTS_CH[1].LIMITH Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled K RW CH2LIMITH Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH See EVENTS_CH[2].LIMITH Clear 1 Disable				Enabled	1						Read: Enabled
Clear 1 Disabled Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear 1 Disabled Enabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Clear 1 Disable	I	RW	CH1LIMITH								Write '1' to Disable interrupt for CH[1].LIMITH event
Clear 1 Disabled Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear 1 Disabled Enabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Clear 1 Disable											See EVENTS_CH[1].LIMITH
Enabled J RW CH1LIMITL Clear Disabled Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear Disabled Read: Disabled Enabled The Read: Enabled Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Clear 1 Disable				Clear	1						
Write '1' to Disable interrupt for CH[1].LIMITL event See EVENTS_CH[1].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled K RW CH2LIMITH Clear 1 Disable Write '1' to Disable interrupt for CH[2].LIMITH Clear 1 Disable											
See EVENTS_CH[1].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled K RW CH2LIMITH Clear 1 Disable Write '1' to Disable interrupt for CH[2].LIMITH Clear 1 Disable				Enabled	1						Read: Enabled
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled K RW CH2LIMITH Clear 1 Disable Clear 1 Disable	J	RW	CH1LIMITL								Write '1' to Disable interrupt for CH[1].LIMITL event
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled K RW CH2LIMITH Clear 1 Disable Clear 1 Disable											See EVENTS CHI11.LIMITL
Disabled 0 Read: Disabled Enabled 1 Read: Enabled K RW CH2LIMITH Clear 1 Disable				Clear	1						
Enabled 1 Read: Enabled K RW CH2LIMITH											
K RW CH2LIMITH Write '1' to Disable interrupt for CH[2].LIMITH event See EVENTS_CH[2].LIMITH Clear 1 Disable											
See EVENTS_CH[2].LIMITH Clear 1 Disable	K	RW	CH2LIMITH		_						
Clear 1 Disable											
				Class							
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No.	Bit n	ıumbe	r		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
No. Field Value Chabled 1 Read Enabled	Id					V U T S R Q P O N M L K J I H G F E D C B A
Enabled 1	Rese	et 0x0	0000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
More 1's to Disable interrupt for CH 2 LMMTL event	Id	RW	Field	Value Id	Value	Description
Sec EVENTS_CHS_LIMBT1				Enabled	1	
Clear	L	RW	CH2LIMITL			Write '1' to Disable interrupt for CH[2].LIMITL event
Disabled Finalized 1 Result Franker 1 R						See EVENTS_CH[2].LIMITL
Enabled 1				Clear	1	Disable
M NW CHSLIMITH				Disabled	0	Read: Disabled
Clear				Enabled	1	
Clear	М	RW	CH3LIMITH			Write '1' to Disable interrupt for CH[3].LIMITH event
N RW CHILIMITL See FVENTS_CHIS_LIMITL Se						See EVENTS_CH[3].LIMITH
Read				Clear		Disable
No. RW CH3UMITL						
See EVENTS_CH[3]_LIMITL		D144		Enabled	1	
Clear	N	RW	CH3LIMITL			Write '1' to Disable interrupt for CH[3].LIMITL event
Disabled Disabled Disabled Read: Enabled Read: Enabl						See EVENTS_CH[3].LIMITL
Final						
Write '1' to Disable interrupt for CH[4], LIMITH event						
Clear		DIA	CHALINATU	Enabled	1	
Clear	U	KVV	CH4LIMITH			write 1 to disable interrupt for CH[4].LIMITH event
Read						
P RW CH4LIMITL						
Clear	D	D\A/	CHALIMITI	Enabled	1	
Clear	F	11.00	CHALIMITE			
Disabled Enabled 1 Read: Enabled 1 Read: Enabled 1 Read: Enabled 2 Read: Enabled 3 Read: Enabled 3 Read: Enabled 3 Read: Enabled 3 Read: Disable interrupt for CH[5].LIMITH event See EVENTS_CH[5].LIMITH EVENTS_CH[5].LIMITH EVENTS_CH[5].LIMITH EVENTS_CH[5].LIMITH EVENTS_CH[5].LIMITL EVENTS_CH[5].LIMITL EVENTS_CH[5].LIMITL EVENTS_CH[5].LIMITL EVENTS_CH[5].LIMITL EVENTS_CH[5].LIMITL EVENTS_CH[5].LIMITL EVENTS_CH[5].LIMITL EVENTS_CH[6].LIMITH EVENTS_CH[6].LIMITH EVENTS_CH[6].LIMITH EVENTS_CH[6].LIMITH EVENTS_CH[6].LIMITH EVENTS_CH[6].LIMITH EVENTS_CH[6].LIMITH EVENTS_CH[6].LIMITH EVENTS_CH[6].LIMITL EVENTS_CH[6].LIMITH						
Raw CHSLIMITH Clear Disabled						
Q RW CHSLIMITH Clear						
Clear 1 Disable R RW CHSLIMITL Clear 1 Disable Clear 1 Clear Clear Clear 1 Clear	Q	RW	CH5LIMITH	Lilabica	-	
Clear 1 Disabled Clear						
Disabled				Clear	1	
R RW CH5LIMITL Clear 1 Disable Enabled T RW CH6LIMITH Clear 1 Disable Enabled Enabled 1 Read: Enabled Clear 1 Disable Enabled 1 Read: Enabled Framework (Fig.). LIMITH Clear 1 Disable Enabled 1 Read: Enabled See EVENTS_CH[6]. LIMITH Clear 1 Disable Clear 1 Disable Disable 0 Read: Disabled Enabled 1 Read: Enabled T RW CH6LIMITH Clear 1 Disable Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Enabled 1 Read: Enabled T Write '1' to Disable interrupt for CH[6]. LIMITH event See EVENTS_CH[6]. LIMITL Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Enabled 1 Read: Enabled Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Clear 1 Disable interrupt for CH[7]. LIMITH event See EVENTS_CH[7]. LIMITH Clear 1 Disable Disable 0 Read: Disabled						
R RW CHSLIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Virte '1' to Disable interrupt for CH[5].LIMITL event See EVENTS_CH[5].LIMITL Write '1' to Disable interrupt for CH[6].LIMITH event See EVENTS_CH[6].LIMITH Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Disabled 0 Read: Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable U RW CH7LIMITH Clear 1 Disable Disabled 0 Read: Disable Read: Disable Disabled 0 Read: Disable						
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled S RW CH6LIMITH Clear 1 Disable Enabled 0 Read: Disable interrupt for CH[6].LIMITH event See EVENTS_CH[6].LIMITH Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Clear 1 Disable Read: Disabled Read: Disabled Read: Disabled	R	RW	CH5LIMITL			
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled S RW CH6LIMITH Clear 1 Disable Enabled 0 Read: Disable interrupt for CH[6].LIMITH event See EVENTS_CH[6].LIMITH Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Enabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Clear 1 Disable Read: Disabled Read: Disabled Read: Disabled						See EVENTS CHIST LIMITI
Disabled 0 Read: Disabled Enabled 1 Read: Enabled S RW CH6LIMITH Clear 1 Disable 1 Read: Enabled T RW CH6LIMITL Clear 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Clear 1 Disable Read: Enabled T RW CH6LIMITL Clear 1 Disable Clear 1 Disable Disable Clear 1 Disable Read: Enabled T Read: Enabled T Read: Enabled Clear 1 Disable Enabled 1 Read: Enabled T Read: Enabled Read: Enabled Clear 1 Disable Enabled 1 Read: Enabled Read: Enabled CH7LIMITH Clear 1 Disable Read: Enabled Clear 1 Disable Read: Enabled Clear 1 Disable Read: Disable Clear 1 Disable Read: Disable Clear 1 Disable Read: Disable Clear 1 Disable Clear 1 Disable Read: Disable				Clear	1	
S RW CH6LIMITH Write '1' to Disable interrupt for CH[6].LIMITH Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Clear 1 Disable See EVENTS_CH[6].LIMITL Write '1' to Disable interrupt for CH[6].LIMITL See EVENTS_CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Clear 1 Disable Read: Enabled Disable O Read: Disabled Read: Disabled						
See EVENTS_CH[6].LIMITH Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled T RW CH6LIMITL Clear 1 Disable Clear 1 Disable Disable OREAD: Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Disable interrupt for CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled				Enabled	1	Read: Enabled
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled TRW CH6LIMITL Clear 1 Disable Disabled 0 Read: Enabled Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Enabled 1 Read: Disabled Write '1' to Disabled Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Disable Disabled 0 Read: Disabled	S	RW	CH6LIMITH			Write '1' to Disable interrupt for CH[6].LIMITH event
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled TRW CH6LIMITL Clear 1 Disable Disabled 0 Read: Enabled Clear 1 Disable Enabled 1 Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Enabled 1 Read: Disabled Write '1' to Disabled Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Disable Disabled 0 Read: Disabled						See EVENTS CH[6].LIMITH
Enabled T RW CH6LIMITL Clear Disabled Disabled T RW CH7LIMITH Clear Disabled Disabled Enabled T RW CH7LIMITH Clear Disabled Enabled Disabled Read: Enabled Write '1' to Disable interrupt for CH[6].LIMITL Disabled Read: Disabled Write '1' to Disabled Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear Disabled Disabled Read: Disabled				Clear	1	
T RW CH6LIMITL Write '1' to Disable interrupt for CH[6].LIMITL event See EVENTS_CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Write '1' to Disable interrupt for CH[7].LIMITH See EVENTS_CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled				Disabled	0	Read: Disabled
See EVENTS_CH[6].LIMITL Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Clear 1 Disable Disabled 0 Read: Disable Read: Enabled				Enabled	1	Read: Enabled
Clear 1 Disable Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Clear 1 Disable Disabled 0 Read: Disabled	Т	RW	CH6LIMITL			Write '1' to Disable interrupt for CH[6].LIMITL event
Disabled 0 Read: Disabled Enabled 1 Read: Enabled U RW CH7LIMITH Clear 1 Disable Disabled 0 Read: Disabled						See EVENTS_CH[6].LIMITL
Enabled 1 Read: Enabled U RW CH7LIMITH Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled				Clear	1	Disable
U RW CH7LIMITH Write '1' to Disable interrupt for CH[7].LIMITH event See EVENTS_CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled				Disabled	0	Read: Disabled
See EVENTS_CH[7].LIMITH Clear 1 Disable Disabled 0 Read: Disabled				Enabled	1	
Clear 1 Disable Disabled 0 Read: Disabled	U	RW	CH7LIMITH			Write '1' to Disable interrupt for CH[7].LIMITH event
Disabled 0 Read: Disabled						See EVENTS_CH[7].LIMITH
				Clear	1	Disable
Enabled 1 Read: Enabled				Disabled	0	Read: Disabled
				Enabled	1	Read: Enabled



Bit	numbe	er		3:	1 30	29	28	8 27	7 2	26 2	5 :	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6 !	5 4	4 3	2	1	0
Id															٧	U	Т	S	R	Q	Р	О	Ν	М	L	K	J	1 1	4	G I	= 6	E D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0)	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 () (0 0	0	0	0
Id	RW	Field	Value Id	V	alue								Des	scri	ptic	on																			
٧	RW	CH7LIMITL										,	Wr	ite ˈ	'1' t	o D	isa	ble	inte	erru	ıpt	for	СН	[7].	LIM	ITL	eve	ent							
												:	See	e EV	/EN	TS_	СН	[7].	LIM	ITL															
			Clear	1									Dis	able	e																				
			Disabled	0									Rea	ad:	Disa	able	ed																		
			Enabled	1									Rea	ad:	Ena	ble	d																		

37.11.4 STATUS

Address offset: 0x400

Status

Bit	numbe	r		33	1 30	29	28	27	26	25	24	23	22	21	20 :	19 1	8 1	.7 1	6 1	5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id																																	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0 () () (0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	V	alue	•						De	scri	ptic	n																		
Α	R	STATUS										Sta	tus																				
			Ready	0								ΑD	C is	rea	dy.	No	on-	goi	ng d	on	ver	sion											
			Busy	1								ΑD	C is	bus	sy. (Conv	/ers	ion	in	oro	gre	SS.											

37.11.5 ENABLE

Address offset: 0x500 Enable or disable ADC

Bitı	numbe	r		31 30 2	9 28 2	27 26	25	24 2	23 2	2 2	1 20	19	18	17 1	.6 1	.5 14	13	12 1	1 1	0 9	8	7	6	5	4	3	2	1 0
Id																												Α
Res	et 0x0	0000000		0 0	0 0	0 0	0	0	0 0	0	0	0	0	0	0 (0 0	0	0	0 (0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value					Desc	ript	tion																	
Α	RW	ENABLE						E	nab	ole c	or di	sabl	e A[OC														
			Disabled	0				[Disal	ble .	ADC	:																
			Enabled	1				E	Enab	le A	ADC																	
								١	Nhe	n ei	nabl	led,	the	ADC	wil	l aco	quire	acc	ess	to th	e ar	alo	g in	put	t			
								ķ	oins	spe	cifie	d in	the	CH	[n].l	PSEL	P an	d CH	l[n].	PSEL	N re	egis	ters	S.				

37.11.6 CH[0].PSELP

Address offset: 0x510

Input positive pin selection for CH[0]

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PSELP		Analog positive input channel
	NC	0 Not connected
	AnalogInput0	1 AINO
	AnalogInput1	2 AIN1
	AnalogInput2	3 AIN2
	AnalogInput3	4 AIN3
	AnalogInput4	5 AIN4
	AnalogInput5	6 AIN5
	AnalogInput6	7 AIN6
	AnalogInput7	8 AIN7
	VDD	9 VDD



37.11.7 CH[0].PSELN

Address offset: 0x514

Input negative pin selection for CH[0]

Bit r	numbe	r		31	30 2	9 2	8 27	7 26	25 2	24 2	3 22	21 2	0 :	19 18	3 1	7 16	5 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3 2	1	0
Id																												A A	A А	Α	Α
Rese	et 0x0	0000000		0	0 () (0	0	0	0 (0 0	0 (0	0 0	(0 0	C) (0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue					D	escr	iptio	n																		
Α	RW	PSELN								Α	nalo	g neg	ati	ve in	ıpu	ıt, eı	nak	les	diff	erei	ntia	l cha	ann	el							
			NC	0						Ν	lot co	onne	cte	d																	
			AnalogInput0	1						Α	IN0																				
			AnalogInput1	2						Α	IN1																				
			AnalogInput2	3						Α	IN2																				
			AnalogInput3	4						Α	NIN3																				
			AnalogInput4	5						Α	IN4																				
			AnalogInput5	6						Α	IN5																				
			AnalogInput6	7						Α	IN6																				
			AnalogInput7	8						Α	IN7																				
			VDD	9						٧	'DD																				

37.11.8 CH[0].CONFIG

Address offset: 0x518

Input configuration for CH[0]

Bit	numb	er		31	30	29	28	27	26 :	25 :	24 2	23	22 23	L 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 -	1 0
Id				-	. 50						G			F			E					D			С				В				A A
	et Oxí	00020000		0	0	0	0	0	0			0	0 0						0	0	0		0				0				0 (0 0
Id		Field	Value Id		lue					_			script				Ē	Ť	Ť	Ť		Ť											
Α	RW	RESP									F	Pos	sitive	cha	nne	l re	sist	or o	on	trol													
			Bypass	0							E	Вур	pass r	esis	tor	lad	der																
			Pulldown	1							F	Pul	II-dow	n to	o GN	ND																	
			Pullup	2							F	Pul	ll-up t	o V	DD																		
			VDD1_2	3							9	Set	t inpu	t at	VDI)/2																	
В	RW	RESN									1	Ne	gative	ch	ann	el r	esis	tor	100	ntro	ol												
			Bypass	0							E	Byp	pass r	esis	tor	lado	der																
			Pulldown	1							F	Pul	II-dow	n to	o GN	ND																	
			Pullup	2							F	Pul	ll-up t	o V	DD																		
			VDD1_2	3							9	Set	t inpu	t at	VDI)/2																	
С	RW	GAIN									(Gai	in cor	itro	l																		
			Gain1_6	0							1	1/6	5																				
			Gain1_5	1							1	1/5	5																				
			Gain1_4	2							1	1/4	4																				
			Gain1_3	3							1	1/3	3																				
			Gain1_2	4							1	1/2	2																				
			Gain1	5							1	1																					
			Gain2	6							2	2																					
			Gain4	7							4	4																					
D	RW	REFSEL									F	Ref	feren	ce c	onti	rol																	
			Internal	0									ernal					V)															
			VDD1_4	1									D/4 a																				
Ε	RW	TACQ									A	Acc	quisiti	on 1	time	e, th	ie ti	ime	th	e A	DC I	use	s to	saı	mpl	e th	ne ii	npu	t				
											١	vol	ltage																				
			3us	0								3 u																					
			5us	1								5 u																					
			10us	2							1	10	us																				
			15us	3							1	15	us																				
			20us	4							2	20	us																				



Bit	numbe	er		31 30	29	28	27	26	25 :	24 2	23 2	2 21	20	19	18	17	16	15	14 1	.3 1	2 1	1 10	9	8	7	6 5	5 4	3	2	1	0
Id										G			F		Ε	Ε	Ε			[)	С	С	С		E	3 E	3		Α	Α
Res	et 0x0	00020000		0 0	0	0	0	0	0	0	0 (0 0	0	0	0	1	0	0	0 (0 (0 0	0	0	0	0	0 () (0	0	0	0
Id	RW	Field	Value Id	Valu	•					ı	Desc	ript	ion																		
			40us	5						4	10 u	S																			
F	RW	MODE								1	Enab	ole d	iffer	ent	ial r	noc	le														
			SE	0						9	Singl	le en	ded	, PS	ELN	l wi	ll b	e ig	nore	ed,	neg	ative	inp	ut t	οА	DC					
										9	hor	ted 1	o G	ND																	
			Diff	1						ı	Diffe	rent	ial																		
G	RW	BURST								E	nat	ole b	urst	mo	de																
			Disabled	0							Burs	t mo	de i	s di	sab	led	(no	rma	al op	oera	oite	1)									
			Enabled	1							Burs	t mo	de i	s er	abl	ed.	SA	ADO	tak	(es	2^0	VER	SAN	1PLE	์ กเ	ımbe	er o	f			
										9	amı	oles	as fa	ast a	as it	car	ո. a	nd :	end	ls tl	ne a	vera	ge t	o D	ata	RAN	1.				

37.11.9 CH[0].LIMIT

Address offset: 0x51C

High/low limits for event monitoring a channel

Bit	nun	nbe	r		31	. 30	29	28	27	7 26	5 25	5 24	1 23	22	21	20	19	18 3	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	1 0
Id					В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	А А	. 4	A A
Res	et (0x7	FFF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0 0	C	0 0
Id	R	w	Field	Value Id	Va	lue							De	scri	ptic	n																			
Α	R	W	LOW		[-3	3276	58 t	0 +	327	767]		Lo	w le	vel	limi	it																		
В	R	w	HIGH		[-3	3276	58 t	0 +	327	767	1		Hi	gh le	evel	lim	it																		

37.11.10 CH[1].PSELP

Address offset: 0x520

Input positive pin selection for CH[1]

Bit number		31	30 2	9 2	28 2	7 2	26 2	5 2	4 2	3 22	2 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6 !	5 4	1 3	2	1	0
Id																											A	Α Α	A	Α	Α
Reset 0x00000000		0	0	0	0 (0	0 0) (0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0
ld RW Field	Value Id	Va	lue						C	escr	ripti	on																			
A RW PSELP									Δ	nalo	g po	ositi	ive	inp	ut	ha	nne	el													
	NC	0							Ν	lot c	onn	ect	ed																		
	AnalogInput0	1							Δ	NIN0																					
	AnalogInput1	2							Δ	NIN1																					
	AnalogInput2	3							Δ	AIN2																					
	AnalogInput3	4							Δ	NIN3																					
	AnalogInput4	5							Δ	IN4																					
	AnalogInput5	6							Δ	IN5																					
	AnalogInput6	7							Δ	IN6																					
	AnalogInput7	8							Δ	IN7																					
	VDD	9							٧	/DD																					

37.11.11 CH[1].PSELN

Address offset: 0x524

Input negative pin selection for CH[1]

Bitı	numbe	er		31 30	29	28	27 :	26 2	25 2	4 23	3 2:	2 21	20	19	18	17	16	15	14	13	12 1	11 1	0 9	8	7	6	5	4	3 2	2 1	L 0
Id																												Α	A A	A A	A А
Res	et 0x0	0000000		0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 () (0
ld	RW	Field	Value Id	Valu	•					D	esc	ript	ion																		
Α	RW	PSELN								A	nal	og n	ega	tive	inį	out,	en	able	es d	iffe	rent	ial	har	nel							
			NC	0						N	ot o	coni	nect	ed																	
			AnalogInput0	1						Α	IN0)																			



Bit number		31	L 30	29	28	27	26	25	24	23 :	22	21 2	20 :	19 :	18 1	17 :	16 1	15	14 1	.3 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																												A A	Δ Δ	Α	Α
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0
Id RW Field	Value Id	Va	alue							Des	cri	ptio	n																		
	AnalogInput1	2								AIN	1																				
	AnalogInput2	3								AIN	2																				
	AnalogInput3	4								AIN	3																				
	AnalogInput4	5								AIN	4																				
	AnalogInput5	6								AIN	5																				
	AnalogInput6	7								AIN	6																				
	AnalogInput7	8								AIN	7																				
	VDD	9								VDI)																				

37.11.12 CH[1].CONFIG

Address offset: 0x528

Input configuration for CH[1]

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d			G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0	0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0
d RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
O RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential
G RW BURST			Enable burst mode
	Disabled	0	Burst mode is disabled (normal operation)



Bit number		31 30 29 28 2	7 26 25 24 23 22 21	20 19 18	3 17 16	5 15 14 13	12 11	10 9	8 7	6	5 4	3 2	1 0)
Id			G	F E	E E		D	СС	С		в в		ΑА	4
Reset 0x00020000		0 0 0 0 0	000000	0 0 0	1 0	0 0 0	0 0	0 0	0 0	0	0 0	0 0	0 0)
Id RW Field	Value Id	Value	Descripti	on										
	Enabled	1	Burst mo	de is enal	bled. S	AADC take	s 2^OVI	RSAI	MPLE	numb	er of			-
			samples	s fast as	it can,	and send	the ave	rage	to Dat	a RAI	٧.			

37.11.13 CH[1].LIMIT

Address offset: 0x52C

High/low limits for event monitoring a channel

Bitı	number			31	30	29	28	27	26	25	24	23	22 2	21 2	20 1	L9 1	L8 1	7 1	6 1	5 1	4 1	3 12	2 11	. 10	9	8	7	6	5	4	3	2	1 (
Id				В	В	В	В	В	В	В	В	В	В	В	В	В	В	ВІ	3 4	\ A	Α Δ	. Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	Δ.	A A
Res	et Ox7FI	FF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	L 1	. (0	0	0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW F	ield	Value Id	Va	lue							Des	crip	tio	n																		
Α	RW L	.OW		[-3	276	8 to	o +3	327	67]			Lov	v lev	el l	imi	t																	

37.11.14 CH[2].PSELP

Address offset: 0x530

Input positive pin selection for CH[2]

Bit i	numbe	er		31	30 :	29 2	28 2	7 26	5 25	24	23 2	22 21	. 20	19	18 1	7 1	6 1	5 14	13	12	11 1	0 9	8	7	6	5		3 2 A A		0 A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0 0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						Des	cripti	on																	
Α	RW	PSELP									Ana	log p	osit	ive i	npu	t ch	ann	el												
			NC	0							Not	conn	ect	ed																
			AnalogInput0	1							AIN)																		
			AnalogInput1	2							AIN:	1																		
			AnalogInput2	3							AIN	2																		
			AnalogInput3	4							AIN:	3																		
			AnalogInput4	5							AIN	4																		
			AnalogInput5	6							AINS	5																		
			AnalogInput6	7							AIN	5																		
			AnalogInput7	8							AIN	7																		
			VDD	9							VDD)																		

37.11.15 CH[2].PSELN

Address offset: 0x534

Input negative pin selection for CH[2]

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		АААА
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PSELN		Analog negative input, enables differential channel
	NC	0 Not connected
	AnalogInput0	1 AINO
	AnalogInput1	2 AIN1
	AnalogInput2	3 AIN2
	AnalogInput3	4 AIN3
	AnalogInput4	5 AIN4
	AnalogInput5	6 AIN5
	AnalogInput6	7 AIN6
	AnalogInput7	8 AIN7



Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id			A A A	A A
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
ld RW Field	Value Id	Value	Description	
	VDD	9	VDD	

37.11.16 CH[2].CONFIG

Address offset: 0x538

Input configuration for CH[2]

Bit r	numbe	er		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id					G F E E E D C C C B B A
Res	et 0x0	0020000		0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW	Field	Value Id	Value	Description
Α	RW	RESP			Positive channel resistor control
			Bypass	0	Bypass resistor ladder
			Pulldown	1	Pull-down to GND
			Pullup	2	Pull-up to VDD
			VDD1_2	3	Set input at VDD/2
В	RW	RESN			Negative channel resistor control
			Bypass	0	Bypass resistor ladder
			Pulldown	1	Pull-down to GND
			Pullup	2	Pull-up to VDD
			VDD1_2	3	Set input at VDD/2
С	RW	GAIN			Gain control
			Gain1_6	0	1/6
			Gain1_5	1	1/5
			Gain1_4	2	1/4
			Gain1_3	3	1/3
			Gain1_2	4	1/2
			Gain1	5	1
			Gain2	6	2
			Gain4	7	4
D	RW	REFSEL			Reference control
			Internal	0	Internal reference (0.6 V)
			VDD1_4	1	VDD/4 as reference
E	RW	TACQ			Acquisition time, the time the ADC uses to sample the input
					voltage
			3us	0	3 us
			5us	1	5 us
			10us	2	10 us
			15us	3	15 us
			20us	4	20 us
			40us	5	40 us
F	RW	MODE			Enable differential mode
			SE	0	Single ended, PSELN will be ignored, negative input to ADC
					shorted to GND
			Diff	1	Differential
G	RW	BURST			Enable burst mode
		-	Disabled	0	Burst mode is disabled (normal operation)
			Enabled	1	Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
				•	

37.11.17 CH[2].LIMIT

Address offset: 0x53C

High/low limits for event monitoring a channel



Bit r	number	31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		B B B B B B	B
Res	et 0x7FFF8000	0 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
		Value	Description
Α	RW LOW	[-32768 to +32767]	Low level limit

37.11.18 CH[3].PSELP

Address offset: 0x540

Input positive pin selection for CH[3]

Bit n	umbe	r		31	30	29 :	28 2	27 2	26 2	5 24	1 23	3 22	21 2	20 1	19 1	18 1	7 16	5 15	14	13	12 1	1 10	9	8	7	6	5 4		3 2 A A	1 A	
Rese	t 0x0	0000000		0	0	0	0 (0	0 0	0	0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	escri	ptio	n																	
Α	RW	PSELP									Aı	nalo	g pos	sitiv	⁄e ir	nput	cha	nne	el												
			NC	0							N	ot co	nne	cte	d																
			AnalogInput0	1							ΑI	IN0																			
			AnalogInput1	2							ΑI	IN1																			
			AnalogInput2	3							ΑI	IN2																			
			AnalogInput3	4							ΑI	IN3																			
			AnalogInput4	5							ΑI	IN4																			
			AnalogInput5	6							ΑI	IN5																			
			AnalogInput6	7							ΑI	IN6																			
			AnalogInput7	8							ΑI	IN7																			
			VDD	9							VI	DD																			

37.11.19 CH[3].PSELN

Address offset: 0x544

Input negative pin selection for CH[3]

Bit no	umbe	r		31	30	29 :	28 2	27 2	26 2	25 2	4 2	23 22	21	20	19	18 1	L7 1	L6 1	15 :	14 1	.3 1	.2 1	1 10	9	8	7	6	,		3 2 A A	_	0 A
Rese	t 0x0	0000000		0	0	0	0	0	0 (0 (0	0 0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						0	escr	ipti	on																		
Α	RW	PSELN									A	nalo	g ne	gat	ive	inpı	ut, e	ena	ble	s di	ffer	enti	al cl	nanr	nel							
			NC	0							١	lot c	onn	ecte	ed																	
			AnalogInput0	1							A	AIN0																				
			AnalogInput1	2							A	NIN1																				
			AnalogInput2	3							A	IN2																				
			AnalogInput3	4							A	NIN3																				
			AnalogInput4	5							A	NIN4																				
			AnalogInput5	6							A	AIN5																				
			AnalogInput6	7							A	NIN6																				
			AnalogInput7	8							A	AIN7																				
			VDD	9							١	/DD																				

37.11.20 CH[3].CONFIG

Address offset: 0x548

Input configuration for CH[3]

Bit number		31	1 3	0 2	9 2	8 2	7 2	26 2	25 2	24 :	23 :	22 :	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2)	1 0
Id										G				F		Ε	Ε	Ε				D		С	С	С			В	В		,	4 А
Reset 0x00020000		0	C	0) (0 ()	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id RW Field	Value Id	Va	alu	e						ı	Des	crip	otic	n																			
Δ RW RESP											ons.	itiv	e cł	nan	nel	res	istr	nr c	ont	rol													



Bit number		31 30	29	28 2	7 2	6 25	5 24	23	3 22 2	1 2	0 1	9 1	8 17	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 9	9 8	3 7	6	5	4	3	2	1	0
Id							G				F	E	E	E				1)	(. (. (2		В	В			Α	Α
Reset 0x00020000		0 0	0	0	0	0 0	0	0	0 0) (0 () () 1	() () (0	0	0) () () (0 0	0	0	0	0	0	0	0
Id RW Field	Value Id	Value						De	escript	tio	n																			
	Bypass	0						Ву	/pass r	esi	isto	r la	dder	r																
	Pulldown	1						Pι	ıll-dov	vn '	to G	SNE)																	
	Pullup	2						Pι	ıll-up 1	to ۱	VDD)																		
	VDD1_2	3						Se	t inpu	ıt a	t VI	DD/	2																	
B RW RESN								Ne	egative	e cl	han	nel	resi	stc	r c	ont	rol													
	Bypass	0						Ву	/pass r	esi	isto	r la	dder	r																
	Pulldown	1						Pι	ıll-dov	vn '	to G	SNE)																	
	Pullup	2						Pι	ıll-up 1	to ۱	VDD)																		
	VDD1_2	3						Se	t inpu	ıt a	t VI	DD/	2																	
C RW GAIN								Ga	ain cor	ntr	ol																			
	Gain1_6	0						1/	6																					
	Gain1_5	1						1/	5																					
	Gain1_4	2						1/	4																					
	Gain1_3	3						1/	'3																					
	Gain1_2	4						1/	2																					
	Gain1	5						1																						
	Gain2	6						2																						
	Gain4	7						4																						
D RW REFSEL								Re	eferen	ce	con	tro																		
	Internal	0						In	ternal	re	fere	nce	(0.	6 V	')															
	VDD1_4	1						V	DD/4 a	ıs r	efei	ren	ce																	
E RW TACQ								Ac	quisit	ion	tin	ne,	the	tim	ne t	he	ΑD	C us	es 1	to s	am	ple	the	inp	out					
								VC	ltage																					
	3us	0						3	us																					
	5us	1						5	us																					
	10us	2						10) us																					
	15us	3						15	i us																					
	20us	4						20) us																					
	40us	5						40) us																					
F RW MODE								Er	nable d	diff	ere	ntia	l mo	ode	9															
	SE	0						Siı	ngle e	nde	ed, I	PSE	LN v	vill	be	igr	ore	ed,	neg	ativ	e ir	npu	t to	ΑD	С					
								sh	orted	to	GN	D																		
	Diff	1						Di	fferen	tia	I																			
G RW BURST								Er	nable b	our	st n	nod	e																	
	Disabled	0						Вι	ırst m	ode	e is	disa	ble	d (nor	ma	l op	era	itio	n)										
	Enabled	1						Вι	ırst m	ode	e is	ena	ble	d. 9	SAA	DC	tal	es	2^C	VE	RSA	MF	PLE r	nur	nbei	of				
								sa	mples	as	fas	t as	it c	an,	, an	d s	end	ls tl	ne a	vei	age	e to	Dat	a R	AM					

37.11.21 CH[3].LIMIT

Address offset: 0x54C

High/low limits for event monitoring a channel

Bit r	umber		31	30	29	28	27	26	25	24	23 :	22 2	21 2	20 1	.9 1	L8 1	17 :	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (
Id			В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A
Rese	et 0x7FFF8000		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
ld	RW Field	Value Id	Va	llue							Des	crip	tio	n																			
Id A	RW Field RW LOW	Value Id				0 +	327	67]				crip			t																		

37.11.22 CH[4].PSELP

Address offset: 0x550

Input positive pin selection for CH[4]



Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A
Reset 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
ld RW Field	Value Id	Value	Description
A RW PSELP			Analog positive input channel
	NC	0	Not connected
	AnalogInput0	1	AIN0
	AnalogInput1	2	AIN1
	AnalogInput2	3	AIN2
	AnalogInput3	4	AIN3
	AnalogInput4	5	AIN4
	AnalogInput5	6	AIN5
	AnalogInput6	7	AIN6
	AnalogInput7	8	AIN7
	VDD	9	VDD

37.11.23 CH[4].PSELN

Address offset: 0x554

Input negative pin selection for CH[4]

Bit r	numbe	er		31	30 2	29 :	28 2	7 2	6 2	5 24	23 2	22 2	1 20	19	18	17	16	15	14	13	12 1	1 10	9	8	7	6	,	3 2	1 . A	0
	et 0x0	000000		0	0	0	0 0		0 0	0	0 (0 0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0		0
Id		Field	Value Id		lue						Desc	crip	tion																	
Α	RW	PSELN									Anal	log ı	nega	tiv	e inp	put,	en	able	es d	iffe	ent	al c	hanı	nel						
			NC	0							Not	con	nect	ed																
			AnalogInput0	1							AINC)																		
			AnalogInput1	2							AIN1	1																		
			AnalogInput2	3							AIN2	2																		
			AnalogInput3	4							AIN	3																		
			AnalogInput4	5							AIN4	4																		
			AnalogInput5	6							AINS	5																		
			AnalogInput6	7							AIN	6																		
			AnalogInput7	8							AIN7	7																		
			VDD	9							VDD)																		

37.11.24 CH[4].CONFIG

Address offset: 0x558

Input configuration for CH[4]

Bit	numbe	er		31	30 2	9 :	28 2	7 2	26 2	5 2	24 2	23 22	2 21	20	19	18	17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id										(G			F		Ε	Ε	Ε				D	С	С	С			В	В		Α	Α
Res	et 0x0	0020000		0	0 ()	0 (0	0 () (0	0 0	0	0	0	0	1	0	0	0	0	0 0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						0	Descr	ripti	on																		
Α	RW	RESP									P	ositi	ive (char	nel	res	ist	or c	ont	rol												$\overline{}$
			Bypass	0							Е	3ypas	ss re	esist	or I	add	ler															
			Pulldown	1							P	Pull-d	dow	n to	GN	D																
			Pullup	2							P	Pull-u	ıp to	o VE	D																	
			VDD1_2	3							S	et in	put	at \	/DD	/2																
В	RW	RESN									١	Nega	tive	cha	nne	el re	sis	tor	con	tro												
			Bypass	0							Е	Bypas	ss re	esist	or I	add	ler															
			Pulldown	1							P	Pull-d	wot	n to	GN	D																
			Pullup	2							P	Pull-u	ıp to	o VE	D																	
			VDD1_2	3							S	Set in	put	at \	/DD	/2																
С	RW	GAIN									C	Gain	con	trol																		
			Gain1_6	0							1	L/6																				
			Gain1_5	1							1	L/5																				



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
	Gain1_4	2 1/4
	Gain1_3	3 1/3
	Gain1_2	4 1/2
	Gain1	5 1
	Gain2	6 2
	Gain4	7 4
D RW REFSEL		Reference control
	Internal	0 Internal reference (0.6 V)
	VDD1_4	1 VDD/4 as reference
E RW TACQ		Acquisition time, the time the ADC uses to sample the input
		voltage
	3us	0 3 us
	5us	1 5 us
	10us	2 10 us
	15us	3 15 us
	20us	4 20 us
	40us	5 40 us
F RW MODE		Enable differential mode
	SE	O Single ended, PSELN will be ignored, negative input to ADC
		shorted to GND
	Diff	1 Differential
G RW BURST		Enable burst mode
	Disabled	0 Burst mode is disabled (normal operation)
	Enabled	1 Burst mode is enabled. SAADC takes 2^OVERSAMPLE number of
		samples as fast as it can, and sends the average to Data RAM.

37.11.25 CH[4].LIMIT

Address offset: 0x55C

High/low limits for event monitoring a channel

Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	B B B B B B	B
Reset 0x7FFF8000	0 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW LOW	[-32768 to +32767]	Low level limit
B RW HIGH	[-32768 to +32767]	High level limit

37.11.26 CH[5].PSELP

Address offset: 0x560

Input positive pin selection for CH[5]

Bit number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		ААААА
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW PSELP		Analog positive input channel
NC	0	Not connected
AnalogInput0	1	AIN0
AnalogInput1	2	AIN1
AnalogInput2	3	AIN2
AnalogInput3	4	AIN3
AnalogInput4	5	AIN4
AnalogInput5	6	AIN5



Bit number		31 30 29 28	27 26 25 24 23 22 21 20 19 1	18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id					$A \; A \; A \; A \; A \; A$
Reset 0x00000000		0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	AnalogInput6	7	AIN6		
	AnalogInput7	8	AIN7		
	VDD	9	VDD		

37.11.27 CH[5].PSELN

Address offset: 0x564

Input negative pin selection for CH[5]

Bit	numb	per		31	30 2	9 2	8 27	26	25	24	23 22	2 21	20	19	18	17 :	16	15	14 1	l3 1	2 1:	. 10	9	8	7	6	5	4 3	2	1	0
Id																												A A	A	Α	Α
Res	et 0x	00000000		0	0 () (0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	/ Field	Value Id	Va	lue						Desc	riptio	on																		
Α	RW	/ PSELN									Analo	og ne	egat	ive	inp	ut,	ena	ble	s di	ffer	enti	al ch	anr	nel							
			NC	0							Not o	conn	ecte	ed																	
			AnalogInput0	1							AIN0																				
			AnalogInput1	2							AIN1																				
			AnalogInput2	3							AIN2																				
			AnalogInput3	4							AIN3																				
			AnalogInput4	5							AIN4																				
			AnalogInput5	6							AIN5																				
			AnalogInput6	7							AIN6																				
			AnalogInput7	8							AIN7																				
			VDD	9							VDD																				

37.11.28 CH[5].CONFIG

Address offset: 0x568

Input configuration for CH[5]

Bit number		31 30 29 28 27 26	5 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			G F E E E D C C C B B A A
Reset 0x00020000		0 0 0 0 0 0	0000000010000000000000000000
ld RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
D RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)



Bit	numbe	er		31	30	29 2	28 2	7 2	6 25	5 24	1 23	22 2	21 20	19	18	17	16	15	14 1	13 1	2 13	l 10	9	8	7	6	5 4	1 3	2	1	0
Id										G			F		Ε	Ε	Ε			[)	С	С	С			В	3		Α	Α
Res	et 0x0	00020000		0	0	0	0 0	0 (0 0	0	0	0	0 0	0	0	1	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						Des	scrip	otion																		
			VDD1_4	1							VDI	D/4	as re	fere	ence	е															
Е	RW	TACQ									Acc	quisi	tion	tim	e, tł	ne t	ime	the	AD	C us	es t	o sa	mp	le th	ne ir	npu	t				
											vol	tage	•																		
			3us	0							3 u	S																			
			5us	1							5 u	S																			
			10us	2							10	us																			
			15us	3							15	us																			
			20us	4							20	us																			
			40us	5							40	us																			
F	RW	MODE									Ena	ble	diffe	ren	tial	mo	de														
			SE	0							Sin	gle e	ende	d, P	SEL	N w	ill b	e ig	nor	ed, ı	nega	ative	inp	ut t	o A	DC					
											sho	rtec	d to 0	SND)																
			Diff	1							Diff	fere	ntial																		
G	RW	BURST									Ena	ble	burs	t m	ode																
			Disabled	0							Bur	st m	node	is d	lisal	oled	l (no	orm	al o	oera	tior	1)									
			Enabled	1							Bur	st m	node	is e	enab	led	. SA	AD	C tal	kes :	2^0	VER	SAN	1PLI	Εnι	ımb	er c	f			
											san	nple	s as i	fast	as i	it ca	ın, a	nd	sen	ds th	ne a	vera	ge t	o D	ata	RAI	M.				

37.11.29 CH[5].LIMIT

Address offset: 0x56C

High/low limits for event monitoring a channel

Bit r	numbe	er	31	L 30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0	
Id			В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	В	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	А А	
Res									1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	LOW		[-3	327	68 t	0 +	327	767]			Lov	v le	vel	lim	it																		
D	RW	HIGH							767]				h le																					

37.11.30 CH[6].PSELP

Address offset: 0x570

Input positive pin selection for CH[6]

Bit r	numbe	er		31	30 2	29 2	28 27	7 26	5 25	24	23 22	2 21 2	20 1	19 1	8 17	7 16	15	14	13 1	.2 11	10	9	8	7	6	5 4	J	2 . A	1	
	et 0x0	0000000		0	0	0	0 0	0	0	0	0 0	0	0	0 (0 0	0	0	0	0 (0 0	0	0	0	0	0	0 0			0	
Id	RW	Field	Value Id	Va	lue						Descr	riptio	n																	
Α	RW	PSELP									Analo	g pos	sitiv	ve in	put	cha	nne	l												_
			NC	0							Not c	onne	cte	d																
			AnalogInput0	1							AIN0																			
			AnalogInput1	2							AIN1																			
			AnalogInput2	3							AIN2																			
			AnalogInput3	4							AIN3																			
			AnalogInput4	5							AIN4																			
			AnalogInput5	6							AIN5																			
			AnalogInput6	7							AIN6																			
			AnalogInput7	8							AIN7																			
			VDD	9							VDD																			

37.11.31 CH[6].PSELN

Address offset: 0x574

Input negative pin selection for CH[6]



Bitı	numbe	er		31	30 2	29 2	28 2	7 2	6 25	24	23 2	2 21	20	19 1	18 :	17 :	16 1	15 :	14 1	.3 1	2 11	10	9	8	7	6	5	4 3	3 2	1	0
Id																												A A	A A	Α	Α
Res	et 0x0	0000000		0	0	0	0 0) (0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						Desc	riptio	on																		
Α	RW	PSELN									Anal	og ne	gat	ive i	inp	ut, e	ena	ble	s di	ffere	entia	ıl ch	ann	el							
			NC	0							Not o	conne	ecte	ed																	
			AnalogInput0	1							AIN0																				
			AnalogInput1	2							AIN1																				
			AnalogInput2	3							AIN2																				
			AnalogInput3	4							AIN3																				
			AnalogInput4	5							AIN4																				
			AnalogInput5	6							AIN5																				
			AnalogInput6	7							AIN6																				
			AnalogInput7	8							AIN7																				
			VDD	9							VDD																				

37.11.32 CH[6].CONFIG

Address offset: 0x578

Input configuration for CH[6]

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			G FEEE D CCC BB AA
Reset 0x00020000		0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW RESP			Positive channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
B RW RESN			Negative channel resistor control
	Bypass	0	Bypass resistor ladder
	Pulldown	1	Pull-down to GND
	Pullup	2	Pull-up to VDD
	VDD1_2	3	Set input at VDD/2
C RW GAIN			Gain control
	Gain1_6	0	1/6
	Gain1_5	1	1/5
	Gain1_4	2	1/4
	Gain1_3	3	1/3
	Gain1_2	4	1/2
	Gain1	5	1
	Gain2	6	2
	Gain4	7	4
D RW REFSEL			Reference control
	Internal	0	Internal reference (0.6 V)
	VDD1_4	1	VDD/4 as reference
E RW TACQ			Acquisition time, the time the ADC uses to sample the input
			voltage
	3us	0	3 us
	5us	1	5 us
	10us	2	10 us
	15us	3	15 us
	20us	4	20 us
	40us	5	40 us
F RW MODE			Enable differential mode
	SE	0	Single ended, PSELN will be ignored, negative input to ADC
			shorted to GND
	Diff	1	Differential



Bit	nur	nbe	r		3	1 30	29	9 28	3 27	7 26	25	24	1 23	3 22	21	20	19	18	17	16	15	14	13	12 1	l1 1	0 9	9 1	3 7	7 6	5 5	5 4	3	2	1	0
Id												G				F		Ε	Ε	Ε				D		2 (2 (2		E	3 B	3		Α	Α
Re	set (0x0(0020000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0) () () (0) (0	0	0	0	0
Id	R	w	Field	Value Id	٧	alue	•						D	escr	pti	on																			
G	R	W	BURST		0 0 0 0 0 0 0 0 0 Value											ırst	mo	de																	_
				Disabled												de i	s di	sab	led	(nc	orm	al o	per	atic	n)										
				Enabled	1								Ві	urst	mo	de i	s er	nab	led	. SA	AD	C ta	kes	2^(OVE	RSA	MI	PLE	nur	nbe	er o	f			
													sa	ampl	es a	s fa	ast a	as it	ca	n, a	ınd	sen	ds t	he i	ave	age	e to	Da	ta R	AN	1.				

37.11.33 CH[6].LIMIT

Address offset: 0x57C

High/low limits for event monitoring a channel

Bit r	umbe	er		31	. 30	29	28	27	26	25	24	23 2	22 2:	1 20	0 19	18	17	16	15	14	13	12	11 1	0 9	9	8	7	6	5	4	3	2 1	L 0
Id		В	В	В	В	В	В	В	В	В	ВВ	В	В	В	В	В	Α	Α	Α	Α	Α /	Δ ,	Α.	Α	Α	Α	Α	Α	Α	A 4	АА		
Res	t Ox7	'FFF8000	0	1	1	1	1	1	1	1	1	1 1	. 1	. 1	1	1	1	1	0	0	0	0 () (0	0	0	0	0	0	0) (0	
Id				0 1 1 1 1 1 1 1 1 Value																													
·u	RW	Field	Value Id	Value									cript	ion	1																		
A			Value Id				:o +:	327	67]				cript leve																				

37.11.34 CH[7].PSELP

Address offset: 0x580

Input positive pin selection for CH[7]

Bit r	numb	er		31	30 2	29 2	28 27	7 26	25	24	23 2:	2 21	20	19	18 1	17 1	16 1	15 1	L4 1	3 1	2 11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id																											,	A A	A A	Α	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						Desc	riptio	on																		
Α	RW	PSELP									Anal	og po	siti	ve i	npu	t ch	anı	nel													
			NC	0							Not o	conne	ecte	ed																	
			AnalogInput0	1							AIN0																				
			AnalogInput1	2							AIN1																				
			AnalogInput2	3							AIN2																				
			AnalogInput3	4							AIN3																				
			AnalogInput4	5							AIN4																				
			AnalogInput5	6							AIN5																				
			AnalogInput6	7							AIN6																				
			AnalogInput7	8							AIN7																				
			VDD	9							VDD																				

37.11.35 CH[7].PSELN

Address offset: 0x584

Input negative pin selection for CH[7]

Bit number	31 30 29 28	3 27 26 25 24	4 23 22 21 20	19 18 17	16 15	14 13	12 11 1	0 9	8 7	6	5 4	3 2	2 1 0
Id											Α	A A	A A A
Reset 0x00000000	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0	0 0	0 0	0 0	0 0	0 0	0	0 0	0 0	0 0
Id RW Field Value Id	Value		Description										
A RW PSELN			Analog negat	ive input	, enabl	es diffe	rential (chann	el				
NC	0		Not connecte	ed									
AnalogInp	out0 1		AIN0										
AnalogInp	out1 2		AIN1										
AnalogInp	out2 3		AIN2										
AnalogInp	out3 4		AIN3										
AnalogInp	out4 5		AIN4										
AnalogInp	out5 6		AIN5										



Bit number		31 30 29 28	8 27 26	25 2	4 2	3 22 2	21 20	19	18 1	7 1	6 15	14	13 :	12 1	1 10	9	8	7	6	5 -	4 3	2	1	C
Id																					A A	Α.	Α .	Δ
Reset 0x00000000		0 0 0 0	0 0	0 0	0 0	0	0 0	0	0	0 0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0	D
ld RW Field	Value Id	Value			D	escrip	otion																	
	AnalogInput6	7			Α	IN6																		
	AnalogInput7	8			Α	IN7																		
	VDD	9			٧	DD																		

37.11.36 CH[7].CONFIG

Address offset: 0x588

Input configuration for CH[7]

Bit r	numbe	er		31 30	2	9 2	8 27	7 26	5 25	5 24	23	3 22 2	1 2	20 :	19	18	17	16	15	1	4 1	13	12	11	. 10) 9)	8	7	6	5	4	3	2	1	(
Id										G				F		Ε	Ε	Ε					D		C	. (С			В	В			Α	. /
Res	et 0x0	0020000		0 0	0) (0	0	0	0	0	0 (0	0	0	0	1	0	0	C)	0	0	0	0	C)	0	0	0	0	0	0	0	0	(
ld	RW	Field	Value Id	Value	е						De	escrip	tio	n																						
Α	RW	RESP									Po	sitive	ch	nanı	nel	res	sist	or	con	itro	ol															
			Bypass	0							Ву	pass	res	isto	or la	ado	ler																			
			Pulldown	1							Pι	ıll-dov	wn	to	GN	D																				
			Pullup	2							Pι	ıll-up	to	VDI	D																					
			VDD1_2	3							Se	t inpu	ut a	at V	DD	/2																				
В	RW	RESN									Ne	egativ	e c	har	nne	l re	esis	to	co	nt	rol															
			Bypass	0							Ву	pass	res	isto	or la	ado	ler																			
			Pulldown	1							Pι	ıll-dov	wn	to	GN	D																				
			Pullup	2							Pι	ıll-up	to	VDI	D																					
			VDD1_2	3							Se	t inpu	ut a	at V	DD	/2																				
С	RW	GAIN									Ga	ain co	ntr	ol																						
			Gain1_6	0							1/	6																								
			Gain1_5	1							1/	5																								
			Gain1_4	2							1/	4																								
			Gain1_3	3							1/	3																								
			Gain1_2	4							1/	2																								
			Gain1	5							1																									
			Gain2	6							2																									
			Gain4	7							4																									
D	RW	REFSEL									Re	eferen	ice	100	ntro	ol																				
			Internal	0							In	ternal	l re	fer	enc	e (0.6	V)																		
			VDD1_4	1							V	DD/4 a	as ı	refe	rer	nce	!																			
E	RW	TACQ									Ac	quisit	tio	n tir	ne,	th	e ti	m	e th	ie /	٩D	Cι	ıse	s t	o s	am	ple	th	e iı	npu	t					
											VC	ltage																								
			3us	0							3	us																								
			5us	1							5	us																								
			10us	2							10) us																								
			15us	3							15	us																								
			20us	4							20) us																								
			40us	5							40) us																								
F	RW	MODE									Er	able	dif	fere	nti	al ı	no	de																		
			SE	0							Siı	ngle e	nd	ed,	PS	ELN	١w	ill	be i	ign	or	ed,	, ne	ega	tiv	e ir	าрเ	ıt t	o A	DC						
											sh	orted	to	GN	ID																					
			Diff	1							Di	fferer	ntia	al																						
G	RW	BURST									Er	able l	bui	rst ı	no	de																				
			Disabled	0							Вι	ırst m	od	le is	dis	ab	led	(n	orr	na	0	pei	rat	ion)											
			Enabled	1								ırst m														RSA	M	PLE	nι	ımb	er	of				
																															M.					

37.11.37 CH[7].LIMIT

Address offset: 0x58C



High/low limits for event monitoring a channel

Bit	numb	er		31	L 30	29	28	27	26	25	24	23	22	21 2	20 1	9 1	8 1	7 16	15	14	13	12	11 :	10	9	8 7	7 (5 5	5 4	3	2	1	C
Id				В	В	В	В	В	В	В	В	В	В	В	В	ВЕ	3 E	В	Α	Α	Α	Α	Α	Α	Α	A A	۱ ۸	A A	Δ Δ	A	Α	Α	4
Res	et 0x7	7FFF8000		0	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	. 1	1	0	0	0	0	0	0	0 () (0	0	0	0	0	D
Id	RW	Field	Value Id	Va	alue							De	scri	ptio	n																		
Α	RW	LOW		[-3	3276	58 t	0 +	327	'67]			Lov	v le	vel l	imit	t																	_
									671			Hig																					

37.11.38 RESOLUTION

Address offset: 0x5F0 Resolution configuration

Bitı	numbe	r		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	10	9 8	3 7	7 (5 5	5 4	1 3	2	1	0
Id																																Α	Α .	А
Res	et 0x0(0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () () () (0	0	0	1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	VAL										Set	th	e re	solu	utio	n																	
			8bit	0								8 b	it																					
			10bit	1								10	bit																					
			12bit	2								12	bit																					
			14bit	3								14	bit																					

37.11.39 OVERSAMPLE

Address offset: 0x5F4

Oversampling configuration. OVERSAMPLE should not be combined with SCAN. The RESOLUTION is applied before averaging, thus for high OVERSAMPLE a higher RESOLUTION should be used.

Bit r	iumbe	r		31	. 30	29	28 2	27 2	26 2	5 24	1 23	3 22	21	20	19 1	L8 1	l7 1	6 1	5 1	4 13	12	11 :	10 !	9	8	7	5 5	4	3	2 :	0
Id																													Α	A A	АА
Rese	et 0x0	0000000		0	0	0	0	0 (0 (0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0)	0	0	0	0 (0
Id	RW	Field	Value Id	Va	llue						D	escri	ptio	n																	
Α	RW	OVERSAMPLE									0	vers	amp	le c	ont	rol															
			Bypass	0							В	ypas	s ov	ersa	amp	ling	3														
			Over2x	1							0	vers	amp	le 2	2x																
			Over4x	2							0	vers	amp	le 4	łх																
			Over8x	3							0	vers	amp	le 8	3x																
			Over16x	4							0	vers	amp	le 1	l6x																
			Over32x	5							0	vers	amp	le 3	32x																
			Over64x	6							0	vers	amp	le 6	54x																
			Over128x	7							0	vers	amp	le 1	28>	(
			Over256x	8							0	vers	amp	le 2	256x	(

37.11.40 SAMPLERATE

Address offset: 0x5F8

Controls normal or continuous sample rate

Bit r	iumbe	er		31 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 17	7 16	15	14	13 :	12 1	1 10	9	8	7	6	5	4	3 2	2 1	0
Id																					В	Α	Α	Α	Α	Α	Α	Α	A A	A /	A A
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Value							Des	crip	otio	n																	
Α	RW	CC		[802	047	7]					Cap	tur	e ar	nd c	omį	pare	val	ue.	Sam	ple	rate	is 1	6 M	Hz/	'CC						
В	RW	MODE									Sele	ect i	noc	de f	or s	amp	ole r	ate	con	trol											
			Task	0							Rat	e is	con	itro	lled	froi	m SA	AMF	PLE t	ask											
			Timers	1							Rat	e is	con	itro	lled	froi	m lo	cal	time	er (u	se C	C to	cor	itro	l th	e ra	ite)				



37.11.41 RESULT.PTR

Address offset: 0x62C

Data pointer

Bit r	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 1	17 1	16 1	.5 1	4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2	1 0	
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	Α Α	λ Δ		А	Α	Α	Α	Α	Α	Α	Α	Α	А А	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	PTR										Dat	ар	oin	ter																			

37.11.42 RESULT.MAXCNT

Address offset: 0x630

Maximum number of buffer words to transfer

Id RW Field	Value Id	Value	Description		
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
Id				$A \; A \; A \; A \; A \; A \; A \; A$. A A A A A A A
Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	7 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0

37.11.43 RESULT.AMOUNT

Address offset: 0x634

Number of buffer words transferred since last START

Bit	numbe	er		31	30	29	28 :	27 2	26 2	25 2	24 2	23 2	22 2	1 2	0 1	9 18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	! 1	L C)
Id																				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		\ <i>F</i>	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () ()
Id	RW	Field	Value Id	Va	lue							Des	crip	tio	1																			
Α	R	AMOUNT									١	lun	nbei	of	buf	fer	ıow	ds 1	ran	sfer	rec	sin	ce l	ast	ST	AR	Г. Т	his						7

register can be read after an END or STOPPED event.

37.12 Electrical specification

37.12.1 SAADC Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
DNL	Differential non-linearity, 10-bit resolution	-0.95	<1		LSB
INL	Integral non-linearity, 10-bit resolution		1		LSB
Vos	Differential offset error (calibrated), 10-bit resolution ^a		+-2		LSB
C_{EG}	Gain error temperature coefficient		0.02		%/°C
f _{SAMPLE}	Maximum sampling rate			200	kHz
t _{ACQ,10k}	Acquisition time (configurable), source Resistance <= 10kOhm		3		μs
t _{ACQ,40k}	Acquisition time (configurable), source Resistance <= 40kOhm		5		μs
t _{ACQ,100k}	Acquisition time (configurable), source Resistance <= 100kOhm		10		μs
t _{ACQ,200k}	Acquisition time (configurable), source Resistance <= 200kOhm		15		μs
t _{ACQ,400k}	Acquisition time (configurable), source Resistance <= 400kOhm		20		μs
t _{ACQ,800k}	Acquisition time (configurable), source Resistance <= 800kOhm		40		μs
t _{CONV}	Conversion time		<2		μs
I _{ADC,CONV}	ADC current during ACQuisition and CONVersion		700		μΑ
I _{ADC,IDLE}	Idle current, when not sampling, excluding clock sources and		<5		μΑ
	regulator base currents ³³				

^a Digital output code at zero volt differential input.

When t_{ACQ} is 10us or longer, and if DC/DC is active, it will be allowed to work in refresh mode if no other resource is requiring a high quality power supply from 1V3. If t_{ACQ} is smaller than 10us and DC/DC is active,



Symbol	Description	Min.	Тур.	Max.	Units
E _{G1/6}	Error ^b for Gain = 1/6	-3		3	%
E _{G1/4}	Error ^b for Gain = 1/4	-3		3	%
E _{G1/2}	Error ^b for Gain = 1/2	-3		4	%
E _{G1}	Error ^b for Gain = 1	-3		4	%
C _{SAMPLE}	Sample and hold capacitance at maximum gain ³⁴		2.5		pF
R _{INPUT}	Input resistance		>1		ΜΩ
E _{NOB}	Effective number of bits, differential mode, 12-bit resolution,		9		Bit
	$1/1$ gain, 3 μs acquisition time, crystal HFCLK, 200 ksps				
S _{NDR}	Peak signal to noise and distortion ratio, differential mode, 12-		56		dB
	bit resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200				
	ksps				
S _{FDR}	Spurious free dynamic range, differential mode, 12-bit		70		dBc
	resolution, 1/1 gain, 3 µs acquisition time, crystal HFCLK, 200				
	ksps				
R _{LADDER}	Ladder resistance		160		kΩ

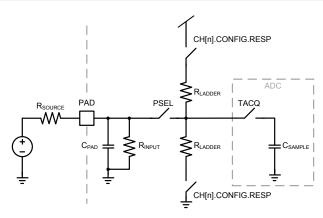


Figure 105: Model of SAADC input (one channel)

Note: SAADC average current calculation for a given application is based on the sample period, conversion and acquisition time (t_{conv} and t_{ACQ}) and conversion and idle current ($t_{ADC,CONV}$). For example, sampling at 4kHz gives a sample period of 250µs. The average current consumption would then be:

$$I_{\mathit{AVERAGE}} = \left(\frac{\left(t_{\mathit{CONV}} + t_{\mathit{ACQ}}\right)}{250}\right) \left(I_{\mathit{ADC},\mathit{CONV}}\right) + \left(\frac{250 - \left(t_{\mathit{CONV}} + t_{\mathit{ACQ}}\right)}{250}\right) \left(I_{\mathit{ADC},\mathit{IDLE}}\right)$$

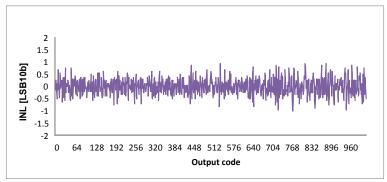


Figure 106: ADC INL vs Output Code

refresh mode will not be allowed, and it will remain in normal mode from the START task to the STOPPED event. So depending on t_{ACQ} and other resources' needs, the appropriate base current needs to be taken into account.

^b Does not include temperature drift

³⁴ Maximum gain corresponds to highest capacitance.



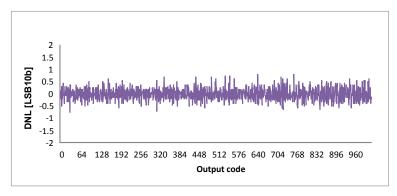


Figure 107: ADC DNL vs Output Code

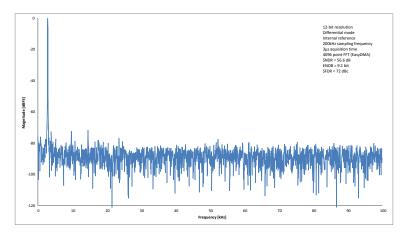


Figure 108: FFT of a 2.8 kHz sine at 200 ksps ()

37.13 Performance factors

Clock jitter, affecting sample timing accuracy, and circuit noise can affect ADC performance.

Jitter can be between START tasks or from START task to acquisition. START timer accuracy and startup times of regulators and references will contribute to variability. Sources of circuit noise may include CPU activity and the DC/DC regulator. Best ADC performance is achieved using START timing based on the TIMER module, HFXO clock source, and Constant Latency mode.



38 COMP — Comparator

The comparator (COMP) compares an input voltage (VIN+) against a second input voltage (VIN-). VIN+ can be derived from an analog input pin (AIN0-AIN7). VIN- can be derived from multiple sources depending on the operation mode of the comparator.

Main features of the comparator are:

- Input range from 0 V to VDD
- Single-ended mode
 - · Fully flexible hysteresis using a 64-level reference ladder
- Differential mode
 - Configurable 50 mV hysteresis
- Reference inputs (VREF):
 - VDD
 - External reference from AIN0 to AIN7 (between 0 V and VDD)
 - Internal references 1.2 V, 1.8 V and 2.4 V
- Three speed/power consumption modes: low-power, normal and high-speed
- Single-pin capacitive sensor support
- Event generation on output changes
 - UP event on VIN- > VIN+
 - DOWN event on VIN- < VIN+
 - · CROSS event on VIN+ and VIN- crossing
 - · READY event on core and internal reference (if used) ready

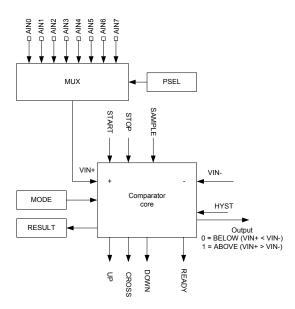


Figure 109: Comparator overview

Once enabled (using the *ENABLE* register), the comparator is started by triggering the START task and stopped by triggering the STOP task. After a start-up time of $t_{COMP,START}$, the comparator will generate a READY event to indicate that it is ready for use and that its output is correct. When the COMP module is started, events will be generated every time VIN+ crosses VIN-.



38 Operation modes

The comparator can be configured to operate in two main operation modes, differential mode and single-ended mode. See the *MODE* register for more information. In both operation modes, the comparator can operate in different speed and power consumption modes (low-power, normal and high-speed). High-speed mode will consume more power compared to low-power mode, and low-power mode will result in slower response time compared to high-speed mode.

Use the *PSEL* register to select any of the AIN0-AIN7 pins as VIN+ input, irregardless of the operation mode selected for the comparator. The source of VIN- depends on which operation mode is used:

- Differential mode: Derived directly from AIN0 to AIN7
- Single-ended mode: Derived from VREF. VREF can be derived from VDD, AIN0-AIN7 or internal 1.2 V, 1.8 V and 2.4 V references.

The selected analog pins will be acquired by the comparator once it is enabled.

An optional hysteresis on VIN+ and VIN- can be enabled when the module is used in differential mode through the *HYST* register. In single-ended mode, VUP and VDOWN thresholds can be set to implement a hysteresis using the reference ladder (see *Figure 112: Comparator in single-ended mode* on page 395). This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 113: Hysteresis example where VIN+ starts below VUP* on page 395 for illustration of the effect of an active hysteresis on a noisy input signal.

An upward crossing will generate an UP event and a downward crossing will generate a DOWN event. The CROSS event will be generated every time there is a crossing, independent of direction.

The immediate value of the comparator can be sampled to *RESULT* register by triggering the SAMPLE task.

38.1 Differential mode

In differential mode, the reference input VIN- is derived directly from one of the AINx pins.

Before enabling the comparator via the *ENABLE* register, the following registers must be configured for the differential mode:

- PSEL
- MODE
- EXTREFSEL

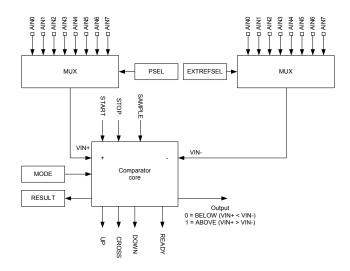


Figure 110: Comparator in differential mode



Restriction: Depending on the device, not all the analog inputs may be available for each MUX. See definitions for *PSEL* and *EXTREFSEL* for more information about which analog pins are available on a particular device.

When *HYST* register is turned on while in this mode, the output of the comparator (and associated events) will change from ABOVE to BELOW whenever VIN+ becomes lower than VIN- - (V_{DIFFHYST} / 2). It will also change from BELOW to ABOVE whenever VIN+ becomes higher than VIN- + (V_{DIFFHYST} / 2). This behavior is illustrated in *Figure 111: Hysteresis enabled in differential mode* on page 394.

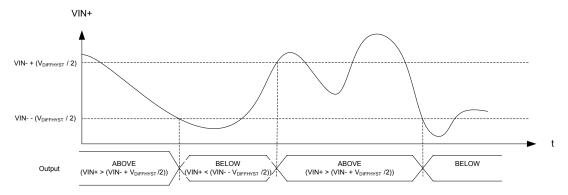


Figure 111: Hysteresis enabled in differential mode

38.2 Single-ended mode

In single-ended mode, VIN- is derived from the reference ladder.

Before enabling the comparator via the *ENABLE* register, the following registers must be configured for the single-ended mode:

- PSEL
- MODE
- REFSEL
- EXTREFSEL
- TH

The reference ladder uses the reference voltage (VREF) to derive two new voltage references, VUP and VDOWN. VUP and VDOWN are configured using THUP and THDOWN respectively in the *TH* register. VREF can be derived from any of the available reference sources, configured using the *EXTREFSEL* and *REFSEL* registers as illustrated in *Figure 112: Comparator in single-ended mode* on page 395. When AREF is selected in the *REFSEL* register, the *EXTREFSEL* register is used to select one of the AIN0-AIN7 analog input pins as reference input. The selected analog pins will be acquired by the comparator once it is enabled.



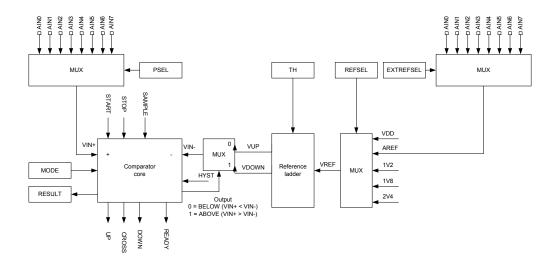


Figure 112: Comparator in single-ended mode

Restriction: Depending on the device, not all the analog inputs may be available for each MUX. See definitions for *PSEL* and *EXTREFSEL* for more information about which analog pins are available on a particular device.

When the comparator core detects that VIN+ > VIN-, i.e. ABOVE as per the *RESULT* register, VIN- will switch to VDOWN. When VIN+ falls below VIN- again, VIN- will be switched back to VUP. By specifying VUP larger than VDOWN, a hysteresis can be generated as illustrated in *Figure 113: Hysteresis example where VIN+ starts below VUP* on page 395 and *Figure 114: Hysteresis example where VIN+ starts above VUP* on page 396.

Writing to HYST has no effect in single-ended mode, and the content of this register is ignored.

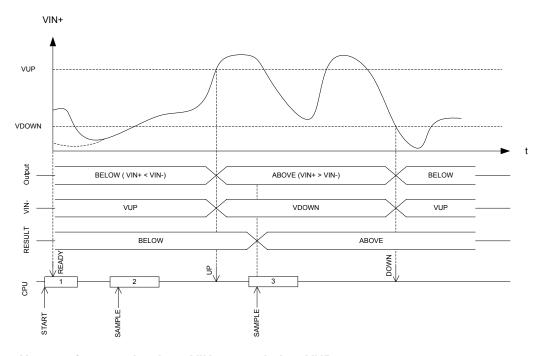


Figure 113: Hysteresis example where VIN+ starts below VUP



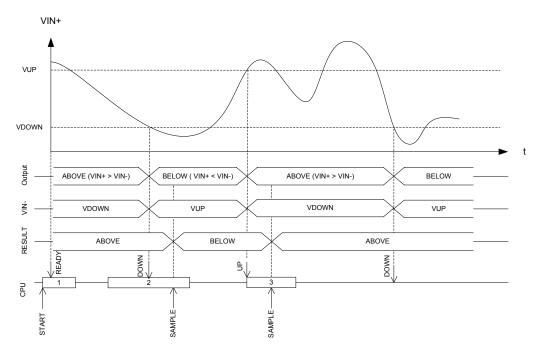


Figure 114: Hysteresis example where VIN+ starts above VUP

38.3 Registers

Table 92: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40013000	COMP	COMP	General purpose comparator		

Table 93: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	COMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	COMP enable
PSEL	0x504	Pin select
REFSEL	0x508	Reference source select for single-ended mode
EXTREFSEL	0x50C	External reference select
TH	0x530	Threshold configuration for hysteresis unit
MODE	0x534	Mode configuration
HYST	0x538	Comparator hysteresis enable
ISOURCE	0x53C	Current source select on analog input

38.3.1 SHORTS

Address offset: 0x200



Shortcut register

Bit	numbe	er		31 30	29	28 2	27 2	6 25	24	23	22	21 2	20	19 1	18 1	17 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6 5	4	3	2	1	0
Id																											Ε	D	С	В	Α
Res	et 0x0	0000000		0 0	0	0	0 (0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0	0	0 0	0	0	0	0	0
Id	RW	Field	Value Id	Value	:					De	scri	iptio	n																		
Α	RW	READY_SAMPLE								Sho	orto	cut b	etv	veer	n RI	EAD	Y e	ven	an	d SA	MF	LE t	ask								
										See	e <i>E</i> V	/ENT	rs_	REA	DΥ	and	TA	SKS	_SA	MPL	.E										
			Disabled	0						Dis	sabl	e sh	ort	cut																	
			Enabled	1						Ena	able	e sho	orto	ut																	
В	RW	READY_STOP								Sho	orto	cut b	etv	veer	n RI	EAD'	Y e	ven	an	d ST	OP	task									
										See	e <i>E</i> V	/ENT	rs_	REA	DΥ	and	TA	SKS	_ST	ОР											
			Disabled	0						Dis	sabl	e sh	ort	cut																	
			Enabled	1						Ena	able	e sho	orto	ut																	
С	RW	DOWN_STOP								Sho	orto	cut b	etv	veer	n D	IWO	N e	ven	t an	d ST	ОР	tasl	(
										See	e <i>E</i> V	/ENT	rs_	DOV	VN	and	TA	SKS	_57	ОР											
			Disabled	0						Dis	sabl	e sh	ort	cut																	
			Enabled	1						Ena	able	e sho	orto	ut																	
D	RW	UP_STOP								Sho	orto	cut b	etv	veer	ı U	P ev	ent	an	d ST	OP 1	tasl	(
										See	e <i>E</i> V	/ENT	rs_	UP a	and	TAS	KS_	ST)P												
			Disabled	0						Dis	sabl	e sh	ort	cut																	
			Enabled	1						Ena	able	e sho	orto	ut																	
Ε	RW	CROSS_STOP								Sho	orto	ut b	etv	veer	n Cl	ROS	S ev	vent	an	d ST	OP	task									
										See	e <i>E</i> V	/ENT	rs	CRO	SS	and	TA.	SKS	ST	OP											
			Disabled	0								e sh	_																		
			Enabled	1						Ena	able	e sho	orto	ut																	

38.3.2 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit r	numbe	er		31	30 29	9 28	27 :	26 2	5 24	23 2	22 2	1 20	19	18 1	17 1	16 1	15 1	4 13	3 12	11 :	10 9	8	7	6	5	4	3 2	1	0
Id																											ОС	В	Α
Res	et Ox0	0000000		0	0 0	0	0	0 0	0	0	0 (0 0	0	0	0 (0 (0 (0	0	0	0 (0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Val	ue					Des	crip	tion																	
Α	RW	READY								Ena	ble (or dis	able	int	terru	upt	for	REA	DY 6	even	t								
										See	EVE	NTS_	REA	DΥ															
			Disabled	0						Disa	ble																		
			Enabled	1						Ena	ble																		
В	RW	DOWN								Ena	ble (or dis	able	int	terrı	upt	for	DO۱	WN (even	it								
										See	EVE	NTS_	DO	WN															
			Disabled	0						Disa	ble																		
			Enabled	1						Ena	ble																		
С	RW	UP								Ena	ble (or dis	able	int	terrı	upt	for	UP (ever	nt									
										See	EVE	NTS_	UP																
			Disabled	0						Disa	ble																		
			Enabled	1						Ena	ble																		
D	RW	CROSS								Ena	ble (or dis	able	int	terrı	upt	for	CRC	SS e	even	t								
										See	EVE	NTS_	CRC	oss															
			Disabled	0						Disa	ble																		
			Enabled	1						Ena	ble																		

38.3.3 INTENSET

Address offset: 0x304



Enable interrupt

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Enable interrupt for READY event
					See EVENTS_READY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	DOWN			Write '1' to Enable interrupt for DOWN event
					See EVENTS_DOWN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	UP			Write '1' to Enable interrupt for UP event
					See EVENTS UP
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	CROSS			Write '1' to Enable interrupt for CROSS event
					See EVENTS_CROSS
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

38.3.4 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW READY			Write '1' to Disable interrupt for READY event
			See EVENTS_READY
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW DOWN			Write '1' to Disable interrupt for DOWN event
			See EVENTS_DOWN
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW UP			Write '1' to Disable interrupt for UP event
			See EVENTS_UP
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW CROSS			Write '1' to Disable interrupt for CROSS event
			See EVENTS_CROSS
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled



38.3.5 RESULT

Address offset: 0x400

Compare result

Bitı	numbe	er		33	1 30	29	28	3 27	7 26	6 25	5 24	1 23	3 22	21	. 20	19	18	17	16	15	14	13	12 1	111	0 9	8	7	6	5	4	3	2	1 0
Id																																	Α
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	V	alue	•						D	esci	ipt	ion																		
Α	R	RESULT										Re	esul	t of	las	t co	mp	are.	De	cisi	on	poiı	ıt S	٩MF	LE 1	task							
			Below	0								In	put	vol	tag	e is	bel	ow	the	thr	esh	old	(VII	V+ <	VIIV	1-)							
			Above	1								In	put	vol	tag	e is	abc	ve	the	thr	esh	old	(VII	V+ >	VII	1-)							

38.3.6 ENABLE

Address offset: 0x500

COMP enable

Bitı	numbe	er		31 30	29	28	27 :	26 2	25 2	24 2	3 2	22 2	1 2	0 19	18	17	16	15	14	13 :	L2 1	11 1	0 9	8	7	6	5	4	3	2	1 0
Id																															А А
Res	et 0x0	0000000		0 0	0	0	0	0	0 (0 (0 (0 (0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value	:					C	eso	crip	tion	ı																	
Α	RW	ENABLE								Е	nak	ble (or d	isab	le 0	ON	1P														
			Disabled	0						C	isa	ble																			
			Enabled	2						Е	nat	ble																			

38.3.7 PSEL

Address offset: 0x504

Pin select

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW PSEL	Analog pin select
AnalogInput0	0 AINO selected as analog input
AnalogInput1	1 AIN1 selected as analog input
AnalogInput2	2 AIN2 selected as analog input
AnalogInput3	3 AIN3 selected as analog input
AnalogInput4	4 AIN4 selected as analog input
AnalogInput5	5 AIN5 selected as analog input
AnalogInput6	6 AIN6 selected as analog input
AnalogInput7	7 AIN7 selected as analog input

38.3.8 REFSEL

Address offset: 0x508

Reference source select for single-ended mode

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 1	0 9	8	7	6	5	4	3	2	1	0
Id																																Α	Α	Α
Res	et 0x0	0000004		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	1	0	0
Id	RW	Field	Value Id	Va	alue							Des	cri	ptio	n																			
Α	RW	REFSEL										Ref	ere	nce	se	lect																		
			Int1V2	0								VRE	F=	int	ern	al 1	.2 ا	V re	efer	enc	e (VD) >=	1.7	V)									
			Int1V8	1								VRE	F=	int	ern	al 1	.8	V re	fer	enc	e (VD) >=	VRI	F +	0.2	V)							
			Int2V4	2								VRE	F=	int	ern	al 2	.4	V re	fer	enc	e (VD) >=	VRI	F +	0.2	V)							
			VDD	4								VRE	F=	· VD	D																			
			ARef	7								VRE	F=	- AR	EF	(VD	D>	-= V	RE	=>=	AF	REFI	MIN)										



38.3.9 EXTREFSEL

Address offset: 0x50C External reference select

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW EXTREFSEL		External analog reference select
	AnalogReference0	0 Use AINO as external analog reference
	AnalogReference1	1 Use AIN1 as external analog reference
	AnalogReference2	2 Use AIN2 as external analog reference
	AnalogReference3	3 Use AIN3 as external analog reference
	AnalogReference4	4 Use AIN4 as external analog reference
	AnalogReference5	5 Use AIN5 as external analog reference
	AnalogReference6	6 Use AIN6 as external analog reference
	AnalogReference7	7 Use AIN7 as external analog reference

38.3.10 TH

Address offset: 0x530

Threshold configuration for hysteresis unit

Bit r	iumbe	er		31 30	29 28	27 26	25 2	24 2	3 22	2 21	20	19	18 1	7 1	5 15	14	13 3	12 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id																	В	В	3 B	В	В			Α	Α	A A	A	A
Res	et OxC	0000000		0 0	0 0	0 0	0 (0 (0 0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value				D	esc	ripti	on																	
Α	RW	THDOWN		[63:0]				٧	/DO\	WN	= (T	HDC	NW	+1),	/64*	'VRE	F											
В	RW	THUP		[63:0]				٧	UP :	= (TI	HUP	+1),	′64*\	√RE	F													

38.3.11 MODE

Address offset: 0x534 Mode configuration

Bit number		31	30 2	29 2	28 2	7 2	5 25	24	23	22 2	21 2) 19	18	17	16	15 1	4 1	3 12	11 :	10 9	8	7	6	5	4 3	2	1	0
Id																					В						Α	Α
Reset 0x00000000		0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0 (0	0	0	0 0	0	0	0	0	0 0	0	0	0
Id RW Field V	alue Id	Val	ue						Des	crip	tion																	
A RW SP									Spe	ed a	and	oow	er r	nod	es													
Lo	ow	0							Lov	v-po	wer	mo	de															
N	lormal	1							noN	mal	l mo	de																
Hi	igh	2							Hig	h-sp	eed	mo	de															
B RW MAIN									Ma	in o	pera	tior	mo	odes														
SE	E	0							Sing	gle-e	ende	d m	ode	9														
D	iff	1							Diff	ere	ntial	mo	de															

38.3.12 HYST

Address offset: 0x538

Comparator hysteresis enable

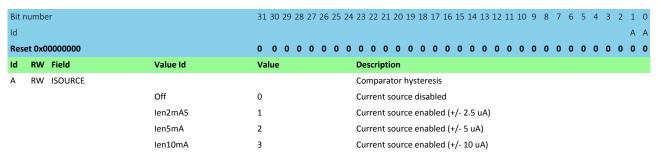
Bit	num	ber	•		31 3	30 2	29 2	8 2	7 2	26 2	5 24	4 2	3 2	2 2:	1 20	19	18	3 17	7 10	5 15	5 1	4 1	3 1	2 1	1 1	0 9	9 8	3 7	' 6	5	4	3	2	1 0
Id																																		Α
Res	et 0	x00	000000		0	0	0	0 (0 (0 0	0) (0	0	0	0	0	0	0	0	0) (0) (0) () (0	0	0	0	0	0	0 0
Id	RV	N	Field	Value Id	Valu	ıe						D	esc	ript	tion																			
Α	RV	Ν	HYST									С	om	par	ato	r hy	ste	resi	s															
				NoHyst	0							С	om	par	ato	r hy	ste	resi	s d	isak	oled	b												
				Hyst50mV	1							С	om	par	ato	r hy	ste	resi	s e	nab	lec	i												



38.3.13 ISOURCE

Address offset: 0x53C

Current source select on analog input



38.4 Electrical specification

38.4.1 COMP Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{COMP,LP}	Core run current in low power mode		2		μΑ
I _{COMP,N}	Core run current in normal mode		5		μΑ
I _{COMP,HS}	Core run current in high-speed mode		10		μΑ
t _{PROPDLY,LP}	Propagation delay, low-power mode ^a		0.6		μS
t _{PROPDLY,N}	Propagation delay, normal mode ^a		0.2		μS
t _{PROPDLY,HS}	Propagation delay, high-speed mode ^a		0.1		μS
V _{DIFFHYST}	Optional hysteresis applied to differential input		30		mV
V _{VDD-VREF}	Required difference between VDD and a selected VREF, VDD >	0.3			V
	VREF				
I _{INT_REF}	Current used by the internal bandgap reference when selected		13		μΑ
	as source for VREF				
t _{INT_REF,START}	Startup time for the internal bandgap reference		50	80	μS
E _{INT_REF}	Internal bandgap reference error	-3		3	%
R _{LADDER}	Reference ladder resistance, I _{LADDER} = VREF / R _{LADDER}		550		kΩ
V _{INPUTOFFSET}	Input offset	-10		10	mV
D _{NLLADDER}	Differential non-linearity of reference ladder		<0.1		LSB
t _{COMP,START}	Startup time for the comparator core		3		μS

Total comparator run current must be calculated from the I_{COMP} , I_{INT_REF} , and I_{LADDER} values for a given reference voltage.

^a Propagation delay is with 10 mV overdrive.



39 LPCOMP — Low power comparator

LPCOMP compares an input voltage against a reference voltage.

Listed here are the main features of LPCOMP:

- 0 VDD input range
- Ultra low power
- Eight input options (AINO to AIN7)
- · Reference voltage options:
 - · Two external analog reference inputs, or
 - 15-level internal reference ladder (VDD/16)
- Optional hysteresis enable on input
- Wakeup source from OFF mode

In System ON, the LPCOMP can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the selected reference. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

Restriction: LPCOMP cannot be used (STARTed) at the same time as COMP. Only one comparator can be used at a time.

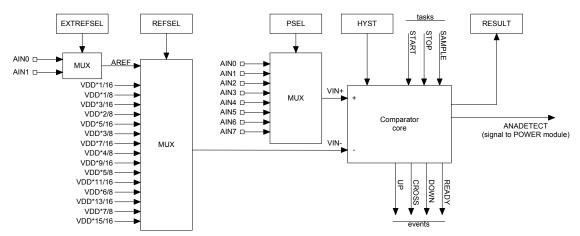


Figure 115: Low power comparator

The wakeup comparator (LPCOMP) compares an input voltage (VIN+), which comes from an analog input pin selected via the PSEL register against a reference voltage (VIN-) selected via the *REFSEL* on page 407 and *EXTREFSEL* registers.

The *PSEL*, *REFSEL*, and *EXTREFSEL* registers must be configured before the LPCOMP is enabled through the *ENABLE* register.

The *HYST* register allows enabling an optional hysteresis in the comparator core. This hysteresis is in the order of magnitude of 50 mV, and shall prevent noise on the signal to create unwanted events. See *Figure 116: Effect of hysteresis on a noisy input signal* on page 403 for illustration of the effect of an active hysteresis on a noisy input signal. It is disabled by default, and shall be configured before enabling LPCOMP as well.

The LPCOMP is started by triggering the START task. After a start-up time of $t_{LPCOMP,STARTUP}$ the LPCOMP will generate a READY event to indicate that the comparator is ready to use and the output of the LPCOMP is correct. The LPCOMP will generate events every time VIN+ crosses VIN-. More specifically, every time VIN+ rises above VIN- (upward crossing) an UP event is generated along with a CROSS event. Every time VIN+ falls below VIN- (downward crossing), a DOWN event is generated along with a CROSS event. When



hysteresis is enabled, the upward crossing level becomes (VIN- + VHYST/2), and the downward crossing level becomes (VIN- - VHYST/2).

The LPCOMP is stopped by triggering the STOP task.

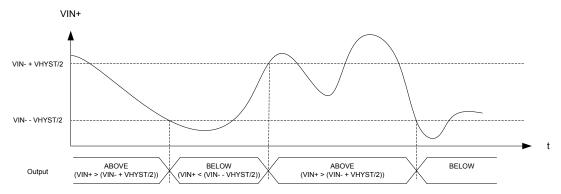


Figure 116: Effect of hysteresis on a noisy input signal

LPCOMP will be operational in both System ON and System OFF mode when it is enabled through the ENABLE register. See *POWER* — *Power supply* on page 78 for more information about power modes. Note that it is not allowed to go to System OFF when a READY event is pending to be generated.

All LPCOMP registers, including *ENABLE*, are classified as retained registers when the LPCOMP is enabled. However, when the device wakes up from System OFF, all LPCOMP registers will be reset.

The LPCOMP can wake up the system from System OFF by asserting the ANADETECT signal. The ANADETECT signal can be derived from any of the event sources that generate the UP, DOWN and CROSS events. In case of wakeup from System OFF, no events will be generated, only the ANADETECT signal. See the ANADETECT register (*ANADETECT* on page 407) for more information on how to configure the ANADETECT signal.

The immediate value of the LPCOMP can be sampled to *RESULT* on page 406 by triggering the SAMPLE task.

See *RESETREAS* on page 85 for more information on how to detect a wakeup from LPCOMP.

39.1 Shared resources

The LPCOMP shares resources with other peripherals.

The LPCOMP shares analog resources with SAADC and COMP. While it is possible to use SAADC at the same time as COMP or LPCOMP, COMP and LPCOMP are mutually exclusive: enabling one will automatically disable the other. In addition, when using SAADC and COMP or LPCOMP simultaneously, it is not possible to select the same analog input pin for both modules.

The LPCOMP peripheral shall not be disabled (by writing to the ENABLE register) before the peripheral has been stopped. Failing to do so may result in unpredictable behaviour.

39.2 Pin configuration

You can use the LPCOMP.PSEL register to select one of the analog input pins, AINO through AIN7, as the analog input pin for the LPCOMP.

See *GPIO* — *General purpose input/output* on page 111 for more information about the pins. Similarly, you can use *EXTREFSEL* on page 407 to select one of the analog reference input pins, AINO and AIN1, as input for AREF in case AREF is selected in *EXTREFSEL* on page 407. The selected analog pins will be acquired by the LPCOMP when it is enabled through *ENABLE* on page 406.



39.3 Registers

Table 94: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40013000	LPCOMP	LPCOMP	Low power comparator	

Table 95: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start comparator
TASKS_STOP	0x004	Stop comparator
TASKS_SAMPLE	0x008	Sample comparator value
EVENTS_READY	0x100	LPCOMP is ready and output is valid
EVENTS_DOWN	0x104	Downward crossing
EVENTS_UP	0x108	Upward crossing
EVENTS_CROSS	0x10C	Downward or upward crossing
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RESULT	0x400	Compare result
ENABLE	0x500	Enable LPCOMP
PSEL	0x504	Input pin select
REFSEL	0x508	Reference select
EXTREFSEL	0x50C	External reference select
ANADETECT	0x520	Analog detect configuration
HYST	0x538	Comparator hysteresis enable

39.3.1 SHORTS

Address offset: 0x200

Shortcut register

Oil	Orto	ut register																															
Bit	numbe	er		31	30	29	28 2	27 2	26 2	25 2	24 :	23 2	2 2	1 20	19	18	17	16	15	14	13	12	11 1	.0 9	9	8	7 (s !	5 4	1 3	2	1	0
Id																													-	D	С	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0	0 (0	0 () (0 (0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						ı	Desc	crip	tion																			
Α	RW	READY_SAMPLE									!	Shor	tcu	t be	twe	en l	REA	DY	eve	nt a	and	SAI	MPL	E ta	sk								
											:	See	EVE	NTS	_RE	AD	Y ar	nd 7	ASI	(S	SAN	1PL	E										
			Disabled	0							- 1	Disa	ble	sho	rtcu	t																	
			Enabled	1							ı	Enak	ole s	shor	tcut	t																	
В	RW	READY_STOP									:	Shor	tcu	t be	twe	en l	REA	DY	eve	nt a	and	STO	OP t	isk									
											:	See	EVE	NTS	_RE	AD	Y ar	nd 7	ASI	(S	STO	P											
			Disabled	0							- 1	Disa	ble	sho	rtcu	t																	
			Enabled	1							- 1	Enak	ole s	shor	tcut	t																	
С	RW	DOWN_STOP									:	Shor	tcu	t be	twe	en l	DO۱	۷N	eve	nt	and	ST	OP t	ask									
											:	See	EVE	NTS	_DC	owi	N ar	nd 7	TASI	KS	STO	P											
			Disabled	0							ı	Disa	ble	sho	rtcu	t																	
			Enabled	1							ı	Enak	ole s	shor	tcut	t																	
D	RW	UP_STOP									:	Shor	tcu	t be	twe	en	UP (eve	nt a	nd	STC	P t	ask										
											:	See	EVE	NTS	_UF	an	d T	4 <i>5K</i>	′S_S	то	P												
			Disabled	0							- 1	Disa	ble	sho	rtcu	t																	
			Enabled	1							- 1	Enak	ole s	shor	tcut	t																	
E	RW	CROSS_STOP										Shor	tcu	t be	twe	en	CRC	SS	eve	nt a	and	STO	OP to	ısk									
											:	See	EVE	NTS	_CR	os:	s an	d 7	ASK	<u>'S_</u> S	то	D											
			Disabled	0							ı	Disa	ble	sho	rtcu	t																	



Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id					E D C B A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		
	Enabled	1	Enable shortcut		

39.3.2 INTENSET

Address offset: 0x304

Enable interrupt

		miorrapi			
Bit	numb	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	READY			Write '1' to Enable interrupt for READY event
					See EVENTS_READY
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
В	RW	DOWN			Write '1' to Enable interrupt for DOWN event
					See EVENTS_DOWN
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
С	RW	UP			Write '1' to Enable interrupt for UP event
					See EVENTS_UP
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	CROSS			Write '1' to Enable interrupt for CROSS event
					See EVENTS_CROSS
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

39.3.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		31	30 2	29 :	28 2	27 2	26 2	5 2	24 2	23 2	22 2	21 2	20 :	19 1	18 :	17 1	16	15 :	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																															D C	В	Α
Res	et OxO	0000000		0	0	0	0	0	0 () (0	0 (0	0 (0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Desc	crip	tio	n																		
Α	RW	READY									١	Writ	e ':	1' tc) Di	isab	le i	nte	rru	pt 1	or	REA	DY 6	ven	t								
											5	See	EV	ENT	'S_I	REA	DΥ																
			Clear	1								Disa	ble	!																			
			Disabled	0							F	Reac	d: C	Disal	ble	d																	
			Enabled	1							F	Reac	d: E	nab	oled	t																	
В	RW	DOWN									١	Writ	e ':	1' tc	D Di	isab	le i	nte	rru	pt 1	for	DOV	VN e	ever	nt								
											5	See	EVI	ENT	'S_I	וסכ	ΝN																
			Clear	1							[Disa	ble	!																			
			Disabled	0							F	Reac	d: C	Disal	ble	d																	
			Enabled	1							F	Reac	d: E	nab	oled	t																	
С	RW	UP									١	Writ	e '	1' tc	D Di	isab	le i	nte	rru	pt 1	or	UP e	ven	t									
											5	See	EV	ENT	'S_1	JР																	



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	
Id RW Field	Value Id	Value	Description
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW CROSS			Write '1' to Disable interrupt for CROSS event
			See EVENTS_CROSS
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

39.3.4 RESULT

Address offset: 0x400

Compare result

Bit n	umbe	er		31	. 30	29	28	27 2	26	25	24	23	22	21	20	19 1	18	17	16	15	14	13	12	11 :	.0	9 8	3 7	7 6	5 5	5 4	3	2	1	0
Id																																		Α
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0
ld	RW	Field	Value Id	Va	llue							Des	scri	ptic	n																			
Α	R	RESULT										Res	sult	of I	ast	con	npa	ire.	De	cisi	on	poi	nt S	ΑM	PLE	tas	k.							
			Bellow	0								Inp	ut v	volt	age	is b	elc	w t	he	ref	ere	nce	thi	esh	old	(VII	۱+۰	< VI	N-).		De	epre	cat	ed
			Below	0								Inp	ut v	volt	age	is b	elc	w t	he	ref	ere	nce	thi	esh	old	(VII	۱+۰	< VI	N-).					
			Above	1								Inp	ut v	volt	age	is a	bo	ve t	he	ref	ere	nce	thi	esh	old	(VII	V+ :	> VI	N-).					

39.3.5 ENABLE

Address offset: 0x500 Enable LPCOMP

Bi	t nı	umbe	r		31	30 2	29 2	28 2	7 2	26 2	5 2	4 2	3 2	2 21	L 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	. 0
Id																																	А	А
R	eset	t 0x0	0000000		0	0	0	0 (0	0 (0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0
Id		RW	Field	Value Id	Val	ıe						D	esc	ript	ion																			
Α		RW	ENABLE									Е	nab	le o	r di	sab	le L	PCC	MC	Р														
				Disabled	0							D	isak	ole																				
				Enabled	1							Ε	nab	le																				

39.3.6 PSEL

Address offset: 0x504

Input pin select

Bit number		31	30 2	29 2	28 2	7 2	6 25	5 24	23	22	21 20) 19	18	17	16 1	15 1	4 1	3 12	2 11	10	9	8 .	7 (5 5	5 4	3	2	1 0
ld Reset 0x00000000		0	0	0	0 0		0 0	0	0	0	0 0	0	0	0	0	0 (0 0	0 0	0	0	0	0 () () (0 (0		A A O O
	Value Id	Va	lue						De	scri	otion																	
A RW PSEL									An	alog	pin :	sele	ct															
,	AnalogInput0	0							AIN	10 s	elect	ed a	s an	alog	g inp	out												
,	AnalogInput1	1							AIN	V1 s	elect	ed a	s an	alog	g inp	out												
,	AnalogInput2	2							AIN	12 s	elect	ed a	s an	alog	g inp	out												
,	AnalogInput3	3							AIN	13 s	elect	ed a	s an	alog	g inp	out												
,	AnalogInput4	4							AIN	14 s	elect	ed a	s an	alog	g inp	out												
,	AnalogInput5	5							AIN	15 s	elect	ed a	s an	alog	g inp	out												
,	AnalogInput6	6							AIN	16 s	elect	ed a	s an	alog	g inp	out												
, and the second se	AnalogInput7	7							AIN	17 s	elect	ed a	s an	alog	g inp	out												



39.3.7 REFSEL

Address offset: 0x508 Reference select

Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			АААА
Reset 0x00000004		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value	Description
A RW REFSEL			Reference select
	Ref1_8Vdd	0	VDD * 1/8 selected as reference
	Ref2_8Vdd	1	VDD * 2/8 selected as reference
	Ref3_8Vdd	2	VDD * 3/8 selected as reference
	Ref4_8Vdd	3	VDD * 4/8 selected as reference
	Ref5_8Vdd	4	VDD * 5/8 selected as reference
	Ref6_8Vdd	5	VDD * 6/8 selected as reference
	Ref7_8Vdd	6	VDD * 7/8 selected as reference
	ARef	7	External analog reference selected
	Ref1_16Vdd	8	VDD * 1/16 selected as reference
	Ref3_16Vdd	9	VDD * 3/16 selected as reference
	Ref5_16Vdd	10	VDD * 5/16 selected as reference
	Ref7_16Vdd	11	VDD * 7/16 selected as reference
	Ref9_16Vdd	12	VDD * 9/16 selected as reference
	Ref11_16Vdd	13	VDD * 11/16 selected as reference
	Ref13_16Vdd	14	VDD * 13/16 selected as reference

39.3.8 EXTREFSEL

Ref15_16Vdd

15

Address offset: 0x50C

External reference select

Bitı	numbe	er		3	1 30	29	28	27	7 26	25	5 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	٧	'alue	•						De	scri	iptio	on																			
Α	RW	EXTREFSEL										Ext	err	nal a	nal	og	refe	erer	ıce	sel	ect													
			AnalogReference0	0								Us	e A	IN0	as e	exte	erna	al ai	nalo	og r	efe	ren	ce											
			AnalogReference1	1								Us	e A	IN1	as e	exte	erna	al ai	nalc	og r	efe	ren	ce											

VDD * 15/16 selected as reference

39.3.9 ANADETECT

Address offset: 0x520

Analog detect configuration

Bitı	numbe	er		31	1 30	29	28 2	27 2	6 2	5 24	4 23	3 22	2 21	20	19	18	17	16	15	14 :	13	12 :	11 1	0 9	9 (3 7	7	6	5	4	3	2	1 0	
Id																																	А А	
Res	et 0x0	0000000		0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () () ()	0	0	0	0	0	0 0	
Id	RW	Field	Value Id	Va	alue						D	esci	ripti	on																				
Α	RW	ANADETECT									Aı	nalo	og de	ete	ct cc	onfi	gur	atic	n															
			Cross	0							G	ene	rate	A٨	IADI	ETE	СТ	on (cros	sin	g, b	oth	upv	var	d cr	oss	ing	an	ıd					
											do	owr	wai	d c	ross	ing																		
			Up	1							G	ene	rate	A٨	IADI	ETE	CT (วท เ	upw	ard	cre	ossi	ng c	nly										
			Down	2							G	ene	rate	A٨	IADI	ETE	СТ	on d	wob	/nw	ard	cro	ssin	g o	nly									

39.3.10 HYST

Address offset: 0x538

Comparator hysteresis enable



Bit	numbe	er		31 30	29	28	27	26	25 2	24 2	23 2	2 2	1 20	19	18	17	16	15	14 1	3 1	2 11	10	9	8	7	6	5	4	3	2	1 0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Value	•						Desc	ript	tion																		
Α	RW	HYST								(Com	par	ator	hys	tere	esis	ena	ble													
			NoHyst	0						(Com	par	ator	hys	tere	esis	disa	able	d												
			Hyst50mV	1						(Com	par	ator	hys	tere	esis	disa	able	ed (t	ур.	50 n	ıV)									

39.4 Electrical specification

39.4.1 LPCOMP Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{LPC}	Run current for low power comparator		0.5		μΑ
t _{LPCANADET}	Time from VIN crossing (>=50mV above threshold) to		5		μs
	ANADETECT signal generated.				
E _{REFLADDER}	Error in reference ladder threshold voltage	-30		30	mV
V _{HYST}	Optional hysteresis		30		mV



40 WDT — Watchdog timer

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up.

The watchdog timer is started by triggering the START task.

The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU. The watchdog is implemented as a down-counter that generates a TIMEOUT event when it wraps over after counting down to 0. When the watchdog timer is started through the START task, the watchdog counter is loaded with the value specified in the CRV register. This counter is also reloaded with the value specified in the CRV register when a reload request is granted.

The watchdog's timeout period is given by:

```
timeout [s] = ( CRV + 1 ) / 32768
```

When started, the watchdog will automatically force the 32.768 kHz RC oscillator on as long as no other 32.768 kHz clock source is running and generating the 32.768 kHz system clock, see chapter *CLOCK*—*Clock control* on page 101.

40.1 Reload criteria

The watchdog has eight separate reload request registers, which shall be used to request the watchdog to reload its counter with the value specified in the CRV register. To reload the watchdog counter, the special value 0x6E524635 needs to be written to all enabled reload registers.

One or more RR registers can be individually enabled through the RREN register.

40.2 Temporarily pausing the watchdog

By default, the watchdog will be active counting down the down-counter while the CPU is sleeping and when it is halted by the debugger. It is however possible to configure the watchdog to automatically pause while the CPU is sleeping as well as when it is halted by the debugger.

40.3 Watchdog reset

A TIMEOUT event will automatically lead to a watchdog reset.

See *Reset* on page 82 for more information about reset sources. If the watchdog is configured to generate an interrupt on the TIMEOUT event, the watchdog reset will be postponed with two 32.768 kHz clock cycles after the TIMEOUT event has been generated. Once the TIMEOUT event has been generated, the impending watchdog reset will always be effectuated.

The watchdog must be configured before it is started. After it is started, the watchdog's configuration registers, which comprise registers CRV, RREN, and CONFIG, will be blocked for further configuration.

The watchdog can be reset from several reset sources, see *Reset behavior* on page 83.

When the device starts running again, after a reset, or waking up from OFF mode, the watchdog configuration registers will be available for configuration again.



40.4 Registers

Table 96: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40010000	WDT	WDT	Watchdog timer	

Table 97: Register Overview

Register	Offset	Description
TASKS_START	0x000	Start the watchdog
EVENTS_TIMEOUT	0x100	Watchdog timeout
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
RUNSTATUS	0x400	Run status
REQSTATUS	0x404	Request status
CRV	0x504	Counter reload value
RREN	0x508	Enable register for reload request registers
CONFIG	0x50C	Configuration register
RR[0]	0x600	Reload request 0
RR[1]	0x604	Reload request 1
RR[2]	0x608	Reload request 2
RR[3]	0x60C	Reload request 3
RR[4]	0x610	Reload request 4
RR[5]	0x614	Reload request 5
RR[6]	0x618	Reload request 6
RR[7]	0x61C	Reload request 7

40.4.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	iumbe	r		31	L 30	29	28	8 2	7 2	26 2	25 2	24	23	22	21	20	19	9 1	8 :	17	16	15	14	13	12	2 1:	1 1) 9	8	7	6	5	4	3	2	1	0
Id																																					Α
Res	et 0x0	0000000		0	0	0	0	0)	0	0	0	0	0	0	0	0) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue								Des	cri	pti	on																					
Α	RW	TIMEOUT										,	Wr	ite	'1'	to I	Ena	abl	ıi e	nte	ru	pt	for	TIN	ΛE	DU.	T ev	/en	:								
												:	See	E١	ÆΝ	ITS_	_TI	IME	0	UT																	
			Set	1									Ena	ble	è																						
			Disabled	0									Rea	ıd:	Dis	abl	ed	I																			
			Enabled	1									Rea	ıd:	Ena	abl	ed																				

40.4.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit	numbe	er		31	L 30	29	2	8 2	7	26	5 2	5	24	23	3 2	2	21	20	1	9 1	18	1	7 :	16	15	5 1	.4	13	1	2 1	1	10	9	8	7	6	5	4	1 3	3	2	1	0
Id																																											Α
Res	et 0x0	0000000		0	0	0	C) (0	0	(0	0	0	(0	0	0	C)	0	0)	0	0	-	0	0	0))	0	0	0	0	0	0	C) ()	0	0	0
Id	RW	Field	Value Id	Va	alue	:								D	esc	riį	oti	on																									
Α	RW	TIMEOUT												W	rit/	e '	1'	to I	Dis	ab	le	in	ite	rrı	ıρ	t f	or	TIP	ИE	0	JT	ev	ent	:									
														Se	ee	ΕV	E٨	TS		IM	EC	οU	T																				
			Clear	1										Di	isa	ble	9																										
			Disabled	0										Re	eac	d: I	Dis	abl	ed	ł																							
			Enabled	1										Re	eac	d: I	Ena	able	ed																								
	NVV	TINESST	Disabled	0 0 0 0 0 0 0 Value									Se Di Re	ee i isal	EV ble	EΛ e Dis	rs_ abl	_T	IM I					, P		Oi	•••	VIL	.0	,			•										



40.4.3 RUNSTATUS

Address offset: 0x400

Run status

Bitı	numbe	r		3:	1 30	29	28	3 27	7 20	6 2	5 24	4 2	3 2	2 2	1 2	0 1	9 1	.8 1	7 1	6 1	5 1	4 13	3 12	2 11	10	9	8	7	6	5	4	3	2	1)
Id																																			Δ
Res	et 0x0	0000000		0	0	0	0	0	0) (0) () (0) () (0 (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	o
Id	RW	Field	Value Id	V	alue	2						D	esc	ript	tior	1																			
Α	R	RUNSTATUS										Ir	ndic	ate	s w	he	the	r or	no	t th	e w	atc	ndo	g is	run	nin	g								
			NotRunning	0								W	Vato	chd	og i	not	rui	nnir	ng																
			Running	1								W	Vato	chd	og i	is r	unn	ing																	

40.4.4 REQSTATUS

Address offset: 0x404

Request status

	umbe	er		31	. 30	29	28 2	27 :	26 2	25 2	24 2	23 2	22 21	1 2	0 19	18	17	' 16	15	14	13	12	11 1	10 9	9 8							1 0
Id																										Н	G	F	Ε	D (C E	3 A
Rese	et 0x0	0000001		0	0	0	0	0	0	0	0 (0	0 0	C	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0 (0 () 1
Id	RW	Field	Value Id	Va	lue						D	Des	cript	ior	١																	
Α	R	RR0									R	Req	uest	sta	itus	for	RR	[0] ı	egi	ste	•											
			DisabledOrRequested	0							R	RR[(0] re	gist	er i	s no	t e	nab	led,	, or	are	alre	ady	rec	lues	sting	rel	oad				
			${\sf EnabledAndUnrequested}$	1							R	RR[(0] re	gist	er i	s en	abl	ed,	and	d ar	e no	t ye	et re	eque	stir	ng re	loa	d				
В	R	RR1									R	Req	uest	sta	itus	for	RR	[1] ı	egi	ste												
			DisabledOrRequested	0							R	RR[:	1] re	gist	er i	s no	t e	nab	led,	, or	are	alre	ady	rec	lues	sting	rel	oad				
			${\sf EnabledAndUnrequested}$	1							R	RR[:	1] re	gist	er i	s en	abl	ed,	and	d ar	e no	t ye	et re	eque	stir	ng re	loa	d				
С	R	RR2									R	Req	uest	sta	itus	for	RR	[2] ı	egi	ste	-											
			DisabledOrRequested	0							R	RR[2	2] re	gist	er i	s no	t ei	nab	led,	, or	are	alre	ady	rec	lues	sting	rel	oad				
			EnabledAndUnrequested	1							R	RR[2	2] re	gist	er i	s en	abl	ed,	and	d ar	e no	t ye	et re	eque	stir	ng re	loa	d				
D	R	RR3									R	Req	uest	sta	itus	for	RR	[3] ı	egi	ste												
			DisabledOrRequested	0							R	RR[3	3] re	gist	er i	s no	t ei	nab	led,	, or	are	alre	ady	rec	lues	sting	rel	oad				
			EnabledAndUnrequested	1							R	RR[3	3] re	gist	er i	s en	abl	ed,	and	d ar	e no	t ye	et re	eque	stir	ng re	loa	d				
E	R	RR4									R	Req	uest	sta	itus	for	RR	[4] ı	egi	ste												
			DisabledOrRequested	0							R	RR[4	4] re	gist	er i	s no	t e	nab	led,	, or	are	alre	ady	rec	lues	sting	rel	oad				
			EnabledAndUnrequested	1							R	RR[4	4] re	gist	er i	s en	abl	ed,	and	d ar	e no	t ye	et re	eque	stir	ng re	loa	d				
F	R	RR5									R	Req	uest	sta	itus	for	RR	[5] ı	egi	ste	-											
			DisabledOrRequested	0							R	RR[5] re	gist	er i	s no	t e	nab	led,	, or	are	alre	ady	rec	lues	sting	rel	oad				
			EnabledAndUnrequested	1							R	RR[5] re	gist	er i	s en	abl	ed,	and	d ar	e no	t ye	et re	eque	stir	ng re	loa	d				
G	R	RR6									R	Req	uest	sta	itus	for	RR	[6] ı	egi	ste												
			DisabledOrRequested	0							R	RR[6	6] re	gist	er i	s no	t ei	nab	led,	, or	are	alre	ady	rec	lues	sting	rel	oad				
			EnabledAndUnrequested	1							R	RR[6	6] re	gist	er i	s en	abl	ed,	and	d ar	e no	t ye	et re	eque	stir	ng re	loa	d				
Н	R	RR7									R	Req	uest	sta	itus	for	RR	[7] ı	egi	ste												
			DisabledOrRequested	0							R	RR[7] re	gist	er i	s no	t ei	nab	led,	, or	are	alre	ady	rec	ues	sting	rel	oad				
			EnabledAndUnrequested	1							R	RR[7] re	gist	er i	s en	abl	ed,	and	d ar	e no	t ye	et re	eque	stir	ng re	loa	d				
												•	- '	-								,				-						

40.4.5 CRV

Address offset: 0x504 Counter reload value

Bit r	numbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				A A A A A A A A A A A A A A A A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value Description
Α	RW	CRV		[0x0000000F0xFFFFFFF Counter reload value in number of cycles of the 32.768 kHz

clock



40.4.6 RREN

Address offset: 0x508

Enable register for reload request registers

Bit r	numbe	er		31	30	29	28 2	27 2	26 2	25 2	4 23	3 2:	2 21	1 20) 19	18	17	16	15	14	13 1	2 1:	1 10	9	8	7	6	5	4 3	2	1	C
Id																										Н	G	F	E 0			
	et 0x0	0000001		0	0	0	0 (0	0 (0 (0 0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0					0 (
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion																		
Α	RW	RRO									Er	nab	le o	r di	sab	le R	R[0] re	gist	er												
			Disabled	0							Di	isak	ole F	RR[()] re	gis	ter															
			Enabled	1							Er	nab	le R	R[0] re	gist	er															
В	RW	RR1									Er	nab	le o	r di	sab	le R	R[1] re	gist	er												
			Disabled	0							Di	isat	ble F	RR[:	1] re	gis	ter															
			Enabled	1							Er	nab	le R	R[1] re	gist	er															
С	RW	RR2									Er	nab	le o	r di	sab	le R	R[2] re	gist	er												
			Disabled	0							Di	isal	ble F	RR[2	2] re	gis	ter															
			Enabled	1							Er	nab	le R	R[2] re	gist	er															
D	RW	RR3									Er	nab	le o	r di	sab	le R	R[3] re	gist	er												
			Disabled	0							Di	isak	ble F	RR[3	3] re	gis	ter															
			Enabled	1							Er	nab	le R	R[3] re	gist	er															
Е	RW	RR4									Er	nab	le o	r di	sab	le R	R[4] re	gist	er												
			Disabled	0							Di	isal	ole F	RR[4	4] re	gis	ter															
			Enabled	1							Er	nab	le R	R[4] re	gist	er															
F	RW	RR5									Er	nab	le o	r di	sab	le R	R[5] re	gist	er												
			Disabled	0							Di	isak	ble F	RR[5] re	gis	ter															
			Enabled	1							Er	nab	le R	R[5] re	gist	er															
G	RW	RR6									Er	nab	le o	r di	sab	le R	R[6] re	gist	er												
			Disabled	0							Di	isat	ole F	RR[6	6] re	gis	ter															
			Enabled	1							Er	nab	le R	R[6] re	gist	er															
Н	RW	RR7									Er	nab	le o	r di	sab	le R	R[7] re	gist	er												
			Disabled	0							Di	isak	ble F	RR[7	7] re	gis	ter															
			Enabled	1							Er	nab	le R	R[7	'] re	gist	er															

40.4.7 CONFIG

Address offset: 0x50C Configuration register

Bit number			31	30 2	9 2	28 2	27 2	6 2	25 2	4 23	3 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																														С		Α
Reset 0x0000	00001		0	0 ()	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	1
Id RW Fi	eld	Value Id	Va	lue						D	escr	ipti	on																			
A RW SL	EEP									C	onfi	gure	e the	e w	atc	hdc	g t	o e	ithe	r b	e p	aus	ed,	or l	kep	t ru	nniı	ng,				
										w	hile	the	CP	U is	sle	epi	ng															
		Pause	0							Pa	ause	wa	tch	dog	wl	nile	the	CF	PU i	s sle	eep	oing										
		Run	1							Ke	eep	the	wat	tcho	gob	rui	nnir	ng v	whi	le tl	he	CPL	J is	slee	pin	g						
C RW H	ALT									C	onfi	gure	e the	e w	atc	hdc	g t	o e	ithe	r b	e p	aus	ed,	or l	kep	t ru	nniı	ng,				
										W	hile	the	CP	U is	ha	lted	l by	th	e d	ebu	gg	er										
		Pause	0							Pa	ause	wa	tch	dog	wl	nile	the	CF	PU i	s ha	alte	ed b	y th	ne d	lebu	ıgge	er					
		Run	1							Ke	еер	the	wat	tcho	gob	rui	nniı	ng v	whi	le tl	he	CPL	J is	halt	ed	by t	the					
										de	ebug	gger	r																			

40.4.8 RR[0]

Address offset: 0x600 Reload request 0



E	3it ni	ımbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18 :	17	16	15	14	13	12 :	11 1	0 9) 8	7	6	5	4	3	2	1	0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	\ A	. 4	A	Α	Α	Α	Α	Α	Α	Α
F	Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0	0	0
ı	d	RW	Field	Value Id	Va	lue							De	scri	ptic	on																			
A	4	W	RR										Re	oac	l re	que	st r	egis	ster																
				Reload	0x	6E5	246	35					Va	lue 1	to r	eau	est	a r	elo	ad d	of tl	ne v	vat	chd	og t	ime	r								

40.4.9 RR[1]

Address offset: 0x604 Reload request 1

Bit	numb	er		31	30	29	28	27	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	1
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0)
Id	RW	Field	Value Id	Va	lue							De	scr	ipti	on																				ı
Α	W	RR										Re	loa	d re	qu	est	regi	iste	r																
			Reload	0x	6E5	246	35					Va	lue	to	rea	ues	taı	relo	ad	of t	the	wa	tch	dos	tin	ner									

40.4.10 RR[2]

Address offset: 0x608 Reload request 2

Bit	numb	er		31	. 30	29	28	3 2	7 2	26	25	24	23	22 :	21	20 1	19 1	l8 1	7 1	5 15	14	13	12	11	10	9	8	7	6	5	4	3 2	! 1	1 0
Id				Α	Α	Α	А		Δ.	Α	Α	Α	Α	Α	Α	Α	Α.	A A	. Δ	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A		A A
Res	et 0x	00000000		0	0	0	0	()	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0 0
Id	RW	Field	Value Id	Va	alue	:							Des	crip	otic	n																		
Α	W	RR											Rel	oad	red	que	st re	egist	er															
			Reload	0x	6E5	524	635	5					Val	ue t	o r	equ	est	a re	loa	d of	the	wa	tcho	log	tim	er								

40.4.11 RR[3]

Address offset: 0x60C Reload request 3

Bitı	numb	er		3	1 3	0 2	9 2	28	27	26	25	5 24	1 23	3 22	21	. 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Δ		Δ	Α	Α	Α	Α	. A	. A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α ,	Δ,	А А
Res	et 0x(0000000		0	O) ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	٧	alu	е							D	esci	ipt	ion																			
Α	W	RR											Re	eloa	d r	equ	est	reg	iste	er															
			Reload	0	x6E	524	463	35					Va	lue	to	rec	ues	t a	relo	oad	of t	the	wa	tch	dog	tin	ner								

40.4.12 RR[4]

Address offset: 0x610 Reload request 4

Bitı	nur	nbe	r		31	L 30	29	28	3 27	7 2	6 2	5 2	24 2	3 2	2 2	1 2	0 19	9 18	3 17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id					Α	Α	Α	Α	A		A 4	۱ ۸	Δ ,	Δ,	Δ ,	A A	A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A А
Res	et (0x0	0000000		0	0	0	0	0) (0) (0 (0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	R	RW	Field	Value Id	Va	alue							C	es	crip	tior	,																		
Α	٧	٧	RR										R	elo	ad	req	uest	re	giste	er															
				Reload	0x	6E5	24	635	5				٧	alu/	e to	re	que	st a	rel	oad	of	the	wa	tch	dog	tim	ner								

40.4.13 RR[5]

Address offset: 0x614 Reload request 5



Bit	numb	er		31	1 30	29	9 2	8 2	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id				Α	Α	. Α		١.	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α
Res	et 0x(00000000		0	0	0	()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Va	alue	е							De	scri	ptic	on																				
Α	W	RR											Rel	oac	l re	que	est r	egis	ster																	_
			Reload	0>	(6E!	524	63	5					Val	ue	to r	equ	uest	ar	elo	ad o	of t	he v	wat	chc	log	tin	ner									

40.4.14 RR[6]

Address offset: 0x618 Reload request 6

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 :	18 1	17 :	16 1	15 1	.4 1	.3 1	.2 1	1 1	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Α.	Α ,	Α ,	Δ,	Δ ,	Δ Α	A	Α	Α	Α	Α	Α	Α	Α	А А
Res	et 0x0	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	scri	otic	n																		
Α	W	RR										Rel	oad	red	que	st r	egis	ter															
			Reload	0x	6E5	246	35					Val	ue t	o r	equ	est	a re	eloa	ad o	f th	ie v	/ato	hdo	og t	me	r							

40.4.15 RR[7]

Address offset: 0x61C Reload request 7

Bitı	numbe	er		31 30 29 2	8 27 26	25 2	24 23	22 21	20 19	18 1	7 16	15	14 1	3 12	11 10	9	8	7	6	5	4	3 2	2 1	0
Id				AAAA	A A A	A	А А	A A	A A	A A	A A	Α	А А	. A	A A	Α	Α	Α	Α	Α	Α	A A	A A	Α
Res	et 0x0	0000000		0 0 0 0	0 0	0	0 0	0 0	0 0	0 0	0	0	0 0	0	0 0	0	0	0	0	0	0	0 (0	0
Id	RW	Field	Value Id	Value			De	cripti	on															
Α	W	RR					Rel	oad re	equest	regist	er													
			Reload	0x6E52463	5		Val	ue to	reques	st a re	load	of t	he w	atcho	dog ti	mer								

40.5 Electrical specification

40.5.1 Watchdog Timer Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{WDT}	Run current for watchdog timer		0.3	2	μΑ
t _{WDT}	Time out interval	458 μs		36 h	



41 SWI — Software interrupts

A set of interrupts have been reserved for use as software interrupts.

41.1 Registers

Table 98: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40014000	SWI	SWI0	Software interrupt 0		
0x40015000	SWI	SWI1	Software interrupt 1		
0x40016000	SWI	SWI2	Software interrupt 2		
0x40017000	SWI	SWI3	Software interrupt 3		
0x40018000	SWI	SWI4	Software interrupt 4		
0x40019000	SWI	SWI5	Software interrupt 5		



42 NFCT — Near field communication tag

The NFCT peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum.

With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

- NFC-A listen mode operation
 - 13.56 MHz input frequency
 - Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- · Programmable frame timing controller
- · Integrated automatic collision resolution, CRC and parity functions

42.1 Overview

The NFC peripheral is an implementation of an NFC Forum compliant listening device NFC-A.

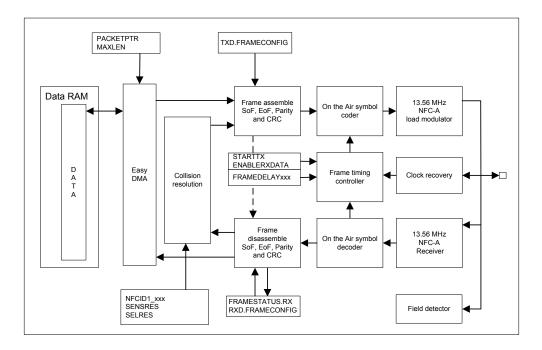


Figure 117: NFC block diagram

The NFC peripheral contains a 13.56 MHz AM receiver and a 13.56 MHz load modulator compatible with the NFC-A technology defined in the NFC Forum with 106 kbps data rate.

The received frames will be automatically disassembled and the data part of the frame transferred to RAM. When transmitting, the frame data will be transferred directly from RAM and transmitted with configurable frame type and delay timing. The system will be notified by an event whenever a complete frame is received or sent.

It also supports the collision detection and resolution ("anticollision") as defined by the NFC Forum.



Wake-on-field is supported in SENSE mode while the device is either in System OFF or System ON mode. When the antenna enters an NFC field, an event will be triggered notifying the system to activate the NFC functionality for incoming frames. In System ON, if the energy detected at the antenna increases beyond a threshold value, the module will generate a FIELDDETECTED event. The module will generate a FIELDLOST event when the quality or strength of the field no longer support NFC communication. Please refer to NFCT Electrical Specification on page 435 for the Low Power Field Detect threshold values.

In system OFF, the NFC Low Power Field Detect function can wake the system up through a reset. The NFC bit in register *RESETREAS* on page 85 will be set as cause of the wake-up.

If the system is put into system OFF mode while a field is already present, the NFC Low Power Field Detect function will wake the system up right away and generate a reset.

Note that as a consequence of reset, NFC is disabled, so the reset handler will have to activate NFC again and set it up properly.

The HFXO must be running before the NFC peripheral goes into ACTIVATED state. Note that the NFC peripheral calibration is automatically done on ACTIVATE task. The HFXO can be turned off when the NFC peripheral goes into SENSE mode. The shortcut FIELDDETECTED_ACTIVATE can be used when the HFXO is already running while in SENSE mode.

Outgoing data will be collected from RAM with the EasyDMA function and assembled according to the TXD.FRAMECONFIG register. Incoming data will be disassembled according to the RXD.FRAMECONFIG register and the data section in the frame will be written to RAM via the EasyDMA function.

The NFC peripheral includes a frame timing controller that can be used to accurately control the inter-frame delay between the incoming frame and a corresponding outgoing frame. It also includes optional CRC functionality.

The NFC peripheral has a set of different states. The module can change state by triggering a task, or when specific operations are finalized. Events and tasks allow software to keep track of and change the current state.

See Figure 117: NFC block diagram on page 416 and Figure 118: NFC state diagram on page 418 for more information.

Notes:

- FIELDLOST event will not be reflected in the state machine (for instance by going back to the DISABLE state), it is up to software to decide on the actions to take when a field lost occurs.
- FIELDLOST event is not generated in SENSE mode.
- FIELDDETECTED event is generated only on the transition from FIELDLOST event to energy detected by the NFC peripheral. So, sending SENSE task while field is still present does not generate FIELDDETECTED event.
- If the FIELDDETECTED event is cleared before sending the ACTIVATE task, then the FIELDDETECTED event shows up again after sending the ACTIVATE task. The shortcut FIELDDETECTED_ACTIVATE can be used to avoid this condition.



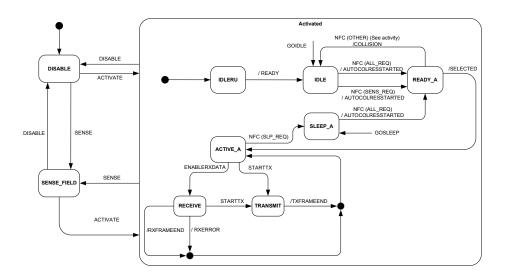


Figure 118: NFC state diagram

42.2 Pin configuration

NFC uses two pins to connect the antenna.

These pins are shared with GPIOs, and the PROTECT field in the NFCPINS register in *UICR* defines the usage of these pins and their protection level against excessive voltages. The content of the NFCPINS register is reloaded at every reset.

When NFCPINS.PROTECT=NFC, a protection circuit will be enabled on the dedicated pins, preventing the chip from being damaged in the presence of a strong NFC field. The GPIO function will be disabled on those pins as well.

When NFCPINS.PROTECT=Disabled, the device will not be protected against strong NFC field damages caught by a connected NFC antenna, and the NFCT peripheral will not operate as expected, as it will never leave the DISABLE state.

The pins dedicated to the NFC antenna function will have some limitation when the pins are configured for normal GPIO operation. The pin capacitance will be higher on those (refer to C_{PAD_NFC} in the *GPIO Electrical Specification* on page 154 below), and some increased leakage current between the two pins is to be expected if they are used in GPIO mode, and are driven to different logical values. To save power the two pins should always be set to the same logical value whenever entering one of the device power saving modes. Please refer to I_{NFC_LEAK} in *GPIO Electrical Specification* on page 154 for details.

42.3 EasyDMA

The NFC peripheral implements EasyDMA for reading and writing of data packets from and to the Data RAM without CPU involvement.

The NFC EasyDMA utilizes one pointer called PACKETPTR for receiving and transmitting packets.

The EasyDMA can either read or write between the NFC peripheral and the RAM, but not at the same time. The event RXFRAMESTART indicates that the EasyDMA has started writing to the RAM for a receive frame and the event RXFRAMEND indicates that the EasyDMA has completed writing to the RAM. Similarly, the event TXFRAMESTART indicates that the EasyDMA has started reading from the RAM for a transmit frame and the event TXFRAMEND indicates that the EasyDMA has completed reading from the RAM. If a transmit and a receive operation is issued at the same time, the transmit operation would be prioritized.

Starting a transmit operation while the EasyDMA has already started writing a receive frame to the RAM will result in unpredictable behavior. Starting an EasyDMA operation whilst there is an ongoing EasyDMA operation may result in unpredictable behavior. It is recommended to wait for the TXFRAMEEND or



RXFRAMEND event for the respective ongoing transmit or receive before starting a new receive or transmit operation.

The MAXLEN register determines the maximum number of bytes that can be read from or written to the RAM. This feature can be used to secure that the NFC peripheral does not overwrite, or read beyond, the RAM assigned to a packet. Note that if the RXD.AMOUNT or TXD.AMOUNT register indicates longer data packets than set in MAXLEN, the frames sent to or received from the physical layer will be incomplete. In RX, the OVERRUN bit in the FRAMESTATUS.RX register will be set and an RXERROR event will be triggered in that situation.

Note that RXD.AMOUNT and TXD.AMOUNT define a frame length in bytes and bits excluding SoF, EoF and parity, but including CRC for RXD.AMOUNT only, make sure to take potential additional bits into account when setting MAXLEN.

Only sending task ENABLERXDATA ensures that a new value in PACKETPTR pointing to the RX buffer in Data RAM is taken into account.

If PACKETPTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See Chapter *Memory* on page 23 for more information about the different memory regions.

The NFC peripherals normally do alternative receive and transmit frames. So, to prepare for the next frame, the PACKETPTR, MAXLEN, TXD.FRAMECONFIG and TXD.AMOUNT can be updated while the receive is in progress, and, similarly, the PACKETPTR, MAXLEN and RXD.FRAMECONFIG can be updated while the transmit is in progress. They can be updated and prepared for the next NFC frame immediately after the STARTED event of the current frame has been received. Updating the TXD.FRAMECONFIG and TXD.AMOUNT during the current transmit frame or updating RXD.FRAMECONFIG during current receive frame may cause unpredictable behaviour.

In accordance with NFC Forum, NFC Digital Protocol Technical Specification, the least a significant bit from the least significant byte is sent on air first. The bytes are stored in increasing order, starting at the lowest address in the EasyDMA buffer in RAM.

42.4 Collision resolution

The NFC peripheral implements an automatic collision resolution function as defined by the NFC Forum.

The SENSRES and SELRES registers need to be programmed upfront in order for the collision resolution to behave correctly. Depending on the NFCIDSIZE field in SENSRES, the following registers also need to be programmed upfront:

- NFCID1 LAST if NFCID1SIZE=NFCID1Single (ID = 4 bytes);
- NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Double (ID = 7 bytes);
- NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST if NFCID1SIZE=NFCID1Triple (ID = 10 bytes);

Table 99: NFCID1 byte allocation (top sent first on air) on page 419 explains the position of the ID bytes in NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST, depending on the ID size, and as compared to the definition used in the NFC Forum, NFC Digital Protocol Technical Specification.

Table 99: NFCID1 byte allocation (top sent first on air)

	ID = 4 bytes	ID = 7 bytes	ID = 10 bytes
NFCID1_Q			nfcid1 ₀
NFCID1_R			nfcid1 ₁
NFCID1_S			nfcid1 ₂
NFCID1_T		nfcid1 ₀	nfcid1 ₃
NFCID1_U		nfcid1 ₁	nfcid1 ₄
NFCID1_V		nfcid1 ₂	nfcid1 ₅
NFCID1_W	nfcid1 ₀	nfcid1 ₃	nfcid1 ₆
NFCID1_X	nfcid1 ₁	nfcid1 ₄	nfcid1 ₇
NFCID1_Y	nfcid1 ₂	nfcid1 ₅	nfcid1 ₈
NFCID1 Z	nfcid13	nfcid1 ₆	nfcid1a

Automatic collision resolution is enabled by default.



The hardware implementation can handle the states from IDLE to ACTIVE_A automatically as defined in the *NFC Forum, NFC Activity Technical Specification*, and the other states are to be handled by software. The software keeps track of the state through events. The collision resolution will trigger an AUTOCOLRESSTARTED event when it has started. Reaching the ACTIVE_A state is indicated by the SELECTED event.

If collision resolution fails, a COLLISION event is triggered. Note that errors occurring during automatic collision resolution may also cause ERROR and/or RXERROR events to be generated. Also, other events may get generated. It is recommended that the software ignores any event except COLLISION, SELECTED and FIELDLOST during automatic collision resolution. Software shall also make sure that any unwanted SHORT or PPI shortcut are disabled during automatic collision resolution.

A pre-defined set of registers, NFC.TAGHEADER0..3, containing a valid NFCID1 value, is available in *FICR*, and can be used by software to populate the NFCID1_3RD_LAST, NFCID1_2ND_LAST and NFCID1_LAST registers. Refer to the release notes of the NFC stack for more details on the format.

The automatic collision resolution will be restarted, if the packets are received with CRC or parity errors while in ACTIVE_A state.

The SLP_REQ is automatically handled by the NFC peripheral. However, this results in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) since the SLP_REQ has no response. This error must be ignored until the SELECTED event is triggered and this error should be cleared by the software when the SELECTED event is triggered.

42.5 Frame timing controller

The NFC peripheral includes a frame timing controller that continuously keeps track of the number of the 13.56 MHz RF-carrier clock periods since the end of the EoF of the last received frame.

The NFC peripheral can be programmed to send a responding frame within a time window or at an exact count of RF carrier periods. In case of FRAMEDELAYMODE = Window a STARTTX task triggered before the frame timing controller counter is equal to FRAMEDELAYMIN will force the transmission to halt until the counter is equal to FRAMEDELAYMIN. If the counter is within FRAMEDELAYMIN and FRAMEDELAYMAX when the STARTTX task is triggered, the peripheral will start the transmission straight away. In case of FRAMEDELAYMODE = ExactVal, a STARTTX task, triggered before the frame delay counter is equal to FRAMEDELAYMAX, will halt the actual transmission start until the counter is equal to FRAMEDELAYMAX.

In case of FRAMEDELAYMODE = WindowGrid, the behaviour is similar to the FRAMEDELAYMODE = Window, but the actual transmission between FRAMEDELAYMIN and FRAMEDELAYMAX starts on a bit grid as defined for NFC-A Listen frames (slot duration of 128 RF carrier periods).

The FRAMEDELAYMIN and FRAMEDELAYMAX values shall only be updated before the STARTTX task is triggered. Failing to do so may cause unpredictable behaviour. An ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS) will be asserted if the frame timing controller counter reaches FRAMEDELAYMAX without any STARTTX task triggered. This may happen even when the response is not required as per *NFC Forum*, *NFC Digital Protocol Technical Specification*. Any commands handled by the automatic collision resolution that don't involve a response being generated may also result in an ERROR event (with FRAMEDELAYTIMEOUT cause in ERRORSTATUS).

The frame timing controller operation is illustrated in *Figure 119: Frame timing controller* (*FRAMEDELAYMODE=Window*) on page 421. The frame timing controller automatically adjusts the frame timing counter based on the last received data bit according to NFC-A technology in the *NFC Forum, NFC Digital Protocol Technical Specification*.



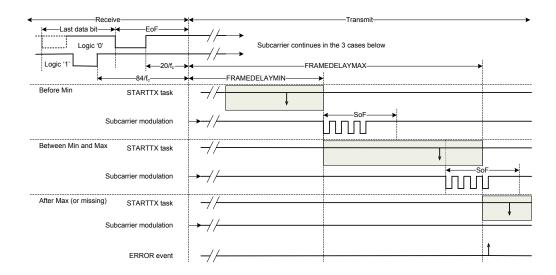


Figure 119: Frame timing controller (FRAMEDELAYMODE=Window)

42.6 Frame assembler

The NFC peripheral implements a frame assembler in hardware.

When the NFC peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For RX, see *Frame disassembler* on page 422. For TX, the software must indicate the address of the source buffer in Data RAM and its size through programming the PACKETPTR and MAXCNT registers respectively, then issuing a TXSTART task.

MAXCNT must be set so that it matches the size of the frame to be sent.

The STARTED event indicates that the PACKETPTR and MAXCNT registers have been captured by the frame assembler's EasyDMA.

When asserting the STARTTX task, the frame assembler module will start reading TXD.AMOUNT.TXDATABYTES bytes (plus one additional byte if TXD.AMOUNT.TXDATABITS > 0) from the RAM position set by the PACKETPTR.

The NFC peripheral transmits the data as read from RAM, adding framing and the CRC calculated on the fly. The NFC peripheral will take (8*TXD.AMOUNT.TXDATABYTES + TXD.AMOUNT.TXDATABITS) bits and assemble a frame according to settings in TXD.FRAMECONFIG. Both short frames, standard frames and bit oriented SDD frames as specified in the NFC Forum, NFC Digital Protocol Technical Specification can be assembled by correct setting of the TXD.FRAMECONFIG register.

The bytes will be transmitted on air in the same order as they are read from RAM with a rising bit order within each byte (least significant bit first). That is, b0 will be transmitted on air before b1, and so on. The bits read from RAM will be coded into symbols as defined in the *NFC Forum*, *NFC Digital Protocol Technical Specification*.

Important: Some NFC Forum documents, such as *NFC Forum, NFC Digital Protocol Technical Specification*, define bit numbering in a byte from b1 (LSB) to b8 (MSB), while most other technical documents from the NFC Forum, and also the Nordic Semiconductor documentation, traditionally numbers them from b0 to b7. The present document uses the b0 to b7 numbering scheme. Be aware of this when comparing with the *NFC Forum, NFC Digital Protocol Technical Specification* to others.

The frame assembler can be configured in TXD.FRAMECONFIG to add Start of Frame (SoF) symbol, calculate and add parity bits, and calculate and add CRC to the data read from RAM when assembling the frame. The total frame will then be longer than what is defined by TXD.AMOUNT.TXDATABYTES and TXDATABITS. DISCARDMODE will select if the first bits in the first byte read from RAM or the last bits in the last byte read from RAM will be discarded if TXD.AMOUNT.TXDATABITS are not equal to zero. Note that if TXD.FRAMECONFIG.PARITY = Parity and TXD.FRAMECONFIG.DISCARDMODE=DiscardStart, a parity bit will be included after the non-complete first byte. No parity will be added after a non-complete last byte.



The Frame Assemble operation is illustrated in *Figure 120: Frame assemble* on page 422 for different settings in TXD.FRAMECONFIG. All shaded bits fields are added by the frame assembler. Some of these bits are optional and appearances are configured in TXD.FRAMECONFIG. Please note that the frames illustrated do not necessarily comply with the NFC specification. The figure is only to illustrate the behavior of the NFC peripheral.

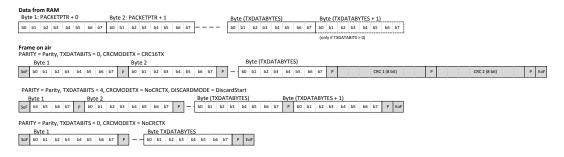


Figure 120: Frame assemble

The accurate timing for transmitting the frame on air is set using the frame timing controller settings.

42.7 Frame disassembler

The NFC peripheral implements a frame disassembler in hardware.

When the NFC peripheral is in the ACTIVE_A state, the software can decide to enter RX or TX mode. For TX, see *Frame assembler* on page 421. For RX, the software must indicate the address of the destination buffer in Data RAM and its size through programming the PACKETPTR and MAXCNT registers respectively, then issuing a ENABLERXDATA task.

The STARTED event indicates that the PACKETPTR and MAXCNT registers have been captured by the frame disassembler's EasyDMA.

When an incoming frame starts, the RXFRAMESTART event will get issued and data will be written to the buffer in Data RAM. The frame disassembler will verify and remove on the fly any parity bits and SoF and End of Frame (EoF) symbols based on RXD.FRAMECONFIG register configuration. It will, however, verify and transfer the CRC bytes into RAM, if the CRC is was enabled through RXD.FRAMECONFIG.

When an EoF symbol is detected, the NFC peripheral will assert the RXFRAMEEND event and write the RXD.AMOUNT register to indicate numbers of received bytes and bits in the data packet. The module does not interpret the content of the data received from the remote NFC device, except for SoF, EoF, parity and CRC checking, as described above. The Frame disassemble operation is illustrated in *Figure 121: Frame disassemble illustration* on page 422.

Per NFC specification, the time between end of frame to the next start of frame can be as short as $86 \mu s$, so care must be taken that PACKETPTR and MAXCNT are ready and ENABLERXDATA is issued on time after the end of previous frame. The use of a PPI shortcut from TXFRAMEEND to ENABLERXDATA is recommended.

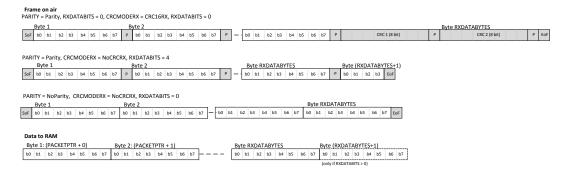


Figure 121: Frame disassemble illustration



42.8 Antenna interface

In ACTIVATED state, an amplitude regulator will adjust the voltage swing on the antenna pins to a value that is within the V_{swinq} limit.

Refer to NFCT Electrical Specification on page 435.

42.9 NFCT antenna recommendations

The NFCT antenna coil must be connected differential between NFC1 and NFC2 pins of the device.

Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz.

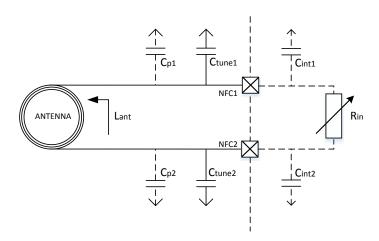


Figure 122: NFCT antenna recommendations

The required tuning capacitor value is given by the below equations:

$$C'_{tune} = \frac{1}{(2\pi \cdot 13.56 \text{ MHz})^2 \cdot L_{ant}} \quad where \ C'_{tune} = \frac{1}{2} \cdot (C_p + C_{int} + C_{tune})$$

$$and \ C_{tune1} = C_{tune2} = C_{tune} \qquad C_{p1} = C_{p2} = C_p \qquad C_{int1} = C_{int2} = C_{int}$$

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56 \text{ MHz})^2 \cdot L_{ant}} - C_p - C_{int}$$

An antenna inductance of $L_{ant} = 2 \mu H$ will give tuning capacitors in the range of 130 pF on each pin. For good performance, match the total capacitance on NFC1 and NFC2.

42.10 Battery protection

If the antenna is exposed to a strong NFC field, current may flow in the opposite direction on the supply due to parasitic diodes and ESD structures.

If the battery used does not tolerate return current, a series diode must be placed between the battery and the device in order to protect the battery.



42.11 References

NFC Forum, NFC Analog Specification version 1.0, www.nfc-forum.org

NFC Forum, NFC Digital Protocol Technical Specification version 1.1, www.nfc-forum.org

NFC Forum, NFC Activity Technical Specification version 1.1, www.nfc-forum.org

42.12 Registers

Table 100: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40005000	NFCT	NFCT	Near Field Communication Tag		

Table 101: Register Overview

Register	Offset	Description
TASKS_ACTIVATE	0x000	Activate NFC peripheral for incoming and outgoing frames, change state to activated
TASKS_DISABLE	0x004	Disable NFC peripheral
TASKS_SENSE	0x008	Enable NFC sense field mode, change state to sense mode
TASKS_STARTTX	0x00C	Start transmission of a outgoing frame, change state to transmit
TASKS_ENABLERXDATA	0x01C	Initializes the EasyDMA for receive.
TASKS_GOIDLE	0x024	Force state machine to IDLE state
TASKS_GOSLEEP	0x028	Force state machine to SLEEP_A state
EVENTS_READY	0x100	The NFC peripheral is ready to receive and send frames
EVENTS_FIELDDETECTED	0 0x104	Remote NFC field detected
EVENTS_FIELDLOST	0x108	Remote NFC field lost
EVENTS_TXFRAMESTART	T 0x10C	Marks the start of the first symbol of a transmitted frame
EVENTS_TXFRAMEEND	0x110	Marks the end of the last transmitted on-air symbol of a frame
EVENTS_RXFRAMESTAR	T 0x114	Marks the end of the first symbol of a received frame
EVENTS_RXFRAMEEND	0x118	Received data have been checked (CRC, parity) and transferred to RAM, and EasyDMA has ended
		accessing the RX buffer
EVENTS_ERROR	0x11C	NFC error reported. The ERRORSTATUS register contains details on the source of the error.
EVENTS_RXERROR	0x128	NFC RX frame error reported. The FRAMESTATUS.RX register contains details on the source of the
		error.
EVENTS_ENDRX	0x12C	RX buffer (as defined by PACKETPTR and MAXLEN) in Data RAM full.
EVENTS_ENDTX	0x130	Transmission of data in RAM has ended, and EasyDMA has ended accessing the TX buffer
EVENTS_AUTOCOLRESST	Г 0x138	Auto collision resolution process has started
EVENTS_COLLISION	0x148	NFC Auto collision resolution error reported.
EVENTS_SELECTED	0x14C	NFC Auto collision resolution successfully completed
EVENTS_STARTED	0x150	EasyDMA is ready to receive or send frames.
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSTATUS	0x404	NFC Error Status register
FRAMESTATUS.RX	0x40C	Result of last incoming frames
CURRENTLOADCTRL	0x430	Current value driven to the NFC Load Control
FIELDPRESENT	0x43C	Indicates the presence or not of a valid field
FRAMEDELAYMIN	0x504	Minimum frame delay
FRAMEDELAYMAX	0x508	Maximum frame delay
FRAMEDELAYMODE	0x50C	Configuration register for the Frame Delay Timer
PACKETPTR	0x510	Packet pointer for TXD and RXD data storage in Data RAM
MAXLEN	0x514	Size of allocated for TXD and RXD data storage buffer in Data RAM
TXD.FRAMECONFIG	0x518	Configuration of outgoing frames
TXD.AMOUNT	0x51C	Size of outgoing frame
RXD.FRAMECONFIG	0x520	Configuration of incoming frames



Register	Offset	Description
RXD.AMOUNT	0x524	Size of last incoming frame
NFCID1_LAST	0x590	Last NFCID1 part (4, 7 or 10 bytes ID)
NFCID1_2ND_LAST	0x594	Second last NFCID1 part (7 or 10 bytes ID)
NFCID1_3RD_LAST	0x598	Third last NFCID1 part (10 bytes ID)
SENSRES	0x5A0	NFC-A SENS_RES auto-response settings
SELRES	0x5A4	NFC-A SEL_RES auto-response settings

42.12.1 SHORTS

Address offset: 0x200

Shortcut register

Bit	numbe	r		31	30 2	29	28 2	27	26 2	25 2	24 2	23 22	21	20	19	18 :	17 :	16 1	15 1	4 1	3 12	2 11	10	9	8	7	6	5 4	4 3	3 2	1	0
Id																															В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	lue						0	escr	iptic	on																		
Α	RW	FIELDDETECTED_ACTIVAT	E								S	hort	cut k	etv	wee	n Fl	IELC	DE.	TEC	TED	eve	ent a	nd .	ACT	IVA	TE	tasl	k				
											S	ee <i>E</i>	VEN	TS_	FIEL	.DD	ETE	СТЕ	D a	ınd	TAS	KS_A	ACTI	VA 1	TE							
			Disabled	0								Disab	le sh	ort	cut																	
			Enabled	1							E	nabl	e sh	orto	cut																	
В	RW	FIELDLOST_SENSE									S	hort	cut b	etv	wee	n Fl	IELC	LO	ST e	ever	t ar	nd SI	NSE	ta	sk							
											S	ee <i>E</i>	VEN	TS_	FIEL	.DL	OST	and	d T /	ASKS	S_SE	NSE										
			Disabled	0							0	Disab	le sh	ort	cut																	
			Enabled	1							Е	nabl	e sh	orto	cut																	

42.12.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	numbe	er		31	30	29	28 2	7 2	26.2	5 24	1 23	3 2	7 2	1 2	0 1	9 1	8 1	7 16	5 15	5 14	1 13	3 12	11	10	9	8	7	6 5	5 4	3	2	1	0
Id											_					S F				N			L		-			G I					Ā
	et 0x0	0000000		0	0	0	0 (0	0 (0	0) (0 0			0 0		0 0	0					0	0			0 (0	
Id	RW	Field	Value Id	Va	lue						D	es	crip	tio	n																		
Α	RW	READY									Er	nal	ble d	or c	lisa	ble	inte	erru	pt f	or F	REA	DY 6	evei	nt									
											Se	ee	EVE	NT.	S_F	REAL	ΟY																
			Disabled	0							D	isa	ble																				
			Enabled	1							Er	nal	ble																				
В	RW	FIELDDETECTED									Eı	nal	ble d	or c	disa	ble	inte	erru	pt f	or F	IEL	.DDE	TEC	CTE) e	/ent							
											Se	ee	EVE	NT.	S_F	IELL	DDE	TEC	TEI	D													
			Disabled	0							D	isa	ble																				
			Enabled	1							Er	nal	ble																				
С	RW	FIELDLOST									Er	nal	ble o	or c	disa	ble	inte	erru	pt f	or F	IEL	.DLC	ST	evei	nt								
											Se	ee	EVE	NT.	S_F	IELL	DLC	ST															
			Disabled	0							D	isa	ble																				
			Enabled	1							Eı	nal	ble																				
D	RW	TXFRAMESTART									Er	nal	ble o	or c	lisa	ble	inte	erru	pt f	or 1	ΓXF	RAN	1ES	TAR	Τeν	vent							
											Se	ee	EVE	NT.	S_1	XFR	ΆN	1EST	AR	Т													
			Disabled	0							D	isa	ble																				
			Enabled	1							Er	nal	ble																				
E	RW	TXFRAMEEND									Er	nal	ble o	or c	disa	ble	inte	erru	pt f	or 1	ΓXF	RAN	1EE	ND 6	eve	nt							
											Se	ee	EVE	NT	'S_1	XFR	ΆN	1EEI	٧D														
			Disabled	0							D	isa	ble																				
			Enabled	1							Eı	nal	ble																				
F	RW	RXFRAMESTART									Er	nal	ble d	or c	disa	ble	inte	erru	pt f	or F	RXF	RAN	1ES	TAR	T e	vent	t						



Bitı	numbe	er		31 30	29 28	27 26	25 24	23 22	21 2	20 19	18	17 1	16 :	15 1	4 1	3 12	11	10	9	8 7	6	5	4	3 2	1	0
Id										T S							L						E			
	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0				0	0						0							
Id		Field	Value Id	Value				Descri																		
								See <i>E</i> \			FRA	MES	STA	RT												
			Disabled	0				Disabl																		
			Enabled	1				Enable	e																	
G	RW	RXFRAMEEND						Enable	e or c	disabl	e in	terr	upt	for	RXI	FRAN	ΛEΕ	ND 6	evei	nt						
								See E	VENT	S_RX	FRA	ME	ENE)												
			Disabled	0				Disabl	le																	
			Enabled	1				Enable	e																	
Н	RW	ERROR						Enable	e or c	disabl	e in	terr	upt	for	ERI	ROR	eve	nt								
								See E	VENT	S_ER	ROF	?														
			Disabled	0				Disabl																		
			Enabled	1				Enable	e																	
K	RW	RXERROR						Enable	e or c	disabl	e in	terr	upt	for	RXI	ERRC)R e	vent	t							
								See E	VENT	S RX	ERR	ROR														
			Disabled	0				Disabl		_																
			Enabled	1				Enable	e																	
L	RW	ENDRX						Enable	e or c	disabl	e in	terr	upt	for	EN	DRX	eve	nt								
								See E	VENT	'S EN	DR)	Υ														
			Disabled	0				Disabl		_																
			Enabled	1				Enable	е																	
М	RW	ENDTX						Enable	e or c	disabl	e in	terr	upt	for	EN	DTX	eve	nt								
								See E	VENT	S_EN	DTX	Υ														
			Disabled	0				Disabl																		
			Enabled	1				Enable	e																	
N	RW	AUTOCOLRESSTARTED						Enable	e or c	disabl	e in	terr	upt	for	ΑU	TOC	OLR	ESS1	AR	TED	eve	nt				
								See E	VENT	S_AU	TO	COLI	RES.	STAI	RTE	D										
			Disabled	0				Disabl																		
			Enabled	1				Enable	e																	
R	RW	COLLISION						Enable	e or c	disabl	e in	terr	upt	for	со	LLISI	ON	ever	nt							
								See E	VENT	s co	LLIS	SION	,													
			Disabled	0				Disabl		_																
			Enabled	1				Enable	e																	
S	RW	SELECTED						Enable	e or c	disabl	e in	terr	upt	for	SEL	ECT	ED 6	even	t							
								See E	VENT	'S SEI	LECT	TED														
			Disabled	0				Disabl		_																
			Enabled	1				Enable	е																	
Т	RW	STARTED						Enable	e or c	disabl	e in	terr	upt	for	STA	ARTE	D e	vent								
								See E\	VENT	S STA	4RT	ED														
			Disabled	0				Disabl																		
			Enabled	1				Enable																		

42.12.3 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		T S R N M L K H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW READY		Write '1' to Enable interrupt for READY event

See EVENTS_READY



Bit r	numbe	er		31 30	29 2	28 27	7 26 2	25 24	23 22 21 20	0 19 1	8 17 1	16 15	14 13	3 12	11 10	0 9	8	7	6 5	5 4	3 :	2 1	0
Id									Т	S F	l		N	М	L K			н	G F	E	D (В	Α
Res	et 0x0	0000000		0 0	0 (0 0	0	0 0	0 0 0 0	0 0	0	0 0	0 0	0	0 0	0	0	0	0 0	0	0 (0	0
Id	RW	Field	Value Id	Value					Description														
			Set	1					Enable														
			Disabled	0					Read: Disab														
-	DIA	FIELD DETECTED	Enabled	1					Read: Enabl					-1.00		T C 0							
В	RW	FIELDDETECTED							Write '1' to See <i>EVENTS</i>				or Fil	ELDL	EIEC	IEL	eve	nt					
			Set	1					Enable														
			Disabled	0					Read: Disab	led													
			Enabled	1					Read: Enabl	ed													
С	RW	FIELDLOST							Write '1' to	Enable	e inter	rupt f	or FIE	ELDL	OST e	ver	nt						
									See EVENTS	_FIELL	DLOST	•											
			Set	1					Enable														
			Disabled	0					Read: Disab														
D	D\A/	TXFRAMESTART	Enabled	1					Read: Enabl		into	runt f	or TV	EDA	NAECT	'A DT	Γονο	nt					
U	KVV	TAFRAIVIESTART							Write '1' to					FKA	IVIEST	AKI	eve	ΠL					
									See EVENTS	_TXFR	AMES	TART											
			Set	1					Enable														
			Disabled Enabled	0					Read: Disab Read: Enable														
E	R\M	TXFRAMEEND	спаріец	1					Write '1' to		into	runt f	or TX	FRΔ	MEEN	ID e	went						
-	11.00	TATRAMELIND											01 17		IVILLI		veni						
									See EVENTS	_TXFR	AME	ND											
			Set	1					Enable	11													
			Disabled Enabled	0					Read: Disab Read: Enable														
F	RW	RXFRAMESTART	Lilabica	_					Write '1' to		e inter	rupt f	or RX	FRA	MEST	AR	Γ eve	nt					
			Set	1					See EVENTS Enable		AIVIES	IANI											
			Disabled	0					Read: Disab	led													
			Enabled	1					Read: Enable														
G	RW	RXFRAMEEND							Write '1' to	Enable	e inter	rupt f	or RX	FRA	MEEN	ND e	event						
									See <i>EVENTS</i>	DVE	ANAEI	ND.											
			Set	1					Enable		AIVILL	IND											
			Disabled	0					Read: Disab	led													
			Enabled	1					Read: Enabl														
Н	RW	ERROR							Write '1' to	Enable	e inter	rupt f	or ER	ROR	even	ıt							
									See <i>EVENTS</i>	FRRC)R												
			Set	1					Enable														
			Disabled	0					Read: Disab	led													
			Enabled	1					Read: Enabl	ed													
K	RW	RXERROR							Write '1' to	Enable	e inter	rupt f	or RX	ERR	OR ev	ent/	:						
									See <i>EVENTS</i>	_RXEF	ROR												
			Set	1					Enable														
			Disabled	0					Read: Disab	led													
			Enabled	1					Read: Enabl	ed													
L	RW	ENDRX							Write '1' to	Enable	e inter	rupt f	or EN	IDRX	ever	nt							
									See EVENTS	_END	RX												
			Set	1					Enable														
			Disabled	0					Read: Disab	led													
			Enabled	1					Read: Enabl	ed													
М	RW	ENDTX							Write '1' to	Enable	inte	rupt f	or EN	IDTX	even	it							
									See EVENTS	_END	ΓX												
			Set	1					Enable														



Bit r	numbe	er		31	30	29 2	8 27	7 26	25	24	23	22 2	1 2	0 19	18	3 17	16	15	14	13 1	12 1	.1 1	0 9	8	7	6	5 -	4 3	2	1	0
Id													Т	S	R				N	1	M I	L F	(Н	G	F	E D	С	В	Α
Res	et 0x0	0000000		0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	lue						Des	scrip	tion	1																	
			Disabled	0							Rea	ad: D	isab	led																	
			Enabled	1							Rea	ad: E	nab	led																	
N	RW	AUTOCOLRESSTARTED									Wr	ite '1	' to	Ena	ble	inte	erru	ıpt f	or A	AUT	occ	DLR	ESST	ART	ED	eve	nt				
											See	e <i>EVE</i>	NTS	AL	JTO	СО	LRE:	SST	4RT	ED											
			Set	1							Ena	able		_																	
			Disabled	0							Rea	ad: D	isab	led																	
			Enabled	1							Rea	ad: E	nab	led																	
R	RW	COLLISION									Wr	ite '1	' to	Ena	ble	inte	erru	pt f	or C	OLI	ISIC	ON (even	t							
											See	e <i>EVE</i>	NTS	s cc	OLLI	ISIO	N														
			Set	1								able																			
			Disabled	0							Rea	ad: D	isab	led																	
			Enabled	1							Rea	ad: E	nab	led																	
S	RW	SELECTED									Wr	ite '1	' to	Ena	ble	inte	erru	ıpt f	or S	ELE	СТЕ	D e	vent								
											Sac	e <i>EVE</i>	NT	S SF	IFC	TFI	,														
			Set	1								able	.141.		LLC	. L L															
			Disabled	0								ad: D	isah	oled																	
			Enabled	1								ad: E																			
Т	RW	STARTED										ite '1			ble	inte	erru	ıpt f	or S	TAF	RTE	D ev	ent								
			C-1	4								e <i>EVE</i>	IN IS	5_51	AR	IED															
			Set	1								able																			
			Disabled	0								ad: D																			
			Enabled	1							Rea	ad: E	nab	led																	

42.12.4 INTENCLR

Address offset: 0x308

Disable interrupt

	number		31 30 29 28 27 26 2	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				TSR NMLK HGFEDCBA
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW READY			Write '1' to Disable interrupt for READY event
				See EVENTS_READY
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW FIELDDETECTED			Write '1' to Disable interrupt for FIELDDETECTED event
				See EVENTS_FIELDDETECTED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW FIELDLOST			Write '1' to Disable interrupt for FIELDLOST event
				See EVENTS_FIELDLOST
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW TXFRAMESTART			Write '1' to Disable interrupt for TXFRAMESTART event
				See EVENTS_TXFRAMESTART
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled



Bit r	numb	er		31	30 2	29 28	3 27	' 26	25 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id										TSR NMLK HGFEDCBA
		0000000				0 0	0	0	0 (0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id		Field	Value Id	Val	ue					Description
Ε	RW	TXFRAMEEND								Write '1' to Disable interrupt for TXFRAMEEND event
										See EVENTS_TXFRAMEEND
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
F	RW	RXFRAMESTART								Write '1' to Disable interrupt for RXFRAMESTART event
										See EVENTS_RXFRAMESTART
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
G	RW	RXFRAMEEND								Write '1' to Disable interrupt for RXFRAMEEND event
										See EVENTS_RXFRAMEEND
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Н	RW	ERROR								Write '1' to Disable interrupt for ERROR event
										See EVENTS_ERROR
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
K	RW	RXERROR								Write '1' to Disable interrupt for RXERROR event
			Clear	1						See EVENTS_RXERROR Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
L	RW	ENDRX	2.102.00	_						Write '1' to Disable interrupt for ENDRX event
			Cl.							See EVENTS_ENDRX
			Clear	1						Disable Read: Disabled
			Disabled Enabled	0						Read: Enabled
М	R\M/	ENDTX	Enabled	1						Write '1' to Disable interrupt for ENDTX event
IVI	11.00	LINDIX								write I to bisable interrupt for ENDTA event
										See EVENTS_ENDTX
			Clear	1						Disable
			Disabled	0						Read: Disabled
N.	D\A/	ALITOCOLDECCTADTED	Enabled	1						Read: Enabled
N	KVV	AUTOCOLRESSTARTED								Write '1' to Disable interrupt for AUTOCOLRESSTARTED event
										See EVENTS_AUTOCOLRESSTARTED
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
R	RW	COLLISION								Write '1' to Disable interrupt for COLLISION event
										See EVENTS_COLLISION
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
S	RW	SELECTED								Write '1' to Disable interrupt for SELECTED event
										See EVENTS_SELECTED
			Clear	1						Disable
			Disabled	0						Read: Disabled
			Enabled	1						Read: Enabled
Т	RW	STARTED								Write '1' to Disable interrupt for STARTED event



Bit number		31 30 29 28 27 26 25	$24\ 23\ 22\ 21\ 20\ 19\ 18\ 17\ 16\ 15\ 14\ 13\ 12\ 11\ 10\ 9\ 8\ 7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$
Id			TSR NMLK HGFEDCBA
Reset 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
			See EVENTS_STARTED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

42.12.5 ERRORSTATUS

Address offset: 0x404 NFC Error Status register

Write a bit to '1' to clear it. Writing '0' has no effect.

Bitı	numbe	r		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 :	19 1	8 1	7 16	5 15	14	13	12	11 1	.0 9	9 (3 7	6	5	4	3	2	1 0
Id																														D	С	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue							Des	scrip	otio	n																	
Α	RW	FRAMEDELAYTIMEOUT										No	STA	RT	ΓX t	ask	trig	gere	d b	efoi	e e	xpir	atio	n of	the	e tim	ie s	et ir	1			
												FR/	AME	DE	LAY	MA	X															
С	RW	NFCFIELDTOOSTRONG										Fiel	ld le	vel	is t	oo l	nigh	at r	nax	loa	d re	sist	ance	9								
D	RW	NFCFIELDTOOWEAK										Fiel	ld le	vel	is t	oo l	ow	at m	nin l	oad	res	ista	nce									

42.12.6 FRAMESTATUS.RX

Address offset: 0x40C

Result of last incoming frames

Write a bit to '1' to clear it. Writing '0' has no effect.

Bitı	numbe	er		31	30	29	28 2	27 :	26 2	5 2	24 2	3 2:	2 21	L 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5 -	4 3	2	1	0
Id																														(В		Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Va	alue						C	esc	ript	ion																			
Α	RW	CRCERROR									١	lo v	alid	Enc	lof	Fra	me	det	ect	ed													
			CRCCorrect	0							١	/alid	CR	C de	etec	ted																	
			CRCError	1							C	RC I	ece	eive	d do	es	not	ma	tch	loc	al c	hec	k										
В	RW	PARITYSTATUS									P	arit	y st	atus	of	rece	eive	d fr	am	e													
			ParityOK	0							F	ram	e re	ecei	ved	wit	h p	arity	y O	K													
			ParityError	1							F	ram	e re	ecei	ved	wit	h p	arity	y er	ror													
С	RW	OVERRUN									C	ver	run	det	ecte	ed																	
			NoOverrun	0							N	10 0	veri	run	dete	ecte	ed																
			Overrun	1							C	ver	run	err	or																		

42.12.7 CURRENTLOADCTRL

Address offset: 0x430

Current value driven to the NFC Load Control

Bitı	numbe	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	L3 1	12 1	1 10	9	8	7	6	5	4	3	2 1	1 0
Id																													Α	Α	Α	A A	A A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																		
	_	CURRENTI OADCTRI										_												ntro									

42.12.8 FIELDPRESENT

Address offset: 0x43C



Indicates the presence or not of a valid field

Bit	numbe	er		31	. 30	29	28	27	26 2	25 2	24 :	23 :	22	21 2	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	0
Id																																	E	ВА
Res	et OxC	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue						- 1	Des	scri	ptio	n																			
Α	R	FIELDPRESENT									ı	Indi	icat	es t	he	pre	sei	nce	or i	not	of a	a va	lid	fiel	d. A	vai	labl	e c	nly	in				
											1	the	act	ivat	ted	sta	te.																	
			NoField	0							ı	No '	vali	id fi	eld	de	tec	ted																
			FieldPresent	1							١	Vali	id fi	ield	de	tec	ted																	
В	R	LOCKDETECT									ı	Indi	icat	es i	f th	ne lo	w	leve	el h	as I	ock	ed 1	to t	he	field	t								
			NotLocked	0							-	Not	t loc	cked	d to	fie	ld																	
			Locked	1							-	Loc	ked	l to	fiel	ld																		

42.12.9 FRAMEDELAYMIN

Address offset: 0x504 Minimum frame delay

В	it nu	mbe	r		31	L 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
lo																					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α.	Δ
R	eset	0x0	0000480		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
Ic		RW	Field	Value Id	Va	alu	•						De	scri	ptic	n																				
Α		RW	FRAMEDELAYMIN										Mi	nim	um	fra	me	del	lav i	in n	um	ber	of	13	.56	МН	lz c	locl	(S							7

42.12.10 FRAMEDELAYMAX

Address offset: 0x508 Maximum frame delay

Bitı	numbe	er		31	30 2	9 2	8 27	26	25 2	24 2	3 2	2 21	1 20	19	18	17 :	L6 1	.5 1	4 13	3 12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id																	,	Δ ,	A A	Α	Α	Α	Α	Α	Α	Α	A A	Δ Δ	A	Α	Α
Res	et 0x0	0001000		0	0 (0	0	0	0	0 (0 (0 0	0	0	0	0	0 (0 (0	1	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Val	ue					C	esc	ript	ion																		
Α	RW	FRAMEDELAYMAX								Ν	Лахі	imu	m fr	rame	e de	lav	in n	uml	oer (of 1	3.56	M	Hz c	locl	(S						_

42.12.11 FRAMEDELAYMODE

Address offset: 0x50C

Configuration register for the Frame Delay Timer

Bit	numb	er		31 3	0 29	9 28	8 27	7 26	25	24	23	22	21 2	20 2	19 1	.8 1	7 1	6 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3	2	1 ()
Id																																A A	4
Re	et 0x0	0000001		0	0 0	0	0	0	0	0	0	0	0	0	0 (0	0 () () (0	0	0	0	0	0	0	0	0	0	0	0	0 1	Ĺ
Id	RW	Field	Value Id	Valu	e						De	scri	ptio	n																			ı
Α	RW	FRAMEDELAYMODE									Со	nfig	urat	ion	reg	iste	er fo	r th	ne F	ran	ne D	ela	/ Tin	ner									
			FreeRun	0							Tra	ansn	nissi	on	is in	de	oen	den	nt o	f fra	me	tim	er a	nd	will	sta	irt v	vhe	en				
											the	e ST.	ART	TX 1	task	is t	rigg	ere	ed.	No t	ime	out											
			Window	1							Fra	ame	is tr	ans	mit	tec	be	twe	en	FRA	ME	DEL	AYN	ΛIN	and	ł							
											FR	AMI	EDEL	.AY	MA	X																	
			ExactVal	2							Fra	ame	is tr	ans	mit	tec	ex	actl	y at	FR	٩M١	DE	IYA_	MA	Χ								
			WindowGrid	3							Fra	ame	is tr	ans	mit	tec	on	a b	it g	rid l	oetv	vee	n FR	AN	1EDE	ELA	ΥM	1IN					
											an	d FR	AM	EDI	ELAY	/M/	AΧ																

42.12.12 PACKETPTR

Address offset: 0x510

Packet pointer for TXD and RXD data storage in Data RAM



Bit number		31	30	29	28	27	26	25	24	23	22 :	21 2	20 1	19 1	L8 1	17 1	16 :	15 1	.4 1	3 1	2 1	1 10	9	8	7	6	5	4	3	2 1	1 0
Id		Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A .	A ,	Α.	Α	Α.	Α ,	A 4	Δ Δ	. A	Α	Α	Α	Α	Α	Α	Α /	4 <i>A</i>	A A
Reset 0x00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0	0	0 (0 (0 0
Id RW Field Va	alue Id	Va	lue							Des	crip	otio	n																		
A RW PTR										Pac	ket	poi	nte	r fo	r T)	XD a	and	l RX	D d	ata	stoi	age	in [Data	R/	M.	Thi	S			

address is a byte aligned RAM address.

42.12.13 MAXLEN

Address offset: 0x514

Size of allocated for TXD and RXD data storage buffer in Data RAM

Bit	number	31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A A
Res	set 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
Α	RW MAXLEN	[0257]	Size of allocated for TXD and RXD data storage buffer in Data
			RAM

42.12.14 TXD.FRAMECONFIG

Address offset: 0x518

Configuration of outgoing frames

Bit r	umbe	r		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					D CBA
Rese	et 0x00	0000017		0 0 0 0 0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value	Description
Α	RW	PARITY			Adding parity or not in the frame
			NoParity	0	Parity is not added in TX frames
			Parity	1	Parity is added TX frames
В	RW	DISCARDMODE			Discarding unused bits in start or at end of a Frame
			DiscardEnd	0	Unused bits is discarded at end of frame
			DiscardStart	1	Unused bits is discarded at start of frame
С	RW	SOF			Adding SoF or not in TX frames
			NoSoF	0	Start of Frame symbol not added
			SoF	1	Start of Frame symbol added
D	RW	CRCMODETX			CRC mode for outgoing frames
			NoCRCTX	0	CRC is not added to the frame
			CRC16TX	1	16 bit CRC added to the frame based on all the data read from
					RAM that is used in the frame

42.12.15 TXD.AMOUNT

Address offset: 0x51C Size of outgoing frame

Bit	numbe	er		31	30	29	28 2	27 2	5 25	24	23	22 2	21 2	20 :	19	18	17 1	16 1	5 1	4 1	3 12	11	10	9	8	7	6	5 4	1 3	2	1	0
Id																						В	В	В	В	В	В	В	3 B	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						Des	crip	ptio	n																		
Α	RW	TXDATABITS		[0.	.7]						Nur	mbe	er o	f bi	ts ii	n th	e la	st c	r fii	rst b	yte	rea	d fro	om	RAN	/I th	at:	shal				
											be i	incl	ude	d ir	n th	e fr	am	e (e	xclu	ıdin	g pa	rity	bit)									
											The	DIS	SCA	RD	МО	DE	fiel	d in	FR	٩ME	со	NFIC	a.TX	sel	ects	if (ınu	sed				
											bits	is c	disc	ard	led	at t	he s	star	t or	at t	he e	end	of a	fra	me.	А١	alu	ie of				
											0 d	ata	byt	es a	and	0 d	lata	bit	is	inva	lid.											
В	RW	TXDATABYTES		[0.	.257	7]					Nur	mbe	er o	f co	omp	let	e by	tes	tha	t sh	all b	e in	clu	ded	in t	he 1	frar	ne,				
											exc	ludi	ing	CRO	C, p	arit	y ar	nd f	am	ing												



42.12.16 RXD.FRAMECONFIG

Address offset: 0x520

Configuration of incoming frames

Bit r	iumbe	er		31	30 2	29 2	28 2	7 2	26 2	5 2	4 2	23 2	22 :	21 2	20 2	19 :	18	17	16	15	14	13	12	11	10	9	8	7	6	5 4	4 3	2	1	0
Id																															2	В		Α
Rese	et 0x0	0000015		0	0	0	0 0	0	0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 0	1	0	1
Id	RW	Field	Value Id	Val	lue							Des	crip	otio	n																			
Α	RW	PARITY									F	Pari	ity e	expe	ecte	ed o	or r	ot	in F	X f	ran	ie												
			NoParity	0							F	Pari	ity i	s no	ot e	хре	ecte	ed i	n R	X fr	am	es												
			Parity	1							F	Pari	ity i	s ex	ре	cte	d ir	RX	fra	me	es.													
В	RW	SOF									S	oF	exp	oect	ted	or	not	in	RX	fra	ne	5												
			NoSoF	0							5	Star	rt o	f Fra	ame	e sy	mt	ool	is n	ot e	exp	ect	ed i	n R	X fr	am	es							
			SoF	1							5	Star	rt o	f Fra	ame	e sy	mt	ool	is e	хре	cte	d ir	R۶	fra	me	S								
С	RW	CRCMODERX									(CRC	mo	ode	for	ind	con	ning	gfra	ame	es													
			NoCRCRX	0							(CRC	is ı	not	exp	oec	ted	in	RX	frai	nes													
			CRC16RX	1							L	.ast	t 16	bit	s in	RX	fra	me	is	CRO	c, c	RC	s c	hec	ked	an	d Cl	RCS	TAT	US				
											ι	pdı	late	d																				

42.12.17 RXD.AMOUNT

Address offset: 0x524

Size of last incoming frame

Bit	numbe	er		33	1 30	29	28	27	26	5 25	24	4 23	3 2	2 2	1 20	0 1	9 18	3 17	7 16	15	14	13	12	11	10	9	8 7	7	6 5	5 4	1 3	2	1	0
Id																								В	В	В	В	3	ВЕ	3 E	3 B	Α	Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	C) (0 0	C	0	0	0	0	0	0	0	0	0	0	0 ()	0 () (0	0	0	0
Id	RW	Field	Value Id	V	alue							D	esc	rip	tion																			
A	R	RXDATABITS										(ir	nclu	udi nes	r of ng C with not	RC n 0	, bu dat	t ex	clu ytes	ding an	g pa	rity	and	d So	F/E	oF 1	fram	ing	g).	t				
В	R	RXDATABYTES													r of Iudir		•		′						frar	ne	(incl	lud	ing (CRC	`,			

42.12.18 NFCID1_LAST

Address offset: 0x590

Last NFCID1 part (4, 7 or 10 bytes ID)

Bit	numbe	er		31	. 30	29	28	3 27	7 26	5 25	5 24	1 23	3 22	21 :	20 1	9 1	8 1	.7 1	.6 1	15 1	.4 1	3 1	2 13	1 10	9	8	7	6	5	4	3 2	2 1	0
Id				D	D	D	D	D	D	D	D	С	С	С	С	C (C (C (С	В	В	ВЕ	3 B	В	В	В	Α	Α	Α	Α	А А	A	A
Res	et 0x0	0006363		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0 (0	0 :	1	1 (0	0	1	1	0	1	1	0	0 0) 1	. 1
Id	RW	Field	Value Id	Va	lue							De	escri	ptio	n																		
Α	RW	NFCID1_Z										NF	CID	1 by	te Z	(ve	ery	last	by	te s	ent)											
В	RW	NFCID1_Y										NF	CID	1 by	te \	,																	
С	RW	NFCID1_X										NF	CID	1 by	te >	(
D	RW	NFCID1 W										NIE	CID	1 hv	t۵۱	۸/																	

42.12.19 NFCID1_2ND_LAST

Address offset: 0x594

Second last NFCID1 part (7 or 10 bytes ID)



Bit r	umbe	r		31 30	29	28	27	26	25	24	23	22 2	21 2	0 19	18	17	16	15	14	13 1	2 11	10	9	8	7	6	5	4 3	3 2	1	0
Id											С	С	c c	: c	С	С	С	В	В	ВЕ	В	В	В	В.	Д	A	Α	A A	A A	Α	Α
Res	t 0x0	0000000		0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Value	•						Des	crip	tior	1																	
Α	RW	NFCID1_V									NFC	CID1	byt	e V																	_
В	RW	NFCID1_U									NFC	CID1	byt	e U																	
С	RW	NFCID1_T									NFC	CID1	byt	e T																	

42.12.20 NFCID1_3RD_LAST

Address offset: 0x598

Third last NFCID1 part (10 bytes ID)

Bit r	umbe	er		3	1 30	29	28	8 2	7 26	5 25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	1 1	0 9	8	7	6	5	4	3	2 :	1 0
Id												С	С	С	С	С	С	С	С	В	В	В	В	3 E	3 E	В	Α	Α	Α	Α	A	Δ ,	A A
Res	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	٧	alue	е						De	scr	ipti	on																		
Α	RW	NFCID1_S										NF	CID	1 b	yte	S																	
В	RW	NFCID1_R										NF	CID	1 b	yte	R																	
С	RW	NFCID1_Q										NF	CID	1 b	yte	Q																	

42.12.21 SENSRES

Address offset: 0x5A0

NFC-A SENS_RES auto-response settings

Bit	number		31 30 29 28 27 26 25 24	1 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				EEEEDDDDCCBAAAA
Res	et 0x00000001		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW BITFRAMESDD			Bit frame SDD as defined by the b5:b1 of byte 1 in SENS_RES
				response in the NFC Forum, NFC Digital Protocol Technical
				Specification
	9	SDD00000	0	SDD pattern 00000
	9	SDD00001	1	SDD pattern 00001
	9	SDD00010	2	SDD pattern 00010
	9	SDD00100	4	SDD pattern 00100
	9	SDD01000	8	SDD pattern 01000
	9	SDD10000	16	SDD pattern 10000
В	RW RFU5			Reserved for future use. Shall be 0.
С	RW NFCIDSIZE			NFCID1 size. This value is used by the Auto collision resolution
				engine.
	I	NFCID1Single	0	NFCID1 size: single (4 bytes)
	ı	NFCID1Double	1	NFCID1 size: double (7 bytes)
	ı	NFCID1Triple	2	NFCID1 size: triple (10 bytes)
D	RW PLATFCONFIG			Tag platform configuration as defined by the b4:b1 of byte 2
				in SENS_RES response in the NFC Forum, NFC Digital Protocol
				Technical Specification
Ε	RW RFU74			Reserved for future use. Shall be 0.

42.12.22 SELRES

Address offset: 0x5A4

NFC-A SEL_RES auto-response settings



Bit	numbe	er		31	30 2	9 :	28 2	27 2	26 2	5 2	4 2	3 22	21	20	19 1	18 1	7 1	5 15	14	13	12	11 1	0 9	8	7	6	5	4	3 2	1	. 0
Id																									Ε	D	D	С	C E	β Δ	A A
Res	et 0x0	0000000		0	0	0	0	0	0 (0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	on																	
Α	RW	RFU10									Re	eser	ved	for	futu	ıre ι	ıse.	Sha	ll be	0.											
В	RW	CASCADE									C	asca	de b	oit (d	cont	roll	ed b	y ha	ardv	vare	e, wi	ite l	nas i	no e	ffe	t)					
			Complete	0							N	FCID)1 co	omp	lete	9															
			NotComplete	1							N	FCID)1 n	ot c	omp	olete	9														
С	RW	RFU43									Re	eser	ved	for	futu	ıre ι	ıse.	Sha	ll be	0.											
D	RW	PROTOCOL									Pi	roto	col a	as d	efin	ed b	y th	ne b	7:b6	of	SEL_	RES	res	por	se i	n th	ie				
											N	FC F	orui	m, N	NFC	Digi	tal I	rot	осо	l Te	chni	cal S	рес	ifica	tio	1					
Е	RW	RFU7									Re	eser	ved	for	futu	ıre ι	ıse.	Sha	II be	e 0.											

42.13 Electrical specification

42.13.1 NFCT Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
f _c	Frequency of operation		13.56		MHz
C _{MI}	Carrier modulation index	95			%
DR	Data Rate		106		kbps
f_s	Modulation sub-carrier frequency		f _c /16		MHz
V_{swing}	Peak differential Input voltage swing on NFC1 and NFC2			VDD	Vp
V _{sense}	Peak differential Field detect threshold level on NFC1-NFC2 ³⁵		1.0		Vp
I _{sense}	Current in SENSE STATE		100		nA
I _{activated}	Current in ACTIVATED STATE		480		μΑ
R _{in_min}	Minimum input resistance when regulating voltage swing			40	Ω
R _{in_max}	Maximum input resistance when regulating voltage swing	1.0			kΩ
$R_{in_loadmod}$	Input resistance when load modulating	8		22	Ω
I _{max}	Maximum input current on NFC pins			80	mA

42.13.2 NFCT Timing Parameters

Symbol	Description	Min.	Тур.	Max.	Units
t _{activate}	Time from task_ACTIVATE in SENSE or DISABLE state to ACTIVATE_A or IDLE state ³⁶			500	us
t _{sense}	Time from remote field is present in SENSE mode to FIELDDETECTED event is asserted			20	us

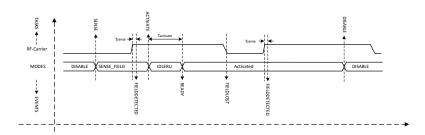


Figure 123: NFCT timing parameters (Shortcuts for FIELDDETECTED and FIELDLOST are disabled)

Input is high impedance in sense mode
 Does not account for voltage supply and oscillator startup times



43 PDM — Pulse density modulation interface

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (Left and Right) data input. Data is transferred directly to RAM buffers using EasyDMA.

Listed here are the main features for PDM:

- Up to two PDM microphones configured as a Left/Right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- · EasyDMA support for sample buffering
- · HW decimation filters

The PDM module illustrated in *Figure 124: PDM module* on page 436 is interfacing up to two digital microphones with the PDM interface. It implements EasyDMA, which relieves real-time requirements associated with controlling the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce PCM samples. The PDM module allows continuous audio streaming.

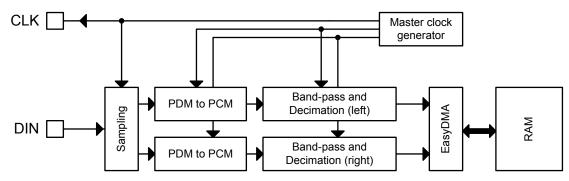


Figure 124: PDM module

43.1 Master clock generator

The FREQ field in the master clock's PDMCLKCTRL register allows adjusting the PDM clock's frequency.

The master clock generator does not add any jitter to the HFCLK source chosen. It is recommended (but not mandatory) to use the Xtal as HFCLK source.

43.2 Module operation

By default, bits from the left PDM microphone are sampled on PDM_CLK falling edge, bits for the right are sampled on the rising edge of PDM_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the PDM stream into 16-bit PCM samples, and filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping Left and Right, so that Left will be sampled on rising edge, and Right on falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM.

Depending on the mode chosen in the OPERATION field in the MODE register, memory either contains alternating left and right 16-bit samples (Stereo), or only left 16-bit samples (Mono).

To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.



The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The STOPPED event indicates that all activity in the module are finished, and that the data is available in RAM (EasyDMA has finished transferring as well). Attempting to restart before receiving the STOPPED event may result in unpredictable behaviour.

43.3 Decimation filter

In order to convert the incoming data stream into PCM audio samples, a decimation filter is included in the PDM interface module.

The input of the filter is the two-channel PDM serial stream (with left channel on clock high, right channel on clock low), its output is 2×16 -bit PCM samples at a sample rate 64 times lower than the PDM clock rate.

The filter stage of each channel is followed by a digital volume control, to attenuate or amplify the output samples in a range of -20 dB to +20 dB around the default (reset) setting, defined by $G_{PDM,default}$. The gain is controlled by the GAINL and GAINR registers.

As an example, if the goal is to achieve 2500 RMS output samples (16 bit) with a 1 kHz 90 dBA signal into a -26 dBFS sensitivity PDM microphone, the user will have to sum the PDM module's default gain ($G_{PDM,default}$) and the gain introduced by the microphone and acoustic path of his implementation (an attenuation would translate into a negative gain), and adjust GAINL and GAINR by this amount. Assuming that only the PDM module influences the gain, GAINL and GAINR must be set to - $G_{PDM,default}$ dB to achieve the requirement.

With $G_{PDM,default}$ =3.2 dB, and as GAINL and GAINR are expressed in 0.5 dB steps, the closest value to program would be 3.0 dB, which can be calculated as:

```
GAINL = GAINR = (DefaultGain - (2 * 3))
```

Remember to check that the resulting values programmed into GAINL and GAINR fall within MinGain and MaxGain.

43.4 EasyDMA

Samples will be written directly to RAM, and EasyDMA must be configured accordingly.

The address pointer for the EasyDMA channel is set in SAMPLE.PTR register. If the destination address set in SAMPLE.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

DMA supports Stereo (Left+Right 16-bit samples) and Mono (Left only) data transfer, depending on setting in the OPERATION field in the MODE register. The samples are stored little endian.

Table 102: DMA sample storage

MODE.OPERATION	Bits per sample	Result stored per RAM word	Physical RAM allocated (32 bit words)	Result boundary indexes in RAM	Note
Stereo	32 (2x16)	L+R	ceil(SAMPLE.MAXCNT/2)	R0=[31:16]; L0=[15:0]	Default
Mono	16	2xL	ceil(SAMPLE.MAXCNT/2)	L1=[31:16]: L0=[15:0]	

The destination buffer in RAM consists of one block, the size of which is set in SAMPLE.MAXCNT register. Format is number of 16-bit samples. The physical RAM allocated is always:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 2;
```

(but the mapping of the samples depends on MODE.OPERATION.

If OPERATION=Stereo, RAM will contain a succession of Left and Right samples.

If OPERATION=Mono, RAM will contain a succession of mono samples.



For a given value of SAMPLE.MAXCNT, the buffer in RAM can contain half the stereo sampling time as compared to the mono sampling time.

The PDM acquisition can be started by the START task, after the SAMPLE.PTR and SAMPLE.MAXCNT registers have been written. When starting the module, it will take some time for the filters to start outputting valid data. Transients from the PDM microphone itself may also occur. The first few samples (typically around 50) might hence contain invalid values or transients. It is therefore advised to discard the first few samples after a PDM start.

As soon as the STARTED event is received, the firmware can write the next SAMPLE.PTR value (this register is double-buffered), to ensure continuous operation.

When the buffer in RAM is filled with samples, an END event is triggered. The firmware can start processing the data in the buffer. Meanwhile, the PDM module starts acquiring data into the new buffer pointed to by SAMPLE.PTR, and sends a new STARTED event, so that the firmware can update SAMPLE.PTR to the next buffer address.

43.5 Hardware example

Connect the microphone clock to CLK, and data to DIN.



Figure 125: Example of a single PDM microphone, wired as left



Figure 126: Example of a single PDM microphone, wired as right

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data. If two microphones are used, one of them has to be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

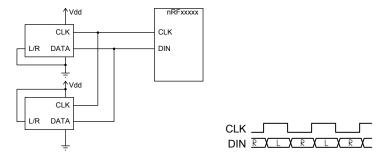


Figure 127: Example of two PDM microphones

43.6 Pin configuration

The CLK and DIN signals associated to the PDM module are mapped to physical pins according to the configuration specified in the PSEL.CLK and PSEL.DIN registers respectively. If the CONNECT field in any PSEL register is set to Disconnected, the associated PDM module signal will not be connected to the required physical pins, and will not operate properly.



The PSEL.CLK and PSEL.DIN registers and their configurations are only used as long as the PDM module is enabled, and retained only as long as the device is in System ON mode. See *POWER — Power supply* on page 78 for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To ensure correct behaviour in the PDM module, the pins used by the PDM module must be configured in the GPIO peripheral as described in *Table 103: GPIO configuration before enabling peripheral* on page 439 before enabling the PDM module. This is to ensure that the pins used by the PDM module are driven correctly if the PDM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the PDM module is supposed to be connected to an external PDM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.

Table 103: GPIO configuration before enabling peripheral

PDM signal	PDM pin	Direction	Output value	Comment
CLK	As specified in PSEL.CLK	Output	0	
DIN	As specified in PSEL.DIN	Input	Not applicable	

43.7 Registers

Table 104: Instances

Base address	Peripheral	Instance	Description	Configuration
0x4001D000	PDM	PDM	Pulse Density Modulation (Digital	
			Microphone Interface)	

Table 105: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous PDM transfer
TASKS_STOP	0x004	Stops PDM transfer
EVENTS_STARTED	0x100	PDM transfer has started
EVENTS_STOPPED	0x104	PDM transfer has finished
EVENTS_END	0x108	The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP
		task has been received) to Data RAM
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PDM module enable register
PDMCLKCTRL	0x504	PDM clock generator control
MODE	0x508	Defines the routing of the connected PDM microphones' signals
GAINL	0x518	Left output gain adjustment
GAINR	0x51C	Right output gain adjustment
PSEL.CLK	0x540	Pin number configuration for PDM CLK signal
PSEL.DIN	0x544	Pin number configuration for PDM DIN signal
SAMPLE.PTR	0x560	RAM address pointer to write samples to with EasyDMA
SAMPLE.MAXCNT	0x564	Number of samples to allocate memory for in EasyDMA mode

43.7.1 INTEN

Address offset: 0x300 Enable or disable interrupt



Bit r	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW STARTED			Enable or disable interrupt for STARTED event
				See EVENTS_STARTED
		Disabled	0	Disable
		Enabled	1	Enable
В	RW STOPPED			Enable or disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Disabled	0	Disable
		Enabled	1	Enable
С	RW END			Enable or disable interrupt for END event
				See EVENTS_END
		Disabled	0	Disable
		Enabled	1	Enable

43.7.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit	number		31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				СВА
Res	set 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW Field	Value Id	Value	Description
Α	RW STARTED			Write '1' to Enable interrupt for STARTED event
				See EVENTS_STARTED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW END			Write '1' to Enable interrupt for END event
				See EVENTS_END
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

43.7.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		31	1 30	29	28	8 27	7 2	6 2	5 2	24 2	23 2	22 2	21 2	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		С	ВА
Res	et 0x0	0000000		0	0	0	0	0) (0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue								Des	crip	otio	n																			
Α	RW	STARTED										١	Vri	te '	1' t	o D	isal	ole	int	err	upt	fo	·ST	AR	ΓED	ev	ent								
												9	See	EV	ENT	rs	STA	RT	ΈD																
			Clear	1								[Disa	ble	•																				
			Disabled	0								F	Rea	d: E	Disa	ble	d																		
			Enabled	1								F	Rea	d: E	nal	ble	b																		
В	RW	STOPPED										١	Wri	te '	1' t	o D	isal	ole	int	err	upt	fo	ST	OP	PED	ev	ent								



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_STOPPED
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW END			Write '1' to Disable interrupt for END event
			See EVENTS_END
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

43.7.4 ENABLE

Address offset: 0x500

PDM module enable register

Bitı	numbe	er		31 30	29	28	27	26	25 2	24 2	23 2	22 2	1 20) 19	18	17	16	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3 2	1	0
Id																															Α
Res	et 0x0	0000000		0 0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value	е						Des	crip	tion																		
Α	RW	ENABLE								E	nal	ole d	or di	sab	le P	DM	mc	du	le												
			Disabled	0						[Disa	ble																			
			Enabled	1						E	nal	ble																			

43.7.5 PDMCLKCTRL

Address offset: 0x504

PDM clock generator control

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x08400000		0 0 0 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW FREQ		PDM_CLK frequency
	1000K	0x08000000 PDM_CLK = 32 MHz / 32 = 1.000 MHz
	Default	0x08400000 PDM_CLK = 32 MHz / 31 = 1.032 MHz
	1067K	0x08800000 PDM_CLK = 32 MHz / 30 = 1.067 MHz

43.7.6 MODE

Address offset: 0x508

Defines the routing of the connected PDM microphones' signals

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		В
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW OPERATION		Mono or stereo operation
	Stereo	0 Sample and store one pair (Left + Right) of 16bit samples per
		RAM word R=[31:16]; L=[15:0]
	Mono	1 Sample and store two successive Left samples (16 bit each) per
		RAM word L1=[31:16]; L0=[15:0]
B RW EDGE		Defines on which PDM_CLK edge Left (or mono) is sampled
	LeftFalling	0 Left (or mono) is sampled on falling edge of PDM_CLK
	LeftRising	1 Left (or mono) is sampled on rising edge of PDM_CLK



43.7.7 GAINL

Address offset: 0x518

Left output gain adjustment

43.7.8 GAINR

Address offset: 0x51C

Right output gain adjustment

Bit	numbe	r		33	1 30	29	28	27	7 2	6 2	5 24	4 23	3 2:	2 2	1 2	0 1	19 :	18	17	16	15	14	13	12	11 :	10	9	8	7	6	5	4	3	2	1	0
Id																												,	4	Α	Α	Α	Α	Α	A	Α
Re	et 0x0	0000028		0	0	0	0	0	0	0	0	0	0	0) () (0	0	0	0	0	0	0	0	0	0	0	0 (כ	0	1	0	1	0	0	0
Id	RW	Field	Value Id	V	alue							D	esc	ript	tior	1																				
Α	RW	GAINR										Ri	ght	t ou	ıtpı	ut g	gair	ac	djus	tm	en	i, in	0.5	dB	ste	ps,	arc	und	th	e						
												d	efa	ult	mo	dul	le g	air	ı (s	ee (ele	tri	al p	ara	me	ters	5)									
			MinGain	0>	x00							-2	0d	Bga	ain	adj	just	tm	ent	(m	iniı	nuı	n)													
			DefaultGain	0>	x28							00	dB g	gair	n ac	djus	stm	en	t ('	250	00 F	MS	s' re	qui	rem	ent	:)									
			MaxGain	0>	x50							+2	20d	lB g	ain	ad	ljus	tm	ent	(n	nax	mι	ım)													
			DefaultGain	0>	x28							-2 00	efai Odi dB (ult i B ga gair	mo ain n ac	dul adj	le g just	air tm	ent	ee ((m 250	eleo inii 00 F	trio mui	cal p m) 5' re	oara	ime	ters	5)									

43.7.9 PSEL.CLK

Address offset: 0x540

Pin number configuration for PDM CLK signal

Bit r	numbe	er		31	30 29	9 28	27	26 2	25 2	24 2	23 22	2 21	20	19	18	17 1	6 15	5 14	13 1	12 13	10	9	8	7	6 5	4	3	2	1 0
Id				В																						Α	Α	Α	А А
Res	et OxF	FFFFFF		1	1 1	1	1	1	1	1	1 1	1	1	1	1	1 1	1	1	1	1 1	1	1	1	1	1 1	. 1	1	1	1 1
Id	RW	Field	Value Id	Val	ıe					ı	Desc	ript	ion																
Α	RW	PIN		[0	31]					ı	Pin n	uml	ber																
В	RW	CONNECT								(Conn	ect	ion																
			Disconnected	1						1	Disco	onne	ect																
			Connected	0						(Conn	ect																	

43.7.10 PSEL.DIN

Address offset: 0x544



Pin number configuration for PDM DIN signal

Bit	numb	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				В	АААА
Re	set 0xl	FFFFFFF		1 1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
В	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

43.7.11 SAMPLE.PTR

Address offset: 0x560

RAM address pointer to write samples to with EasyDMA

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW SAMPLEPTR		Address to write PDM samples to over DMA

43.7.12 SAMPLE.MAXCNT

Address offset: 0x564

Number of samples to allocate memory for in EasyDMA mode

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
Id		A A A A A A A A A A A A A A A A A A A	A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0
Id RW Field	Value Id	Value Description	
A RW BUFFSIZE		[032767] Length of DMA RAM allocation in number of samples	

43.8 Electrical specification

43.8.1 PDM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PDM,stereo}	PDM module active current, stereo operation ³⁷		1.4		mA
f _{PDM,CLK}	PDM clock speed		1.032		MHz
t _{PDM,JITTER}	Jitter in PDM clock output			20	ns
T _{dPDM,CLK}	PDM clock duty cycle	40	50	60	%
$t_{PDM,DATA}$	Decimation filter delay			5	ms
t _{PDM,cv}	Allowed clock edge to data valid			125	ns
t _{PDM,ci}	Allowed (other) clock edge to data invalid	0			ns
t _{PDM,s}	Data setup time at f _{PDM,CLK} =1.024 MHz	65			ns
t _{PDM,h}	Data hold time at f _{PDM,CLK} =1.024 MHz	0			ns
G _{PDM,default}	Default (reset) absolute gain of the PDM module		3.2		dB

³⁷ Average current including PDM and DMA transfers, excluding clock and power supply base currents



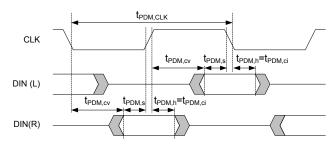


Figure 128: PDM timing diagram



44 I²S — Inter-IC sound interface

The I²S (Inter-IC Sound) module, supports the original two-channel I²S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention.

The I²S peripheral has the following main features:

- · Master and Slave mode
- · Simultaneous bi-directional (TX and RX) audio streaming
- Original I²S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- · Various sample rates

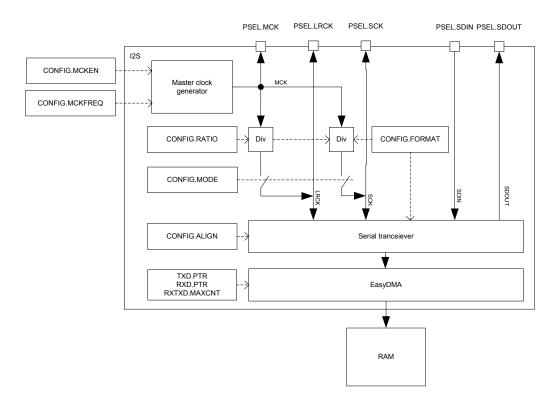


Figure 129: I²S master

44.1 Mode

The I²S protocol specification defines two modes of operation, Master and Slave.

The I²S mode decides which of the two sides (Master or Slave) shall provide the clock signals LRCK and SCK, and these signals are always supplied by the Master to the Slave.

44.2 Transmitting and receiving

The I²S module supports both transmission (TX) and reception (RX) of serial data. In both cases the serial data is shifted synchronously to the clock signals SCK and LRCK.



TX data is written to the SDOUT pin on the falling edge of SCK, and RX data is read from the SDIN pin on the rising edge of SCK. The most significant bit (MSB) is always transmitted first.

TX and RX are available in both Master and Slave modes and can be enabled/disabled independently in the CONFIG.TXEN on page 455 and CONFIG.RXEN on page 455.

Transmission and/or reception is started by triggering the START task. When started and transmission is enabled (in *CONFIG.TXEN* on page 455), the TXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 458 number of transmitted data words (containing one or more samples). Similarly, when started and reception is enabled (in *CONFIG.RXEN* on page 455), the RXPTRUPD event will be generated for every *RXTXD.MAXCNT* on page 458 received data words.

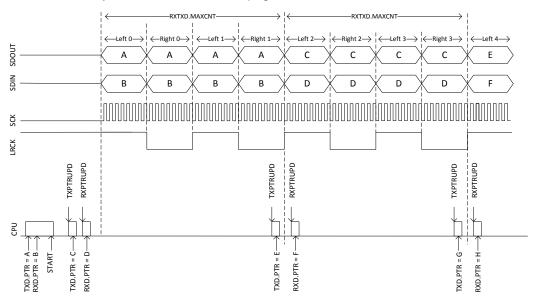


Figure 130: Transmitting and receiving. CONFIG.FORMAT = Aligned, CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo, RXTXD.MAXCNT = 1.

44.3 Left right clock (LRCK)

The Left Right Clock (LRCK), often referred to as "word clock", "sample clock" or "word select" in I²S context, is the clock defining the frames in the serial bit streams sent and received on SDOUT and SDIN, respectively.

In I2S mode, each frame contains one left and right sample pair, with the left sample being transferred during the low half period of LRCK followed by the right sample being transferred during the high period of LRCK.

In Aligned mode, each frame contains one left and right sample pair, with the left sample being transferred during the high half period of LRCK followed by the right sample being transferred during the low period of LRCK.

Consequently, the LRCK frequency is equivalent to the audio sample rate.

When operating in Master mode, the LRCK is generated from the MCK, and the frequency of LRCK is then given as:

```
LRCK = MCK / CONFIG.RATIO
```

LRCK always toggles around the falling edge of the serial clock SCK.

44.4 Serial clock (SCK)

The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.



When operating in Master mode the SCK is generated from the MCK, and the frequency of SCK is then given as:

```
SCK = 2 * LRCK * CONFIG.SWIDTH
```

The falling edge of the SCK falls on the toggling edge of LRCK.

When operating in Slave mode SCK is provided by the external I²S master.

44.5 Master clock (MCK)

The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode.

The MCK is generated by an internal MCK generator. This generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in slave mode can be useful in the case where the external Master is not able to generate its own master clock.

The MCK generator is enabled/disabled in the register *CONFIG.MCKEN* on page 456, and the generator is started or stopped by the START or STOP tasks.

In Master mode the LRCK and the SCK frequencies are closely related, as both are derived from MCK and set indirectly through *CONFIG.RATIO* on page 456 and *CONFIG.SWIDTH* on page 457.

When configuring these registers, the user is responsible for fulfilling the following requirements:

1. SCK frequency can never exceed the MCK frequency, which can be formulated as:

```
CONFIG.RATIO >= 2 * CONFIG.SWIDTH
```

2. The MCK/LRCK ratio shall be a multiple of 2 * CONFIG.SWIDTH, which can be formulated as:

```
Integer = (CONFIG.RATIO / (2 * CONFIG.SWIDTH))
```

The MCK signal can be routed to an output pin (specified in PSEL.MCK) to supply external I²S devices that require the MCK to be supplied from the outside.

When operating in Slave mode, the I²S module does not use the MCK and the MCK generator does not need to be enabled.

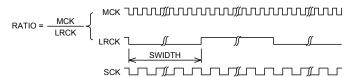


Figure 131: Relation between RATIO, MCK and LRCK.

Table 106: Configuration examples

Desired LRCK [Hz]	CONFIG.SWIDTH	CONFIG.RATIO	CONFIG.MCKFREQ	MCK [Hz]	LRCK [Hz]	LRCK error [%]
16000	16Bit	32X	32MDIV63	507936.5	15873.0	-0.8
16000	16Bit	64X	32MDIV31	1032258.1	16129.0	0.8
16000	16Bit	256X	32MDIV8	4000000.0	15625.0	-2.3
32000	16Bit	32X	32MDIV31	1032258.1	32258.1	0.8
32000	16Bit	64X	32MDIV16	2000000.0	31250.0	-2.3
32000	16Bit	256X	32MDIV4	8000000.0	31250.0	-2.3
44100	16Bit	32X	32MDIV23	1391304.3	43478.3	-1.4
44100	16Bit	64X	32MDIV11	2909090.9	45454.5	3.1
44100	16Bit	256X	32MDIV3	10666666.7	41666.7	-5.5

44.6 Width, alignment and format

The CONFIG.SWIDTH register primarily defines the sample width of the data written to memory. In master mode, it then also sets the amount of bits per frame. In Slave mode it controls padding/trimming if required. Left, right, transmitted, and received samples always have the same width. The CONFIG.FORMAT register specifies the position of the data frames with respect to the LRCK edges in both Master and Slave modes.



When using I²S format, the first bit in a half-frame (containing one left or right sample) gets sampled on the second rising edge of the SCK after a LRCK edge. When using Aligned mode, the first bit in a half-frame gets sampled on the first rising edge of SCK following a LRCK edge.

For data being received on SDIN the sample value can be either right or left-aligned inside a half-frame, as specified in *CONFIG.ALIGN* on page 457. *CONFIG.ALIGN* on page 457 affects only the decoding of the incoming samples (SDIN), while the outgoing samples (SDOUT) are always left-aligned (or justified).

When using left-alignment, each half-frame starts with the MSB of the sample value (both for data being sent on SDOUT and received on SDIN).

When using right-alignment, each half-frame of data being received on SDIN ends with the LSB of the sample value, while each half-frame of data being sent on SDOUT starts with the MSB of the sample value (same as for left-alignment).

In Master mode, the size of a half-frame (in number of SCK periods) equals the sample width (in number of bits), and in this case the alignment setting does not care as each half-frame in any case will start with the MSB and end with the LSB of the sample value.

In slave mode, however, the sample width does not need to equal the frame size. This means you might have extra or fewer SCK pulses per half-frame than what the sample width specified in *CONFIG.SWIDTH* requires.

In the case where we use **left-alignment** and the number of SCK pulses per half-frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits after the LSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0.

In the case where we use **left-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

· Data sent and received on SDOUT and SDIN will be truncated with the LSBs being removed first.

In the case where we use **right-alignment** and the number of SCK pulses per frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits before the MSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0 (same behavior as for left-alignment).

In the case where we use **right-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data received on SDIN will be sign-extended to "sample width" number of bits before being written to memory.
- Data sent on SDOUT will be truncated with the LSBs being removed first (same behavior as for leftalignment).

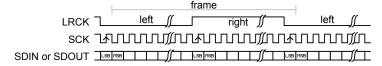


Figure 132: I²S format. CONFIG.SWIDTH equalling half-frame size.

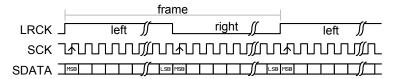


Figure 133: Aligned format. CONFIG.SWIDTH equalling half-frame size.



44.7 EasyDMA

The I²S module implements EasyDMA for accessing internal Data RAM without CPU intervention.

The source and destination pointers for the TX and RX data are configured in *TXD.PTR* on page 458 and *RXD.PTR* on page 458. The memory pointed to by these pointers will only be read or written when TX or RX are enabled in *CONFIG.TXEN* on page 455 and *CONFIG.RXEN* on page 455.

The addresses written to the pointer registers *TXD.PTR* on page 458 and *RXD.PTR* on page 458 are double-buffered in hardware, and these double buffers are updated for every *RXTXD.MAXCNT* on page 458 words (containing one or more samples) read/written from/to memory. The events TXPTRUPD and RXPTRUPD are generated whenever the TXD.PTR and RXD.PTR are transferred to these double buffers.

If *TXD.PTR* on page 458 is not pointing to the Data RAM region when transmission is enabled, or *RXD.PTR* on page 458 is not pointing to the Data RAM region when reception is enabled, an EasyDMA transfer may result in a HardFault and/or memory corruption. See *Memory* on page 23 for more information about the different memory regions.

Due to the nature of I²S, where the number of transmitted samples always equals the number of received samples (at least when both TX and RX are enabled), one common register *RXTXD.MAXCNT* on page 458 is used for specifying the sizes of these two memory buffers. The size of the buffers is specified in a number of 32-bit words. Such a 32-bit memory word can either contain four 8-bit samples, two 16-bit samples or one right-aligned 24-bit sample sign extended to 32 bit.

In stereo mode (CONFIG.CHANNELS=Stereo), the samples are stored as "left and right sample pairs" in memory. Figure Figure 134: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo. on page 449, Figure 136: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo. on page 450 and Figure 138: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo. on page 450 show how the samples are mapped to memory in this mode. The mapping is valid for both RX and TX.

In mono mode (CONFIG.CHANNELS=Left or Right), RX sample from only one channel in the frame is stored in memory, the other channel sample is ignored. Illustrations *Figure 135: Memory mapping for 8 bit mono.* CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left. on page 450, Figure 137: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left. on page 450 and Figure 139: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left. on page 451 show how RX samples are mapped to memory in this mode.

For TX, the same outgoing sample read from memory is transmitted on both left and right in a frame, resulting in a mono output stream.

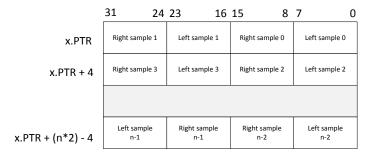


Figure 134: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo.



	31 24	23 16	15 8	7 0
x.PTR	Left sample 3	Left sample 2	Left sample 1	Left sample 0
x.PTR + 4	Left sample 7	Left sample 6	Left sample 5	Left sample 4
x.PTR + n - 4	Left sample n-1	Left sample n-2	Left sample n-3	Left sample n-4

Figure 135: Memory mapping for 8 bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left.

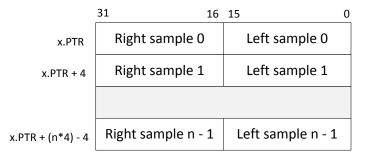


Figure 136: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo.

	31 16	15 0
x.PTR	Left sample 1	Left sample 0
x.PTR + 4	Left sample 3	Left sample 2
x.PTR + (n*2) - 4	Left sample n - 1	Left sample n - 2

Figure 137: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left.

	31	23)
x.PTR	Sign ext.	Left sample 0	
x.PTR + 4	Sign ext.	Right sample 0	
x.PTR + (n*8) - 8	Sign ext.	Left sample n - 1	
x.PTR + (n*8) - 4	Sign ext.	Right sample n - 1	

Figure 138: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo.



	31	23	0
x.PTR	Sign ext.	Left sample 0	
x.PTR + 4	Sign ext.	Left sample 1	
x.PTR + (n*4) - 4	Sign ext.	Left sample n - 1	

Figure 139: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left.

44.8 Module operation

Described here is a typical operating procedure for the I²S module.

1. Configure the I²S module using the CONFIG registers

```
// Enable reception
NRF I2S->CONFIG.RXEN = (I2S CONFIG RXEN RXEN Enabled <<
                                        I2S_CONFIG_RXEN_RXEN_Pos);
// Enable transmission
NRF I2S->CONFIG.TXEN = (I2S CONFIG TXEN TXEN Enabled <<
                                        I2S CONFIG TXEN TXEN Pos);
// Enable MCK generator
NRF_I2S->CONFIG.MCKEN = (I2S_CONFIG_MCKEN_MCKEN_Enabled <<</pre>
                                        12S CONFIG MCKEN MCKEN Pos);
// MCKFREQ = 4 MHz
NRF_12S->CONFIG.MCKFREQ = 12S_CONFIG_MCKFREQ_MCKFREQ_32MDIV8 <<
                                        12S CONFIG MCKFREQ MCKFREQ Pos;
// Ratio = 256
NRF I2S->CONFIG.RATIO = I2S CONFIG RATIO RATIO 256X <<
                                       12S CONFIG RATIO RATIO Pos;
// MCKFREQ = 4 MHz and Ratio = 256 gives sample rate = 15.625 ks/s
// Sample width = 16 bit
NRF I2S->CONFIG.SWIDTH = I2S CONFIG SWIDTH SWIDTH 16Bit <<
                                        12S CONFIG SWIDTH SWIDTH Pos;
// Alignment = Left
NRF I2S->CONFIG.ALIGN = I2S CONFIG ALIGN ALIGN Left <<
                                       12S CONFIG ALIGN ALIGN Pos;
// Format = I2S
NRF I2S->CONFIG.FORMAT = I2S CONFIG FORMAT FORMAT I2S <<
                                        12S CONFIG FORMAT FORMAT Pos;
// Use stereo
NRF I2S->CONFIG.CHANNELS = I2S CONFIG CHANNELS CHANNELS Stereo <<
                                        12S CONFIG CHANNELS CHANNELS Pos;
```

2. Map IO pins using the PINSEL registers



3. Configure TX and RX data pointers using the TXD, RXD and RXTXD registers

```
NRF_I2S->TXD.PTR = my_tx_buf;
NRF_I2S->RXD.PTR = my_rx_buf;
NRF_I2S->TXD.MAXCNT = MY_BUF_SIZE;
```

4. Enable the I²S module using the ENABLE register

```
NRF_I2S->ENABLE = 1;
```

5. Start audio streaming using the START task

```
NRF_I2S->TASKS_START = 1;
```

6. Handle received and transmitted data when receiving the TXPTRUPD and RXPTRUPD events

```
if (NRF_I2S->EVENTS_TXPTRUPD != 0)
{
    NRF_I2S->TXD.PTR = my_next_tx_buf;
    NRF_I2S->EVENTS_TXPTRUPD = 0;
}

if (NRF_I2S->EVENTS_RXPTRUPD != 0)
{
    NRF_I2S->RXD.PTR = my_next_rx_buf;
    NRF_I2S->EVENTS_RXPTRUPD = 0;
}
```

44.9 Pin configuration

The MCK, SCK, LRCK, SDIN and SDOUT signals associated with the I²S module are mapped to physical pins according to the pin numbers specified in the PSEL.x registers.

These pins are acquired whenever the I²S module is enabled through the register *ENABLE* on page 455.

When a pin is acquired by the I²S module, the direction of the pin (input or output) will be configured automatically, and any pin direction setting done in the GPIO module will be overridden. The directions for the various I²S pins are shown below in *Table 107: GPIO configuration before enabling peripheral (master mode)* on page 452 and *Table 108: GPIO configuration before enabling peripheral (slave mode)* on page 453.

To secure correct signal levels on the pins when the system is in OFF mode, and when the I²S module is disabled, these pins must be configured in the GPIO peripheral directly.

Table 107: GPIO configuration before enabling peripheral (master mode)

I ² S signal	I ² S pin	Direction	Output value	Comment
MCK	As specified in PSEL.MCK	Output	0	
LRCK	As specified in PSEL.LRCK	Output	0	



I ² S signal	I ² S pin	Direction	Output value	Comment
SCK	As specified in PSEL.SCK	Output	0	
SDIN	As specified in PSEL.SDIN	Input	Not applicable	
SDOUT	As specified in PSEL.SDOUT	Output	0	

Table 108: GPIO configuration before enabling peripheral (slave mode)

I ² S signal	I ² S pin	Direction	Output value	Comment
MCK	As specified in PSEL.MCK	Output	0	
LRCK	As specified in PSEL.LRCK	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
SDIN	As specified in PSEL.SDIN	Input	Not applicable	
SDOUT	As specified in PSEL.SDOUT	Output	0	

44.10 Registers

Table 109: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40025000	I2S	125	Inter-IC Sound Interface		

Table 110: Register Overview

Register	Offset	Description
TASKS_START	0x000	Starts continuous I2S transfer. Also starts MCK generator when this is enabled.
TASKS_STOP	0x004	Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the {event:STOPPED}
		event to be generated.
EVENTS_RXPTRUPD	0x104	The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started
		and RX is enabled, this event will be generated for every RXTXD.MAXCNT words that are received on
		the SDIN pin.
EVENTS_STOPPED	0x108	12S transfer stopped.
EVENTS_TXPTRUPD	0x114	The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started
		and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the
		SDOUT pin.
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	Enable I2S module.
CONFIG.MODE	0x504	I2S mode.
CONFIG.RXEN	0x508	Reception (RX) enable.
CONFIG.TXEN	0x50C	Transmission (TX) enable.
CONFIG.MCKEN	0x510	Master clock generator enable.
CONFIG.MCKFREQ	0x514	Master clock generator frequency.
CONFIG.RATIO	0x518	MCK / LRCK ratio.
CONFIG.SWIDTH	0x51C	Sample width.
CONFIG.ALIGN	0x520	Alignment of sample within a frame.
CONFIG.FORMAT	0x524	Frame format.
CONFIG.CHANNELS	0x528	Enable channels.
RXD.PTR	0x538	Receive buffer RAM start address.
TXD.PTR	0x540	Transmit buffer RAM start address.
RXTXD.MAXCNT	0x550	Size of RXD and TXD buffers.
PSEL.MCK	0x560	Pin select for MCK signal.
PSEL.SCK	0x564	Pin select for SCK signal.
PSEL.LRCK	0x568	Pin select for LRCK signal.
PSEL.SDIN	0x56C	Pin select for SDIN signal.
PSEL.SDOUT	0x570	Pin select for SDOUT signal.

44.10.1 INTEN

Address offset: 0x300 Enable or disable interrupt



Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				F C B
Rese	et 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
В	RW RXPTRUPD			Enable or disable interrupt for RXPTRUPD event
				See EVENTS_RXPTRUPD
		Disabled	0	Disable
		Enabled	1	Enable
С	RW STOPPED			Enable or disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Disabled	0	Disable
		Enabled	1	Enable
F	RW TXPTRUPD			Enable or disable interrupt for TXPTRUPD event
				See EVENTS_TXPTRUPD
		Disabled	0	Disable
		Enabled	1	Enable

44.10.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		F C B
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
B RW RXPTRUPD		Write '1' to Enable interrupt for RXPTRUPD event
		See EVENTS_RXPTRUPD
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
C RW STOPPED		Write '1' to Enable interrupt for STOPPED event
		See EVENTS_STOPPED
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled
F RW TXPTRUPD		Write '1' to Enable interrupt for TXPTRUPD event
		See EVENTS_TXPTRUPD
	Set	1 Enable
	Disabled	0 Read: Disabled
	Enabled	1 Read: Enabled

44.10.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	er		33	1 30	29	2	8 2	7 :	26	25	24	23	22	21	20	19	18	17	16	15	5 14	1 13	3 12	2 13	10	9	8	7	6	5	4	3	2	1 ()
Id																															F			С	В	
Res	et 0x0	0000000		0	0	0	C	0 0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (כ
Id	RW	Field	Value Id	V	alue								De	scr	ipti	on																				
В	RW	RXPTRUPD											Wı	rite	'1'	to [Disa	ble	in	teri	up	t fo	r R	KPT	RU	PD 6	ver	nt								
													Se	e <i>E</i>	VEN	ITS_	RX	PTF	RUF	PD																
			Clear	1									Dis	ab	le																					
			Disabled	0									Re	ad:	Dis	abl	ed																			
			Enabled	1									Re	ad:	Ena	able	ed																			
С	RW	STOPPED											Wı	rite	'1'	to [Disa	ble	in	teri	up	t fo	r Sī	ОР	PE) ev	ent									



Bit n	umbe	er		31	30	29 :	28 2	27 2	26 2	:5 2	24 2	23 22	2 21	1 20) 19	18	17	16	15	14 1	.3 1	2 11	10	9	8	7	-	5 4 F	1 3	2 C	1 0
	t 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0			0 0		
Id	RW	Field	Value Id	Va	lue						0	esc	ript	ion																	
											S	ee E	VEI	NTS	_ST	ОРІ	PED														
			Clear	1							0	Disab	le																		
			Disabled	0							F	Read	: Di	sab	led																
			Enabled	1							F	Read	: En	nabl	ed																
F	RW	TXPTRUPD									٧	Vrite	e '1'	' to	Disa	able	int	erru	ıpt 1	or T	XPT	RUP	D e	ven	t						
											S	ee E	VE	NTS	_TX	PTF	RUP	D													
			Clear	1							0	Disab	ole																		
			Disabled	0							F	Read	: Di	sab	led																
			Enabled	1							F	Read	: En	nabl	ed																

44.10.4 ENABLE

Address offset: 0x500 Enable I2S module.

Bit	num	nber			31 3	0 2	9 2	8 2	7 2	6 2	5 24	1 23	3 22	21	20	19	18	17	16	15	14	13 :	12	11 :	10	9	8	7	6	5 .	4 3	2	1	0
Id																																		Α
Res	et 0)x00	000000		0	0 (0 (0 0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	R۱	w	Field	Value Id	Valu	ie						D	escr	ipti	on																			
Α	R۱	W	ENABLE									Er	nabl	e 12	S m	odu	ıle.																	
				Disabled	0							Di	isab	le																				
				Enabled	1							Er	nabl	e																				

44.10.5 CONFIG.MODE

Address offset: 0x504

I2S mode.

Bit	numbe	er		31	. 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11 :	.0	9 8	3 .	7 (5 5	5 4	3	2	1	0
Id																																		Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0	0
Id	RW	Field	Value Id	Va	lue							De	scri	iptio	on																			
Α	RW	MODE										125	mo	ode.																				_
			Master	0								Ma	ste	r m	ode	e. S0	СК а	and	LR	CK §	gen	era	ted	froi	n in	ter	nal	ma	ster					
												clc	ok ((MC	K) a	and	out	tpu	t or	n pi	ns c	lefi	ned	by	PSE	L.xx	x.							
			Slave	1								Sla	ve	mod	de.	SCK	an	d LI	RCK	ge	ner	ate	d b	y ex	terr	al r	nas	ter	and	ł				
												rec	eiv	ed o	on p	oins	de	fine	ed b	у Р	SEL	.xx	K											

44.10.6 CONFIG.RXEN

Address offset: 0x508 Reception (RX) enable.

Bit number	31 30 29 28 27 26 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
A RW RXEN		Reception (RX) enable.
Disabled	0	Reception disabled and now data will be written to the RXD.PTR
		address.
Enabled	1	Reception enabled.

44.10.7 CONFIG.TXEN

Address offset: 0x50C



Transmission (TX) enable.

Bit nun	mber		31	30 2	9 28	3 27	26	25	24	23	22 2	1 20	19	18	17 :	16 1	L5 1	4 1	3 12	11	10	9 8	3 7	6	5	4	3	2	1	0
Id																														Α
Reset (0x00000001		0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	0 (0	0	0	0	0	0	0	1
ld R	W Field	Value Id	Val	ue						Des	cript	tion																		
A R	W TXEN									Trai	nsmi	ssio	n (T	X) e	nab	le.														
		Disabled	0							Trai	nsmi	ssio	n di	sabl	ed a	nd	nov	v da	ta w	ill be	re	ad f	rom	the	:					
										RXC	TXI.	ad	dres	ss.																
		Enabled	1							Trai	nsmi	ssio	n er	abl	ed.															

44.10.8 CONFIG.MCKEN

Address offset: 0x510

Master clock generator enable.

Bitı	numbe	er		31	1 30	29	28	27	26	5 25	5 24	23	3 22	21	20	19	18	17	16	15	14	13 :	L2 1	11 1	0 9	8	7	6	5	4	3	2 :	1 0
Id																																	Α
Res	et 0x0	000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0 (0 1
Id	RW	Field	Value Id	Va	alue	:						De	escri	ptic	n																		
Α	RW	MCKEN										М	aste	r clo	ock	ger	era	itor	en	abl	e.												
			Disabled	0								М	aste	r clo	ock	ger	era	tor	dis	abl	ed	and	PSI	EL.N	1CK	not							
												со	nne	cted	d(av	/aila	ble	as	GΡ	10).													
			Enabled	1								М	aste	r clo	ock	ger	era	tor	rui	nniı	ng a	nd	MC	Κοι	ıtpı	ıt o	n PS	EL.I	MCk	ί.			

44.10.9 CONFIG.MCKFREQ

Address offset: 0x514

Master clock generator frequency.

Bit number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id		$A \ A \ A \ A \ A \ A \ A$	A A A A A A A A A A A A A A A A A A A
Reset 0x20000000		0 0 1 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW MCKFREQ			Master clock generator frequency.
	32MDIV2	0x80000000	32 MHz / 2 = 16.0 MHz
	32MDIV3	0x50000000	32 MHz / 3 = 10.6666667 MHz
	32MDIV4	0x40000000	32 MHz / 4 = 8.0 MHz
	32MDIV5	0x30000000	32 MHz / 5 = 6.4 MHz
	32MDIV6	0x28000000	32 MHz / 6 = 5.3333333 MHz
	32MDIV8	0x20000000	32 MHz / 8 = 4.0 MHz
	32MDIV10	0x18000000	32 MHz / 10 = 3.2 MHz
	32MDIV11	0x16000000	32 MHz / 11 = 2.9090909 MHz
	32MDIV15	0x11000000	32 MHz / 15 = 2.1333333 MHz
	32MDIV16	0x10000000	32 MHz / 16 = 2.0 MHz
	32MDIV21	0x0C000000	32 MHz / 21 = 1.5238095
	32MDIV23	0x0B000000	32 MHz / 23 = 1.3913043 MHz
	32MDIV30	0x0880000	32 MHz / 30 = 1.0666667 MHz
	32MDIV31	0x08400000	32 MHz / 31 = 1.0322581 MHz
	32MDIV32	0x08000000	32 MHz / 32 = 1.0 MHz
	32MDIV42	0x06000000	32 MHz / 42 = 0.7619048 MHz
	32MDIV63	0x04100000	32 MHz / 63 = 0.5079365 MHz
	32MDIV125	0x020C0000	32 MHz / 125 = 0.256 MHz

44.10.10 CONFIG.RATIO

Address offset: 0x518 MCK / LRCK ratio.



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A
Reset 0x00000006		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
A RW RATIO			MCK / LRCK ratio.
	32X	0	LRCK = MCK / 32
	48X	1	LRCK = MCK / 48
	64X	2	LRCK = MCK / 64
	96X	3	LRCK = MCK / 96
	128X	4	LRCK = MCK / 128
	192X	5	LRCK = MCK / 192
	256X	6	LRCK = MCK / 256
	384X	7	LRCK = MCK / 384
	512X	8	LRCK = MCK / 512

44.10.11 CONFIG.SWIDTH

Address offset: 0x51C

Sample width.

Bit numbe	er		31	L 30	29	28	27	26	25	24	23	22	21 :	20	19 1	18 1	17 1	16	15	14 :	L3 1	.2 1	1 1	9	8	7	6	5	4	3	2	1	0
Id																																Α	Α
Reset 0x0	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	1
Id RW	Field	Value Id	Va	alue							De	scri	ptio	n																			
A RW	SWIDTH										Saı	mpl	e wi	idth	١.																		
		8Bit	0								8 b	it.																					
		16Bit	1								16	bit.																					
		24Bit	2								24	bit.																					

44.10.12 CONFIG.ALIGN

Address offset: 0x520

Alignment of sample within a frame.

Bit	nun	nber			3:	1 30	29	28	3 27	7 26	5 25	24	23	22	21	20	19	18	17 :	16 :	15 :	14	13 :	12 :	11 1	.0 9	Э	8	7	6	5 4	1 3	2	1	0
Id																																			Α
Res	et (0x00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0 ()	0	0 (0 0	0	0	0
Id	R	w	Field	Value Id	V	alue	•						De	scri	ptio	on																			
Α	R	W	ALIGN										Ali	gnn	nen	t of	san	nple	e wi	thi	n a	frai	ne.												
				Left	0								Let	ft-al	lign	ed.																			
				Right	1								Rig	ght-	alig	ned																			

44.10.13 CONFIG.FORMAT

Address offset: 0x524

Frame format.

Bit	num	ber			31 3	0 29	9 28	8 27	7 26	5 25	24	23	22	21	20	19	18	17	16	15 :	14	L3 1	.2 1	.1 1	9	8	7	6	5	4	3	2	1 0
Id																																	Α
Res	et O	x00	000000		0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0 0
Id	RV	N	Field	Value Id	Valu	e						De	scri	ipti	on																		
Α	RV	Ν	FORMAT									Fra	ame	e fo	rma	t.																	
				12S	0							Or	igin	al I	2S f	orm	at.																
				Aligned	1							Alt	tern	ate	(le	ft- o	r ri	ght-	alig	gne	d) f	orm	at.										

44.10.14 CONFIG.CHANNELS

Address offset: 0x528 Enable channels.



В	t nı	umbe	r		3	1 3	0 29	9 2	8 2	7 2	26 :	25	24	23	22	21	20	19	18	3 17	7 10	5 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4	3	2	1 ()
Id																																				A A	
R	ese	t 0x0	0000000		0	0	0) () ()	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	,
Id		RW	Field	Value Id	٧	alu	е							De	scr	ipti	on																				
Α		RW	CHANNELS											En	abl	e cl	nan	nel	s.																		
				Stereo	0									Ste	ere	э.																					
				Left	1									Le	ft o	nly																					
				Right	2									Rig	ght	onl	у.																				

44.10.15 RXD.PTR

Address offset: 0x538

Receive buffer RAM start address.

Bit	numb	er		31	. 30	29	28	8 2	7 2	6 2	5 2	4 2	3 2	2 21	20	19	18	17	16 3	15 :	14 1	3 12	2 11	10	9	8	7	6	5	4	3 2	2 1	0
Id				Α	Α	Α	Α	Α Α	۱ ۸	4 <i>A</i>	Δ Α	4 4	A A	AA	Α	Α	Α	Α	Α	Α	A	4 A	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	et 0x	00000000		0	0	0	0	0) (0 (0 (0 () (0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							D	esc	ripti	on																		
Α	RW	PTR										R	ece	ive l	ouff	er [ata	RA	M s	tar	t ad	dres	s. W	her	re	eiv	ing	, w	ord:	s			
												C	ont	ainir	ng sa	amp	oles	wil	be	wri	itter	to 1	this	add	ress	s. Tl	his a	add	res	S			
												is	a v	vord	alie	ne	d D:	ata	RΔN	/ ac	ddra	cc											

44.10.16 TXD.PTR

Address offset: 0x540

Transmit buffer RAM start address.

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21 2	0 19	9 18	17	16	15	14	13 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	ДД	Α	Α	Α	Α	Α	A A	Α	Α	Α	Α	Α	Α	Α	Α	A A	A	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	alue	•						De	scri	ptio	n																	
Α	RW	PTR										Tra	nsn	nit b	uffe	r Da	ta F	RAN	1 sta	irt a	ddre	ss. \	Nhe	n tr	ans	mit	ting	g,				
												wo	rds	con	taini	ng s	amı	ples	wil	l be	fetc	hed	fror	n th	is a	ddr	ess	. Th	nis			
												ado	dres	s is	a wo	ord a	ligr	ned	Dat	a R	AM a	ddre	ess.									

44.10.17 RXTXD.MAXCNT

Address offset: 0x550

Size of RXD and TXD buffers.

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 1	7 16 15 14 13 12 11 10	9 8 7 6 5 4 3	3 2 1 0
Id				AAAA	A A A A A A	A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0	0000000	0000000	0 0 0
Id RW Field	Value Id	Value	Description			
A RW MAXCNT			Size of RXD and TXD	buffers in number of 32 b	oit words.	

44.10.18 PSEL.MCK

Address offset: 0x560

Pin select for MCK signal.

Bit r	iumbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect



44.10.19 PSEL.SCK

Address offset: 0x564
Pin select for SCK signal.

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	$1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;1\;$
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

44.10.20 PSEL.LRCK

Address offset: 0x568

Pin select for LRCK signal.

umbe	r		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
			С	АААА
t OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
RW	Field	Value Id	Value	Description
RW	PIN		[031]	Pin number
RW	CONNECT			Connection
		Disconnected	1	Disconnect
		Connected	0	Connect
	et 0xF RW RW	umber et 0xFFFFFFF RW Field RW PIN RW CONNECT	RW Field Value Id RW PIN RW CONNECT Disconnected	C T T T T T T T T T

44.10.21 PSEL.SDIN

Address offset: 0x56C

Pin select for SDIN signal.

Bitı	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

44.10.22 PSEL.SDOUT

Address offset: 0x570

Pin select for SDOUT signal.

Bitı	numbe	er		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	A A A A
Res	et OxF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect



44.11 Electrical specification

44.11.1 I2S timing specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{S_SDIN}	SDIN setup time before SCK rising	20			ns
t _{H_SDIN}	SDIN hold time after SCK rising	15			ns
t _{S_SDOUT}	SDOUT setup time after SCK falling	40			ns
t _{H_SDOUT}	SDOUT hold time before SCK falling	6			ns
t _{SCK_LRCK}	SCLK falling to LRCK edge	-5	0	5	ns
f _{MCK}	MCK frequency			4000	kHz
f_{LRCK}	LRCK frequency			48	kHz
f _{SCK}	SCK frequency			2000	kHz
DCCK	Clock duty cycle (MCK, LRCK, SCK)	45		55	%

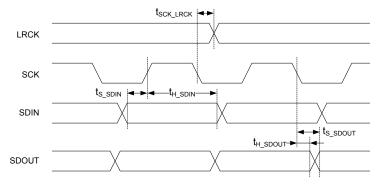


Figure 140: I2S timing diagram



45 MWU — Memory watch unit

The Memory watch unit (MWU) can be used to generate events when a memory region is accessed by the CPU. The MWU can be configured to trigger events for access to Data RAM and Peripheral memory segments. The MWU allows an application developer to generate memory access events during development for debugging or during production execution for failure detection and recovery.

Listed here are the main features for MWU:

- Six memory regions, four user-configurable and two fixed regions in peripheral address space
- Flexible configuration of regions with START and END addresses
- Generate events on CPU read and/or write to a defined region of Data RAM or peripheral memory address space
- Programmable maskable or non-maskable (NMI) interrupt on events
- Peripheral interfaces can be watched for read and write access using subregions of the two fixed memory regions

Table 111: Memory regions

Memory region	START address	END address
REGION[03]	Configurable	Configurable
PREGION[0]	0x4000000	0x4001FFFF
PREGION[1]	0x40020000	0x4003FFFF

Each MWU region is defined by a start address and an end address, configured by the START and END registers respectively. These addresses are byte aligned and inclusive. The END register value has to be greater or equal to the START register value. Each region is associated with a pair of events that indicate that either a write access or a read access from the CPU has been detected inside the region.

For regions containing subregions (see below), a set of status registers PERREGION[0..1].SUBSTATWA and PERREGION[0..1].SUBSTATRA indicate which subregion(s) caused the EVENT_PREGION[0..1].WA and EVENT_PREGION[0..1].RA respectively.

The MWU is only able to detect memory accesses in the Data RAM and Peripheral memory segments from the CPU, see *Memory* on page 23 for more information about the different memory segments. EasyDMA accesses are not monitored by the MWU. The MWU requires two HCLK cycles to detect and generate the event.

The peripheral regions, PREGION[0...1], are divided into 32 equally sized subregions, SR[0...31]. All subregions are excluded in the main region by default, and any can be included by specifying them in the SUBS register. When a subregion is excluded from the main region, the memory watch mechanism will not trigger any events when that subregion is accessed.

Subregions in PREGION[0..1] cannot be individually configured for read or write access watch. Watch configuration is only possible for a region as a whole. The PRGNiRA and PRGNiWA (i=0..1) fields in the REGIONEN register control watching read and write access.

REGION[0..3] can be individually enabled for read and/or write access watching through their respective RGNiRA and RGNiWA (i=0..3) fields in the REGIONEN register.

REGIONENSET and REGIONENCLR allow respectively enabling and disabling one or multiple REGIONs or PREGIONs watching in a single write access.

45.1 Registers

Table 112: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40020000	MWU	MWU	Memory Watch Unit	



Table 113: Register Overview

Register	Offset	Description
EVENTS_REGION[0].WA	0x100	Write access to region 0 detected
EVENTS_REGION[0].RA	0x104	Read access to region 0 detected
EVENTS_REGION[1].WA	0x108	Write access to region 1 detected
EVENTS_REGION[1].RA	0x10C	Read access to region 1 detected
EVENTS_REGION[2].WA	0x110	Write access to region 2 detected
EVENTS_REGION[2].RA	0x114	Read access to region 2 detected
EVENTS_REGION[3].WA	0x118	Write access to region 3 detected
EVENTS_REGION[3].RA	0x11C	Read access to region 3 detected
EVENTS_PREGION[0].W	/A 0x160	Write access to peripheral region 0 detected
EVENTS_PREGION[0].RA	A 0x164	Read access to peripheral region 0 detected
EVENTS_PREGION[1].W	/A 0x168	Write access to peripheral region 1 detected
EVENTS_PREGION[1].RA	A 0x16C	Read access to peripheral region 1 detected
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
NMIEN	0x320	Enable or disable non-maskable interrupt
NMIENSET	0x324	Enable non-maskable interrupt
NMIENCLR	0x328	Disable non-maskable interrupt
PERREGION[0].SUBSTAT	TI 0x400	Source of event/interrupt in region 0, write access detected while corresponding subregion was
		enabled for watching
PERREGION[0].SUBSTAT	T/ 0x404	Source of event/interrupt in region 0, read access detected while corresponding subregion was
		enabled for watching
PERREGION[1].SUBSTAT	TI 0x408	Source of event/interrupt in region 1, write access detected while corresponding subregion was
		enabled for watching
PERREGION[1].SUBSTAT	T/ 0x40C	Source of event/interrupt in region 1, read access detected while corresponding subregion was
		enabled for watching
REGIONEN	0x510	Enable/disable regions watch
REGIONENSET	0x514	Enable regions watch
REGIONENCLR	0x518	Disable regions watch
REGION[0].START	0x600	Start address for region 0
REGION[0].END	0x604	End address of region 0
REGION[1].START	0x610	Start address for region 1
REGION[1].END	0x614	End address of region 1
REGION[2].START	0x620	Start address for region 2
REGION[2].END	0x624	End address of region 2
REGION[3].START	0x630	Start address for region 3
REGION[3].END	0x634	End address of region 3
PREGION[0].START	0x6C0	Reserved for future use
PREGION[0].END	0x6C4	Reserved for future use
PREGION[0].SUBS	0x6C8	Subregions of region 0
PREGION[1].START	0x6D0	Reserved for future use
PREGION[1].END	0x6D4	Reserved for future use
PREGION[1].SUBS	0x6D8	Subregions of region 1

45.1.1 INTEN

Address offset: 0x300 Enable or disable interrupt

Bitı	numbe	r		31	30	29	28 :	27 2	26 2	25 2	4 2	3 2	2 21	1 20	0 19	18	3 17	16	15	14	13 1	12 1	1 10	9	8	7	6	5	4	3 2	2 1	L 0
Id								L	K .	JI	ı															Н	G	F	Е	D (СВ	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0 () (0 (0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0 (0 0	0 (
Id	RW	Field	Value Id	Va	lue						D	esc	ript	ion	1																	
Α	RW	REGION0WA									Ε	nab	le o	r d	isab	le i	nte	rrup	t fo	r Ri	GIC	N[C)].W	۹ ev	ent							
											S	ee l	EVEI	NTS	S_RE	GIO	ON[0].v	VA													
			Disabled	0							D	Disal	ble																			



Bit	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
В	RW REGIONORA	Enabled	1 Enable Enable or disable interrupt for REGION[0].RA event See EVENTS_REGION[0].RA
		Disabled	0 Disable
С	RW REGION1WA	Enabled	1 Enable Enable or disable interrupt for REGION[1].WA event
Č	W REGIONITY		See EVENTS_REGION[1].WA
		Disabled	0 Disable
D	RW REGION1RA	Enabled	1 Enable Enable or disable interrupt for REGION[1].RA event
D	NW REGIONINA		See EVENTS_REGION[1].RA
		Disabled	0 Disable
		Enabled	1 Enable
Ε	RW REGION2WA		Enable or disable interrupt for REGION[2].WA event
			See EVENTS_REGION[2].WA
		Disabled	0 Disable
F	RW REGION2RA	Enabled	1 Enable Enable or disable interrupt for REGION[2].RA event
·			See EVENTS_REGION[2].RA
		Disabled	0 Disable
		Enabled	1 Enable
G	RW REGION3WA		Enable or disable interrupt for REGION[3].WA event See EVENTS_REGION[3].WA
		Disabled	0 Disable
		Enabled	1 Enable
Н	RW REGION3RA		Enable or disable interrupt for REGION[3].RA event
		Disabled	See EVENTS_REGION[3].RA 0 Disable
		Enabled	1 Enable
I	RW PREGIONOWA		Enable or disable interrupt for PREGION[0].WA event
			See EVENTS_PREGION[0].WA
		Disabled	0 Disable
		Enabled	1 Enable
J	RW PREGIONORA		Enable or disable interrupt for PREGION[0].RA event See EVENTS_PREGION[0].RA
		Disabled	0 Disable
		Enabled	1 Enable
K	RW PREGION1WA		Enable or disable interrupt for PREGION[1].WA event
		Disabled	See EVENTS_PREGION[1].WA
		Disabled Enabled	0 Disable 1 Enable
L	RW PREGION1RA	Lilabicu	Enable or disable interrupt for PREGION[1].RA event
			See EVENTS_PREGION[1].RA
		Disabled	0 Disable
		Enabled	1 Enable

45.1.2 INTENSET

Address offset: 0x304 Enable interrupt



Bit r	number		31 30 29 28 27 26	25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K	J I H G F E D C B A
Res	et 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
Α	RW REGIONOWA			Write '1' to Enable interrupt for REGION[0].WA event
				See EVENTS_REGION[0].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
В	RW REGIONORA			Write '1' to Enable interrupt for REGION[0].RA event
				See EVENTS_REGION[0].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW REGION1WA			Write '1' to Enable interrupt for REGION[1].WA event
				See EVENTS_REGION[1].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW REGION1RA			Write '1' to Enable interrupt for REGION[1].RA event
				See EVENTS_REGION[1].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW REGION2WA			Write '1' to Enable interrupt for REGION[2].WA event
				See EVENTS_REGION[2].WA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW REGION2RA			Write '1' to Enable interrupt for REGION[2].RA event
				See EVENTS_REGION[2].RA
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW REGION3WA			Write '1' to Enable interrupt for REGION[3].WA event
		Set	1	See EVENTS_REGION[3].WA Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW REGION3RA			Write '1' to Enable interrupt for REGION[3].RA event
		Set	1	See EVENTS_REGION[3].RA Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
ı	RW PREGIONOWA	2.100.00		Write '1' to Enable interrupt for PREGION[0].WA event
		Cat	1	See EVENTS_PREGION[0].WA
		Set Disabled	1 0	Enable Read: Disabled
		Enabled	1	Read: Enabled
J	RW PREGIONORA	z.idbica	<u>-</u>	Write '1' to Enable interrupt for PREGION[0].RA event
		C-+	4	See EVENTS_PREGION[0].RA
		Set	1	Enable Read Disabled
		Disabled	0 1	Read: Disabled
K	RW PREGION1WA	Enabled	1	Read: Enabled Write '1' to Enable interrupt for PREGION[1].WA event
IX	WAN LUCGIONIAMA			write 1 to chable interrupt for Predicin[1].WA event



Bit number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		l	LK JI H G F E D C B A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description
			See EVENTS_PREGION[1]. WA
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
L RW PREGIO	N1RA		Write '1' to Enable interrupt for PREGION[1].RA event
			See EVENTS_PREGION[1].RA
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

45.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number			31 30 29 28			23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
d				L K J		H G F E D C B A
Reset 0x0000				0 0 0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Fi		Value Id	Value			Description
A RW RE	EGION0WA					Write '1' to Disable interrupt for REGION[0].WA event
						See EVENTS_REGION[0].WA
		Clear	1			Disable
		Disabled	0			Read: Disabled
		Enabled	1			Read: Enabled
B RW RE	EGION0RA					Write '1' to Disable interrupt for REGION[0].RA event
						See EVENTS_REGION[0].RA
		Clear	1			Disable
		Disabled	0			Read: Disabled
		Enabled	1			Read: Enabled
C RW RE	EGION1WA					Write '1' to Disable interrupt for REGION[1].WA event
						See EVENTS_REGION[1].WA
		Clear	1			Disable
		Disabled	0			Read: Disabled
		Enabled	1			Read: Enabled
D RW RE	EGION1RA	21100100	-			Write '1' to Disable interrupt for REGION[1].RA event
						See EVENTS_REGION[1].RA
		Clear	1			Disable
		Disabled	0			Read: Disabled
5 DW D	CIONIZIA/A	Enabled	1			Read: Enabled
E RW RE	EGION2WA					Write '1' to Disable interrupt for REGION[2].WA event
						See EVENTS_REGION[2].WA
		Clear	1			Disable
		Disabled	0			Read: Disabled
		Enabled	1			Read: Enabled
F RW RE	EGION2RA					Write '1' to Disable interrupt for REGION[2].RA event
						See EVENTS_REGION[2].RA
		Clear	1			Disable
		Disabled	0			Read: Disabled
		Enabled	1			Read: Enabled
G RW RE	EGION3WA					Write '1' to Disable interrupt for REGION[3].WA event
						See EVENTS_REGION[3].WA
		Clear	1			Disable



Bit	number	31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		L k	(JI H G F E D C B A
Res	et 0x00000000	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field Value Id	Value	Description
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
Н	RW REGION3RA		Write '1' to Disable interrupt for REGION[3].RA event
			See EVENTS_REGION[3].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
I	RW PREGIONOWA		Write '1' to Disable interrupt for PREGION[0].WA event
			See EVENTS_PREGION[0].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
J	RW PREGIONORA		Write '1' to Disable interrupt for PREGION[0].RA event
			See EVENTS_PREGION[0].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
K	RW PREGION1WA		Write '1' to Disable interrupt for PREGION[1].WA event
			See EVENTS_PREGION[1].WA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
L	RW PREGION1RA		Write '1' to Disable interrupt for PREGION[1].RA event
			See EVENTS_PREGION[1].RA
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

45.1.4 NMIEN

Address offset: 0x320

Enable or disable non-maskable interrupt

Bitı	numbe	er		31 3	0 29	28 2	7 2	6 25	24	23 2	22 21	20	19 1	.8 1	7 16	15	14	13 1	2 13	1 10	9	8	7 6	5	4	3	2	1 0
Id							L I	(J	-1														H G	F	Е	D	C I	3 A
Res	et 0x0	0000000		0 0	0	0 (0 (0	0	0 (0 0	0	0 (0 (0	0	0	0 (0	0	0	0	0 0	0	0	0	0 (0 0
Id	RW	Field	Value Id	Valu	e					Desc	cripti	ion																
Α	RW	REGION0WA								Enab	ble o	r dis	able	non	n-ma	iska	ble	inter	rupt	t for	REC	OIG	۱[0]۱	WA				
										even	nt																	
										See	EVEN	VTS_	REG	ION	[0].V	NA												
			Disabled	0						Disal	able																	
			Enabled	1						Enab	ble																	
В	RW	REGIONORA								Enab	ble o	r dis	able	non	n-ma	iska	ble	inter	rupt	t for	REC	OIG	1[0].	RA				
										even	nt																	
										See	EVEN	VTS_	REG	ION	[0].F	RA												
			Disabled	0						Disal	able																	
			Enabled	1						Enab	ble																	
С	RW	REGION1WA								Enab	ble o	r dis	able	nor	n-ma	ska	ble	inter	rupt	t for	REC	OIG	۱[1].۱	WA				
										even	nt																	
										See	EVEN	VTS_	REG	ION	[1]. V	NA												
			Disabled	0						Disal	able																	
			Enabled	1						Enab	ble																	



Bit	numbe	er		31 30	29 28	3 27	26 2	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id						L	K	JI	H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0	0	0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value					Description
D	RW	REGION1RA							Enable or disable non-maskable interrupt for REGION[1].RA event See EVENTS_REGION[1].RA
			Disabled	0					Disable
			Enabled	1					Enable
E	RW	REGION2WA							Enable or disable non-maskable interrupt for REGION[2].WA event See EVENTS_REGION[2].WA
			Disabled	0					Disable
			Enabled	1					Enable
F	RW	REGION2RA							Enable or disable non-maskable interrupt for REGION[2].RA event
			Disabled	0					See EVENTS_REGION[2].RA
			Disabled Enabled	1					Disable Enable
G	RW	REGION3WA		-					Enable or disable non-maskable interrupt for REGION[3].WA event
									See EVENTS_REGION[3].WA
			Disabled	0					Disable
		250,011024	Enabled	1					Enable
Н	RW	REGION3RA							Enable or disable non-maskable interrupt for REGION[3].RA event See EVENTS_REGION[3].RA
			Disabled	0					Disable
			Enabled	1					Enable
I	RW	PREGIONOWA							Enable or disable non-maskable interrupt for PREGION[0].WA event
				_					See EVENTS_PREGION[0].WA
			Disabled	0					Disable
J	R\M	PREGIONORA	Enabled	1					Enable Enable or disable non-maskable interrupt for PREGION[0].RA
J		THE GIOTOLIA							event
			Disabled	0					See EVENTS_PREGION[0].RA Disable
			Enabled	1					Enable
K	RW	PREGION1WA							Enable or disable non-maskable interrupt for PREGION[1].WA event
									See EVENTS_PREGION[1].WA
			Disabled	0					Disable
			Enabled	1					Enable
L	RW	PREGION1RA							Enable or disable non-maskable interrupt for PREGION[1].RA event
									See EVENTS_PREGION[1].RA
			Disabled	0					Disable
			Enabled	1					Enable

45.1.5 NMIENSET

Address offset: 0x324

Enable non-maskable interrupt



					23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id L Reset 0x00000000					H G F E D C B A
rese Id		Field	Value Id	Value	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
A	RW	REGIONOWA	value lu	Value	Write '1' to Enable non-maskable interrupt for REGION[0].WA event
			6.1		See EVENTS_REGION[0].WA
			Set	0	Enable Pand Displied
			Disabled Enabled	1	Read: Disabled Read: Enabled
В	R\M/	REGIONORA	Eliabled	1	Write '1' to Enable non-maskable interrupt for REGION[0].RA
					event
					See EVENTS_REGION[0].RA
			Set	1	Enable Part Dischlad
			Disabled	0	Read: Disabled
_	D\A/	REGION1WA	Enabled	1	Read: Enabled Write '1' to Enable non-maskable interrupt for REGION[1].WA
С	RW	REGIONIWA			event
					See EVENTS_REGION[1].WA
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
D	RW	REGION1RA			Write '1' to Enable non-maskable interrupt for REGION[1].RA event
					See EVENTS_REGION[1].RA
			Set	1	Enable
			Disabled	0	Read: Disabled
	DIA	DECIONANA	Enabled	1	Read: Enabled
E	KVV	REGION2WA			Write '1' to Enable non-maskable interrupt for REGION[2].WA event
					See EVENTS_REGION[2].WA
			Set	1	Enable
			Disabled	0	Read: Disabled
-	DVA	DECIONADA	Enabled	1	Read: Enabled
F	KVV	REGION2RA			Write '1' to Enable non-maskable interrupt for REGION[2].RA event
					See EVENTS_REGION[2].RA
			Set	1	Enable
			Disabled	0	Read: Disabled
_			Enabled	1	Read: Enabled
G	RW	REGION3WA			Write '1' to Enable non-maskable interrupt for REGION[3].WA event
					See EVENTS_REGION[3].WA
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
Н	RW	REGION3RA			Write '1' to Enable non-maskable interrupt for REGION[3].RA event
					See EVENTS_REGION[3].RA
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
I	RW	PREGIONOWA			Write '1' to Enable non-maskable interrupt for PREGION[0].WA event



Bit number		31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		L K J I	H G F E D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
ld RW Field	Value Id	Value	Description
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
J RW PREGIONORA			Write '1' to Enable non-maskable interrupt for PREGION[0].RA
			event
			See EVENTS_PREGION[0].RA
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
K RW PREGION1WA			Write '1' to Enable non-maskable interrupt for PREGION[1].WA
			event
			See EVENTS_PREGION[1].WA
	Set	1	Enable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
L RW PREGION1RA			Write '1' to Enable non-maskable interrupt for PREGION[1].RA
			event
			Car EVENTS DESCION[4] DA
	Cot	1	See EVENTS_PREGION[1].RA Enable
	Set	1	
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled

45.1.6 NMIENCLR

Address offset: 0x328

Disable non-maskable interrupt

	umbe	r		31 30	0 29	28					23	22	21	20	19	18	17	16	15 1	14 1	L3 1	2 1	1 10	9	8					3 2		L O
Id							L	K J	J I	l																Н	G	F	E [) C	: В	3 A
Rese	t 0x0	0000000		0 0	0	0	0	0 () () (0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Valu	е					D)e	scri	ptic	on																		
Α	RW	REGION0WA								٧	۷r	rite '	'1' t	o D	isal	ole	non	-m	aska	able	int	erri	upt 1	or I	REGI	ON	[0].	WA				
										е	eve	ent																				
										S	ee	e <i>EV</i>	ΈN	TS_	REC	3101	N[0	1. W	'A													
			Clear	1						D	Dis	sable	е																			
			Disabled	0						R	Rea	ad: I	Disa	able	ed																	
			Enabled	1						R	Rea	ad: I	Ena	ble	d																	
В	RW	REGIONORA								٧	٧r	rite '	'1' t	o D	isal	ole	non	-m	aska	able	e int	erri	upt 1	or I	REGI	ON	[0].	RA				
										е	eve	ent																				
										S	ee	e <i>EV</i>	ΈN	TS_	REC	3101	N[0	l.R	4													
			Clear	1						D	Dis	sable	е																			
			Disabled	0						R	Rea	ad: I	Disa	able	ed																	
			Enabled	1						R	Rea	ad: I	Ena	ble	d																	
С	RW	REGION1WA								٧	۷r	rite '	'1' t	o D	isal	ole	non	-m	aska	able	int	errı	upt 1	or I	REGI	ON	[1].	WA				
										е	eve	ent																				
										S	ee	e <i>EV</i>	ΈN	TS_	REC	3101	N[1	1. W	'A													
			Clear	1						D	Dis	sable	е																			
			Disabled	0						R	Rea	ad: I	Disa	able	ed																	
			Enabled	1						R	Rea	ad: I	Ena	ble	d																	
D	RW	REGION1RA								٧	۷r	rite '	'1' t	o D	isal	ole	non	-m	aska	able	e int	erri	ıpt 1	or I	REGI	ON	[1].	RA				
										е	eve	ent																				



Bit	number		31 30 29 28 2	7 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				L K J I H G F E D C B A
Res	set 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Е	RW REGION2WA			Write '1' to Disable non-maskable interrupt for REGION[2].WA
				event
				See EVENTS_REGION[2].WA
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW REGION2RA			Write '1' to Disable non-maskable interrupt for REGION[2].RA
				event
				See EVENTS_REGION[2].RA
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW REGION3WA			Write '1' to Disable non-maskable interrupt for REGION[3].WA
				event
				See EVENTS_REGION[3].WA
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW REGION3RA			Write '1' to Disable non-maskable interrupt for REGION[3].RA
				event
				See EVENTS_REGION[3].RA
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
1	RW PREGIONOWA			Write '1' to Disable non-maskable interrupt for PREGION[0].WA
				event
				See EVENTS_PREGION[0].WA
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
J	RW PREGIONORA			Write '1' to Disable non-maskable interrupt for PREGION[0].RA
				event
				See EVENTS_PREGION[0].RA
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
K	RW PREGION1WA			Write '1' to Disable non-maskable interrupt for PREGION[1].WA
				event
				See EVENTS_PREGION[1].WA
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
L	RW PREGION1RA			Write '1' to Disable non-maskable interrupt for PREGION[1].RA
				event
				See EVENTS_PREGION[1].RA
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled



45.1.7 PERREGION[0].SUBSTATWA

Address offset: 0x400

Source of event/interrupt in region 0, write access detected while corresponding subregion was enabled for watching

Rit r	numbe	r		31 30 2	9 28 2	7 26 2	5 24	23 22 21 20	∩ 19 1	8 17 ·	16 15	14 13	12 1	1 10	9 8	7	6 5	. 4	3 :) 1
Id	idilibe	'						X W V L												
	et 0x0	000000						0 0 0 0												
Id	RW	Field	Value Id	Value				Description	1											
Α	RW	SR0						Subregion (0 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
В	RW	SR1						Subregion 1	1 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
С	RW	SR2						Subregion 2	2 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
D	RW	SR3						Subregion 3	3 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
E	RW	SR4						Subregion 4	4 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
F	RW	SR5						Subregion 5	5 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
G	RW	SR6						Subregion 6	6 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
Н	RW	SR7						Subregion 7	7 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) o	occurr	ed in 1	his su	bregi	ion						
I	RW	SR8						Subregion 8	8 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
J	RW	SR9						Subregion 9	9 in reg	gion 0	(write	'1' to	clear	r)						
			NoAccess	0				No write ac	ccess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
K	RW	SR10						Subregion 1	10 in re	gion	0 (wri	e '1' te	o clea	ar)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
L	RW	SR11						Subregion 1	11 in re	gion	0 (wri	e '1' te	o clea	ar)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
М	RW	SR12						Subregion 1	12 in re	gion	0 (wri	e '1' te	o clea	ar)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) o	occurr	ed in 1	his su	bregi	ion						
N	RW	SR13						Subregion 1	13 in re	gion	0 (wri	e '1' te	o clea	ar)						
			NoAccess	0				No write ac	ccess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) o	occurr	ed in 1	his su	bregi	ion						
0	RW	SR14						Subregion 1	14 in re	gion	0 (wri	e '1' t	o clea	ar)						
			NoAccess	0				No write ac	cess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in 1	his su	bregi	ion						
Р	RW	SR15						Subregion 1	15 in re	gion	0 (wri	e '1' te	o clea	ar)						
			NoAccess	0				No write ac	ccess o	ccurre	ed in t	his sub	regio	on						
			Access	1				Write acces	ss(es) c	occurr	ed in t	his su	bregi	ion						
Q	RW	SR16						Subregion 1	16 in re	egion	0 (wri	e '1' t	o clea	ar)						



Bitı	numbe	er		31 30	29 28	3 27	7 26	25 24	1 23	22 23	1 20	19	18	17 1	16 15	14	13 :	12 1	1 10	9	8	7	5 5	4	3	2 1	0
Id				f e	d c	b	а	Z Y	Х	w v	/ U	Т	S	R	Q P	0	N	M L	_ K	J	1 1	+ (3 F	Е	D	СВ	Α
Res	et 0x0	0000000		0 0	0 0	0	0	0 0	0	0 0	0	0	0	0	0 0	0	0	0 0	0	0	0	0	0 0	0	0	0 0	0
Id	RW	Field	Value Id	Value					Des	script	tion																
			NoAccess	0					No	write	e ac	cess	occi	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
R	RW	SR17							Sub	bregio	on 1	.7 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
S	RW	SR18							Sub	bregio	on 1	.8 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
Т	RW	SR19							Sub	bregio	on 1	.9 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
U	RW	SR20							Sub	bregio	on 2	0 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
V	RW	SR21							Sub	bregio	on 2	1 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occi	urre	d in	this	subr	egic	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
W	RW	SR22							Sub	bregio	on 2	2 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occi	urre	d in	this	subr	egic	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
Χ	RW	SR23							Sub	bregio	on 2	3 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
Υ	RW	SR24							Sub	bregio	on 2	4 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
Z	RW	SR25							Sub	bregio	on 2	5 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occi	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
а	RW	SR26							Sub	bregio	on 2	6 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
b	RW	SR27							Sub	bregio	on 2	7 in	regi	ion () (wr	ite '	1' to	clea	ir)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
C	RW	SR28							Sub	bregio	on 2	8 in	regi	ion () (wr	ite '	1' to	clea	ir)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
d	RW	SR29							Sub	bregio	on 2	.9 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	occ	curr	ed in	this	sub	regi	on								
e	RW	SR30							Suk	bregio	on 3	0 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	oco	curr	ed in	this	sub	regi	on								
f	RW	SR31							Sub	bregio	on 3	1 in	regi	ion () (wr	ite '	1' to	clea	ar)								
			NoAccess	0					No	write	e ac	cess	occ	urre	d in	this	subr	egio	n								
			Access	1					Wr	ite ac	ces	s(es)	occ	curr	ed in	this	sub	regi	on								

45.1.8 PERREGION[0].SUBSTATRA

Address offset: 0x404

Source of event/interrupt in region 0, read access detected while corresponding subregion was enabled for watching



Bit r	numbe	er		31 30	29 28	27 26	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id								/ X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
Α	RW	SR0						Subregion 0 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
В	RW	SR1						Subregion 1 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
С	RW	SR2						Subregion 2 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
D	RW	SR3						Subregion 3 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Е	RW	SR4						Subregion 4 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
F	RW	SR5						Subregion 5 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
G	RW	SR6						Subregion 6 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Н	RW	SR7						Subregion 7 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
I	RW	SR8						Subregion 8 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
J	RW	SR9						Subregion 9 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
K	RW	SR10						Subregion 10 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
L	RW	SR11						Subregion 11 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
М	RW	SR12						Subregion 12 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
N	RW	SR13						Subregion 13 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
0	RW	SR14						Subregion 14 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Р	RW	SR15						Subregion 15 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Q	RW	SR16						Subregion 16 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
R	RW	SR17						Subregion 17 in region 0 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
S	RW	SR18						Subregion 18 in region 0 (write '1' to clear)



Reset 00000000000000000000000000000000000
id RW Field Value Id Value Description I NoAccess 0 No read access occurred in this subregion I RW RS19 Access 1 Read access(es) occurred in this subregion I RW SR19 NoAccess 0 No read access occurred in this subregion I RW RS20 L Subregion 20 in region 0 (write "1" to clear) NoAccess 0 No read access occurred in this subregion RW RW RS21 Subregion 20 in region 0 (write "1" to clear) NoAccess 1 Read access(es) occurred in this subregion No Read access occurred in this subregion No read access occurred in this subregion W RW RS22 No Access 0 No read access occurred in this subregion W RW RS23 No Read access occurred in this subregion No read access occurred in this subregion W RW RS23 No Read access(es) occurred in this subregion No read access occurred in this subregion Y RW RS24 Subregion 24 in re
id RW Field Value Id Value Description I NoAccess 0 No read access occurred in this subregion I RW RS19 Access 1 Read access(es) occurred in this subregion I RW SR19 NoAccess 0 No read access occurred in this subregion I RW RS20 L Subregion 20 in region 0 (write "1" to clear) NoAccess 0 No read access occurred in this subregion RW RW RS21 Subregion 20 in region 0 (write "1" to clear) NoAccess 1 Read access(es) occurred in this subregion No Read access occurred in this subregion No read access occurred in this subregion W RW RS22 No Access 0 No read access occurred in this subregion W RW RS23 No Read access occurred in this subregion No read access occurred in this subregion W RW RS23 No Read access(es) occurred in this subregion No read access occurred in this subregion Y RW RS24 Subregion 24 in re
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion T RW SA19 NoAccess 0 No read access occurred in this subregion No Read access occurred in this subregion No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access
T RW SR19 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion Occurred In this subr
T RW SR19 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion Occurred In this sub
No Access 1 Read access(es) occurred in this subregion
U RW SR20 NoAccess 0 No read access occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion V RW SR21 SR21 Subregion 21 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion W RW SR22 Subregion 22 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion X RW SR23 Subregion 22 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion X No Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion X No Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 2 Subregion 25 in region 0 (write '1' to clear) No read access occurred in this subregion Access 3 Subregion 26 in region 0 (write '1' to clear) No read access occurred in this subregion Access 3 Subregion 26 in region 0 (write '1' to clear)
Access 1 Read access(es) occurred in this subregion V RW SR21 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion No read access occurred in this subregion No RW SR22 NoAccess 0 No read access occurred in this subregion Access 1 Read access occurred in this subregion No Read access occurred in this subregion
V RW RW RW SR21 Subregion 21 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion W RW
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion W RW SR22 Subregion 22 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion X RW SR23 Subregion 23 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion X NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion X RW SR24 Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion X Subregion 24 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion X RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion X RW SR26 Subregion 26 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion X RW SR26 Subregion 26 in region 0 (write '1' to clear)
Access 1 Read access(es) occurred in this subregion W RW SR22 Subregion 22 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion X RW SR23 Subregion 23 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Y RW SR24 SR24 Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion X SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion X Read access(es) occurred in this subregion X Read access(es) occurred in this subregion X Read access occurred in this subregion X Subregion 25 in region 0 (write '1' to clear) X Subregion 26 in region 0 (write '1' to clear)
W RW SR22 Subregion 22 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 23 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion No Read access occurred in this subregion No Read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion No Read access(es) occurred in this subregion Read access(es) occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion X RW SR23 Subregion 23 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Y RW SR24 Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion X Subregion 24 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion X RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion X RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 1 Read access(es) occurred in this subregion X SR26 Subregion 26 in region 0 (write '1' to clear)
Access 1 Read access(es) occurred in this subregion X RW SR23 Subregion 23 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion X RW SR24 SR24 Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion X No Read access(es) occurred in this subregion No No read access occurred in this subregion X RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion X No Read access(es) occurred in this subregion X RW SR25 Subregion 25 in region 0 (write '1' to clear) X No Read access occurred in this subregion X Read access(es) occurred in this subregion X SR26 Subregion 26 in region 0 (write '1' to clear)
X RW SR23 NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Y RW SR24 NoAccess 0 No read access occurred in this subregion NoAccess 1 Read access(es) occurred in this subregion No read access occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion Read access(es) occurred in this subregion No read access occurred in this subregion Subregion 26 in region 0 (write '1' to clear) Subregion 26 in region 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Y RW SR24 Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Access 1 Read access(es) occurred in this subregion Z RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 25 in region 0 (write '1' to clear) NoAccess Subregion 26 in region 0 (write '1' to clear)
Access 1 Read access(es) occurred in this subregion Y RW SR24 SR24 SR24 SR25 Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion No Read access(es) occurred in this subregion No Read access(es) occurred in this subregion Read access(es) occurred in this subregion Subregion 26 in region 0 (write '1' to clear)
Y RW SR24 Subregion 24 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Z RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion Subregion 26 in region 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Z RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion Subregion 26 in region 0 (write '1' to clear)
Access 1 Read access(es) occurred in this subregion Z RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Read access(es) occurred in this subregion Subregion 26 in region 0 (write '1' to clear)
Z RW SR25 Subregion 25 in region 0 (write '1' to clear) NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 26 in region 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion Subregion 26 in region 0 (write '1' to clear)
Access 1 Read access(es) occurred in this subregion a RW SR26 Subregion 26 in region 0 (write '1' to clear)
a RW SR26 Subregion 26 in region 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion
Access 1 Read access(es) occurred in this subregion
b RW SR27 Subregion 27 in region 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion
Access 1 Read access(es) occurred in this subregion
c RW SR28 Subregion 28 in region 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion
Access 1 Read access(es) occurred in this subregion
d RW SR29 Subregion 29 in region 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion
Access 1 Read access(es) occurred in this subregion
e RW SR30 Subregion 30 in region 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion
Access 1 Read access(es) occurred in this subregion
f RW SR31 Subregion 31 in region 0 (write '1' to clear)
NoAccess 0 No read access occurred in this subregion Access 1 Read access(es) occurred in this subregion

45.1.9 PERREGION[1].SUBSTATWA

Address offset: 0x408

Source of event/interrupt in region 1, write access detected while corresponding subregion was enabled for watching

Bit	numbe	er		3:	1 30	29	28	27	7 26	25	24	23	22 :	21 2	20 1	.9 1	.8 1	7 16	5 15	14	13 3	12 :	11 1	0 9	8	7	6	5	4	3	2	1 0
Id				f	е	d	С	b	а	Z	Υ	Х	W	V	U .	Т :	S R	Q	P	0	N	M	L I	(J	-1	Н	G	F	Ε	D	С	3 A
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value					De	scrip	otio	n																				
Α	RW	SR0		Value					Sul	oreg	ion	0 ir	re	gion	1 (writ	e '1'	to c	lea	r)												
			NoAccess	0					No	wri	te a	cce	ss o	ccu	rred	in t	his	subr	egi	on												
			Access	1					Wr	ite a	ессе	ess(e	es) (occu	irre	d in	this	sub	reg	ion												



Rit r	numbe	or .		31 30	29 28	27	26.2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	iuiiibo	-1							X W V U T S R Q P O N M L K J I H G F E D C B A
	et Ox0	0000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
В	RW	SR1							Subregion 1 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
С	RW	SR2							Subregion 2 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
D	RW	SR3							Subregion 3 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Е	RW	SR4							Subregion 4 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
F	RW	SR5							Subregion 5 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
G	RW	SR6							Subregion 6 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Н	RW	SR7							Subregion 7 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
I	RW	SR8							Subregion 8 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
J	RW	SR9							Subregion 9 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
K	RW	SR10							Subregion 10 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
	DIA	CD11	Access	1					Write access(es) occurred in this subregion
L	KW	SR11	NaAssass	0					Subregion 11 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
N 4	D\A/	CD12	Access	1					Write access(es) occurred in this subregion
М	KVV	SR12	NoAccors	0					Subregion 12 in region 1 (write '1' to clear)
			NoAccess Access	0					No write access occurred in this subregion Write access(es) occurred in this subregion
N	R\M	SR13	Access	1					Subregion 13 in region 1 (write '1' to clear)
IN	IVV	31(13	NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
0	RW	SR14	recess	-					Subregion 14 in region 1 (write '1' to clear)
_			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Р	RW	SR15		-					Subregion 15 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Q	RW	SR16							Subregion 16 in region 1 (write '1' to clear)
-			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
R	RW	SR17							Subregion 17 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
S	RW	SR18							Subregion 18 in region 1 (write '1' to clear)
			NoAccess	0					No write access occurred in this subregion
			Access	1					Write access(es) occurred in this subregion
Т	RW	SR19							Subregion 19 in region 1 (write '1' to clear)



Bit number		31 30 29 28 27 26 25 24 23	22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			W V U T S R Q P O N M L K J I H G F E D C B A
Reset 0x00000000			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id		scription
	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
U RW SR20			pregion 20 in region 1 (write '1' to clear)
0 1111 51120	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
V RW SR21	7.000055		pregion 21 in region 1 (write '1' to clear)
	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
W RW SR22	Access		pregion 22 in region 1 (write '1' to clear)
VV IVVV SIVEE	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
X RW SR23	Access		pregion 23 in region 1 (write '1' to clear)
A 111V 31123	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
Y RW SR24	Access		pregion 24 in region 1 (write '1' to clear)
1 1111 31124	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
Z RW SR25	Access		pregion 25 in region 1 (write '1' to clear)
Z 1(W 31(2)	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
a RW SR26	Access		pregion 26 in region 1 (write '1' to clear)
a 111V 31120	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
b RW SR27	Access		pregion 27 in region 1 (write '1' to clear)
D INV SINZ/	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
c RW SR28	Access		pregion 28 in region 1 (write '1' to clear)
C NW 3NZO	NoAccess		write access occurred in this subregion
	Access		ite access(es) occurred in this subregion
d RW SR29	Access		pregion 29 in region 1 (write '1' to clear)
u KW SK29	No Assess		
	NoAccess		write access occurred in this subregion
o DW CD30	Access		ite access(es) occurred in this subregion
e RW SR30	No Appears		pregion 30 in region 1 (write '1' to clear)
	NoAccess		write access occurred in this subregion
f DW CD34	Access		ite access(es) occurred in this subregion
f RW SR31	No A		pregion 31 in region 1 (write '1' to clear)
	NoAccess		write access occurred in this subregion
	Access	1 Wri	ite access(es) occurred in this subregion

45.1.10 PERREGION[1].SUBSTATRA

Address offset: 0x40C

Source of event/interrupt in region 1, read access detected while corresponding subregion was enabled for watching

Bit nu	ımbe	r		31	30	29	28 2	27 2	26 2	25 2	24 2	3 2	2 21	20	19	18	17 1	16	15 1	4 1	3 12	11	10	9	8	7 (6 5	4	3	2	1 0
Id				f	e	d	С	b	a Z	Z	Υ 2	X V	V V	U	Т	S	R	Q	Р (1 C	I M	L	K	J	1 1	1 (G F	E	D	С	в А
Reset	0x0	0000000		0	0	0	0	0	0 (0	0 (0 (0	0	0	0	0	0	0 (0 0	0	0	0	0	0 () (0 0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						C	esc	ripti	on																	
Α	RW	SR0									S	ubr	egio	n 0	in r	egic	n 1	(w	rite	'1' t	o cle	ear)									
			NoAccess	0							١	lo r	ead	ассе	ess (occi	ırre	d in	thi	s su	breg	gion									
			Access	1							R	lead	acc	ess((es)	occ	urre	d i	n th	is su	ıbre	gion	1								
В	RW	SR1									S	ubr	egio	n 1	in r	egic	n 1	(w	rite	'1' t	o cle	ear)									
			NoAccess	0							١	lo r	ead	ассе	ess (occi	ırre	d in	thi	s su	breg	gion									
			Access	1							R	lead	acc	ess((es)	occ	urre	d i	n th	is sı	ıbre	gion	1								



Bit r	numbe	er		31 30	29 28	27 26	25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	Z Y	'X W V U T S R Q P O N M L K J I H G F E D C B A
Res	et 0x0	0000000		0 0	0 0	0 0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value				Description
С	RW	SR2						Subregion 2 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
D	RW	SR3						Subregion 3 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Е	RW	SR4						Subregion 4 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
F	RW	SR5						Subregion 5 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
G	RW	SR6						Subregion 6 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Н	RW	SR7						Subregion 7 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
I	RW	SR8						Subregion 8 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
J	RW	SR9						Subregion 9 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
K	RW	SR10						Subregion 10 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
L	RW	SR11						Subregion 11 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
М	RW	SR12						Subregion 12 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
N	RW	SR13						Subregion 13 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
0	RW	SR14						Subregion 14 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Р	RW	SR15						Subregion 15 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Q	RW	SR16						Subregion 16 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
R	RW	SR17						Subregion 17 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
S	RW	SR18						Subregion 18 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
Т	RW	SR19						Subregion 19 in region 1 (write '1' to clear)
			NoAccess	0				No read access occurred in this subregion
			Access	1				Read access(es) occurred in this subregion
U	RW	SR20						Subregion 20 in region 1 (write '1' to clear)



Bitı	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Res	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
٧	RW SR21		Subregion 21 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
W	RW SR22		Subregion 22 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Χ	RW SR23		Subregion 23 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Υ	RW SR24		Subregion 24 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
Z	RW SR25		Subregion 25 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
a	RW SR26		Subregion 26 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
b	RW SR27		Subregion 27 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
С	RW SR28		Subregion 28 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
d	RW SR29		Subregion 29 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
e	RW SR30		Subregion 30 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion
f	RW SR31		Subregion 31 in region 1 (write '1' to clear)
		NoAccess	0 No read access occurred in this subregion
		Access	1 Read access(es) occurred in this subregion

45.1.11 REGIONEN

Address offset: 0x510

Enable/disable regions watch

Bit r	iumbe	r		31	30 2	29 2	28 2	7 26	5 25	5 24	23	3 22	21	20	19 1	18 1	l7 1	6 1	15 :	14 1	13 1	2 11	. 10	9	8	7	6	5	4 3	3 2	1	0
Id							L	. K	J	-1																Н	G	F	E [) С	В	Α
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 ()	0	0	0 (0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Val	lue						De	escri	ptio	n																		
Α	RW	RGN0WA									En	able	e/dis	ab	le w	rite	aco	es	s w	atcl	n in	regi	on[C)]								
			Disable	0							Dis	sabl	e wi	ite	acc	ess	wat	tch	in	this	reg	ion										
			Enable	1							En	able	e wr	ite	acce	ess	wat	ch	in t	his	regi	on										
В	RW	RGNORA									En	able	e/dis	ab	le re	ead	acc	ess	wa	atch	in r	egio	n[0]	l								
			Disable	0							Dis	sabl	e re	ad a	acce	ess	wat	ch i	in t	his	regi	on										
			Enable	1							En	able	e rea	ıd a	ссе	ss v	vato	h i	n th	nis r	egic	n										
С	RW	RGN1WA									En	able	e/dis	ab	le w	rite	acc	es	s w	atcl	n in	regi	on[1	.]								
			Disable	0							Dis	sabl	e wi	ite	acc	ess	wat	ch	in	this	reg	ion										
			Enable	1							En	able	e wr	ite	ассе	ess	wat	ch	in t	his	regi	on										
D	RW	RGN1RA									En	able	e/dis	ab	le re	ead	acc	ess	wa	atch	in r	egio	n[1]	l								



Bitı	numbe	er		33	L 30	29	28 2	7 2	6 25	5 24	1 23	3 2	2 21	1 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id								LI	(J	-1																	н	G	F	Е	D	C E	ВА
Res	et 0x0	0000000		0	0	0	0 (0 (0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	Field	Value Id	V	alue						D	esc	ript	ion																			
			Disable	0							Di	isal	ble r	reac	laco	ess	wa	tch	in 1	this	re	gior	ı										
			Enable	1							Er	nab	le r	ead	acc	ess	wat	ch	in t	his	reg	ion											
Е	RW	RGN2WA									Er	nab	ole/c	disa	ble v	writ	e ac	ces	s w	/ato	h iı	ı re	gio	n[2	l								
			Disable	0							Di	isal	ble v	writ	e ac	ces	s wa	atch	in	thi	re	gio	n										
			Enable	1							Er	nab	le v	vrite	aco	cess	wa	tch	in	this	re	gioi	า										
F	RW	RGN2RA									Er	nab	ole/c	disa	ble ı	eac	d ac	ces	s w	atc	n in	re	gior	[2]									
			Disable	0							Di	isal	ble r	reac	laco	ess	wa	tch	in	this	re	gior	ı										
			Enable	1							Er	nab	le r	ead	acc	ess	wat	ch	in t	his	reg	ion											
G	RW	RGN3WA									Er	nab	ole/c	disa	ble v	writ	e ac	ces	s w	/ato	h iı	ı re	gio	n[3	ı								
			Disable	0							Di	isal	ble v	writ	e ac	ces	s wa	atch	in	thi	re	gio	n										
			Enable	1							Er	nab	ole v	vrite	e acc	ess	wa	tch	in	this	re	gioi	า										
Н	RW	RGN3RA									Er	nab	ole/c	disa	ble ı	eac	d ac	ces	s w	atc	n in	re	gior	[3]									
			Disable	0							Di	isal	ble r	reac	laco	ess	wa	tch	in	this	re	gior	ı										
			Enable	1							Er	nab	le r	ead	acc	ess	wat	ch	in t	his	reg	ion											
1	RW	PRGNOWA									Er	nab	ole/c	disa	ble v	writ	e ac	ces	s w	/ato	h iı	n Pl	REG	101	I[0]	j							
			Disable	0							Di	isal	ble v	writ	e ac	ces	s wa	atch	in	thi	s PF	REG	ION	ı									
			Enable	1							Er	nab	ole v	vrite	e acc	ess	wa	tch	in	this	PR	EG	ION										
J	RW	PRGNORA									Er	nab	ole/c	disa	ble ı	eac	d ac	ces	s w	atc	n in	PR	EGI	ON	[0]								
			Disable	0							Di	isal	ble r	reac	laco	ess	wa	tch	in	this	PR	EG	ON										
			Enable	1							Er	nab	le r	ead	acc	ess	wat	ch	in t	his	PRI	GI	ON										
K	RW	PRGN1WA									Er	nab	ole/c	disa	ble v	writ	e ac	ces	s w	/ato	h iı	n Pl	REG	101	I[1]	j							
			Disable	0							Di	isal	ble v	writ	e ac	ces	s wa	atch	in	thi	s PF	REG	ION	ı									
			Enable	1							Er	nab	ole v	vrite	aco	ess	wa	tch	in	this	PR	EG	ION										
L	RW	PRGN1RA									Er	nab	ole/c	disa	ble ı	eac	dac	ces	s w	atc	n in	PR	EGI	ON	[1]								
			Disable	0							Di	isal	ble r	reac	laco	ess	wa	tch	in	this	PR	EGI	ON										
			Enable	1							Er	nab	le r	ead	acc	ess	wat	ch	in t	his	PRI	GI	ON										

45.1.12 REGIONENSET

Address offset: 0x514 Enable regions watch

Bit	numb	er		31 3	30 29	28	27	26	25	24	23 2	22 2	21 2	0 1	9 18	17	16	15	14 :	13 1:	2 11	. 10	9	8	7	6	5	4	3 2	1	0
Id							L	K	J	1															Н	G	F	Е	D C	В	Α
Res	et 0x0	0000000		0	0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Valu	ıe						Des	crip	otion	,																	
Α	RW	RGN0WA									Enal	ble	writ	e a	cces	s w	atch	in ı	regi	on[0]										
			Set	1							Enal	ble	writ	e a	cces	s w	atch	in t	this	regi	on										
			Disabled	0							Writ	te a	cces	ss w	atcl	n in	this	reg	ion	is di	sabl	ed									
			Enabled	1							Writ	te a	cces	ss w	atcl	n in	this	reg	ion	is er	nabl	ed									
В	RW	RGN0RA									Enal	ble	reac	d ac	cess	wa	tch	in r	egic	n[0]											
			Set	1							Enal	ble	reac	d ac	cess	wa	tch	in t	his ı	regio	n										
			Disabled	0							Read	ıd a	cces	s w	atch	in t	his	regi	on i	s dis	able	ed									
			Enabled	1							Read	ıd ad	cces	s w	atch	in t	his	regi	on i	is en	able	d									
С	RW	RGN1WA									Enal	ble	writ	e a	cces	s w	atch	inı	regi	on[1]										
			Set	1							Enal	ble	writ	e a	cces	s w	atch	in t	this	regi	on										
			Disabled	0							Writ	te a	cces	ss w	atcl	n in	this	reg	ion	is di	sabl	ed									
			Enabled	1							Writ	te a	cces	ss w	atcl	n in	this	reg	ion	is er	nabl	ed									
D	RW	RGN1RA									Enal	ble	reac	d ac	cess	wa	tch	in r	egic	n[1]											
			Set	1							Enal	ble	reac	d ac	cess	wa	tch	in t	his ı	regio	n										
			Disabled	0							Read	ıd ad	cces	s w	atch	in t	his	regi	on i	s dis	able	ed									
			Enabled	1							Read	ıd a	cces	s w	atch	in t	his	regi	on i	is en	able	d									
E	RW	RGN2WA									Enal	ble	writ	e a	cces	s w	atch	inı	regi	on[2]										
			Set	1							Enal	ble	writ	e a	cces	s w	atch	in t	this	regi	on										
			Disabled	0							Writ	te a	icces	ss w	atcl	n in	this	reg	ion	is di	sabl	ed									



Bit	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			L K J I	H G F E D C B A
Res	set 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value	Description
		Enabled	1	Write access watch in this region is enabled
F	RW RGN2RA			Enable read access watch in region[2]
		Set	1	Enable read access watch in this region
		Disabled	0	Read access watch in this region is disabled
		Enabled	1	Read access watch in this region is enabled
G	RW RGN3WA			Enable write access watch in region[3]
		Set	1	Enable write access watch in this region
		Disabled	0	Write access watch in this region is disabled
		Enabled	1	Write access watch in this region is enabled
Н	RW RGN3RA			Enable read access watch in region[3]
		Set	1	Enable read access watch in this region
		Disabled	0	Read access watch in this region is disabled
		Enabled	1	Read access watch in this region is enabled
1	RW PRGN0WA			Enable write access watch in PREGION[0]
		Set	1	Enable write access watch in this PREGION
		Disabled	0	Write access watch in this PREGION is disabled
		Enabled	1	Write access watch in this PREGION is enabled
J	RW PRGNORA			Enable read access watch in PREGION[0]
		Set	1	Enable read access watch in this PREGION
		Disabled	0	Read access watch in this PREGION is disabled
		Enabled	1	Read access watch in this PREGION is enabled
K	RW PRGN1WA			Enable write access watch in PREGION[1]
		Set	1	Enable write access watch in this PREGION
		Disabled	0	Write access watch in this PREGION is disabled
		Enabled	1	Write access watch in this PREGION is enabled
L	RW PRGN1RA			Enable read access watch in PREGION[1]
		Set	1	Enable read access watch in this PREGION
		Disabled	0	Read access watch in this PREGION is disabled
		Enabled	1	Read access watch in this PREGION is enabled

45.1.13 REGIONENCLR

Address offset: 0x518 Disable regions watch

Bit	numb	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				LKJI	H G F E D C B A
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value	Description
Α	RW	RGN0WA			Disable write access watch in region[0]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
В	RW	RGN0RA			Disable read access watch in region[0]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled
С	RW	RGN1WA			Disable write access watch in region[1]
			Clear	1	Disable write access watch in this region
			Disabled	0	Write access watch in this region is disabled
			Enabled	1	Write access watch in this region is enabled
D	RW	RGN1RA			Disable read access watch in region[1]
			Clear	1	Disable read access watch in this region
			Disabled	0	Read access watch in this region is disabled
			Enabled	1	Read access watch in this region is enabled



Bit	numbe	er		31 30 29 28	27 26 25 24	\$ 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					L K J I	H G F E D C B A
Res	et 0x0	0000000		0 0 0 0	0 0 0 0	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
Id	RW	Field	Value Id	Value		Description
Ε	RW	RGN2WA				Disable write access watch in region[2]
			Clear	1		Disable write access watch in this region
			Disabled	0		Write access watch in this region is disabled
			Enabled	1		Write access watch in this region is enabled
F	RW	RGN2RA				Disable read access watch in region[2]
			Clear	1		Disable read access watch in this region
			Disabled	0		Read access watch in this region is disabled
			Enabled	1		Read access watch in this region is enabled
G	RW	RGN3WA				Disable write access watch in region[3]
			Clear	1		Disable write access watch in this region
			Disabled	0		Write access watch in this region is disabled
			Enabled	1		Write access watch in this region is enabled
Н	RW	RGN3RA				Disable read access watch in region[3]
			Clear	1		Disable read access watch in this region
			Disabled	0		Read access watch in this region is disabled
			Enabled	1		Read access watch in this region is enabled
1	RW	PRGN0WA				Disable write access watch in PREGION[0]
			Clear	1		Disable write access watch in this PREGION
			Disabled	0		Write access watch in this PREGION is disabled
			Enabled	1		Write access watch in this PREGION is enabled
J	RW	PRGNORA				Disable read access watch in PREGION[0]
			Clear	1		Disable read access watch in this PREGION
			Disabled	0		Read access watch in this PREGION is disabled
			Enabled	1		Read access watch in this PREGION is enabled
K	RW	PRGN1WA				Disable write access watch in PREGION[1]
			Clear	1		Disable write access watch in this PREGION
			Disabled	0		Write access watch in this PREGION is disabled
			Enabled	1		Write access watch in this PREGION is enabled
L	RW	PRGN1RA				Disable read access watch in PREGION[1]
			Clear	1		Disable read access watch in this PREGION
			Disabled	0		Read access watch in this PREGION is disabled
			Enabled	1		Read access watch in this PREGION is enabled

45.1.14 REGION[0].START

Address offset: 0x600 Start address for region 0

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW START		Start address for region

45.1.15 REGION[0].END

Address offset: 0x604 End address of region 0

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0											
Id	A A A A A A A A A A A A A A A A A A A											
Reset 0x00000000	$\begin{smallmatrix} & & & & & & & & & & & & & & & & & & &$											
ld RW Field Value Id	Value Description											
A RW END	End address of region.											



45.1.16 REGION[1].START

Address offset: 0x610 Start address for region 1

Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	A A A A A A A A A A A A A A A A A A A
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
A RW START	Start address for region

45.1.17 REGION[1].END

Address offset: 0x614 End address of region 1

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW END		End address of region.

45.1.18 REGION[2].START

Address offset: 0x620 Start address for region 2

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	4 А
Re	set 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0
Id	RW	/ Field	Value Id	Va	lue							De	scri	ptic	on																			
Α	RW	START		Start address for regi											gior	ı																		

45.1.19 REGION[2].END

Address offset: 0x624 End address of region 2

-	Bit numb	er			31	. 30	29	28	27	26	25	24	23	22	21	20 :	19 1	l8 1	7 1	6 1	5 14	13	12	11	10	9	8	7	6	5 4	4 3	3 2	1	0
1	d				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ Α	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α.	Α.	A A	Δ ,	A	Α	Α
ı	Reset 0x	00	000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0
ı	d RW	,	Field	Value Id	Va	llue	•						Des	cri	ptic	n																		
7	A RW	,	END										Enc	l ad	ldre	SS C	of re	gio	n.															

45.1.20 REGION[3].START

Address offset: 0x630 Start address for region 3

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value Description
A RW START		Start address for region

45.1.21 REGION[3].END

Address offset: 0x634 End address of region 3



Bit r	iumbe	er		31	30	29	28	27	26	25	24	23	22 :	21	20	19	18	17	16	15	14	13 1	12 :	11 1	0 9	9 8	8 7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	۱ ۸	4 <i>A</i>	. Д	Α	Α	Α	Α	А А
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0) () (0 0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	otic	n																		
Α	RW	END										Enc	l ad	dre	ss (of re	egic	on.															

45.1.22 PREGION[0].START

Address offset: 0x6C0

Reserved for future use

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	١,	4 А
Res	et 0x(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 0
Id	d RW Field Value Id		Va	lue							De	scr	pti	on																				
	_											_			,	٠.																		

A R START Reserved for future use

45.1.23 PREGION[0].END

Address offset: 0x6C4

Reserved for future use

Bitı	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1)
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	Α	Δ
Res	et Ox(0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0)
Id	RW	Field	Value Id	Va	lue							De	scr	pti	on																				ı
Α	R	END										Re	ser	ved	for	fut	ure	use	e																7

45.1.24 PREGION[0].SUBS

Address offset: 0x6C8 Subregions of region 0

Bit r	numbe	er		31	30 :	29 2	28 2	7 26	5 25	5 24	23	22 :	21 :	20 1	19 1	18 1	7 1	6 1	5 14	1 13	12	11	10 9	9 :	8 7	6	5	4	3	2 1	. 0
Id				f	e	d	c b	а	Z	Υ	Х	W	V	U .	т :	S I	R C	Q P	C	N	М	L	Κ.	J	I H	G	F	Ε	D	СВ	3 A
Res	et 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0 (0 (0 (0	0	0	0	0	0 (0 (0 0	0	0	0	0	0 0	0
Id	RW	Field	Value Id	Va	lue						De	escrip	otio	on																	
Α	RW	SR0									Inc	clude	or	exc	lud	e sı	ıbre	gio	n 0	in re	gio	n									
			Exclude	0							Ex	clude	е																		
			Include	1							Inc	clude	è																		
В	RW	SR1									Inc	clude	or	exc	lud	e sı	ıbre	gio	n 1	in re	gio	n									
			Exclude	0							Ex	clude	е																		
			Include	1							Inc	clude	9																		
С	RW	SR2									Inc	clude	or	exc	lud	e sı	ıbre	gio	n 2	in re	gio	n									
			Exclude	0							Ex	clude	е																		
			Include	1							Inc	clude	9																		
D	RW	SR3									Inc	clude	or	exc	lud	e sı	ıbre	gio	n 3	in re	gio	n									
			Exclude	0							Ex	clude	е																		
			Include	1							Inc	clude	9																		
Ε	RW	SR4									Inc	clude	or	exc	lud	e sı	ıbre	gio	n 4	in re	gio	n									
			Exclude	0							Ex	clude	е																		
			Include	1							Inc	clude	è																		
F	RW	SR5									Inc	clude	or	exc	lud	e sı	ıbre	gio	n 5	in re	gio	n									
			Exclude	0							Ex	clude	е																		
			Include	1							Inc	clude	9																		
G	RW	SR6									Inc	clude	or	exc	lud	e sı	ıbre	gio	n 6	in re	gio	n									
			Exclude	0							Ex	clude	е																		
			Include	1							Inc	clude	9																		



Rit n	iumbe	er .		31 30	29 28	27	26.2	5 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		-							X W V U T S R Q P O N M L K J I H G F E D C B A
Rese	et 0x0	0000000							0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
Н	RW	SR7							Include or exclude subregion 7 in region
			Exclude	0					Exclude
			Include	1					Include
I	RW	SR8							Include or exclude subregion 8 in region
			Exclude	0					Exclude
			Include	1					Include
J	RW	SR9							Include or exclude subregion 9 in region
			Exclude	0					Exclude
			Include	1					Include
K	RW	SR10							Include or exclude subregion 10 in region
			Exclude	0					Exclude
			Include	1					Include
L	RW	SR11		_					Include or exclude subregion 11 in region
			Exclude	0					Exclude
N 4	D) 1 1	CD12	Include	1					Include
М	кW	SR12	Evaluda	0					Include or exclude subregion 12 in region
			Exclude	0					Exclude Include
NI	D\A/	CD12	Include	1					
N	KVV	SR13	Exclude	0					Include or exclude subregion 13 in region Exclude
			Include	1					Include
0	R\M/	SR14	include	1					Include or exclude subregion 14 in region
Ü	11.44	31(14	Exclude	0					Exclude
			Include	1					Include
Р	RW	SR15		_					Include or exclude subregion 15 in region
			Exclude	0					Exclude
			Include	1					Include
Q	RW	SR16							Include or exclude subregion 16 in region
			Exclude	0					Exclude
			Include	1					Include
R	RW	SR17							Include or exclude subregion 17 in region
			Exclude	0					Exclude
			Include	1					Include
S	RW	SR18							Include or exclude subregion 18 in region
			Exclude	0					Exclude
			Include	1					Include
Т	RW	SR19							Include or exclude subregion 19 in region
			Exclude	0					Exclude
			Include	1					Include
U	RW	SR20		_					Include or exclude subregion 20 in region
			Exclude	0					Exclude
	P 1	5024	Include	1					Include
V	RW	SR21	5.1.1	_					Include or exclude subregion 21 in region
			Exclude	0					Exclude
\A/	DVA	CD22	Include	1					Include
W	ĸW	SR22	Evoludo	0					Include or exclude subregion 22 in region
			Exclude	0					Exclude
Y	D/V	SR23	Include	1					Include Include or exclude subregion 23 in region
X	KVV	JILZO	Exclude	0					Exclude Exclude
			Include	1					Include
Υ	R/V/	SR24	maduc	1					Include or exclude subregion 24 in region
•	11.00	JILT	Exclude	0					Exclude
			Include	1					Include
Z	RW	SR25		-					Include or exclude subregion 25 in region
_									



Bit number	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id	fedcbaZYXWVUTSRQPONMLKJIHGFEDCBA
Reset 0x00000000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value Description
Exclude	0 Exclude
Include	1 Include
a RW SR26	Include or exclude subregion 26 in region
Exclude	0 Exclude
Include	1 Include
b RW SR27	Include or exclude subregion 27 in region
Exclude	0 Exclude
Include	1 Include
c RW SR28	Include or exclude subregion 28 in region
Exclude	0 Exclude
Include	1 Include
d RW SR29	Include or exclude subregion 29 in region
Exclude	0 Exclude
Include	1 Include
e RW SR30	Include or exclude subregion 30 in region
Exclude	0 Exclude
Include	1 Include
f RW SR31	Include or exclude subregion 31 in region
Exclude	0 Exclude
Include	1 Include

45.1.25 PREGION[1].START

Address offset: 0x6D0

Reserved for future use

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	L8 1	.7 1	6 1	5 14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	Α Α	Α Α	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	A A
Res	et 0x	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0 0
Id	RW	Field	Value Id	Va	lue							Des	cri	ptic	n																		
Α	R	START										Res	erv	ed '	for	futı	ıre ı	use															

45.1.26 PREGION[1].END

Address offset: 0x6D4

Reserved for future use

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	4
Re	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	on																				ı
Α	R	END										Re	serv	ved	for	fut	ure	use	e																7

45.1.27 PREGION[1].SUBS

Address offset: 0x6D8 Subregions of region 1

Bit r	numb	er		31	. 30	29	28	3 27	7 26	25	24	23	22	21	20	19 :	18 1	.7 1	16 1	15 1	.4 1	13 1	2 1	1 10	9	8	7	6	5	4	3 2	2 :	1 0
Id				f	е	d	С	b	а	Z	Υ	Χ	W	٧	U	Т	S I	R (Q	Р	Э	N N	νı	. K	J	1	Н	G	F	Ε	D (С Е	3 A
Res	et 0x	00000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0 (0	0	0	0	0	0	0	0 () (0 0
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	SR0										Ind	lud	e or	exc	lud	e sı	ıbr	egic	on () in	reg	ion										
			Exclude	0								Ex	clud	e																			



Bit r	numbe	er		31 30	29 28	27 2	6 25 2	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				f e	d c	b a	a Z	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Rese	et 0x0	0000000		0 0	0 0	0 0	0 ($0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id	RW	Field	Value Id	Value				Description
			Include	1				Include
В	RW	SR1						Include or exclude subregion 1 in region
			Exclude	0				Exclude
			Include	1				Include
С	RW	SR2						Include or exclude subregion 2 in region
			Exclude	0				Exclude
			Include	1				Include
D	RW	SR3						Include or exclude subregion 3 in region
			Exclude	0				Exclude
			Include	1				Include
E	RW	SR4						Include or exclude subregion 4 in region
			Exclude	0				Exclude
_			Include	1				Include
F	RW	SR5						Include or exclude subregion 5 in region
			Exclude	0				Exclude
_	Ditt	SDC	Include	1				Include
G	RW	SR6	5 1 1					Include or exclude subregion 6 in region
			Exclude	0				Exclude
	DIA	CD7	Include	1				Include
Н	KVV	SR7	Evoludo	0				Include or exclude subregion 7 in region Exclude
			Exclude Include	1				Include
1	D\A/	SR8	iliciade	1				Include or exclude subregion 8 in region
'	IVV	310	Exclude	0				Exclude
			Include	1				Include
J	RW	SR9	meidae	_				Include or exclude subregion 9 in region
,	11.44	31.5	Exclude	0				Exclude
			Include	1				Include
K	RW	SR10	melade	-				Include or exclude subregion 10 in region
			Exclude	0				Exclude
			Include	1				Include
L	RW	SR11						Include or exclude subregion 11 in region
			Exclude	0				Exclude
			Include	1				Include
М	RW	SR12						Include or exclude subregion 12 in region
			Exclude	0				Exclude
			Include	1				Include
N	RW	SR13						Include or exclude subregion 13 in region
			Exclude	0				Exclude
			Include	1				Include
0	RW	SR14						Include or exclude subregion 14 in region
			Exclude	0				Exclude
			Include	1				Include
Р	RW	SR15						Include or exclude subregion 15 in region
			Exclude	0				Exclude
			Include	1				Include
Q	RW	SR16						Include or exclude subregion 16 in region
			Exclude	0				Exclude
			Include	1				Include
R	RW	SR17						Include or exclude subregion 17 in region
			Exclude	0				Exclude
			Include	1				Include
S	RW	SR18						Include or exclude subregion 18 in region
			Exclude	0				Exclude
			Include	1				Include



Bit	numb	er		31 30	29 2	28 2	7 26	25 24	1 2	2 22 2	1 2	20 1	9 1	8 1	.7 1	16	15	14	13 :	12	11 :	.0	9 8	3 7	6	5	4	3	2	1 0
Id				f e	d	c k	оа	Z Y	>	x w '	V	U 1	Г	S	R (Q	Р	О	N	М	L	K .	J	Н	G	F	Ε	D	С	ВА
Res	et 0x0	0000000		0 0	0	0 (0 0	0 0	C	0 0	0	0 ()	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Value					D	escrip	tio	n																		
Т	RW	SR19							lr	nclude	or	excl	lud	e sı	ıbr	egi	on	19 i	n re	egio	n									
			Exclude	0					Ε	xclude	!																			
			Include	1					lr	nclude																				
U	RW	SR20							lr	nclude	or	excl	lud	e sı	ıbr	egi	on	20 i	n re	egio	n									
			Exclude	0					Ε	xclude																				
			Include	1					lr	nclude																				
٧	RW	SR21							lr	nclude	or	excl	lud	e sı	ubr	egi	on	21 i	n re	egio	n									
			Exclude	0					E	xclude																				
			Include	1					lr	nclude																				
W	RW	SR22							lr	nclude	or	excl	lud	e sı	ıbr	egi	on	22 i	n re	egio	n									
			Exclude	0					Ε	xclude	!																			
			Include	1					lr	nclude																				
Х	RW	SR23							lr	nclude	or	excl	lud	e sı	ıbr	egi	on	2 3 i	n re	egio	n									
			Exclude	0					E	xclude																				
			Include	1					lr	nclude																				
Υ	RW	SR24							lr	nclude	or	excl	lud	e sı	ıbr	egi	on	24 i	n re	egio	n									
			Exclude	0					Ε	xclude	!																			
			Include	1					Ir	nclude																				
Z	RW	SR25							lr	nclude	or	excl	lud	e sı	ıbr	egi	on	2 5 i	n re	egio	n									
			Exclude	0					E	xclude																				
			Include	1					lr	nclude																				
а	RW	SR26							Ir	nclude	or	excl	lud	e sı	ıbr	egi	on	2 6 i	n re	egio	n									
			Exclude	0					Ε	xclude	!																			
			Include	1					Ir	nclude																				
b	RW	SR27							Ir	nclude	or	excl	lud	e sı	ıbr	egi	on	27 i	n re	egio	n									
			Exclude	0					E	xclude	!																			
			Include	1					lr	nclude																				
С	RW	SR28							Ir	nclude	or	excl	lud	e sı	ıbr	egi	on	28 i	n re	egio	n									
			Exclude	0					Ε	xclude																				
			Include	1					Ir	nclude																				
d	RW	SR29							lr	nclude	or	excl	lud	e sı	ubr	egi	on	2 9 i	n re	egio	n									
			Exclude	0					Ε	xclude																				
			Include	1					lr	nclude																				
е	RW	SR30							Ir	nclude	or	excl	lud	e sı	ubr	egi	on	30 i	n re	egio	n									
			Exclude	0					Ε	xclude	!																			
			Include	1					lr	nclude																				
f	RW	SR31							Ir	nclude	or	excl	lud	e sı	ıbr	egi	on	31 i	n re	egio	n									
			Exclude	0					Ε	xclude																				
			Include	1					lr	nclude																				



46 EGU — Event generator unit

The Event generator unit (EGU) provides support for inter-layer signaling. This means support for atomic triggering of both CPU execution and hardware tasks from both firmware (by CPU) and hardware (by PPI). This feature can, for instance, be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's ISR execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- · Enables SW triggering of interrupts
- 6 EGU instances separate interrupt vectors
- Up to 16 separate event flags per interrupt for multiplexing

The EGU implements a set of tasks which can individually be triggered to generate the corresponding event, i.e., the corresponding event for TASKS_TRIGGER[n] is EVENTS_TRIGGERED[n].

Table 114: EGU configuration

EGU instance	Number of event flags
0-5	16

46.1 Registers

Table 115: Instances

Base address	Peripheral	Instance	Description	Configuration
0x40014000	EGU	EGU0	Event Generator Unit 0	
0x40015000	EGU	EGU1	Event Generator Unit 1	
0x40016000	EGU	EGU2	Event Generator Unit 2	
0x40017000	EGU	EGU3	Event Generator Unit 3	
0x40018000	EGU	EGU4	Event Generator Unit 4	
0x40019000	EGU	EGU5	Event Generator Unit 5	

Table 116: Register Overview

Decistor	Officet	Description
Register	Offset	Description
TASKS_TRIGGER[0]	0x000	Trigger 0 for triggering the corresponding TRIGGERED[0] event
TASKS_TRIGGER[1]	0x004	Trigger 1 for triggering the corresponding TRIGGERED[1] event
TASKS_TRIGGER[2]	0x008	Trigger 2 for triggering the corresponding TRIGGERED[2] event
TASKS_TRIGGER[3]	0x00C	Trigger 3 for triggering the corresponding TRIGGERED[3] event
TASKS_TRIGGER[4]	0x010	Trigger 4 for triggering the corresponding TRIGGERED[4] event
TASKS_TRIGGER[5]	0x014	Trigger 5 for triggering the corresponding TRIGGERED[5] event
TASKS_TRIGGER[6]	0x018	Trigger 6 for triggering the corresponding TRIGGERED[6] event
TASKS_TRIGGER[7]	0x01C	Trigger 7 for triggering the corresponding TRIGGERED[7] event
TASKS_TRIGGER[8]	0x020	Trigger 8 for triggering the corresponding TRIGGERED[8] event
TASKS_TRIGGER[9]	0x024	Trigger 9 for triggering the corresponding TRIGGERED[9] event
TASKS_TRIGGER[10]	0x028	Trigger 10 for triggering the corresponding TRIGGERED[10] event
TASKS_TRIGGER[11]	0x02C	Trigger 11 for triggering the corresponding TRIGGERED[11] event
TASKS_TRIGGER[12]	0x030	Trigger 12 for triggering the corresponding TRIGGERED[12] event
TASKS_TRIGGER[13]	0x034	Trigger 13 for triggering the corresponding TRIGGERED[13] event
TASKS_TRIGGER[14]	0x038	Trigger 14 for triggering the corresponding TRIGGERED[14] event
TASKS_TRIGGER[15]	0x03C	Trigger 15 for triggering the corresponding TRIGGERED[15] event
EVENTS_TRIGGERED[0]	0x100	Event number 0 generated by triggering the corresponding TRIGGER[0] task
EVENTS_TRIGGERED[1]	0x104	Event number 1 generated by triggering the corresponding TRIGGER[1] task
EVENTS_TRIGGERED[2]	0x108	Event number 2 generated by triggering the corresponding TRIGGER[2] task
EVENTS_TRIGGERED[3]	0x10C	Event number 3 generated by triggering the corresponding TRIGGER[3] task
EVENTS_TRIGGERED[4]	0x110	Event number 4 generated by triggering the corresponding TRIGGER[4] task



Register	Offset	Description
EVENTS_TRIGGERED[5]	0x114	Event number 5 generated by triggering the corresponding TRIGGER[5] task
EVENTS_TRIGGERED[6]	0x118	Event number 6 generated by triggering the corresponding TRIGGER[6] task
EVENTS_TRIGGERED[7]	0x11C	Event number 7 generated by triggering the corresponding TRIGGER[7] task
EVENTS_TRIGGERED[8]	0x120	Event number 8 generated by triggering the corresponding TRIGGER[8] task
EVENTS_TRIGGERED[9]	0x124	Event number 9 generated by triggering the corresponding TRIGGER[9] task
EVENTS_TRIGGERED[10	0] 0x128	Event number 10 generated by triggering the corresponding TRIGGER[10] task
EVENTS_TRIGGERED[11	.] 0x12C	Event number 11 generated by triggering the corresponding TRIGGER[11] task
EVENTS_TRIGGERED[12	!] 0x130	Event number 12 generated by triggering the corresponding TRIGGER[12] task
EVENTS_TRIGGERED[13	3] 0x134	Event number 13 generated by triggering the corresponding TRIGGER[13] task
EVENTS_TRIGGERED[14	l] 0x138	Event number 14 generated by triggering the corresponding TRIGGER[14] task
EVENTS_TRIGGERED[15	i] 0x13C	Event number 15 generated by triggering the corresponding TRIGGER[15] task
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt

46.1.1 INTEN

Address offset: 0x300 Enable or disable interrupt

	abic	or disable interre	apt.		
Bit	numbe	r		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					PONMLKJIHGFEDCBA
Res	et 0x0	0000000		0 0 0 0 0 0 0 0	$\begin{smallmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 $
Id	RW	Field	Value Id	Value	Description
Α	RW	TRIGGERED0			Enable or disable interrupt for TRIGGERED[0] event
					See EVENTS_TRIGGERED[0]
			Disabled	0	Disable
			Enabled	1	Enable
В	RW	TRIGGERED1			Enable or disable interrupt for TRIGGERED[1] event
					See EVENTS_TRIGGERED[1]
			Disabled	0	Disable
			Enabled	1	Enable
С	RW	TRIGGERED2			Enable or disable interrupt for TRIGGERED[2] event
					See EVENTS_TRIGGERED[2]
			Disabled	0	Disable
			Enabled	1	Enable
D	RW	TRIGGERED3			Enable or disable interrupt for TRIGGERED[3] event
					See EVENTS_TRIGGERED[3]
			Disabled	0	Disable
			Enabled	1	Enable
E	RW	TRIGGERED4			Enable or disable interrupt for TRIGGERED[4] event
					See EVENTS_TRIGGERED[4]
			Disabled	0	Disable
			Enabled	1	Enable
F	RW	TRIGGERED5			Enable or disable interrupt for TRIGGERED[5] event
					See EVENTS_TRIGGERED[5]
			Disabled	0	Disable
			Enabled	1	Enable
G	RW	TRIGGERED6			Enable or disable interrupt for TRIGGERED[6] event
					See EVENTS_TRIGGERED[6]
			Disabled	0	Disable
			Enabled	1	Enable
Н	RW	TRIGGERED7			Enable or disable interrupt for TRIGGERED[7] event
					See EVENTS_TRIGGERED[7]
			Disabled	0	Disable



Bit r	numbe	er		31 30	29 2	28 2	7 26	25 2	4 2	3 22 21	1 2	0 19	18	3 17	16	5 15	14	4 1	.3 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0
Id																Р	C)	N N	1 1	_ K	J	-1	Н	G	F	Ε	D	С	В	Α
Res	et 0x0	0000000		0 0	0	0 0	0	0 0	0 0	0 0) (0	0	0	0	0	0) (0 0) (0 0	0	0	0	0	0	0	0	0	0	0
Id	RW	Field	Value Id	Value					D	escript	tior	1																			
			Enabled	1					Er	nable																					Ī
I	RW	TRIGGERED8							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGI	RE	D[8] ev	ent								
									Se	ee <i>EVEI</i>	NT	S_TR	IG	GER	ED	[8]															
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
J	RW	TRIGGERED9							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGI	ERE	D[9] ev	ent								
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[9]															
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
K	RW	TRIGGERED10							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGE	ERE	D[1	0] e	ever	nt							
									Se	ee <i>EVEI</i>	NT	S_TR	IG	GER	ED	[10]															
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
L	RW	TRIGGERED11							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGE	ERE	D[1	1] e	ever	nt							
									Se	ee <i>EVEI</i>	NT	S_TR	IG	GER	ED	[11]	1														
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
М	RW	TRIGGERED12							Er	nable o	or d	isab	le i	nte	rru	pt f	or '	TR	IGGI	ERE	D[1	2] ∈	ever	nt							
									Se	ee <i>EVEI</i>	NT	S_TR	IG	GER	ED	[12]															
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
N	RW	TRIGGERED13							Eı	nable o	or d	isab	le i	nte	rru	pt f	or '	TR	IGGI	ERE	D[1	3] e	ever	nt							
									Se	ee <i>EVEI</i>	NT	S_TR	IG	GER	ED	[13]	1														
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
0	RW	TRIGGERED14							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGI	ERE	D[1	4] €	ever	nt							
									Se	ee <i>EVEI</i>	NT	S_TR	IG	GER	ED	[14]	1														
			Disabled	0					D	isable																					
			Enabled	1					Er	nable																					
Р	RW	TRIGGERED15							Er	nable o	or d	isab	le i	nte	ru	pt f	or '	TR	IGGE	ERE	D[1	5] e	ever	nt							
									Se	ee <i>EVEI</i>	NTS	S_TR	IG	GER	ED	[15]	,														
			Disabled	0						isable																					
			Enabled	1						nable																					

46.1.2 INTENSET

Address offset: 0x304

Enable interrupt

Bit r	iumbe	r		31	. 30	29	28	27	26	25 :	24 2	23 22	2 21	20	19 1	8 1	7 1	6 1	5 1	4 1	3 1	2 11	10	9	8	7	6	5	4	3 2	1	0
Id																		F	· (1 C	۱ N	1 L	K	J	1	Н	G	F	E I) (В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0 (0) () (0	0	0	0	0	0	0	0	0	0 (0	0	0
Id	RW	Field	Value Id	Va	alue							Desc	riptic	n																		
Α	RW	TRIGGERED0									١	Write	e '1' t	o E	nab	e in	ter	rup	t fo	r Ti	RIGO	GERE	D[0] ev	/ent							
											9	See E	VEN	TS_	TRIC	GE	REC	0[0]														
			Set	1							E	Enab	le																			
			Disabled	0							F	Read	: Disa	ble	d																	
			Enabled	1							F	Read	: Ena	ble	d																	
В	RW	TRIGGERED1									١	Write	e '1' t	o E	nab	e in	ter	rup	t fo	r Ti	RIGO	GERE	D[1] e\	/ent							
											9	See E	VEN	TS_	TRIC	GE	REC	[1]														
			Set	1							E	Enab	le																			



Bit r	number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 C
	et 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW Field	Value Id	Value Description
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
С	RW TRIGGE	RED2	Write '1' to Enable interrupt for TRIGGERED[2] event
			See EVENTS_TRIGGERED[2]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
D	RW TRIGGE	RED3	Write '1' to Enable interrupt for TRIGGERED[3] event
			See EVENTS_TRIGGERED[3]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
E	RW TRIGGE		Write '1' to Enable interrupt for TRIGGERED[4] event
			Con EVENTE TRICCEDEDIAL
		Sot	See EVENTS_TRIGGERED[4] 1 Enable
		Set Disabled	1 Enable 0 Read: Disabled
		Enabled	1 Read: Enabled
F	RW TRIGGE		Write '1' to Enable interrupt for TRIGGERED[5] event
•	1111002	NEDS	
			See EVENTS_TRIGGERED[5]
		Set	1 Enable
		Disabled	0 Read: Disabled
_	DW TRICCE	Enabled	1 Read: Enabled
G	RW TRIGGE	KEDb	Write '1' to Enable interrupt for TRIGGERED[6] event
			See EVENTS_TRIGGERED[6]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
Н	RW TRIGGE	RED/	Write '1' to Enable interrupt for TRIGGERED[7] event
			See EVENTS_TRIGGERED[7]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
I	RW TRIGGE	RED8	Write '1' to Enable interrupt for TRIGGERED[8] event
			See EVENTS_TRIGGERED[8]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
J	RW TRIGGE	RED9	Write '1' to Enable interrupt for TRIGGERED[9] event
			See EVENTS_TRIGGERED[9]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
K	RW TRIGGE	RED10	Write '1' to Enable interrupt for TRIGGERED[10] event
			See EVENTS_TRIGGERED[10]
		Set	1 Enable
		Disabled	0 Read: Disabled
		Enabled	1 Read: Enabled
L	RW TRIGGE	RED11	Write '1' to Enable interrupt for TRIGGERED[11] event
			See EVENTS_TRIGGERED[11]
		Set	1 Enable
		Disabled	0 Read: Disabled



Bit	numbe	er		31	30	29 2	28 27	7 26	25	24 23	3 22	21 2	20 2	19 1	18	17 1	.6 :	15 1	4 1	.3 1	2 1	1 10	9	8	7	6	5 4	3	2	1 0
Id																		Р (O	N N	1 L	. K	J	1	Н	G	E	D	С	ВА
Res	et 0x0	0000000		0	0	0	0 0	0	0	0 0	0 0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue					D	escr	iptio	n																	
			Enabled	1						Re	ead:	Enal	oled	t																
М	RW	TRIGGERED12								W	Vrite	'1' to	o Er	nabl	le i	nter	rup	ot fo	r T	RIG	SER	ED[12]	eve	nt					
										Se	ee <i>E</i>	VENT	S_	TRIC	GGI	EREL)[1	2]												
			Set	1						Er	nabl	e																		
			Disabled	0						Re	ead:	Disa	ble	d																
			Enabled	1						Re	ead:	Enal	oled	t																
N	RW	TRIGGERED13								W	Vrite	'1' to	o Er	nabl	le i	nter	rup	ot fo	r T	RIG	SER	ED[13]	eve	nt					
										Se	ee <i>E</i>	VENT	S _1	TRIC	3GI	EREL)[1	3]												
			Set	1						Er	nabl	e																		
			Disabled	0						Re	ead:	Disa	ble	d																
			Enabled	1						Re	ead:	Enal	oled	t																
0	RW	TRIGGERED14								W	Vrite	'1' to	o Er	nabl	le i	nter	rup	ot fo	or T	RIG	SER	ED[14]	eve	nt					
										Se	ee <i>E</i>	VENT	S _	TRIC	GGI	EREL)[1	4]												
			Set	1						Er	nabl	e																		
			Disabled	0						Re	ead:	Disa	ble	d																
			Enabled	1						Re	ead:	Enal	oled	t																
Р	RW	TRIGGERED15								W	Vrite	'1' to	o Er	nabl	le i	nter	rup	ot fo	r T	RIG	SER	ED[15]	eve	nt					
										Se	ee <i>E</i>	VENT	S_	TRIC	GGI	EREL)[1	5]												
			Set	1						Er	nabl	e																		
			Disabled	0						Re	ead:	Disa	ble	d																
			Enabled	1						Re	ead:	Enal	oled	t																

46.1.3 INTENCLR

Address offset: 0x308

Disable interrupt

·			
Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			PONMLKJIHGFEDCBA
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A RW TRIGGEREDO			Write '1' to Disable interrupt for TRIGGERED[0] event
			See EVENTS_TRIGGERED[0]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
B RW TRIGGERED1			Write '1' to Disable interrupt for TRIGGERED[1] event
			See EVENTS_TRIGGERED[1]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
C RW TRIGGERED2			Write '1' to Disable interrupt for TRIGGERED[2] event
			See EVENTS_TRIGGERED[2]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
D RW TRIGGERED3			Write '1' to Disable interrupt for TRIGGERED[3] event
			See EVENTS_TRIGGERED[3]
	Clear	1	Disable
	Disabled	0	Read: Disabled
	Enabled	1	Read: Enabled
E RW TRIGGERED4			Write '1' to Disable interrupt for TRIGGERED[4] event



Bit r	numbe	er		31 30	29	28 2	7 26	25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id									PONMLKJIHGFEDCBA
Res		0000000			0	0 (0	0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value					Description
			CI.						See EVENTS_TRIGGERED[4]
			Clear	1					Disable Disabled
			Disabled	0					Read: Disabled
-	DIA	TRICCEREDE	Enabled	1					Read: Enabled
F	KW	TRIGGERED5							Write '1' to Disable interrupt for TRIGGERED[5] event
									See EVENTS_TRIGGERED[5]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
G	RW	TRIGGERED6							Write '1' to Disable interrupt for TRIGGERED[6] event
									See EVENTS_TRIGGERED[6]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
Н	RW	TRIGGERED7							Write '1' to Disable interrupt for TRIGGERED[7] event
									See EVENTS TRIGGERED[7]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
ı	RW	TRIGGERED8							Write '1' to Disable interrupt for TRIGGERED[8] event
									See EVENTS_TRIGGERED[8]
			Clear	1					Disable
			Disabled	0					Read: Disabled
1	D\A/	TRICCEREDO	Enabled	1					Read: Enabled
J	KVV	TRIGGERED9							Write '1' to Disable interrupt for TRIGGERED[9] event
									See EVENTS_TRIGGERED[9]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
K	RW	TRIGGERED10							Write '1' to Disable interrupt for TRIGGERED[10] event
									See EVENTS_TRIGGERED[10]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
L	RW	TRIGGERED11							Write '1' to Disable interrupt for TRIGGERED[11] event
									See EVENTS_TRIGGERED[11]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
М	RW	TRIGGERED12							Write '1' to Disable interrupt for TRIGGERED[12] event
									Con EVENTS TRICCEPED[42]
			Class	1					See EVENTS_TRIGGERED[12] Disable
			Clear	1					
			Disabled Enabled	1					Read: Disabled Read: Enabled
N	R/V/	TRIGGERED13	LIIANICU	1					Write '1' to Disable interrupt for TRIGGERED[13] event
IN	IVVV	IMIGOLINED 13							
									See EVENTS_TRIGGERED[13]
			Clear	1					Disable
			Disabled	0					Read: Disabled
			Enabled	1					Read: Enabled
0	RW	TRIGGERED14							Write '1' to Disable interrupt for TRIGGERED[14] event
									See EVENTS_TRIGGERED[14]



Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Id			PONMLKJIHGFEDCBA	
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
Id RW Field	Value Id	Value	Description	
	Clear	1	Disable	
	Disabled	0	Read: Disabled	
	Enabled	1	Read: Enabled	
P RW TRIGGERED15		Write '1' to Disable interrupt for TRIGGERED[15] event		
			See EVENTS_TRIGGERED[15]	
	Clear	1	Disable	
	Disabled	0	Read: Disabled	
	Enabled	1	Read: Enabled	

46.2 Electrical specification

46.2.1 EGU Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
t _{EGU,EVT}	Latency between setting an EGU event flag and the system		1		cycles
	setting an interrupt				



47 PWM — Pulse width modulation

The PWM module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

Three PWM modules can provide up to 12 PWM channels with individual frequency control in groups of up to four channels. Furthermore, a built-in decoder and EasyDMA capabilities make it possible to manipulate the PWM duty cycles without CPU intervention. Arbitrary duty-cycle sequences are read from Data RAM and can be chained to implement ping-pong buffering or repeated into complex loops.

Listed here are the main features of one PWM module:

- Fixed PWM base frequency with programmable clock divider
- Up to four PWM channels with individual polarity and duty-cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty-cycle arrays (sequences) defined in Data RAM
- · Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA
- · Change of polarity, duty-cycle, and base frequency possibly on every PWM period
- · Data RAM sequences can be repeated or connected into loops

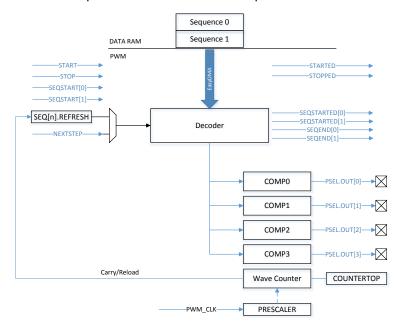


Figure 141: PWM Module

47.1 Wave counter

The wave counter is responsible for generating the pulses at a duty-cycle that depends on the compare values, and at a frequency that depends on COUNTERTOP.

There is one common 15-bit counter with four compare channels. Thus, all four channels will share the same period (PWM frequency), but can have individual duty-cycle and polarity. The polarity is set by the value read from RAM (see *Figure 144: Decoder memory access modes* on page 498), while the MODE register controls if the counter counts up, or up and down. The timer top value is controlled by the COUNTERTOP register. This register value in conjunction with the selected PRESCALER of the PWM_CLK will result in a given PWM period. A COUNTERTOP value smaller than the compare setting will result in a state where no PWM edges are generated. Respectively, OUT[n] is held high, given that the polarity is set to FallingEdge. All the compare registers are internal and can only be configured through the decoder presented later.

COUNTERTOP can be safely written at any time. It will get sampled following a START task. If DECODER.LOAD is anything else than WaveForm, it will also get sampled following a STARTSEQ[n] task,



and when loading a new value from RAM during a sequence playback. If DECODER.LOAD=WaveForm, the register value is ignored, and taken from RAM instead (see *Decoder with EasyDMA* on page 498 below).

Figure 142: PWM up counter example - FallingEdge polarity on page 496 shows the counter operating in up (MODE=PWM_MODE_Up) mode with three PWM channels with the same frequency but different duty cycle. The counter is automatically reset to zero when COUNTERTOP is reached and OUT[n] will invert. OUT[n] is held low if the compare value is 0 and held high respectively if set to COUNTERTOP given that the polarity is set to FallingEdge. Running in up counter mode will result in pulse widths that are edge-aligned. See the code example below:

```
uint16 t pwm seq[4] = {PWM CH0 DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
PWM CH3 DUTY);
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                        (PWM PSEL OUT CONNECT Connected <<
                                                  PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                        (PWM PSEL OUT CONNECT Connected <<
                                                 PWM_PSEL_OUT_CONNECT_Pos);
                      = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
NRF PWM0->ENABLE
NRF PWM0->MODE
                      = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->PRESCALER = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                  PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
NRF PWM0->LOOP
                    = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF PWM0->DECODER
                   = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos)
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF PWM0->SEQ[0].PTR = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(pwm seq) / sizeof(uint16_t)) < < 
                                                 PWM SEQ CNT CNT Pos);
NRF_PWM0 \rightarrow SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

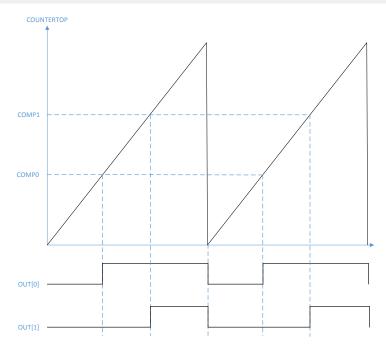


Figure 142: PWM up counter example - FallingEdge polarity

In up counting mode, the following formula can be used to compute PWM period and step size:

```
PWM period: T<sub>PWM</sub> (U<sub>p</sub>) = T<sub>PWM</sub> C<sub>LK</sub> * COUNTERTOP
```

Step width/Resolution: $T_{\text{steps}} = T_{\text{PWM_CLK}}$



Figure 143: PWM up-and-down counter example on page 497 shows the counter operating in up and down mode with (MODE=PWM_MODE_UpAndDown) two PWM channels with the same frequency but different duty cycle and output polarity. The counter starts decrementing to zero when COUNTERTOP is reached and will invert the OUT[n] when compare value is hit for the second time. This results in a set of pulses that are center- aligned.

```
uint16 t pwm seq[4] = {PWM CHO DUTY, PWM CH1 DUTY, PWM CH2 DUTY,
 PWM CH3 DUTY);
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |</pre>
                                                                      (PWM PSEL OUT CONNECT Connected <<
                                                                                                                                              PWM PSEL OUT CONNECT Pos);
NRF PWM0->PSEL.OUT[1] = (second pin << PWM PSEL OUT PIN Pos) |
                                                                      (PWM PSEL OUT CONNECT Connected <<
                                                                                                                                             PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                                                               = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                                                               = (PWM MODE UPDOWN UpAndDown << PWM MODE UPDOWN Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                                                                                                             PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
                                                               = (PWM LOOP CNT Disabled << PWM LOOP CNT Pos);
NRF
          PWM0->LOOP
NRF PWM0->DECODER
                                                          = (PWM DECODER LOAD Individual << PWM DECODER LOAD Pos)
                                                               (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF_PWM0->SEQ[0].PTR = ((uint32_t)(pwm_seq) << PWM_SEQ PTR PTR Pos);
NRF_PWM0 - SEQ[0].CNT = ((sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(pwm_seq) / sizeof(uint16_t)) < colspan="2">(sizeof(uint16_t)) < col
                                                                                                                                             PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0 \rightarrow SEQ[0].REFRESH = 0;
NRF PWM0 -> SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

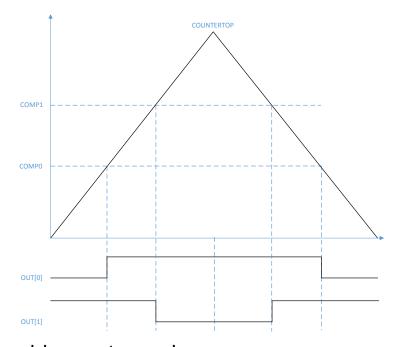


Figure 143: PWM up-and-down counter example

In up-and-down counting modes, the following formula can be used to compute PWM period and step size:

```
T_{PWM}(Up And Down) = T_{PWM} CLK * 2 * COUNTERTOP
```

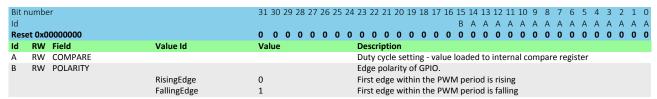
Step width/Resolution: $T_{\text{Steps}} = T_{\text{PWM CLK}} * 2$



47.2 Decoder with EasyDMA

The decoder uses EasyDMA to take PWM parameters stored in Data RAM by ways of EasyDMA and updates the internal compare registers of the wave counter based on the mode of operation.

The mentioned PWM parameters are organized into a sequence containing at least one half word (16 bit). Its most significant bit[15] denotes the polarity of the OUT[n] while bit[14:0] is the 15-bit compare value. See below for further details of these RAM defined registers.



The DECODER register controls how the RAM content is interpreted and loaded to the internal compare registers. The LOAD field can be used to control if the RAM values are loaded to all compare channels - or alternatively to update a group or all channels with individual values. *Figure 144: Decoder memory access modes* on page 498 illustrates how the parameters stored in RAM are organized and routed to the various compare channels in the different modes.

A special mode of operation is available when DECODER.LOAD is set to WaveForm. In this mode, up to three PWM channels can be enabled - OUT[0] to OUT[2]. In RAM, four values are loaded at a time: the first, second and third location are used to load the values, and the fourth RAM location is used to load the COUNTERTOP register. This way one can have up to three PWM channels with a frequency base that changes on a per PWM period basis. This mode of operation is useful for arbitrary wave form generation in applications such as LED lighting.

The register SEQ[n].REFRESH=N (one per sequence n=0 or 1) will instruct a new RAM stored pulse width value on every (N+1)th PWM period. Setting the register to zero will result in a new duty cycle update every PWM period as long as the minimum PWM period is observed.

Note that registers SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored when DECODER.MODE=NextStep . The next value is loaded upon receiving every NEXTSTEP task.

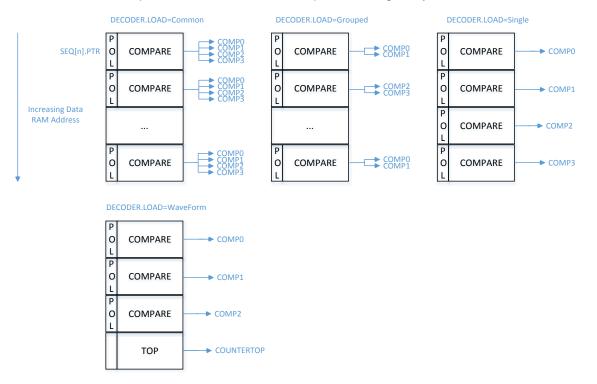


Figure 144: Decoder memory access modes



SEQ[n].PTR is the pointer used to fetch COMPARE values from RAM. If the SEQ[n].PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See *Memory* on page 23 for more information about the different memory regions.

After the SEQ[n].PTR is set to the desired RAM location, the SEQ[n].CNT register must be set to the number of 16-bit half words in the sequence. It is important to observe that the Grouped and Single modes require one half word per group or one half word per channel respectively, and thus increases RAM size occupation. If PWM generation was not running yet at that point, sending the SEQSTART[n] task will load the first value from RAM, then start the PWM generation. A SEQSTARTED[n] event is generated as soon as the EasyDMA has read the first PWM parameter from RAM and the wave counter has started executing it. When LOOP.CNT=0, sequence n=0 or 1 is played back once. After the last value in the sequence has been loaded and started executing, a SEQEND[n] event is generated. The PWM generation will then continue with the last loaded value. See *Figure 145: Simple sequence example* on page 500 for an example of such simple playback.

To completely stop the PWM generation and force the associated pins to a defined state, a STOP task can be fired at any time. A STOPPED event is generated when the PWM generation has stopped at the end of currently running PWM period, and the pins go into their idle state as defined in GPIO->OUT. PWM generation can then only be restarted through a SEQSTART[n] task. SEQSTART[n] will resume PWM generation after having loaded the first value from the RAM buffer defined in the SEQ[n].PTR register.

The table below provides indication of when specific registers get sampled by the hardware. Care should be taken when updating these registers to avoid values to be applied earlier than expected.

Table 117: When to safely update PWM registers

Register	Taken into account by hardware	Recommended (safe) update
SEQ[n].PTR	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[n].CNT	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[0].ENDDELAY	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the	When no more value from sequence [0] gets loaded from RAM (indicated by the SEQEND[0] event)
	PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].ENDDELAY	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	When no more value from sequence [1] gets loaded from RAM (indicated by the SEQEND[1] event)
	PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
SEQ[0].REFRESH	When sending the SEQSTART[0] task	Before starting sequence [0] through a SEQSTART[0] task
	Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [1] (which starts when the SEQSTARTED[1] event is fired)
SEQ[1].REFRESH	When sending the SEQSTART[1] task	Before starting sequence [1] through a SEQSTART[1] task
	Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	At any time during sequence [0] (which starts when the SEQSTARTED[0] event is fired)
COUNTERTOP	In DECODER.LOAD=WaveForm: this register is ignored.	Before starting PWM generation through a SEQSTART[n] task
	In all other LOAD modes: at the end of current PWM period (indicated by the PWMPERIODEND event)	After a STOP task has been issued, and the STOPPED event has been received.
MODE	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
DECODER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PRESCALER	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
LOOP	Immediately	Before starting PWM generation through a SEQSTART[n] task
		After a STOP task has been issued, and the STOPPED event has been received.
PSEL.OUT[n]	Immediately	Before enabling the PWM instance through the ENABLE register

Important: SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored at the end of a complex sequence, indicated by a LOOPSDONE event. The reason for this is that the last value loaded from RAM is maintained until further action from software (restarting a new sequence, or stopping PWM generation).



Figure 145: Simple sequence example on page 500 depicts the source code used for configuration and timing details in a sequence where only sequence 0 is used and only run once with a new PWM duty cycle for each period.

```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM_PSEL_OUT_PIN_Pos)
                           (PWM PSEL OUT CONNECT Connected <<
                                                      PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                        = (PWM ENABLE ENABLE Enabled << PWM ENABLE ENABLE Pos);
                        = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->MODE
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                                      PWM PRESCALER PRESCALER Pos);
NRF_PWM0->COUNTERTOP = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec NRF_PWM0->LOOP = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF PWM0->DECODER
                      = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos)
                        (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(seq0 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[0].CNT = ((sizeof(seq0 ram) / sizeof(\overline{uint16 t})) < \overline{<})
                                                      PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 0;
NRF PWM0->SEQ[0].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

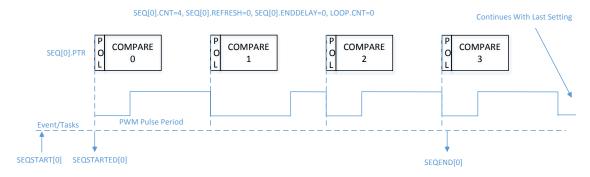


Figure 145: Simple sequence example

A more complex example is shown in *Figure 146: Example using two sequences* on page 501, where LOOP.CNT>0. In this case, an automated playback takes place, consisting of SEQ[0], delay 0, SEQ[1], delay 1, then again SEQ[0], etc. The user can choose to start a complex playback with SEQ[0] or SEQ[1] through sending the SEQSTART[0] or SEQSTART[1] task.

The complex playback always ends with delay 1.

The two sequences 0 and 1 are defined with address of values tables in Data RAM (pointed by SEQ[n].PTR) and respective buffer size (SEQ[n].CNT). The rate at which a new value is loaded is defined individually for each sequence by SEQ[n].REFRESH . The chaining of sequence 1 following sequence 0 is implicit, the LOOP.CNT register allows the chaining of sequence 1 to sequence 0 for a determined number of times. In other words, it allows to repeat a complex sequence a number of times in a fully automated way.

In the example below, sequence 0 is defined with SEQ[0].REFRESH set to one - that means that a new PWM duty cycle is pushed every second PWM period. This complex sequence is started with the SEQSTART[0] task, so SEQ[0] is played first. Since SEQ[0].ENDDELAY=1 there will be one PWM period delay between last period on sequence 0 and the first period on sequence 1. Since SEQ[1].ENDDELAY=0 there is no delay 1, so SEQ[0] would be started immediately after the end of SEQ[1]. However, as LOOP.CNT is one, the playback stops after having played only once SEQ[1], and both SEQEND[1] and LOOPSDONE are generated (their order is not guaranteed in this case).



```
NRF PWM0->PSEL.OUT[0] = (first pin << PWM PSEL OUT PIN Pos)
                       (PWM PSEL OUT CONNECT Connected <<
                                              PWM PSEL OUT CONNECT Pos);
NRF PWM0->ENABLE
                    = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_
   PWM0->MODE
                    = (PWM MODE UPDOWN Up << PWM MODE UPDOWN Pos);
NRF PWM0->PRESCALER = (PWM PRESCALER PRESCALER DIV 1 <<
                                              PWM PRESCALER PRESCALER Pos);
NRF PWM0->COUNTERTOP = (16000 << PWM COUNTERTOP COUNTERTOP Pos); //1 msec
                   = (1 \ll PWM LOOP CNT Pos);
NRF PWM0->LOOP
NRF PWM0->DECODER
                  = (PWM DECODER LOAD Common << PWM DECODER LOAD Pos) |
                    (PWM DECODER MODE RefreshCount << PWM DECODER MODE Pos);
NRF PWM0->SEQ[0].PTR = ((uint32 t)(seq0 ram) << PWM SEQ PTR PTR Pos);
PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[0].REFRESH = 1;
NRF PWM0->SEQ[0].ENDDELAY = 1;
NRF PWM0->SEQ[1].PTR = ((uint32 t)(seq1 ram) << PWM SEQ PTR PTR Pos);
NRF PWM0->SEQ[1].CNT = ((sizeof(seq1 ram) / sizeof(uint16 t)) <<
                                              PWM SEQ CNT CNT Pos);
NRF PWM0->SEQ[1].REFRESH = 0;
NRF PWM0->SEQ[1].ENDDELAY = 0;
NRF PWM0->TASKS SEQSTART[0] = 1;
```

SEQ[0].CNT=2, SEQ[1].CNT=3, SEQ[0].REFRESH=1, SEQ[1].REFRESH=0, SEQ[0].ENDDELAY=1, SEQ[1].ENDDELAY=0, LOOP.CNT=1

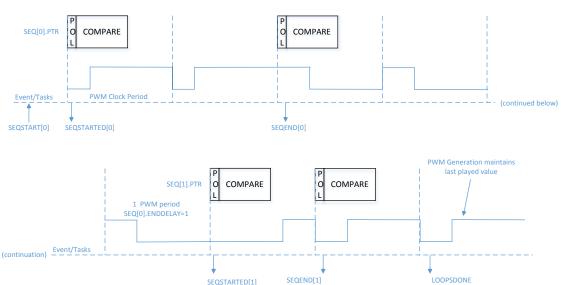


Figure 146: Example using two sequences

The decoder can also be configured to asynchronously load a new PWM duty cycle. If the DECODER.MODE register is set to NextStep - then the NEXTSTEP task will cause an update of the internal compare registers on the next PWM period.

The figures below provide an overview of each part of an arbitrary sequence, in various modes (LOOP.CNT=0 and LOOP.CNT>0). In particular are represented:

- Initial and final duty cycle on the PWM output(s)
- Chaining of SEQ[0] and SEQ[1] if LOOP.CNT>0
- · Influence of registers on the sequence
- · Events fired during a sequence
- DMA activity (loading of next value and applying it to the output(s))

Note that the single-shot example applies also to SEQ[1], only SEQ[0] is represented for simplicity.



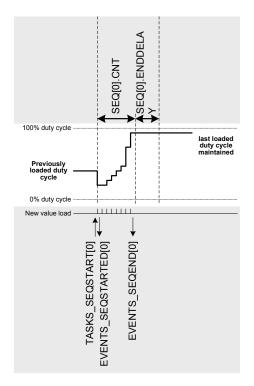


Figure 147: Single shot (LOOP.CNT=0)

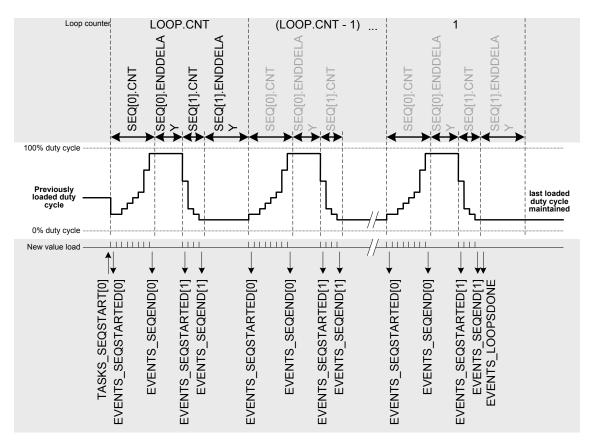


Figure 148: Complex sequence (LOOP.CNT>0) starting with SEQ[0]



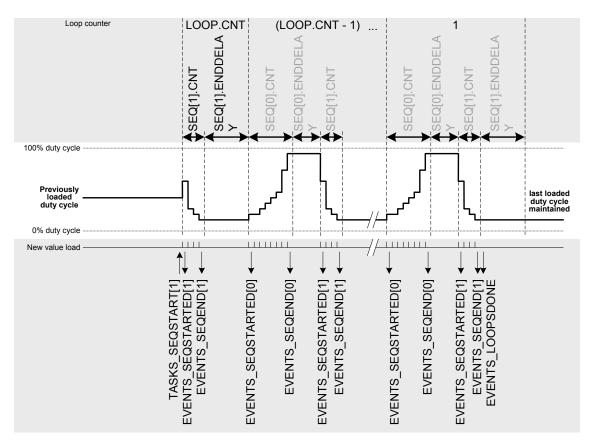


Figure 149: Complex sequence (LOOP.CNT>0) starting with SEQ[1]

Note that if a sequence is in use in a simple or complex sequence, it must have a length of SEQ[n].CNT > 0.

47.3 Limitations

The previous compare value will be repeated if the PWM period is selected to be shorter than the time it takes for the EasyDMA to fetch from RAM and update the internal compare registers.

This is to ensure a glitch-free operation even if very short PWM periods are chosen.

47.4 Pin configuration

The OUT[n] (n=0..3) signals associated to each channel of the PWM module are mapped to physical pins according to the configuration specified in the respective PSEL.OUT[n] registers. If a PSEL.OUT[n].CONNECT is set to Disconnected, the associated PWM module signal will not be connected to any physical pins.

The PSEL.OUT[n] registers and their configurations are only used as long as the PWM module is enabled and PWM generation is active (wave counter started), and retained only as long as the device is in System ON mode, see *POWER* chapter for more information about power modes.

To ensure correct behaviour in the PWM module, the pins used by the PWM module must be configured in the GPIO peripheral as described in *Table 118: Recommended GPIO configuration before starting PWM generation* on page 504 before enabling the PWM module. The pins' idle state is defined by the OUT registers in the GPIO module. This is to ensure that the pins used by the PWM module are driven correctly, if PWM generation is stopped through a STOP task, the PWM module itself is temporarily disabled, or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected IOs as long as the PWM module is supposed to be connected to an external PWM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behaviour.



Table 118: Recommended GPIO configuration before starting PWM generation

PWM signal	PWM pin	Direction	Output value	Comment
OUT[n]	As specified in PSEL.OUT[n]	Output	0	Idle state defined in GPIO->OUT
	(n=0, 3)			

47.5 Registers

Table 119: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x4001C000	PWM	PWM0	Pulse Width Modulation Unit 0		
0x40021000	PWM	PWM1	Pulse Width Modulation Unit 1		
0x40022000	PWM	PWM2	Pulse Width Modulation Unit 2		

Table 120: Register Overview

Register	Offset	Description
TASKS_STOP	0x004	Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence
		playback
TASKS_SEQSTART[0]	0x008	Loads the first PWM value on all enabled channels from sequence 0, and starts playing that
		sequence at the rate defined in SEQ[0]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_SEQSTART[1]	0x00C	Loads the first PWM value on all enabled channels from sequence 1, and starts playing that
		sequence at the rate defined in SEQ[1]REFRESH and/or DECODER.MODE. Causes PWM generation to
		start it was not running.
TASKS_NEXTSTEP	0x010	Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep.
		Does not cause PWM generation to start it was not running.
EVENTS_STOPPED	0x104	Response to STOP task, emitted when PWM pulses are no longer generated
EVENTS_SEQSTARTED[0]	0x108	First PWM period started on sequence 0
EVENTS_SEQSTARTED[1]	0x10C	First PWM period started on sequence 1
EVENTS_SEQEND[0]	0x110	Emitted at end of every sequence 0, when last value from RAM has been applied to wave counter
EVENTS_SEQEND[1]	0x114	Emitted at end of every sequence 1, when last value from RAM has been applied to wave counter
EVENTS_PWMPERIODEN	0x118	Emitted at the end of each PWM period
EVENTS_LOOPSDONE	0x11C	Concatenated sequences have been played the amount of times defined in LOOP.CNT
SHORTS	0x200	Shortcut register
INTEN	0x300	Enable or disable interrupt
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ENABLE	0x500	PWM module enable register
MODE	0x504	Selects operating mode of the wave counter
COUNTERTOP	0x508	Value up to which the pulse generator counter counts
PRESCALER	0x50C	Configuration for PWM_CLK
DECODER	0x510	Configuration of the decoder
LOOP	0x514	Amount of playback of a loop
SEQ[0].PTR	0x520	Beginning address in Data RAM of this sequence
SEQ[0].CNT	0x524	Amount of values (duty cycles) in this sequence
SEQ[0].REFRESH	0x528	Amount of additional PWM periods between samples loaded into compare register
SEQ[0].ENDDELAY	0x52C	Time added after the sequence
SEQ[1].PTR	0x540	Beginning address in Data RAM of this sequence
SEQ[1].CNT	0x544	Amount of values (duty cycles) in this sequence
SEQ[1].REFRESH	0x548	Amount of additional PWM periods between samples loaded into compare register
SEQ[1].ENDDELAY	0x54C	Time added after the sequence
PSEL.OUT[0]	0x560	Output pin select for PWM channel 0
PSEL.OUT[1]	0x564	Output pin select for PWM channel 1
PSEL.OUT[2]	0x568	Output pin select for PWM channel 2
PSEL.OUT[3]	0x56C	Output pin select for PWM channel 3



47.5.1 SHORTS

Address offset: 0x200 Shortcut register

Bit r	numbe	er		31 30	29	28	27 :	26 2	5 2	4 23	3 2	2 2	21 2	0 1	9 18	3 17	16	15	14	L3 1	.2 1	1 10	9	8	7	6 5	4	3	2 :	1 0
Id																											Ε	D	C E	ВА
Res	et 0x0	0000000		0 0	0	0	0	0 (0	0) (0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0 0	0	0	0 (0 0
Id	RW	Field	Value Id	Value	•					D	esc	crip	tior	1																
Α	RW	SEQENDO_STOP								Sł	hor	tcu	ıt be	etwe	een	SEQ	ĮΕΝ	D[0]	eve	ent a	and	STO	P ta	sk						
										Se	ee	EVE	NT	s_si	EQE	ND[0] a	ınd	TAS	KS_S	STO	P								
			Disabled	0						D	isa	ble	sho	rtcı	ut															
			Enabled	1						Er	nak	ole	sho	rtcu	t															
В	RW	SEQEND1_STOP								Sł	hor	tcu	ıt be	etwe	een	SEQ	ĮΕΝ	D[1]	eve	ent a	and	STO	P ta	sk						
										Se	ee	EVE	NT	s_sı	EQE	ND[1] a	ınd	TAS	KS_S	sto	P								
			Disabled	0						D	isa	ble	sho	rtcı	ut															
			Enabled	1						Er	nak	ole	sho	rtcu	t															
С	RW	LOOPSDONE_SEQSTARTO								Sł	hor	tcu	ıt be	etwe	een	LOC	PS	NOO	IE e	ven	t an	d SE	QST	ART	[0]	task				
										Se	ee	EVE	NT:	S_ <i>L</i> (OOF	SDC	ONE	and	d <i>TA</i>	SKS	_SE	QST	ART	[0]						
			Disabled	0						D	isa	ble	sho	rtcı	ut															
			Enabled	1						Er	nak	ole	sho	rtcu	t															
D	RW	LOOPSDONE_SEQSTART1								Sł	hor	tcu	ıt be	etwe	een	LOC	PS	OO	IE e	ven	t an	d SE	QST	ART	[1]	task				
										Se	ee	EVE	NT	S_ <i>L</i> (OOF	SDC	ONE	and	d <i>TA</i>	SKS	_SE	QST	ART	[1]						
			Disabled	0						D	isa	ble	sho	rtcı	ut															
			Enabled	1						Er	nak	ole	sho	rtcu	t															
E	RW	LOOPSDONE_STOP								Sł	hor	tcu	ıt be	etwe	een	LOC	PS	100	IE e	ven	t an	d ST	OP	task						
										Se	ee	EVE	NT	S_ <i>L</i> (OOF	SDC	ONE	and	d <i>TA</i>	SKS	_ST	OP								
			Disabled	0						D	isa	ble	sho	rtcı	ut															
			Enabled	1						Eı	nat	ole	sho	rtcu	t															

47.5.2 INTEN

Address offset: 0x300 Enable or disable interrupt

Bit	numbe	er		31 3	30 29	28	27	26 25	5 24	23 2	22 2	1 20	19	18	17 1	16 1	L5 1	4 1	3 12	11	10	9	8	7 6	5	4	3	2	1 0
Id																								H G	F	Ε	D	C I	3
Res	et 0x0	0000000		0	0 0	0	0	0 0	0	0	0 0	0	0	0	0	0	0 (0 (0	0	0	0	0	0 0	0	0	0	0	0 0
Id	RW	Field	Value Id	Valu	ıe					Des	crip	tion																	
В	RW	STOPPED								Ena	ble o	or dis	sable	e int	terr	upt	for	STC	OPPE	D e	vent	t							
										See	EVE	NTS_	STC	PP	ED														
			Disabled	0						Disa	able																		
			Enabled	1						Ena	ble																		
С	RW	SEQSTARTED0								Ena	ble o	or dis	sable	e int	terr	upt	for	SEC	QSTA	RTE	D[0] ev	ent						
										See	EVE	NTS_	SEC	QSTA	4RT	ED[0]												
			Disabled	0						Disa	able																		
			Enabled	1						Ena	ble																		
D	RW	SEQSTARTED1								Ena	ble o	or dis	sable	e int	terr	upt	for	SEC	QSTA	RTE	D[1] ev	ent						
										See	EVE	NTS_	SEC	QSTA	4RT	ED[1]												
			Disabled	0						Disa	able																		
			Enabled	1						Ena	ble																		
Ε	RW	SEQEND0								Ena	ble o	or dis	sable	e int	terr	upt	for	SEC	QENI	D[0]	eve	nt							
										See	EVE	NTS_	SEC	QEN	D[0]	1													
			Disabled	0						Disa	able																		
			Enabled	1						Ena	ble																		
F	RW	SEQEND1								Ena	ble o	or dis	sable	e int	terr	upt	for	SEC	QENI	0[1]	eve	nt							



Bit r	numbe	r		31 30 29 28 27 26							23 2	2 21	. 20	19	18	17 :	16	15 :	14 1	l3 1	2 11	10	9	8	7	6	5	4	3 :	2 1	0 1
Id																									Н	G	F	Ε	D (СВ	3
Res	et 0x0	0000000		0	0 0	(0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0 0	0 0
Id	RW	Field	Value Id	Va	lue						Desc	ripti	ion																		
											See	EVEN	VTS_	SEC	QΕN	D[1]														
			Disabled	0							Disa	ble																			
			Enabled	1							Enab	ole																			
G	RW	PWMPERIODEND									Enak	ole o	r dis	abl	e in	terr	upt	for	rPV	VMP	ERIC	DDE	ND	eve	nt						
											See	EVEN	NTS_	PW	MF	PERI	OD.	ENL)												
			Disabled	0							Disa	ble																			
			Enabled	1							Enab	ole																			
Н	RW	LOOPSDONE									Enab	ole o	r dis	abl	e in	terr	upt	for	r LO	OPS	DON	IE e	ven	t							
											See	EVEN	NTS_	LO	OPS	DO	NE														
			Disabled	0							Disa	ble																			
			Enabled	1							Enab	ole																			

47.5.3 INTENSET

Address offset: 0x304

Enable interrupt

	olo ilitorrapt			
Bit num	mber		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				HGFEDCB
Reset 0	0x00000000		0 0 0 0 0 0 0 0	
Id R	RW Field	Value Id	Value	Description
B R	RW STOPPED			Write '1' to Enable interrupt for STOPPED event
				See EVENTS_STOPPED
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
C R	RW SEQSTARTEDO			Write '1' to Enable interrupt for SEQSTARTED[0] event
				See EVENTS_SEQSTARTED[0]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D R	RW SEQSTARTED1			Write '1' to Enable interrupt for SEQSTARTED[1] event
				See EVENTS_SEQSTARTED[1]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E R'	RW SEQENDO			Write '1' to Enable interrupt for SEQEND[0] event
				See EVENTS_SEQEND[0]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F R	RW SEQEND1			Write '1' to Enable interrupt for SEQEND[1] event
				See EVENTS_SEQEND[1]
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G R	RW PWMPERIODEND			Write '1' to Enable interrupt for PWMPERIODEND event
				See EVENTS_PWMPERIODEND
		Set	1	Enable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
H R	RW LOOPSDONE			Write '1' to Enable interrupt for LOOPSDONE event



Bit number	31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		HGFEDCB
Reset 0x00000000	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field Value Id	Value	Description
		See EVENTS_LOOPSDONE
Set	1	Enable
Disabled	0	Read: Disabled
Enabled	1	Read: Enabled

47.5.4 INTENCLR

Address offset: 0x308

Disable interrupt

	number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (
Id				HGFEDCB
Res	et 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ld	RW Field	Value Id	Value	Description
В	RW STOPPED			Write '1' to Disable interrupt for STOPPED event
				See EVENTS_STOPPED
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
С	RW SEQSTARTEDO			Write '1' to Disable interrupt for SEQSTARTED[0] event
				See EVENTS_SEQSTARTED[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
D	RW SEQSTARTED1			Write '1' to Disable interrupt for SEQSTARTED[1] event
				See EVENTS_SEQSTARTED[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
E	RW SEQENDO			Write '1' to Disable interrupt for SEQEND[0] event
				See EVENTS_SEQEND[0]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
F	RW SEQEND1			Write '1' to Disable interrupt for SEQEND[1] event
				See EVENTS_SEQEND[1]
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
G	RW PWMPERIODEND			Write '1' to Disable interrupt for PWMPERIODEND event
				See EVENTS_PWMPERIODEND
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled
Н	RW LOOPSDONE			Write '1' to Disable interrupt for LOOPSDONE event
				See EVENTS_LOOPSDONE
		Clear	1	Disable
		Disabled	0	Read: Disabled
		Enabled	1	Read: Enabled

47.5.5 ENABLE

Address offset: 0x500



PWM module enable register

Bit	numbe	er							24	23	22 2	21 2	0 1	9 1	8 17	16	15	14	13	12 :	1 1	9	8	7	6	5	4	3	2	1 0	
Id																															Α
Res	et 0x0	0000000		0 0 0 0 0 0 0 0 Value						0	0	0	0	0 0) (0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id								Des	crip	otio	n																	
Α	RW	ENABLE		Value							Ena	ble	or o	disal	ole	lWq	M n	nod	ule												
			Disabled	0						Disa	able	d																			
			Enabled	1					Ena	ble																					

47.5.6 MODE

Address offset: 0x504

Selects operating mode of the wave counter

Bit r	numb	er		31 30 29 28 27 26 25 24 2	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id					A
Res	et Ox	0000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value [Description
Α	RW	UPDOWN		S	Selects up or up and down as wave counter mode
			Up	0	Up counter - edge aligned PWM duty-cycle
			UpAndDown	1 (Up and down counter - center aligned PWM duty cycle

47.5.7 COUNTERTOP

Address offset: 0x508

Value up to which the pulse generator counter counts

																														_
Bit	numbe	er		31 30	29	28 2	7 26	25	24	23 2	22 2	1 20	19	18	17	16 1	15 1	4 13	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id																	1	A A	Α	Α	Α	Α	Α	Α	Α	Α.	А А	Α	Α	Α
Res	et 0x0	00003FF		0 0	0	0 (0	0	0	0	0 0	0	0	0	0	0	0 (0	0	0	0	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Value						Des	cript	tion																		
Α	RW	COUNTERTOP		[332	767]]			,	Valu	ie up	o to	whi	ch th	ie p	oulse	e ge	nera	tor	cou	nte	r co	ount	s. 1	Γhis					
					register is ignored when DECODER.MODE=WaveForm and only																									
					بيادي	oc f	rom	DAN	∕l wi	IJЬ		- 4																		

47.5.8 PRESCALER

Address offset: 0x50C

Configuration for PWM_CLK

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PRESCALER		Pre-scaler of PWM_CLK
	DIV_1	0 Divide by 1 (16MHz)
	DIV_2	1 Divide by 2 (8MHz)
	DIV_4	2 Divide by 4 (4MHz)
	DIV_8	3 Divide by 8 (2MHz)
	DIV_16	4 Divide by 16 (1MHz)
	DIV_32	5 Divide by 32 (500kHz)
	DIV_64	6 Divide by 64 (250kHz)
	DIV_128	7 Divide by 128 (125kHz)

47.5.9 DECODER

Address offset: 0x510

Configuration of the decoder



Bit r	numbe	r		31	. 30	29	28	27 :	26 2	5 2	4 23	3 22	2 21	20	19	18	17 1	16 1	L5 1	4 1	3 12	11	10	9	8	7 (6 5	5 4	3	2	1	0
Id																									В						Α	Α
Res	et 0x0	0000000		0	0	0	0	0	0 (0 (0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 (0 (0	0	0	0	0
Id	RW	Field	Value Id	Va	lue	:					D	esc	ripti	on																		
Α	RW	LOAD									Н	ow	a se	que	nce	is r	ead	fro	m F	RAM	lan	d sp	reac	l to	the	cor	npa	re				
											re	egist	ter																			
			Common	0							19	st h	alf w	vord	1 (16	5-bit	t) us	ed	in a	II P\	۸M	cha	nne	ls 0	3							
			Grouped	1							19	st h	alf w	vord	1 (16	5-bit	t) us	ed	in c	han	nel	01	; 2n	d w	ord	in c	han	nel				
											2.	3																				
			Individual	2							19	st h	alf w	vord	1 (16	5-bit	t) in	ch.	.0; 2	nd	in cl	1.1;	; 4	lth i	in ch	1.3						
			WaveForm	3							19	st h	alf w	vord	1 (16	5-bit	t) in	ch.	.0; 2	nd	in cl	1.1;	; 4	lth i	in							
											C	100	NTEF	RTO	P																	
В	RW	MODE									Se	elec	cts so	ourc	e fo	or ac	dvar	ncir	ng th	ne a	ctiv	e se	que	nce								
			RefreshCount	0							SE	EQ[ı	n].RI	EFR	ESH	is u	sed	to	det	erm	ine	load	ding	inte	erna	l co	mp	are				
											re	egist	ters																			
			NextStep	1							N	EXT	ΓSΤΕΙ	P ta	sk c	aus	es a	ne	w v	alue	to	be l	oade	ed t	o in	terr	al					
											cc	omp	pare	reg	iste	rs																

47.5.10 LOOP

Address offset: 0x514

Amount of playback of a loop

Bit	numb	er		31	. 30	29	28	27	26	25	24	23	22 :	21 2	20 1	9 1	8 1	7 16	5 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
Id																			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	4 4	٨
Res	et 0x(0000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0									0	0	0 () (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ()
Id	RW	Field	Value Id										crip	otio	n																			ı
Α	RW	CNT										Am	our	it of	pla	yba	ick d	of p	atte	rn d	ycl	es												
			Disabled	0								Loc	pin	g di	sabl	ed	(sto	p at	the	e en	d o	f th	e se	que	enc	e)								

47.5.11 SEQ[0].PTR

Address offset: 0x520

Beginning address in Data RAM of this sequence

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Beginning address in Data RAM of this sequence

47.5.12 SEQ[0].CNT

Address offset: 0x524

Amount of values (duty cycles) in this sequence

Bit	numb	er		31	30	29	28 2	27 20	5 2	5 24	1 23	3 22	21	20 1	L9 1	l8 1	7 1	6 15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id																			Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	АА	A	. A
Res	et 0x0	0000000		0	0	0	0	0 0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue						De	escri	ptic	n																		
Α	RW	CNT									Ar	nou	nt o	f val	lues	s (dı	uty	cycle	es) i	n th	is s	equ	enc	ce								
			Disabled	0							Se	que	nce	is d	isat	oled	, an	d sh	all	not	be s	tar	ted	as	it is	em	pty	,				

47.5.13 SEQ[0].REFRESH

Address offset: 0x528

Amount of additional PWM periods between samples loaded into compare register



Bit	numb	er		33	1 30	29	28	3 27	7 26	5 25	24	23	22	21 :	20 :	19 1	18 1	7 1	6 1	5 1	4 1	3 12	11	10	9	8	7	6	5	4	3 2	2 1	0
Id												Α	Α	Α	Α	Α.	Α /	Δ ,	A 4	Δ ,	Δ Δ	A	Α	Α	Α	Α	Α	Α	Α.	Α	A A	A	Α
Re	et 0x	0000001		0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 () (0 (0	0	0	0	0	0	0	0	0	0	0 0	0	1
Id	RW	Field	Value Id	V	alue							De	scri	ptio	n																		
Α	RW	CNT										Am	our	nt o	f ad	lditi	iona	ΙPV	٧M	pe	riod	s be	twe	en s	sam	ple	s lo	ade	ed				
												int	о со	mp	are	reg	giste	r (lo	oad	ev	ery l	REFF	RESH	I.CN	IT+:	1 P\	٧M						
												pei	riod	s)																			
			Continuous	0								Up	date	e ev	ery	PW	/M į	peri	od														

47.5.14 SEQ[0].ENDDELAY

Address offset: 0x52C

Time added after the sequence

E	Bit nu	ımbe	er		31	30 2	9	28 2	7 2	26 2	25 2	24 :	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 ()
1	d												Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	A A	٨
F	Reset	0x0	0000000		0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0)
ı	d	RW	Field	Value Id	Val	lue						ı	Des	cri	ptic	on																				
-	7	RW/	CNT										Tim	ne a	hh	he	afte	r th	16.5	eai	ıen	re i	n P'	۸/۱۸	1 ne	rio	ds									7

47.5.15 SEQ[1].PTR

Address offset: 0x540

Beginning address in Data RAM of this sequence

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW PTR		Beginning address in Data RAM of this sequence

47.5.16 SEQ[1].CNT

Address offset: 0x544

Amount of values (duty cycles) in this sequence

Bit	numb	er		31 30	29	28	3 27	7 26	25	5 24	23	22	21	20	19	18	17 :	16	15 :	14	13	12 :	11 :	LO	9	8	7	6	5	4	3 2	1	0
Id																				Α	Α	Α	Α	A .	Α	A .	Α	Α.	Α	A	4 A	A	Α
Res	et 0x(0000000		0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Value	•						De	escri	ptic	on																			
Α	RW	CNT									Ar	nou	nt o	f va	alue	s (d	uty	су	les) in	thi	s se	qu	enc	е								
			Disabled	Λ							Se	que	nco	ic r	lica	hlar	۱ ۵	hd.	cha	ll n	at k	ω c	art	ha	ac i	t ic	۵m	ntv					

47.5.17 SEQ[1].REFRESH

Address offset: 0x548

Amount of additional PWM periods between samples loaded into compare register

Bit number		31	1 30	29	9 2	8 2	7 2	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (,
Id											Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A A	A A	Ĺ
Reset 0x00000001		0	0	0	(0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 :	
ld RW Field	Value Id	Va	alue	•							Des	scri	ptic	on																				l
A RW CNT											Am	our	nt o	f a	ddi	tion	nal I	PW	Μŗ	eri	ods	bet	we	en s	sam	ple	s lo	ad	ed					Ī
											into	о со	mp	are	e re	gist	ter	(loa	ıd e	ver	y RI	EFR	ESH	.CN	IT+:	1 P\	٧N	1						
											per	iod	s)																					
	Continuous	0									Upo	date	e ev	/ery	y P\	٧N	1 pe	rio	d															

47.5.18 SEQ[1].ENDDELAY

Address offset: 0x54C



Time added after the sequence

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		A A A A A A A A A A A A A A A A A A A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
A RW CNT		Time added after the sequence in PWM periods

47.5.19 PSEL.OUT[0]

Address offset: 0x560

Output pin select for PWM channel 0

Bit	numbe	er		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	ААААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

47.5.20 PSEL.OUT[1]

Address offset: 0x564

Output pin select for PWM channel 1

Bit	numbe	er		31 30 29 28 27 26 25 24	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

47.5.21 PSEL.OUT[2]

Address offset: 0x568

Output pin select for PWM channel 2

Bit	numbe	er		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				С	АААА
Res	et 0xF	FFFFFF		1 1 1 1 1 1 1 1	$. \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ $
Id	RW	Field	Value Id	Value	Description
Α	RW	PIN		[031]	Pin number
С	RW	CONNECT			Connection
			Disconnected	1	Disconnect
			Connected	0	Connect

47.5.22 PSEL.OUT[3]

Address offset: 0x56C

Output pin select for PWM channel 3

Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		С	ААААА
Reset 0xFFFFFFF		1 1 1 1 1 1 1	$1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \; 1 \;$
Id RW Field	Value Id	Value	Description
A RW PIN		[031]	Pin number



Bit r	numbe	er		31 30	29	28 2	27 2	6 2	5 24	23	22 2	21 2) 19	18	17 1	.6 1	5 14	13	12 1	.1 10	9	8	7	6	5	4	3 2	1	0
Id				С																						Α	A A	Α	Α
Res	et OxF	FFFFFF		1 1	1	1	1 1	L 1	۱ 1	1	1	1 1	. 1	1	1	1 1	1	1	1	1 1	1	1	1	1	1	1	1 1	1	1
Id	RW	Field	Value Id	Value						De	scrip	tion	ı																
С	RW	CONNECT								Co	nnec	tion																	
			Disconnected	1						Dis	coni	nect																	
			Connected	0						Со	nned	t																	

47.6 Electrical specification

47.6.1 PWM Electrical Specification

Symbol	Description	Min.	Тур.	Max.	Units
I _{PWM,16MHz}	PWM run current, Prescaler set to DIV_1 (16 MHz), excluding		200		μΑ
	DMA and GPIO				
I _{PWM,8MHz}	PWM run current, Prescaler set to DIV_2 (8 MHz), excluding		150		μΑ
	DMA and GPIO				
I _{PWM,125kHz}	PWM run current, Prescaler set to DIV_128 (125 kHz), excluding		150		μΑ
	DMA and GPIO				



48 SPI — Serial peripheral interface master

The SPI master provides a simple CPU interface which includes a TXD register for sending data and an RXD register for receiving data. This section is added for legacy support for now.

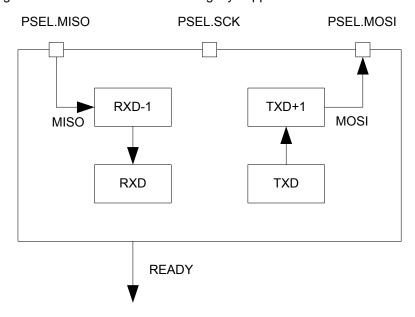


Figure 150: SPI master

RXD-1 and TXD+1 illustrate the double buffered version of RXD and TXD respectively.

48.1 Functional description

The TXD and RXD registers are double-buffered to enable some degree of uninterrupted data flow in and out of the SPI master.

The SPI master does not implement support for chip select directly. Therefore, the CPU must use available GPIOs to select the correct slave and control this independently of the SPI master. The SPI master supports SPI modes 0 through 3.

Table 121: SPI modes

Mode	Clock polarity	Clock phase
	CPOL	СРНА
SPI_MODE	0 (Leading)	0 (Active High)
SPI_MODE	0 (Leading)	1 (Active Low)
SPI_MODE	1 (Trailing)	0 (Active High)
SPI_MODE	1 (Trailing)	1 (Active Low)

48.1.1 SPI master mode pin configuration

The different signals SCK, MOSI, and MISO associated with the SPI master are mapped to physical pins.

This mapping is according to the configuration specified in the PSELSCK, PSELMOSI, and PSELMISO registers respectively. If a value of 0xFFFFFFF is specified in any of these registers, the associated SPI master signal is not connected to any physical pin. The PSELSCK, PSELMOSI, and PSELMISO registers and their configurations are only used as long as the SPI master is enabled, and retained only as long as the device is in ON mode. PSELSCK, PSELMOSI, and PSELMISO must only be configured when the SPI master is disabled.

To secure correct behavior in the SPI, the pins used by the SPI must be configured in the GPIO peripheral as described in *Table 122: GPIO configuration* on page 514 prior to enabling the SPI. The SCK must



always be connected to a pin, and that pin's input buffer must always be connected for the SPI to work. This configuration must be retained in the GPIO for the selected IOs as long as the SPI is enabled.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 122: GPIO configuration

SPI master signal	SPI master pin	Direction	Output value
SCK	As specified in PSELSCK	Output	Same as CONFIG.CPOL
MOSI	As specified in PSELMOSI	Output	0
MISO	As specified in PSELMISO	Input	Not applicable

48.1.2 Shared resources

The SPI shares registers and other resources with other peripherals that have the same ID as the SPI. Therefore, the user must disable all peripherals that have the same ID as the SPI before the SPI can be configured and used.

Disabling a peripheral that has the same ID as the SPI will not reset any of the registers that are shared with the SPI. It is therefore important to configure all relevant SPI registers explicitly to secure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

48.1.3 SPI master transaction sequence

An SPI master transaction is started by writing the first byte, which is to be transmitted by the SPI master, to the TXD register.

Since the transmitter is double buffered, the second byte can be written to the TXD register immediately after the first one. The SPI master will then send these bytes in the order they are written to the TXD register.

The SPI master is a synchronous interface, and for every byte that is sent, a different byte will be received at the same time; this is illustrated in *Figure 151: SPI master transaction* on page 515. Bytes that are received will be moved to the RXD register where the CPU can extract them by reading the register. The RXD register is double buffered in the same way as the TXD register, and a second byte can therefore be received at the same time as the first byte is being extracted from RXD by the CPU. The SPI master will generate a READY event every time a new byte is moved to the RXD register. The double buffered byte will be moved from RXD-1 to RXD as soon as the first byte is extracted from RXD. The SPI master will stop when there are no more bytes to send in TXD and TXD+1.



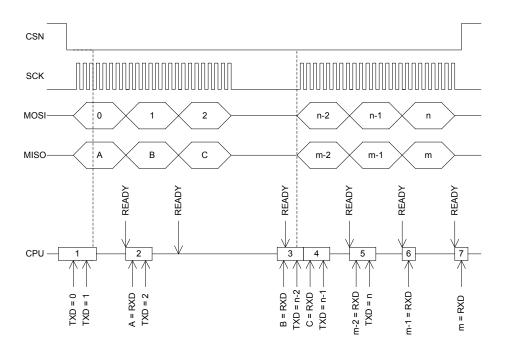


Figure 151: SPI master transaction

The READY event of the third byte transaction is delayed until B is extracted from RXD in occurrence number 3 on the horizontal lifeline. The reason for this is that the third event is generated first when C is moved from RXD-1 to RXD after B is read.

The SPI master will move the incoming byte to the RXD register after a short delay following the SCK clock period of the last bit in the byte. This also means that the READY event will be delayed accordingly, see *Figure 152: SPI master transaction* on page 515. Therefore, it is important that you always clear the READY event, even if the RXD register and the data that is being received is not used.

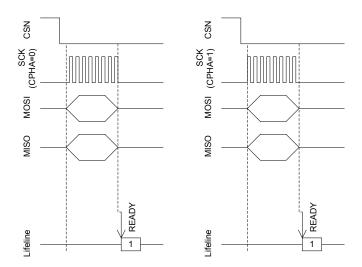


Figure 152: SPI master transaction



48.2 Registers

Table 123: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	SPI	SPI0	SPI master 0		Deprecated
0x40004000	SPI	SPI1	SPI master 1		Deprecated
0x40023000	SPI	SPI2	SPI master 2		Deprecated

Table 124: Register Overview

Register	Offset	Description	
EVENTS_READY	0x108	TXD byte sent and RXD byte received	
INTENSET	0x304	Enable interrupt	
INTENCLR	0x308	Disable interrupt	
ENABLE	0x500	Enable SPI	
PSELSCK	0x508	Pin select for SCK	Deprecated
PSELMOSI	0x50C	Pin select for MOSI	Deprecated
PSELMISO	0x510	Pin select for MISO	Deprecated
PSEL.SCK	0x508	Pin select for SCK	
PSEL.MOSI	0x50C	Pin select for MOSI	
PSEL.MISO	0x510	Pin select for MISO	
RXD	0x518	RXD register	
TXD	0x51C	TXD register	
FREQUENCY	0x524	SPI frequency	
CONFIG	0x554	Configuration register	

48.2.1 INTENSET

Address offset: 0x304

Enable interrupt

Bit	numbe	er		31	30	29	28	27	26	25	24	4 2	3 2:	2 2	21 2	0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id																																		Α	
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0	0) (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							D	esc	rip	tio	n																			
Α	RW	READY										W	/rite	e '1	1' to	Eı	nab	le i	inte	erru	pt	for	RE.	AD۱	ev ev	ent									
												Se	ee E	EVE	ENT	S _1	REA	D)	,																
			Set	1								E	nab	le																					
			Disabled	0								R	ead	l: D	isa	ble	d																		
			Enabled	1								R	ead	l: E	nak	le	b																		

48.2.2 INTENCLR

Address offset: 0x308

Disable interrupt

Bit r	numbe	r		31	. 30	29	28	3 27	7 2	6 2	5 2	4 2	23 2	2 2	1 2	20 1	19 :	18	17	16	15	14	13	12	11 1	10	9	8	7	6 !	5 4	4 :	3 2	2 1	. 0
Id																																	A	Ą	
Res	et 0x0	0000000		0	0	0	0	0) () () ()	0 (0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0)	0 () (0 () (0	0
Id	RW	Field	Value Id	Va	lue							0	Desc	crip	tio	n																			
Α	RW	READY										٧	Vrit	e '1	l' to) Di	isak	ole	int	erru	ıpt	for	REA	ADY	eve	nt									
												S	ee	EVE	NT	S_F	REA	ΙDΥ	,																
			Clear	1									Disa	ble																					
			Disabled	0								F	Read	d: D	isa	ble	d																		
			Enabled	1								F	Read	d: E	nak	oled	t																		



48.2.3 ENABLE

Address offset: 0x500

Enable SPI

Bitı	numb	er		31 30	29	28	27 2	26 2	25 2	24 2	23 2	2 2:	1 20	19	18	17	16 1	15 1	4 13	3 12	11	10	9	8 7	7 6	5	4	3	2	1 0
Id																												Α	Α	А А
Res	et 0x	0000000		0 0	0	0	0	0	0 (0 (0 0	0	0	0	0	0	0	0 (0	0	0	0	0	0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Value	:					C	Desc	ript	ion																	
Α	RW	ENABL								Е	nab	le c	r di	sabl	e SF	PI														
			Disabled	0						C	Disab	ole S	SPI																	
			Enabled	1						Е	nab	le S	PI																	

48.2.4 PSELSCK (Deprecated)

Address offset: 0x508 Pin select for SCK

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 18	3 17	16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	ΑА	A	А	Α	Α	Α	Α	A	4 <i>A</i>	. A	Α	Α	Α	Α	Α	Α .	Δ ,	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	1	. 1	1	1	1	1	1	1 1	. 1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	RW	PSELSCK					Pin	nur	nbe	r co	nfig	urat	tion	for	SPI	SCI	(sig	nal														
			Disconnected	0xFFFFFFF I		Dis	con	nec	t																							

48.2.5 PSELMOSI (Deprecated)

Address offset: 0x50C Pin select for MOSI

Bit r	number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			A A A A A A A	
Res	et 0xFFFFFFF		1 1 1 1 1 1 1 1	. 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Ia	RW Field	Value Id	Value	Description
A	RW FIELD RW PSELMOSI	Value Id	[031]	Description Pin number configuration for SPI MOSI signal

48.2.6 PSELMISO (Deprecated)

Address offset: 0x510 Pin select for MISO

Bit number		31 30 29 28 27	26 25 2	4 23 22	21 2	20 19	18 1	7 16	15	14 13	3 12	11 1	0 9	8	7	6	5	4 3	2	1 ()
Id		A A A A A	A A A	A A A	A	А А	ΑА	A	Α	А А	Α	A A	A	Α	Α	Α	Α	A A	A	Α ,	Δ
Reset 0xFFFFFFF		1 1 1 1 1	1 1 1	l 1 1	1	1 1	1 1	. 1	1	1 1	1	1 1	l 1	1	1	1	1	1 1	. 1	1 :	1
Id RW Field	Value Id	Value		Descr	iptio	n															
A RW PSELMISO		[031]	Pin nı	ımbe	r con	figura	tion	for	SPI N	1ISO	signa	al									
	Disconnected	0xFFFFFFF		Disco	nnect	t															

48.2.7 PSEL.SCK

Address offset: 0x508 Pin select for SCK

Bit	numbe	er		31	L 30	29	28	27	' 26	25	24	23	22	21	20	19	18 1	17 1	.6 1	.5 1	4 13	12	11	10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A	Δ,	Δ /	A A	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ ,	4 А
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	l 1	1	1	1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	alue	:						De	scri	ptic	n																		
Α	RW	PSELSCK		[0	31]						Pir	nu	mb	er c	onf	igur	atio	n f	or S	PI S	CK s	igna	ıl									
			Disconnected	Ох	FFF	FFF	FF					Dis	con	nec	t																		



48.2.8 PSEL.MOSI

Address offset: 0x50C Pin select for MOSI

Bitı	numb	er		31	L 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	.8 1	7 1	5 15	5 14	13	12	11 :	LO	9	8	7 6	5 5	4	3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	A A	4 <i>A</i>	A A	. A	Α	Α	Α	Α	A .	Α.	Α ,	4 4	λ Α	A	Α	Α	Α	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 1	L 1	1	1	1	1	1	1	1	1 :	1 1	l 1	. 1	1	1	1	1
Id	RW	Field	Value Id	Va	alue							De	scrip	otio	n																		
Α	RW	PSELMOSI		[0	31]						Pin	nur	nbe	er co	onfi	gura	atio	n fo	r SP	ΙM	OSI	sign	al									_
			Disconnected	0х	FFF	FFF	FF					Dis	con	nec	t																		

48.2.9 PSEL.MISO

Address offset: 0x510 Pin select for MISO

Bitı	numbe	er		31	. 30	29	28	27	7 26	25	24	23	22 :	21	20 :	19 :	18 1	7 1	16 1	15 :	14 1	.3 1	.2 1	111	0 9	9	8 7	7	6	5	4	3 2	2 1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ.	A	Α	A	Δ.	Δ.	A A	Α Α	Α,	Δ ,	Δ.	Α.	Α	Α	A A	A A	A
Res	et 0xF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 :	1 :	L	1 :	1	1	1	1	1 :	L 1	1
Id	RW	Field	Value Id	Va	lue							De	scrip	otic	n																			
Α	RW	PSELMISO		[0	31]						Pin	nur	mbe	er c	onf	igur	atio	on f	or	SPI	MIS	0 9	ign	al									
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t																			

48.2.10 RXD

Address offset: 0x518

RXD register

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Id			A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
A R RXD			RX data received. Double buffered

48.2.11 TXD

Address offset: 0x51C

TXD register

Bit number		31 30 29 28 27 2	26 25 24 23 22 21 20 19 18 17	16 15 14 13 12 11 10 9 8	3 7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	000000000
Id RW Field	Value Id	Value	Description		
A RW TXD			TX data to send. Doub	le buffered	

48.2.12 FREQUENCY

Address offset: 0x524

SPI frequency

Bit	numbe	r		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 1	11 1	LO	9 8	3	7 6	5 5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	Α.	A	A A	Δ ,	Δ Α	Α Δ	A	Α	Α	A A
Res	et 0x0	400000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () () (0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue							De	cri	otic	n																		
Α	RW	FREQUENCY										SPI	ma	ste	r da	ita	rat	е															
			K125	0x(020	000	000					125	kb	ps																			
			K250	0x(040	000	000					250) kb	ps																			
			K500	0x(080	000	000					500) kb	ps																			
			M1	0x	100	000	000					1 N	1bp	S																			



Bit number		31 30 29 28 27	' 26 25 24 23 22 21 20	19 18 17 16 15 14 1	13 12 11 10 9 8 7	7 6 5 4 3 2 1 0
Id		A A A A A	A A A A A A	A A A A A A	A A A A A A	A A A A A A A
Reset 0x04000000		0 0 0 0 0	1 0 0 0 0 0 0	0 0 0 0 0 0	000000	0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description			
	M2	0x20000000	2 Mbps			
	M2 M4	0x20000000 0x40000000	2 Mbps 4 Mbps			

48.2.13 CONFIG

Address offset: 0x554 Configuration register

Bit n	umbe	r		31	30 2	29 :	28 2	27 2	26 2	5 24	4 2	3 22	21	20	19	18	17	16	15	14	13	12	11 1	10 9	9 8	3 7	7 6	5 5	4	3	2	1 0
Id																															С	ВА
Rese	t 0x0	0000000		0	0	0	0	0	0 (0) (0	0	0	0	0	0	0	0	0	0	0	0	0 () (0 () (0	0	0	0	0 0
Id	RW	Field	Value Id	Va	lue						D	escr	iptic	n																		
Α	RW	ORDER									В	it or	der																			
			MsbFirst	0							N	1ost	signi	ifica	ant	bit	shi	fte	d ou	ut fi	rst											
			LsbFirst	1							Le	east	signi	ifica	ant	bit	shi	fte	d ou	ut fi	rst											
В	RW	СРНА									S	erial	cloc	k (S	SCK) pł	nase	9														
			Leading	0							S	amp	le or	ı le	adiı	ng e	edg	e o	fclo	ock,	shi	ft s	eria	l da	ta c	n tı	aili	ng				
											е	dge																				
			Trailing	1							S	amp	le or	n tra	ailir	ng e	edge	e of	clc	ck,	shi	ft se	erial	dat	a o	n le	adi	ng				
											е	dge																				
С	RW	CPOL									S	erial	cloc	k (S	SCK) po	olar	ity														
			ActiveHigh	0							Α	ctive	hig	h																		
			ActiveLow	1							Α	ctive	low	/																		

48.3 Electrical specification

48.3.1 SPI master interface

Symbol	Description	Min.	Тур.	Max.	Units
f _{SPI}	Bit rates for SPI ³⁸			8 ³⁹	Mbps
I _{SPI,2Mbps}	Run current for SPI, 2 Mbps			50	μΑ
I _{SPI,8Mbps}	Run current for SPI, 8 Mbps			50	μΑ
I _{SPI,IDLE}	Idle current for SPI (STARTed, no CSN activity)		<1		μΑ
t _{SPI,START,LP}	Time from writing TXD register to transmission started, low		t _{SPI,START}	,CI	μs
	power mode		+		
			t _{START_HE}	IN	
t _{SPI,START,CL}	Time from writing TXD register to transmission started, constant		1		μs
	latency mode				

48.3.2 Serial Peripheral Interface (SPI) Master timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
t _{SPI,CSCK,8Mbps}	SCK period at 8Mbps		125		ns
t _{SPI,CSCK,4Mbps}	SCK period at 4Mbps		250		ns
t _{SPI,CSCK,2Mbps}	SCK period at 2Mbps		500		ns
t _{SPI,RSCK,LD}	SCK rise time, low drive ^a			t _{RF,25pF}	
t _{SPI,RSCK,HD}	SCK rise time, high drive ^a			t _{HRF,25pF}	
t _{SPI,FSCK,LD}	SCK fall time, low drive ^a			t _{RF,25pF}	
t _{SPI,FSCK,HD}	SCK fall time, high drive ^a			t _{HRF,25pF}	

Higher bit rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.

The actual maximum data rate depends on the slave's CLK to MISO and MOSI setup and hold timings.

^a At 25pF load, including GPIO capacitance, see GPIO spec.



Symbol	Description	Min.	Тур.	Max.	Units
t _{SPI,WHSCK}	SCK high time ^a	(0.5*t _{CSC}	:ĸ]		
		- t _{RSCK}			
$t_{SPI,WLSCK}$	SCK low time ^a	(0.5*t _{CSC}	:ĸ]		
		$-t_{FSCK}$			
t _{SPI,SUMI}	MISO to CLK edge setup time	19			ns
t _{SPI,HMI}	CLK edge to MISO hold time	18			ns
t _{SPI,VMO}	CLK edge to MOSI valid			59	ns
t _{SPI,HMO}	MOSI hold time after CLK edge	20			ns

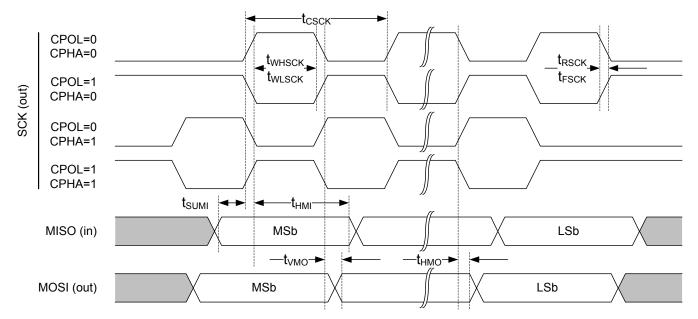


Figure 153: SPI master timing diagram



49 TWI — I²C compatible two-wire interface

The TWI master is compatible with I²C operating at 100 kHz and 400 kHz.

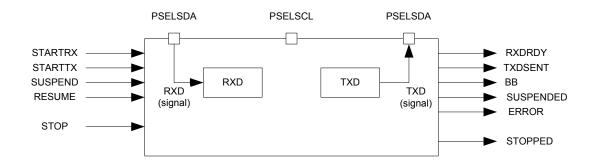


Figure 154: TWI master's main features

49.1 Functional description

This TWI master is not compatible with CBUS. The TWI transmitter and receiver are single buffered.

See, Figure 154: TWI master's main features on page 521.

A TWI setup comprising one master and three slaves is illustrated in *Figure 155: A typical TWI setup comprising one master and three slaves* on page 521. This TWI master is only able to operate as the only master on the TWI bus.

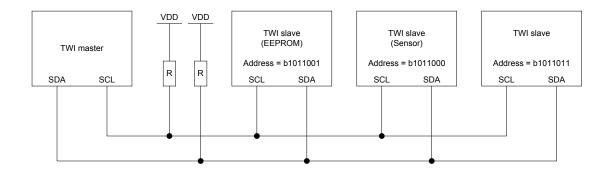


Figure 155: A typical TWI setup comprising one master and three slaves

This TWI master supports clock stretching performed by the slaves. The TWI master is started by triggering the STARTTX or STARTRX tasks, and stopped by triggering the STOP task.

If a NACK is clocked in from the slave, the TWI master will generate an ERROR event.

49.2 Master mode pin configuration

The different signals SCL and SDA associated with the TWI master are mapped to physical pins according to the configuration specified in the PSELSCL and PSELSDA registers respectively.

If a value of 0xFFFFFFF is specified in any of these registers, the associated TWI master signal is not connected to any physical pin. The PSELSCL and PSELSDA registers and their configurations are only used



as long as the TWI master is enabled, and retained only as long as the device is in ON mode. PSELSCL and PSELSDA must only be configured when the TWI is disabled.

To secure correct signal levels on the pins used by the TWI master when the system is in OFF mode, and when the TWI master is disabled, these pins must be configured in the GPIO peripheral as described in *Table 125: GPIO configuration* on page 522.

Only one peripheral can be assigned to drive a particular GPIO pin at a time, failing to do so may result in unpredictable behavior.

Table 125: GPIO configuration

TWI master signal	TWI master pin	Direction	Drive strength	Output value
SCL	As specified in PSELSCL	Input	SOD1	Not applicable
SDA	As specified in PSELSDA	Input	SOD1	Not applicable

49.3 Shared resources

The TWI shares registers and other resources with other peripherals that have the same ID as the TWI.

Therefore, you must disable all peripherals that have the same ID as the TWI before the TWI can be configured and used. Disabling a peripheral that has the same ID as the TWI will not reset any of the registers that are shared with the TWI. It is therefore important to configure all relevant TWI registers explicitly to secure that it operates correctly.

The Instantiation table in *Instantiation* on page 24 shows which peripherals have the same ID as the TWI.

49.4 Master write sequence

A TWI master write sequence is started by triggering the STARTTX task. After the STARTTX task has been triggered, the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 0 (WRITE=0, READ=1).

The address must match the address of the slave device that the master wants to write to. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK=1) generated by the slave.

After receiving the ACK bit, the TWI master will clock out the data bytes that are written to the TXD register. Each byte clocked out from the master will be followed by an ACK/NACK bit clocked in from the slave. A TXDSENT event will be generated each time the TWI master has clocked out a TXD byte, and the associated ACK/NACK bit has been clocked in from the slave.

The TWI master transmitter is single buffered, and a second byte can only be written to the TXD register after the previous byte has been clocked out and the ACK/NACK bit clocked in, that is, after the TXDSENT event has been generated.

If the CPU is prevented from writing to TXD when the TWI master is ready to clock out a byte, the TWI master will stretch the clock until the CPU has written a byte to the TXD register.

A typical TWI master write sequence is illustrated in *Figure 156: The TWI master writing data to a slave* on page 523. Occurrence 3 in the figure illustrates delayed processing of the TXDSENT event associated with TXD byte 1. In this scenario the TWI master will stretch the clock to prevent writing erroneous data to the slave.



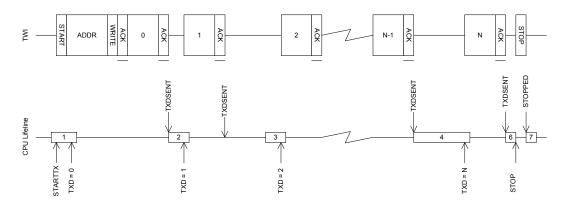


Figure 156: The TWI master writing data to a slave

The TWI master write sequence is stopped when the STOP task is triggered whereupon the TWI master will generate a stop condition on the TWI bus.

49.5 Master read sequence

A TWI master read sequence is started by triggering the STARTRX task. After the STARTRX task has been triggered the TWI master will generate a start condition on the TWI bus, followed by clocking out the address and the READ/WRITE bit set to 1 (WRITE = 0, READ = 1).

The address must match the address of the slave device that the master wants to read from. The READ/WRITE bit is followed by an ACK/NACK bit (ACK=0 or NACK = 1) generated by the slave.

After having sent the ACK bit the TWI slave will send data to the master using the clock generated by the master.

The TWI master will generate a RXDRDY event every time a new byte is received in the RXD register.

After receiving a byte, the TWI master will delay sending the ACK/NACK bit by stretching the clock until the CPU has extracted the received byte, that is, by reading the RXD register.

The TWI master read sequence is stopped by triggering the STOP task. This task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the stop condition.

A typical TWI master read sequence is illustrated in *Figure 157: The TWI master reading data from a slave* on page 524. Occurrence 3 in this figure illustrates delayed processing of the RXDRDY event associated with RXD byte B. In this scenario the TWI master will stretch the clock to prevent the slave from overwriting the contents of the RXD register.



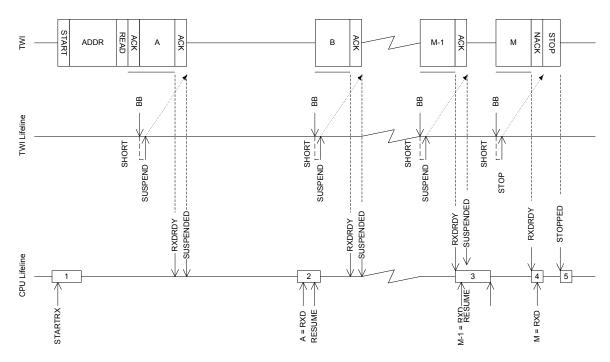


Figure 157: The TWI master reading data from a slave

49.6 Master repeated start sequence

A typical repeated start sequence is one in which the TWI master writes one byte to the slave followed by reading M bytes from the slave. Any combination and number of transmit and receive sequences can be combined in this fashion. Only one shortcut to STOP can be enabled at any given time.

The figure below illustrates a repeated start sequence where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between.

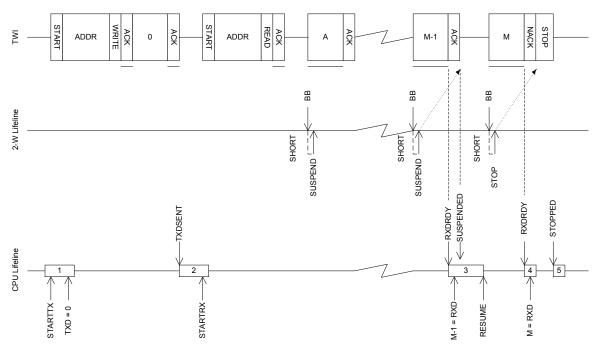


Figure 158: A repeated start sequence, where the TWI master writes one byte, followed by reading M bytes from the slave without performing a stop in-between



To generate a repeated start after a read sequence, a second start task must be triggered instead of the STOP task, that is, STARTRX or STARTTX. This start task must be triggered before the last byte is extracted from RXD to ensure that the TWI master sends a NACK back to the slave before generating the repeated start condition.

49.7 Low power

When putting the system in low power and the peripheral is not needed, lowest possible power consumption is achieved by stopping, and then disabling the peripheral.

The STOP task may not be always needed (the peripheral might already be stopped), but if it is sent, software shall wait until the STOPPED event was received as a response before disabling the peripheral through the ENABLE register.

49.8 Registers

Table 126: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40003000	TWI	TWI0	Two-wire interface master 0		Deprecated
0x40004000	TWI	TWI1	Two-wire interface master 1		Deprecated

Table 127: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start TWI receive sequence
TASKS_STARTTX	0x008	Start TWI transmit sequence
TASKS_STOP	0x014	Stop TWI transaction
TASKS_SUSPEND	0x01C	Suspend TWI transaction
TASKS_RESUME	0x020	Resume TWI transaction
EVENTS_STOPPED	0x104	TWI stopped
EVENTS_RXDREADY	0x108	TWI RXD byte received
EVENTS_TXDSENT	0x11C	TWI TXD byte sent
EVENTS_ERROR	0x124	TWI error
EVENTS_BB	0x138	TWI byte boundary, generated before each byte that is sent or received
EVENTS_SUSPENDED	0x148	TWI entered the suspended state
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x4C4	Error source
ENABLE	0x500	Enable TWI
PSELSCL	0x508	Pin select for SCL
PSELSDA	0x50C	Pin select for SDA
RXD	0x518	RXD register
TXD	0x51C	TXD register
FREQUENCY	0x524	TWI frequency
ADDRESS	0x588	Address used in the TWI transfer

49.8.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number		31 30 29 28 27 26 2	5 24 23 22 21 20 19 18 :	17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Id					ВА
Reset 0x00000000		0 0 0 0 0 0	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description		

A RW BB_SUSPEND

Shortcut between BB event and SUSPEND task



Bit number		31 30 29 28 27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			В А
Reset 0x00000000		0 0 0 0 0 0 0	$0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \$
Id RW Field	Value Id	Value	Description
			See EVENTS_BB and TASKS_SUSPEND
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut
B RW BB_STOP			Shortcut between BB event and STOP task
			See EVENTS_BB and TASKS_STOP
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

49.8.2 INTENSET

Address offset: 0x304

Enable interrupt

		у и поттарт																															
	numb	er		31	L 30	29	28 2	27 2	6 2	5 24	4 2	23 2	22 21 2	20 1			17 :	16	15		13	12	11					6	5	4 3			
Id																F				Ε					D		С					А	
Res		0000000		0			0	0 (0 0	0			0 0		0 (0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0
Id		Field	Value Id	V	alue								criptio																				
Α	RW	STOPPED									٧	Vrit	ite '1' te	o Er	nabl	e ii	nte	rru	pt f	or	STO	PP	ED	eve	nt								
											S	ee	EVENT	'S_S	STO	PPI	ED																
			Set	1							Ε	nal	ble																				
			Disabled	0							R	lea	d: Disa	ble	d																		
			Enabled	1							R	lea	d: Enal	oled	b																		
В	RW	RXDREADY									٧	Vrit	ite '1' t	o Er	nabl	e ii	nte	rru	pt f	or	RXD	RE	AD'	Y ev	en								
											S	ee	EVENT	5 1	RXD	RE	4D)	γ															
			Set	1									ıble	_																			
			Disabled	0							R	lea	d: Disa	ble	d																		
			Enabled	1							R	lea	d: Enal	oled	d																		
С	RW	TXDSENT									٧	Vrit	ite '1' t	o Er	nabl	e ii	nte	rru	pt f	or	TXD	SEI	NT	evei	nt								
											S	ee	EVENT	S	TXD.	SEI	VΤ																
			Set	1									ble	Ī																			
			Disabled	0							R	lea	d: Disa	ble	d																		
			Enabled	1							R	lea	d: Enal	oled	d																		
D	RW	ERROR									٧	Vrit	ite '1' t	o Er	nabl	e ii	nte	rru	pt 1	or	ERR	OR	ev	ent									
											S	ee	EVENT	'S_I	ERR	OR																	
			Set	1							Ε	nal	ble																				
			Disabled	0							R	lea	d: Disa	ble	d																		
			Enabled	1							R	lea	d: Enal	oled	b																		
Е	RW	ВВ									٧	Vrit	ite '1' t	o Er	nabl	e ii	nte	rru	pt f	or	вв е	eve	nt										
											S	ee	EVENT	'S 1	ВВ																		
			Set	1									ıble	_																			
			Disabled	0							R	lea	d: Disa	ble	d																		
			Enabled	1							R	lea	id: Enal	oled	d																		
F	RW	SUSPENDED									٧	Vrit	ite '1' t	o Er	nabl	e ii	nte	rru	pt f	or	sus	PEI	NDI	ED e	eve	nt							
											S	ee	EVEN1	3	SUSI	PEI	VDE	D															
			Set	1									ıble																				
			Disabled	0									id: Disa	ble	d																		
			Enabled	1									d: Enal																				

49.8.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	numb	er		31 30	29 2	8 27	26 2	5 24	1 23	22 21	20 1	.9 1	8 17	16	15 :	14 13	3 12	11	10	9 1	8 7	6	5	4 3	2	1 (
Id												F	=			E				D	С				В	Α
Res	et 0x0	0000000		0 0	0 (0 0	0 (0 0	0	0 0	0 (0 (0 0	0	0	0 0	0	0	0	0	0 0	0	0	0 0	0	0 (
Id	RW	Field	Value Id	Value	!				De	escripti	on															
Α	RW	STOPPED							Wı	rite '1'	to Di	sabl	le int	erru	ıpt f	or S	ГОР	PED	eve	nt						
									Se	e <i>EVEN</i>	ITS_S	TOF	PPED	ı												
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	b														
			Enabled	1					Re	ad: Ena	abled	ı														
В	RW	RXDREADY							Wı	rite '1'	to Di	sabl	le int	erru	ıpt f	or R	XDR	EAD	Y ev	ent						
									Se	e <i>EVEN</i>	ITS_R	RXDI	READ	ŊΥ												
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	d														
			Enabled	1					Re	ad: Ena	abled	ı														
С	RW	TXDSENT							Wı	rite '1'	to Di	sabl	le int	erru	ıpt f	or T	KDSI	NT	eve	nt						
									Se	e <i>EVEN</i>	ITS_T	XDS	SENT													
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	b														
			Enabled	1					Re	ad: Ena	abled	I														
D	RW	ERROR							Wı	rite '1'	to Di	sabl	le int	erru	ıpt f	or El	RRO	R ev	ent							
									Se	e <i>EVEN</i>	ITS_E	RRC	OR													
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	d														
			Enabled	1					Re	ad: Ena	abled	ı														
E	RW	ВВ							Wı	rite '1'	to Di	sabl	le int	erru	ıpt f	or B	B ev	ent								
									Se	e <i>EVEN</i>	ITS_B	BB														
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	b														
			Enabled	1					Re	ad: Ena	abled	I														
F	RW	SUSPENDED							Wı	rite '1'	to Di	sabl	le int	erru	ıpt f	or SI	JSPI	END	ED e	ever	it					
									Se	e <i>EVEN</i>	ITS_S	USF	PEND	ED												
			Clear	1					Dis	sable																
			Disabled	0					Re	ad: Dis	abled	b														
			Enabled	1					Re	ad: Ena	abled	ı														

49.8.4 ERRORSRC

Address offset: 0x4C4

Error source

	numbe	er		31	30 2	9 2	8 27	7 26	25	24	1 23 2	22 2	1 20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1 0
ld Res	et 0x0	0000000		0	0 0) (0 0	0	0	0	0	0 (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		3 A 0 0
Id	RW	Field	Value Id	Val	ue						Des	crip	tion																			
Α	RW	OVERRUN									Ove	rrur	erro	or																		
													yte v e fro							•				-			by					
			NotPresent	0							Rea	d: n	o ove	errı	ın c	occi	ırec	ł														
			Present	1							Rea	d: o	verru	ın o	occi	ure	t															
			Clear	1							Writ	te: c	lear	err	or c	on v	vrit	ing	'1'													
В	RW	ANACK									NAC	CK re	eceiv	ed	afte	er s	end	ing	the	e ad	dre	ess (wri	te '	1' to	clo	ear))				
			NotPresent	0							Rea	d: ei	rrorı	not	pre	esei	nt															
			Present	1							Rea	d: ei	rror	pre	sen	t																
			Clear	1							Writ	te: c	lear	err	or c	on v	vrit	ing	'1'													
С	RW	DNACK									NAC	K re	eceiv	ed	afte	er s	end	ing	a d	ata	by	te (writ	e '1	' to	cle	ear)					
			NotPresent	0							Rea	d: ei	rror ı	not	pre	esei	nt															



Bit number		31 30 29 28 27 26 25 24	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			C B A
Reset 0x00000000		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
	Present	1	Read: error present
	Clear	1	Write: clear error on writing '1'

49.8.5 ENABLE

Address offset: 0x500

Enable TWI

Bit n	umbe	r		33	1 30	29	28	27	26	25	24	23	22 :	21 :	20 :	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	L 0
Id																																A A	A A	А А
Rese	t 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0
Id	RW	Field	Value Id	V	alue)						Des	crip	otio	n																			
Α	RW	ENABLE										Ena	ble	or	disa	able	٠T٧	۷I																
			Disabled	0								Disa	able	: TV	VI																			
			Enabled	5								Ena	ble	ΤW	/I																			

49.8.6 PSELSCL

Address offset: 0x508
Pin select for SCL

Bit	numb	er		31	30	29	28	27	26	25	24	23	22	21	20 :	19 1	l8 1	7 1	5 15	14	13	12	11 :	10	9	8	7	6 !	5 .	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Α Α	A	Α	Α	Α	Α	A	Α	Α.	Α.	A A	Δ.	ДД	A	Α	Α
Res	et Oxl	FFFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1 1	L 1	. 1	1	1	1	1	1	1	1	1	1 :	1	1 1	. 1	1	1
Id	RW	Field	Value Id	Va	lue							De	scri	ptic	n																		
Α	RW	PSELSCL		[0.	.31]							Pir	nu	mb	er c	onfi	gura	atio	n fo	r TV	VI S	CL s	igna	ıl									
			Disconnected	0x	FFFI	FFF	FF					Dis	con	nec	t																		

49.8.7 PSELSDA

Address offset: 0x50C Pin select for SDA

Bit	numbe	er		31	L 30	29	28	27	26	25	24	23	22 2	1 2	0 19	9 18	3 17	16	15	14	13 1	.2 1	1 10	9	8	7	6	5	4	3 2	1	. 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Δ,	Д Д	. 4	Α	Α	Α	Α	A	Δ /	A A	Α	Α	Α	Α	Α	Α	A A	A	A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	1	. 1	1	1	1	1	1 1	l 1	1	1	1	1	1	1	1 :	. 1	. 1
Id	RW	Field	Value Id	Va	alue							Des	crip	tio	n																	
Α	RW	PSELSDA		[0	31]						Pin	nun	nbe	r co	nfig	urat	tion	for	TW	I SD	A si	gnal									
			Disconnected	0x	FFF	FFF	FF					Disc	conr	ect	t																	

49.8.8 RXD

Address offset: 0x518

RXD register

Bit number		31 30 29 28 27	26 25 24 23 22 21 20 19 18 17	7 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Id					A A A A A A A
Reset 0x00000000		0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
ld RW Field	Value Id	Value	Description		
A R RXD			RXD register		

49.8.9 TXD

Address offset: 0x51C

TXD register



В	Bit nu	umbe	er		31	30 29	9 2	28 2	7 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	2 1	0
																																		_
10	d																											Α	Α	Α	A A	Α Α	A A	Α
R	Reset	t 0x0	0000000		0	0 0) (0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 0	0 (0
10	d	RW	Field	Value Id	Val	ue						De	scri	ipti	on																			
	_														•••																			
		RW	TXD										D re	: _																				
I	_			Value Id	Val	ue								•																				

49.8.10 FREQUENCY

Address offset: 0x524

TWI frequency

Bit	num	nbei			31	. 30	29	28	27	26	5 25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0
Id					Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	ΑА	Α	Α
Re	set 0	0x04	000000		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id	R	w	Field	Value Id	Va	lue							De	escri	ptic	on																			
Α	R۱	W	FREQUENCY										TV	VI m	ast	er c	loc	k fr	equ	ıen	су														
				K100	0x	019	800	000					10	0 kb	ps																				
				K250	0x	040	000	000					25	0 kb	ps																				
				K400	Λv	:066	ลกด	ากก					40	0 kb	nnc	lact	tual	rat	۸ ۵	10	256	. Lh	nc۱												

49.8.11 ADDRESS

Address offset: 0x588

Address used in the TWI transfer

Bitı	numb	er		31 30 2	9 28 2	27 26	25	24	23 2	2 21	L 20	19	18 :	17 1	6 1	5 1	4 13	3 12	11	10	9	8	7	6	5	4 3	2	1	0
Id																								Α	Α	A A	A	Α	Α
Res	et 0x0	0000000		0 0 (0 0	0 0	0	0	0 (0 0	0	0	0	0	0 (0	0	0	0	0	0	0	0	0	0	0 0	0	0	0
Id	RW	Field	Value Id	Value					Desc	ript	ion																		
Δ	RW/	ADDRESS							Δddr	ress	IISE	d in	the	T\//	l tra	nsf	er												

49.9 Electrical specification

49.9.1 TWI interface electrical specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWI}	Bit rates for TWI ⁴⁰	100		400	kbps
I _{TWI,100kbps}	Run current for TWI, 100 kbps		50		μΑ
I _{TWI,400kbps}	Run current for TWI, 400 kbps		50		μΑ
t _{TWI,START,LP}	Time from STARTRX/STARTTX task to transmission started, Low		t _{TWI,STAI}	RT,C	μs
	power mode		+		
			t _{START_H}	IFIN	
t _{TWI,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1.5		μs
	Constant latency mode				

49.9.2 Two Wire Interface (TWI) timing specifications

Symbol	Description	Min.	Тур.	Max.	Units
f _{TWI,SCL,100kbps}	SCL clock frequency, 100 kbps		100		kHz
f _{TWI,SCL,250kbps}	SCL clock frequency, 250 kbps		250		kHz
f _{TWI,SCL,400kbps}	SCL clock frequency, 400 kbps		400		kHz
t _{TWI,SU_DAT}	Data setup time before positive edge on SCL – all modes	300			ns
t _{TWI,HD_DAT}	Data hold time after negative edge on SCL – all modes	500			ns
t _{TWI,HD_STA,100kbps}	TWI master hold time for START and repeated START condition,	10000			ns
	100 kbps				

⁴⁰ Higher bit rates or stronger pull-ups may require GPIOs to be set as High Drive, see GPIO chapter for more details.



Symbol	Description	Min.	Тур.	Max.	Units
t _{TWI,HD_STA,250kbps}	TWI master hold time for START and repeated START condition,	4000			ns
	250kbps				
t _{TWI,HD_STA,400kbps}	TWI master hold time for START and repeated START condition,	2500			ns
	400 kbps				
$t_{\text{TWI},\text{SU_STO},100\text{kbps}}$	TWI master setup time from SCL high to STOP condition, 100	5000			ns
	kbps				
$t_{TWI,SU_STO,250kbps}$	TWI master setup time from SCL high to STOP condition, 250	2000			ns
	kbps				
$t_{TWI,SU_STO,400kbps}$	TWI master setup time from SCL high to STOP condition, 400	1250			ns
	kbps				
t _{TWI,BUF,100kbps}	TWI master bus free time between STOP and START conditions,	5800			ns
	100 kbps				
t _{TWI,BUF,250kbps}	TWI master bus free time between STOP and START conditions,	2700			ns
	250 kbps				
t _{TWI,BUF,400kbps}	TWI master bus free time between STOP and START conditions,	2100			ns
	400 kbps				

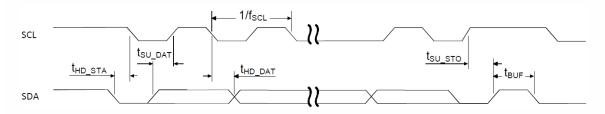


Figure 159: TWI timing diagram, 1 byte transaction



50 UART — Universal asynchronous receiver/ transmitter

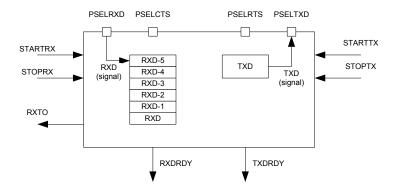


Figure 160: UART configuration

50.1 Functional description

Listed here are the main features of UART.

The UART implements support for the following features:

- Full-duplex operation
- · Automatic flow control
- Parity checking and generation for the 9th data bit

As illustrated in *Figure 160: UART configuration* on page 531, the UART uses the TXD and RXD registers directly to transmit and receive data. The UART uses one stop bit.

50.2 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UART are mapped to physical pins according to the configuration specified in the PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers respectively.

If a value of 0xFFFFFFFF is specified in any of these registers, the associated UART signal will not be connected to any physical pin. The PSELRXD, PSELCTS, PSELRTS, and PSELTXD registers and their configurations are only used as long as the UART is enabled, and retained only for the duration the device is in ON mode. PSELRXD, PSELCTS, PSELRTS and PSELTXD must only be configured when the UART is disabled.

To secure correct signal levels on the pins by the UART when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in *Pin configuration* on page 531.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

Table 128: GPIO configuration

UART pin	Direction		Output value
RXD		nput	Not applicable
CTS		nput	Not applicable
RTS	C	utput	1
TXD	C	output	1



50.3 Shared resources

The UART shares registers and other resources with other peripherals that have the same ID as the UART.

Therefore, you must disable all peripherals that have the same ID as the UART before the UART can be configured and used. Disabling a peripheral that has the same ID as the UART will not reset any of the registers that are shared with the UART. It is therefore important to configure all relevant UART registers explicitly to ensure that it operates correctly.

See the Instantiation table in *Instantiation* on page 24 for details on peripherals and their IDs.

50.4 Transmission

A UART transmission sequence is started by triggering the STARTTX task.

Bytes are transmitted by writing to the TXD register. When a byte has been successfully transmitted the UART will generate a TXDRDY event after which a new byte can be written to the TXD register. A UART transmission sequence is stopped immediately by triggering the STOPTX task.

If flow control is enabled a transmission will be automatically suspended when CTS is deactivated and resumed when CTS is activated again, as illustrated in *Figure 161: UART transmission* on page 532. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended. For more information, see *Suspending the UART* on page 533.

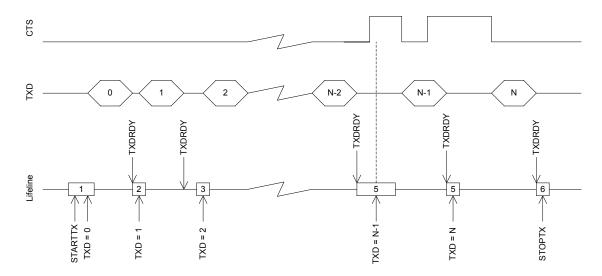


Figure 161: UART transmission

50.5 Reception

A UART reception sequence is started by triggering the STARTRX task.

The UART receiver chain implements a FIFO capable of storing six incoming RXD bytes before data is overwritten. Bytes are extracted from this FIFO by reading the RXD register. When a byte is extracted from the FIFO a new byte pending in the FIFO will be moved to the RXD register. The UART will generate an RXDRDY event every time a new byte is moved to the RXD register.

When flow control is enabled, the UART will deactivate the RTS signal when there is only space for four more bytes in the receiver FIFO. The counterpart transmitter is therefore able to send up to four bytes after the RTS signal is deactivated before data is being overwritten. To prevent overwriting data in the FIFO, the counterpart UART transmitter must therefore make sure to stop transmitting data within four bytes after the RTS line is deactivated.



The RTS signal will first be activated again when the FIFO has been emptied, that is, when all bytes in the FIFO have been read by the CPU, see *Figure 162: UART reception* on page 533.

The RTS signal will also be deactivated when the receiver is stopped through the STOPRX task as illustrated in *Figure 162: UART reception* on page 533. The UART is able to receive four to five additional bytes if they are sent in succession immediately after the RTS signal has been deactivated. This is possible because the UART is, even after the STOPRX task is triggered, able to receive bytes for an extended period of time dependent on the configured baud rate. The UART will generate a receiver timeout event (RXTO) when this period has elapsed.

To prevent loss of incoming data the RXD register must only be read one time following every RXDRDY event.

To secure that the CPU can detect all incoming RXDRDY events through the RXDRDY event register, the RXDRDY event register must be cleared before the RXD register is read. The reason for this is that the UART is allowed to write a new byte to the RXD register, and therefore can also generate a new event, immediately after the RXD register is read (emptied) by the CPU.

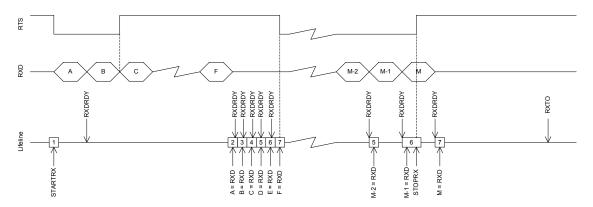


Figure 162: UART reception

As indicated in occurrence 2 in the figure, the RXDRDY event associated with byte B is generated first after byte A has been extracted from RXD.

50.6 Suspending the UART

The UART can be suspended by triggering the SUSPEND task.

SUSPEND will affect both the UART receiver and the UART transmitter, i.e. the transmitter will stop transmitting and the receiver will stop receiving. UART transmission and reception can be resumed, after being suspended, by triggering STARTTX and STARTRX respectively.

Following a SUSPEND task, an ongoing TXD byte transmission will be completed before the UART is suspended.

When the SUSPEND task is triggered, the UART receiver will behave in the same way as it does when the STOPRX task is triggered.

50.7 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.



50.8 Using the UART without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

50.9 Parity configuration

When parity is enabled, the parity will be generated automatically from the even parity of TXD and RXD for transmission and reception respectively.

50.10 Registers

Table 129: Instances

Base address	Peripheral	Instance	Description	Configuration	
0x40002000	UART	UART0	Universal Asynchronous Receiver/		Deprecated
			Transmitter		

Table 130: Register Overview

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_SUSPEND	0x01C	Suspend UART
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ERROR	0x124	Error detected
EVENTS_RXTO	0x144	Receiver timeout
SHORTS	0x200	Shortcut register
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSELRTS	0x508	Pin select for RTS
PSELTXD	0x50C	Pin select for TXD
PSELCTS	0x510	Pin select for CTS
PSELRXD	0x514	Pin select for RXD
RXD	0x518	RXD register
TXD	0x51C	TXD register
BAUDRATE	0x524	Baud rate
CONFIG	0x56C	Configuration of parity and hardware flow control

50.10.1 SHORTS

Address offset: 0x200

Shortcut register

Bit number	31 30 29 28 27	26 25 24 23 22 21 20 19 18 17 1	16 15 14 13 12 11 10 9	8 7 6 5 4 3 2 1 0
Id				ВА
Reset 0x00000000	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0
Id RW Field Value	ld Value	Description		

A RW CTS_STARTRX

Shortcut between CTS event and STARTRX task



Bit number		31 30 29 28 27 26 25 2	4 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id			ВА
Reset 0x00000000		0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value	Description
			See EVENTS_CTS and TASKS_STARTRX
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut
B RW NCTS_STOPRX			Shortcut between NCTS event and STOPRX task
			See EVENTS_NCTS and TASKS_STOPRX
	Disabled	0	Disable shortcut
	Enabled	1	Enable shortcut

50.10.2 INTENSET

Address offset: 0x304

Enable interrupt

		лионарс																															
Bit n	numbe	er		31	. 30	29	28 2	27 2	6 25	5 24	1 2	3 2	22 21	20	19 3	18	17	16	15	14	13	12	11	10	9	8	7	6 !	5 4	4 3	2	1	0
Id																	F								Ε		D				С	В	Α
Rese	et 0x0	0000000		0	0	0	0	0 (0	0	0)	0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 (0 (0	0	0	0
Id	RW	Field	Value Id	Va	lue						D	es	scripti	on																			
Α	RW	CTS									W	Vri	ite '1' 1	to E	nab	le i	nte	rru	pt	or	CTS	ev	ent										
											Se	ee	EVEN	ITS_	CTS																		
			Set	1							Eı	na	able																				
			Disabled	0							R	ea	ad: Dis	abl	ed																		
			Enabled	1							R	ea	ad: Ena	able	ed																		
В	RW	NCTS									W	Vri	ite '1'	to E	nab	le i	nte	rru	pt ·	or	NCT	S e	ven	t									
											Se	ee	EVEN	ITS	NCT	rs																	
			Set	1									able	_																			
			Disabled	0							R	ea	ad: Dis	abl	ed																		
			Enabled	1							R	ea	ad: Ena	able	ed																		
С	RW	RXDRDY									W	Vri	ite '1'	to E	nab	le i	nte	rru	pt ·	or	RXD	RD	Y e	vent	t								
											Se	ee	EVEN	ITS_	RXD	ORD	ΟY																
			Set	1							Ei	na	able																				
			Disabled	0							R	ea	ad: Dis	abl	ed																		
			Enabled	1							R	ea	ad: Ena	able	ed																		
D	RW	TXDRDY									W	Vri	ite '1'	to E	nab	le i	nte	rru	pt	or	TXD	RD	Y ev	/ent									
											Se	ee	EVEN	ITS_	TXD	RD	ŊΥ																
			Set	1							Eı	na	able																				
			Disabled	0							R	ea	ad: Dis	abl	ed																		
			Enabled	1							R	ea	ad: Ena	able	ed																		
Е	RW	ERROR									W	Vri	ite '1'	to E	nab	le i	nte	rru	pt	or	ERR	OR	eve	ent									
											Se	ee	EVEN	ITS_	ERR	OR	?																
			Set	1							Ei	na	able																				
			Disabled	0							R	ea	ad: Dis	abl	ed																		
			Enabled	1							R	ea	ad: Ena	able	ed																		
F	RW	RXTO									W	Vri	ite '1'	to E	nab	le i	nte	rru	pt	or	RXT	0 6	ver	nt									
											Se	ee	EVEN	ITS_	RXT	0																	
			Set	1									able																				
			Disabled	0							R	ea	ad: Dis	abl	ed																		
			Enabled	1							R	ea	ad: Ena	able	ed																		

50.10.3 INTENCLR

Address offset: 0x308 Disable interrupt



Bit	numbe	er		31	30	29	28	27 2	6 2	25 24	4 2	23	22 2	1 2	20	19	1	3 17	1	6	15	14	13	12	11	. 10	9	8	7	6	5	4	3	2	1	0
Id																		F									Ε		D					С	В	Α
Res	et 0x0	0000000		0	0	0	0	0 () (0 0) (0	0 (0	0	0	0	0	()	0	0	0	0	0	0	0	C	0	C	0	0	0	0	0	0
ld	RW	Field	Value Id	Val	ue						D	Des	scrip	tio	n																					
Α	RW	CTS									۷	٧r	ite '1	l' to	о С	Disa	bl	e in	ter	rru	pt 1	for	CT:	S e	ver	nt										
											S	See	e EVE	N	rs_	СТ	S																			
			Clear	1							D	Dis	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
В	RW	NCTS									۷	٧r	ite '1	L' to	о С	Disa	ıbl	e in	ter	rru	pt 1	for	NC	TS	eve	ent										
											S	See	e EVE	N	rs_	NC	TS																			
			Clear	1							D	Dis	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
С	RW	RXDRDY									۷	٧r	ite '1	L' to	о С	Disa	ıbl	e in	ter	rru	pt 1	for	RX	DR	DY	eve	ent									
											S	See	e EVE	N	rs_	RX	DF	DY																		
			Clear	1							D	Dis	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
D	RW	TXDRDY									٧	٧r	ite '1	l' te	о С	Disa	bl	e in	ter	rru	pt i	or	TX	DR	DY	eve	nt									
											S	See	e EVE	N	rs_	ТX	DF	DY																		
			Clear	1							D	Dis	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
Ε	RW	ERROR									۷	٧r	ite '1	l' to	о С	Disa	bl	e in	ter	rru	pt 1	for	ER	RO	R e	ver	it									
											S	See	e EVE	N	rs_	ER	RC)R																		
			Clear	1							D	Dis	able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				
F	RW	RXTO									٧	٧r	ite '1	L' to	о С	Disa	ıbl	e in	ter	rru	pt 1	for	RX	то	ev	ent										
											S	See	e EVE	N	rs_	RX	TC)																		
			Clear	1									able																							
			Disabled	0							R	Rea	ad: D	isa	ble	ed																				
			Enabled	1							R	Rea	ad: E	nal	ble	d																				

50.10.4 ERRORSRC

Address offset: 0x480

Error source

Bit r	numbe	er		31	30	29	28	27	26	25	24	23 22	21	20	19	18	17	16	15	14	13	12 1	1 1	9	8	7	6	5	4	3 2	1	0
Id																														D C	В	Α
Res	et 0x0	0000000		0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	0	0
Id	RW	Field	Value Id	Va	lue							Descr	iptic	on																		
Α	RW	OVERRUN										Overr	un e	erro	r																	
												A staı	t bit	is r	rece	ive	d w	hile	e th	e p	revi	ous	dat	a sti	II lie	es ir	ı RX	D.				
												(Prev	ious	dat	a is	los	t.)			Ċ												
			NotPresent	0								Read	erro	or n	ot p	res	sent	t														
			Present	1								Read:	erro	or p	res	ent																
В	RW	PARITY										Parity	erro	or																		
												A cha	ract	orv	vi+h	ha	d n	rit	, ic	roc	o iv	٠d :	f⊔\	V n-	rity	chi	ock i	ic				
														ei v	VILII	Da	u p	arit	y 15	Tec	eive	eu, i	IПV	v pa	iiity	CIR	CK	15				
												enabl	ed.																			
			NotPresent	0								Read:	erro	or n	ot p	res	sent	t														
			Present	1								Read:	erro	or p	res	ent																
С	RW	FRAMING										Frami	ng e	rro	r oc	cur	red															



Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id		D C B A
Reset 0x00000000		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id RW Field	Value Id	Value Description
		A valid stop bit is not detected on the serial data input after all
		bits in a character have been received.
	NotPresent	0 Read: error not present
	Present	1 Read: error present
D RW BREAK		Break condition
		The serial data input is '0' for longer than the length of a data
		frame. (The data frame length is 10 bits without parity bit, and
		11 bits with parity bit.).
	NotPresent	0 Read: error not present
	Present	1 Read: error present

50.10.5 ENABLE

Address offset: 0x500

Enable UART

Bit numbe	r		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	. 0
Id																															A A	A	A
Reset 0x0	0000000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0
Id RW	Field	Value Id	Va	alue	•						De	scri	ptic	on																			
A RW	ENABLE										Ena	ble	or	disa	able	e U	AR	Γ															
		Disabled	0								Dis	able	e U	ART	•																		
		Enabled	4								Ena	ble	U/	ART																			

50.10.6 PSELRTS

Address offset: 0x508 Pin select for RTS

Bit	numb	er		31	1 30	29	28	27	26	25	24	23	22 2	21 2	20 19	9 18	3 17	16	15	14	13 :	.2 1	1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	A	Α,	А А	. A	Α	Α	Α	Α	Α	Δ ,	4 A	Α	Α	Α	Α	Α	Α	Α ,	۱ ۸	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1 :	1 1	1	1	1	1	1	1	1 :	l 1	1	1	1	1	1	1	1 :	ι :	l 1
Id	RW	Field	Value Id	Va	alue							Des	crip	tio	n																	
Α	RW	PSELRTS		[0	31]						Pin	nun	nbe	r co	nfig	urat	ion	for	UA	RT F	TS:	signa	al								
			Disconnected	0х	FFF	FFF	FF					Dis	conr	nect	t																	

50.10.7 PSELTXD

Address offset: 0x50C

Pin select for TXD

Bitı	numbe	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 1	3 17	7 16	15	14	13 1	2 1	1 10	9	8	7	6	5	4 3	2	1	0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	A A	Δ Δ	A	Α	Α	Α	A	A 4	A	Α	Α	Α	Α	Α.	А А	Α	Α	Α
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	l 1	. 1	1	1	1	1	L 1	. 1	1	1	1	1	1	1 1	1	1	1
Id	RW	Field	Value Id	Va	lue							Des	scrip	otio	n																	
Α	RW	PSELTXD		[0	31]						Pin	nur	nbe	r co	nfig	ura	tior	for	UA	RT T	XD:	signa	ıl								
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t																	

50.10.8 PSELCTS

Address offset: 0x510 Pin select for CTS



Bitı	numb	er		31	. 30	29	28	27	26	25	24	23	22 2	21 2	20 1	9 18	3 17	16	15	14	13	12 1	.1 10	9	8	7	6	5	4	3	2 :	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	ΑА	A	А	Α	Α	Α	Α	A .	4 A	Α	Α	Α	Α	Α	Α	Α ,	Δ ,	A A
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1 1	. 1	. 1	1	1	1	1	1	1 1	1	1	1	1	1	1	1	1 :	1 1
Id	RW	Field	Value Id	Va	lue							Des	crip	otio	n																	
Α	RW	PSELCTS		[0.	31]						Pin	nur	nbe	r co	nfig	urat	tion	for	UA	RT (CTS	sign	al								
			Disconnected	0x	FFF	FFF	FF					Dis	con	nec	t																	

50.10.9 PSELRXD

Address offset: 0x514
Pin select for RXD

Bit	numbe	er		31	1 30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
Id				Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α.	А А
Res	et OxF	FFFFFF		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 1
Id	RW	Field	Value Id	Va	alue							De	scri	ptic	on																			
Α	RW	PSELRXD		[0	31	.]						Pin	nu	mb	er c	onf	igu	rati	on	for	UA	RT	RXI) si	gna	I								
			Disconnected	0>	ĸFFF	FFF	FF					Dis	con	neo	ct																			

50.10.10 RXD

Address offset: 0x518

RXD register

Bit number		31 30 29 28 27 2	6 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ld.			A A A A A A A A
Id			
Reset 0x00000000		0 0 0 0 0 0	
Id RW Field	Value Id	Value	Description
Δ R RXD			RX data received in previous transfers, double huffered

50.10.11 TXD

Address offset: 0x51C

TXD register

Bit n	umbe	er		31	L 30	29	28 2	7 26	25	24	23	22 :	21 2	20 1	19 1	.8 1	.7 1	6 1	5 14	4 13	12	11	10	9	8 7	' 6	5	4	3	2	1 0
Id																									A	Α	A	Α	Α	Α	А А
Rese	t 0x0	0000000		0	0	0	0 0	0	0	0	0	0	0	0	0	0 (0 () (0	0	0	0	0	0	0 (0	0	0	0	0	0 0
Id	RW	Field	Value Id	Va	alue						Des	cri	otio	n																	
Α	W	TXD									TX o	data	a to	be	trar	nsfe	erre	d													

50.10.12 BAUDRATE

Address offset: 0x524

Baud rate

Bit n	umbe	er		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Id				
Rese	t 0x0	400000		0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Id	RW	Field	Value Id	Value Description
Α	RW	BAUDRATE		Baud rate
			Baud1200	0x0004F000 1200 baud (actual rate: 1205)
			Baud2400	0x0009D000 2400 baud (actual rate: 2396)
			Baud4800	0x0013B000 4800 baud (actual rate: 4808)
			Baud9600	0x00275000 9600 baud (actual rate: 9598)
			Baud14400	0x003B0000 14400 baud (actual rate: 14414)
			Baud19200	0x004EA000 19200 baud (actual rate: 19208)
			Baud28800	0x0075F000 28800 baud (actual rate: 28829)
			Baud38400	0x009D5000 38400 baud (actual rate: 38462)
			Baud57600	0x00EBF000 57600 baud (actual rate: 57762)
			544437000	57000 bada (actual rate, 57702)

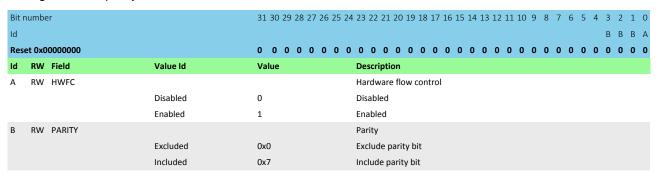


Bit number		31	1 3	0 29	28	3 27	7 26	5 25	24	1 23	3 22	21	20	19	18	17	16	15	14	13	12 1	.1 1	9	8	7	6	5	4	3 2	2 2	1 0
Id		Α	A	A	А	A	Α	Α	Α	A	A	Α	Α	Α	Α	Α	Α	Α	Α	Α	Α .	4 Δ	A	Α	Α	Α	Α	Α	A A	Α Α	А А
Reset 0x04000000		0	(0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0 0) (0 0
Id RW Field	Value Id	Va	alu	e						D	escr	ipti	on																		
	Baud76800	0x	(01	3A9	00	0				76	5800) ba	ud	(act	ual	rat	e: 7	769	23)												
	Baud115200	0x	(01	D7E	00	0				11	1520	00 b	auc	d (ad	ctua	al ra	ite:	11	594	2)											
	Baud230400	0x	(03	AFB	000	0				23	3040	00 b	auc	d (ad	ctua	al ra	ite:	23	188	4)											
	Baud250000	0x	(04	000	000	0				25	5000	00 b	auc	t																	
	Baud460800	0x	(07	5F7	000)				46	5080	00 b	auc	d (ad	ctua	al ra	ite:	47	058	8)											
	Baud921600	0x	(OE	BED	00	0				92	2160	00 b	auc	d (ad	ctua	al ra	ite:	94	117	6)											
	Baud1M	0x	(10	000	000	0				11	Иeg	a ba	aud																		

50.10.13 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control



50.11 Electrical specification

50.11.1 UART electrical specification

Symbol	Description	Min.	Тур.	Max.	Units
f _{UART}	Baud rate for UART ⁴¹ .			1000	kbps
I _{UART1M}	Run current at max baud rate.		55		μΑ
I _{UART115k}	Run current at 115200 bps.		55		μΑ
I _{UART1k2}	Run current at 1200 bps.		55		μΑ
I _{UART,IDLE}	Idle current for UART		1		μΑ
t _{UART,CTSH}	CTS high time	1			μs
t _{UART,START,LP}	Time from STARTRX/STARTTX task to transmission started, low		t _{UART,STAR}	Т	μs
	power mode		+		
			t _{START_HFII}	N	
t _{UART,START,CL}	Time from STARTRX/STARTTX task to transmission started,		1		μs
	constant latency mode				

Higher baud rates may require GPIOs to be set as High Drive, see GPIO chapter for more details.



51 Mechanical specifications

The mechanical specifications for the packages show the dimensions in millimeters.

51.1 QFN48 6 x 6 mm package

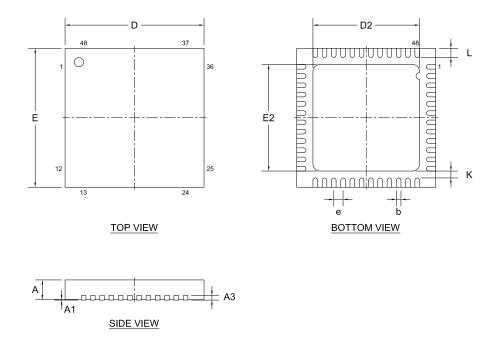


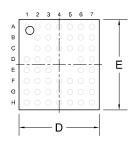
Figure 163: QFN48 6 x 6 mm package

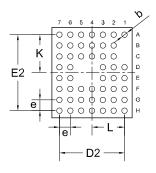
Table 131: QFN48 dimensions in millimeters

Package	Α	A1	А3	b	D, E	D2, E2	е	К	L	
	0.80	0.00		0.15		4.50		0.20	0.35	Min.
QFN48 (6x6)	0.85	0.02	0.2	0.20	6.0	4.60	0.4		0.40	Nom.
	0.90	0.05		0.25		4.70			0.45	Max.



51.2 WLCSP package





TOP VIEW

BOTTOM VIEW



SIDE VIEW

Figure 164: WLCSP package

Table 132: WLCSP packet dimensions in millimeters

Package	Α	A1	А3	b	D	E	D2	E2	е	K	L	
	0.351	0.13		0.19								Min.
WLCSP (3.0×3.2)	0.375	0.15	0.225	0.20	2.956	3.226	2.4	2.8	0.4	1.4	1.2	Nom.
	0.399	0.17		0.25								Max.



52 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

52.1 IC marking

The nRF52832 IC package is marked like described below.

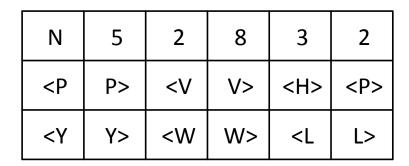


Figure 165: Package marking

52.2 Box labels

Here are the box labels used for the nRF52832.

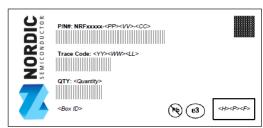


Figure 166: Inner box label



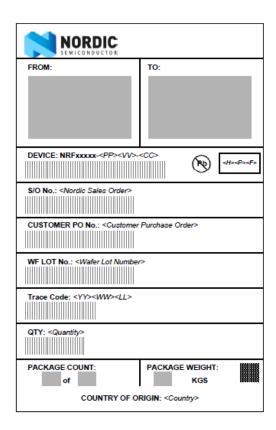


Figure 167: Outer box label

52.3 Order code

Here are the nRF52832 order codes and definitions.

n R F 5 2 8 3 2 - <p p=""> <v v=""> - <c< th=""></c<></v></p>

Figure 168: Order code

Table 133: Abbreviations

Abbreviation	Definition and implemented codes
N52/nRF52	nRF52 Series product
832	Part code
<pp></pp>	Package variant code
<vv></vv>	Function variant code
<h><p><f></f></p></h>	Build code
	H - Hardware version code
	P - Production configuration code (production site, etc.)
<yy><ww><ll></ll></ww></yy>	F - Firmware version code (only visible on shipping container label) Tracking code
	YY - Year code
	WW - Assembly week number
	LL - Wafer lot code
<cc></cc>	Container code

52.4 Code ranges and values

Defined here are the nRF52832 code ranges and values.



Table 134: Package variant codes

<pp></pp>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
QF	QFN	6 x 6	48	0.4
CI	WLCSP	3.0 x 3.2	50	0.4

Table 135: Function variant codes

<vv></vv>	Flash (kB)	RAM (kB)
AA	512	64
AB	256	32

Table 136: Hardware version codes

<h>></h>	Description
[A Z]	Hardware version/revision identifier (incremental)

Table 137: Production configuration codes

<p></p>	Description
[09]	Production device identifier (incremental)
[A Z]	Engineering device identifier (incremental)

Table 138: Production version codes

<f></f>	Description
[A N, P Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 139: Year codes

<yy></yy>	Description
[1599]	Production year: 2015 to 2099

Table 140: Week codes

Table 141: Lot codes

<ll></ll>	Description	
[AA ZZ]	Wafer production lot identifier	

Table 142: Container codes

<cc></cc>	Description
R7	7" Reel
R	13" Reel
T	Tray

52.5 Product options

Defined here are the nRF52832 product options.

Table 143: nRF52832 order codes

Order code	Minimum ordering quantity (MOQ)	Comment
nRF52832-QFAA-R7	1000	Availability to be announced.
nRF52832-QFAA-R	3000	
nRF52832-QFAA-T	490	
nRF52832-CIAA-R7	1500	
nRF52832-CIAA-R	7000	
nRF52832-QFAB-R	3000	
nRF52832-QFAB-R7	1000	
nRF52832-QFAB-T	490	

Table 144: Development tools order code

Order code	Description
nRF52-DK	nRF52 Development Kit



53 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from *Reference layout nRF52 Series*.

53.1 Schematic QFAA and QFAB QFN48 with internal LDO setup

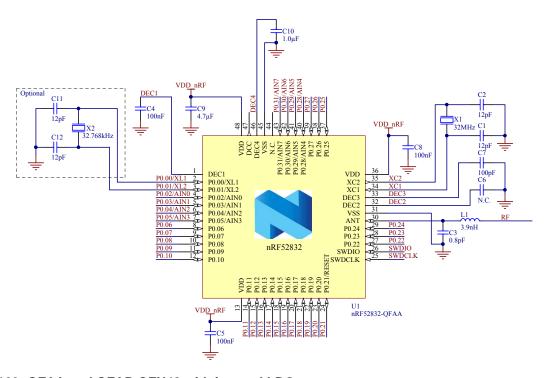


Figure 169: QFAA and QFAB QFN48 with internal LDO setup

Table 145: Bill of material for QFAA and QFAB QFN48 with internal LDO setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
U1	nRF52832-QFAA and nRF52832-QFAB	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, total tol. ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, CI=9 pF, total tol. ±50 ppm	XTAL 3215



53.2 Schematic QFAA and QFAB QFN48 with DC/DC regulator setup

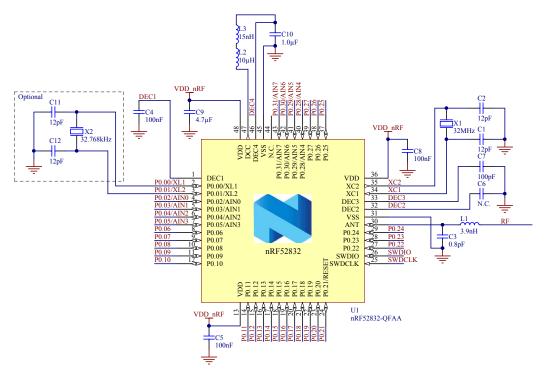


Figure 170: QFAA and QFAB QFN48 with DC/DC regulator setup

Table 146: Bill of material for QFAA and QFAB QFN48 with DC/DC regulator setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
L1	3.9 nH	High frequency chip inductor ±5%	0402
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-QFAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	QFN-48
	and nRF52832-QFAB		
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, total tol. ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, CI=9 pF, total tol. ±50 ppm	XTAL_3215



53.3 Schematic QFAA and QFAB QFN48 with DC/DC regulator and NFC setup

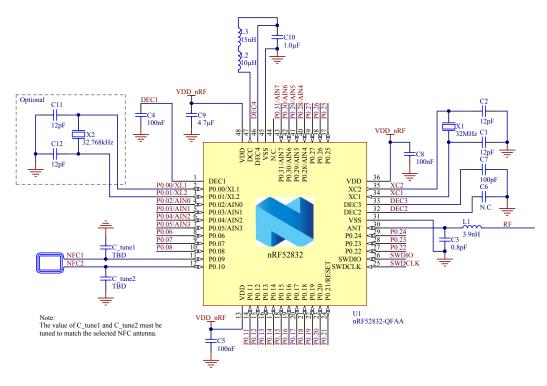


Figure 171: QFAA and QFAB QFN48 with DC/DC regulator and NFC setup

Table 147: Bill of material for QFAA and QFAB QFN48 with DC/DC converter and NFC setup

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, ±2%	0402
C3	0.8 pF	Capacitor, NPO, ±5%	0402
C4, C5, C8	100 nF	Capacitor, X7R, ±10%	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, ±5%	0402
C9	4.7 μF	Capacitor, X5R, ±10%	0603
C10	1.0 μF	Capacitor, X7R, ±10%	0603
C _{tune1} , Ctune2	TBD pF	Capacitor, NPO, ±5%	0402
L1	3.9 nH	High frequency chip inductor ±5%	0402
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-QFAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	QFN-48
	and nRF52832-QFAB		
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, CI=9 pF, ±50 ppm	XTAL_3215



53.4 Schematic CIAA WLCSP with internal LDO setup

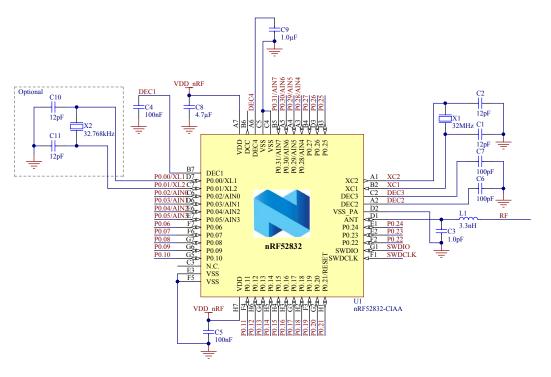


Figure 172: CIAA WLCSP with internal LDO setup

Table 148: Bill of material for CIAA WLCSP with internal LDO setup

Designator	Value	Description	Footprint
C1, C2, C10, C11	12 pF	Capacitor, NPO, ±2%	0201
C3	1.0 pF	Capacitor, NPO, ±5%	0201
C4, C5	100 nF	Capacitor, X7R, ±10%	0201
C6, C7	100 pF	Capacitor, NPO, ±5%	0201
C8	4.7 μF	Capacitor, X5R, ±10%	0603
C9	1.0 μF	Capacitor, X5R, ±5%	0402
L1	3.3 nH	High frequency chip inductor ±5%	0201
U1	nRF52832-CIAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	WLCSP_C50
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, total tol. ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 2012, 32.768 kHz, CI=9 pF, ±50 ppm	XTAL_2012



53.5 Schematic CIAA WLCSP with DC/DC regulator setup

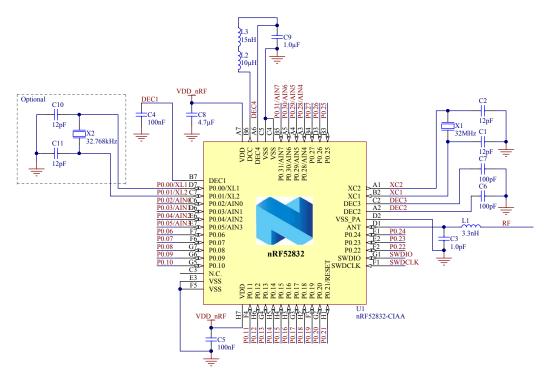


Figure 173: CIAA WLCSP with DC/DC regulator setup

Table 149: Bill of material for CIAA WLCSP with DC/DC regulator setup

Designator	Value	Description	Footprint
C1, C2, C10, C11	12 pF	Capacitor, NPO, ±2%	0201
C3	1.0 pF	Capacitor, NPO, ±5%	0201
C4, C5	100 nF	Capacitor, X7R, ±10%	0201
C6, C7	100 pF	Capacitor, NPO, ±5%	0201
C8	4.7 μF	Capacitor, X5R, ±10%	0603
C9	1.0 μF	Capacitor, X5R, ±5%	0402
L1	3.3 nH	High frequency chip inductor ±5%	0201
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-CIAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	WLCSP_C50
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 2012, 32.768 kHz, CI=9 pF, ±50 ppm	XTAL 2012



53.6 Schematic CIAA WLCSP with DC/DC regulator and NFC setup

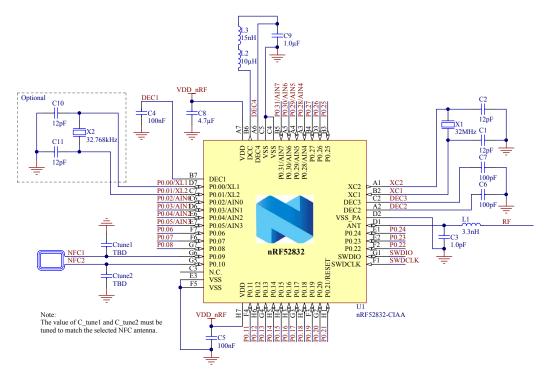


Figure 174: CIAA WLCSP with DC/DC regulator and NFC setup

For PCB reference layouts, see Reference layout nRF52 Series.

Table 150: Bill of material for CIAA WLCSP with DC/DC converter and NFC setup

Designator	Value	Description	Footprint
C1, C2, C10, C11	12 pF	Capacitor, NPO, ±2%	0201
C3	1.0 pF	Capacitor, NPO, ±5%	0201
C4, C5	100 nF	Capacitor, X7R, ±10%	0201
C6, C7	100 pF	Capacitor, NPO, ±5%	0201
C8	4.7 μF	Capacitor, X5R, ±10%	0603
C9	1.0 μF	Capacitor, X5R, ±5%	0402
C _{tune1} , C _{tune2}	TBD pF	Capacitor, NPO, ±5%	0201
L1	3.3 nH	High frequency chip inductor ±5%	0201
L2	10 μΗ	Chip inductor, IDC,min = 50 mA, ±20%	0603
L3	15 nH	High frequency chip inductor ±10%	0402
U1	nRF52832-CIAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	WLCSP_C50
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ±40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 2012, 32.768 kHz, CI=9 pF, ±50 ppm	XTAL_2012

53.7 PCB guidelines

A well-designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality.

A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from *Reference layout nRF52 Series*.

To ensure optimal performance, it is essential that you follow the schematics and layout references closely. Especially in the case of the antenna matching circuitry (components between device pin ANT and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 ohm single end antenna.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna



matching circuitry (components between device pin ANT and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the RF pin ANT and the antenna, to match the antenna impedance (normally 50 ohm) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in the recommended package reference circuitry in *Reference circuitry* on page 545 above.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Fast switching digital signals should not be routed close to the crystal or the power supply lines. Capacitive loading of fast switching digital output lines should be minimized in order to avoid radio interference.

53.8 PCB layout example

The PCB layout shown below is a reference layout for the QFN package with internal LDO setup.

Important: Pay attention to how the capacitor C3 is grounded. It is not directly connected to the ground plane, but grounded via VSS pin 31. This is done to create additional filtering of harmonic components.

For all available reference layouts, see Reference layout nRF52 Series.

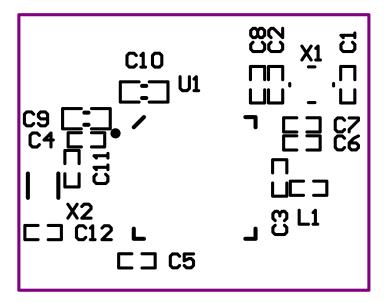


Figure 175: Top silk layer



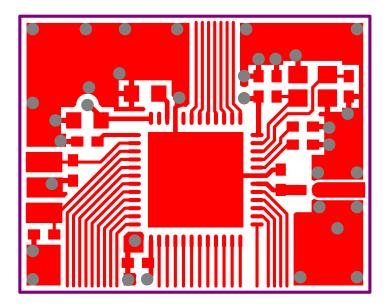


Figure 176: Top layer

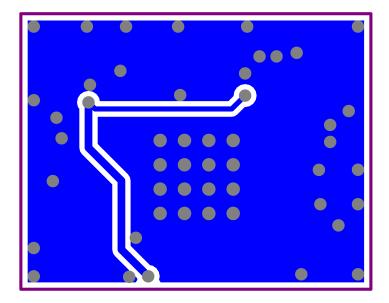


Figure 177: Bottom layer

Important: No components in bottom layer.



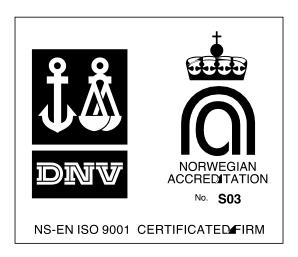
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BCM20737A1KML2G BCM43236BKMLG EM06ELA-512-SGAS CYBL10463-56LQXI CYBL10562-56LQXI CYBL10563-68FLXIT

ATBTLC1000A-UU-T EC25AUFA-MINIPCIE BCM43242KFFBG BCM20707UA1KFFB1G ATWILC1000B-UU-T BCM4322KFBGH

ETRX3DVK357 EC25VFA-MINIPCIE EC25JFA-MINIPCIE EC25MXGA-MINIPCIE EC25AFXGA-MINIPCIE EC25AUXGA-MINIPCIE

EC25AUTFA-MINIPCIE EC25AFFA-MINIPCIE EP06ALA-512-SGAD EM06ALA-512-SGAD EM12GPA-512-SGAD EC25EUGA
MINIPCIE TLSR8367EP16 EC25AFA-MINIPCIE CYBL10463-56LQXIT CC2511F32RSPR AX-SFEU-API-1-01-TB05 NRF51422-CFAC
R NRF51822-CDAB-R XR1015-QH-0G00 NCH-RSL10-101Q48-ABG AX8052F143-3-TX30 BLUENRG-232 ESP32-D2WD

AWR1642ABIGABLQ1 ESP32-D0WD ESP8266EX CYBL10561-56LQXI ATWINC1500B-MU-Y DA14531-00000FX2 ESP32-C3FH4

ESP32-C3 ESP32-D0WDQ6 ESP32-D0WDQ6-V3 ESP32-D0WD-V3 ESP32-PICO-V3 ESP32-PICO-V3-02 ESP32-S2