

### Product Overview

The NCA9511 is a hot-swappable I<sup>2</sup>C bus buffer that supports I/O card insertion into a live backplane without corruption of the data and clock buses. Control circuitry prevents the backplane-side I<sup>2</sup>C lines (in) from being connected to the card-side I<sup>2</sup>C lines (out) until a stop command or bus idle condition occurs on the backplane without bus contention on the card. When the connection is made, this device provides bidirectional buffering, keeping the backplane and card capacitances separated. During insertion, the SDA and SCL lines are pre-charged to 1 V to minimize the current required to charge the parasitic capacitance of the device.

When the I<sup>2</sup>C bus is idle, the NCA9511 can be put into shutdown mode by setting the EN pin low, reducing power consumption. When EN is pulled high, the NCA9511 resumes normal operation. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together. When READY is high, the SDAIN and SCLIN are connected to SDAOUT and SCLOUT. When the two sides are disconnected, READY is low.

### Key Features

- Supports bidirectional data transfer of I2C bus signals
- Operating power-supply voltage range of 2.7 V to 5.5 V
- TA ambient air temperature range of -40 °C to 105 °C
- 1-V pre-charge on all SDA and SCL lines prevents corruption during live insertion
- Accommodates standard mode and fast mode I<sup>2</sup>C devices
- Supports clock stretching, arbitration and synchronization
- Powered-off high-impedance I<sup>2</sup>C pins

### Applications

- Servers
- Enterprise Switching
- Telecom switching equipment
- Base stations
- Industrial automation equipment

### Device Information

| Part Number  | Package | Body Size     |
|--------------|---------|---------------|
| NCA9511-DMSR | MSOP8   | 3.00mm*3.00mm |
| NCA9511-DSPR | SOP8    | 4.90mm*3.90mm |

### Functional Block Diagrams

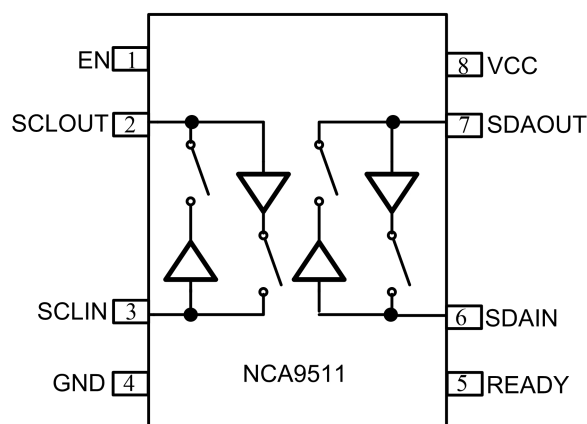


Figure 1. NCA9511 Block Diagram

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### 1. Pin Configuration and Functions

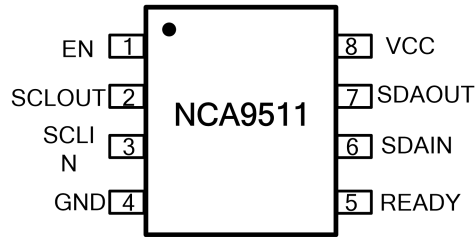


Figure 1.1 NCA9511 Package

**Table 1 Pin Configuration and Description**

| Symbol | Pin | Description   |
|--------|-----|---|
| EN     | 1   | Active-high chip enable pin. If EN is low, the NCA9511 is in a low current mode. It also disables the rise-time accelerators, disables the bus pre-charge circuitry, drives READY low, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT. EN should be high (at VCC) for normal operation. Connect EN to VCC if this feature is not being used. |
| SCLOUT | 2   | Serial clock output. Connect this pin to the SCL bus on the card.   |
| SCLIN  | 3   | Serial clock input. Connect this pin to the SCL bus on the backplane.   |
| GND    | 4   | Supply ground   |
| READY  | 5   | Connection flag. Ready is low when either EN is low or the startup sequence has not been completed. READY goes high when EN is high and start-up is complete. Connect a 10-kΩ resistor from this pin to VCC to provide the pull-up current.   |
| SDAIN  | 6   | Serial data input. Connect this pin to the SDA bus on the backplane.  |
| SDAOUT | 7   | Serial data output. Connect this pin to the SDA bus on the card.  |
| VCC    | 8   | Supply Power. Main input power supply from backplane. This is the supply voltage for the devices on the backplane I <sup>2</sup> C buses. Connect pull-up resistors from SDAIN and SCLIN (and also from SDAOUT and SCLOUT) to this supply. Place a bypass capacitor of at least 0.01 μF close to this pin for best results.                             |

### 2. Absolute Maximum Ratings

| Parameters                            | Symbol                         | Min  | Max   | Unit | Conditions                            |
|---------------------------------------|--------------------------------|------|-------|------|---------------------------------------|
| Supply Voltage                        | VCC                            | -0.5 | 7     | V    |                                       |
| Maximum Input/output Voltage          | V <sub>I</sub> /V <sub>O</sub> | -0.5 | 7     | V    | SDAIN,SCLIN,SDAIN,SDAOUT,READY,ENABLE |
| Input clamp current                   | I <sub>IK</sub>                |      | -50   | mA   | V <sub>I</sub> <0V                    |
| Output clamp current                  | I <sub>OK</sub>                |      | -50   | mA   | V <sub>O</sub> <0V                    |
| Continuous output current             | I <sub>O</sub>                 |      | ± 50  | mA   | SDAIN,SCLIN,SDAIN,SDAOUT,READY,       |
| Continuous current through VCC or GND | I <sub>CC</sub>                |      | 100   | mA   |                                       |
| Operating Temperature                 | T <sub>opr</sub>               | -40  | 105   | °C   |                                       |
| Storage Temperature                   | T <sub>stg</sub>               | -65  | 150   | °C   |                                       |
| Electrostatic discharge               | HBM                            |      | ±2000 | V    |                                       |
|                                       | CDM                            |      | ±1000 | V    |                                       |

### 3. Recommended Operating Conditions

| Parameters                 | Symbol   | Min | Max | Unit | Conditions                   |
|----------------------------|----------|-----|-----|------|------------------------------|
| Supply voltage             | $V_{CC}$ | 2.7 | 5.5 | V    |                              |
| Input voltage range        | $V_i$    | 0   | 5.5 | V    | EN input                     |
| Input/output voltage range | $V_{IO}$ | 0   | 5.5 | V    | SDAIN, SCLIN, SDAOUT, SCLOUT |
| Output voltage range       | $V_o$    | 0   | 5.5 | V    | READY                        |
| Ambient temperature        | $T_A$    | -40 | 105 | °C   |                              |

### 4. Thermal Information

| Parameters                               | Symbol              | MSOP8 | SOP8 | Unit |
|--|---------------------|-------|------|------|
| Junction-to-ambient thermal resistance   | $\theta_{JA}$       | 177.1 | 114  | °C/W |
| Junction-to-case(top) thermal resistance | $\theta_{JC (top)}$ | 64.5  | 63   | °C/W |
| Junction-to-board thermal resistance     | $\theta_{JB}$       | 99.6  | 54.8 | °C/W |

## 5. Specifications

### 5.1. Electrical Characteristics

VCC = 2.7V to 5.5V; Tamb = -40°C to +105°C; unless otherwise noted. Typical specification are at TA=25°C, VCC=3.3V

| Parameters   | Symbol               | Min    | Typ | Max    | Unit | Conditions   |
|--|----------------------|--------|-----|--------|------|--|
| <b>Supply</b>  |                      |        |     |        |      |  |
| Supply voltage Range                                   | V <sub>CC</sub>      | 2.7    | -   | 5.5    | V    |  |
| Under voltage lockout (rising)                         | UVLO+                |        | 2.4 |        | V    |  |
| Under voltage lockout (falling)                        | UVLO-                |        | 2.3 |        | V    |  |
| Supply current   | I <sub>CC</sub>      | -      | 4.5 | 10     | mA   | Operating mode; VCC=EN = 5.5 V; all other pins at GND,BUS disconnected         |
| Shut down mode supply current                          | I <sub>CC(sd)</sub>  | -      | 0.1 | 5      | uA   | Shut down mode; VCC = 5.5 V;EN=0V;;all other pins at VCC or GND                |
| <b>START-UP CIRCUITRY</b>                              |                      |        |     |        |      |  |
| Pre-charge voltage                                     | V <sub>pch</sub>     | 0.8    | 1.1 | 1.35   | V    | SDA,SCL floating   |
| LOW-level input voltage(EN)                            | V <sub>IL</sub>      | -      | -   | 0.3VCC | V    |  |
| HIGH-level input voltage(EN)                           | V <sub>IH</sub>      | 0.7VCC | -   | -      | V    |  |
| Input leakage current(EN)                              | I <sub>LI</sub>      | -1     | -   | +1     | μA   | VCC = 2.7 V to 5.5 V; VI = VCC or GND  |
| Time from VPOR to digital being ready                  | t <sub>EN</sub>      |        | 110 | 175    | us   | VCC transition from 0V to VCC Time from V PORR to earliest stop bit Recognized |
| Bus idle time to READY active                          | t <sub>IDLE</sub>    |        | 105 | 175    | us   | SDA,SCL = 10 kΩ to VCC<br>EN = VCC<br>Measured at 0.5 × V CC                   |
| Time from EN high to low to READY low <sup>1</sup>     | t <sub>DISABLE</sub> | -      | 30  | -      | ns   | SDA,SCL,READY = 10 kΩ to VCC<br>Measured at 0.5 × VCC                          |
| SDAIN to READY delay after stop condition <sup>1</sup> | t <sub>STOP</sub>    |        | 1.2 |        | us   | SDA,SCL,READY = 10 kΩ to VCC<br>Measured at 0.5 × VCC                          |
| SCLOUT/SDAOUT to READY <sup>1</sup>                    | t <sub>READY</sub>   |        | 0.8 |        | us   | SDA,SCL,READY = 10 kΩ to VCC<br>Measured at 0.5 × VCC                          |
| <b>RISE TIME ACCELERATORS</b>                          |                      |        |     |        |      |  |
| RTA pull up current                                    | I <sub>PU</sub>      |        | 5   |        | mA   | VCC=2.7V; slew rate=1.25V/us   |

| Input-Output Connection       |                         |    |      |     |               |   |
|-------------------------------|-------------------------|----|------|-----|---------------|---|
| Offset voltage                | $V_{\text{OFFSET}}$     | 0  | 130  | 300 | mV            | VCC=3.3V,SDA,SCL pull up to VCC with 10k $\Omega$                             |
| Low level output voltage      | $V_{\text{OL}}$         | 0  | 0.3  | 0.5 | V             | VCC=2.7V,VIN=0V;I <sub>OL</sub> =3mA,SDAn, SCLn                               |
|                               |                         | 0  | 0.03 | 0.4 | V             | VCC=2.7V,READY, I <sub>OL</sub> =3mA  |
| Input leakage current         | $I_{\text{LI}}$         | -1 | -    | +1  | $\mu\text{A}$ | VCC=5.5V, SDAn, SCLn pins   |
| Ready pin leakage             | $I_{\text{L,RDY}}$      | -1 | -    | +1  | $\mu\text{A}$ | EN=VCC,BUS connected, READY=VCC   |
| LOW to HIGH propagation delay | $t_{\text{PLH}}$        | -  | 0    | -   | ns            | SCL to SCL and SDA to SDA;10k $\Omega$ to VCC,C <sub>L</sub> =100pF each side |
| HIGH to LOW propagation delay | $t_{\text{PHL}}$        | -  | 70   | -   | ns            | SCL to SCL and SDA to SDA;10k $\Omega$ to VCC,C <sub>L</sub> =100pF each side |
| SCL and SDA input capacitance | $C_{\text{i(SCL/SDA)}}$ | -  | 5    | 7   | pF            |   |

1.Guaranteed by design

## 5.2. Timing Requirements

| Parameters                                       | Symbol              | Standard-mode I <sup>2</sup> C-bus |      | Fast-mode I <sup>2</sup> C-bus |     | Unit          |
|--|---------------------|------------------------------------|------|--------------------------------|-----|---------------|
|  |                     | Min                                | Max  | Min                            | Max |               |
| SCL clock frequency                              | $f_{\text{SCL}}$    | 0                                  | 100  | 0                              | 400 | kHz           |
| bus free time between a STOP and START condition | $t_{\text{BUF}}$    | 4.7                                | -    | 1.3                            | -   | $\mu\text{s}$ |
| hold time (repeated) START condition             | $t_{\text{HD,STA}}$ | 4.0                                | -    | 0.6                            | -   | $\mu\text{s}$ |
| set-up time for a repeated START condition       | $t_{\text{SU,STA}}$ | 4.7                                | -    | 0.6                            | -   | $\mu\text{s}$ |
| set-up time for STOP condition                   | $t_{\text{SU,STO}}$ | 4.0                                | -    | 0.6                            | -   | $\mu\text{s}$ |
| data hold time                                   | $t_{\text{HD,DAT}}$ | 0                                  | -    | 0                              | -   | ns            |
| data set-up time                                 | $t_{\text{SU,DAT}}$ | 250                                | -    | 100                            | -   | ns            |
| LOW period of the SCL clock                      | $t_{\text{LOW}}$    | 4.7                                | -    | 1.3                            | -   | $\mu\text{s}$ |
| HIGH period of the SCL clock                     | $t_{\text{HIGH}}$   | 4.0                                | -    | 0.6                            | -   | $\mu\text{s}$ |
| fall time of both SDA and SCL signals            | $t_{\text{f}}$      | -                                  | 300  |                                | 300 | ns            |
| rise time of both SDA and SCL signals            | $t_{\text{r}}$      | -                                  | 1000 |                                | 300 | ns            |

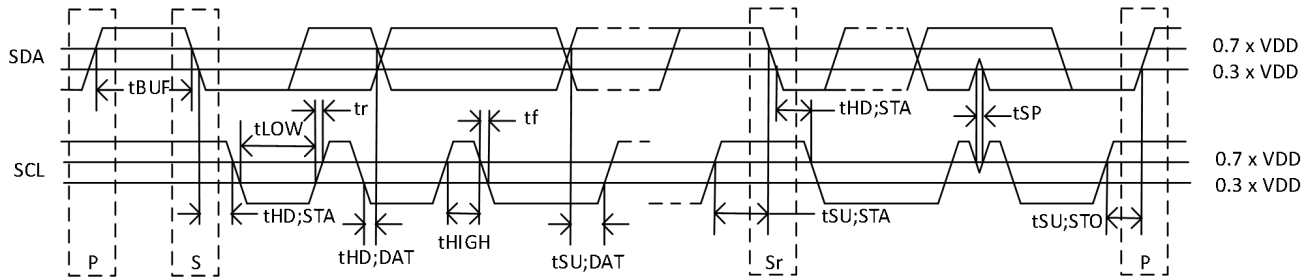


Figure 5. 1 Definition of timing on I<sup>2</sup>C-bus

## 6. Detailed Description

### 6.1. Overview

The NCA9511 is a hot-swappable I<sup>2</sup>C bus buffer that supports I/O card insertion into a live backplane without corruption of the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle condition occurs on the backplane without bus contention on the card. When the connection is made, this device provides bidirectional buffering, keeping the backplane and card capacitances isolated. During insertion, the SDA and SCL lines are pre-charged to 1 V to minimize the current required to charge the parasitic capacitance of the device.

When the I<sup>2</sup>C bus is idle, the NCA9511 is put into shutdown mode by setting the EN pin low. When EN is high, the NCA9511 resumes normal operation. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together. When READY is high, the SDAIN and SCLIN are connected to SDAOUT and SCLOUT. When the two sides are disconnected, READY is low.

### 6.2. Functional block diagram

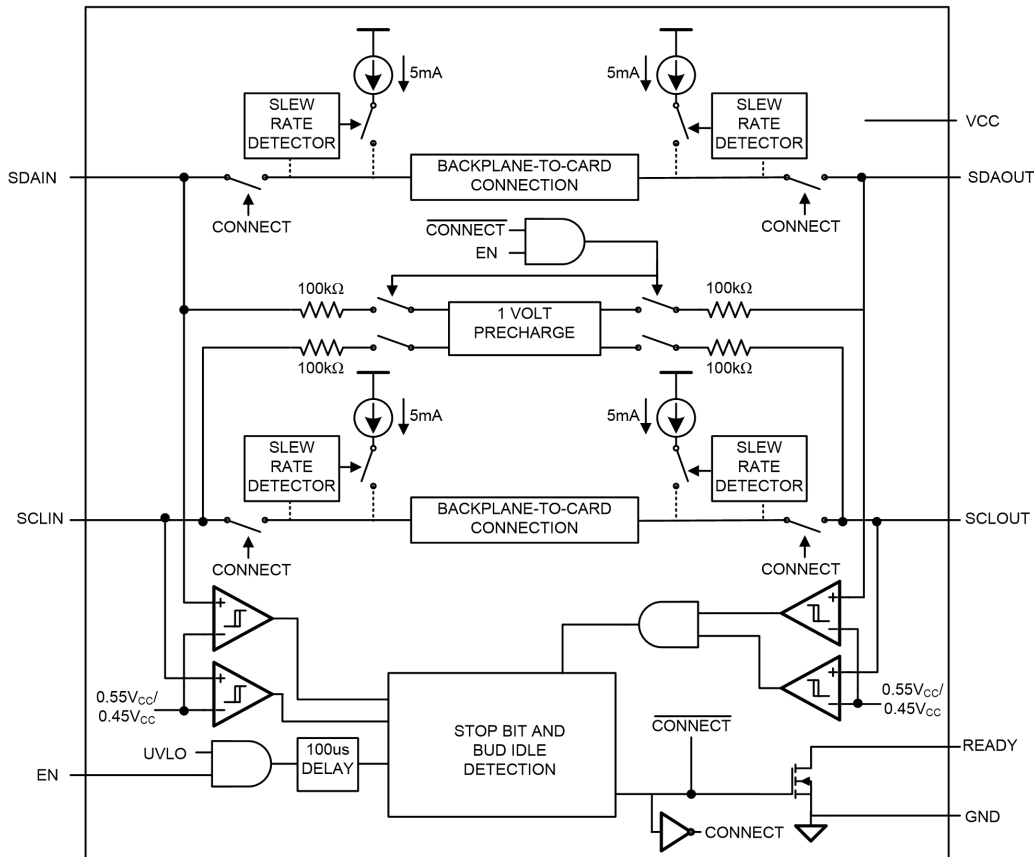


Figure 6. 1 Functional block diagram

### 6.3. Connect circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical with each acting as a bidirectional buffer that isolates the input capacitance from the output bus capacitance while communicating the logic levels. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the part. The same is also true for the SCL pins. Noise between 0.7VCC and VCC is generally ignored because a falling edge is only recognized when it falls below 0.7VCC with a slew rate of at least 1.25 V/us. When a falling edge is seen on one pin, the other pin in the pair turns on a pull-down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load initially, because it does not start until the first falling pin is below 0.7VCC. The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate then the initial pull-down rate will continue. If the first falling pin has a slow slew rate then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage then they will both continue down at the slew rate of the first.

Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same value for instance, 10 mV by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving that pin will rise until the internal driver pulls it down to the offset voltage. When the last external driver stops driving a LOW, that pin will rise up and settle out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least 1.25 V/us, when the pin voltage exceeds 0.6 V for the NCA9511, the rise time accelerator's circuits are turned on and the pull-down driver is turned off.

### 6.4. Feature Description

#### Hot bus insertion

During a hot bus insertion event, the NCA9511 keeps the buses disconnected to ensure that no data corruption occurs on either bus. Once the buses are idle, the NCA9511 connects the buses and READY goes high.

#### Pre-charge voltage

Both the SDA and SCL pins feature a 1-V pre-charge circuit through an internal 100 kΩ resistor prior to the pins being connected to an I2C bus. This feature helps minimize disruptions as a result of a hot bus insertion event.

#### Rise time accelerators

The NCA9511 features a rise time accelerator (RTA) on all I2C pins that during a positive bus transition, switches on a current source to quickly slew the bus pins high. This allows the use of weaker pull-up resistors.

#### Bus ready output indicator

The READY pin is an open drain output that provides an indicator to whether the buses are connected and ready for traffic. This pin is pulled low when the connection between IN/OUT is high impedance. Once the bus is idle and the connection between IN/OUT is made, the READY pin is released and pulled high by an external pull-up resistor, signaling that it is ready for traffic.

#### Powered-off high impedance for I2C and I/O pins

When the supply voltage is below the UVLO threshold, the I2C and digital I/O pins are a high impedance state to prevent leakage currents from flowing through the device. When the EN pin is taken low, the device enters an isolation state and present a high impedance on all bus pins, and pull READY pin low.

#### Supports clock stretching and arbitration

The NCA9511 supports full clock stretching, and arbitration without lock up.

### 6.5. Device Functional Modes

#### Start-up and pre-charge

When the NCA9511 first receives power on the VCC pin, either during power-up or during live insertion, it starts in an under voltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until VCC rises above UVLO. Once the ENABLE pin has been high long enough to complete the initialization state, the 'Stop Bit and Bus Idle detect circuit is enabled and the device enters the bus idle state.

When VCC rises above UVLO, the pre-charge circuitry will activate, which biases the bus pins on both sides to about 1 V through an internal 100 kΩ resistor.



**Bus idle**

After the Stop Bit and Bus Idle detect circuits are enabled the device enters the bus idle state. The pre-charge circuitry becomes active and forces 1 V through 100 kΩ nominal resistors to the SCL and SDA pins. The precharge circuitry minimizes the voltage differential seen by the SCL/SDA pins during a hot insertion event. This minimizes the amount of disturbance seen by the I/O card.

The device waits for the SDAIN and SCLIN pins to be high for the bus idle time or a STOP condition is observed on the SDAIN and SCLIN pins. The SDAOUT and SCLOUT pins must be high and the SDAIN and SCLIN pins must meet 1 of the 2 qualifiers (idle timer or a STOP condition) before connecting SDAIN to SDAOUT and SCLIN to SCLOUT. Once the bus connections have been made, the pre-charge circuitry is disabled and the device enters the bus active state.

**6.6. Bus active**

In the bus active mode, the I2C IN and OUT pins are connected, and the input is passed bi-directionally from IN/OUT side of the bus to the OUT/IN side respectively. The buses remain connected until the EN pin is taken low.

When the bus is connected, the driven-low side of the device is reflected on the opposite side, but with a small offset voltage. For example, if the input is pulled low to 100 mV, the output side will be pulled to roughly 160 mV.

This offset allows the device to determine which side is currently being driven and avoid getting stuck low.

**7. Application and Implementation**

**7.1. Typical Application**

The typical application is to place the NCA9511 on the card that is being inserted or connected to a live bus, rather than being placed on the live bus. The reason for this is to provide maximum benefit by ensuring that the bus stays disconnected until an idle condition or stop condition is seen.

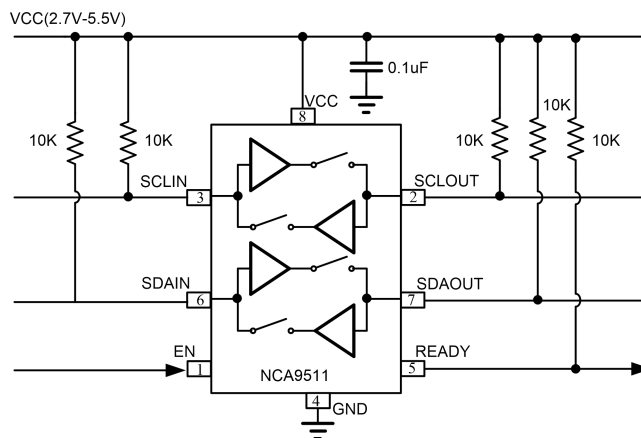


Figure 7.1 Typical application

**7.2. Design Requirements**

**Series connections**

It is possible to have multiple buffers in series, but care must be taken when designing a system.

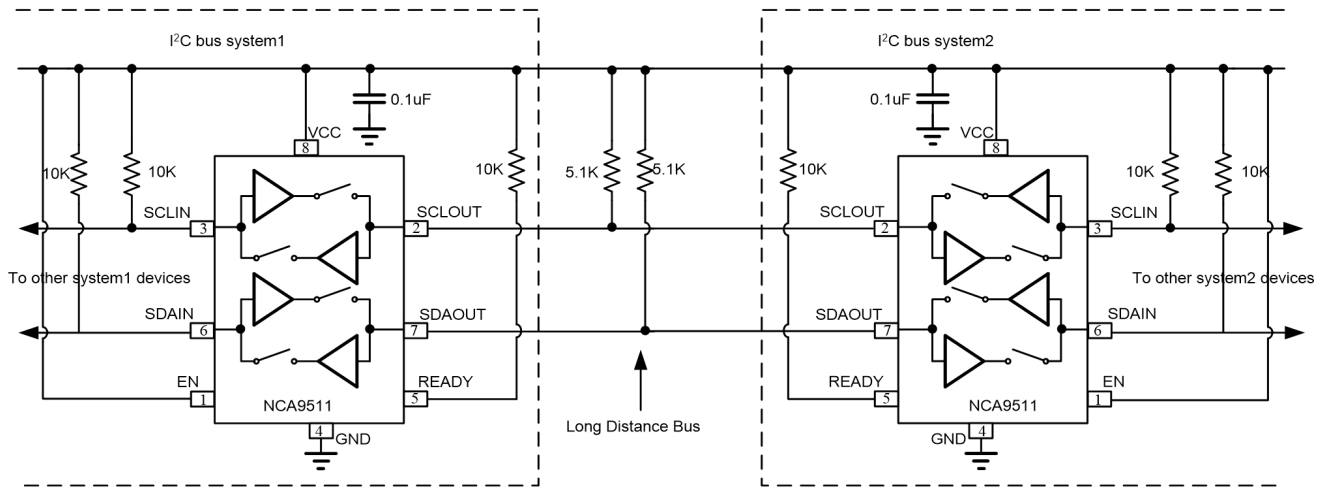


Figure 7.2 Bus extender application using NCA9511

Each buffer adds approximately 50 mV of offset. Maximum offset (VOFFSET) should be considered. The low level at the signal origination end is dependent upon bus load. The I2C-bus specification requires that a 3 mA current produces no larger than a 0.4 V VOL. As an example, if the VOL at the master is 0.1 V, and there are 4 buffers in series (each adding about 50 mV), then the VOL at the farthest buffer is approximately 0.3 V. This device has a rise time accelerator (RTA) that activates at 0.6 V. With great care, a system with 4 buffers may work, but as the VOL moves up, it may be possible to trigger the RTA, creating a false edge on the clock.

It is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset. Another special consideration of series connections is the effect on round-trip-delay. This is the sum of propagation delays through the buffers and any effects on rise time. It is possible that fast mode speeds (400kHz) are not possible due to delays and bus loading.

**Multiple connections to a common node**

It is possible to have multiple buffers in connect to a common node, but care must be taken when designing a system.

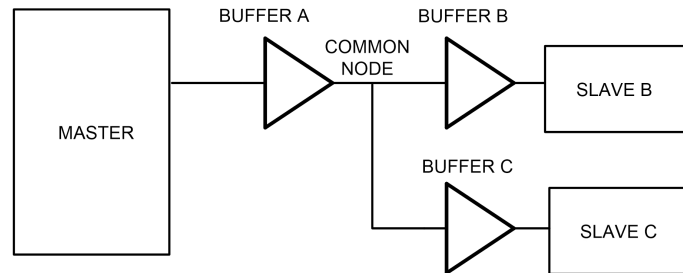


Figure 7.3 Connections to Common Node

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B in series as shown in Figure 7.3. Consider if the VOL at the input of buffer A is 0.3 V and the VOL of Slave B (when acknowledging) is 0.36 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change the user should observe VIL at the input of buffer A of 0.3 V and its output, the common node, is ~0.36 V. The output of buffer B and buffer C would be ~0.5 V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of buffer C is ~0.5 V. When the Master pull-down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node rises to 0.5 V before the buffer B output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V, the accelerators on both buffer A and buffer C will fire, contending with the output of buffer B. The node on the input of buffer A goes high as will the input node of buffer C. After the common node voltage is stable for a while, the rising edge accelerators turn off, and the common node returns to ~0.5 V because the buffer B is still on. The voltage at both the Master and Slave C nodes then fall to ~0.6 V until Slave B turned off. This does not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.56 V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which causes a system error.

**Propagation delays**

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The tPLH may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The tPHL can never be negative because the output does not start to fall until the input is below 0.7 × VCC, the output turn on has a non-zero delay, and the output has a limited maximum slew rate. Even if the input slew rate is slow enough that the output catches up, it would still lag the falling voltage of the input by the offset voltage. The maximum tPHL occurs when the input is driven low with zero delay and the output is still limited by its turn-on delay and the falling edge slew rate.

**Detailed Design Procedure**

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/μs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula given in Equation 1.

$$R \leq 800 \times 10^3 \left( \frac{V_{CC(MIN)} - 0.6}{C} \right) \tag{1}$$

where R is the pull-up resistor value in Ω, V<sub>CC(MIN)</sub> is the minimum VCC voltage in volts, and C is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose R<sub>PU</sub> ≤ 65.7 kΩ for VCC = 5.5 V, R<sub>PU</sub> ≤ 45 kΩ for VCC = 3.3 V, and R<sub>PU</sub> ≤ 33 kΩ for VCC = 2.5 V. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the pre-charge voltage.

**Application Curves**

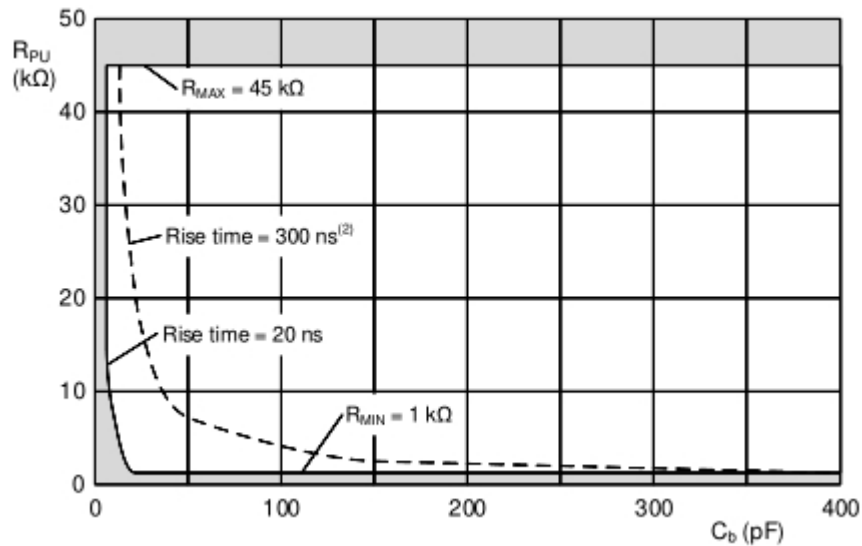


Figure 7.4 Bus requirements for 3.3V systems

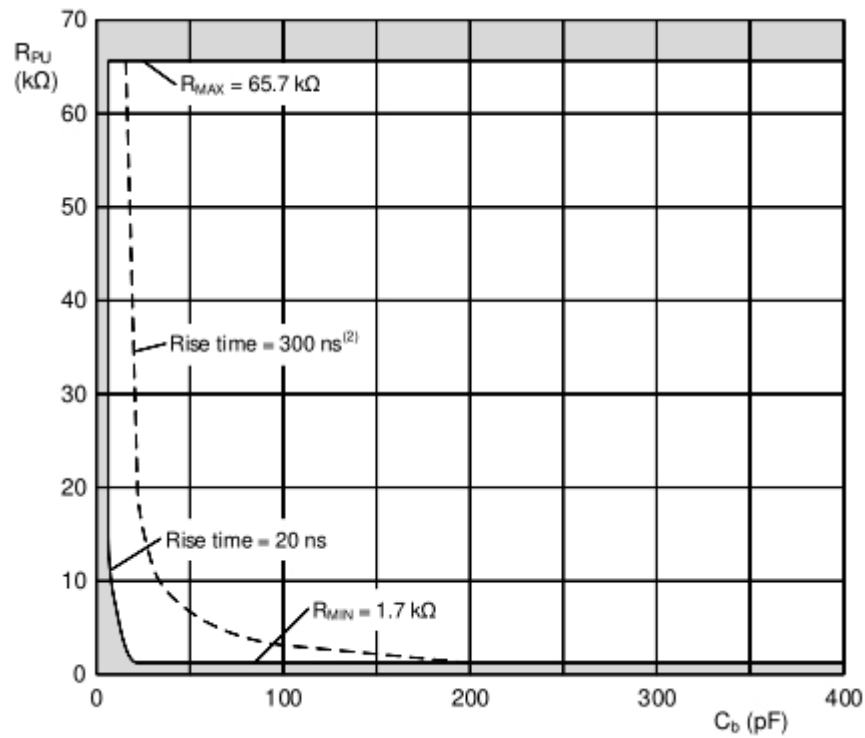


Figure 7.5 Bus requirements for 5V systems

### 7.3. Typical Application on a Backplane

As shown in Figure 7.6, the NCA9511 is used in a backplane connection. The NCA9511 is placed on the I/O peripheral card and connects the I2C devices on the card to the backplane safely upon a hot insertion event. Note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card; however, isolates the card capacitance from the backplane. For a given I/O card, the NCA9511 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

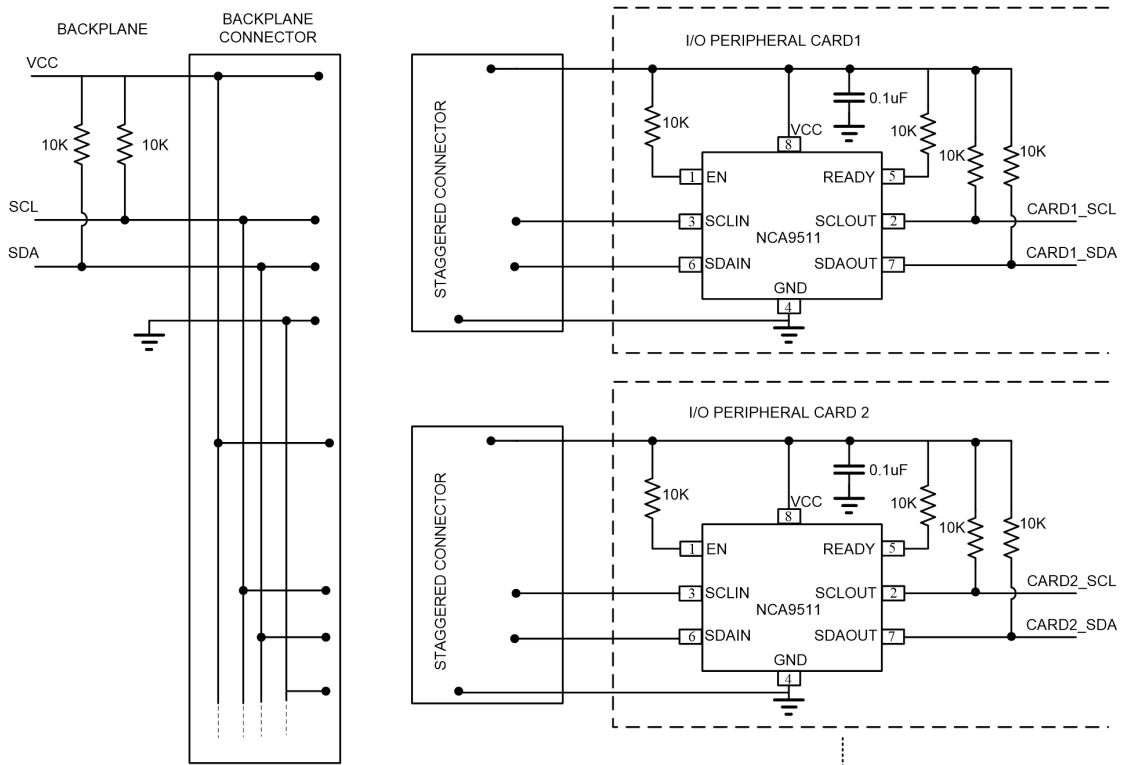


Figure 7.6 Backplane application schematic

**Design Requirements**

There are a few considerations when using these hot swap buffers. It is NOT recommended to place the NCA9511 on the backplane connector as it cannot isolate the cards from one another which will possibly result in disturbing on-going I2C transactions. Instead, place the NCA9511 on the I/O peripheral card to maximize benefit.

**Detailed Design Procedure**

The design procedure is the same as outlined in Detailed Design Procedure.

**8. Power Supply Recommendations**

**8.1. Power supply best practices**

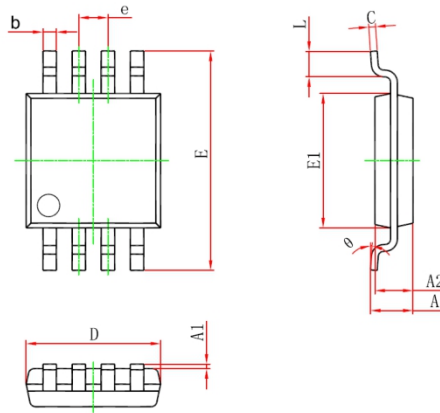
In order for the pre-charge circuitry to dampen the effect of hot-swap insertion of the NCA9511 into an active I2C bus, VCC must be applied before the SCL and SDA pins make contact to the main I2C bus. This is essential when the NCA9511 is placed on the add-on card circuit board, as in Typical Application on a Backplane. Although the pre-charge circuitry exists on both the -IN and -OUT side, the example in Typical Application on a Backplane shows SCLIN and SDAIN connecting to the main bus. The supply voltage to VCC can be applied early by ensuring that the VCC and GND pin contacts are physically longer than the contacts for the SCLIN and SDAIN pins. If a voltage supervisor will also be used to control the voltage supply on the add-on card, additional delay will exist before the 1 V pre-charge voltage is present on the SCL and SDA pins.

**8.2. Power-on reset requirements**

In order to ensure that the part starts up in the correct state, it is recommended that the power supply ramp rates meet the below requirements.

| Parameter | Symbol          | Min | Max  | Unit | Comments |
|-----------|-----------------|-----|------|------|----------|
| Rise rate | t <sub>RT</sub> | 0.1 | 1000 | ms   |          |
| Fall rate | t <sub>FT</sub> | 0.1 | 1000 | ms   |          |

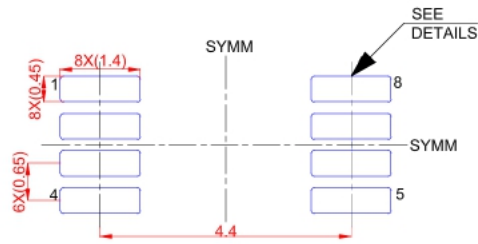
9. Package information



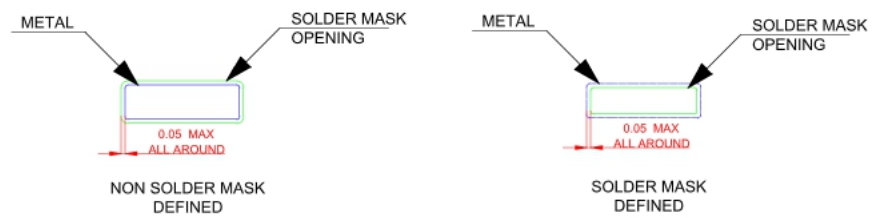
NOTES:  
ALL DIMENSIONS MEET JEDEC STANDARD MO-187 AA

| Symbol | Dimensions In Millimeters |       | Dimensions In Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min                       | Max   | Min                  | Max   |
| A      | ---                       | 1.100 | ---                  | 0.043 |
| A1     | 0.020                     | 0.150 | 0.001                | 0.006 |
| A2     | 0.750                     | 0.950 | 0.030                | 0.037 |
| b      | 0.250                     | 0.380 | 0.010                | 0.015 |
| c      | 0.090                     | 0.230 | 0.004                | 0.009 |
| D      | 2.900                     | 3.100 | 0.114                | 0.122 |
| e      | 0.650 (BSC)               |       | 0.026 (BSC)          |       |
| E      | 4.750                     | 5.050 | 0.187                | 0.199 |
| E1     | 2.900                     | 3.100 | 0.114                | 0.122 |
| L      | 0.400                     | 0.800 | 0.016                | 0.031 |
| 0      | 0°                        | 6°    | 0°                   | 6°    |

Figure 9.1 Package outline for MSOP8

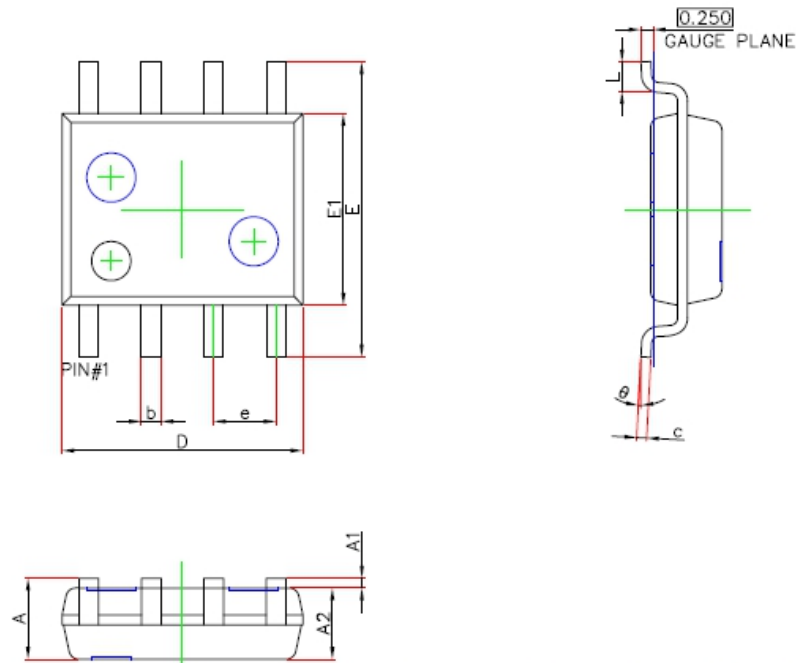


LAND PATTERN EXAMPLE(mm)



### SOLDER MASK DETAILS

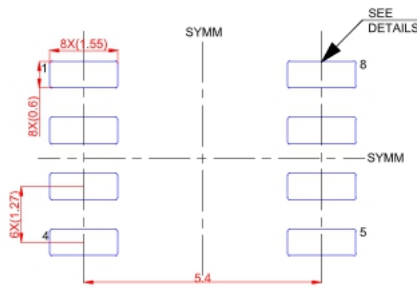
Figure 9.2 MSOP8 Package Board Layout Example



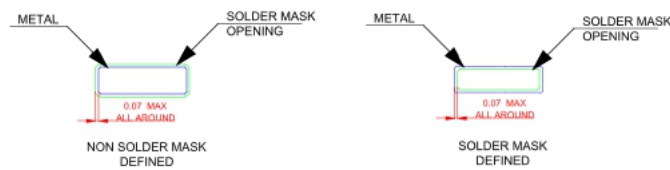
| Symbol   | Dimensions In Millimeters |       | Dimensions In Inches |       |
|----------|---------------------------|-------|----------------------|-------|
|          | Min.                      | Max.  | Min.                 | Max.  |
| A        | 1.450                     | 1.750 | 0.057                | 0.069 |
| A1       | 0.100                     | 0.250 | 0.004                | 0.010 |
| A2       | 1.350                     | 1.550 | 0.053                | 0.061 |
| b        | 0.330                     | 0.510 | 0.013                | 0.020 |
| c        | 0.170                     | 0.250 | 0.007                | 0.010 |
| D        | 4.700                     | 5.100 | 0.185                | 0.201 |
| E        | 5.800                     | 6.200 | 0.228                | 0.244 |
| E1       | 3.800                     | 4.000 | 0.150                | 0.157 |
| e        | 1.270(BSC)                |       | 0.050(BSC)           |       |
| L        | 0.400                     | 1.270 | 0.016                | 0.050 |
| $\theta$ | 0°                        | 8°    | 0°                   | 8°    |

Figure 9.3 Package outline for SOP8





LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 9.4 SOP8 Package Board Layout Example

## 10. Order information

| Part Number  | Pins | Temperature  | MSL | Package Type | Package Qty |
|--------------|------|--------------|-----|--------------|-------------|
| NCA9511-DMSR | 8    | -40 to 105°C | 3   | MSOP8        | 4000        |
| NCA9511-DSPR | 8    | -40 to 105°C | 3   | SOP8         | 4000        |

### 11. Documentation Support

| Part Number | Product Folder             | Datasheet                  | Technical Documents        | Isolator selection guide   |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|
| NCA9511     | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12. Tape and Reel Information

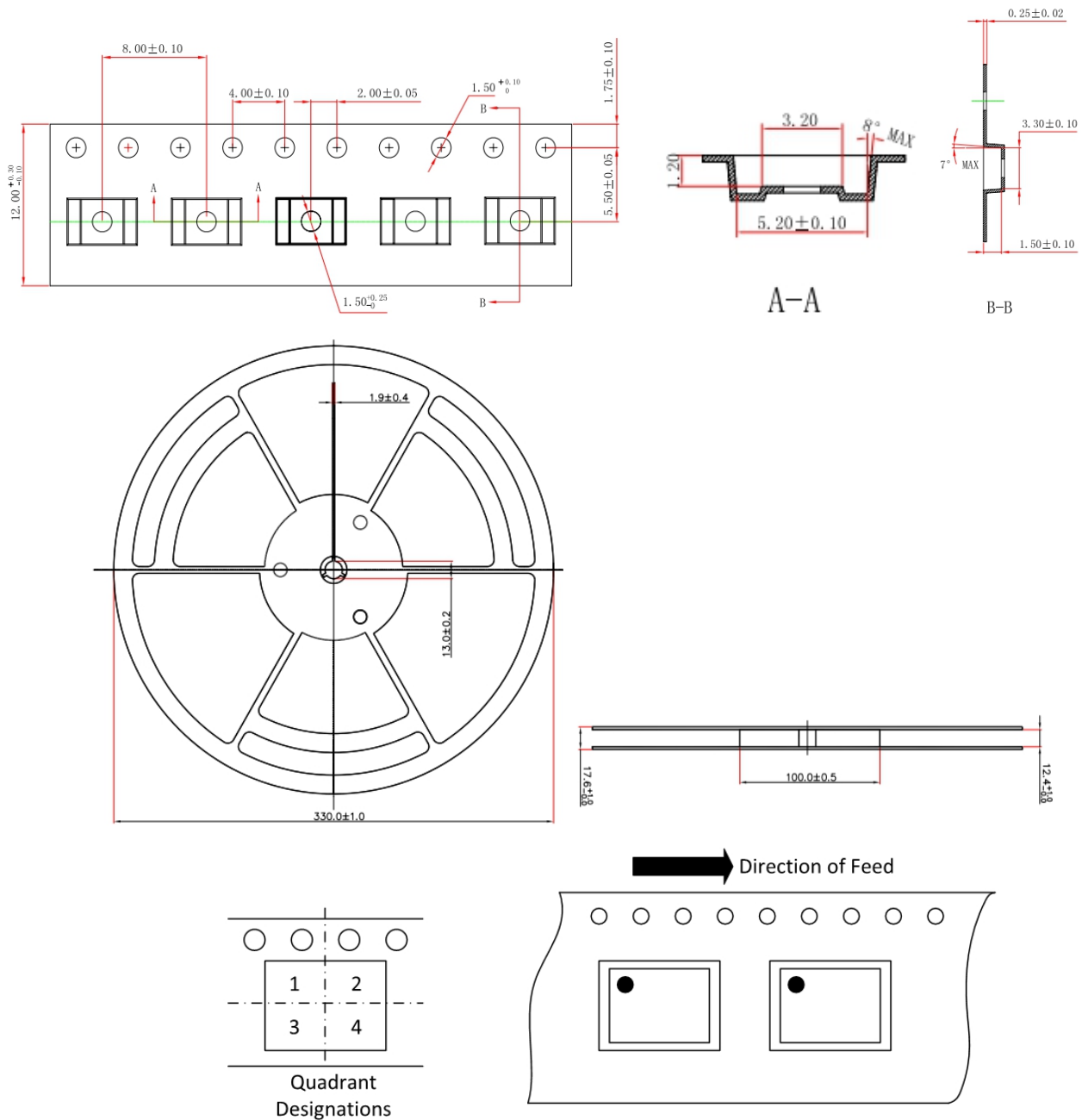


Figure 12.1 Tape and Reel Information of MSOP8

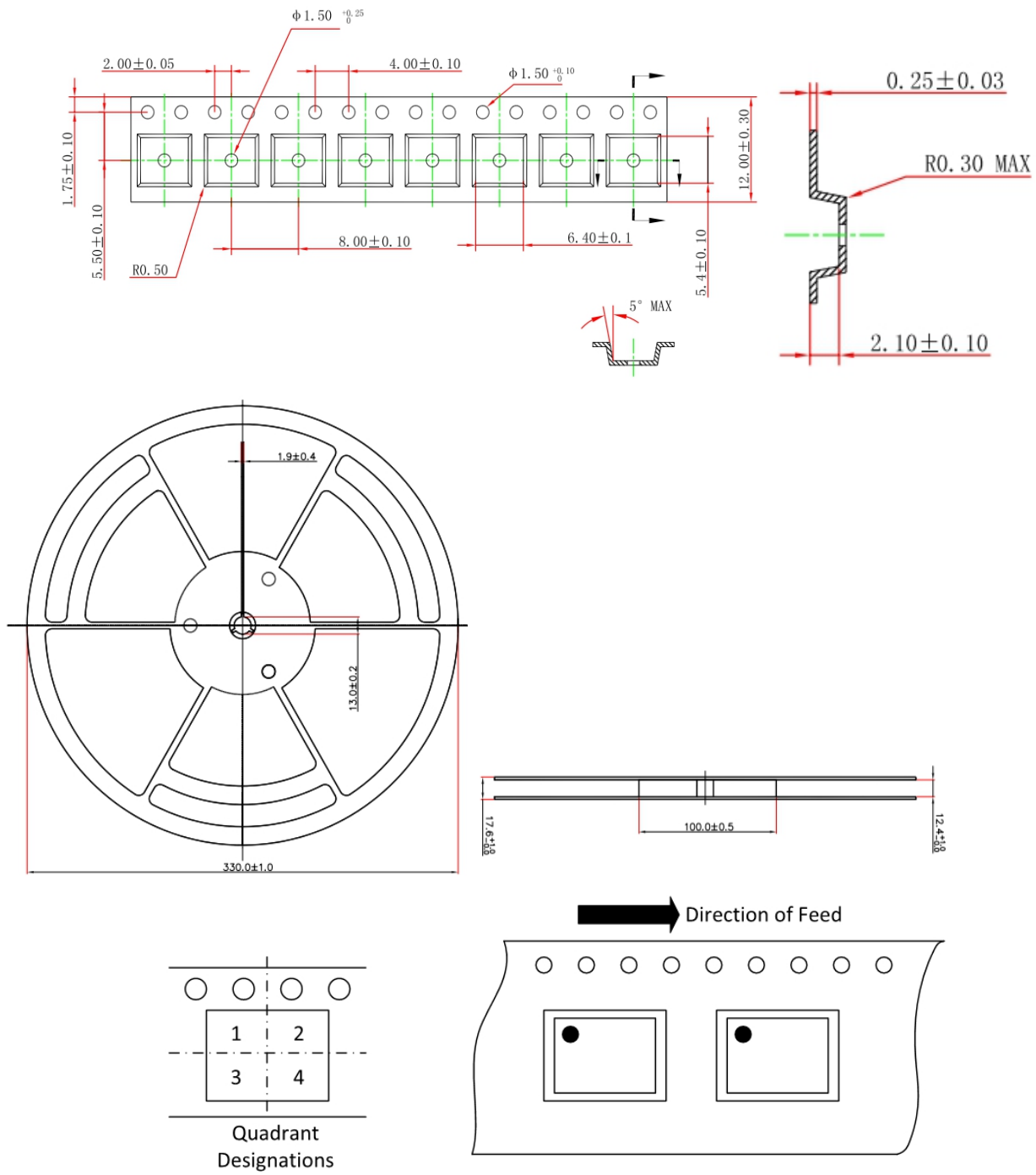


Figure 12.2 Tape and Reel Information of SOP8

### 13. Revision history

| Revision | Description  | Date       |
|----------|--|------------|
| 1.0      | Initial version  | 2019/12/27 |
| 1.1      | Added tape and reel information, changed operation temperature range                                 | 2020/7/6   |
| 1.2      | Changed Storage temperature range and reel pin 1 information, and added Package Board Layout Example | 2022/4/25  |

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