

## Product Overview

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050 device is safety certified by UL1577 support 5kV<sub>rms</sub> insulation withstand voltages, while providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps, and it can support at least 110 CAN nodes. The NSi1050 provides thermal protection and transmit data dominant time out function.

## Key Features

- Fully compatible with the ISO11898-2 standard
- Up to 5000Vrms Insulation voltage
- Power supply voltage
  - VDD1: 2.5V to 5.5V
  - VDD2: 4.5V to 5.5V
- Bus fault protection of -40V to +40V
- Transmit data (TXD) dominant time out function
- Over current and over temperature protection
- Date rate: up to 1Mbps
- High CMTI: 100kV/us
- Low loop delay: <200ns
- High system level EMC performance:
  - Enhanced system level ESD, EFT, Surge immunity
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:
  - SOW16

DUB8

## Safety Regulatory Approvals

- UL recognition: up to 5000Vrms for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

## Applications

- Industrial automation system
- Isolated CAN Bus
- Telecom

## Device Information

Part Number	Package	Body Size
NSi1050-DDBR	DUB8	9.30mm x6.40mm
NSi1050-DSWR	SOW16	10.30mm x 7.50mm

## Functional Block Diagrams

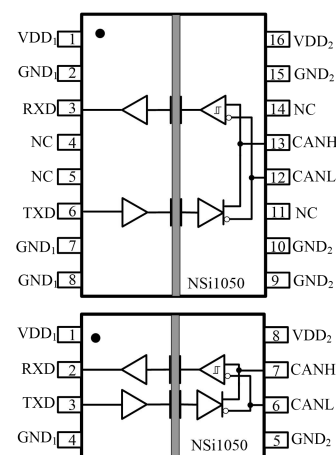


Figure 1. NSi1050 Block Diagram

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### 1.0 PIN CONFIGURATION AND FUNCTIONS

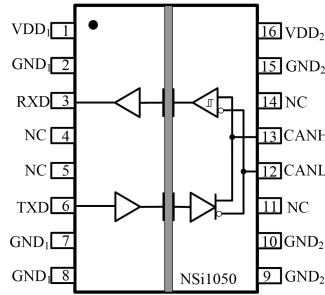


Figure 1.1 NSi1050-DSWR Package

Table1.1 NSi1050-DSWR Pin Configuration and Description

NSi1050-DSWR PIN NO.	SYMBOL	FUNCTION
1	VDD <sub>1</sub>	Power Supply for Side 1
2	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	NC	No Connection
5	NC	No Connection
6	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
7	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
8	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
9	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Bus Side
10	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Bus Side
11	NC	No Connection
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	NC	No Connection
15	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Bus Side
16	VDD <sub>2</sub>	Power supply for Bus Side

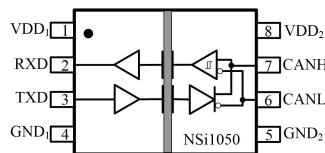


Figure 1.2 NSi1050-DDBR Package

Table1.2 NSi1050-DDBR Pin Configuration and Description

NSi1050-DDBR PIN NO.	SYMBOL	FUNCTION
1	VDD <sub>1</sub>	Power Supply for Side 1
2	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
3	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
4	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
5	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Bus Side
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	VDD <sub>2</sub>	Power supply for Bus Side

## 2.0 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD <sub>1</sub> , VDD <sub>2</sub>	-0.5		6.5	V	
Maximum Input Voltage	V <sub>TXD</sub>	-0.4		VDD <sub>1</sub> +0.4	V	
Maximum BUS Pin Voltage	V <sub>CANH</sub> , V <sub>CANL</sub>	-40		+40	V	
Output current	I <sub>o</sub>	-15		15	mA	
Operating Temperature	T <sub>opr</sub>	-40		125	°C	
Storage Temperature	T <sub>stg</sub>	-40		150	°C	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

## 3.0 RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply voltage, controller side	V <sub>CC1</sub>	2.5		5.5	V	
Supply voltage, bus side	V <sub>CC2</sub>	4.5	5	5.5	V	
Voltage at bus pins (separately or common mode)	V <sub>I</sub> or V <sub>IC</sub>	-12		12	V	
High-level input voltage	V <sub>IH</sub>	2		5.25	V	TXD
Low-level input voltage	V <sub>IL</sub>	0		0.8	V	TXD
High-level output current	I <sub>OH</sub>	-70			mA	Driver
		-4			mA	Receiver
Low-level output current	I <sub>OL</sub>			70	mA	Driver
				4	mA	Receiver

Ambient Temperature	$T_A$	-40		125	°C	
Junction temperature	$T_J$	-40		150	°C	

## 4.0 THERMAL INFORMATION

Parameters	Symbol	DUB8	SOW16	Unit
Junction-to-ambient thermal resistance	$\theta_{JA}$	73.3	76.0	°C/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$	63.2	41	
Junction-to-board thermal resistance	$\theta_{JB}$	43.0	47.7	

## 5.0 SPECIFICATIONS

### 5.1 ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V,  $T_a$ =-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V,  $T_a$  = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	VDD <sub>1</sub>	2.5		5.5	V	
	VDD <sub>2</sub>	4.5	5	5.5	V	
Logic side supply current	IDD <sub>1</sub>		1.97	3.00	mA	VDD <sub>1</sub> =3.3V, TXD=0
			0.97	1.50	mA	VDD <sub>1</sub> =3.3V, TXD=VCC1
			2.02	3.00	mA	VDD <sub>1</sub> =5V, TXD=0
			1.02	1.50	mA	VDD <sub>1</sub> =5V, TXD=VCC1
Bus side supply current	IDD <sub>2</sub>		46	70	mA	TXD=0V, R <sub>Load</sub> =60Ω
			4.45	10	mA	TXD=VDD <sub>2</sub>
Thermal-Shutdown Threshold	T <sub>TS</sub>	155	165	180	°C	
Common Mode Transient Immunity	CMTI	±80	±100		kV/us	
<b>Logic Side</b>						
High level input voltage	V <sub>IH</sub>	2			V	TXD pin
Low level input voltage	V <sub>IL</sub>			0.8	V	TXD pin
High level input current	I <sub>IH</sub>			10	uA	TXD pin
Low level input current	I <sub>IL</sub>	-10			uA	TXD pin
Output Voltage High	V <sub>OH</sub>	VDD <sub>1</sub> -0.4			V	I <sub>OH</sub> = -4mA, RXD pin

Output Voltage Low	$V_{OL}$			0.4	V	$I_{OL} = 4\text{mA}$ , RXD pin
Input Capacitance	$C_{IN}$		2		pF	TXD pin
<b>Driver</b>						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.8	3.44	4	V	$V_I=0\text{V}$ , $R_{Load}=60\Omega$
CANL output voltage (Dominant)	$V_{OL(D)}$	0.8	1.33	2	V	$V_I=0\text{V}$ , $R_{Load}=60\Omega$
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	2.5	3	V	$TXD=VCC1$ , $R_{Load}=60\Omega$
Differential output voltage(Dominant)	$V_{OD(D)}$	1.5		3	V	$TXD=0$ , $R_{Load}=60\Omega$
		1		3		$TXD=0$ , $R_{Load}=45\Omega$
Differential output voltage(Recessive)	$V_{OD(R)}$	-0.12		0.012	V	$TXD=VCC1$ , $R_{Load}=60\Omega$ , see Figure 2.1
		-0.5		0.05	V	$TXD=VCC1$ , NO Load
Common-mode output voltage	$V_{OC}$	2	2.5	3	V	
Peak-to-peak Common-mode output voltage	$V_{OC(PP)}$		250		mV	
Short- circuit output current	$I_{OS}$	-105	-44.1		mA	CANH=-12V, CANL open, see Figure 2.10
			0.28	1	mA	CANH=12V, CANL open, see Figure 2.10
		-1	-0.44		mA	CANL=-12V, CANH open, see Figure 2.10
			42.5	105	mA	CANL=12V, CANH open, see Figure 2.10
<b>Receiver</b>						
Positive-going bus input threshold voltage	$V_{IT+}$		750	900	mV	
Negative-going bus input threshold voltage	$V_{IT-}$	500	650		mV	
Hysteresis voltage	$V_{HYS}$		100		mV	
Input capacitance to ground	$C_I$		13		pF	CANH or CANL
Differential input	$C_{ID}$		5		pF	
Differential input resistance	$R_{ID}$	30		80	k $\Omega$	
Input resistance	$R_{IN}$	15	30	40	k $\Omega$	
Input resistance matching	$R_{I\text{match}}$	-3		+3	%	CANH=CANL
Common-mode voltage range	$V_{COM}$	-12		+12	V	

## 5.2. SWITCHING ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=4.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Loop delay1	T <sub>loop1</sub>	100	165	210	ns	Driver input to receiver output, Recessive to Dominant
Loop delay2	T <sub>loop2</sub>	80	125	170	ns	Driver input to receiver output, Dominant to Recessive
<b>Driver</b>						
Propagation delay time, recessive -to- dominant output	t <sub>PLH</sub>		53	140	ns	
Propagation delay time, dominant -to- recessive output	t <sub>PHL</sub>		78	110	ns	
Differential output signal rise time	t <sub>r</sub>		42		ns	
Differential output signal fall time	t <sub>f</sub>		32		ns	
Bus dominant time-out time	t <sub>TXD_DTO</sub>	300	468	700	us	See Figure 2.9
<b>Receiver</b>						
Propagation delay time, low-to-high-level output	t <sub>PLH</sub>	80	100	150	ns	
Propagation delay time, high-to-low-level output	t <sub>PHL</sub>	65	80	150	ns	
RXD signal rise time	t <sub>r</sub>		3		ns	
RXD signal fall time	t <sub>f</sub>		3		ns	
Fail-Safe output delay time from bus-side power loss	t <sub>fs</sub>		4.2		us	VDD <sub>1</sub> =5V

## 5.3. PARAMETER MEASUREMENT INFORMATION

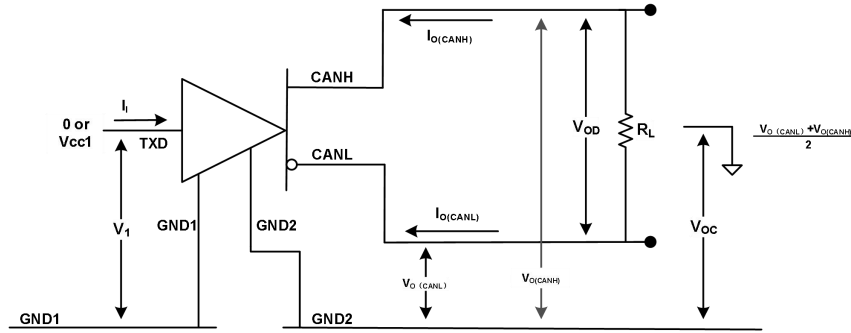


Figure 3.1. Driver Voltage, Current and Test Definitions

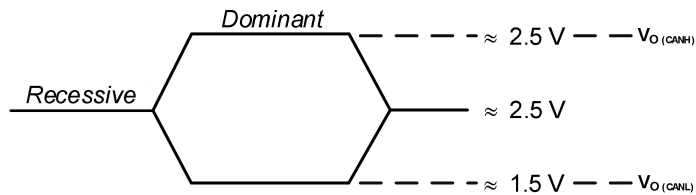


Figure 3.2. Bus Logic State Voltage Definitions

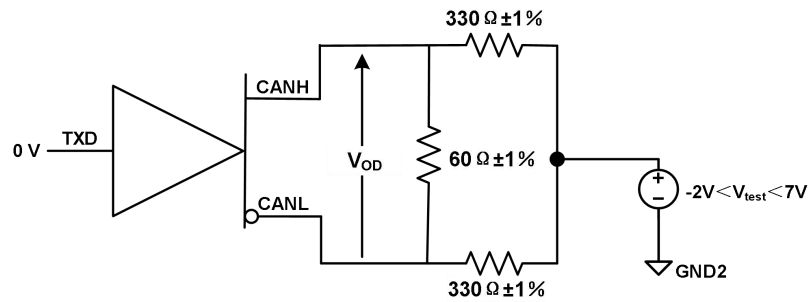
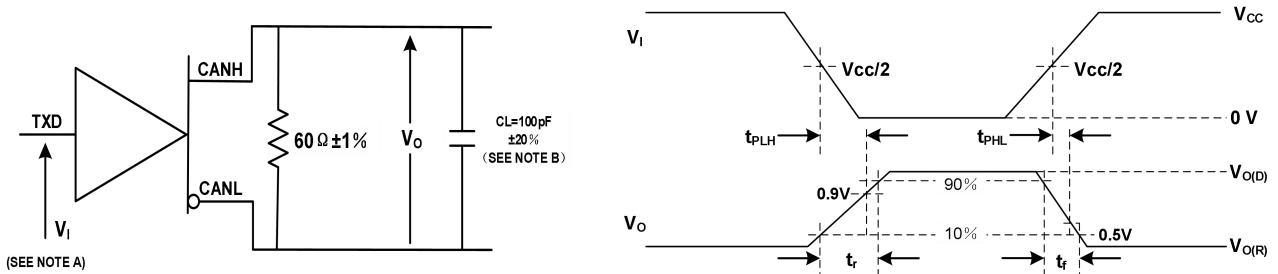


Figure 3.3. Driver VOD With Common-Mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 125 \text{ kHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $ZO = 50 \text{ } \Omega$ .

B. CL includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 3.4. Driver Test Circuit and Voltage Waveform



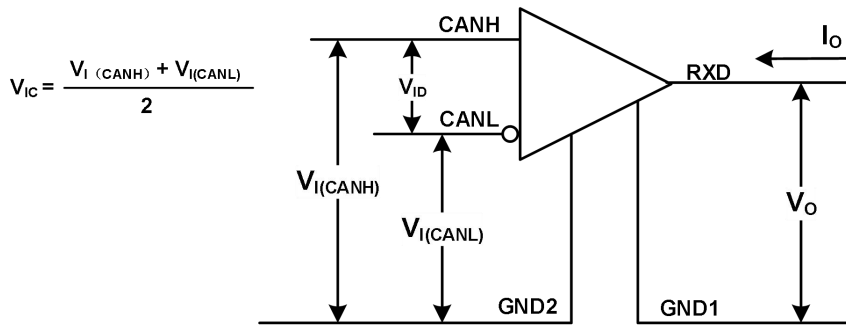
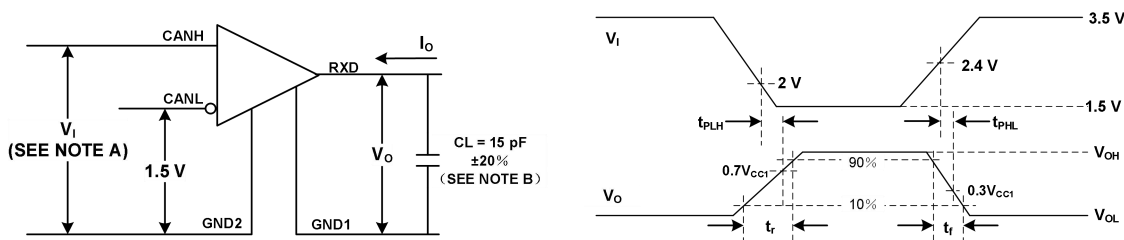


Figure 3.5. Receiver Voltage and Current Definitions



- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 125 \text{ kHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 3.6. Receiver Test Circuit and Voltage Waveform

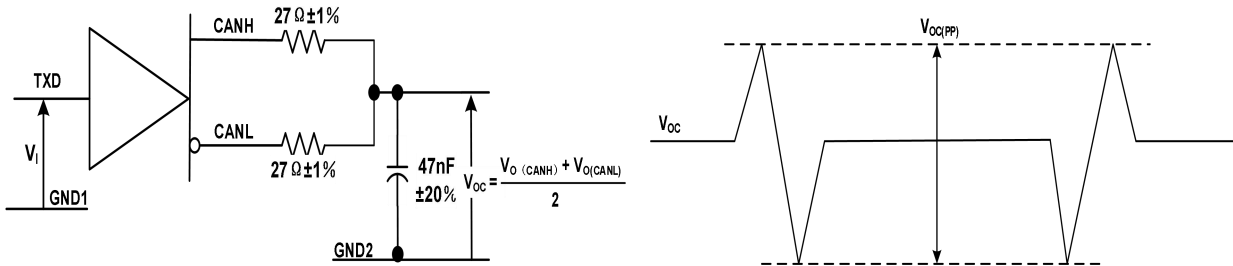


Figure 3.7. Peak-to-Peak Output Voltage Test Circuit and Waveform

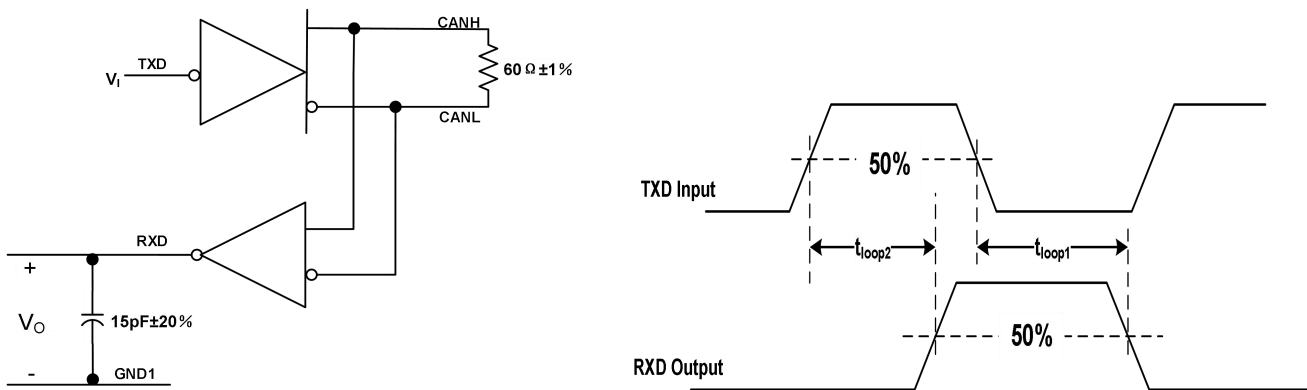
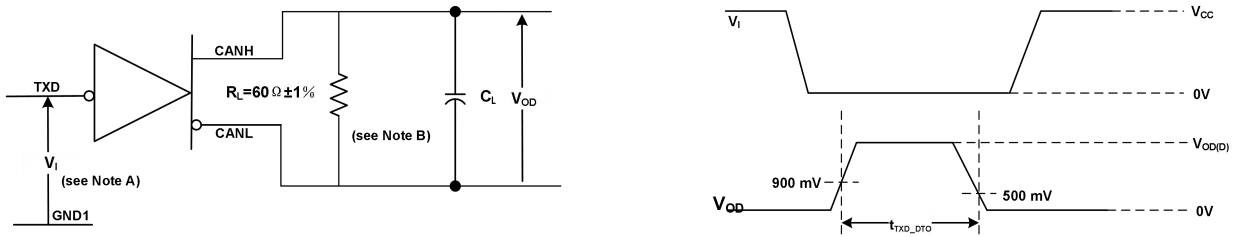


Figure 3.8.  $t_{LOOP}$  Test Circuit and Voltage Waveform



- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 125 \text{ kHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_0 = 50 \ \Omega$ .
- B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 3.9. Dominant Time-out Test Circuit and Voltage Waveform

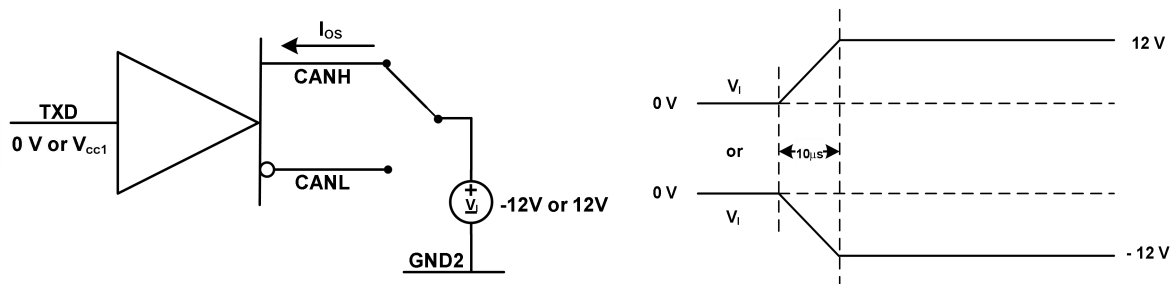


Figure 3.10. Driver Short-Circuit Current Test Circuit and Waveform

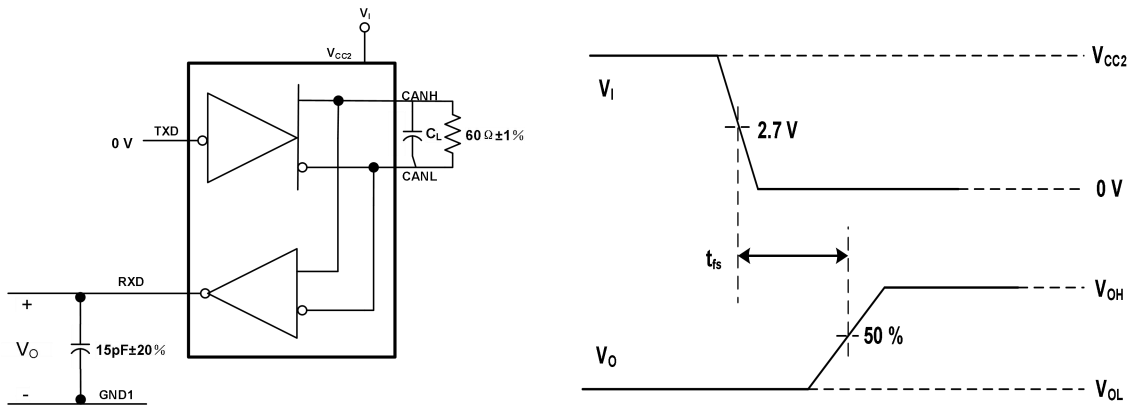


Figure 3.11. Fail-Safe Delay Time Test Circuit and Voltage Waveform

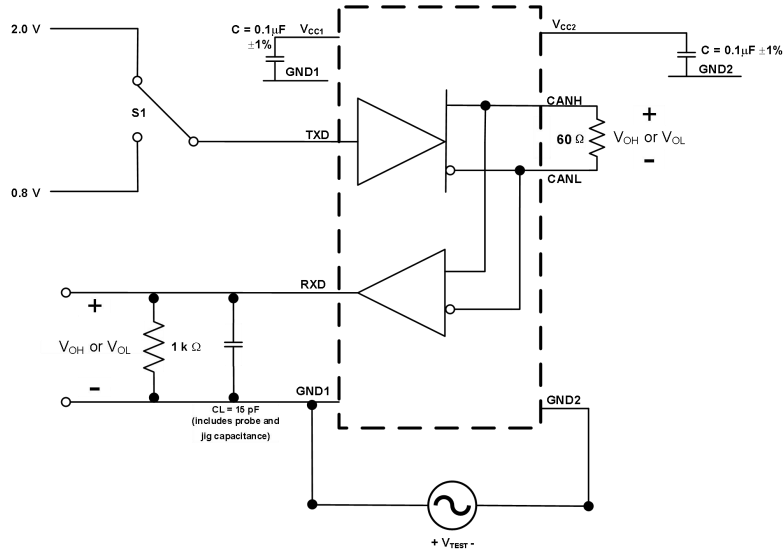


Figure 3.12. Common-Mode Transient Immunity Test Circuit

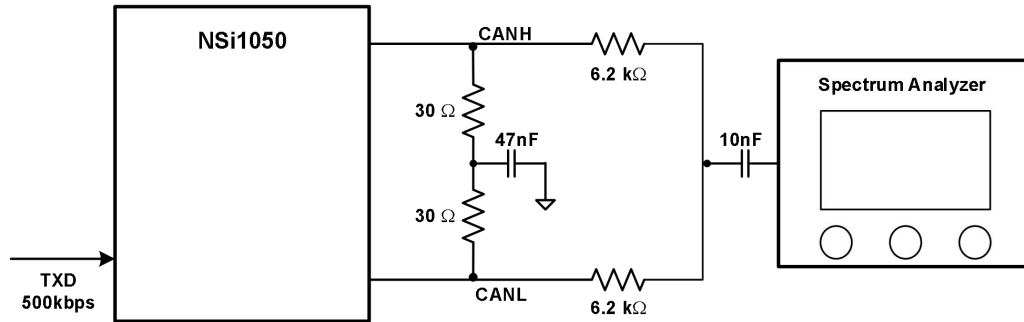


Figure 3.13. Electromagnetic Emissions Measurement Setup

## 6.0 HIGH VOLTAGE FEATURE DESCRIPTION

### 6.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	Symbol	Value		Unit	Comments
		DUB8	SOW16		
Minimum External Air Gap (Clearance)	L(I01)	6.5	8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	6.5	8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20		um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>400	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		II	I		

6.2. DIN VDE V 0884-11 (VDE V 0884-11) :2017-01 INSULATION CHARACTERISTICS

Description	Test Condition	Symbol	Value		Unit
			DUB8	SOW16	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage $\leq 150V_{rms}$			I to IV	I to IV	
For Rated Mains Voltage $\leq 300V_{rms}$			I to III	I to III	
For Rated Mains Voltage $\leq 400V_{rms}$			I to III	I to III	
Climatic Classification			10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum Working Isolation Voltage	AC voltage	$V_{IOWM}$	400	1500	$V_{RMS}$
	DC voltage		565	2121	$V_{DC}$
Maximum repetitive isolation voltage		$V_{IORM}$	565	2121	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$ , 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	847	/	Vpeak
	$V_{IORM} \times 1.875 = V_{pd(m)}$ , 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge $< 5$ pC		/	3977	Vpeak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	678	/	Vpeak
	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC		/	3394	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	678	2545	Vpeak
Maximum transient isolation voltage	$t = 60$ sec	$V_{IOTM}$	5300	8000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST} = V_{IOSM} \times 1.3$	$V_{IOSM}$	5384	/	Vpeak

	Test method per IEC60065, 1.2/50us waveform, $V_{TEST}=V_{IOSM}\times 1.6$		/	6250	Vpeak
Isolation resistance	$V_{IO}=500V$ at $T_{amb}=T_S$	RIO	$>10^9$	$>10^9$	$\Omega$
	$V_{IO}=500V$ at $100^\circ C \leq T_{amb} \leq 125^\circ C$		$>10^{11}$	$>10^{11}$	$\Omega$
Isolation capacitance	$f = 1MHz$	CIO	0.8	0.8	pF
Input capacitance		CI	2	2	pF
Total Power Dissipation at 25°C		Ps	1.7	1.5	W
Safety input, output, or supply current	$\theta_{JA} = 72^\circ C/W$ , $V_I = 5.5 V$ , $T_J = 150^\circ C$ , $T_A = 25^\circ C$	Is	310		mA
Safety input, output, or supply current	$\theta_{JA} = 84^\circ C/W$ , $V_I = 5.5 V$ , $T_J = 150^\circ C$ , $T_A = 25^\circ C$	Is		299	mA
Case Temperature		Ts	150	150	$^\circ C$

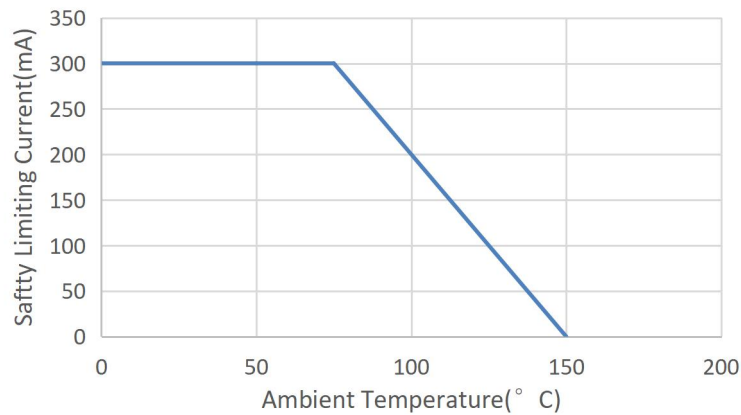


Figure 3.1 NSi1050-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

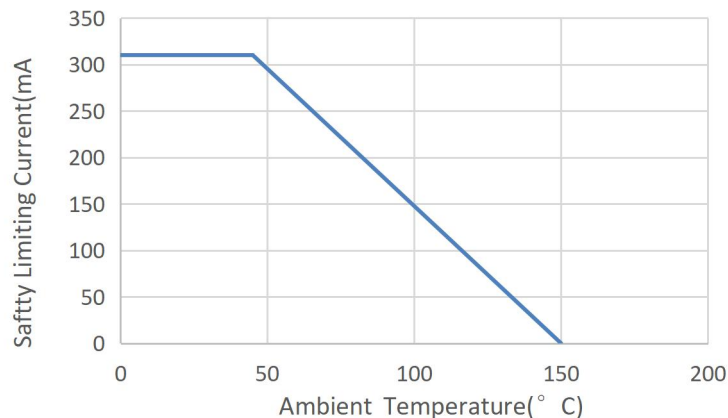


Figure 3.1 NSi1050-DDBR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

### 6.3. REGULATORY INFORMATION

The NSi1050-DDBR is approved by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01 <sup>2</sup>	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750V <sub>rms</sub> Isolation voltage	Single Protection, 3750V <sub>rms</sub> Isolation voltage	Basic Insulation 565V <sub>peak</sub> , V <sub>IOSM</sub> =5384V <sub>peak</sub>	Basic insulation at 400V <sub>rms</sub> (565V <sub>peak</sub> )
File (E500602)	File (E500602)	File (40050121)	File (CQC20001263786)

The NSi1050-DSWR is approved by the organizations listed in table.

<i>CUL</i>		<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01 <sup>2</sup>	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V <sub>rms</sub> Isolation voltage	Single Protection, 5000V <sub>rms</sub> Isolation voltage	Reinforced Insulation 2121V <sub>peak</sub> , V <sub>IOSM</sub> =6250V <sub>peak</sub>	Basic insulation at 1500V <sub>rms</sub> (2121V <sub>peak</sub> )
File (E500602)	File (E500602)	File (pending)	File (CQC20001264939)

## 7.0 FUNCTION DESCRIPTION

The NSi1050 is a isolated CAN transceiver which fully compatible with the ISO11898-2 standard. The NSi1050 integrated two channel digital isolators and a high reliability CAN transceiver. The digital isolator is silicon oxide isolation based on Novosense capacity isolation technology. The high integrated solution can help to simplify system design and improve reliability. The NSi1050-DSWR device is safety certified by UL1577 support 5kV<sub>rms</sub> insulation withstand voltages, while the NSi1050-DDBR device is safety certified by UL1577 support 3kV<sub>rms</sub> insulation withstand voltages. The NSi1050 is providing high electromagnetic immunity and low emissions. The data rate of the NSi1050 is up to 1Mbps, and it can support at least 110 CAN nodes. The NSi1050 provides thermal protection and transmit data dominant time out function.

### 7.1. DEVICE FUNCTIONAL MODES

Table 4.1. Driver Function Table

<i>TXD</i>	<i>CANH</i>	<i>CANL</i>	<i>BUS STATE</i>
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

<sup>1</sup> H= high level; L=low level; Z= common mode(recessive) bias to  $V_{CC}/2$

Table 4.2. Receiver Function Table

$V_{ID}=CANH-CANL$	RXD	BUS STATE
$V_{ID} \geq 0.9V$	L	Dominant
$0.5 < V_{ID} < 0.9V$	X	Uncertain
$V_{ID} \leq 0.5V$	H	Recessive
Open	H	Recessive

<sup>1</sup> H= high level; L=low level; X= uncertain

### 7.2. TXD DOMINANT TIME-OUT FUNCTION

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state(blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value ( $t_{TXD\_DTO}$ ), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

### 7.3. CURRENT PROTECTION

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

### 7.4. OVER TEMPERATURE PROTECTION

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature  $T_{TS}$ , the output drivers will be disabled until the virtual junction temperature becomes lower than  $T_{TS}$  and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

## 8.0 APPLICATION NOTE

### 8.1. TYPICAL APPLICATION

The NSi1050 requires a 0.1  $\mu F$  bypass capacitors between VDD1 and GND1, VDD2and GND2. The capacitor should be placed as close as possible to the package. The figure5.1 is the basic schematic of NSi1050.

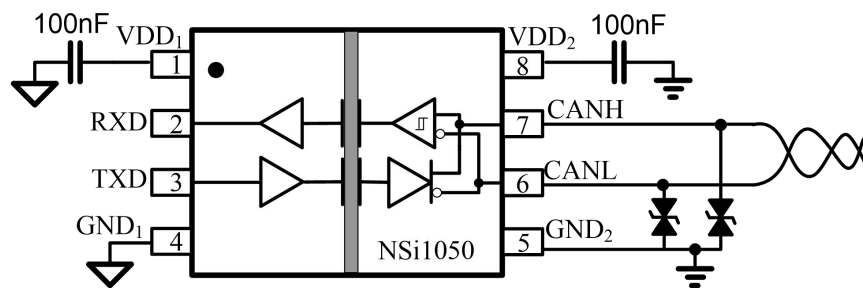


Figure6.1 Basic schematic of NSi1050

8.2. PCB LAYOUT

The recommended PCB layout shown below.

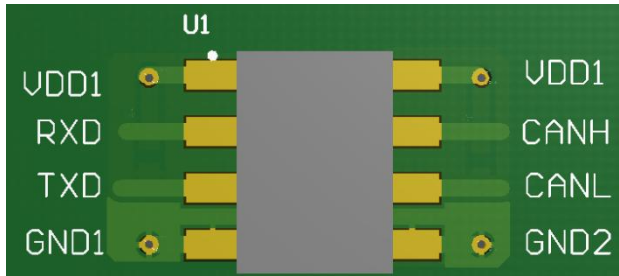


Figure 6.2 Recommended PCB Layout — Top Layer



Figure 6.3 Recommended PCB Layout — Bottom Layer

9.0 PACKAGE INFORMATION

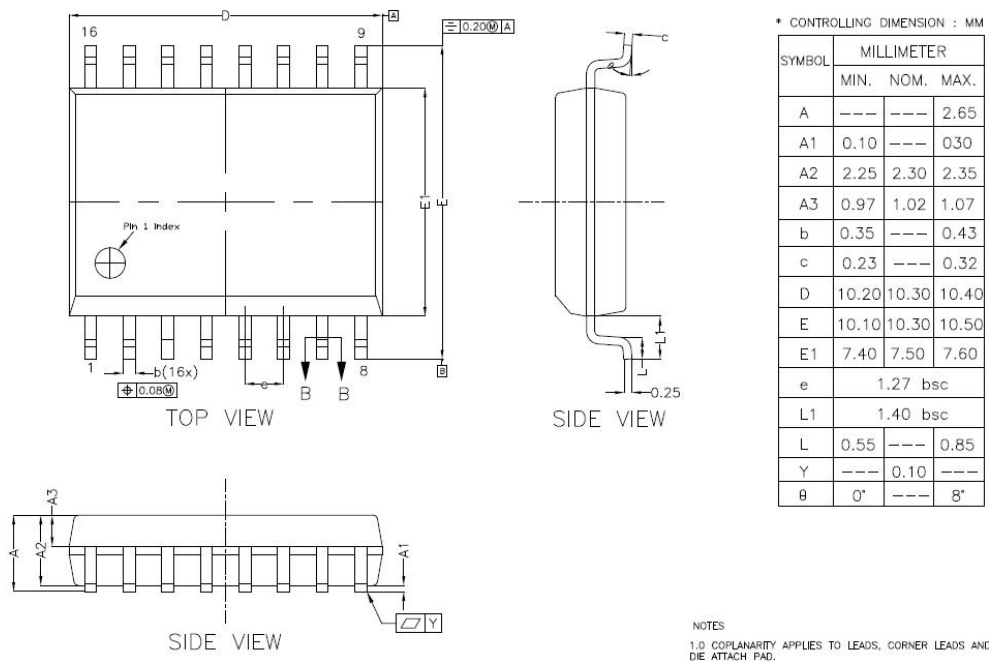
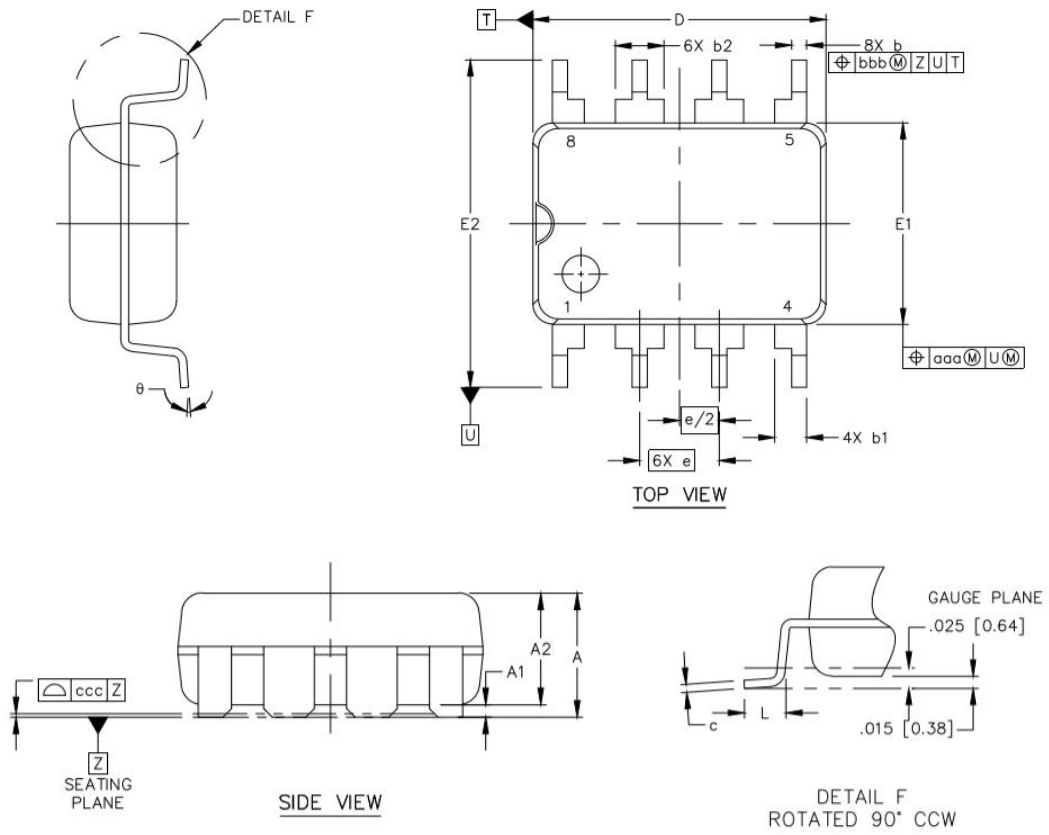


Figure 7.1 SOW16 Package Shape and Dimension in millimeters (inches)





	SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.141	---	.165	3.58	---	4.19
STAND OFF	A1	.015	---	.023	0.38	---	0.58
MOLD THICKNESS	A2	.126	---	.142	3.20	---	3.61
LEAD WIDTH	b	.014	---	.022	0.36	---	0.56
	b1	---	0.039 REF	---	---	0.99 REF	---
	b2	---	0.06 REF	---	---	1.524 REF	--
L/F THICKNESS	c	.008	---	.014	0.20	---	0.36
BODY SIZE	D	.365	---	.369	9.27	---	9.37
	E1	.244	---	.260	6.20	---	6.60
	E2	.398	---	.421	10.11	---	10.69
LEAD PITCH	e	.100 BSC			2.54 BSC		
LEAD LENGTH	L	.0453	---	.0571	1.15	---	1.45
	θ	0°	---	8°	0°	---	8°
LEAD OFFSET	aaa	.010			0.254		

Figure 7.2 DUB8 Package Shape and Dimension in millimeters (inches)

## 10.0 ORDER INFORMATION

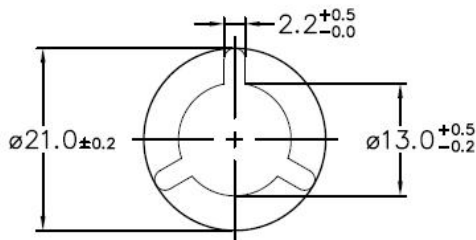
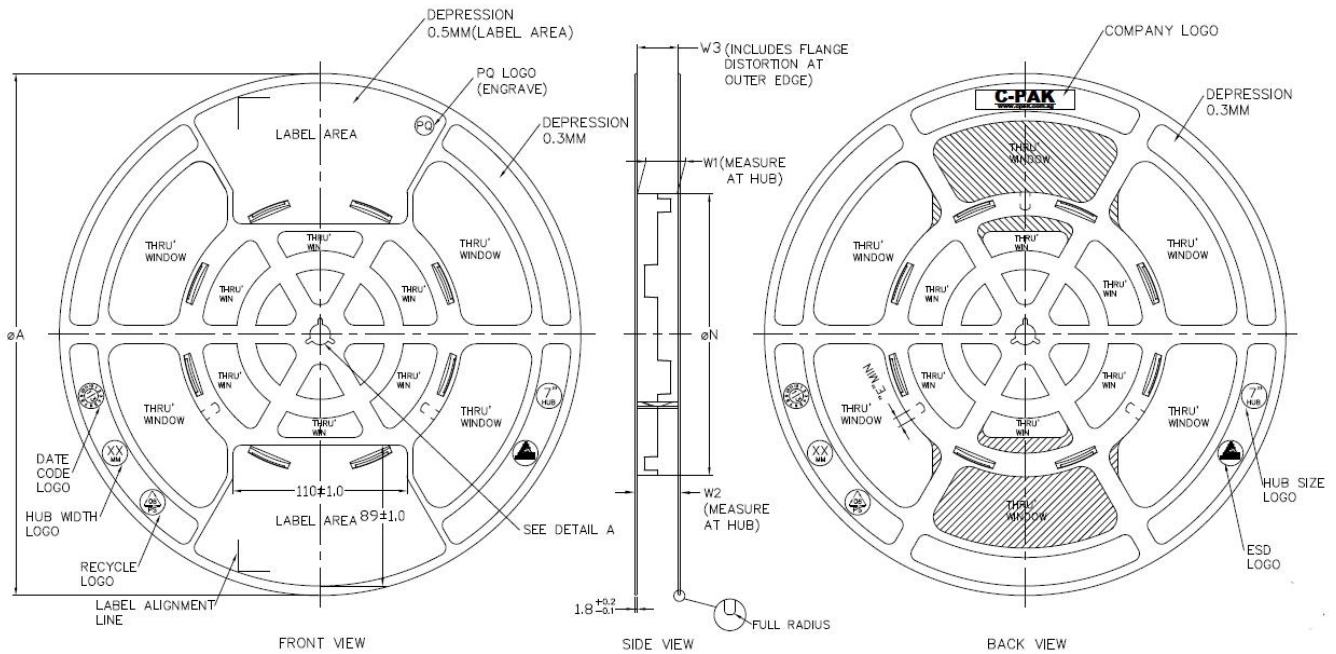
Part Number	Isolation Rating (kV)	Max Data Rate (Mbps)	Temperature	MSL	Package Type	Package Drawing	SPQ
NSI1050-DDBR	3	1	-40 to 125°C	3	DUB8	DUB8	800
NSI1050-DSWR	5	1	-40 to 125°C	2	SOW16 (300mil)	SOW16	1000

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

### 11.0 DOCUMENTATION SUPPORT

Part Number	Product Folder	Datasheet	Technical Documents	Isolator selection guide
NSi1050	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

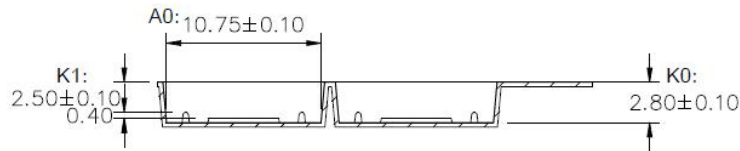
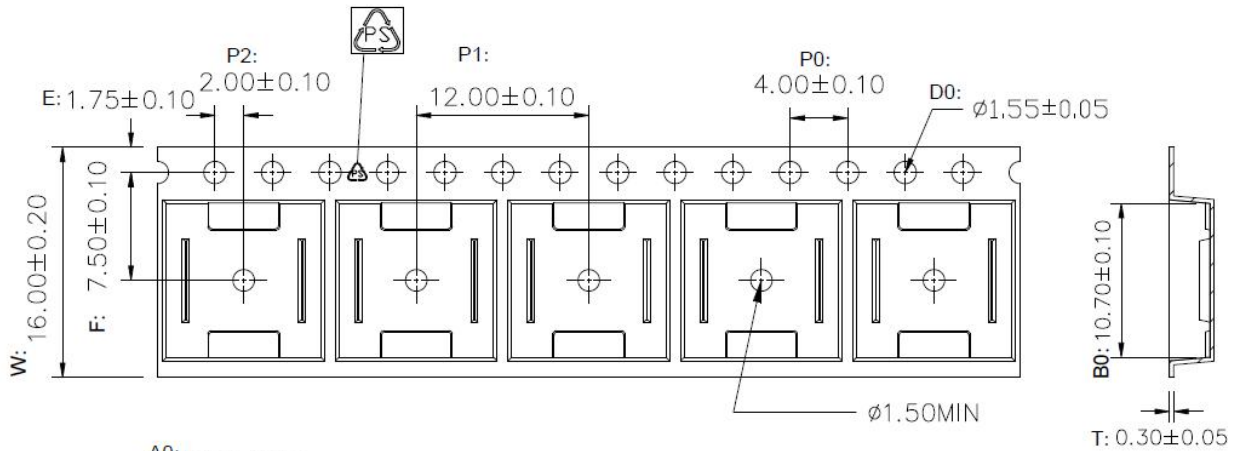
### 12.0 TAPE AND REEL INFORMATION



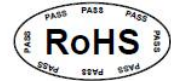
ARBOR HOLE  
DETAIL A  
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	$\phi A$ $\pm 2.0$	$\phi N$ $\pm 2.0$	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 <sup>+1.5</sup> <sub>-0.0</sub>	14.4	SMALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	18.4		5.5
16MM	330	178	16.4 <sup>+2.0</sup> <sub>-0.0</sub>	22.4		5.5
24MM	330	178	24.4 <sup>+2.0</sup> <sub>-0.0</sub>	30.4		5.5
32MM	330	178	32.4 <sup>+2.0</sup> <sub>-0.0</sub>	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10 <sup>12</sup>	ANTISTATIC	ALL TYPES
B	10 <sup>8</sup> TO 10 <sup>11</sup>	STATIC DISSIPATIVE	BLACK ONLY
C	10 <sup>5</sup> & BELOW 10 <sup>5</sup>	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10 <sup>8</sup> TO 10 <sup>11</sup>	ANTISTATIC (COATED)	ALL TYPES



1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.20$  .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness :  $0.30 \pm 0.05$ mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :  $10^5 \sim 10^{10} \Omega/\square$



W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

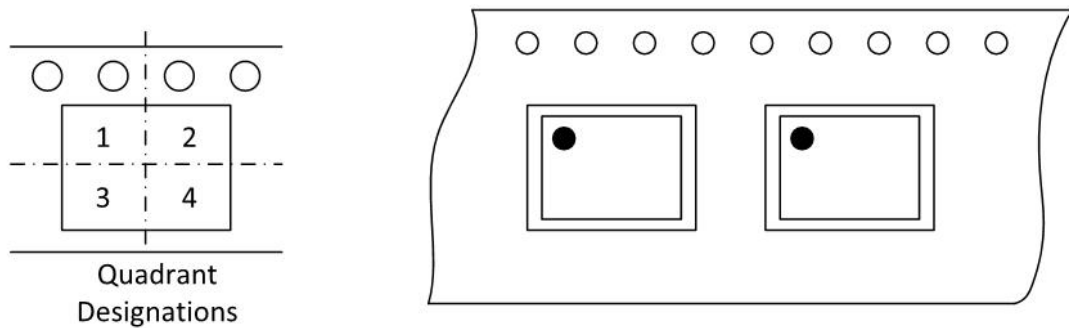
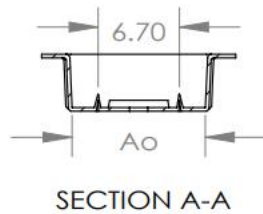
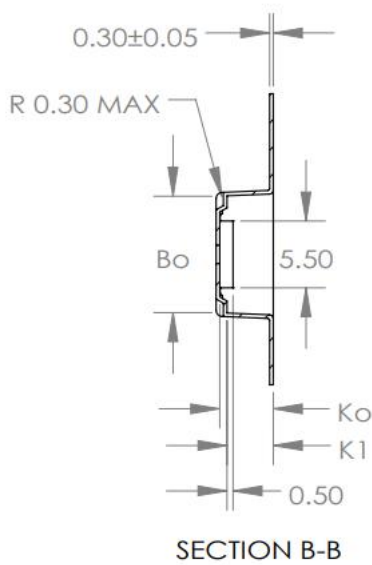
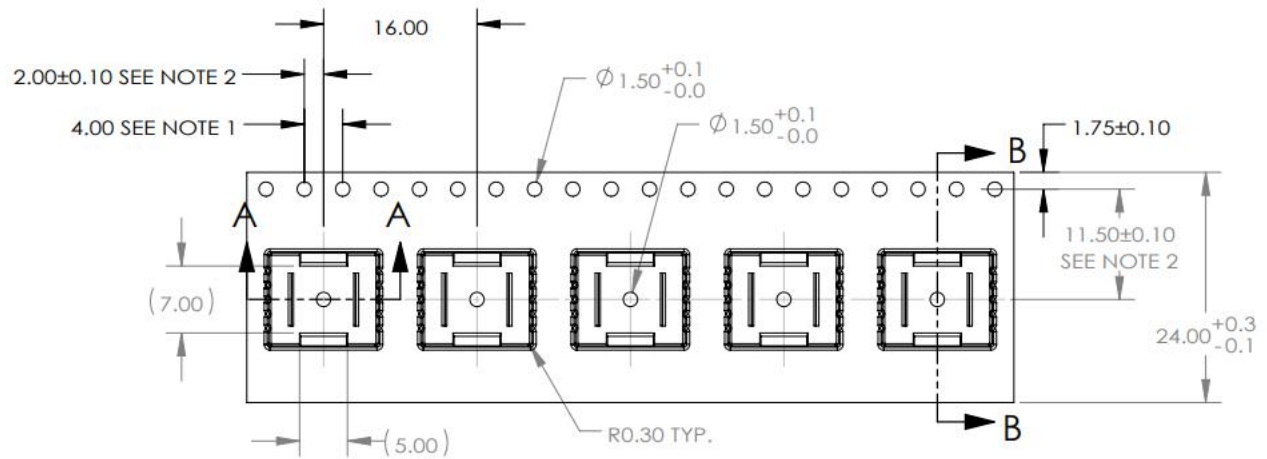


Figure 7.1 Tape and Reel Information of SOW16



	DIM	±
Ao	11.00	0.10
Bo	9.60	0.10
Ko	4.40	0.10
K1	3.80	0.10

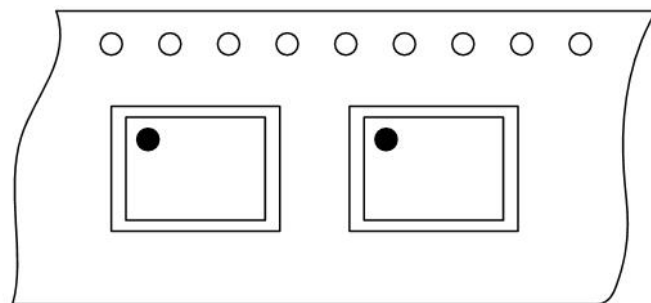
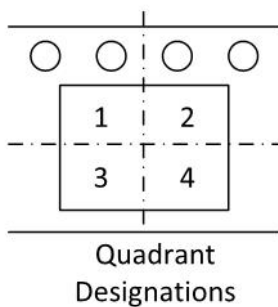


Figure 7.2 Tape and Reel Information of DUB8

### 13.0 REVISION HISTORY

Revision	Description	Date
1.0	Initial version	2020/8/7

1.1	Changed tape and reel information	2020/12/20
1.2	Added DUB8 tape and reel information	2021/3/1
1.3	Update Regulatory information	2021/4/13

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[SIT1042AT/3](#) [SIT1043QT](#) [SIT1042ATK/3](#) [SIT1057TK/3](#) [SL1040S](#) [SJA1000M/TR](#)