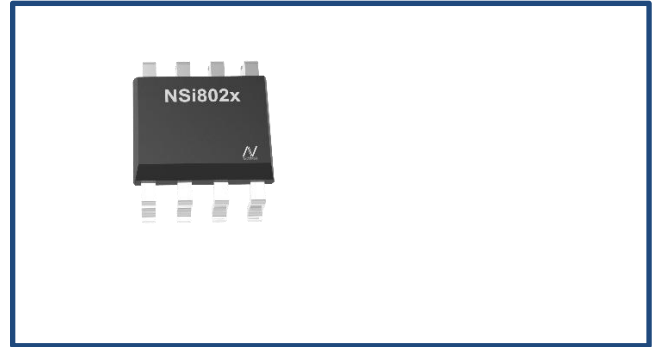


## Product Overview

The NSI802x devices are high reliability dual-channel digital isolator. The NSI802x device is safety certified by UL1577 support  $3kV_{rms}$  insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI802x is up to 10Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. The NSI802x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI802x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

## Key Features

- Up to  $3000V_{rms}$  Insulation voltage
- Data rate: DC to 10Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 100kV/us
- Chip level ESD: HBM:  $\pm 4kV$
- High system level EMC performance:
  - Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Isolation barrier life: >40 years
- Low power consumption: 1mA/ch (500kbps)
- Propagation delay: <500ns
- Operation temperature:  $-40^{\circ}C \sim 125^{\circ}C$
- RoHS-compliant packages:
  - SOIC-8 narrow body



## Safety Regulatory Approvals

- UL recognition: up to  $3000V_{rms}$  for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

## Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

## Functional Block Diagrams

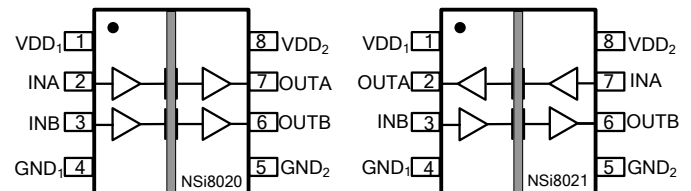


Figure 1. NSI802xN Block Diagram

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## 1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB	-0.4		VDD+0.4 <sup>1</sup>	V	
Maximum Output Voltage	V <sub>OUTA</sub> , V <sub>OUTB</sub>	-0.4		VDD+0.4 <sup>1</sup>	V	
Maximum Input/Output Pulse Voltage	VINA, VINB, V <sub>OUTA</sub> , V <sub>OUTB</sub>	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Common-Mode Transients	CMTI			±100	kV/us	
Output current	I <sub>o</sub>	-15		15	mA	
Maximum Surge Isolation Voltage	V <sub>IOSM</sub>			5.3	kV	
Operating Temperature	T <sub>opr</sub>	-40		125	°C	
Storage Temperature	T <sub>stg</sub>	-40		150	°C	
Electrostatic discharge	HBM			±4000	V	
	CDM			±2000	V	

<sup>1</sup>The maximum voltage must not exceed 6.5V.

## 2.0 SPECIFICATIONS

### 2.1. ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD <sub>POR</sub>		2.2		V	POR threshold as during power-up
	VDD <sub>HYS</sub>		0.1		V	POR threshold Hysteresis
High Level Input Voltage	V <sub>IH</sub>	0.7*VDD			V	
Low Level Input Voltage	V <sub>IL</sub>			0.3*VDD	V	
High Level Output Voltage	V <sub>OH</sub>	VDD-0.3			V	I <sub>OH</sub> ≤ 4mA
Low Level Output Voltage	V <sub>OL</sub>			0.3	V	I <sub>OL</sub> ≤ 4mA
Output Impedance	R <sub>out</sub>		50		ohm	
Input Pull high or low Current	I <sub>pull</sub>		8	15	uA	

# NSI8020/NSI8021

Start Up Time after POR	trbs		40		usec	
Common Mode Transient Immunity	CMTI	±80		±100	kV/us	

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSI8020</b>					
	I <sub>DD1</sub> (Q0)		0.48		mA	All Input 0V for NSI8020x0 Or All Input at supply for NSI8020x1
	I <sub>DD2</sub> (Q0)		1.02		mA	
	I <sub>DD1</sub> (Q1)		1.57		mA	All Input at supply for NSI8020x0 Or All Input 0V for NSI8020x1
	I <sub>DD2</sub> (Q1)		1.02		mA	
	I <sub>DD1</sub> (0.5M)		1.03		mA	All Input with 500kbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (0.5M)		1.11		mA	
	<b>NSI8021</b>					
	I <sub>DD1</sub> (Q0)		0.8		mA	All Input 0V for NSI8021x0 Or All Input at supply for NSI8021x1
	I <sub>DD2</sub> (Q0)		0.8		mA	
	I <sub>DD1</sub> (Q1)		1.4		mA	All Input at supply for NSI8021x0 Or All Input 0V for NSI8021x1
	I <sub>DD2</sub> (Q1)		1.4		mA	
	I <sub>DD1</sub> (0.5M)		1.25		mA	All Input with 500kbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (0.5M)		1.25		mA	
Data Rate	DR	0		10	Mbps	
Minimum Pulse Width	PW			50.0	ns	
Propagation Delay	t <sub>PLH</sub>		30		ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>		30		ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			10.0	ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
Peak Eye Diagram Jitter	t <sub>JIT</sub> (PK)		350		ps	
Channel-to-Channel Delay Skew	t <sub>SK</sub> (c2c)			10.0	ns	
Part-to-Part Delay Skew	t <sub>SK</sub> (p2p)			10.0	ns	

# NSI8020/NSI8021

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSI8020</b>					
	I <sub>DD1</sub> (Q0)		0.44		mA	All Input 0V for NSI8020x0 Or All Input at supply for NSI8020x1
	I <sub>DD2</sub> (Q0)		0.98		mA	
	I <sub>DD1</sub> (Q1)		1.53		mA	All Input at supply for NSI8020x0 Or All Input 0V for NSI8020x1
	I <sub>DD2</sub> (Q1)		1		mA	
	I <sub>DD1</sub> (0.5M)		1		mA	All Input with 500kbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (0.5M)		1.04		mA	
	<b>NSI8021</b>					
	I <sub>DD1</sub> (Q0)		0.77		mA	All Input 0V for NSI8021x0 Or All Input at supply for NSI8021x1
	I <sub>DD2</sub> (Q0)		0.77		mA	
	I <sub>DD1</sub> (Q1)		1.35		mA	All Input at supply for NSI8021x0 Or All Input 0V for NSI8021x1
	I <sub>DD2</sub> (Q1)		1.35		mA	
I <sub>DD1</sub> (0.5M)		1.11		mA	All Input with 500kbps, C <sub>L</sub> = 15pF	
I <sub>DD2</sub> (0.5M)		1.11		mA		
Data Rate	DR	0		10	Mbps	
Minimum Pulse Width	PW			50.0	ns	
Propagation Delay	t <sub>PLH</sub>		30		ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>		30		ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			10.0	ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 2.7</a> , C <sub>L</sub> = 15pF
Peak Eye Diagram Jitter	t <sub>JIT</sub> (PK)		350		ps	
Channel-to-Channel Delay Skew	t <sub>sk</sub> (c2c)			10.0	ns	
Part-to-Part Delay Skew	t <sub>sk</sub> (p2p)			10.0	ns	

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
------------	--------	-----	-----	-----	------	----------

Supply current	<b>NSI8020</b>					
	$I_{DD1}(Q0)$		0.43		mA	All Input 0V for NSI8020x0 Or All Input at supply for NSI8020x1
	$I_{DD2}(Q0)$		0.96		mA	
	$I_{DD1}(Q1)$		1.52		mA	All Input at supply for NSI8020x0 Or All Input 0V for NSI8020x1
	$I_{DD2}(Q1)$		0.98		mA	
	$I_{DD1}(0.5M)$		1		mA	All Input with 500kbps, $C_L = 15pF$
	$I_{DD2}(0.5M)$		1		mA	
	<b>NSI8021</b>					
	$I_{DD1}(Q0)$		0.75		mA	All Input 0V for NSI8021x0 Or All Input at supply for NSI8021x1
	$I_{DD2}(Q0)$		0.75		mA	
	$I_{DD1}(Q1)$		1.33		mA	All Input at supply for NSI8021x0 Or All Input 0V for NSI8021x1
	$I_{DD2}(Q1)$		1.33		mA	
	$I_{DD1}(0.5M)$		1.08		mA	All Input with 500kbps, $C_L = 15pF$
	$I_{DD2}(0.5M)$		1.08		mA	
Data Rate	DR	0		10	Mbps	
Minimum Pulse Width	PW			50.0	ns	
Propagation Delay	$t_{PLH}$		440		ns	See <a href="#">Figure 2.7</a> , $C_L = 15pF$
	$t_{PHL}$		440		ns	See <a href="#">Figure 2.7</a> , $C_L = 15pF$
Pulse Width Distortion $ t_{PHL} - t_{PLH} $	PWD			10.0	ns	See <a href="#">Figure 2.7</a> , $C_L = 15pF$
Rising Time	$t_r$			5.0	ns	See <a href="#">Figure 2.7</a> , $C_L = 15pF$
Falling Time	$t_f$			5.0	ns	See <a href="#">Figure 2.7</a> , $C_L = 15pF$
Peak Eye Diagram Jitter	$t_{JIT}(PK)$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			10.0	ns	
Part-to-Part Delay Skew	$t_{SK}(p2p)$			5.0	ns	

## 2.2. PARAMETER MEASUREMENT INFORMATION

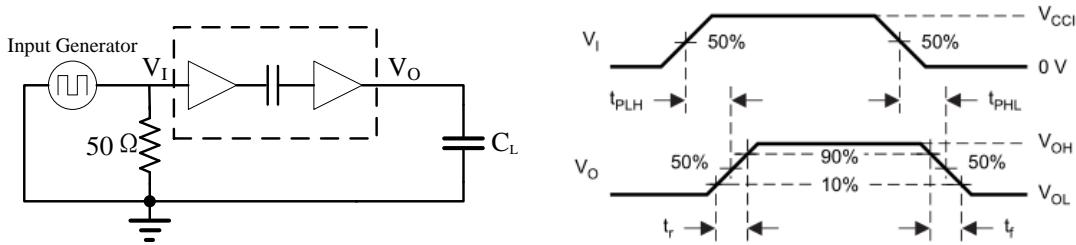


Figure 2.7 Switching Characteristics Test Circuit and Waveform

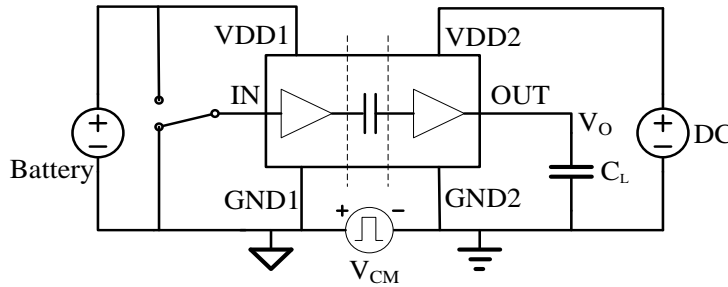


Figure 2.8 Common-Mode Transient Immunity Test Circuit

## 3.0 HIGH VOLTAGE FEATURE DESCRIPTION

### 3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	Symbol	Value	Unit	Comments
		SOIC-8		
Minimum External Air Gap (Clearance)	L(I01)	4.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20	um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>400	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		II		

### 3.2. DIN VDE V 0884-11 (VDE V 0884-11) :2017-01 INSULATION CHARATERISTICS

Description	Test Condition	Symbol	Value	Unit
			SOIC-8	

Installation Classification per DIN VDE 0110				
For Rated Mains Voltage $\leq 150V_{rms}$			I to IV	
For Rated Mains Voltage $\leq 300V_{rms}$			I to III	
For Rated Mains Voltage $\leq 400V_{rms}$			I to III	
Climatic Classification			10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive isolation voltage		VIORM	565	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$ , 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	847	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	678	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	678	Vpeak
Maximum transient isolation voltage	$t = 60$ sec	VIOTM	5300	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065, 1.2/50us waveform, $V_{TEST} = V_{IOSM} \times 1.3$	VIOSM	5384	Vpeak
Isolation resistance	$V_{IO} = 500V$	RIO	$>10^9$	$\Omega$
Isolation capacitance	$f = 1MHz$	CIO	0.6	pF
Input capacitance		CI	2	pF
Total Power Dissipation at 25°C		Ps		mW
Safety input, output, or supply current	$\theta_{JA} = 140$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C	Is	160	mA
	$\theta_{JA} = 84$ °C/W, $V_I = 5.5$ V, $T_J = 150$ °C, $T_A = 25$ °C			mA
Case Temperature		Ts	150	°C



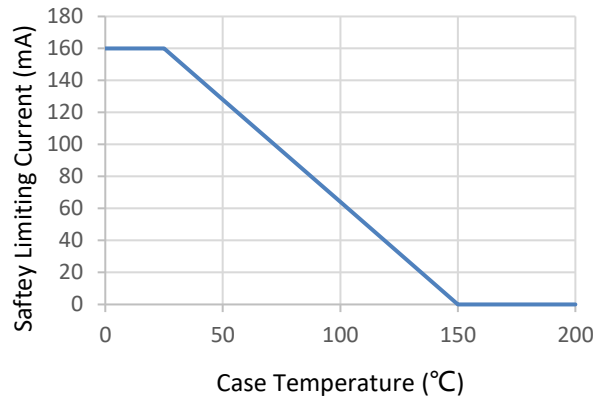


Figure 3.1 NSI8020N/NSI8021N/NSI8022N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

### 3.3. REGULATORY INFORMATION

The NSI8020N/NSI8021N are approved by the organizations listed in table.

	<i>CUL</i>	<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01 <sup>2</sup>	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000V <sub>rms</sub> Isolation voltage	Single Protection, 3000V <sub>rms</sub> Isolation voltage	Basic Insulation 565V <sub>peak</sub> , V <sub>IOSM</sub> =5384V <sub>peak</sub>	Basic insulation at 400V <sub>rms</sub> (565V <sub>peak</sub> )
File (E500602)	File (E500602)	File (5024579-4880-0001)	File (pending)

<sup>1</sup> In accordance with UL 1577, each NSI8020N/NSI8021N is proof tested by applying an insulation test voltage  $\geq 3600$  V<sub>rms</sub> for 1 sec.

<sup>2</sup> In accordance with DIN VDE V 0884-11, each NSI8020N/NSI8021N is proof tested by applying an insulation test voltage  $\geq 847$  V<sub>peak</sub> for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN VDE V 0884-11 approval.

## 4.0 FUNCTION DESCRIPTION

The NSI802x is a Dual-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSI802x devices are high reliability dual-channel digital isolator. The NSI802x device is safety certified by UL1577 support 3kV<sub>rms</sub> insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSI802x is up to 10Mbps, and the common-mode transient immunity (CMTI) is up to 100kV/us. The NSI802x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSI802x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSI802x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 4.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 1us after powering up.

# NSI8020/NSI8021

Table 4.1 Output status vs. power status

Input	VDD1 status	VDD2 status	Output	Comment
H	Ready	Ready	H	Normal operation.
L	Ready	Ready	L	
X	Unready	Ready	L(NSI802xN0) H(NSI802xN1)	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDD2 is powered on.

## 5.0 APPLICATION NOTE

### 5.1. PCB LAYOUT

The NSI802x requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 5.1 to Figure 5.4 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω ) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

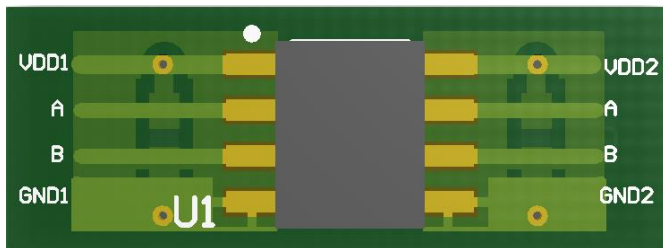


Figure 5.1 Recommended PCB Layout — Top Layer

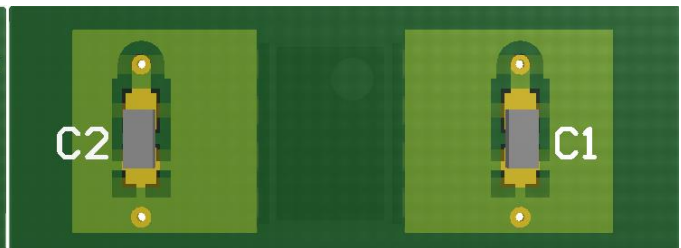


Figure 5.2 Recommended PCB Layout — Bottom Layer

## 6.0 PACKAGE INFORMATION

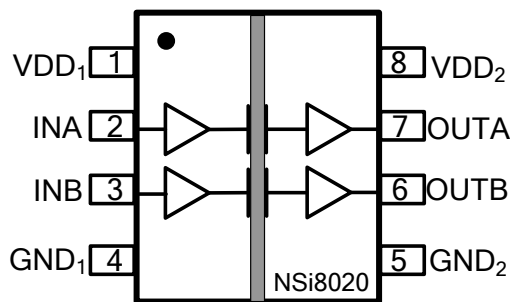


Figure 6.1 NSI8020N Package

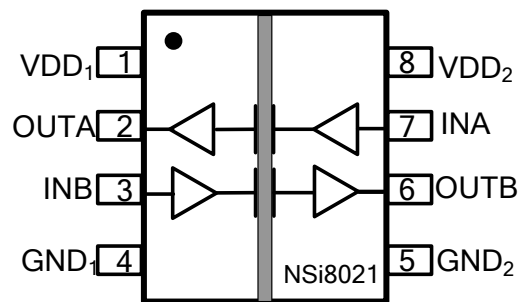


Figure 6.2 NSI8021N Package

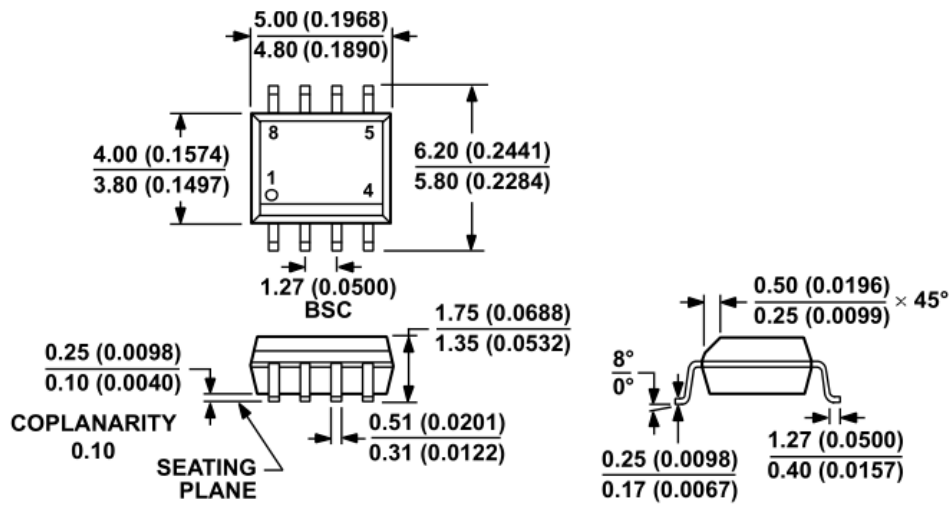
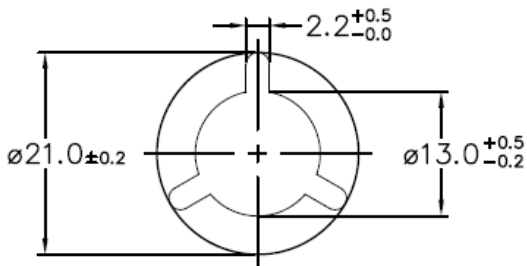
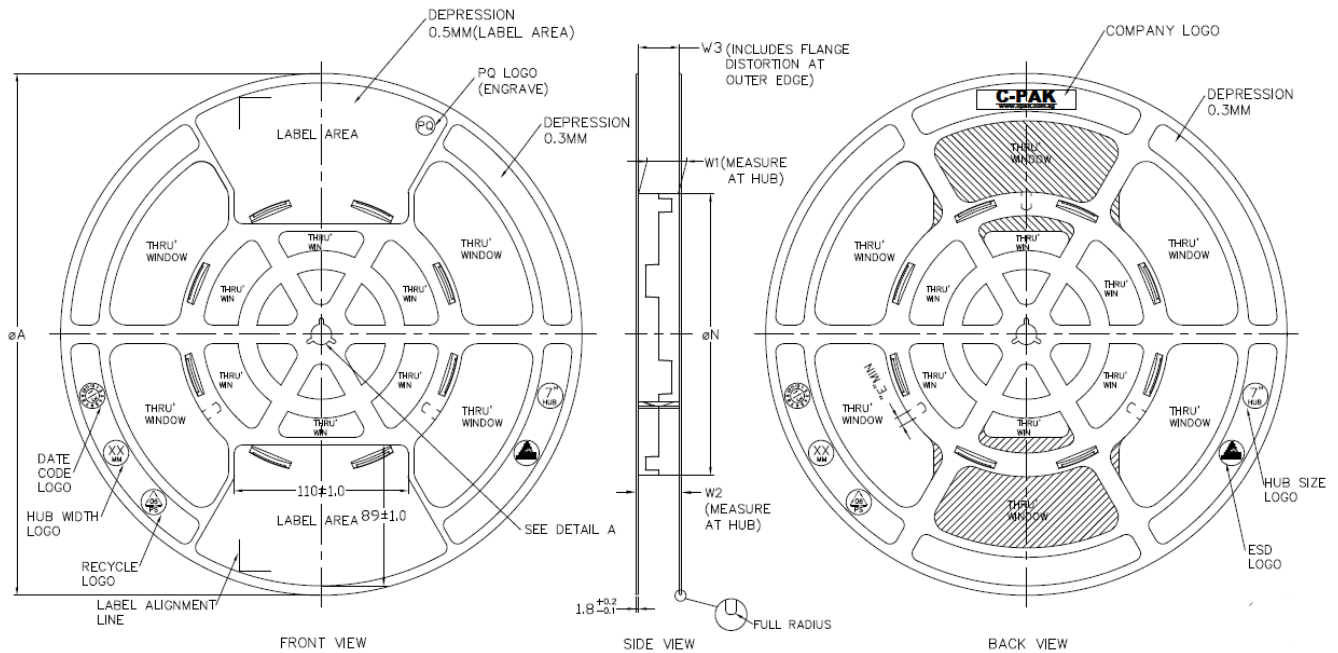


Figure 6.3 SOIC8 Package Shape and Dimension in millimeters (inches)

Table 6.1 NSI8020N/ NSI8021N Pin Configuration and Description

NSI8020N PIN NO.	NSI8021N PIN NO.	SYMBOL	FUNCTION
1	1	VDD1	Power Supply for Isolator Side 1
2	7	INA	Logic Input A
3	3	INB	Logic Input B
4	4	GND1	Ground 1, the ground reference for Isolator Side 1
5	5	GND2	Ground 2, the ground reference for Isolator Side 2
6	6	OUTB	Logic Output B
7	2	OUTA	Logic Output A
8	8	VDD2	Power Supply for Isolator Side 2

7.0 TAPE AND REEL INFORMATION



ARBOR HOLE  
DETAIL A  
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	$\phi A$ $\pm 2.0$	$\phi N$ $\pm 2.0$	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW $10^{12}$	ANTISTATIC	ALL TYPES
B	$10^8$ TO $10^{11}$	STATIC DISSIPATIVE	BLACK ONLY
C	$10^9$ & BELOW $10^9$	CONDUCTIVE (GENERIC)	BLACK ONLY
E	$10^8$ TO $10^{11}$	ANTISTATIC (COATED)	ALL TYPES

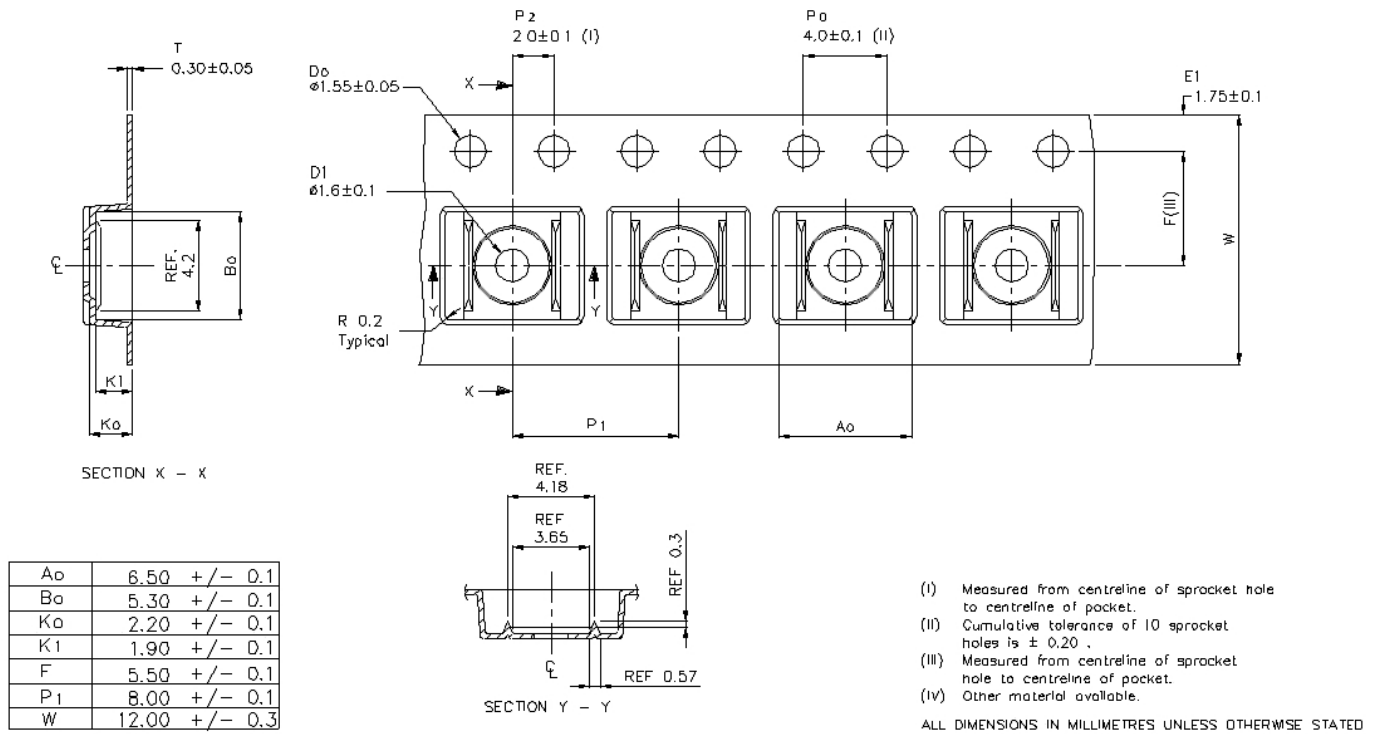


Figure 7.1 Tape and Reel Information of SOIC8

## 8.0 ORDER INFORMATION

### Part Number Rule:

Part No.	Isolation Rating(kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	SPQ	Package
NSI8020N0-DSPR	3	2	0	0.5	Low	-40 to 125°C	2500	SOIC8
NSI8020N1-DSPR	3	2	0	0.5	High	-40 to 125°C	2500	SOIC8
NSI8021N0-DSPR	3	1	1	0.5	Low	-40 to 125°C	2500	SOIC8
NSI8021N1-DSPR	3	1	1	0.5	High	-40 to 125°C	2500	SOIC8

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

## 9.0 REVISION HISTORY

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# NSI8020/NSI8021

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Revision	Description	Date
1.0	Original	2019/10/10

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