

Product Overview

The NSi824x devices are high reliability quad-channel digital isolators. The NSi824x device is safety certified by UL1577 support several insulations withstand voltages (3kVrms, 3.75kVrms, 5kVrms, 8kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi824x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 250kV/us. The NSi824x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi824x device supports to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- High CMTI: 250kV/us
- Chip level ESD: HBM: ±8kV
- Robust Electromagnetic Compatibility (EMC)
 - System-Level ESD, EFT, and Surge Immunity
 - Low Emissions
- Default output high level or low-level option
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -55°C~125°C
- RoHS-compliant packages:
 - SOP16(150mil)
 - SSOP16
 - SOP16(300mil)
 - SOP16(600mil)

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V0884-11:2017-01

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Device Information

| Part Number | Package | Body Size |
|----------------|---------------|------------------|
| NSi824xN-DSPNR | SOP16(150mil) | 9.90mm x 3.90mm |
| NSi824xS-DSSR | SSOP16 | 4.90mm x 3.90mm |
| NSi824xW-DSWR | SOP16(300mil) | 10.30mm x 7.50mm |
| NSi824xW-DSWWR | SOP16(600mil) | 10.52mm x 14.0mm |

Functional Block Diagrams

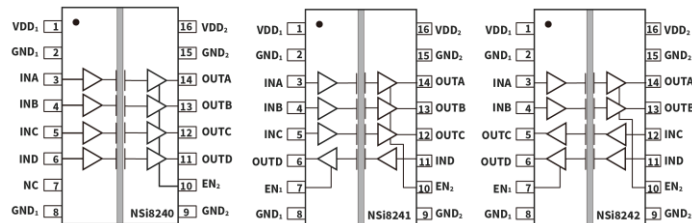


Figure 1. NSi824x Block Diagram

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1. Pin Configuration and Functions

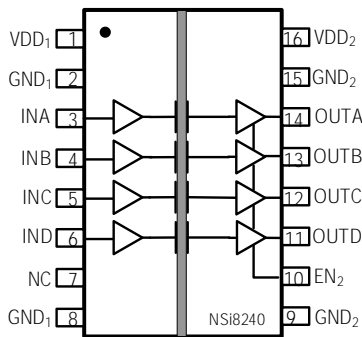


Figure 1.1 NSi8240 Package

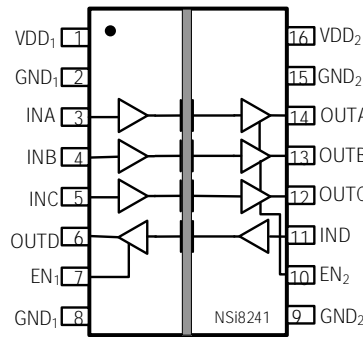


Figure 1.2 NSi8241 Package

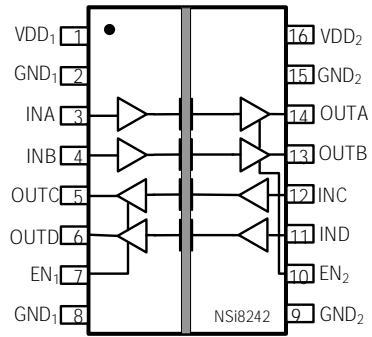


Figure 1.3 NSi8242 Package

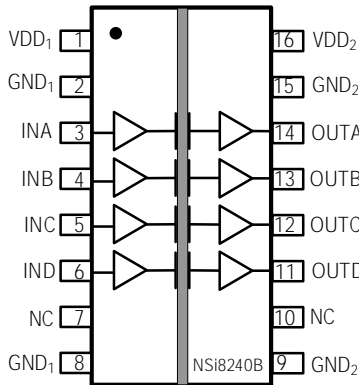


Figure 1.4 NSi8240B Package

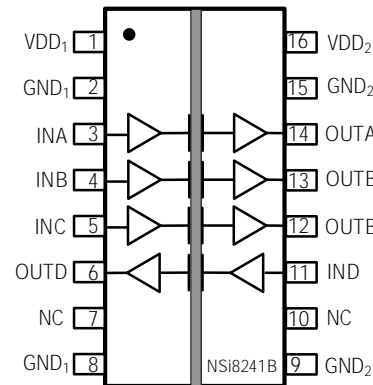


Figure 1.5 NSi8241B Package

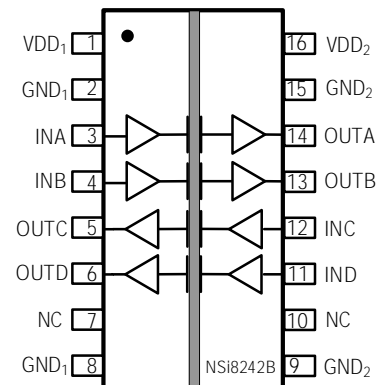


Figure 1.6 NSi8242B Package

Table 1.1 NSi824x Pin Configuration and Description

| NSi8240 PIN NO. | NSi8241 PIN NO. | NSi8242 PIN NO. | SYMBOL | FUNCTION |
|--------------------|--------------------|--------------------|-----------------------------------|---|
| 1 | 1 | 1 | VDD ₁ | Power Supply for Isolator Side 1 |
| 2 | 2 | 2 | GND ₁ | Ground 1, the ground reference for Isolator Side 1 |
| 3 | 3 | 3 | INA | Logic Input A |
| 4 | 4 | 4 | INB | Logic Input B |
| 5 | 5 | 12 | INC | Logic Input C |
| 6 | 11 | 11 | IND | Logic Input D |
| 7 | 7 | 7 | NC ¹ / EN ₁ | No Connection. Or Output Enable 1. Active high logic input. When EN ₁ is high or NC, the output of Side 1 is enabled. When EN ₁ is low, the output of Side 1 is disabled to high impedance state. |
| 8 | 8 | 8 | GND ₁ | Ground 1, the ground reference for Isolator Side 1 |

| | | | | |
|----|----|----|-----------------------------------|---|
| 9 | 9 | 9 | GND ₂ | Ground 2, the ground reference for Isolator Side 2 |
| 10 | 10 | 10 | NC ¹ / EN ₂ | No Connection. Or Output Enable 2. Active high logic input. When EN ₂ is high or NC, the output of Side 2 is enabled. When EN ₂ is low, the output of Side 2 is disabled to high impedance state. |
| 11 | 6 | 6 | OUTD | Logic Output D |
| 12 | 12 | 5 | OUTC | Logic Output C |
| 13 | 13 | 13 | OUTB | Logic Output B |
| 14 | 14 | 14 | OUTA | Logic Output A |
| 15 | 15 | 15 | GND2 | Ground 2, the ground reference for Isolator Side 2 |
| 16 | 16 | 16 | VDD2 | Power Supply for Isolator Side 2 |

1) For NSi824xB, EN1/EN2 are always high internally.

2. Absolute Maximum Ratings

| <i>Parameters</i> | <i>Symbol</i> | <i>Min</i> | <i>Typ</i> | <i>Max</i> | <i>Unit</i> | <i>Comments</i> |
|------------------------------------|--|------------|------------|------------|-------------|---|
| Power Supply Voltage | VDD1, VDD2 | -0.5 | | 6.5 | V | |
| Maximum Input Voltage | VINA, VINB, VINC, VIND | -0.4 | | VDD+0.4 | V | The maximum voltage must not exceed 6.5V |
| Maximum Output Voltage | VOUTA, VOUTB, VOUTC, VOUTD | -0.4 | | VDD+0.4 | V | The maximum voltage must not exceed 6.5V |
| Maximum Input/Output Pulse Voltage | VINA, VINB, VINC, VIND, VOUTA, VOUTB, VOUTC, VOUTD | -0.8 | | VDD+0.8 | V | Pulse width should be less than 100ns, and the duty cycle should be less than 10% |
| Output current | I _o | -15 | | 15 | mA | |
| Maximum Surge Isolation Voltage | V _{IOSM} | | | 6.25 | kV | |
| Operating Temperature | T _{opr} | -55 | | 125 | °C | |
| Junction Temperature | T _j | | | 150 | °C | |
| Storage Temperature | T _{stg} | -65 | | 150 | °C | |
| Electrostatic discharge | HBM | | | ±8000 | V | |
| | CDM | | | ±2000 | V | |

3. Recommended Operating Conditions

| <i>Parameters</i> | <i>Symbol</i> | <i>min</i> | <i>typ</i> | <i>max</i> | <i>unit</i> |
|--------------------------|------------------|------------|------------|------------|-------------|
| Power Supply Voltage | VDD1, VDD2 | 2.5 | | 5.5 | V |
| Operating Temperature | T _{opr} | -55 | | 125 | °C |
| High Level Input Voltage | V _{IH} | 2 | | | V |
| Low Level Input Voltage | V _{IL} | | | 0.8 | V |
| Data rate | DR | | | 150 | Mbps |

4. Thermal Information

| Parameters | Symbol | SOP16(150mil) | SSOP16 | SOP16(300mil) | SOP16(600mil) | Unit |
|---|---------------------|---------------|--------|---------------|---------------|------|
| IC Junction-to-Air Thermal Resistance | θ_{JA} | 78.9 | 140 | 78.9 | 78.9 | °C/W |
| Junction-to-case (top) thermal resistance | $\theta_{JC (top)}$ | 41.1 | 54.4 | 41.6 | 41.1 | °C/W |
| Junction-to-board thermal resistance | θ_{JB} | 49.5 | 51.9 | 43.6 | 49.5 | °C/W |

5. Specifications

5.1. Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|--------------------------------|--------------------|---------|------|-----|-------|---|
| Power on Reset | VDD _{POR} | | 2.2 | | V | POR threshold as during power-up |
| | VDD _{HYS} | | 0.1 | | V | POR threshold Hysteresis |
| High Level Input Voltage | V _{IH} | 2 | | | V | |
| Low Level Input Voltage | V _{IL} | | | 0.8 | V | |
| High Level Output Voltage | V _{OH} | VDD-0.4 | | | V | I _{OH} = -4mA |
| Low Level Output Voltage | V _{OL} | | | 0.4 | V | I _{OL} = 4mA |
| Output Impedance | R _{out} | | 50 | | ohm | |
| Input Pull high or low Current | I _{pull} | | 8 | 15 | uA | |
| Start Up Time after POR | tr _{bs} | | 10 | | us | |
| Common Mode Transient Immunity | CMTI | ±200 | ±250 | | kV/us | See Figure 5.11 , C _t = 15pF |

5.2. Supply Current Characteristics – 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|----------------|-------------------------|-----|-------|-------|------|---|
| Supply current | NSi8240 | | | | | |
| | I _{DD1} (Q0) | | 1.24 | 2.04 | mA | All Input 0V for NSi8240x0 Or All Input at supply for NSi8240x1 |
| | I _{DD2} (Q0) | | 2.94 | 4.84 | mA | |
| | I _{DD1} (Q1) | | 5.26 | 8.68 | mA | All Input at supply for NSi8240x0 Or All Input 0V for NSi8240x1 |
| | I _{DD2} (Q1) | | 3.02 | 4.98 | mA | |
| | I _{DD1} (1M) | | 3.4 | 5.1 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.78 | 4.39 | mA | |
| | I _{DD1} (10M) | | 3.56 | 5.34 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 4.26 | 6.68 | mA | |
| | I _{DD1} (100M) | | 4.98 | 7.47 | mA | All Input with 100Mbps, C _L =15pF |
| | I _{DD2} (100M) | | 18.44 | 38.12 | mA | |
| | NSi8241 | | | | | |
| | I _{DD1} (Q0) | | 1.66 | 2.74 | mA | All Input 0V for NSi8241x0 Or All Input at supply for NSi8241x1 |
| | I _{DD2} (Q0) | | 2.51 | 4.14 | mA | |
| | I _{DD1} (Q1) | | 4.70 | 7.76 | mA | All Input at supply for NSi8241x0 Or All Input 0V for NSi8241x1 |
| | I _{DD2} (Q1) | | 3.58 | 5.91 | mA | |
| | I _{DD1} (1M) | | 3.25 | 4.875 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.94 | 4.41 | mA | |
| | I _{DD1} (10M) | | 3.74 | 5.61 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 4.09 | 6.135 | mA | |
| | I _{DD1} (100M) | | 8.35 | 12.76 | mA | All Input with 100Mbps, C _L = 15pF |
| | I _{DD2} (100M) | | 15.08 | 29.67 | mA | |
| | NSi8242 | | | | | |
| | I _{DD1} (Q0) | | 2.09 | 3.44 | mA | All Input 0V for NSi8242x0 Or All Input at supply for NSi8242x1 |
| | I _{DD2} (Q0) | | 2.09 | 3.44 | mA | |
| | I _{DD1} (Q1) | | 4.14 | 6.83 | mA | All Input at supply for NSi8242x0 |

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|------------|-------------------------|-----|-------|-------|------|--|
| | I _{DD2} (Q1) | | 4.14 | 6.83 | mA | Or All Input 0V for NSi8242x1 |
| | I _{DD1} (1M) | | 3.09 | 4.635 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 3.09 | 4.635 | mA | |
| | I _{DD1} (10M) | | 3.91 | 5.865 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 3.91 | 5.865 | mA | |
| | I _{DD1} (100M) | | 11.71 | 21.22 | mA | All Input with 100Mbps, C _L = 15pF |
| | I _{DD2} (100M) | | 11.71 | 21.22 | mA | |

5.3. Supply Current Characteristics –3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|----------------|-------------------------|-----|-------|-------|------|---|
| Supply current | NSi8240 | | | | | |
| | I _{DD1} (Q0) | | 1.19 | 1.96 | mA | All Input 0V for NSi8240x0 Or All Input at supply for NSi8240x1 |
| | I _{DD2} (Q0) | | 2.87 | 4.74 | mA | |
| | I _{DD1} (Q1) | | 5.21 | 8.59 | mA | All Input at supply for NSi8240x0 Or All Input 0V for NSi8240x1 |
| | I _{DD2} (Q1) | | 2.95 | 4.86 | mA | |
| | I _{DD1} (1M) | | 3.32 | 4.98 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.62 | 4.22 | mA | |
| | I _{DD1} (10M) | | 3.42 | 5.13 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 3.60 | 5.72 | mA | |
| | I _{DD1} (100M) | | 4.40 | 6.6 | mA | All Input with 100Mbps, C _L =15pF |
| | I _{DD2} (100M) | | 13.00 | 25.73 | mA | |
| | NSi8241 | | | | | |
| | I _{DD1} (Q0) | | 1.61 | 2.66 | mA | All Input 0V for NSi8241x0 Or All Input at supply for NSi8241x1 |
| | I _{DD2} (Q0) | | 2.45 | 4.04 | mA | |
| | I _{DD1} (Q1) | | 4.64 | 7.66 | mA | All Input at supply for NSi8241x0 Or All Input 0V for NSi8241x1 |
| | I _{DD2} (Q1) | | 3.51 | 5.79 | mA | |
| | I _{DD1} (1M) | | 3.15 | 4.725 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.80 | 4.2 | mA | |

| Parameters | Symbol | Min | Typ | Max | Unit | Comments | |
|-------------------------|-------------------------|------|-------|-------|------|--|--|
| | I _{DD1} (10M) | | 3.47 | 5.205 | mA | All Input with 10Mbps, C _L =15pF | |
| | I _{DD2} (10M) | | 3.56 | 5.34 | mA | | |
| | I _{DD1} (100M) | | 6.55 | 9.825 | mA | All Input with 100Mbps, C _L = 15pF | |
| | I _{DD2} (100M) | | 10.85 | 20.31 | mA | | |
| | NSi8242 | | | | | | |
| | I _{DD1} (Q0) | | 2.03 | 3.35 | mA | All Input 0V for NSi8242x0 Or All Input at supply for NSi8242x1 | |
| | I _{DD2} (Q0) | | 2.03 | 3.35 | mA | | |
| | I _{DD1} (Q1) | | 4.08 | 6.72 | mA | All Input at supply for NSi8242x0 Or All Input 0V for NSi8242x1 | |
| | I _{DD2} (Q1) | | 4.08 | 6.72 | mA | | |
| | I _{DD1} (1M) | | 2.97 | 4.455 | mA | All Input with 1Mbps, C _L =15pF | |
| | I _{DD2} (1M) | | 2.97 | 4.455 | mA | | |
| | I _{DD1} (10M) | | 3.51 | 5.265 | mA | All Input with 10Mbps, C _L =15pF | |
| | I _{DD2} (10M) | | 3.51 | 5.265 | mA | | |
| | I _{DD1} (100M) | | 8.70 | 14.93 | mA | All Input with 100Mbps, C _L = 15pF | |
| I _{DD2} (100M) | | 8.70 | 14.93 | mA | | | |

5.4. Supply Current Characteristics–2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 2.5V, VDD2 = 2.5V, Ta = 25°C)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|----------------|-------------------------|-----|------|------|------|--|
| Supply current | NSi8240 | | | | | |
| | I _{DD1} (Q0) | | 1.17 | 1.92 | mA | All Input 0V for NSi8240x0 Or All Input at supply for NSi8240x1 |
| | I _{DD2} (Q0) | | 2.83 | 4.66 | mA | |
| | I _{DD1} (Q1) | | 5.13 | 8.46 | mA | All Input at supply for NSi8240x0 Or All Input 0V for NSi8240x1 |
| | I _{DD2} (Q1) | | 2.89 | 4.77 | mA | |
| | I _{DD1} (1M) | | 3.28 | 4.92 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.54 | 4.1 | mA | |
| | I _{DD1} (10M) | | 3.34 | 5.01 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 3.30 | 5.23 | mA | |
| | I _{DD1} (100M) | | 3.96 | 5.94 | mA | All Input with 100Mbps, |

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|----------------|-------------------------|-----|-------|-------|------|---|
| | I _{DD2} (100M) | | 10.44 | 20.15 | mA | C _L =15pF |
| NSi8241 | | | | | | |
| | I _{DD1} (Q0) | | 1.58 | 2.61 | mA | All Input 0V for NSi8241x0 Or All Input at supply for NSi8241x1 |
| | I _{DD2} (Q0) | | 2.41 | 3.98 | mA | |
| | I _{DD1} (Q1) | | 4.57 | 7.54 | mA | All Input at supply for NSi8241x0 Or All Input 0V for NSi8241x1 |
| | I _{DD2} (Q1) | | 3.45 | 5.69 | mA | |
| | I _{DD1} (1M) | | 3.10 | 4.65 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.73 | 4.095 | mA | |
| | I _{DD1} (10M) | | 3.33 | 4.995 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 3.31 | 4.965 | mA | |
| | I _{DD1} (100M) | | 5.58 | 8.37 | mA | All Input with 100Mbps, C _L = 15pF |
| | I _{DD2} (100M) | | 8.82 | 16.05 | mA | |
| NSi8242 | | | | | | |
| | I _{DD1} (Q0) | | 2.00 | 3.29 | mA | All Input 0V for NSi8242x0 Or All Input at supply for NSi8242x1 |
| | I _{DD2} (Q0) | | 2.00 | 3.29 | mA | |
| | I _{DD1} (Q1) | | 4.01 | 6.62 | mA | All Input at supply for NSi8242x0 Or All Input 0V for NSi8242x1 |
| | I _{DD2} (Q1) | | 4.01 | 6.62 | mA | |
| | I _{DD1} (1M) | | 2.91 | 4.365 | mA | All Input with 1Mbps, C _L =15pF |
| | I _{DD2} (1M) | | 2.91 | 4.365 | mA | |
| | I _{DD1} (10M) | | 3.32 | 4.98 | mA | All Input with 10Mbps, C _L =15pF |
| | I _{DD2} (10M) | | 3.32 | 4.98 | mA | |
| | I _{DD1} (100M) | | 7.20 | 12.21 | mA | All Input with 100Mbps, C _L = 15pF |
| | I _{DD2} (100M) | | 7.20 | 12.21 | mA | |

5.5. Switching Characteristics - 5V Supply

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V, Ta = 25°C**)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|--|----------------------|-----|------|-----|------|---|
| Data Rate | DR | 0 | | 150 | Mbps | |
| Minimum Pulse Width | PW | | | 5.0 | ns | |
| Propagation Delay | t _{PLH} | 2.5 | 6.54 | 15 | ns | See Figure 5.9 , C _L = 15pF |
| | t _{PHL} | 2.5 | 8.30 | 15 | ns | See Figure 5.9 , C _L = 15pF |
| Pulse Width Distortion t _{PHL} - t _{PLH} | PWD | | | 5.0 | ns | See Figure 5.9 , C _L = 15pF |
| Rising Time | t _r | | | 5.0 | ns | See Figure 5.9 , C _L = 15pF |
| Falling Time | t _f | | | 5.0 | ns | See Figure 5.9 , C _L = 15pF |
| Peak Eye Diagram Jitter | t _{JIT(PK)} | | 350 | | ps | |
| Channel-to-Channel Delay Skew | t _{SK(C2C)} | | | 2.5 | ns | |
| Part-to-Part Delay Skew | t _{SK(P2P)} | | | 5.0 | ns | |
| Disable high to Tri-State | t _{PHZ} | | 10.0 | 30 | ns | See Figure 5.10 , C _L = 15pF, R _L =1k |
| Enable to Data high Valid | t _{PZH} | | 8.3 | 30 | ns | See Figure 5.10 , C _L = 15pF, R _L =1k |
| Disable low to Tri-State | t _{PLZ} | | 10.2 | 30 | ns | See Figure 5.10 , C _L = 15pF, R _L =1k |
| Enable to Data high Valid | t _{PZL} | | 8.6 | 30 | ns | See Figure 5.10 , C _L = 15pF, R _L =1k |

5.6. Switching Characteristics - 3.3V Supply

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-55°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C**)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|--|------------------|-----|-----|-----|------|--|
| Data Rate | DR | 0 | | 150 | Mbps | |
| Minimum Pulse Width | PW | | | 5.0 | ns | |
| Propagation Delay | t _{PLH} | 2.5 | 7.5 | 15 | ns | See Figure 5.9 , C _L = 15pF |
| | t _{PHL} | 2.5 | 8.7 | 15 | ns | See Figure 5.9 , C _L = 15pF |
| Pulse Width Distortion t _{PHL} - t _{PLH} | PWD | | | 5.0 | ns | See Figure 5.9 , C _L = 15pF |
| Rising Time | t _r | | | 5.0 | ns | See Figure 5.9 , C _L = 15pF |

| | | | | | | |
|-------------------------------|-----------------------------|--|------|-----|----|---|
| Falling Time | t_f | | | 5.0 | ns | See Figure 5.9 , $C_L = 15\text{pF}$ |
| Peak Eye Diagram Jitter | $t_{\text{JIT}}(\text{PK})$ | | 350 | | ps | |
| Channel-to-Channel Delay Skew | $t_{\text{SK}}(\text{c2c})$ | | | 2.5 | ns | |
| Part-to-Part Delay Skew | $t_{\text{SK}}(\text{p2p})$ | | | 5.0 | ns | |
| Disable high to Tri-State | t_{PHZ} | | 11.6 | 30 | ns | See Figure 5.10 , $C_L = 15\text{pF}$, $R_i = 1\text{k}$ |
| Enable to Data high Valid | t_{PZH} | | 11.7 | 30 | ns | See Figure 5.10 , $C_L = 15\text{pF}$, $R_i = 1\text{k}$ |
| Disable low to Tri-State | t_{PLZ} | | 14.5 | 30 | ns | See Figure 5.10 , $C_L = 15\text{pF}$, $R_i = 1\text{k}$ |
| Enable to Data high Valid | t_{PZL} | | 11.8 | 30 | ns | See Figure 5.10 , $C_L = 15\text{pF}$, $R_i = 1\text{k}$ |

5.7. Switching Characteristics - 2.5V Supply

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V**, Ta = 25°C)

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|---|-----------------------------|-----|------|-----|------|---|
| Data Rate | DR | 0 | | 150 | Mbps | |
| Minimum Pulse Width | PW | | | 5.0 | ns | |
| Propagation Delay | t_{PLH} | 2.5 | 9.0 | 15 | ns | See Figure 5.9 , $C_L = 15\text{pF}$ |
| | t_{PHL} | 2.5 | 9.3 | 15 | ns | See Figure 5.9 , $C_L = 15\text{pF}$ |
| Pulse Width Distortion $ t_{\text{PHL}} - t_{\text{PLH}} $ | PWD | | | 5.0 | ns | See Figure 5.9 , $C_L = 15\text{pF}$ |
| Rising Time | t_r | | | 5.0 | ns | See Figure 5.9 , $C_L = 15\text{pF}$ |
| Falling Time | t_f | | | 5.0 | ns | See Figure 5.9 , $C_L = 15\text{pF}$ |
| Peak Eye Diagram Jitter | $t_{\text{JIT}}(\text{PK})$ | | 350 | | ps | |
| Channel-to-Channel Delay Skew | $t_{\text{SK}}(\text{c2c})$ | | | 2.5 | ns | |
| Part-to-Part Delay Skew | $t_{\text{SK}}(\text{p2p})$ | | | 5.0 | ns | |
| Disable high to Tri-State | t_{PHZ} | | 12.2 | 30 | ns | See Figure 5.10 , $C_L = 15\text{pF}$, $R_i = 1\text{k}$ |
| Enable to Data high Valid | t_{PZH} | | 17.0 | 30 | ns | See Figure 5.10 , $C_L = 15\text{pF}$, $R_i = 1\text{k}$ |
| Disable low to Tri-State | t_{PLZ} | | 17.2 | 30 | ns | See Figure 5.10 , $C_L = 15\text{pF}$, $R_i = 1\text{k}$ |
| Enable to Data high Valid | t_{PZL} | | 17.8 | 30 | ns | See Figure 5.10 , $C_L = 15\text{pF}$, $R_i = 1\text{k}$ |

5.8. Typical Performance Characteristics

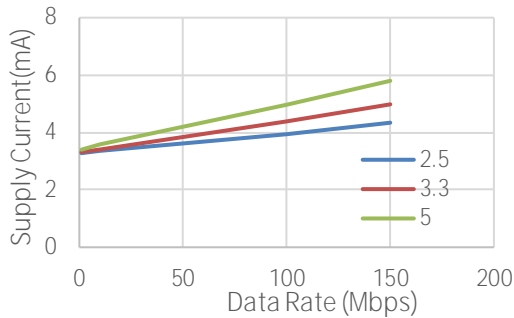


Figure 5.1 NSi8240 VDD1 Supply Current vs Data Rate

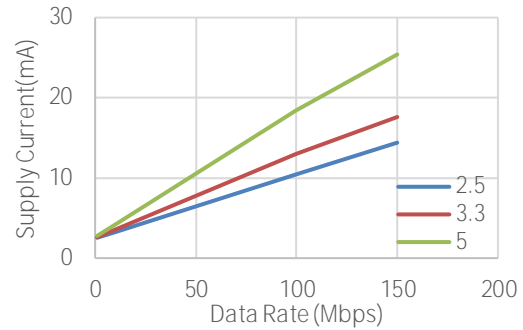


Figure 5.2 NSi8240 VDD2 Supply Current vs Data Rate

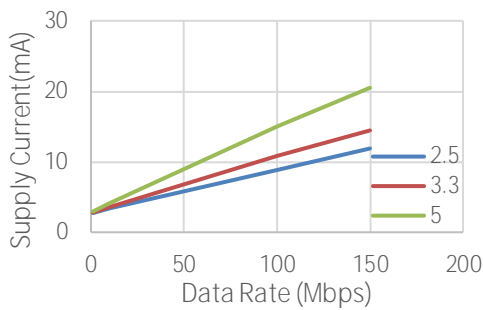


Figure 5.3 NSi8241 VDD1 Supply Current vs Data Rate

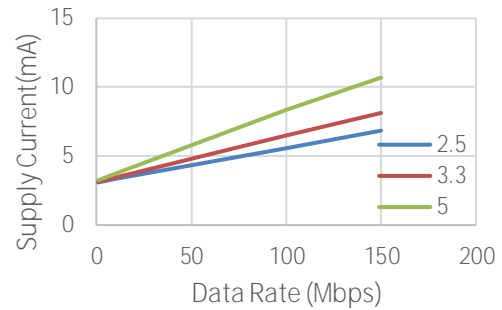


Figure 5.4 NSi8241 VDD2 Supply Current vs Data Rate

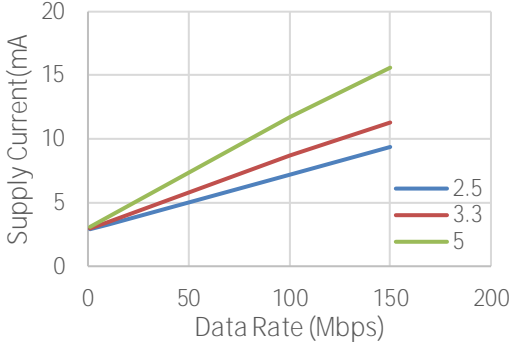


Figure 5.5 NSi8242 VDD1 Supply Current vs Data Rate

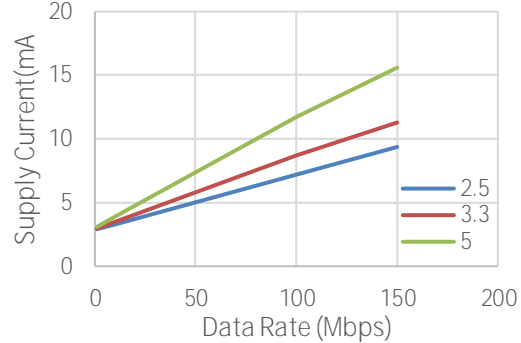


Figure 5.6 NSi8242 VDD2 Supply Current vs Data Rate

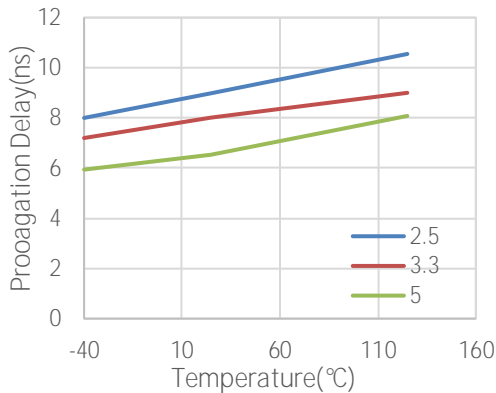


Figure 5.7 Rising Edge Propagation Delay Vs Temp

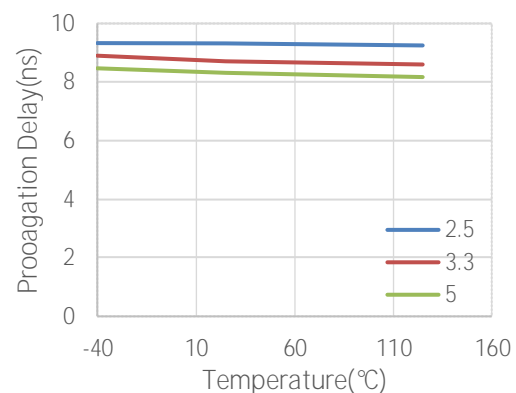


Figure 5.8 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information

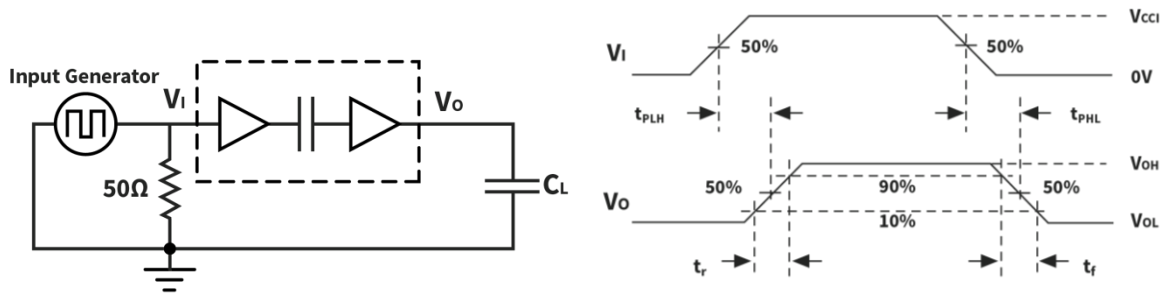


Figure 5.9 Switching Characteristics Test Circuit and Waveform

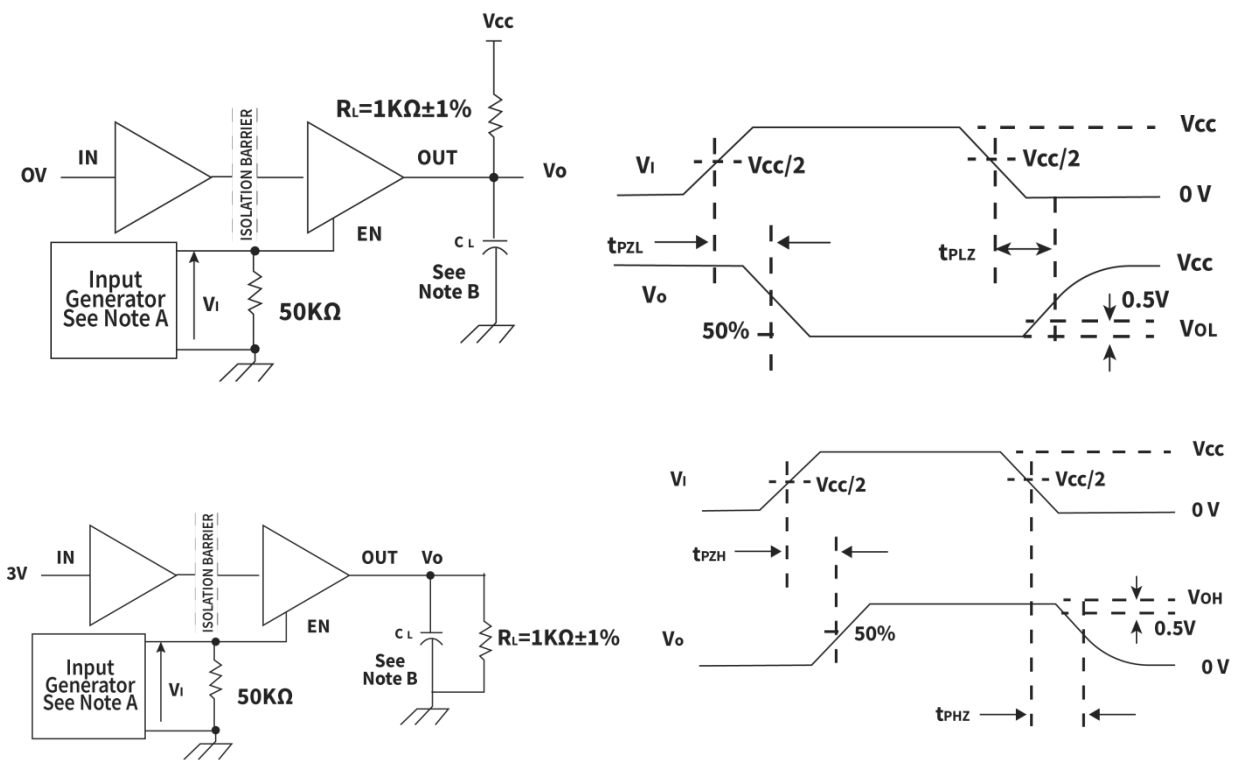


Figure 5.10 Enable/Disable Propagation Delay Time Test Circuit and Waveform

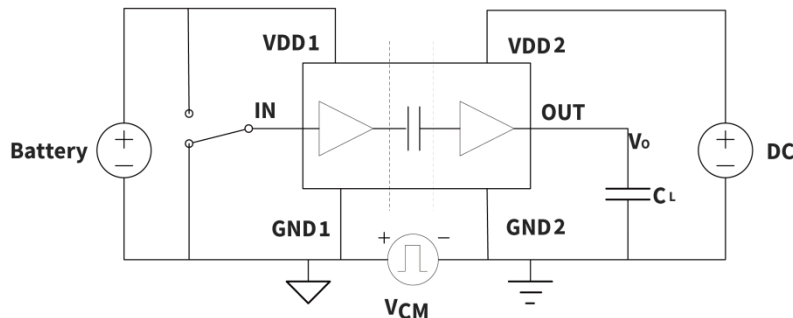


Figure 5.11 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

| Description | Test Condition | Symbol | Value | | | | Unit |
|--|--|-------------|-------------------|-------------------|----------|-------------------|------------|
| | | | SOP16 (300mil) | SOP16 (600mil) | SSOP16 | SOP16 (150mil) | |
| Min. External Air Gap (Clearance) | | CLR | 8 | 15 | 3.9 | 4.0 | mm |
| Min. External Tracking (Creepage) | | CPG | 8 | 15 | 3.9 | 4.0 | mm |
| Distance through the Insulation | | DTI | 28 | | | | um |
| Comparative Tracking Index | DIN EN 60112 (VDE 0303-11) | CTI | >600 | | >400 | >400 | V |
| Material Group | IEC 60112 | | I | | II | II | |
| Installation Classification per DIN VDE 0110 | | | | | | | |
| For Rated Mains Voltage ≤ 150Vrms | | | I to IV | I to IV | I to IV | I to IV | |
| For Rated Mains Voltage ≤ 300Vrms | | | I to IV | I to IV | I to III | I to III | |
| For Rated Mains Voltage ≤ 600Vrms | | | I to IV | I to IV | I to II | I to II | |
| For Rated Mains Voltage ≤ 1000Vrms | | | I to III | I to IV | I | I to II | |
| Insulation Specification per DIN VDE V 0884-11:2017-01 ¹⁾ | | | | | | | |
| Climatic Category | | | 40/125/21 | | | | |
| Pollution Degree | per DIN VDE 0110, Table 1 | | 2 | | | | |
| Maximum Working Isolation Voltage | AC voltage | V_{IOWM} | 1500 | 1500 | 400 | 400 | V_{RMS} |
| | DC voltage | | 2121 | 2121 | 565 | 565 | V_{DC} |
| Maximum Repetitive Isolation Voltage | | V_{IORM} | 2121 | 2121 | 565 | 565 | V_{peak} |
| Input to Output Test Voltage, Method B1 | $V_{ini.b} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.875$, $t_{ini} = t_m = 1 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$, 100% production test | $V_{pd(m)}$ | 3977 | 3977 | / | / | V_{peak} |
| | $V_{ini.b} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.5$, $t_{ini} = t_m = 1 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$, 100% production test | $V_{pd(m)}$ | / | / | 847 | 847 | V_{peak} |
| Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1 | $V_{ini.a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.6$, $t_{ini} = 60 \text{ sec}$, $t_m = 10 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$ | $V_{pd(m)}$ | 3394 | 3394 | / | / | V_{peak} |
| | $V_{ini.a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.2$, | $V_{pd(m)}$ | / | / | 678 | 678 | V_{peak} |

| Description | Test Condition | Symbol | Value | | | | Unit |
|--|--|-------------|------------|-------|------|------|------------|
| | $t_{ini} = 60 \text{ sec}, t_m = 10 \text{ sec}, q_{pd} \leq 5 \text{ pC}$ | | | | | | |
| Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3 | $V_{ini.a} = V_{IOTM}, V_{pd(m)} = V_{IORM} \times 1.2,$ $t_{ini} = 60 \text{ sec}, t_m = 10 \text{ sec}, q_{pd} \leq 5 \text{ pC}$ | $V_{pd(m)}$ | 2545 | 2545 | 678 | 678 | V_{peak} |
| Maximum Transient Isolation Voltage | $t = 60 \text{ sec}$ | V_{IOTM} | 8000 | 12000 | 5000 | 6500 | V_{peak} |
| Maximum Surge Isolation Voltage | Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ | V_{IOSM} | 6250 | 6250 | / | / | V_{peak} |
| | Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ | V_{IOSM} | / | / | 5384 | 5384 | V_{peak} |
| Isolation Resistance | $V_{IO} = 500 \text{ V}, T_{amb} = T_S$ | R_{IO} | $>10^9$ | | | | Ω |
| | $V_{IO} = 500 \text{ V}, 100^\circ\text{C} \leq T_{amb} \leq 125^\circ\text{C}$ | | $>10^{11}$ | | | | Ω |
| Isolation Capacitance | $f = 1\text{MHz}$ | C_{IO} | 1.2 | | | | pF |
| Insulation Specification per UL1577 | | | | | | | |
| Withstand Isolation Voltage | $V_{TEST} = 1.2 \times V_{ISO}, t = 1 \text{ sec},$ 100% production test | V_{ISO} | 5000 | 8000 | 3000 | 3750 | V_{rms} |

1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSi824x-DSWxR (SOP16(300mil)/SOP16(600mil))

| Description | Test Condition | Value | Unit |
|----------------------------------|--|-------|------|
| Safety Supply Power | $R_{\theta JA} = 78.9^\circ\text{C}/\text{W}^{1)}, T_J = 150^\circ\text{C}, T_A = 25^\circ\text{C}$ | 1584 | mW |
| Safety Supply Current | $R_{\theta JA} = 78.9^\circ\text{C}/\text{W}^{1)}, V_I = 5\text{V}, T_J = 150^\circ\text{C}, T_A = 25^\circ\text{C}$ | 316.8 | mA |
| Safety Temperature ²⁾ | | 150 | °C |

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(300mil)/SOP16(600mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

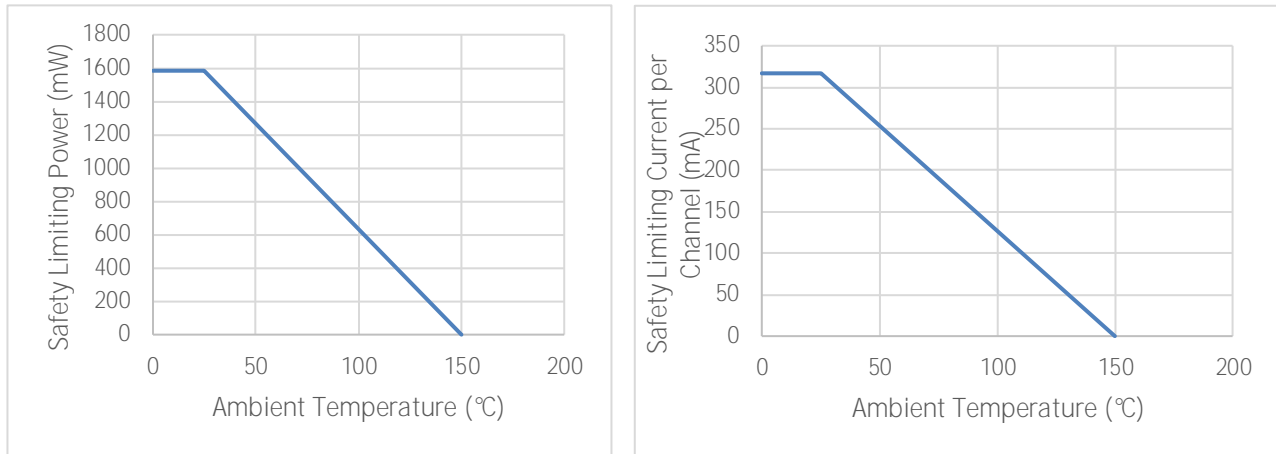


Figure 6.1 NSi824x Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi824x-DSSR (SSOP16)

| Description | Test Condition | Value | Unit |
|----------------------------------|--|-------|--------------------|
| Safety Supply Power | $R_{\theta JA} = 140^{\circ}\text{C}/\text{W}^{1)}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$ | 880 | mW |
| Safety Supply Current | $R_{\theta JA} = 140^{\circ}\text{C}/\text{W}^{1)}$, $V_I = 5\text{V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$ | 176 | mA |
| Safety Temperature ²⁾ | | 150 | $^{\circ}\text{C}$ |

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SSOP16 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

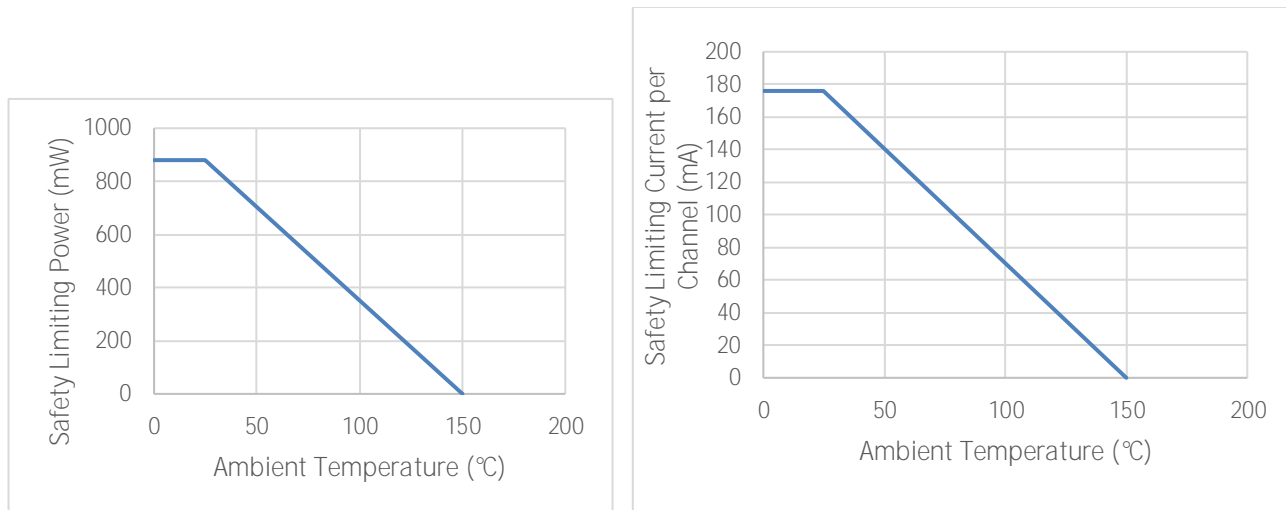


Figure 6.2 NSi824xS Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSi824x-DSPNR (SOP16(150mil))

| Description | Test Condition | Value | Unit |
|----------------------------------|---|-------|--------------------|
| Safety Supply Power | $R_{\theta JA} = 78.9^{\circ}\text{C}/\text{W}^{1)}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$ | 1584 | mW |
| Safety Supply Current | $R_{\theta JA} = 78.9^{\circ}\text{C}/\text{W}^{1)}$, $V_I = 5\text{V}$, $T_J = 150^{\circ}\text{C}$, $T_A = 25^{\circ}\text{C}$ | 316 | mA |
| Safety Temperature ²⁾ | | 150 | $^{\circ}\text{C}$ |

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16(150mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

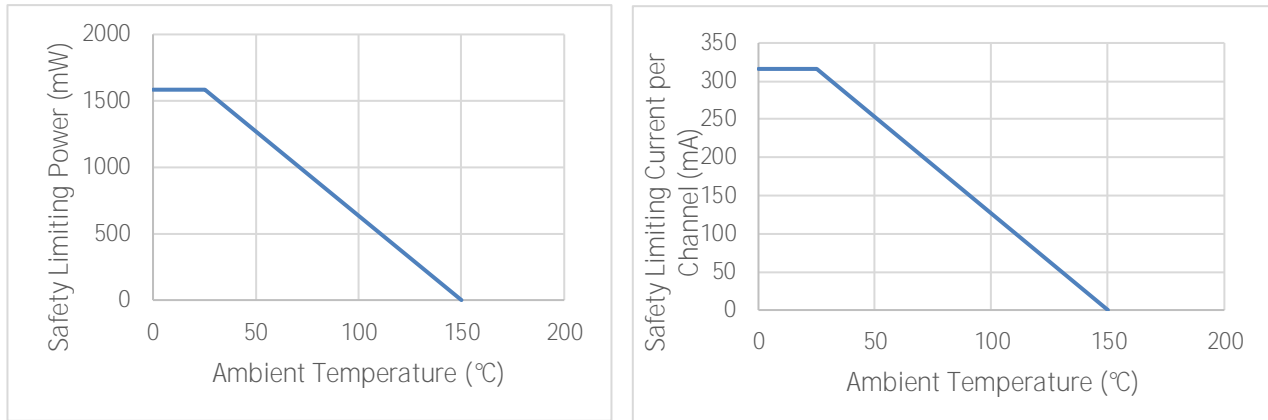


Figure 6.3 NSi824xN Thermal derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSi824xW-DSWR are approved or pending approval by the organizations listed in table.

| CUL | | VDE | CQC |
|---|---|--|---|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | DIN VDE V 0884-11(VDE V 0884-11):2017-01 | Certified by CQC11-471543-2012 GB4943.1-2011 |
| Single Protection, 5000V _{rms} Isolation voltage | Single Protection, 5000V _{rms} Isolation voltage | Reinforce Insulation 2121V _{peak} , V _{IOSM} =6250V _{peak} | Reinforced insulation |
| File (E500602) | File (E500602) | File (40052820) | File (CQC20001264939) |

The NSi824xW-DSWWR are approved or pending approval by the organizations listed in table.

| <i>CUL</i> | | <i>VDE</i> | <i>CQC</i> |
|---|---|---|---|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | DIN VDE V 0884-11(VDE V 0884-11):2017-01 | Certified by CQC11-471543-2012 GB4943.1-2011 |
| Single Protection, 8000V _{rms} Isolation voltage | Single Protection, 8000V _{rms} Isolation voltage | Reinforce Insulation 2121V _{peak} , V _{IOSM} =6250V _{peak} | Reinforced insulation |
| File (pending) | File (pending) | File (pending) | File (pending) |

The NSi824xS-DSSR are approved or pending approval by the organizations listed in table.

| <i>CUL</i> | | <i>VDE</i> | <i>CQC</i> |
|---|---|--|---|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | DIN VDE V 0884-11(VDE V 0884-11):2017-01 | Certified by CQC11-471543-2012 GB4943.1-2011 |
| Single Protection, 3000V _{rms} Isolation voltage | Single Protection, 3000V _{rms} Isolation voltage | Basic Insulation 565V _{peak} , V _{IOSM} =5384V _{peak} | Basic insulation |
| File (E500602) | File (pending) | File (pending) | File (pending) |

The NSi824xN-DSPNR are approved or pending approval by the organizations listed in table.

| <i>CUL</i> | | <i>VDE</i> | <i>CQC</i> |
|---|---|--|---|
| UL 1577 Component Recognition Program | Approved under CSA Component Acceptance Notice 5A | DIN VDE V 0884-11(VDE V 0884-11):2017-01 | Certified by CQC11-471543-2012 GB4943.1-2011 |
| Single Protection, 3750V _{rms} Isolation voltage | Single Protection, 3750V _{rms} Isolation voltage | Basic Insulation 565V _{peak} , V _{IOSM} =5384V _{peak} | Basic insulation |
| File (pending) | File (pending) | File (pending) | File (pending) |

7. Function Description

7.1. Overview

The NSi824x is a Quad-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi824x devices are high reliability quad-channel digital isolator. The NSi824x device is safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi824x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The NSi824x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi824x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi824x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A after powering up.

Table 7.1 Output status vs. power status

| Input | EN_x | VDD1 status | VDD2 status | Output | Comment |
|--|-----------------------|--------------------|--------------------|------------------------------|---|
| H | H or NC | Ready | Ready | H | Normal operation. |
| L | H or NC | Ready | Ready | L | |
| X | L | Ready | Ready | Z | Output Disabled, the output is high impedance |
| X | H or NC | Unready | Ready | L(NSi824xx0) H(NSi824xx1) | The output follows the same status with the input after input side VDD1 is powered on. |
| X | L | Unready | Ready | Z | Output Disabled, the output is high impedance |
| X | X | Ready | Unready | X | The output follows the same status with the input after output side VDD2 is powered on. |
| Note: H=Logic high; L=Logic low; X=Logic low or logic high VDD1 is input side power; VDD2 is outside power. | | | | | |

7.2. OOK Modulation

NSi824x is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 7.1 to Figure 7.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

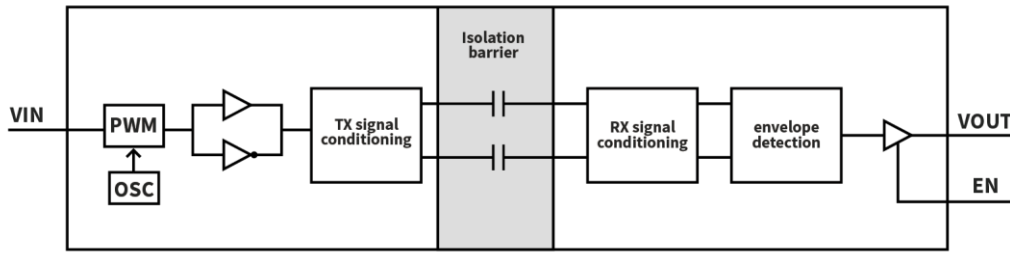


Figure 7.1 Single Channel Function Block Diagram

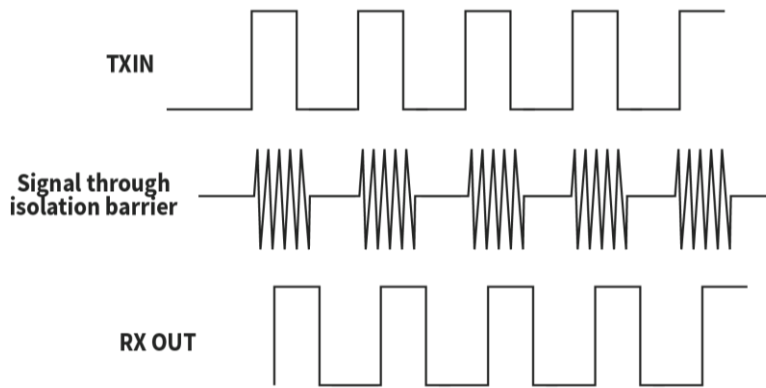


Figure 7.2 OOK Modulation

8. Application Note

8.1. Typical Application Circuit

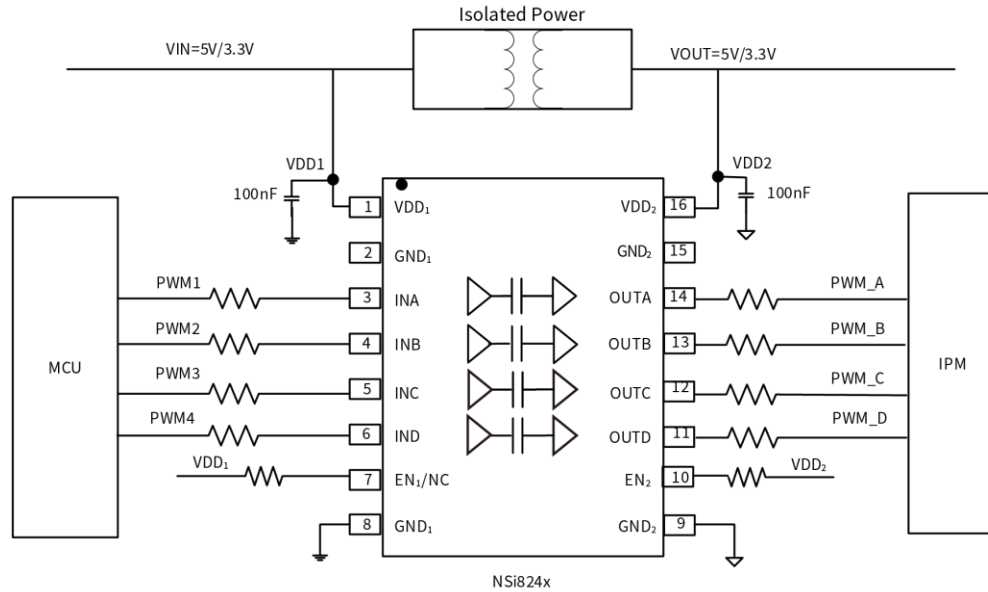


Figure 8.1 Typical PWM isolation circuit for IPM

8.2. PCB Layout

The NSi824x requires a 0.1 μ F bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω , $\pm 40\%$. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

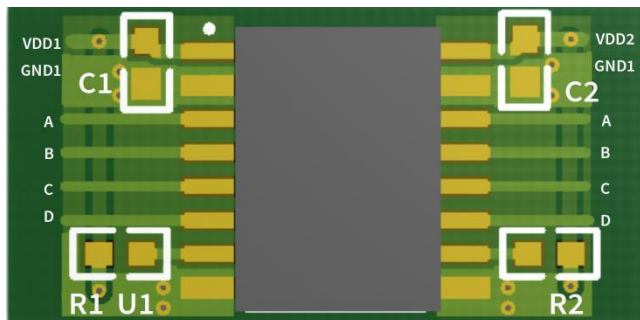


Figure8.2 Recommended PCB Layout — Top Layer



Figure8.3 Recommended PCB Layout — Bottom Layer

8.3. High Speed Performance

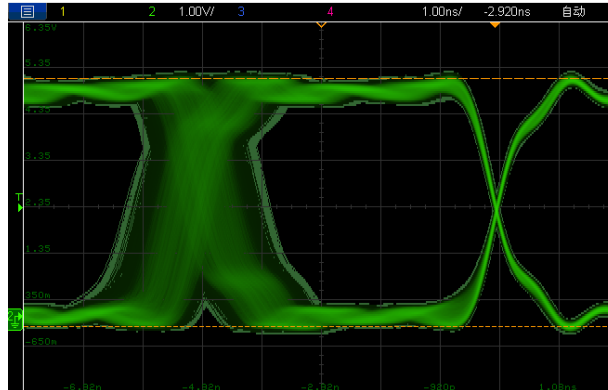


Figure8.4 Eye Diagram

8.4. Typical Supply Current Equations

The typical supply current of NSi824x can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF.

NSi8240:

$$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$$

$$I_{DD2} = 1.36 + VDD2 * f * C_L * c1 * 10^{-9}$$

When $a1$ is the channel number of default state input at side 1, $b1$ is the channel number of non-default state input at side 1, $c1$ is the channel number of switch signal input at side 1.

NSi8241:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$$

When $b1$ is the channel number of non-default state input at side 1, $c1$ is the channel number of switch signal input at side 1, $b2$ is the channel number of non-default state input at side 2, $c2$ is the channel number of switch signal input at side 2.

NSi8242:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD2 * f * C_L * c1 * 10^{-9}$$

When $b1$ is the channel number of non-default state input at side 1, $c1$ is the channel number of switch signal input at side 1, $b2$ is the channel number of non-default state input at side 2, $c2$ is the channel number of switch signal input at side 2.

9. Package Information

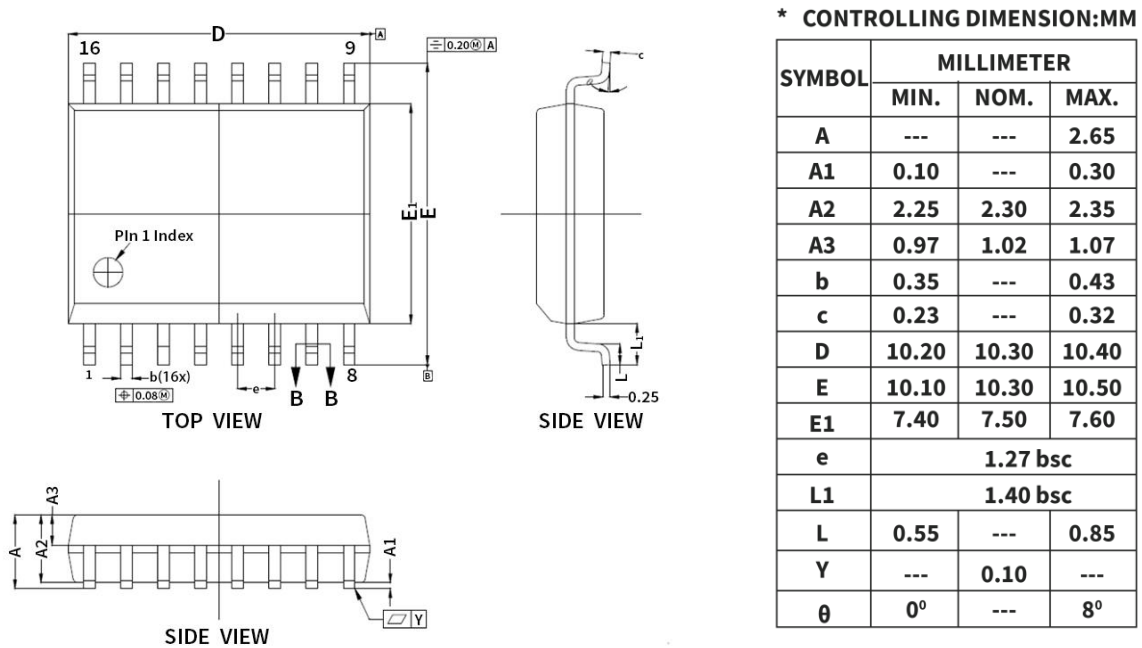


Figure 9.1 SOP16(300mil)/SOW16 Package Shape and Dimension in millimeters

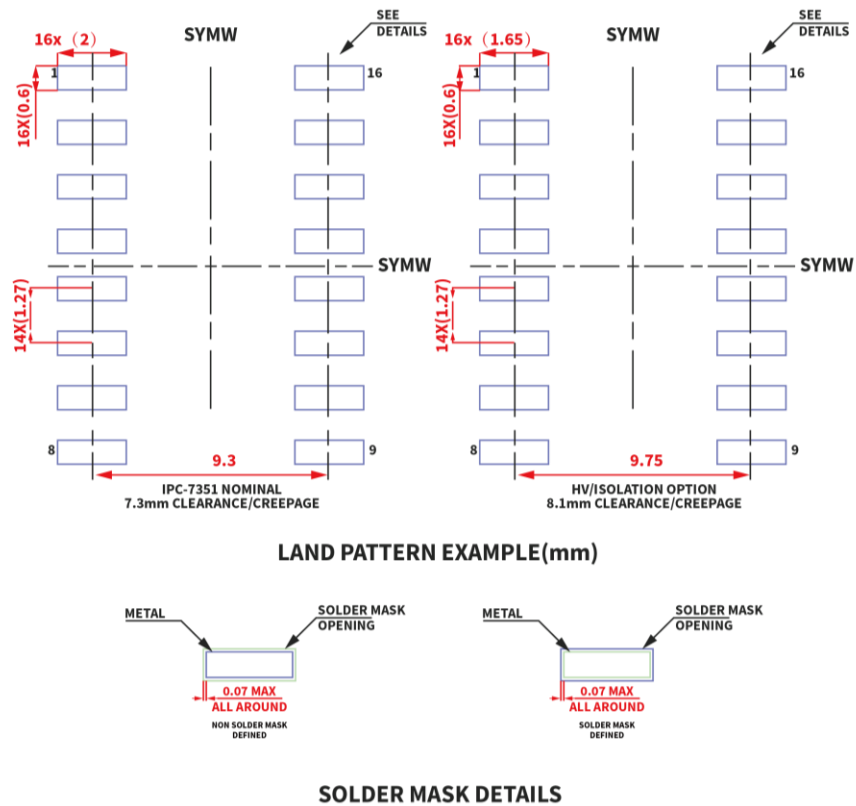


Figure 9.2 SOP16(300mil) SOW16 Package Board Layout Example

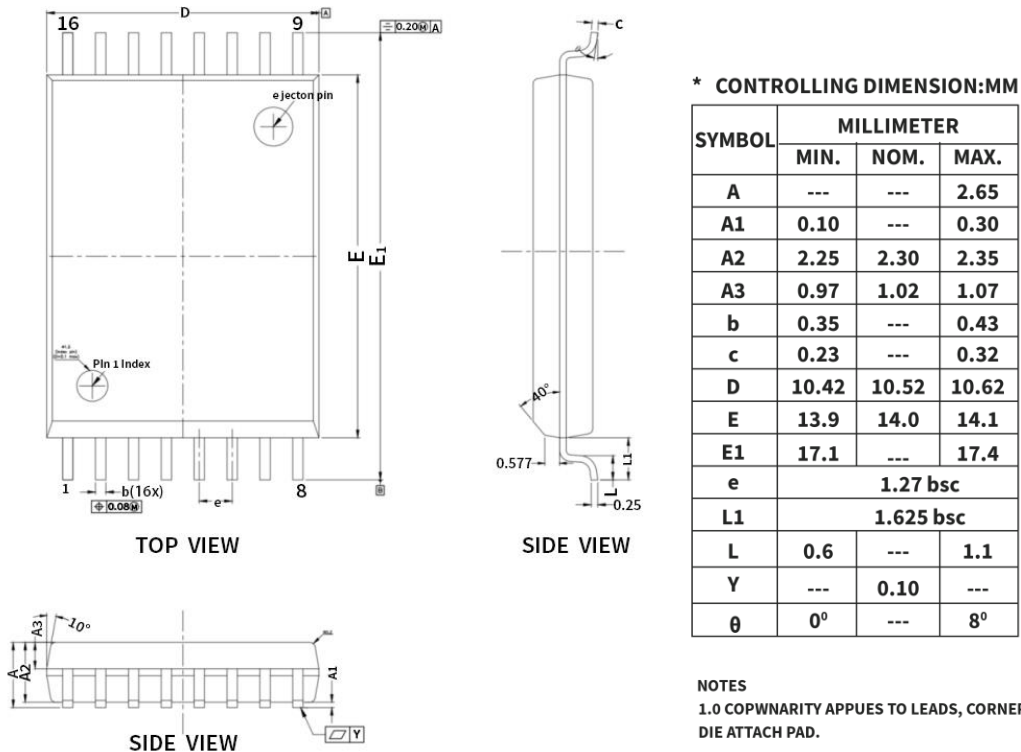


Figure 9.3 SOP16(600mil)/SOWW16 Package Shape and Dimension in millimeters

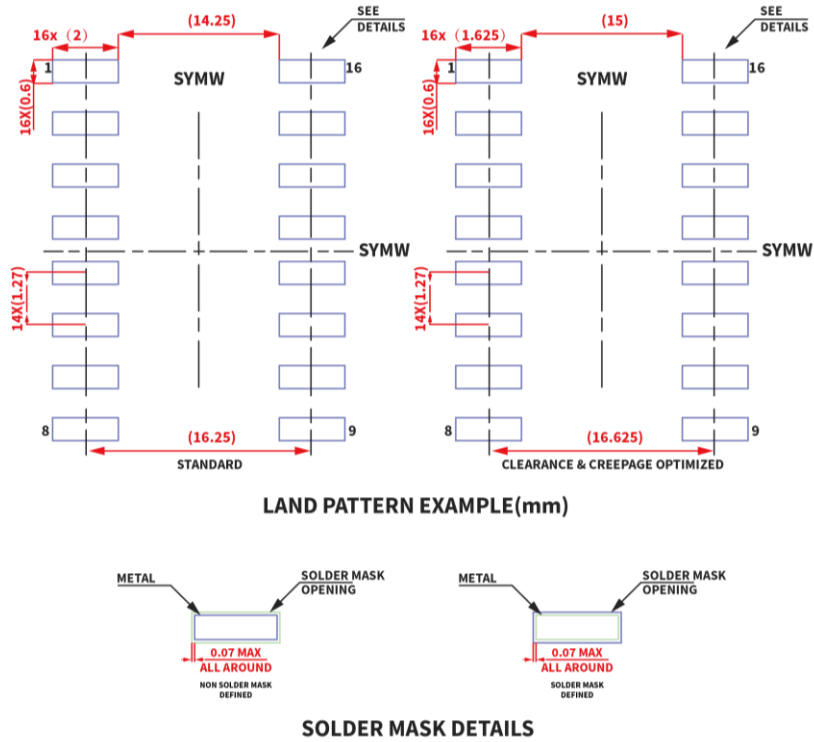
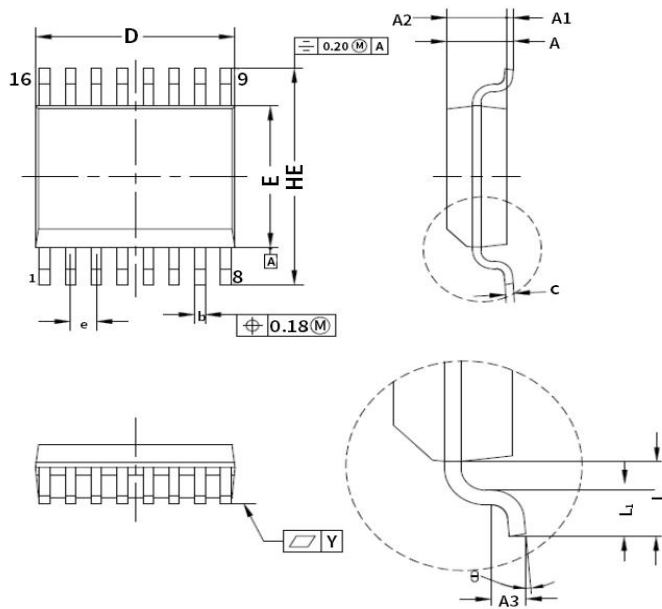


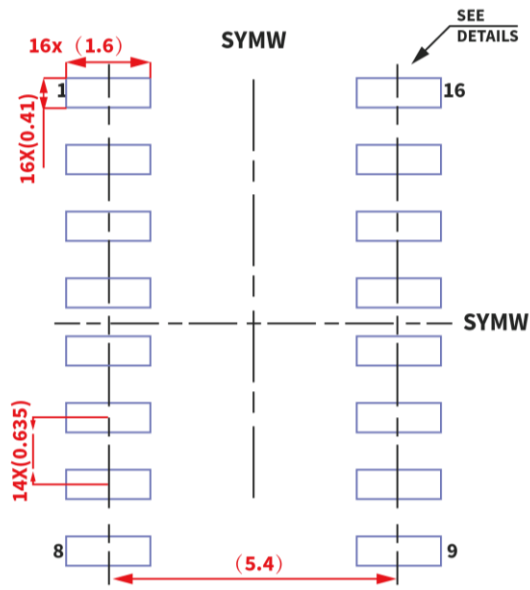
Figure 9.4 SOP16(600mil)/SOWW16 Package Board Layout Example



* CONTROLLING DIMENSION:MM

| SYMBOL | MILLIMETER | | | INCH | | |
|--------|------------|------|------|-----------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | --- | --- | 1.73 | --- | --- | 0.068 |
| A1 | 0.10 | --- | 0.25 | 0.004 | --- | 0.010 |
| A2 | 1.40 | --- | 1.55 | 0.055 | --- | 0.061 |
| b | 0.20 | --- | 0.31 | 0.008 | --- | 0.012 |
| c | 0.18 | --- | 0.25 | 0.007 | --- | 0.010 |
| D | 4.80 | --- | 5.00 | 0.189 | --- | 0.197 |
| E | 3.80 | --- | 4.00 | 0.150 | --- | 0.157 |
| HE | 5.80 | --- | 6.20 | 0.228 | --- | 0.244 |
| e | 0.635 bsc | | | 0.025 bsc | | |
| L | 1.00 bsc | | | 0.039 bsc | | |
| L1 | 0.41 | --- | 0.89 | 0.016 | --- | 0.035 |
| Y | --- | 0.09 | --- | --- | 0.004 | --- |
| A3 | --- | 0.25 | --- | --- | 0.010 | --- |
| θ | 0° | --- | 8° | 0° | --- | 8° |

Figure 9.5 SSOP16 Package Shape and Dimension in millimeters



LAND PATTERN EXAMPLE(mm)



Figure 9.6 SSOP16 Package Board Layout Example

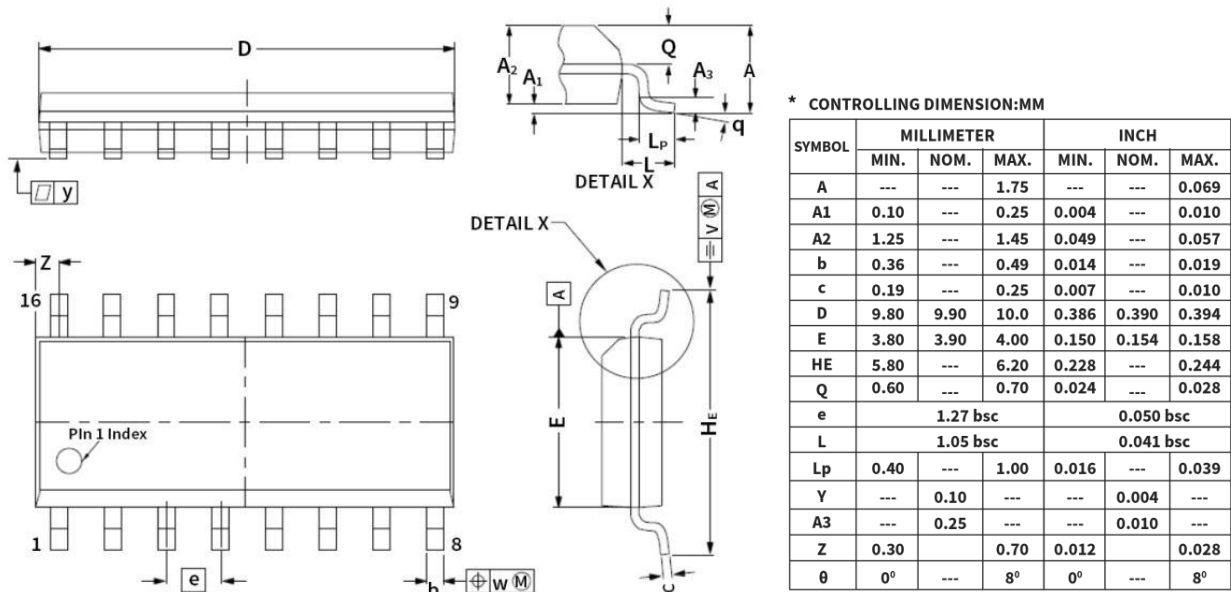


Figure 9.7 SOP16(150mil) Package Shape and Dimension in millimeters

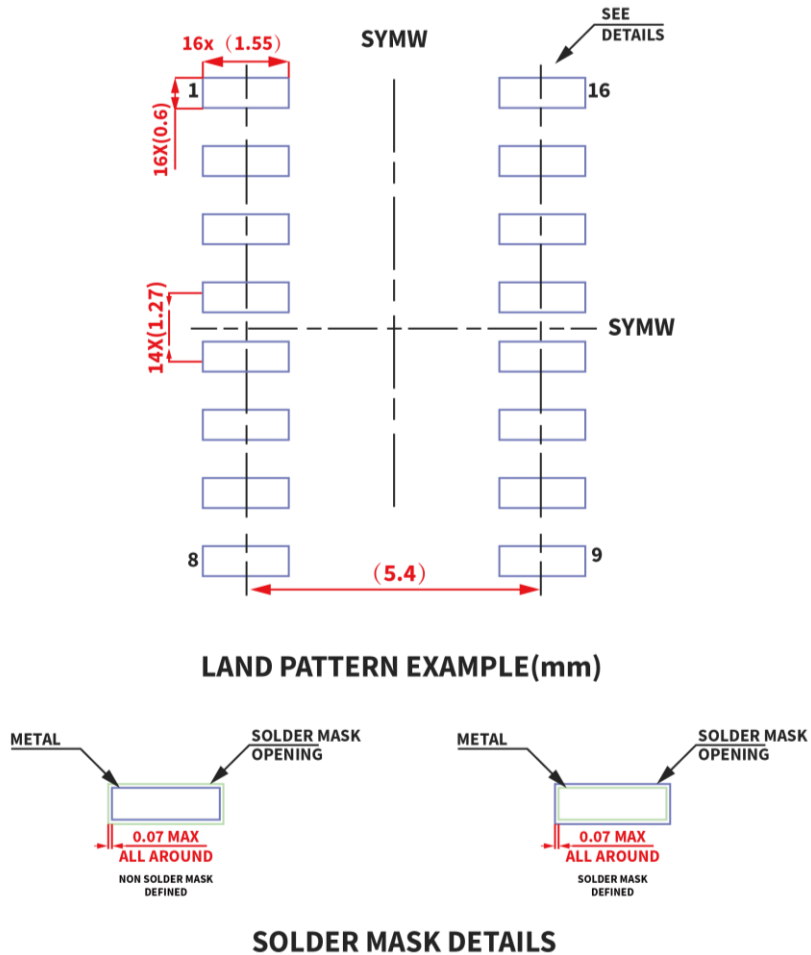


Figure 9.8 SOP16(150mil) Package Board Layout Example

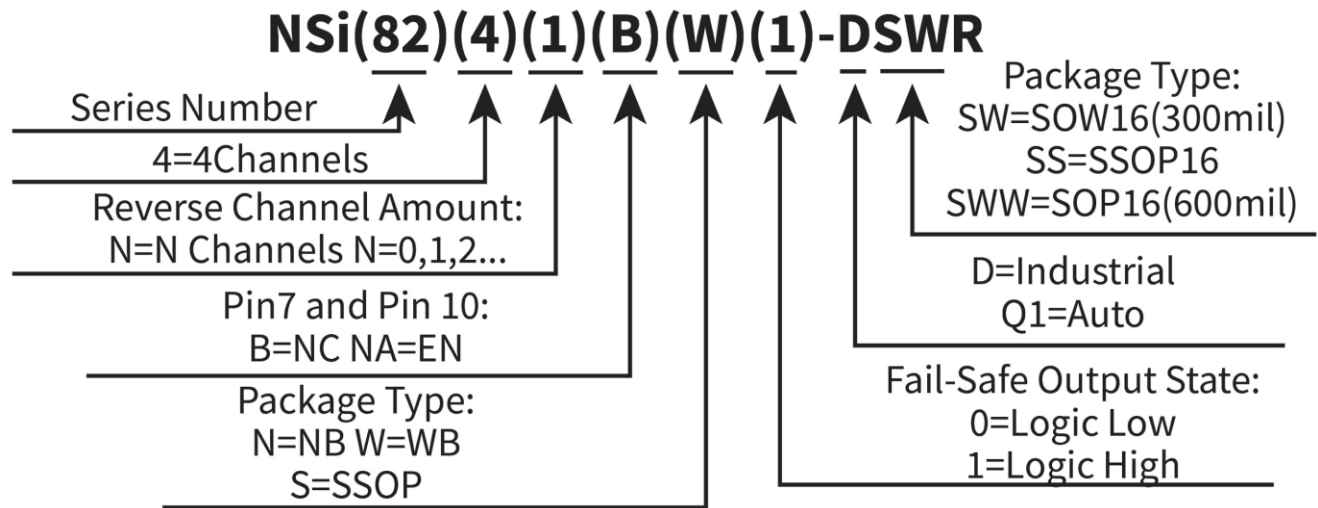
10. Order Information

| Part Number | Isolation Rating (kV) | Number of side 1 inputs | Number of side 2 inputs | Max Data Rate (Mbps) | Default Output State | Temperature | MSL | Package Type | Package Drawing | SPQ |
|-----------------|-----------------------|-------------------------|-------------------------|----------------------|----------------------|--------------|-----|----------------|-----------------|------|
| NSi8240W0-DSWR | 5 | 4 | 0 | 150 | Low | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8240W1-DSWR | 5 | 4 | 0 | 150 | High | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8241W0-DSWR | 5 | 3 | 1 | 150 | Low | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8241W1-DSWR | 5 | 3 | 1 | 150 | High | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8242W0-DSWR | 5 | 2 | 2 | 150 | Low | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8242W1-DSWR | 5 | 2 | 2 | 150 | High | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8240W0-DSWWR | 8 | 4 | 0 | 150 | Low | -55 to 125°C | 3 | SOP16 (600mil) | SOWW16 | 1000 |
| NSi8240W1-DSWWR | 8 | 4 | 0 | 150 | High | -55 to 125°C | 3 | SOP16 (600mil) | SOWW16 | 1000 |
| NSi8241W0-DSWWR | 8 | 3 | 1 | 150 | Low | -55 to 125°C | 3 | SOP16 (600mil) | SOWW16 | 1000 |
| NSi8241W1-DSWWR | 8 | 3 | 1 | 150 | High | -55 to 125°C | 3 | SOP16 (600mil) | SOWW16 | 1000 |
| NSi8242W0-DSWWR | 8 | 2 | 2 | 150 | Low | -55 to 125°C | 3 | SOP16 (600mil) | SOWW16 | 1000 |
| NSi8242W1-DSWWR | 8 | 2 | 2 | 150 | High | -55 to 125°C | 3 | SOP16 (600mil) | SOWW16 | 1000 |
| NSi8240S0-DSSR | 3 | 4 | 0 | 150 | Low | -55 to 125°C | 1 | SSOP16 | SSOP16 | 2500 |
| NSi8240S1-DSSR | 3 | 4 | 0 | 150 | High | -55 to 125°C | 1 | SSOP16 | SSOP16 | 2500 |
| NSi8241S0-DSSR | 3 | 3 | 1 | 150 | Low | -55 to 125°C | 1 | SSOP16 | SSOP16 | 2500 |
| NSi8241S1-DSSR | 3 | 3 | 1 | 150 | High | -55 to 125°C | 1 | SSOP16 | SSOP16 | 2500 |
| NSi8242S0-DSSR | 3 | 2 | 2 | 150 | Low | -55 to 125°C | 1 | SSOP16 | SSOP16 | 2500 |
| NSi8242S1-DSSR | 3 | 2 | 2 | 150 | High | -55 to 125°C | 1 | SSOP16 | SSOP16 | 2500 |
| NSi8240N0-DSPNR | 3 | 4 | 0 | 150 | Low | -55 to 125°C | 1 | SOP16 (150mil) | SOP16 | 2500 |
| NSi8240N1-DSPNR | 3 | 4 | 0 | 150 | High | -55 to 125°C | 1 | SOP16 (150mil) | SOP16 | 2500 |
| NSi8241N0-DSPNR | 3 | 3 | 1 | 150 | Low | -55 to 125°C | 1 | SOP16 (150mil) | SOP16 | 2500 |

| | | | | | | | | | | |
|-----------------|---|---|---|-----|------|--------------|---|----------------|-------|------|
| NSi8241N1-DSPNR | 3 | 3 | 1 | 150 | High | -55 to 125°C | 1 | SOP16 (150mil) | SOP16 | 2500 |
| NSi8242N0-DSPNR | 3 | 2 | 2 | 150 | Low | -55 to 125°C | 1 | SOP16 (150mil) | SOP16 | 2500 |
| NSi8242N1-DSPNR | 3 | 2 | 2 | 150 | High | -55 to 125°C | 1 | SOP16 (150mil) | SOP16 | 2500 |
| NSi8240BW0-DSWR | 5 | 4 | 0 | 150 | Low | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8240BW1-DSWR | 5 | 4 | 0 | 150 | High | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8241BW0-DSWR | 5 | 3 | 1 | 150 | Low | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8241BW1-DSWR | 5 | 3 | 1 | 150 | High | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8242BW0-DSWR | 5 | 2 | 2 | 150 | Low | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |
| NSi8242BW1-DSWR | 5 | 2 | 2 | 150 | High | -55 to 125°C | 2 | SOP16 (300mil) | SOW16 | 1000 |

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

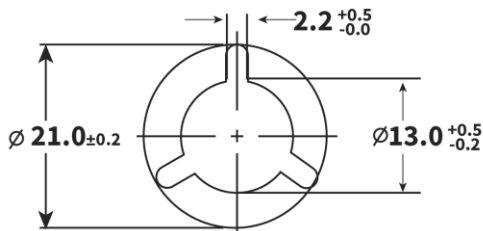
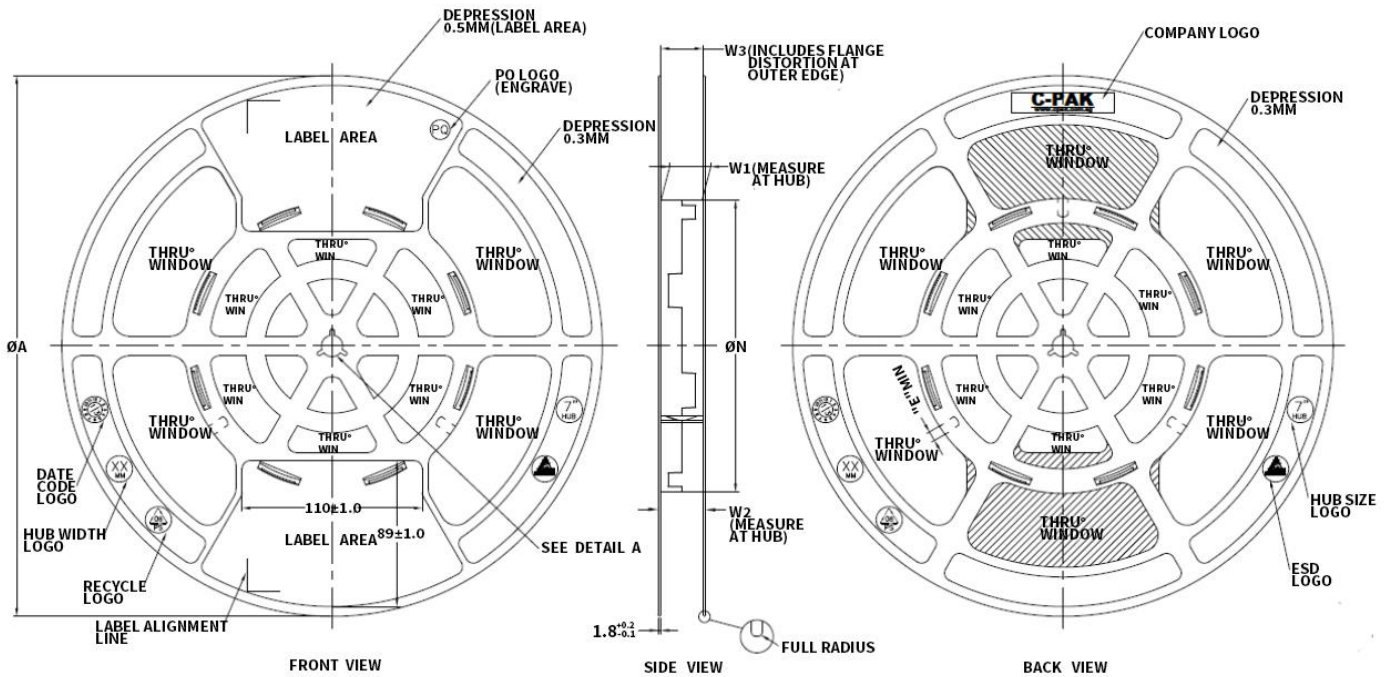
Part Number Rule:



11. Documentation Support

| Part Number | Product Folder | Datasheet | Technical Documents | Isolator selection guide |
|-------------|----------------|-----------|---------------------|--------------------------|
| NSi824x | tbd | tbd | tbd | tbd |

12. Tape and Reel Information

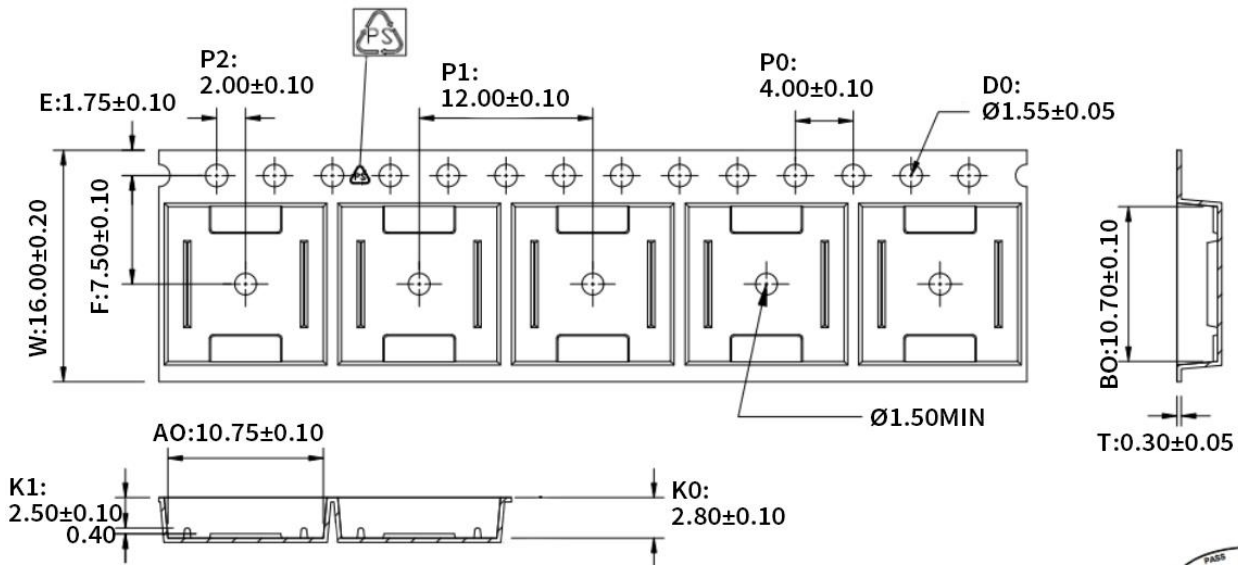


**ARBOR HOLE
DETAIL A
SCALE: 3:1**

| PRODUCT SPECIFICATION | | | | | | |
|-----------------------|-------------|-------------|--------------------------------------|-------------|---|------------|
| TAPE WIDTH | Ø A ±2.0 | Ø N ±2.0 | W1 | W2 (Max) | W3 | E (MIN) |
| 08MM | 330 | 178 | 8.4 ^{+1.5} _{-0.0} | 14.4 | SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE | 5.5 |
| 12MM | 330 | 178 | 12.4 ^{+2.0} _{-0.0} | 18.4 | | 5.5 |
| 16MM | 330 | 178 | 16.4 ^{+2.0} _{-0.0} | 22.4 | | 5.5 |
| 24MM | 330 | 178 | 24.4 ^{+2.0} _{-0.0} | 30.4 | | 5.5 |
| 32MM | 330 | 178 | 32.4 ^{+2.0} _{-0.0} | 38.4 | | 5.5 |

| SURFACE RESISTIVITY | | | |
|---------------------|---|---------------------|------------|
| LEGEND | SR RANGE | TYPE | COLOUR |
| A | BELOW 10 ¹² | ANTISTATIC | ALL TYPES |
| B | 10 ⁶ TO 10 ¹¹ | STATIC DISSIPATIVE | BLACK ONLY |
| C | 10 ⁵ & BELOW 10 ⁵ | CONDUCTIVE(GENERIC) | BLACK ONLY |
| E | 10 ⁹ TO 10 ¹¹ | ANTISTATIC(COATED) | ALL TYPES |

Figure 12.1 Reel Information (for all packages)



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity: $10^5 \sim 10^{10} \Omega/\square$

| | |
|----|------------|
| W | 16.00±0.20 |
| A0 | 10.75±0.10 |
| B0 | 10.70±0.10 |
| K0 | 2.80±0.10 |
| K1 | 2.50±0.10 |

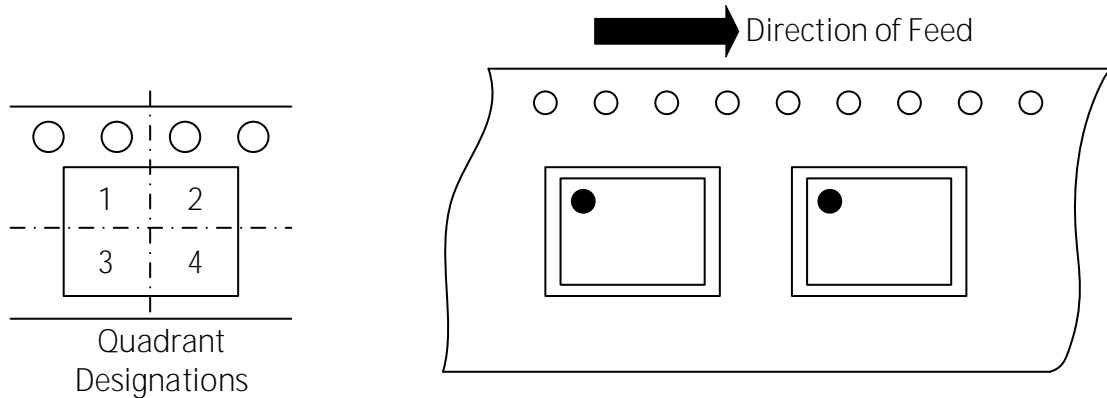


Figure 12.2 Tape Information of SOP16(300mil)

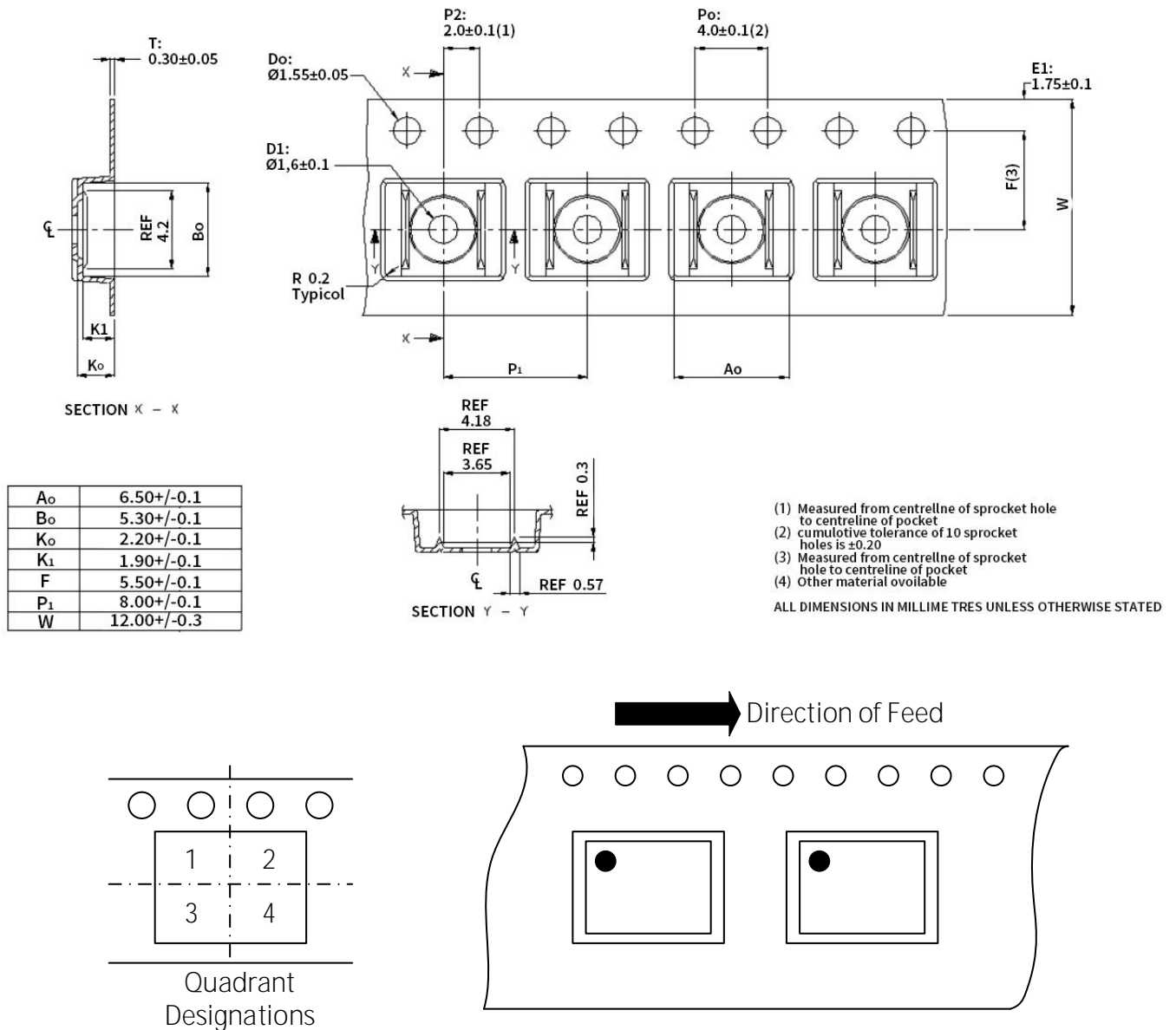


Figure 12.3 Tape Information of SSOP16

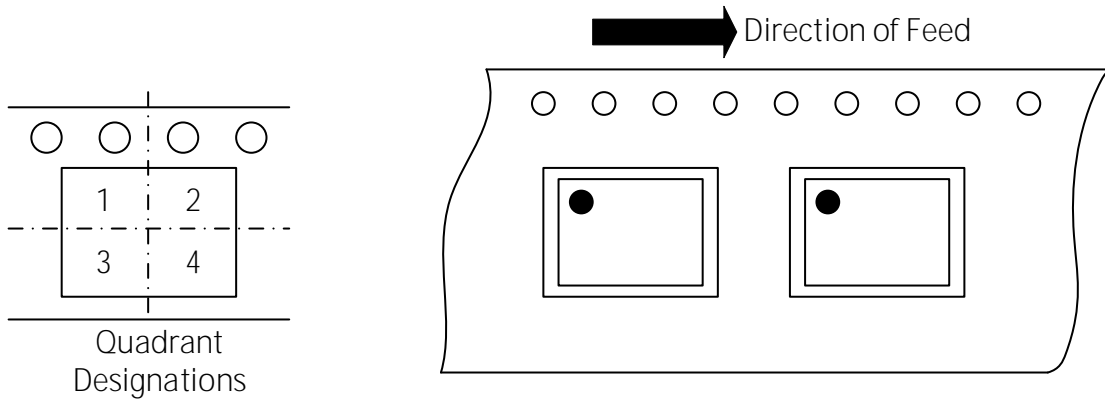
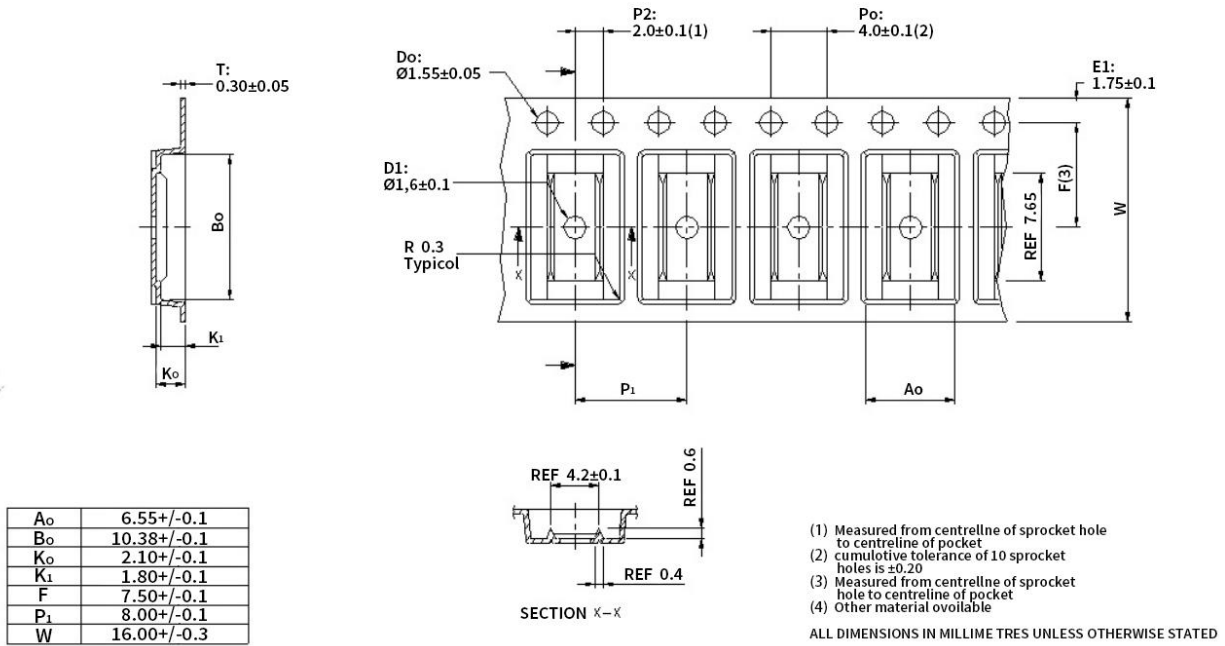
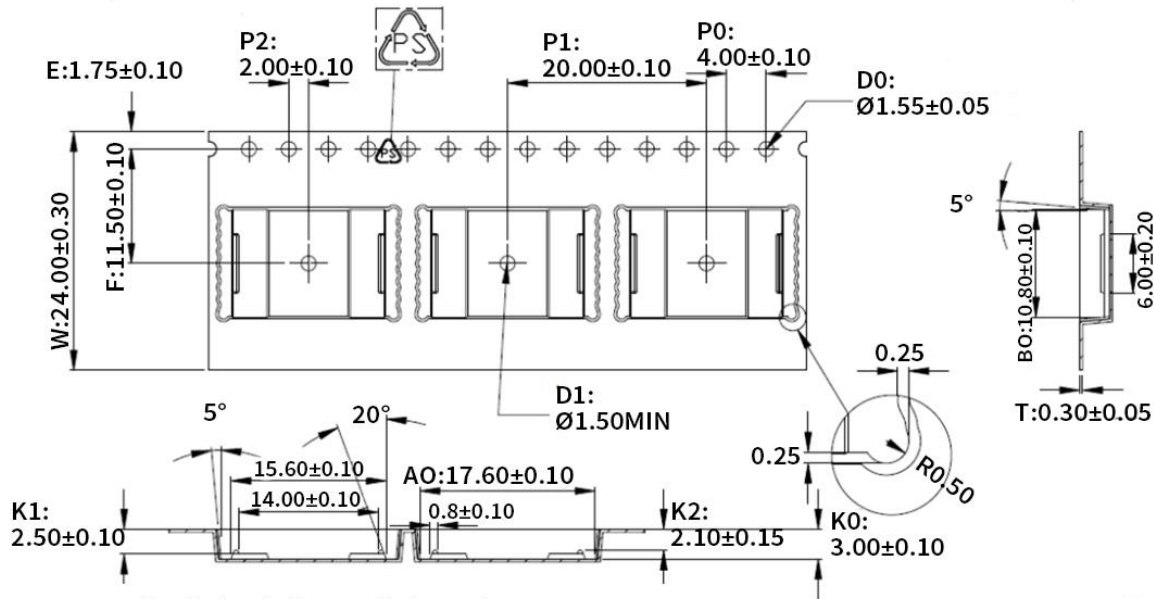


Figure 12.4 Tape Information of SOP16(150mil)



- 1.10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Packing length per 19" reel: 246.0 Meters.(Rewind 1:13)
7. Component load per 13" reel: 5000 pcs.
8. Surface resistivity: $10^5 \sim 10^{10} \Omega/\square$

| | |
|----|------------|
| W | 24.00±0.30 |
| A0 | 17.60±0.10 |
| B0 | 10.80±0.10 |
| K0 | 3.00±0.10 |
| K1 | 2.50±0.10 |

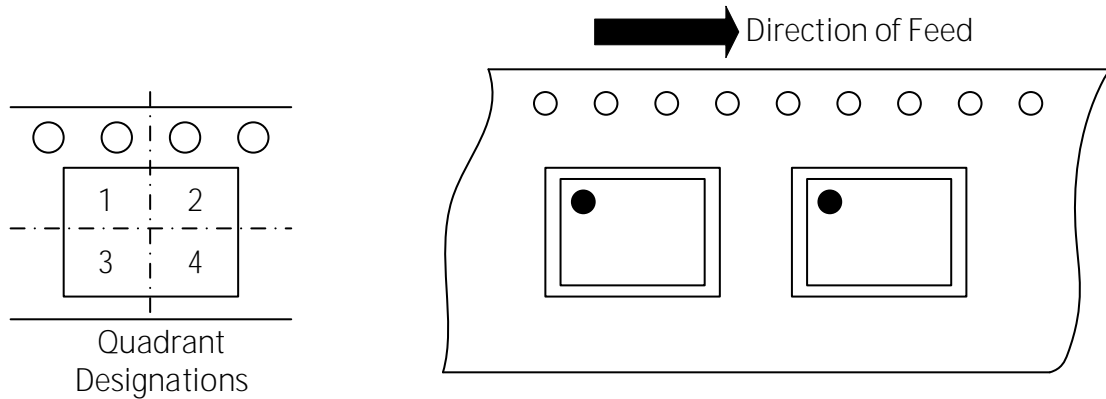


Figure 12.5 Tape Information of SOP16(600mil)

13. Revision History

| Revision | Description | Date |
|----------|--|------------|
| 1.0 | Initial version | 2020/11/13 |
| 1.1 | Changed tape and reel information | 2020/12/20 |
| 1.2 | Operating temperature support -55 to 125 °C | 2021/7/7 |
| 1.3 | Update Package Board Layout Example, update CQC information, Add SSOP16 package products | 2021/12/29 |
| 1.4 | Add SOP16 package products. Update SSOP16 Package Shape and Dimension in millimeters. Changed AEC-Q100 description. Update Part Number Rule, Package Board Layout Example. Update SOWW16 VISO. Update Regular Information NSi824xS-DSSR UL1577 file. Correct SOWW16 MSL. | 2022/9/7 |
| 1.5 | Update Typical Supply Current Equations | 2023/2/7 |

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