

Product Overview

NSi83085E is a high reliability isolated half duplex RS-485 transceiver based on NOVOSENSE digital isolation technology, while NSi83086E is an isolated full duplex RS-485 transceiver. Both devices are safety certified by UL1577 support 5kV_{rms} insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption.

The Bus pins of NSi83085E/NSi83086E are protected from ±10kV system level ESD to GND2 on Bus side. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus.

The data rate of NSi83085E is 12Mbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line. The data rate of NSi83086E is up to 16Mbps.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Bus side power supply voltage: 3.0V to 5.5V
- VDD1 supply voltage: 2.5V to 5.5V
- High CMTI: ±150kV/us
- High system level EMC performance:
Bus Pins meet IEC61000-4-2 ±10kV ESD
- Fail-safe protection receiver
- Up to 256 transceivers on the bus
- Operation temperature: -40°C~105°C
- RoHS-compliant packages:
SOW16

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated RS-485 communication
- Smart electric meter and water meter
- Security and protection monitoring

Device Information

Part Number	Package	Body Size
NSi83085E-DSWR	SOW16	10.30mm × 7.50mm
NSi83086E-DSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

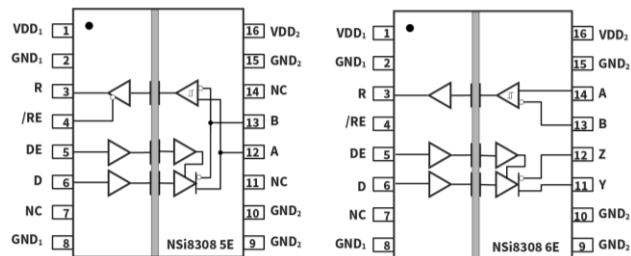


Figure 1. NSi83085E & NSi83086E Block Diagrams

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1. Pin Configuration and Functions

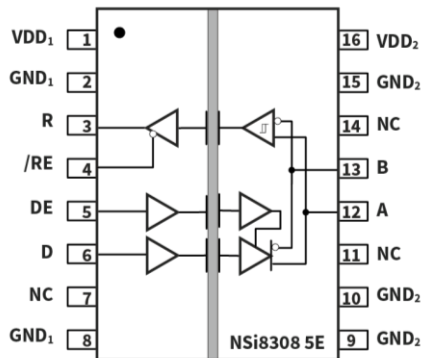


Figure 1.1 NSi83085E Package

Table 1.1 NSi83085E Pin Configuration and Description

NSi83085E PIN NO.	SYMBOL	FUNCTION
1	VDD ₁	Power Supply for Isolator Side 1
2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	R	Receive output
4	/RE	Receive enable input. This is an active low input.
5	DE	Driver enable input. This is an active high input
6	D	Driver transmit data input.
7	NC	No Connection.
8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	GND ₂	Ground 2, the ground reference for Isolator Side 2
11	NC	No Connection.
12	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when VDD ₁ or VDD ₂ is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when VDD ₁ or VDD ₂ is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
14	NC	No Connection.
15	GND ₂	Ground 2, the ground reference for Isolator Side 2
16	VDD ₂	Power Supply for Isolator Side 2

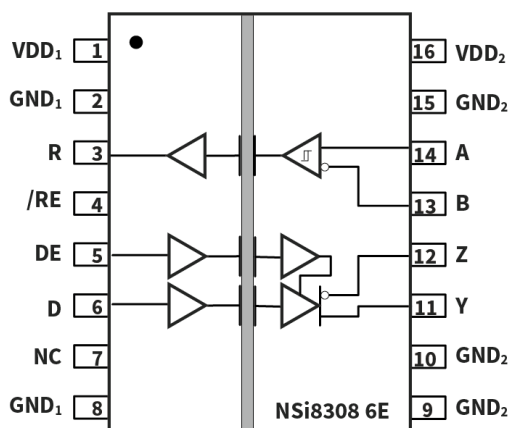


Figure 1.2 NSi83086E Package

Table 1.2 NSi83086E Pin Configuration and Description

NSi83086E PIN NO.	SYMBOL	FUNCTION
1	VDD ₁	Power Supply for Isolator Side 1
2	GND ₁	Ground 1, the ground reference for Isolator Side 1
3	R	Receive output
4	/RE	Receive enable input. This is an active low input.
5	DE	Driver enable input. This is an active high input
6	D	Driver transmit data input.
7	NC	No Connection.
8	GND ₁	Ground 1, the ground reference for Isolator Side 1
9	GND ₂	Ground 2, the ground reference for Isolator Side 2
10	GND ₂	Ground 2, the ground reference for Isolator Side 2
11	Y	Noninverting Driver Output. When the driver is disabled, or when VDD ₁ or VDD ₂ is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
12	Z	Inverting Driver Output. When the driver is disabled, or when VDD ₁ or VDD ₂ is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Receiver Input.
14	A	Noninverting Receiver Input.
15	GND ₂	Ground 2, the ground reference for Isolator Side 2
16	VDD ₂	Power Supply for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD ₁ , VDD ₂	-0.5		6	V	
Maximum Input Voltage	/RE, DE, TXD	-0.4		VDD+0.4	V	
Driver Output/Receiver Input Voltage	VA, VB, VY, VZ	-7		12	V	
Differential input voltage, A with respect to B	V _{ID}	-18		18	V	
Voltage input, transient pulse (through 100Ω)	V _{IT}	-30		30	V	A, B, Y and Z
Receiver Output Current	I _o	-15		15	mA	
Maximum Surge Isolation Voltage	V _{IOSM}			6.25	kV	
Operating Temperature	Topr	-40		105	°C	
Junction Temperature	T _j	-40		150		
Storage Temperature	T _{stg}	-65		150	°C	
Electrostatic discharge	HBM (Bus pins and GND)			±8000	V	
	HBM (All pins)			±6000	V	
	CDM			±2000	V	

3. Thermal Information

Parameters	Symbol	SOP16(300mil)	Unit
IC Junction-to-Air Thermal Resistance	θ _{JA}	67.9	°C/W
Junction-to-case (top) thermal resistance	θ _{JC (top)}	27.7	°C/W
Junction-to-board thermal resistance	θ _{JB}	29.4	°C/W

4. Specifications

4.1. DC Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=3.0V~5.5V, Ta=-40°C to 105°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power supply voltage	VDD ₁	2.5		5.5	V	
	VDD ₂	3.0		5.5	V	Bus Side
Logic-side supply current	I _{DD1}		2.97	4.98	mA	VDD ₁ =5V, DE=high, /RE=D =low, no load
			2.94	4.89	mA	VDD ₁ =3V, DE=high, /RE=D =low, no load
Bus-side supply current	I _{DD2}		2.83	5.02	mA	VDD ₂ =5V, DE=high, /RE=D =low, no load (NSi83085E)
			2.15	3.23	mA	VDD ₂ =5V, DE=high, /RE=D =low, no load (NSi83086E)
Thermal-Shutdown Threshold	T _{TS}		165		°C	
Thermal-Shutdown Hysteresis	T _{TSH}		15		°C	
Common Mode Transient Immunity	CMTI	±100	±150		kV/us	
Logic Side						
Input High Voltage	V _{IH}	2			V	DE, D,
		0.7*V _{D1}				/RE
Input Low Voltage	V _{IL}			0.8	V	DE, D
				0.3*V _{D1}		/RE
Input Pull up Current	I _{PU}			20	µA	DE,/RE
Input Pull down Current	I _{PD}	-20			µA	DI
Output Voltage High	V _{OH}	VDD ₁ -0.3			V	I _{OH} = -4mA
Output Voltage Low	V _{OL}			0.3	V	I _{OL} = 4mA
Output Short-Circuit Current	I _{OSR}			150	mA	0 ≤ V _R ≤ VDD ₁
Three-State Output Current	I _{OZ}	-15			µA	0 ≤ V _R ≤ VDD ₁ , /RE = high

Input Capacitance	C_{IN}		2		pF	DE, D, /RE
Driver						
Differential Output Voltage	$ V_{OD} $			VDD2	V	No Load
		2.7		VDD2	V	See Figure 4.11, $R_L=100\Omega$ (RS-422), VDD2=5V
		1.5		VDD2	V	See Figure 4.11, $R_L=100\Omega$ (RS-422), VDD2=3.3V
		2.1		VDD2	V	See Figure 4.11, $R_L=54\Omega$ (RS-485), VDD2=5V
		1.3		VDD2	V	See Figure 4.11, $R_L=54\Omega$ (RS-485), VDD2=3.3V
Change in magnitude of the differential output voltage	$\Delta V_{OD} $			0.2	V	See Figure 4.11, $R_L=100\Omega$ or $R_L=54\Omega$
Common-Mode Output Voltage	$ V_{OC} $		VDD ₂ /2	3.5	V	See Figure 4.11, $R_L=100\Omega$ or $R_L=54\Omega$
Change in Magnitude of Common-Mode Voltage	$\Delta V_{OC} $			0.2	V	See Figure 4.11, $R_L=100\Omega$ or $R_L=54\Omega$
Driver Short-Circuit Output Current	I_{OSD}			250	mA	$0 \leq V_{OUT} \leq +12V$
		-250			mA	$-7V \leq V_{OUT} \leq VDD_2$
Output Leakage Current (Y and Z) Full-Duplex	I_o			200	μ A	DE=GND, VIN=12V
		-150			μ A	DE=GND, VIN=-7V
Receiver						
Input Current (A and B)	I_A, I_B			200	μ A	DE=GND, VDD ₂ =GND, VIN=12V
		-200			μ A	DE=GND, VDD ₂ =GND, VIN=-7V
Receiver Differential Threshold Voltage	V_{TH}	-200	-125	-10	mV	$-7V \leq V_{CM} \leq 12V$
Receiver Input Hysteresis	ΔV_{TH}		15		mV	$V_A+V_B=0$
Receiver Input Resistance	R_{IN}	96			k Ω	$-7V \leq V_{CM} \leq 12V$, DE=low

4.2. Switching Electrical Characteristics

(VDD1=2.5V~5.5V, VDD2=3.0V~5.5V, Ta=-40°C to 105°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Driver (NSi83085E)						
Maximum Data Rate	f _{MAX}	12			Mbps	
Driver Propagation Delay	t _{PLH}		30	50	ns	See Figure 4.12, R_L=54Ω, C_L=50pF
	t _{PHL}		30	50	ns	See Figure 4.12, R_L=54Ω, C_L=50pF
Driver Pulse Width Distortion, t _{PHL} - t _{PLH}	PWD		1	10	ns	See Figure 4.12, R_L=54Ω, C_L=50pF
Driver Output Falling Time or Rising time	t _F		8	16	ns	See Figure 4.12, R_L=54Ω, C_L=50pF
	t _R		7	14	ns	See Figure 4.12, R_L=54Ω, C_L=50pF
Driver Enable to Output High	t _{ZH}		17.2	60	ns	See Figure 4.13, R_L=110Ω, C_L=50pF
Driver Enable to Output Low	t _{ZL}		26.8	60	ns	See Figure 4.13, R_L=110Ω, C_L=50pF
Driver Output High to Disable	t _{HZ}		17	60	ns	See Figure 4.13, R_L=110Ω, C_L=50pF
Driver Output Low to Disable	t _{LZ}		24	60	ns	See Figure 4.13, R_L=110Ω, C_L=50pF
Receiver (NSi83085E)						
Maximum Data Rate	f _{MAX}	12			Mbps	
Receiver Propagation Delay	t _{PLH}		76	120	ns	See Figure 4.14, C_L=15pF
	t _{PHL}		78	120	ns	See Figure 4.14, C_L=15pF
Receiver Pulse Width Distortion	PWD		4	25	ns	t _{PHL} - t _{PLH} , See Figure 4.14, C_L=15pF
Receiver Output Falling Time or Rising time	t _F		2.4	5	ns	See Figure 4.14, C_L=15pF
	t _R		3.4	7	ns	See Figure 4.14, C_L=15pF
Receiver Enable to Output High	t _{ZH}		16	60	ns	See Figure 4.15, R_L=1kΩ, C_L=15pF

Receiver Enable to Output Low	t_{zL}		16	60	ns	See Figure 4.15, $R_L=1k\Omega, C_L=15pF$
Receiver Disable to Output High	t_{Hz}		17	60	ns	See Figure 4.15, $R_L=1k\Omega, C_L=15pF$
Receiver Disable to Output Low	t_{Lz}		14	60	ns	See Figure 4.15, $R_L=1k\Omega, C_L=15pF$
Driver (NSi83086E)						
Maximum Data Rate	f_{MAX}	16			Mbps	
Driver Propagation Delay	t_{PLH}		30	50	ns	See Figure 4.12, $R_L=54\Omega, C_L=50pF$
	t_{PHL}		30	50	ns	See Figure 4.12, $R_L=54\Omega, C_L=50pF$
Driver Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	PWD		1	10	ns	See Figure 4.12, $R_L=54\Omega, C_L=50pF$
Driver Output Falling Time or Rising time	t_F		8	16	ns	See Figure 4.12, $R_L=54\Omega, C_L=50pF$
	t_R		7	14	ns	See Figure 4.12, $R_L=54\Omega, C_L=50pF$
Driver Enable to Output High	t_{zH}		17.2	60	ns	See Figure 4.13, $R_L=110\Omega, C_L=50pF$
Driver Enable to Output Low	t_{zL}		26.8	60	ns	See Figure 4.13, $R_L=110\Omega, C_L=50pF$
Driver Disable to Output High	t_{Hz}		17	60	ns	See Figure 4.13, $R_L=110\Omega, C_L=50pF$
Driver Disable to Output Low	t_{Lz}		24	60	ns	See Figure 4.13, $R_L=110\Omega, C_L=50pF$
Receiver (NSi83086E)						
Maximum Data Rate	f_{MAX}	16			Mbps	
Receiver Propagation Delay	t_{PLH}		76	120	ns	See Figure 4.14, $C_L=15pF$
	t_{PHL}		78	120	ns	See Figure 4.14, $C_L=15pF$
Receiver Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	PWD		4	25	ns	See Figure 4.14, $C_L=15pF$
Receiver Output Falling Time or Rising time	t_F		2.4	5	ns	See Figure 4.14, $C_L=15pF$
	t_R		3.4	7	ns	See Figure 4.14, $C_L=15pF$

Receiver Enable to Output High	t _{ZH}		16	60	ns	See Figure 4.15. R_L=1kΩ, C_L=15pF
Receiver Enable to Output Low	t _{ZL}		16	60	ns	See Figure 4.15. R_L=1kΩ, C_L=15pF
Receiver Disable to Output High	t _{HZ}		17	60	ns	See Figure 4.15. R_L=1kΩ, C_L=15pF
Receiver Disable to Output Low	t _{LZ}		14	60	ns	See Figure 4.15. R_L=1kΩ, C_L=15pF

4.3. Typical Performance Characteristics

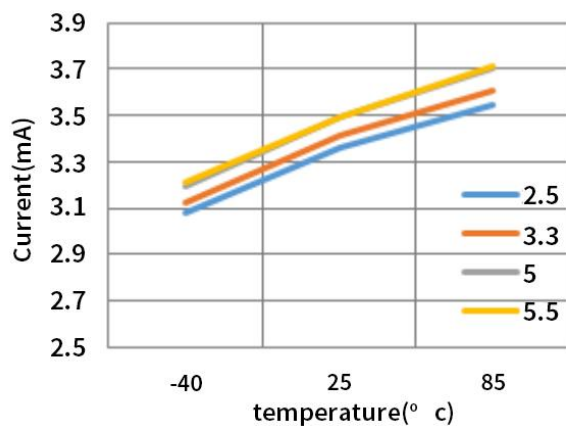


Figure 4.1 NSi83085E VDD1 supply current vs Temperature

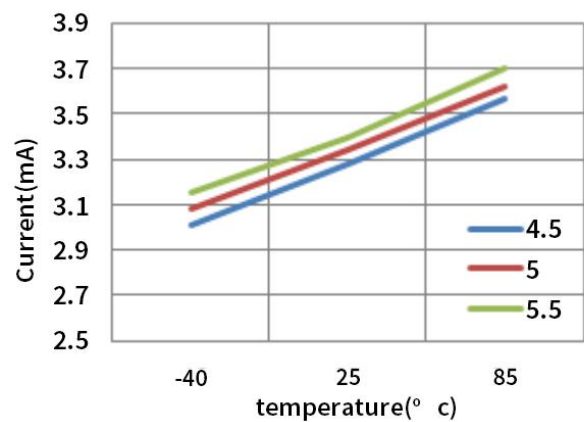


Figure 4.2 NSi83085E VDD2 supply current vs Temperature

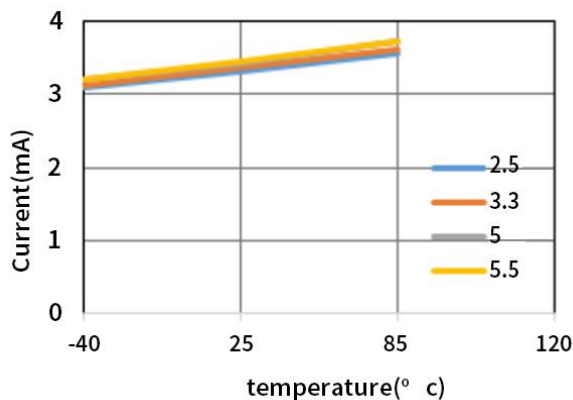


Figure 4.3 NSi83086E VDD1 supply current vs Temperature

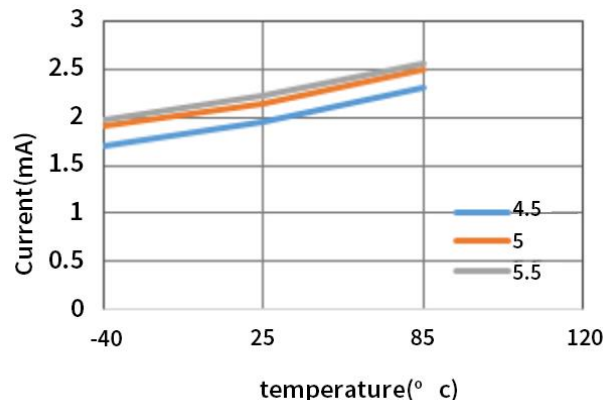


Figure 4.4 NSi83086E VDD2 supply current vs Temperature

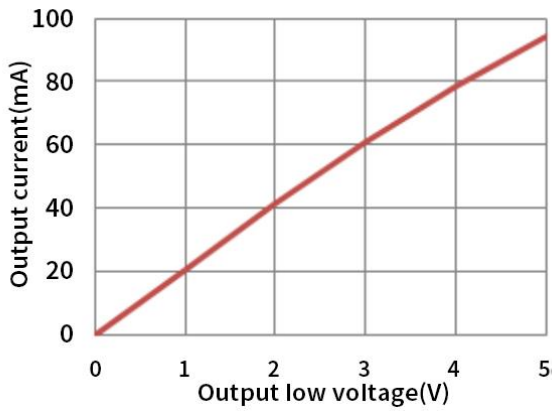


Figure 4.5 Receiver output current vs Output low voltage

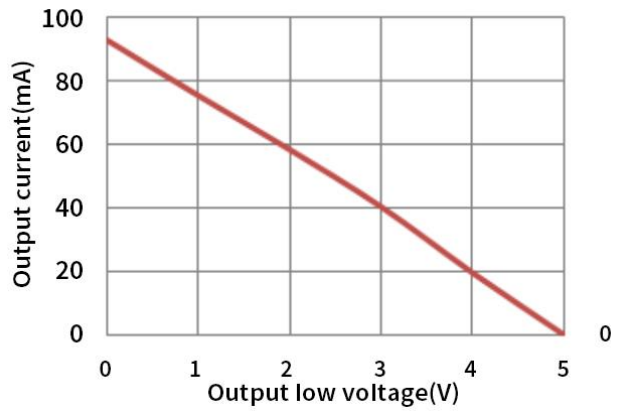


Figure 4.6 Receiver output current vs Output High voltage

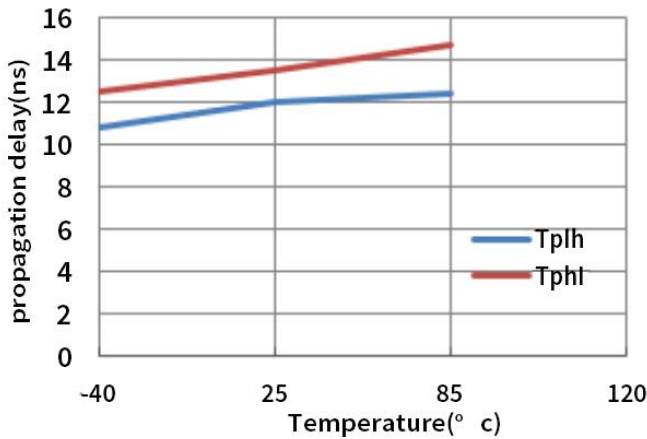


Figure 4.7 NSi83085E Transmitter Propagation Delay vs Temperature

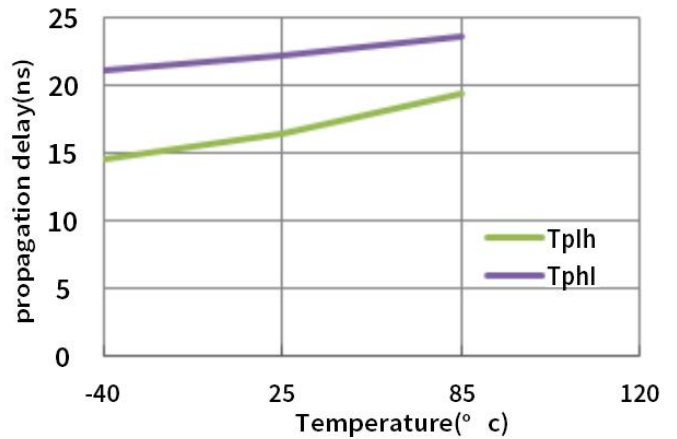


Figure 4.8 NSi83085E Receiver Propagation Delay vs Temperature

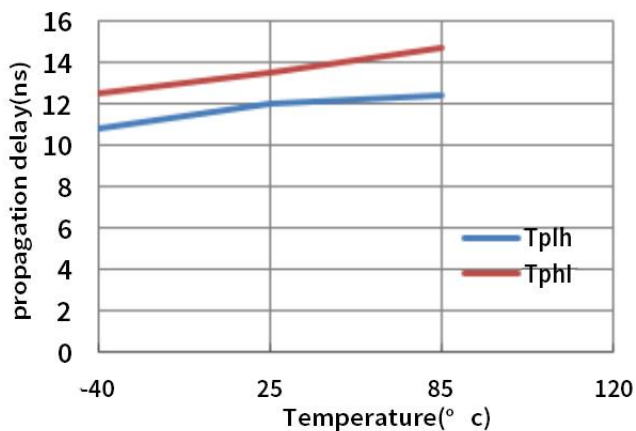


Figure 4.9 NSi83086E Transmitter Propagation Delay vs Temperature

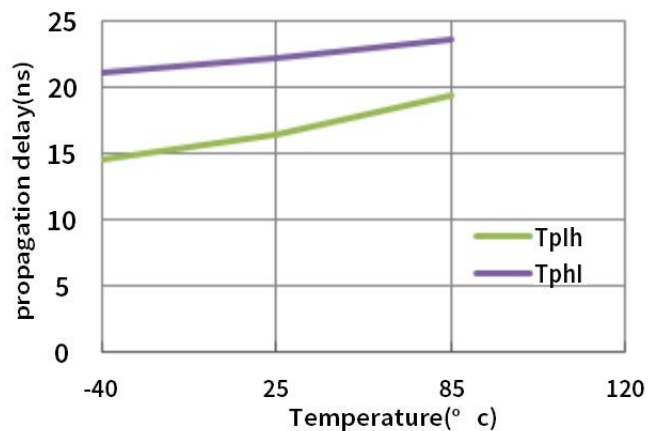


Figure 4.10 NSi83086E Receiver Propagation Delay vs Temperature

4.4. Parameter Measurement Information

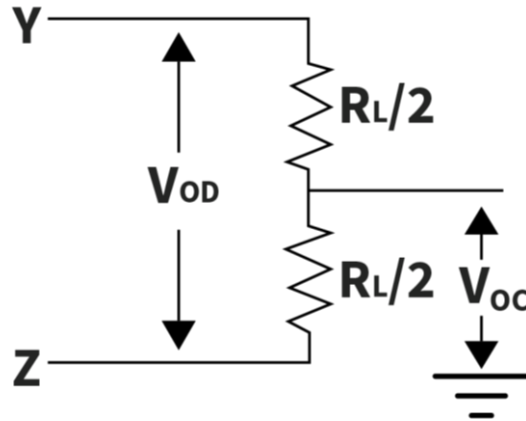


Figure 4.11 Driver DC Test Load

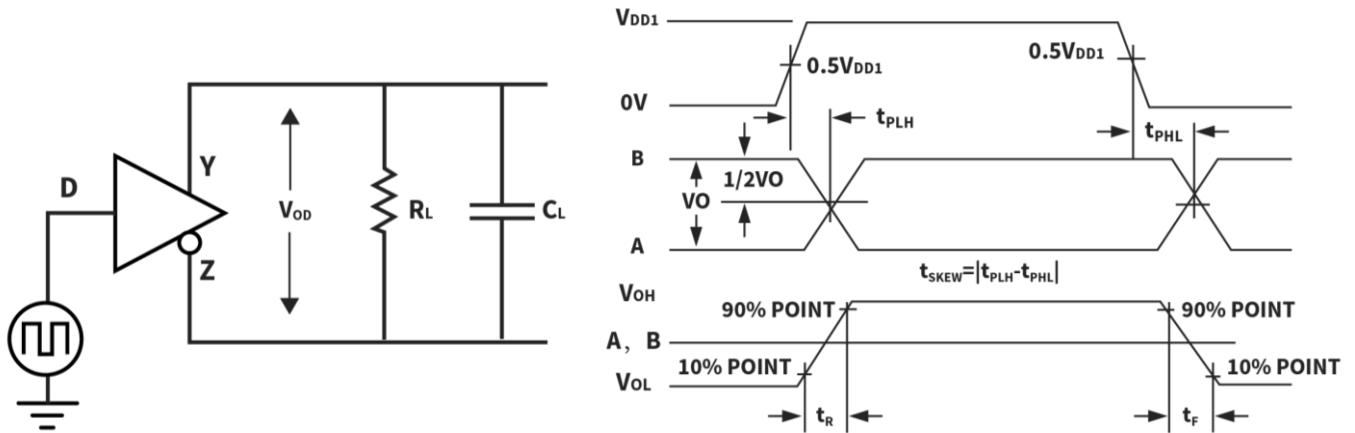


Figure 4.12 Driver Timing Test Circuit and waveform

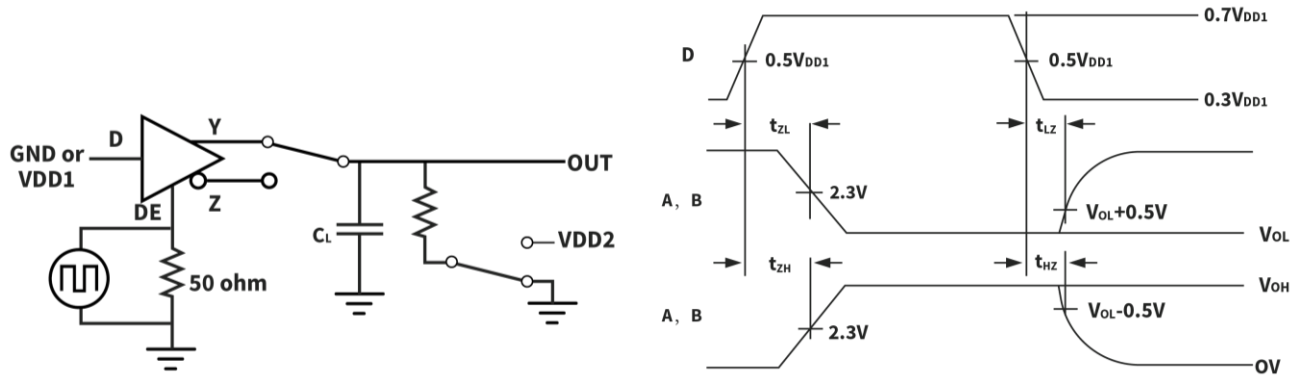


Figure 4.13 Driver Enable Disable Timing Test Circuit and waveform

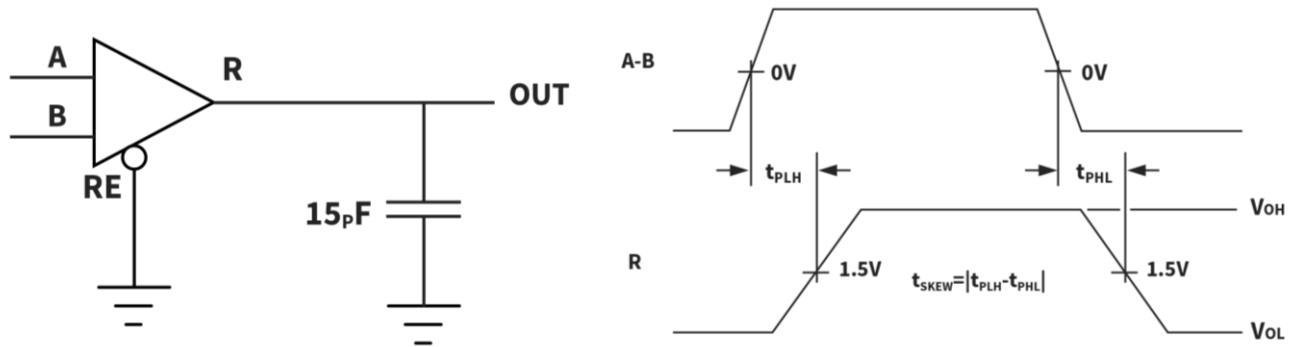


Figure 4.14 Receiver Propagation Delay Test Circuit and waveform

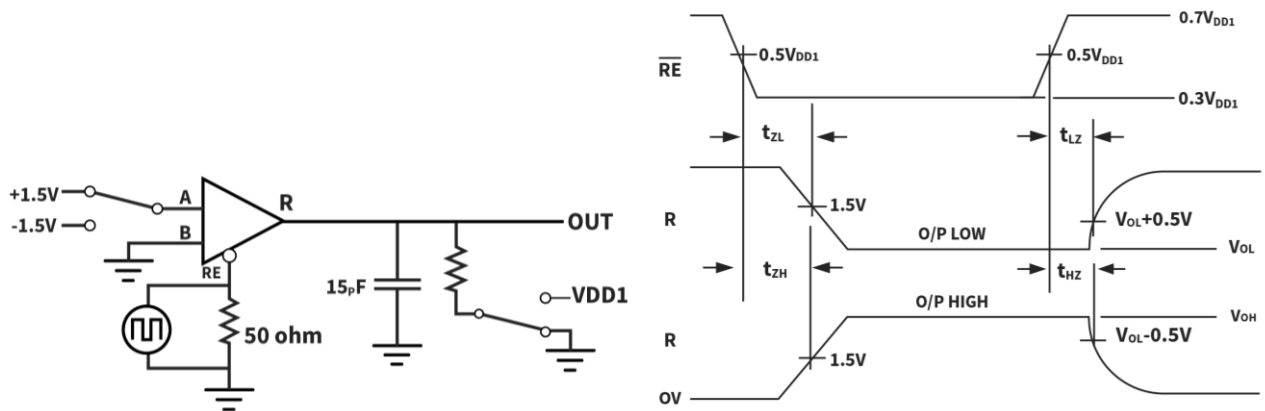


Figure 4.15 Receiver Enable Disable Timing Test Circuit and waveform

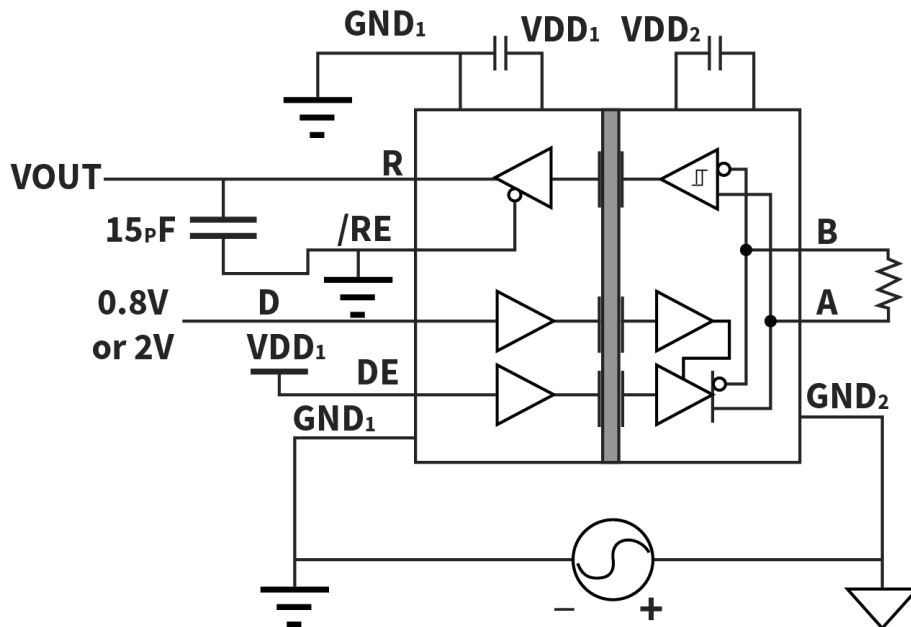


Figure 4.16 Common-Mode Transient Immunity Test Circuit

5. High Voltage Feature Description

5.1. Insulation and Safety Related Specifications

Description	Test Condition	Symbol	Value	Unit
Min. External Air Gap (Clearance)		CLR	8	mm
Min. External Tracking (Creepage)		CPG	8	mm
Distance through the Insulation		DTI	28	um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600	V
Material Group	IEC 60112		I	
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage $\leq 150V_{rms}$			I to IV	
For Rated Mains Voltage $\leq 300V_{rms}$			I to IV	
For Rated Mains Voltage $\leq 600V_{rms}$			I to IV	
For Rated Mains Voltage $\leq 1000V_{rms}$			I to III	
Insulation Specification per DIN VDE V 0884-11:2017-01 ¹⁾				
Climatic Classification			10/105/2 1	
Pollution Degree	per DIN VDE 0110, Table 1		2	
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	V_{RMS}
	DC voltage		2121	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	2121	V_{peak}
Input to Output Test Voltage, Method B1	$V_{ini. b} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.875$, $t_{ini} = t_m = 1 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$, 100% production test	$V_{pd(m)}$	3977	V_{peak}
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{ini. a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.6$, $t_{ini} = 60 \text{ sec}$, $t_m = 10 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	3394	V_{peak}
Input to Output Test Voltage, Method A. After Input and Output Safety Test Subgroup 2 and Subgroup 3	$V_{ini. a} = V_{IOTM}$, $V_{pd(m)} = V_{IORM} \times 1.2$, $t_{ini} = 60 \text{ sec}$, $t_m = 10 \text{ sec}$, $q_{pd} \leq 5 \text{ pC}$	$V_{pd(m)}$	2545	V_{peak}
Maximum transient isolation voltage	$t = 60 \text{ sec}$	V_{IOTM}	8000	V_{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST} = 1.6 \times V_{IOSM}$	V_{IOSM}	6250	V_{peak}
Isolation resistance	$V_{IO} = 500 \text{ V}$, $T_{amb} = T_s$	R_{IO}	$>10^9$	Ω
	$V_{IO} = 500 \text{ V}$, $100 \text{ }^\circ\text{C} \leq T_{amb} \leq 125 \text{ }^\circ\text{C}$		$>10^{11}$	Ω

Isolation capacitance	f = 1MHz	C _{IO}	0.6	pF
Insulation Specification per UL1577				
Withstand Isolation Voltage	V _{TEST} = 1.2 × V _{ISO} , t = 1 sec, 100% production test	V _{ISO}	5000	V _{rms}

- 1) This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

5.2. Safety-Limiting Values

Description	Test Condition	Value	Unit
Safety Supply Power	R _{θJA} = 67.9 °C/W ¹⁾ , T _J = 150 °C, T _A = 25 °C	1840	mW
Safety Supply Current	R _{θJA} = 67.9 °C/W ¹⁾ , V _I = 5V, T _J = 150 °C, T _A = 25 °C	368	mA
Safety Temperature ²⁾		150	°C

- 1) Calculate with the junction-to-air thermal resistance, R_{θJA}, of SOP16(300mil) package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

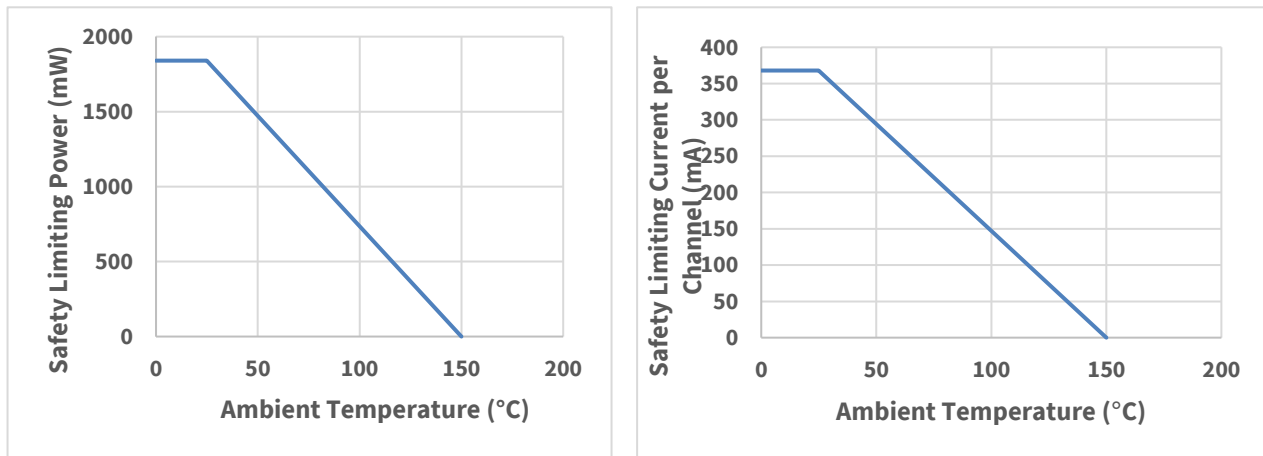


Figure 5.1 NSi83085E/NSi83086E Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

5.3. Regulatory information

The NSi83085E/NSi83086E are approved or pending approval by the organizations listed in table.

CUL	VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01
Single Protection, 5000Vrms Isolation voltage	Single Protection, 5000Vrms Isolation voltage	Reinforce Insulation 2121Vpeak, VIOSM=6250Vpeak
		Certified by CQC11-471543-2012 GB4943.1-2011
		Reinforced insulation

File (E500602)	File (E500602)	File (40052820)	File (pending)
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6. Function Description

NSi83085E is a high reliability isolated half duplex RS-485 transceiver, while NSi83086E is an isolated full duplex RS-485 transceiver. Data isolation is achieved using Novosense integrated capacitive isolation that allows data transmission between the logic side and the Bus side. Both devices are safety certified by UL1577 support 5kV_{RMS} insulation withstand voltages.

6.1. Data rate

The data rate of NSi83085E is 12Mbps. The device is slew limited to reduce EMI and reflections with improperly terminated transmission line. The data rate of NSi83086E is up to 16Mbps.

6.2. True Fail-safe receiver inputs

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -10mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage ($V_A - V_B$) is greater than or equal to -50mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

6.3. Truth tables

Table 6.1 Driver Function Table¹

<i>VDD1 status</i>	<i>VDD2 status</i>	<i>Input (D)</i>	<i>Enable Input (DE)</i>	<i>Outputs¹</i>	
				<i>A/Y</i>	<i>B/Z</i>
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Z	Z
PU	PU	X	OPEN	Z	Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Z	Z
PU	PD	X	X	Z	Z
PD	PD	X	X	Z	Z

¹ PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance; Driver output pins are Y and Z for NSi83086E, A and B for NSi83085E.

Table 6.2 Receiver Function Table¹

<i>VDD1 status</i>	<i>VDD2 status</i>	<i>Differential Input (V_A-V_B)</i>	<i>Enable Input (/RE)</i>	<i>Output (R)</i>
PU	PU	≥-10mV	L/Open	H
PU	PU	≤-200mV	L/Open	L
PU	PU	Open/Short	L/Open	H
PU	PU	X	H	Z
PU	PU	Idle	L	H

VDD1 status	VDD2 status	Differential Input (V_A-V_B)	Enable Input (/RE)	Output (R)
PD	PU	X	X	Z
PU	PD	X	L/Open	H
PD	PD	X	X	Z

¹ PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance.

6.4. Thermal shutdown

The device is protected from over temperature damage by integrated thermal shutdown circuitry. When the junction temperature (TJ) exceeds +165°C (typ), the driver outputs go high-impedance. The device resumes normal operation when TJ falls below +145°C (typ).

7. Application Note

7.1. 256 transceivers on the bus

The devices have a 1/8-unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

7.2. ESD protection

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handling and assembly. The Bus pins have extra protection against static electricity to both the logic side (VDD1 side) and bus side (VDD2 side).

ESD protection can be tested in various ways. Below is the ESD spec of the devices.

Bus pins:

- ± 8kV HBM.
- ±10kV using the Contact Discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- ±6kV HBM.
- ±7kV using the Contact Discharge method specified in IEC 61000-4-2

7.3. Layout considerations

The NSi83085E/NSi83086E requires a 0.1 μF bypass capacitor between VDD and GND. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to have the bus connectors and termination resistor as close as possible to the A and B, Y and Z pins.

7.4. Typical application

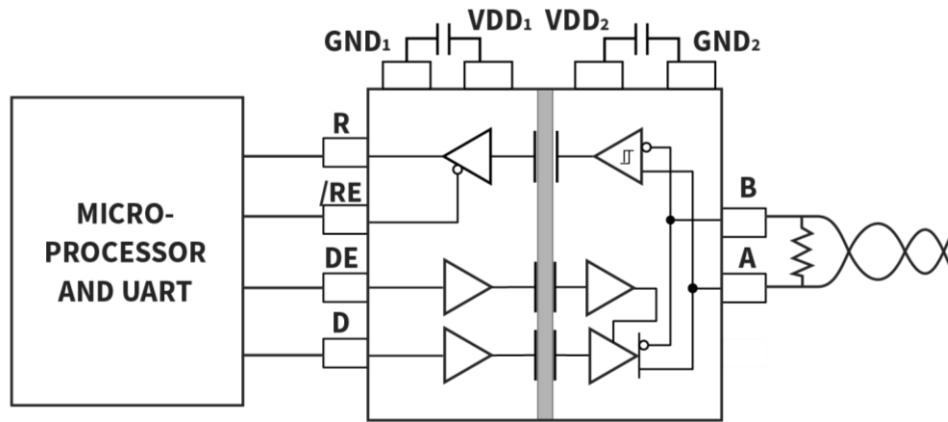


Figure 7.1 NSi83085E typical application circuit

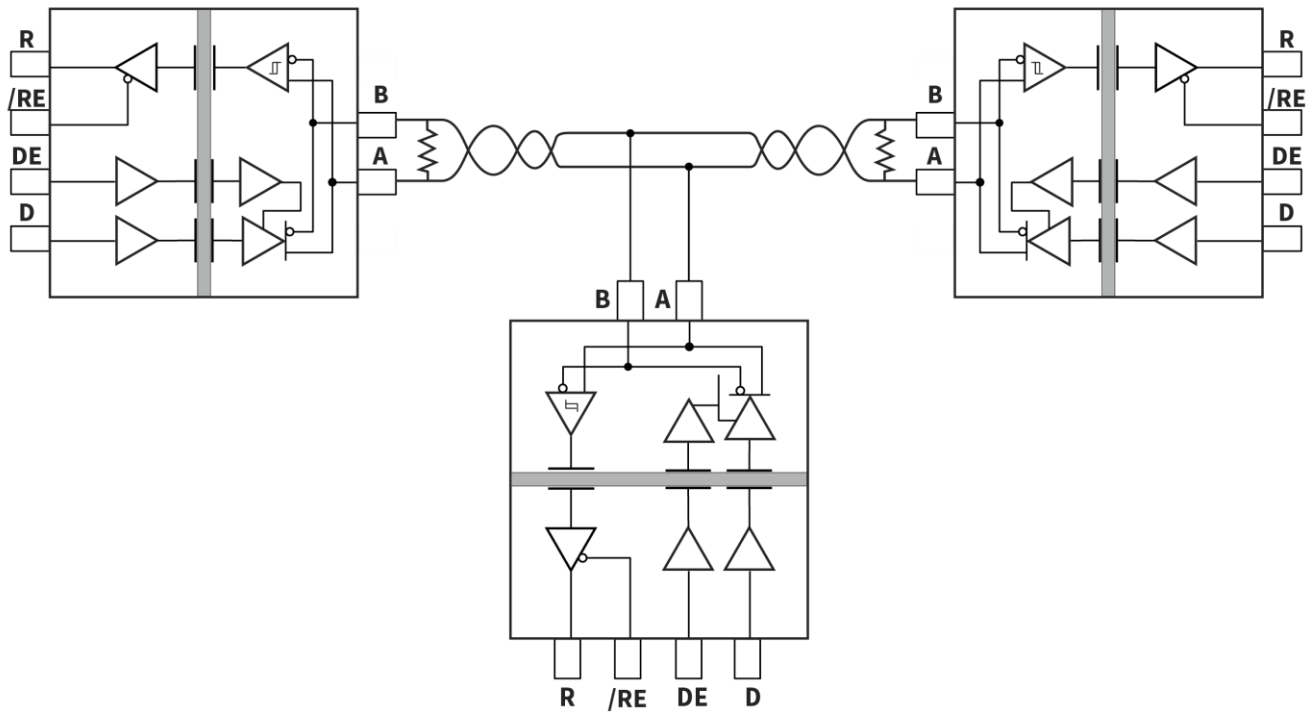


Figure 7.2 Typical isolated Half-Duplex RS-485 application

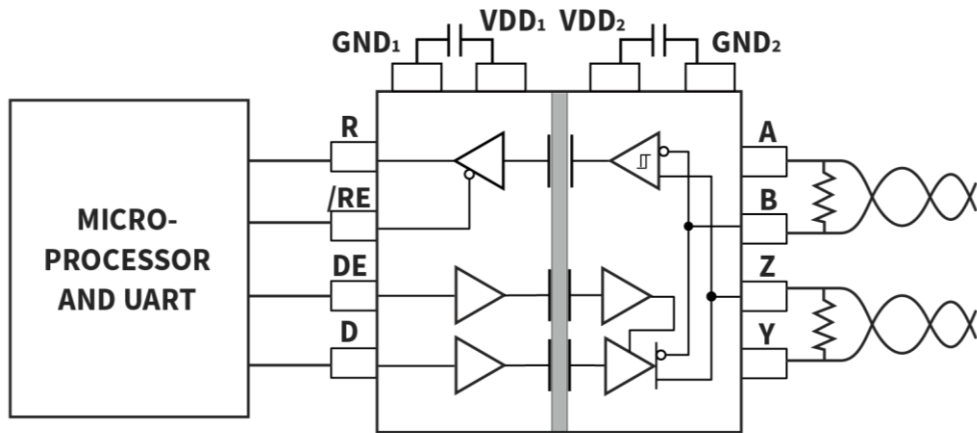


Figure 7.3 NSi83086E typical application circuit

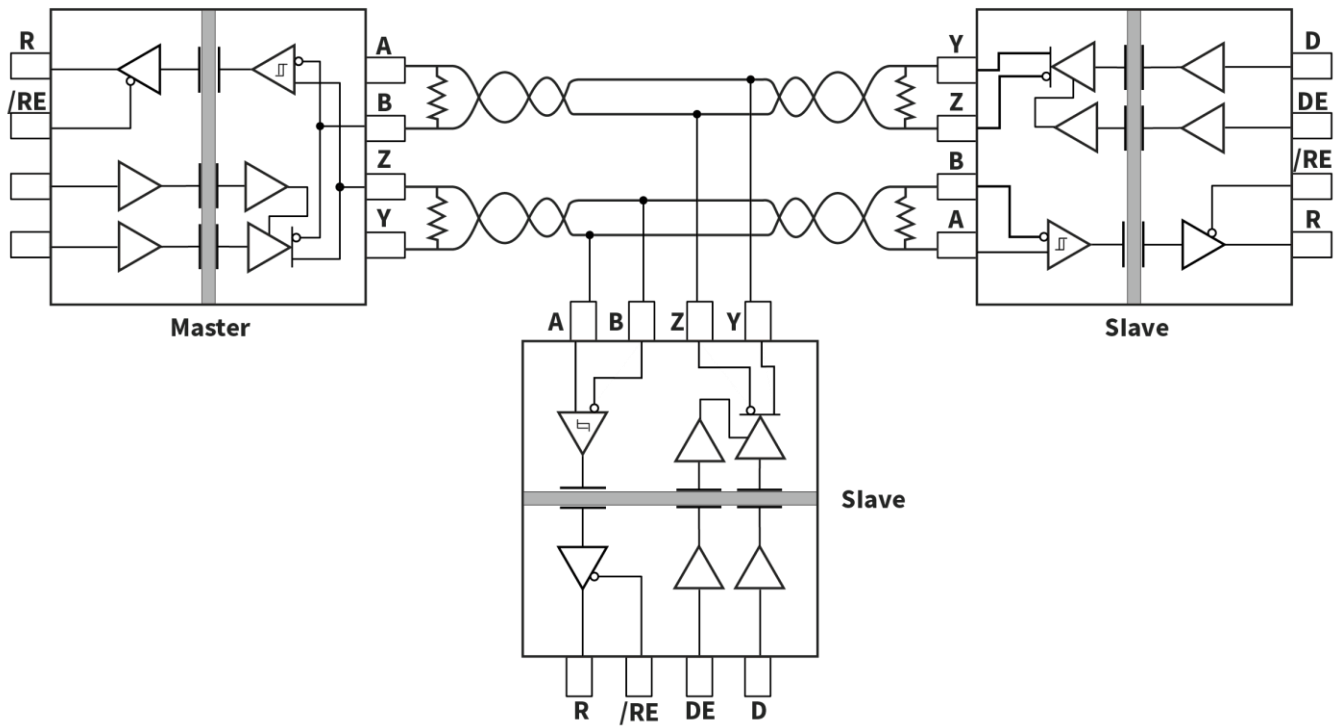


Figure 7.4 Typical isolated Full-Duplex RS-485 application

8. Package Information

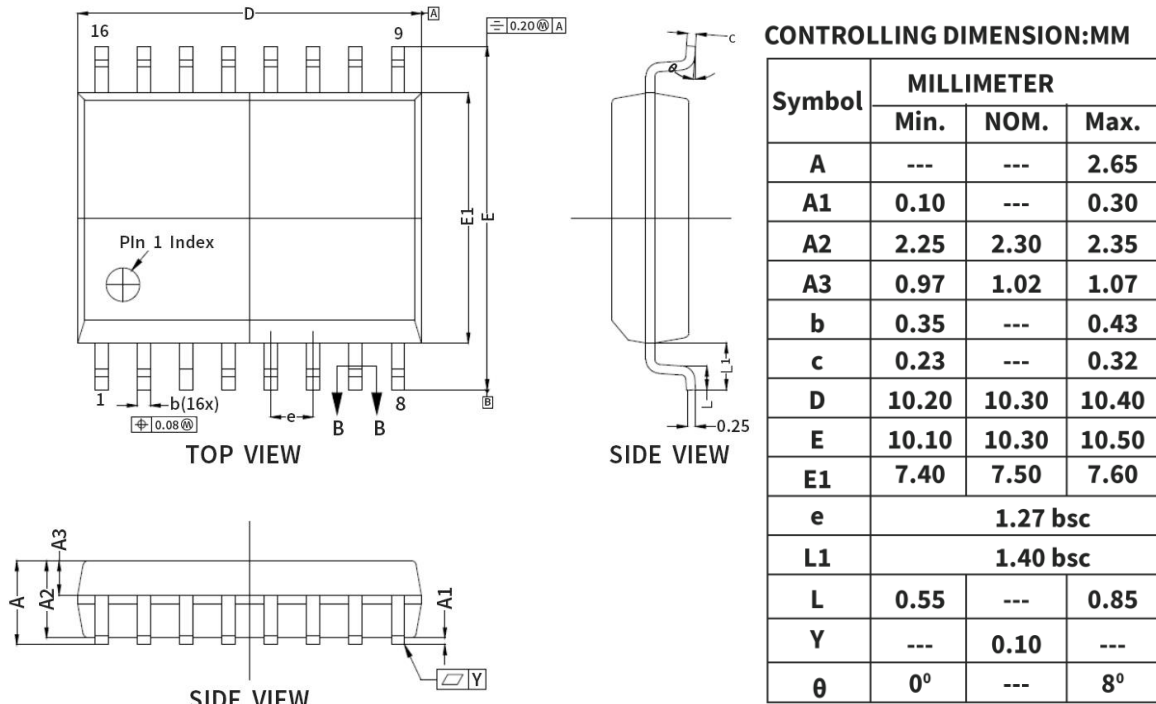


Figure 8.1 SOW16 Package Shape and Dimension in millimeters

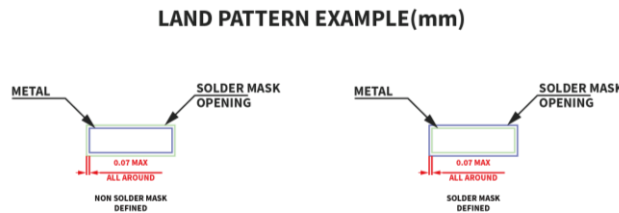
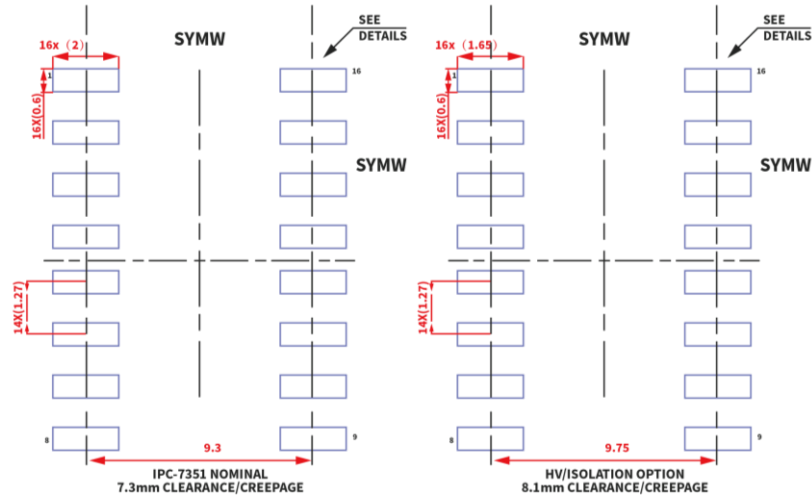
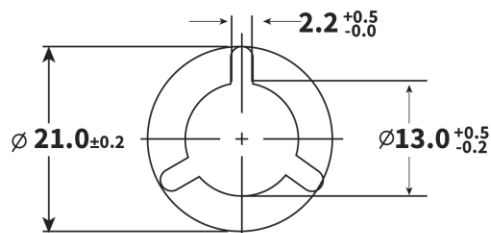
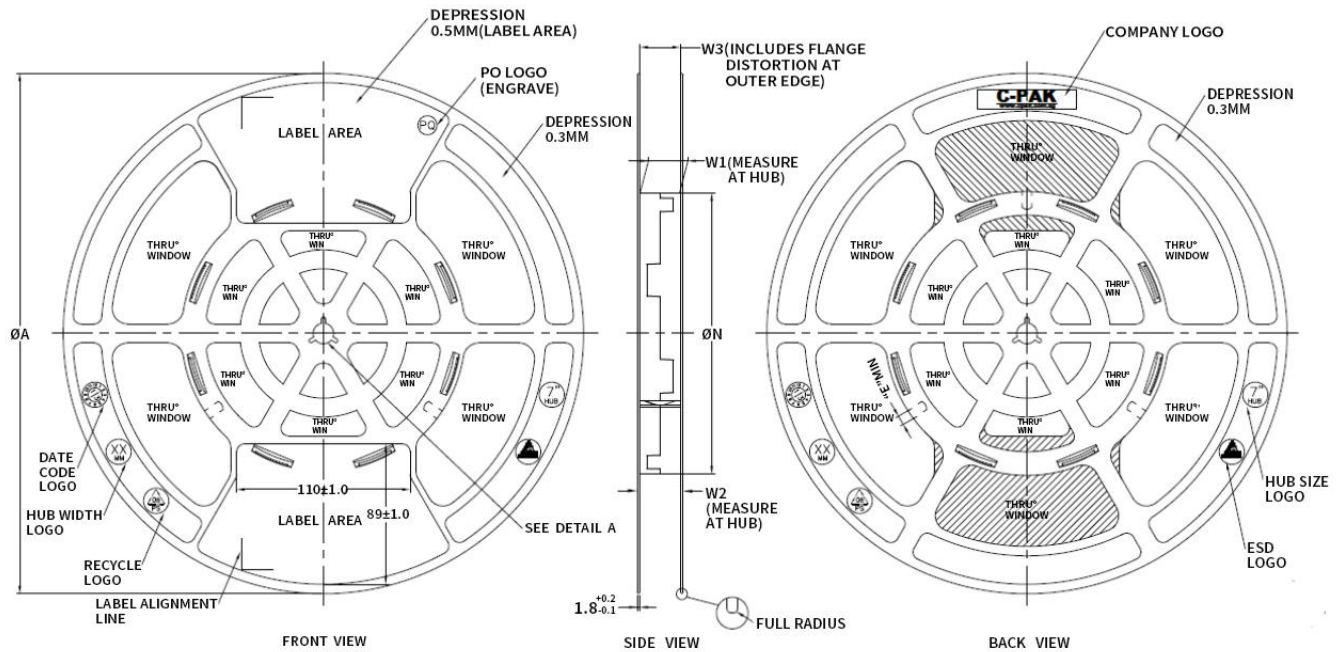


Figure 8.2 SOW16 Package Board Layout Example

9. Order Information

<i>Part Number</i>	<i>Isolation Rating (kV)</i>	<i>Duplex</i>	<i>Max Data Rate (Mbps)</i>	<i>No. of Nodes</i>	<i>Temperature</i>	<i>MSL</i>	<i>Package Type</i>	<i>Package Drawing</i>	<i>SPQ</i>
NSi83085E-DSWR	5	Half	12	256	-40 to 105°C	2	SOP16 (300mil)	SOW16	1000
NSi83086E-DSWR	5	Full	16	256	-40 to 105°C	2	SOP16 (300mil)	SOW16	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.									

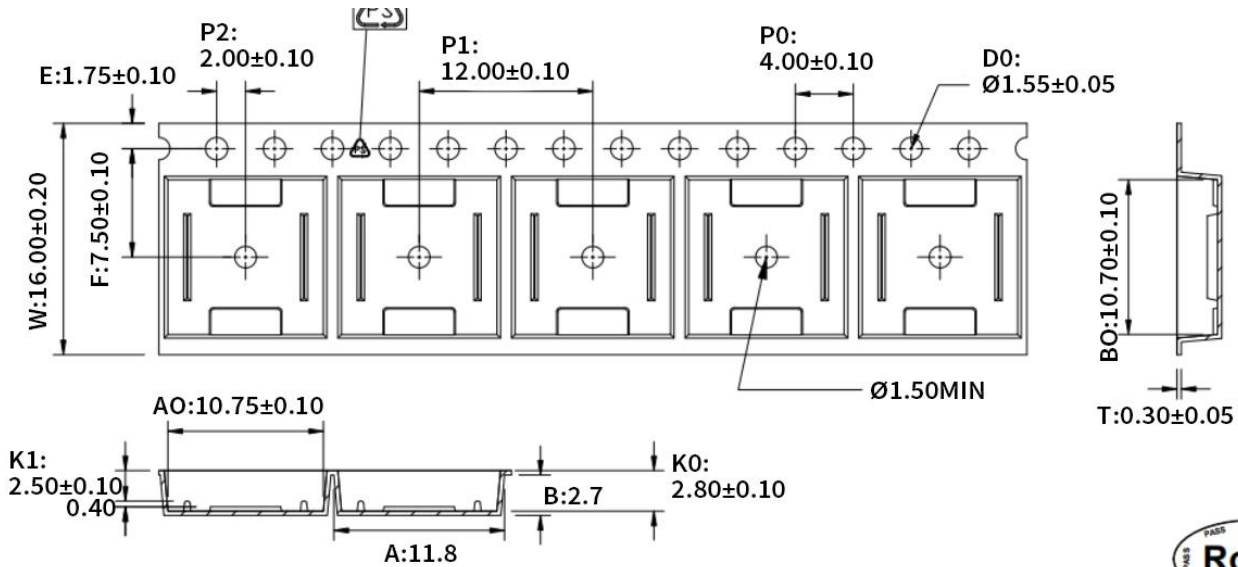
10. Tape and Reel Information



**ARBOR HOLE
DETAIL A
SCALE: 3:1**

PRODUCT SPECIFICATION						
TAPE WIDTH	$\varnothing A$ ± 2.0	$\varnothing N$ ± 2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	$8.4^{+1.5}_{-0.0}$	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	$12.4^{+2.0}_{-0.0}$	18.4		5.5
16MM	330	178	$16.4^{+2.0}_{-0.0}$	22.4		5.5
24MM	330	178	$24.4^{+2.0}_{-0.0}$	30.4		5.5
32MM	330	178	$32.4^{+2.0}_{-0.0}$	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^6 TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^5 & BELOW 10^5	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^9 TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



- 1.10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(復卷 N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity: 10⁵~ 10¹⁰Ω/□

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

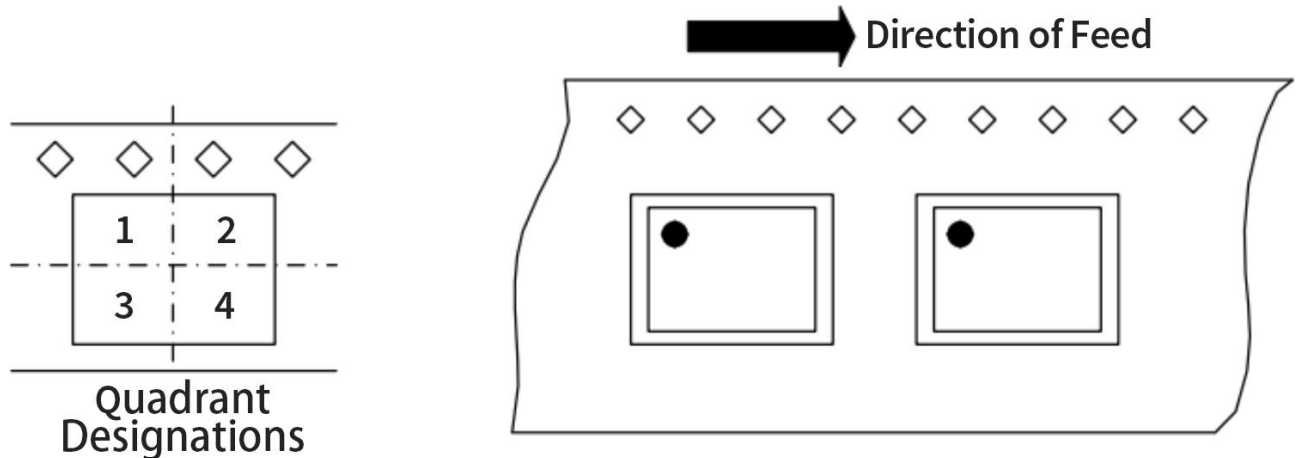


Figure 10.1 Tape and Reel Information of SOW16

11. Revision History

<i>Revision</i>	<i>Description</i>	<i>Date</i>
1.0	Initial version	2021/7/21
1.1	Add Junction Temperature, change PIN7 to NC	2022/4/25
1.2	Update Storage Temperature, Specifications, Regulatory information, land pattern. Update VIT in 2. Absolute Maximum Ratings. Update Reciever Function Table.	2022/10/12

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