

**ISD Cortex™-M0 Audio SOC**  
**ISD91200 Series**  
**Datasheet**

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## 1 GENERAL DESCRIPTION

The ISD91200 series is a system-on-chip product optimized for low power, audio record and playback with an embedded ARM® Cortex™-M0 32-bit microcontroller core.

The ISD91200 device embeds a Cortex™-M0 core running up to 50 MHz with 64K/128K byte of non-volatile flash memory and 12K-byte of embedded SRAM. It also comes equipped with a variety of peripheral devices, such as Timers, Watchdog Timer (WDT), Real-time Clock (RTC), Peripheral Direct Memory Access (PDMA), a variety of serial interfaces (UART, SPI/SSP, I<sup>2</sup>C, I<sup>2</sup>S), PWM modulators, GPIO, LDO, SDADC, SARADC, DPWM, Low Voltage Detector and Brown-out detector.

The ISD91200 comes equipped with a rich set of power saving modes including a Deep Power Down (DPD) mode drawing less than 1μA. A micro-power 10KHz oscillator can periodically wake up the device from deep power down to check for other events. Standby Power Down (SPD) mode can maintain a real time clock function with less than 5 μA.

For audio functionality the ISD91200 includes a Sigma-Delta ADC with 91dB SNR performance coupled with a Programmable Gain Amplifier (PGA with 0-6/12dB gain) and volume control (36dB to -108dB) in digital domain to enable direct connection of a microphone. Audio output is provided by a Differential Class D amplifier (DPWM) that can deliver 0.5W of power to an 8Ω speaker.

The ISD91200 provides eight analog enabled general purpose IO pins (GPIO). These pins can be configured to connect to an analog comparator, can be configured as analog current sources or can be routed to the SDADC for analog conversion. They can also be used as a relaxation oscillator to perform capacitive touch sensing.

## 2 FEATURES

- Core
  - ARM® Cortex™-M0 core running up to 50 MHz for normal speed.
  - One 24-bit System tick timer for operating system support.
  - Supports a variety of low power sleep and power down modes.
  - Single-cycle 32-bit hardware multiplier.
  - NVIC (Nested Vector Interrupt Controller) for 32 interrupt inputs, each with 4-levels of priority.
  - Serial Wire Debug (SWD) supports with 2 watchpoints/4 breakpoints.
- Power Management
  - Wide operating voltage range from 1.8V to 5.5V.
  - Power management Unit (PMU) providing four levels of power control.
  - Deep Power Down (DPD) mode with sub micro-amp leakage (<2μA).
  - Wakeup from Deep Power Down via dedicated WAKEUP pin or timed operation from internal low power 10KHz oscillator.
  - Standby current in SPD mode with limited RAM (256byte SBRAM) retention and RTC operation <5μA.
  - Standby current in STOP mode with full SRAM retention <10μA.
  - Wakeup from Standby can be from any GPIO interrupt, RTC or BOD.
  - Sleep mode with minimal dynamic power consumption.
  - 3V LDO for operation of external 3V devices such as serial flash.
- Flash EPROM Memory
  - 64K/128K bytes Flash EPROM for program code and data storage.
  - Mini-cache to maintain near zero-wait state memory access.
  - Support In-system program (ISP) and In-circuit program (ICP) application code update
  - 512 byte page erase for flash.
  - Configurable boundary to delineate code and data flash.
  - Support 2 wire In-circuit Programming (ICP) update from SWD ICE interface
- SRAM Memory
  - 12K bytes embedded SRAM.
- Clock Control
  - High speed and low speed oscillators providing flexible selection for different applications. No external components necessary.
  - Built-in trimmable oscillator with range of 16-50MHz. Factory trimmed within 1% to settings of 49.152MHz and 32.768MHz. User trimmable with in-built frequency measurement block (OSCFM) using reference clock of 32kHz crystal or external reference source.
  - Ultra-low power (<1uA) 10kHz oscillator for watchdog and wakeup from power-down or sleep operation.
  - External 32kHz crystal input for RTC function and low power system operation.
  - External 12 MHz crystal input for precise timing operation.
- GPIO
  - Four I/O modes:
    - ◆ Quasi bi-direction
    - ◆ Push-Pull output
    - ◆ Open-Drain output
    - ◆ Input only with high impendence
  - Schmitt trigger input selectable.

- I/O pin can be configured as interrupt source with edge/level setting.
- Supports High Driver and High Sink IO mode.
- Capacitive Touch: 16
- Maximal 32 GPIO
  
- Audio Analog to Digital converter
  - Sigma Delta ADC with configurable decimation filter and 16 bit output.
  - 90dB Signal-to-Noise (SNR) performance.
  - Programmable gain amplifier with 32 steps from -12 to 35.25dB in 0.75dB steps.
  - Boost gain stage of 26dB, giving maximum total gain of 61dB.
  - Input selectable from dedicated MIC pins or analog enabled GPIO.
  - Programmable biquad filter to support multiple sample rates from 8-32kHz.
  - DMA support for minimal CPU intervention.
  
- Differential Audio PWM Output (DPWM)
  - Direct connection of speaker
  - 0.5W drive capability into 8 $\Omega$  load.
  - Configurable up-sampling to support sample rates from 8-48kHz.
  - Programmable volume control from -128dB to +36dB in 0.5 dB step
  - Programmable biquad filter to support multiple sample rates from 8-48kHz
  - DMA support for minimal CPU intervention.
  
- Timers
  - Two timers with 8-bit pre-scaler and 24-bit resolution.
  - Counter auto reload.
  
- Watch Dog Timer
  - Default ON/OFF by configuration setting
  - Multiple clock sources
  - 8 selectable time out period from micro seconds to seconds (depending on clock source)
  - WDT can wake up power down/sleep.
  - Interrupt or reset selectable on watchdog time-out.
  
- RTC
  - Real Time Clock counter (second, minute, hour) and calendar counter (day, month, year)
  - Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Time tick and alarm interrupts.
  - Device wake up function.
  - Supports software compensation of crystal frequency by compensation register (FCR)
  
- PWM/Capture
  - Four 16-bit PWM generators provide four single ended PWM outputs or two complementary paired PWM outputs.
  - The PWM generator equipped with a clock source selector, a clock divider, an 8-bit pre-scaler and Dead-Zone generator for complementary paired PWM.
  - PWM interrupt synchronous to PWM period.
  - 16-bit digital Capture timers (shared with PWM timers) provide rising/falling capture inputs.
  - Support Capture interrupt
  
- UART
  - Up to two uart controller
  - UART ports with flow control (TX, RX, CTS and RTS)

- 8-byte FIFO.
- Support IrDA (SIR) and LIN function
- Programmable baud-rate generator up to 1/16 of system clock.
- SPI
  - Up to two SPI controller
  - SPI Clock up to 24 MHz.
  - SPI data rate in Quad mode up to 98 Mbps
  - Support MICROWIRE/SPI master/slave mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 4 bytes
  - MSB or LSB first data transfer
  - 2 slave/device select lines when used in master mode.
  - DMA support.( 64bit (16x4) data FIFO)
  - Quad/Dual SPI support.
- I2C
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
  - Programmable clock allowing versatile rate control.
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up by address recognition (for 1st slave address only)
- I<sup>2</sup>S
  - Interface with external audio CODEC.
  - Operate as either master or slave.
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Mono and stereo audio data supported
  - I<sup>2</sup>S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports DMA requests, for transmit and receive
- SARADC
  - 12-bit SAR ADC with 350K SPS
  - Up to 10-ch single-end input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by software programming or external input
  - Supports PDMA mode
- Low Voltage Reset
  - Threshold voltage levels: 1.8V

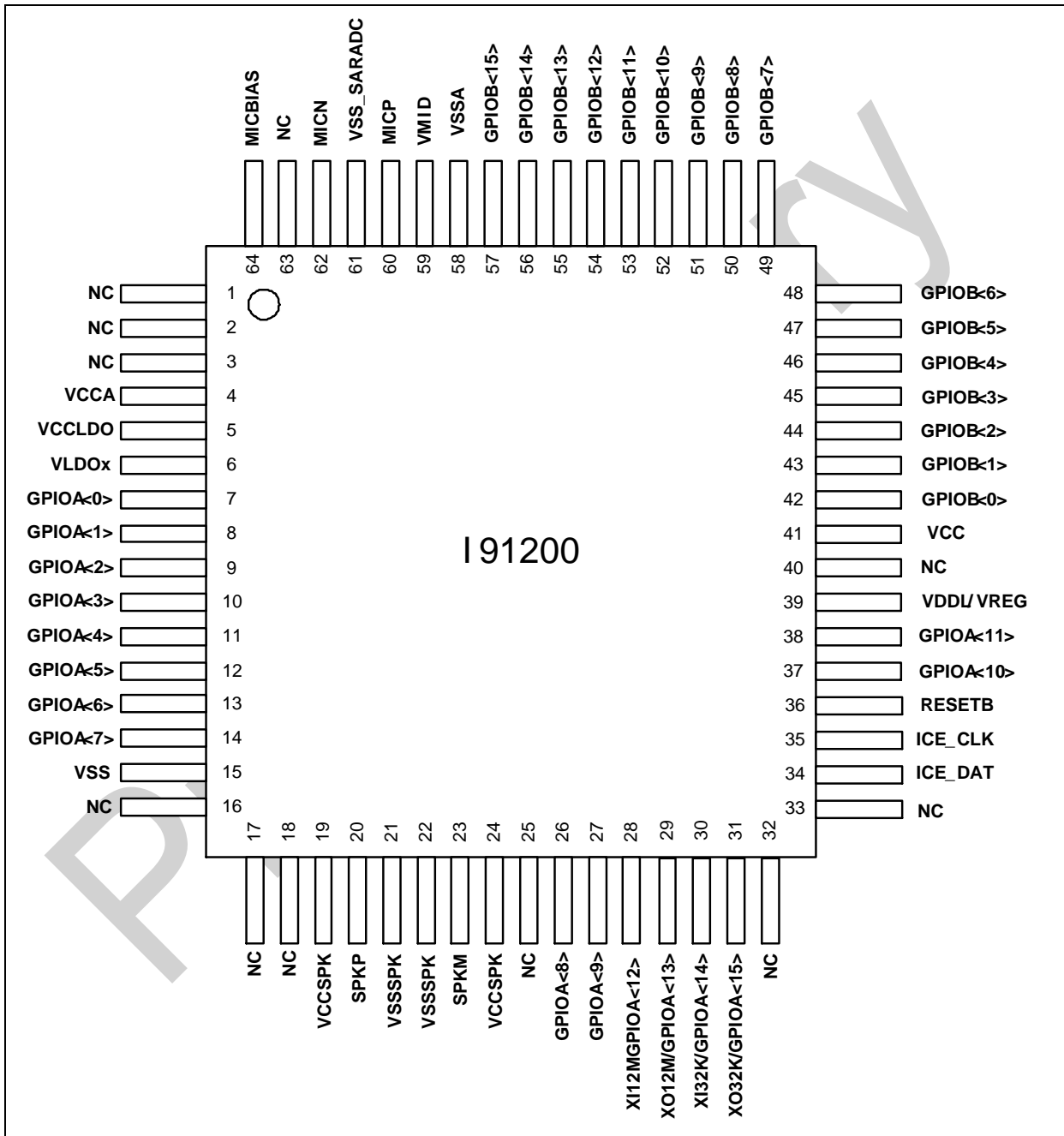
- Brown-out detector
  - Supports 8-level brown-out setting.
  - Supports time-multiplex operation to minimize power consumption.
  - Supports Brownout Interrupt and Reset option
- Built in Low Dropout Voltage Regulator (LDO)
  - Capable of delivering 30mA load current.
  - Configurable 8 output voltage selections from 1.5V – 3.3V.
  - LDO output powers IO ring for GPIOA<7:0> and can supply power to external SPI Flash.
  - Can be bypassed and voltage domain supplied directly from system power.
- Additional Features
  - Over temperature alarm. Can generate interrupt if device exceeds safe operating temperature.
  - Temperature proportional voltage source which can be routed to ADC for temperature measurements.
  - Digital Microphone interface.
  - 2 Low noise high impedance high working temperature OPAMPs suitable for smoke-detect application.
- Standby current in STOP mode with SRAM retention  $\leq 10\mu\text{A}$  at 25°C.
- Operating Temperature: -40C~85C
- Package:
  - All Green package (RoHS)
    - ◆ LQFP 64-pin

Preliminary

## 3 PART INFORMATION AND PIN CONFIGURATION

### 3.1 Pin Configuration

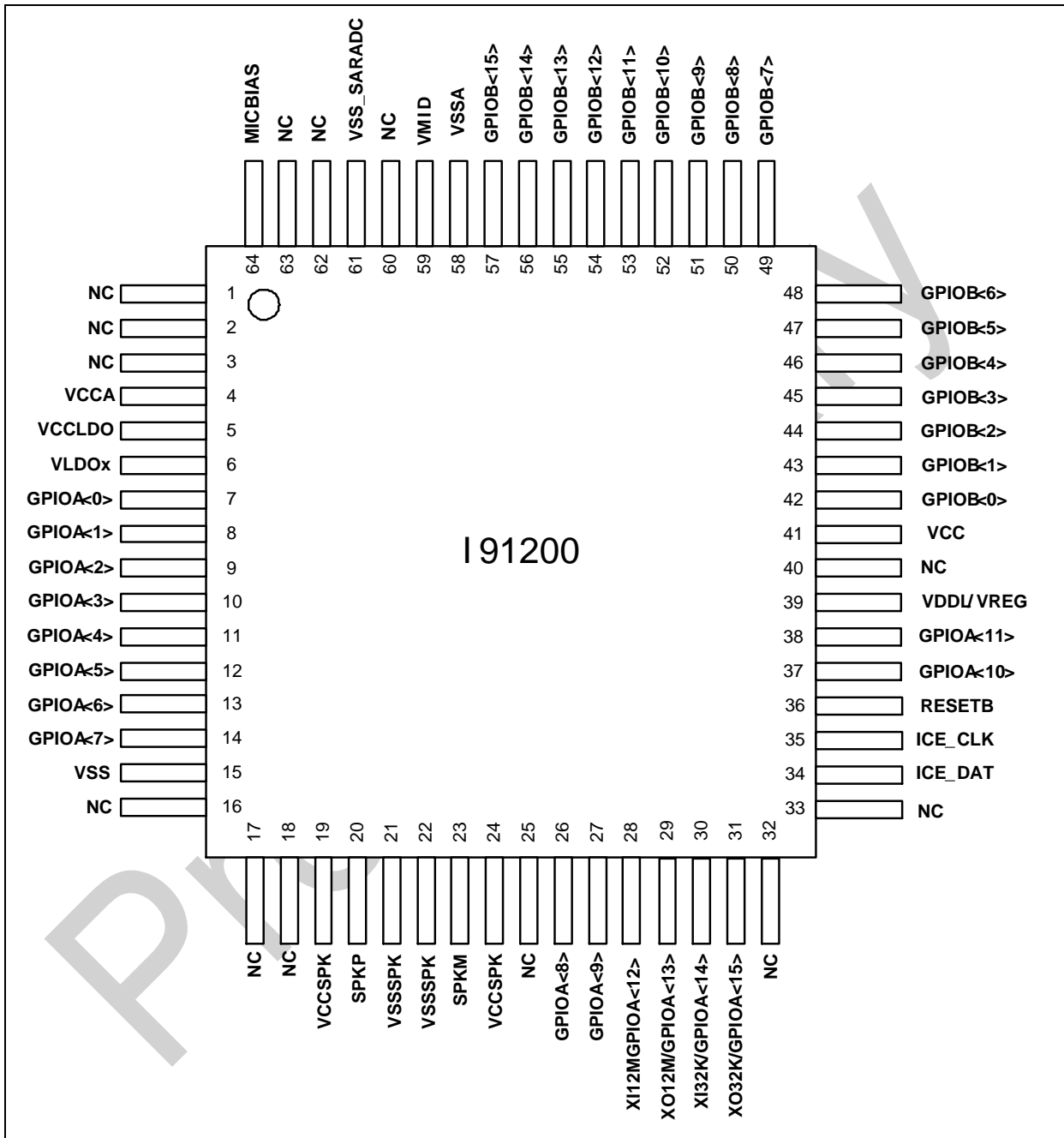
#### 3.1.1 ISD91200 LQFP 64 pin (Normal & C series)





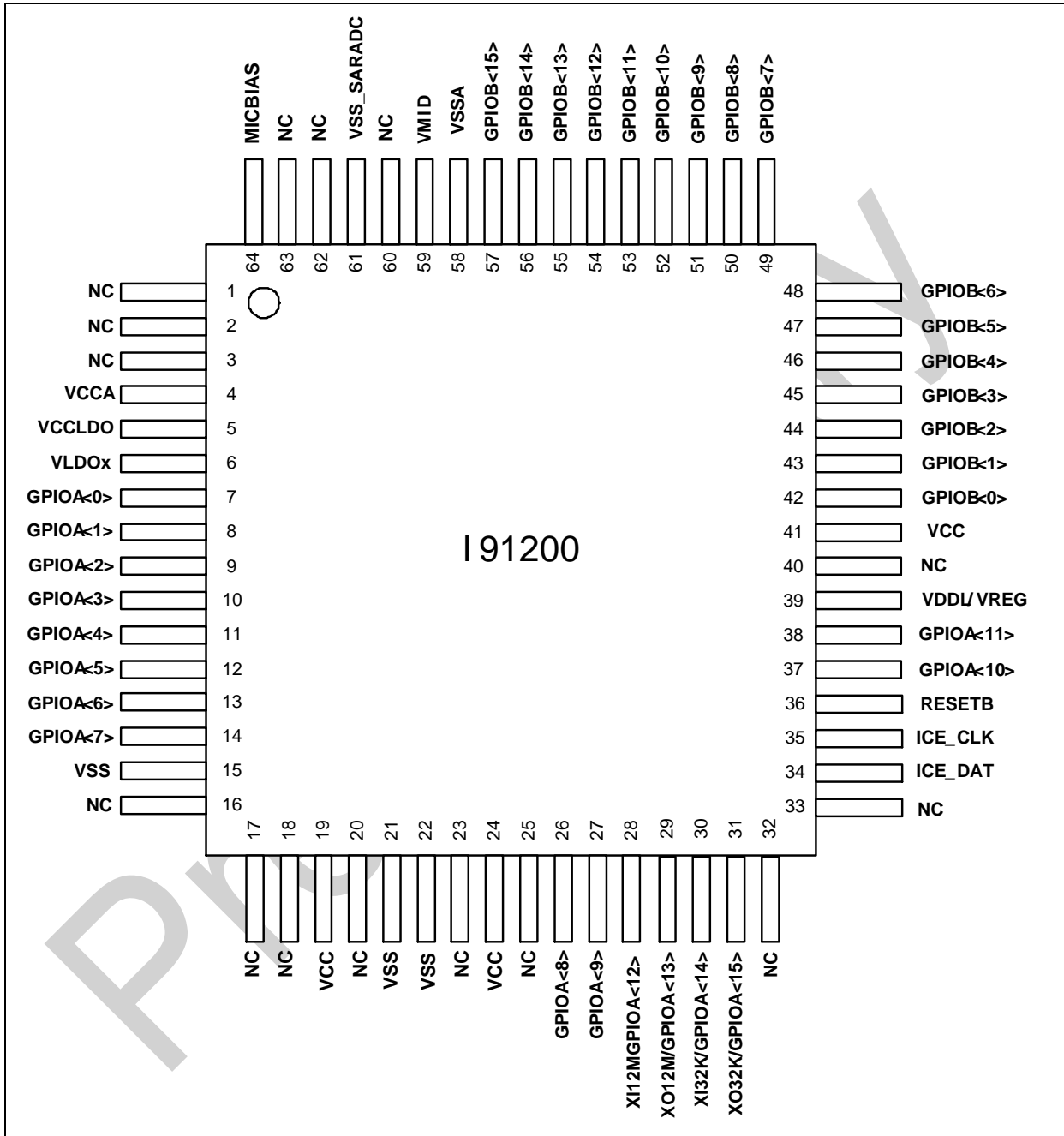
## 3.1.2 ISD91200 LQFP 64 pin (P series)

Basic feature & play-back only



### 3.1.3 ISD91200 LQFP 64 pin (G series)

Basic feature, no MIC & SPK supported



### 3.2 Pin Description

The ISD91200 is a low pin count device where many pins are configurable to alternative functions. All General Purpose Input/Output (GPIO) pins can be configured to alternate functions as described in the tables below.

Pin No.	Pin Name	Pin Type	Alt CFG	Description
LQFP 64				
1	NC			
2	NC			
3	NC			
4	VCCA	P		Analog power supply.
5	VCCLDO	P		Power supply for LDO, should be connected to VCCD.
6	VLDOx	P		LDO regulator output. if used, a 1 $\mu$ F decoupling capacitor must be placed. If not used then tie to VCCD.
7	PA.0	I/O	0	General purpose input/output pin; Port A, bit 0
	SPI0_MISO1	O	1	2nd Master In, Slave Out for SPI0 interface
	SPI0_SSB1	O	2	Slave Select Bar 1 for SPI0 interface
	I2S0_FS	I/O	3	Frame Sync Clock for I2S interface
8	PA.1	I/O	0	General purpose input/output pin; Port A, bit 1
	SPI0_MOSI0	O	1	1st Master Out, Slave In for SPI0 interface
	I2S0_BCLK	I/O	3	Bit Clock for I2S interface
9	PA.2	I/O	0	General purpose input/output pin; Port A, bit 2
	SPI0_SCLK0	I/O	1	Serial Clock for SPI0 interface
	DMIC_DAT	I	2	DMIC data
	I2S0_SDI	I	3	Serial Data Input for I2S interface
10	PA.3	I/O	0	General purpose input/output pin; Port A, bit 3
	SPI0_SSB0	O	1	Slave Select Bar 0 for SPI0 interface
	SARADC_TRIG	I	2	SARADC Trigger
	I2S0_SDO	O	3	Serial Data Output for I2S interface
11	PA.4	I/O	0	General purpose input/output pin; Port A, bit 4
	SPI0_MISO0	O	1	Master In, Slave Out channel 0 for SPI interface
	UART0_TX	O	2	Transmit channel of UART 0
	SPI1_MOSI	O	3	Master Out, Slave In for SPI1 interface
12	PA.5	I/O	0	General purpose input/output pin; Port A, bit 5
	SPI0_MOSI1	O	1	2nd Master Out, Slave In for SPI0 interface
	UART0_RX	I	2	Receive channel of UART 0
	SPI1_SCLK	I/O	3	Serial Clock for SPI1 interface
13	PA.6	I/O	0	General purpose input/output pin; Port A, bit 6
	UART0_TX	O	1	Transmit channel of UART 0
	I2C0_SDA	I/O	2	Serial Data, I2C interface
	SPI1_SSB	O	3	Slave Select Bar for SPI1 interface
14	PA.7	I/O	0	General purpose input/output pin; Port A, bit 7
	UART0_RX	I	1	Receive channel of UART 0
	I2C0_SCL	I/O	2	Serial Clock, I2C interface
	SPI1_MISO	I	3	Master In, Slave Out for SPI1 interface
15	VSSD	P		Digital Ground.

Pin No.	Pin Name	Pin Type	Alt CFG	Description
LQFP 64				
16	NC			
17	NC			
18	NC			
19	VCCSPK	P		Power Supply for PWM Speaker Driver. Need VCC connection for G series.
20	SPKP	O		Positive Speaker Driver Output. Not support for G series.
21	VSSSPK	P		Ground for PWM Speaker Driver. Need VSS connection for G series.
22	VSSSPK	P		Ground for PWM Speaker Driver. Need VSS connection for G series.
23	SPKN	O		Positive Speaker Driver Output. Not support for G series.
24	VCCSPK	P		Power Supply for PWM Speaker Driver. Need VCC connection for G series.
25	NC			
26	PA.8	I/O	0	General purpose input/output pin; Port A, bit 8
	I2C0_SDA	I/O	1	Serial Data, I2C interface
	UART1_TX	O	2	Transmit channel of UART 1
	UART0_RTS	O	3	UART 0 Request to Send Output.
27	PA.9	I/O	0	General purpose input/output pin; Port A, bit 9
	I2C0_SCL	I/O	1	Serial Clock, I2C interface
	UART1_RX	I	2	Receive channel of UART 1
	UART0_CTS	I	3	UART 0 Clear to Send Input.
28	I2C0_SCL	I/O	3	Serial Clock, I2C interface
	PA.12	I/O	0	General purpose input/output pin; Port A, bit 12
	PWM0CH2	O	1	PWM0CH2 Output.
	XI12M	I	2	12MHz Crystal Oscillator Input. Max Voltage 1.8V
29	PA.13	I/O	0	General purpose input/output pin; Port A, bit 13
	PWM0CH3	O	1	PWM0CH3 Output.
	XO12M	O	2	12MHz Crystal Oscillator Output
	I2C0_SCL	I/O	3	Serial Clock, I2C interface
30	PA.14	I/O	0	General purpose input/output pin; Port A, bit 14
	UART1_TX	O	1	Transmit channel of UART 1
	DMIC_CLK	IO	2	DMIC clock
	XI32K	I	3	32.768kHz Crystal Oscillator Input. Max Voltage 1.8V
31	PA.15	I/O	0	General purpose input/output pin; Port A, bit 15
	UART1_RX	I	1	Receive channel of UART 1
	MCLK	O	2	Master clock output for synchronizing external device
	XO32K	O	3	32.768kHz Crystal Oscillator Output
32	NC			
33	NC			
34	ICE_DAT	I/O		Serial Wire Debug port clock pin. Has internal weak pull-up.

Pin No.	Pin Name	Pin Type	Alt CFG	Description
LQFP 64				
35	ICE_CLK	O		Serial Wire Debug port data pin. Has internal weak pull-up.
36	RESETN	I		External reset input. Pull this pin low to reset device to initial state. Has internal weak pull-up.
37	PA.10	I/O	0	General purpose input/output pin; Port A, bit 10
	PWM0CH0	O	1	PWM0CH0 Output.
	TM0	I	2	External input to Timer 0
	DPWM_P	O	3	Audio PWM positive
38	PA.11	I/O	0	General purpose input/output pin; Port A, bit 11
	PWM0CH1	O	1	PWM0CH1 Output.
	TM1	I	2	External input to Timer 1
	DPWM_N	O	3	Audio PWM negative
39	VREG	P		Logic regulator output decoupling pin. A 1 $\mu$ F capacitor returning to VSSD must be placed on this pin.
40	NC			
41	VCCD	P		Main Digital Supply for Chip. Supplies all IO except analog, Speaker Driver
42	PB.0	I/O	0	General purpose input/output pin, analog capable; Port B, bit 0. Triggers external interrupt 0 (EINT0/IRQ2)
	SPI1_MOSI	O	1	Master Out, Slave In for SPI1 interface
	CS0	AI		Touch scan channel 0
	A0P	AI		Operational Amplifier 0 positive input
43	PB.1	I/O	0	General purpose input/output pin, analog capable; Port B, bit 1. Triggers external interrupt 1 (EINT1/IRQ3)
	SP1_SCLK	I/O	1	Serial Clock for SPI1 interface
	CS1	AI		Touch scan channel 1
	A0N	AI		Operational Amplifier 0 negative input
44	PB.2	I/O	0	General purpose input/output pin, analog capable; Port B, bit 2
	SPI1_SSB	O	1	Slave Select Bar for SPI1 interface
	CS2	AI		Touch scan channel 1
	A0E	AO		Operational Amplifier 0 output
	SAR11	AI		SARADC channel 11
45	PB.3	I/O	0	General purpose input/output pin, analog capable; Port B, bit 3
	SPI1_MISO	I	1	Master In, Slave Out for SPI1 interface
	CS3	AI		Touch scan channel 3
	A1P	AI		Operational Amplifier 1 positive input
46	PB.4	I/O	0	General purpose input/output pin, analog capable; Port B, bit 4
	I2S0_FS	I/O	1	Frame Sync Clock for I2S interface
	CS4	AI		Touch scan channel 4
	A1N	AO		Operational Amplifier 1 negative input

Pin No.	Pin Name	Pin Type	Alt CFG	Description
47	PB.5	I/O	0	General purpose input/output pin, analog capable; Port B, bit 5
	I2S0_BCLK	I/O	1	Bit Clock for I2S interface
	CS5	AI		Touch scan channel 5
	A1E	AO		Operational Amplifier 1 output
	SAR10	AI		SARADC channel 10
48	PB.6	I/O	0	General purpose input/output pin, analog capable; Port B, bit 6
	I2S0_SDI	I	1	Serial Data Input for I2S interface
	CS6	AI		Touch scan channel 6
	CNP	AI		Comparator 1 positive input and comparator 2 negative input
	SAR8	AI		SARADC channel 8
49	PB.7	I/O	0	General purpose input/output pin, analog capable; Port B, bit 7
	I2S0_SDO	O	1	Serial Data Output for I2S interface
	CS7	AI		Touch scan channel 7
	C1N	AI		Comparator 1 negative input
	SAR9	AI		SARADC channel 9
50	PB.8	I/O	0	General purpose input/output pin, analog capable; Port B, bit 8.
	I2C0_SDA	I/O	1	Serial Data, I2C interface
	I2S0_FS	I/O	2	Frame Sync Clock for I2S interface
	UART1_RTS	O	3	UART 1 Request to Send Output.
	CS8	AI		Touch scan channel 8
	C2P	AI		Comparator 2 positive input
	SAR0	AI		SARADC channel 0
51	PB.9	I/O	0	General purpose input/output pin, analog capable; Port B, bit 9.
	I2C0_SCL	I/O	1	Serial Clock, I2C interface
	I2S0_BCLK	I/O	2	Bit Clock for I2S interface
	UART1_CTS	I	3	UART 1 Clear to Send Input.
	CS9	AI		Touch scan channel 9
	SAR1	AI		SARADC channel 1
52	PB.10	I/O	0	General purpose input/output pin, analog capable; Port B, bit 10
	CMP1	O	1	Compare 1 Output
	I2S0_SDI	I	2	Serial Data Input for I2S interface
	UART1_TX	O	3	Transmit channel of UART 1
	CS10	AI		Touch scan channel 10
	SAR2	AI		SARADC channel 2
53	PB.11	I/O	0	General purpose input/output pin, analog capable; Port B, bit 11
	CMP2	O	1	Compare 2 Output
	I2S0_SDO	O	2	Serial Data Output for I2S interface
	UART1_RX	I	3	Receive channel of UART 1

Pin No.	Pin Name	Pin Type	Alt CFG	Description
LQFP 64	CS11	AI		Touch scan channel 11
	SAR3	AI		SARADC channel 3
54	PB.12	I/O	0	General purpose input/output pin, analog capable; Port B, bit 12
	SPI0_MISO0	I/O	1	1st Master In, Slave Out for SPI0 interface
	SPI1_MOSI	I/O	2	Master Out, Slave In for SPI1 interface
	DMIC_DAT	I	3	DMIC data
	CS12	AI		Touch scan channel 12
	SAR4	AI		SARADC channel 4
55	PB.13	I/O	0	General purpose input/output pin, analog capable; Port B, bit 13
	SPI0_MOSIO	I/O	1	1st Master Out, Slave In for SPI0 interface
	SPI1_SCLK	I/O	2	Serial Clock for SPI1 interface
	SARADC_TRIG	I	3	SARADC Trigger
	CS13	AI		Touch scan channel 13
	SAR5	AI		SARADC channel 5
56	PB.14	I/O	0	General purpose input/output pin, analog capable; Port B, bit 14
	SPI0_SCLK0	I/O	1	1st Serial Clock for SPI0 interface
	SPI1_SSB	O	2	Slave Select Bar 1 for SPI1 interface
	DMIC_CLK	O	3	DMIC clock
	CS14	AI		Touch scan channel 14
	SAR6	AI		SARADC channel 6
57	PB.15	I/O	0	General purpose input/output pin, analog capable; Port B, bit 15
	SPI0_SSB0	O	1	Slave Select Bar 0 for SPI0 interface
	SPI1_MISO	I/O	2	Master In, Slave Out for SPI1 interface
	MCLK	O	3	Master clock output for synchronizing external device
	CS15	AI		Touch scan channel 15
	SAR7	AI		SARADC channel 7
58	VSSA	AP		Ground for analog circuitry.
59	VMID	O		Mid rail reference. Connect 4.7μF to VSSA.
60	MICP	AI		SDADC positive input. Not support for G & P series.
61	VSS_SARADC	AP		SARADC ground
62	MICN	AI		SDADC negative input. Not support for G & P series.
63	NC			
64	MICBIAS	O		Microphone bias output. Only support SARADC VREF for G & P series.

Note:

- Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; AO=Analog Output; P=Power Pin; AP=Analog Power

## 4 BLOCK DIAGRAM

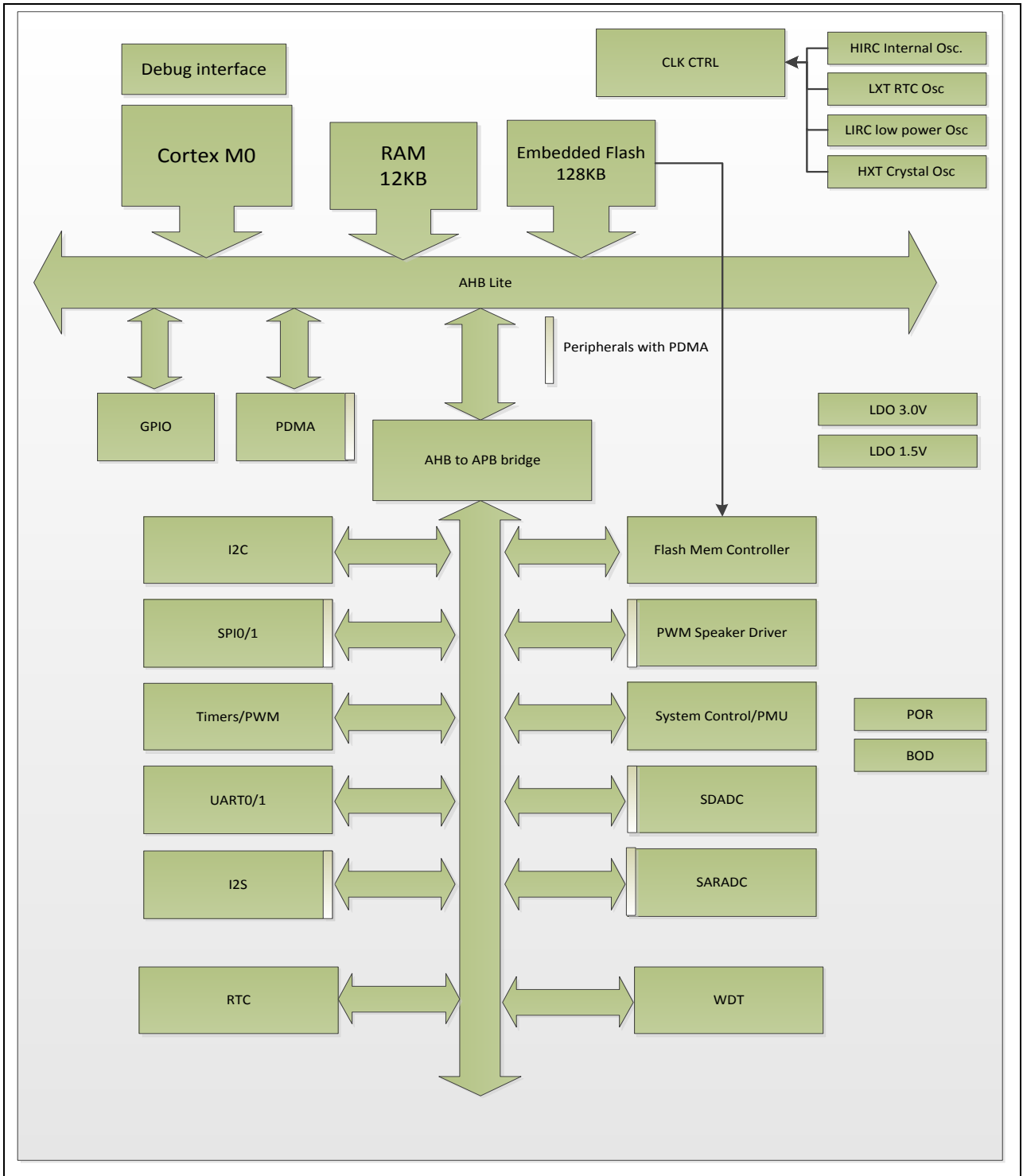
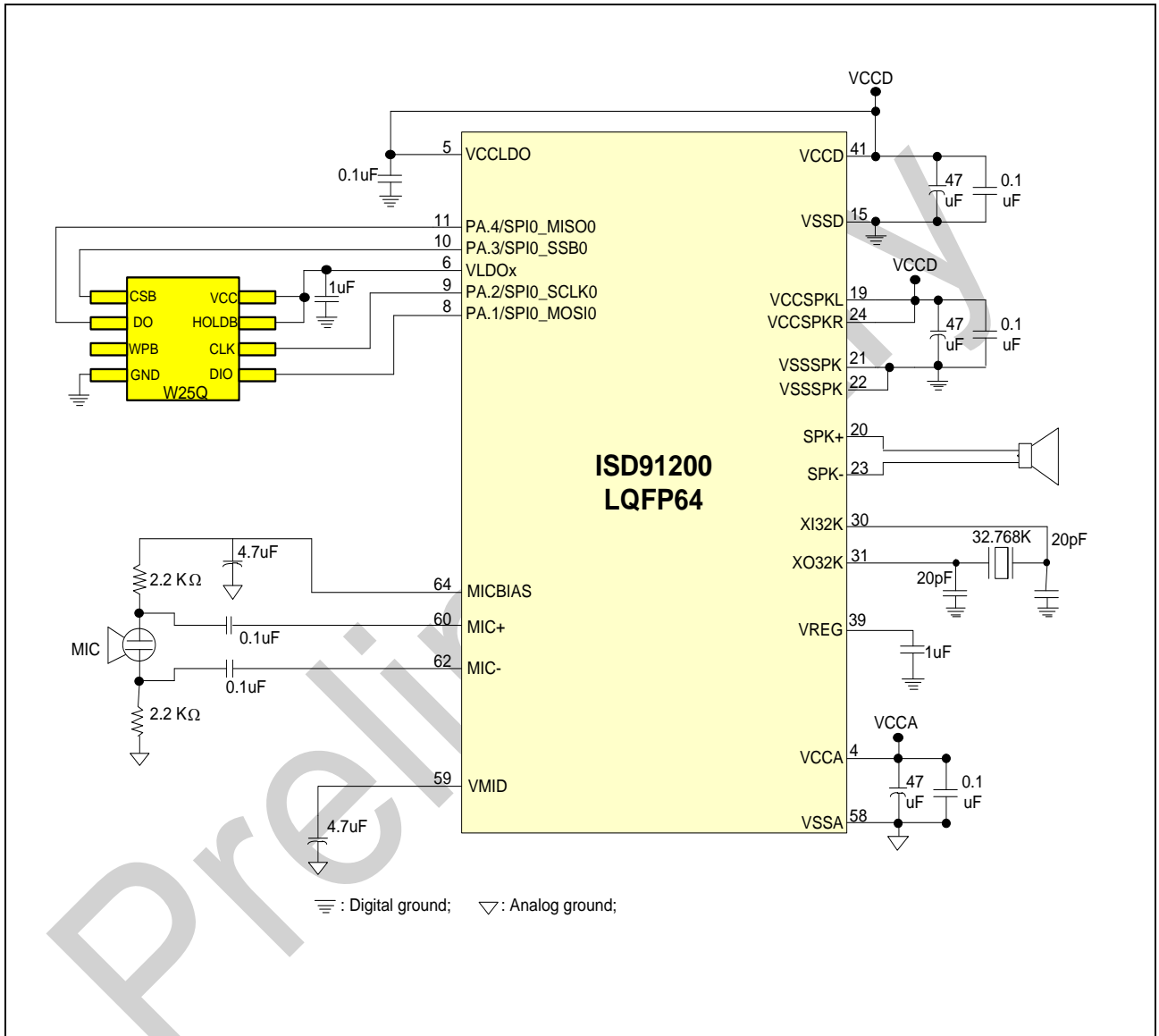


Figure 4-1 ISD91200 Block Diagram



## 5 APPLICATION DIAGRAM



**Note:**

1. For SPI flash quad mode access, disconnect HOLDB & WPB from VDDDB, then connect HOLDB to PA.0 and WPB to PA.5.

## 6 ELECTRICAL CHARACTERISTICS

### 6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD-VSS	-0.3	+6.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	1/t <sub>CLCL</sub>	0	40	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V <sub>DD</sub>		-	120	mA
Maximum Current out of V <sub>SS</sub>			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

## 6.2 DC Electrical Characteristics

(V<sub>DD</sub>-V<sub>SS</sub>=3.3V, T<sub>A</sub> = 25°C, F<sub>OSC</sub> = 49.152 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V <sub>DD</sub>	1.8		5.5	V	V <sub>DD</sub> = 1.8V ~ 5.5V up to 50 MHz
Power Ground	V <sub>SS</sub> AV <sub>SS</sub>	-0.3			V	
LDO Output Voltage	V <sub>LDO</sub>	-10%	1.5	+10%	V	V <sub>DD</sub> > 1.8V
Analog Operating Voltage	AV <sub>DD</sub>	0		V <sub>DD</sub>	V	
Analog Reference Voltage	V <sub>ref</sub>	0		AV <sub>DD</sub>	V	
Operating Current Normal Run Mode @ 50Mhz	I <sub>DD1</sub>		50		mA	V <sub>DD</sub> = 5.5V@50Mhz, enable all IP, XTAL=12MHz
	I <sub>DD2</sub>		33		mA	V <sub>DD</sub> =5.5V@50Mhz, disable all IP, XTAL=12MHz
	I <sub>DD3</sub>		45		mA	V <sub>DD</sub> = 3V@50Mhz, enable all IP, XTAL=12MHz
	I <sub>DD4</sub>		27		mA	V <sub>DD</sub> = 3V@50Mhz, disable all IP, XTAL=12MHz
Operating Current Normal Run Mode @ 12Mhz	I <sub>DD5</sub>		22		mA	V <sub>DD</sub> = 5.5V@12Mhz, enable all IP a, XTAL=12MHz
	I <sub>DD6</sub>		15		mA	V <sub>DD</sub> = 5.5V@12Mhz, disable all IP XTAL=12MHz
	I <sub>DD7</sub>		20		mA	V <sub>DD</sub> = 3V@12Mhz, enable all IP, XTAL=12MHz
	I <sub>DD8</sub>		12		mA	V <sub>DD</sub> = 3V@12Mhz, disable all IP, XTAL=12MHz

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Operating Current Normal Run Mode @ 4Mhz	I <sub>DD9</sub>	5.8	MA	V <sub>DD</sub> = 5V@4Mhz, Enable All IP, XTAL=4MHz
	I <sub>DD10</sub>	4.2	mA	V <sub>DD</sub> = 5V@4Mhz, disable all IP, XTAL=4MHz
	I <sub>DD11</sub>	5.1	mA	V <sub>DD</sub> = 3V@4Mhz, enable all IP, XTAL=4MHz
	I <sub>DD12</sub>	3.6	mA	V <sub>DD</sub> = 3V@4Mhz, disable all IP, XTAL=4MHz
Operating Current Idle Mode @ 50Mhz	I <sub>IDLE1</sub>	35	mA	V <sub>DD</sub> = 5.5V@50Mhz, enable all IP, XTAL=12MHz
	I <sub>IDLE2</sub>	15	mA	V <sub>DD</sub> =5.5V@50Mhz, disable all IP, XTAL=12MHz
	I <sub>IDLE3</sub>	34	mA	V <sub>DD</sub> = 3V@50Mhz, enable all IP, XTAL=12MHz
	I <sub>IDLE4</sub>	13	mA	V <sub>DD</sub> = 3V@50Mhz, disable all IP a XTAL=12MHz
Operating Current Idle Mode @ 12Mhz	I <sub>IDLE5</sub>	14	mA	V <sub>DD</sub> = 5.5V@12Mhz, enable all IP XTAL=12MHz
	I <sub>IDLE6</sub>	5	mA	V <sub>DD</sub> = 5.5V@12Mhz, disable all IP XTAL=12MHz
	I <sub>IDLE7</sub>	12	mA	V <sub>DD</sub> = 3V@12Mhz, enable all IP, XTAL=12MHz
	I <sub>IDLE8</sub>	4	mA	V <sub>DD</sub> = 3V@12Mhz, disable all IP, XTAL=12MHz
Operating Current Idle Mode @ 4Mhz	I <sub>IDLE9</sub>	3.4	mA	V <sub>DD</sub> = 5V@4Mhz, enable all IP XTAL=4MHz
	I <sub>IDLE10</sub>	1.8	mA	V <sub>DD</sub> = 5V@4Mhz, disable all IP XTAL=4MHz
	I <sub>IDLE11</sub>	2.8	mA	V <sub>DD</sub> = 3V@4Mhz, enable all IP, XTAL=4MHz
	I <sub>IDLE12</sub>	1.2	mA	V <sub>DD</sub> = 3V@4Mhz, disable all IP, XTAL=4MHz

Supply Current at STOP Mode (special characteristic)	ISTOP		10		μA	XTAL32K ON; RTC OFF; NO LOAD
Supply Current at Standby Power Down Mode	ISPD		5		μA	XTAL32K ON; RTC ON; NO LOAD
Supply Current at Deep Sleep	IDSLP		200		μA	XTAL32K ON; RTC OFF; NO LOAD
Supply Current Sleep Mode	ISLP		6		mA	
Supply Current at Deep Power Down Mode	IDPD		2		μA	Wakeup with Wakeup Pin
Input Current PA, PB, (Quasi-bidirectional mode)	I <sub>IN1</sub>	-75	-	+15	μA	V <sub>DD</sub> = 5.5V, V <sub>IN</sub> = 0V or V <sub>IN</sub> =V <sub>DD</sub>
Input Current at /RESET <sup>[1]</sup>	I <sub>IN2</sub>	-75	-45	-30	μA	V <sub>DD</sub> = 3.3V, V <sub>IN</sub> = 0.45V
Input Leakage Current PA, PB,	I <sub>LK</sub>	-2	-	+2	μA	V <sub>DD</sub> = 5.5V, 0<V <sub>IN</sub> <V <sub>DD</sub>
Logic 1 to 0 Transition Current PA~PB (Quasi-bidirectional mode)	I <sub>TL</sub> <sup>[3]</sup>	-650	-	-200	μA	V <sub>DD</sub> = 5.5V, V <sub>IN</sub> <2.0V
Input Low Voltage PA, PB (TTL input)	V <sub>IL1</sub>	-0.3	-	0.8	V	V <sub>DD</sub> = 4.5V
		-0.3	-	0.6		V <sub>DD</sub> = 2.5V
Input High Voltage PA, PB (TTL input)	V <sub>IH1</sub>	2.0	-	V <sub>DD</sub> +0.2	V	V <sub>DD</sub> = 5.5V
		1.5	-	V <sub>DD</sub> +0.2		V <sub>DD</sub> = 3.0V
Input Low Voltage XT1 <sup>[2]</sup>	V <sub>IL3</sub>	0	-	0.8	V	V <sub>DD</sub> = 4.5V
		0	-	0.4		V <sub>DD</sub> = 3.0V
Input High Voltage XT1 <sup>[2]</sup>	V <sub>IH3</sub>	3.5	-	V <sub>DD</sub> +0.2	V	V <sub>DD</sub> = 5.5V
		2.4	-	V <sub>DD</sub> +0.2		V <sub>DD</sub> = 3.0V
Input Low Voltage X321 <sup>[2]</sup>	V <sub>IL4</sub>	0	-	0.4	V	
Input High Voltage X321 <sup>[2]</sup>	V <sub>IH4</sub>	1.7		2.5	V	
Negative going threshold (Schmitt input), /REST	V <sub>ILS</sub>	-0.5	-	0.3V <sub>DD</sub>	V	
Positive going threshold (Schmitt input), /REST	V <sub>IHS</sub>	0.7V <sub>DD</sub>	-	V <sub>DD</sub> +0.5	V	
Hysteresis voltage of PA~PB(Schmitt input)	V <sub>HY</sub>		0.2V <sub>DD</sub>		V	

Source Current PA, PB, Quasi-Bidirectional Mode)	$I_{SR11}$	-300	-370	-450	$\mu\text{A}$	$V_{DD} = 4.5\text{V}, V_S = 2.4\text{V}$
	$I_{SR12}$	-50	-70	-90	$\mu\text{A}$	$V_{DD} = 2.7\text{V}, V_S = 2.2\text{V}$
	$I_{SR12}$	-40	-60	-80	$\mu\text{A}$	$V_{DD} = 2.5\text{V}, V_S = 2.0\text{V}$
Source Current PA, PB (Push-pull Mode)	$I_{SR21}$	-20	-24	-28	mA	$V_{DD} = 4.5\text{V}, V_S = 2.4\text{V}$
	$I_{SR22}$	-4	-6	-8	mA	$V_{DD} = 2.7\text{V}, V_S = 2.2\text{V}$
	$I_{SR22}$	-3	-5	-7	mA	$V_{DD} = 2.5\text{V}, V_S = 2.0\text{V}$
Sink Current PA, PB (Quasi-bidirectional and Push-pull Mode)	$I_{SK1}$	10	16	20	mA	$V_{DD} = 4.5\text{V}, V_S = 0.45\text{V}$
	$I_{SK1}$	7	10	13	mA	$V_{DD} = 2.7\text{V}, V_S = 0.45\text{V}$
	$I_{SK1}$	6	9	12	mA	$V_{DD} = 2.5\text{V}, V_S = 0.45\text{V}$
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	$V_{BH}$	30	-	150	mV	$V_{DD} = 2.5\text{V}-5.5\text{V}$

**Notes:**

1. /REST pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of  $V_{DD}=5.5\text{V}$ , 5 $\mu\text{s}$  transition current reaches its maximum value when  $V_{in}$  approximates to 2V.

### 6.3 AC Electrical Characteristics

#### 6.3.1 External 32kHz XTAL Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	°C
V <sub>DD</sub>	-	2.4	-	5.5	V

#### 6.3.2 Internal 49.152MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	1.8	-	5.5	V
Center Frequency	-	-	49.152	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; V <sub>DD</sub> =3V	-0.5	-	0.5	%
	-40°C~+85°C; V <sub>DD</sub> =2.4V~5.5V	-2.0	-	1.0	%

#### 6.3.3 Internal 16 kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.4	-	5.5	V
Center Frequency	-	-	16	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V <sub>DD</sub> =3V	-10	-	10	%
	-40°C~+85°C; V <sub>DD</sub> =2.4V~5.5V	-20	-	20	%

#### 6.3.4 External 12MHz XTAL Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	12	-	MHz
Temperature	-	-40	-	85	°C
V <sub>DD</sub>	-	1.8	-	5.5	V

## 6.4 Analog Characteristics

### 6.4.1 Specification of ADC and Speaker Driver

Conditions: V<sub>CCD</sub> = 3.3V, V<sub>CCA</sub> = 3.3V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz, 16-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
<b>Analog to Digital Converter (SDADC)</b>						
Full scale input signal <sup>1</sup>	V <sub>INFS</sub>	PGAGAIN = 0dB		0.85 -1.41		V <sub>rms</sub> dBV
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted	tbd	95		dB
Total harmonic distortion <sup>2</sup>	THD+N	Input = -3dB FS input		-85	tbd	dB
<b>PWM Speaker Output (8Ω bridge-tied-load)</b>						
Full scale output <sup>4</sup>				V <sub>CCSPK</sub> / 3.3		V <sub>rms</sub>
Total harmonic distortion <sup>2</sup>	THD+N	P <sub>o</sub> = 200mW, V <sub>DDSPK</sub> =3.3V		53		dB
		P <sub>o</sub> = 320mW, V <sub>DDSPK</sub> = 3.3V				dB
		P <sub>o</sub> = 500mW, V <sub>DDSPK</sub> = 5V		-56		dB
		P <sub>o</sub> = 1000mW, V <sub>DDSPK</sub> = 5V				dB
Signal-to-noise ratio	SNR	V <sub>DDSPK</sub> = 3.3V		80		dB
		V <sub>DDSPK</sub> =5V		80		dB
Power supply rejection ratio (50Hz - 22kHz)	PSRR	V <sub>DDSPK</sub> = 3.3V		70		dB
		V <sub>DDSPK</sub> = 5V		72		dB

### 6.4.2 Specification of PGA

Conditions: V<sub>CCD</sub> = 3.3V, V<sub>CCA</sub> = 3.3V, V<sub>ido</sub>=1.5V T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 48kHz, 16-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
<b>Microphone Inputs (MICP, MICN) and Programmable Gain Amplifier (PGA)</b>						
Full scale input signal <sup>1</sup>		PGAGAIN = 0dB		0.85 -1.41		V <sub>rms</sub> dBV



Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Programmable gain		Low impedance mode		0	6	dB
		High impedance mode		6	12	dB
Programmable gain step size		Guaranteed Monotonic		6		dB
Mute Attenuation				120		dB
Input resistance, each input pin		Low impedance mode		12		kΩ
		High impedance mode		500		kΩ
Input capacitance				10		pF
PGA equivalent input noise		0 to 20kHz, 0dB gain, low impedance mode		8.5		μVrms

### 6.4.3 Specification of ALC and MICBIAS

Conditions: VCCD = 3.3V, VCCA = 3.3V, T<sub>A</sub> = +25°C, 1kHz signal, f<sub>s</sub> = 10kHz, 16-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
<b>Automatic Level Control (ALC) &amp; Limiter:</b>						
Target record level			-22.5		-1.5	dBFS
Programmable gain			-12		35.25	dB
Gain hold time <sup>3</sup>	t <sub>HOLD</sub>	Doubles every gain step, with 16 steps total	0 / 2.67 / 5.33 / ... / 43691			ms
Gain ramp-up (decay) <sup>3</sup>	t <sub>DCY</sub>	ALC Mode ALC = 0	4 / 8 / 16 / ... / 4096			ms
		Limiter Mode ALC = 1	1 / 2 / 4 / ... / 1024			ms
Gain ramp-down (attack) <sup>3</sup>	t <sub>ATK</sub>	ALC Mode ALC = 0	1 / 2 / 4 / ... / 1024			ms
		Limiter Mode ALC = 1	0.25 / 0.5 / 1 / ... / 128			ms
Mute Attenuation				120		dB
<b>Microphone Bias</b>						
Mic Bias voltage	V <sub>MICBIAS</sub>	Gain settings	1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8,			V <sub>ido</sub>
		Output voltage	1.5, 1.8, 1.95, 2.1, 2.25, 2.4, 2.55, 2.7			V
Maximum output current	I <sub>MICBIAS</sub>				3	mA
Output noise voltage	V <sub>n</sub>	1kHz to 20kHz		46		nV/√Hz

#### Notes

1. Full Scale is relative to the magnitude of  $V_{ido}$ .
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. Time values scale proportionally with HCLK. Complete descriptions and definitions for these values are contained in the detailed descriptions of the ALC functionality.

## 6.4.4 Specification of LDO and Power Management

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	1.8	5	5.5	V	$V_{DD}$ input voltage
Output Voltage (bypass=0)	-10%	1.5	+10%	V	$V_{DD} > 1.8V$
Temperature	-40	25	85	°C	
Quiescent Current (PD=0, bypass=0)	-	100	-	uA	
Quiescent Current (PD=1, bypass=0)	-	5	-	uA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	uA	
Cbp	-	1u	-	F	Resr=1ohm
Cload	-	250p	-	F	

### Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VCCD and the VSSD pin of the device.
2. To ensure regulator stability, a 1.0uF capacitor must be connected between LDO pin and the VSSD pin of the device. Also a 100nF bypass capacitor between LDO and VSSD will help suppress output noise.

## 6.4.5 Specification of Brownout Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.8	-	5.5	V
Quiescent current	AVDD=5.5V	-	-	125	μA
Temperature	-	-40	25	85	°C
Brown-out voltage	BOV_VL[3:0]=1111		4.6		V
	BOV_VL [3:0]=1110		4.2		V
	BOV_VL [3:0]=1101		3.9		V

	BOV_VL [3:0]=1100		3.7		V
	BOV_VL [3:0]=1011		3.6		V
	BOV_VL [3:0]=1010		3.4		V
	BOV_VL [3:0]=1001		3.1		V
	BOV_VL [3:0]=1000		3.0		V
	BOV_VL [3:0]=0111		2.8		V
	BOV_VL [3:0]=0110		2.6		V
	BOV_VL [3:0]=0101		2.4		V
	BOV_VL [3:0]=0100		2.2		V
	BOV_VL [3:0]=0011		2.1		V
	BOV_VL [2:0]=0010		2.0		V
	BOV_VL [3:0]=0001		1.9		V
	BOV_VL [2:0]=0000		1.8		V
Hysteresis	-	40		130	mV

#### 6.4.6 Specification of Power-On Reset (VCCD)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	°C
Reset voltage	VCC ramping down	-	1.0	-	V
Reset Release voltage	VCC ramping up		1.5		V
Quiescent current	V <sub>in</sub> >reset voltage	-	60	-	nA

## 6.4.7 Specification of Comparator( for capsense)

PARAMETER	MIN.	TYP.	MAX.	Condition
Temperature	-40°C	25 °C	85°C	-
VCCA	1.8	3	5.5	-
VCCA current	-	20uA	40uA	20uA@VDD=3V
Input offset voltage	-	5mV	15mV	-
Input common mode range	0.1	-	VDD-1.2	-
DC gain	-	70dB	-	-
Propagation delay	-	200ns	-	@VCM=1.2V & VDIFF=0.1V
Comparison voltage	10mV	20mV	-	20mV@VCM=1V 50mV@VCM=0.1V 50mV@VCM=VDD-1.2 @10mV for non-hysteresis
Hysteresis	-	±10mV	-	One bit control W/O & W. hysteresis @VCM=0.4V ~ VDD-1.2V
Wake up time	-	-	2us	@CINP=1.3V CINN=1.2V

## 6.4.8 OP Amplifier Electrical Characteristics

Conditions: VCCD = 5.0V, VCCA = 5.0V, T<sub>A</sub> = +25°C,

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
D.C. Characteristic						
Operating voltage	Vdd	-	1.8	-	5.5	V
Quiescent current	Idd	5V No load, A0OEN/A1OEN fixed to 0	-	200	350	uA
Input offset voltage	Vopos	5V	-2	-	+2	mV
Input offset current	Iopos	VDD=5V, VCM=1/2VDD, Ta=-40~85C	-	10	-	nA

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Common Mode Voltage Range	Vcm	-	Vss	-	Vdd-1.4	V
Power Supply Rejection Ratio	PSRR	-	58	80	-	dB
Common Mode Rejection Ratio	CMRR	VDD=5V, VCM=0~VDD-1.4V	58	80	-	dB
A.C. Characteristic						
Open Loop Gain	Aol	-	60	80	-	dB
Slew Rate+, Rate	SR	No load	-	0.1	-	V/us
Gain Band Width	GBW	RL=1MΩ, CL=100pF	1	2	-	MHz

## Notes

### 6.4.9 Specification of Comparator( for OP)

PARAMETER	MIN.	TYP.	MAX.	Condition
Temperature	-40°C	25 °C	85°C	-
VCCA	1.8	3	5.5	-
VCCA current	-	20uA	40uA	20uA@VDD=3V
Comparator 1 Input offset voltage		10mV		-
Comparator 2 Input offset voltage		4mV		-
Input common mode range	0.1	-	VDD-1.2	-
DC gain	-	80dB	-	-
Propagation delay	-	200ns	-	@VCM=1.2V & VDIFF=0.1V
Comparison voltage	10mV	20mV	-	20mV@VCM=1V 50mV@VCM=0.1V 50mV@VCM=VDD-1.2 @10mV for non-hysteresis
Hysteresis	-	±10mV	-	One bit control W/O & W. hysteresis @VCM=0.4V ~ VDD-1.2V
Wake up time	-	-	2us	@CINP=1.3V CINN=1.2V

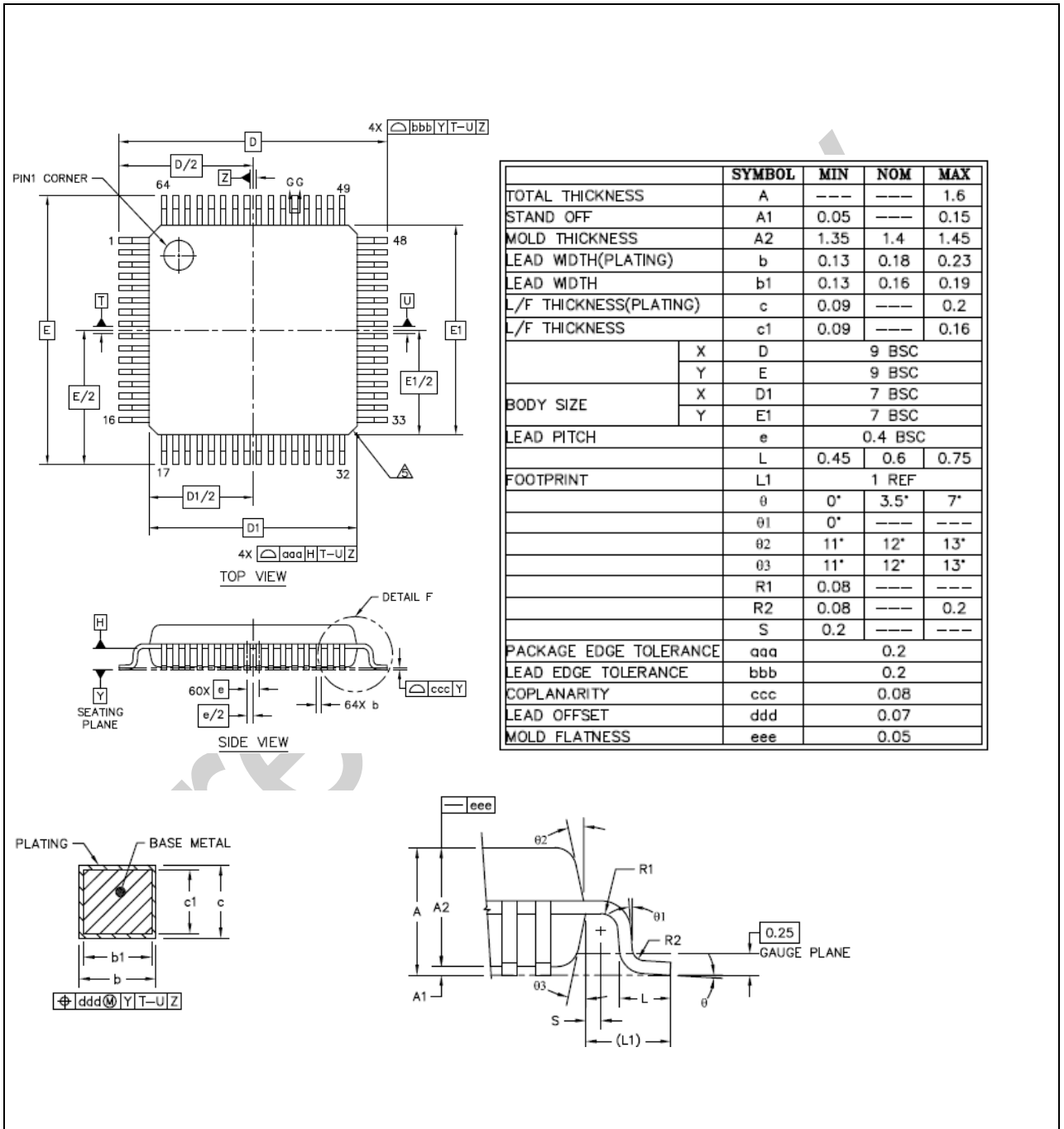
#### 6.4.10 SARADC Spec

Conditions: VCCD = 5.0V, VCCA = 5.0V, T<sub>A</sub> = +25°C,

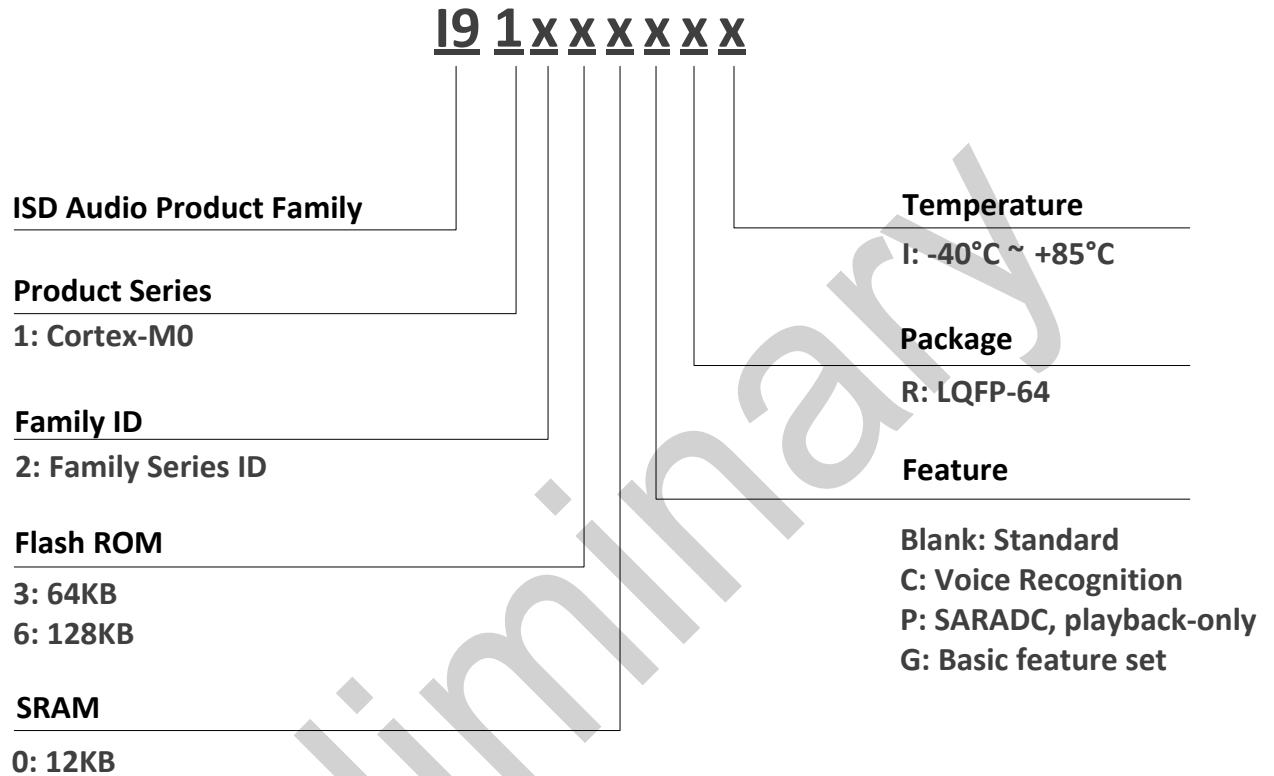
Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Resolution		3V			12	Bit
Differential nonlinearity error	DNL	3V	-	-1 ~ 2	-1 ~ 4	LSB
Integral nonlinearity error	INL	3V	-	2	4	LSB
Offset error	EO	3V	-	1	10	LSB
Gain error (Transfer gain)	EG	3V	-	1	1.005	-
Monotonic	-	3V	-	-	-	-
SARADC clock frequency (AVDD = 5V/3V)	Fadc	3V	-	-	10	Mhz
Sample rate	Fs	3V	-	-	357	KSPS
Supply voltage	Vdda	3V	1.8	-	5.5	V
Supply current (Avg.)	Idd	3V	-	0.5		mA
	Idda	3V	-	0.5		mA
Reference voltage	Vref	3V	3	-	Vdda	V
Reference current (Avg.)	Iref		-	0.5		mA
Input voltage	Vin		0	-	Vref	V

## 7 PACKAGE DIMENSIONS

### 7.1.1 64L LQFP (7x7x1.4mm footprint 2.0mm)



## 8 ORDERING INFORMATION



Preliminary



## 9 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V0.12	Aug 24, 2017	-	Preliminary Release.
V0.13	Oct 25, 2017		Some DC current change. Add SARADC characteristic
V0.14	Dec 19,2017		Add analog pin function in pin description section Add part for ordering information Add pin diagram for P & G series

Preliminary

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