# NuMicro® Family
# M480 Series
# Datasheet



For additional information or questions, please contact: Nuvoton Technology Corporation.

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# 1 GENERAL DESCRIPTION

The NuMicro® M480 series 32-bit microcontroller powered by Arm® Cortex®-M4F with DSP extension runs up to 192 MHz with 175µA/MHz power consumption. Its 256/512 KB embedded Flash memory in dual-bank architecture supports Over-The-Air firmware upgrade. The 96/160 KB embedded SRAM includes 32 KB cache for speeding up code execution from the external SPI Flash. Built-in 4 KB Secure Protection ROM provides a safe space for saving confidential program or data. System supports a wide voltage range from 1.8V to 3.6V in industrial operating temperature from -40°C to 105°C.

The M480 series is equipped with a large number of high speed digital peripherals, such as a USB 2.0 high speed interface with on-chip transceiver working in device/host/OTG mode, a USB 2.0 full speed interface with on-chip transceiver working in device/host/OTG mode, up to nine UART interfaces including three ISO-7816-3 interfaces, up to four composite SPI/$I^2S$ interfaces, a Quad-SPI interface, a SPI Flash interface supporting quad mode, three $I^2C$ interfaces, a 192 kHz/32-bit $I^2S$ interface, two SDIO interfaces, two CAN 2.0B interfaces, two QEI interfaces, a 10/100 Mbps Ethernet MAC supporting RMII and two Universal Serial Control Interfaces which can be configured as UART, SPI or $I^2C$. The M480 series also supports 16 channels peripheral DMA and up to 32 channels PWM running up to 192 MHz.

The M480 series provides high performance analog peripherals, such as a 12-bit 5MSPS SAR ADC with up to 16 channels, two 12-bit 1MSPS DAC, two analog comparators and three operational amplifiers, as well as a built-in hardware cryptography accelerator that supports ECC, AES, DES, triple DES, SHA, HMAC and a random number generator (RNG).

The NuMicro® M480 series includes the following sub-series:

- NuMicro® M481 Base series: Delivers high performance computing power with low power consumption for running complex algorithm.
- NuMicro® M482 USB FS OTG series: Built-in USB 2.0 full speed interface with on-chip OTG transceiver working in device/host/OTG mode.
- NuMicro® M483 CAN series: Built-in two sets of CAN 2.0B bus interfaces.
- NuMicro® M484 USB HS OTG series: Built-in USB 2.0 high speed interface with on-chip OTG transceiver working in device/host/OTG mode.
- NuMicro® M485 Crypto series: Built-in hardware cryptography engine and random number generator.
- NuMicro® M487 Ethernet series: Built-in 10/100Mbps Ethernet MAC supports industrial RMII, MDC and MDIO for communicating with an external transceiver.

# 2 FEATURES

## 2.1 NuMicro® M480 Features

| | |
|---|---|
| ***Core and System*** | |
| **ARM® Cortex®-M4** | • ARM® Cortex®-M4 processor, running up to 192 MHz<br>• Built-in Memory Protection Unit (MPU)<br>• Built-in Nested Vectored Interrupt Controller (NVIC)<br>• Hardware IEEE 754 compliant Floating-point Unit (FPU)<br>• DSP extension with hardware divider and single-cycle 32-bit hardware multiplier<br>• 24-bit system tick timer<br>• Programmble and maskable interrupt<br>• Low Power Sleep mode by WFI and WFE instructions |
| **Brown-out Detector (BOD)** | • Eight-level BOD with brown-out interrupt and reset option. (3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V) |
| **Low Voltage Reset (LVR)** | • LVR with 1.5V threshold voltage level. |
| **Security** | • 96-bit Unique ID (UID).<br>• 128-bit Unique Customer ID (UCID).<br>• One built-in temperature sensor with 1℃ resolution. |
| ***Memories*** | |
| **Flash** | • Dual bank 512/256 KB on-chip Application ROM (APROM) for Over-The-Air (OTA) upgrade<br>• 192 MHz maximum frequency, with performance at zero wait cycle in continuous address read access<br>• 4 KB on-chip Flash for user-defined loader (LDROM)<br>• 8 KB non-readble Key Protection ROM (KPROM) for firmware programming protection<br>• 4 KB non-readble Security Protection ROM (SPROM) for intelectual property protection<br>• 2 KB One Time Programable (OTP) ROM for data security<br>• All on-chip Flash support 4 KB page erase<br>• Fast Flash programming verification with CRC<br>• On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities<br>• Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM)<br>• Data Flash with configurable memory size<br>• 2-wired ICP Flash updating through SWD interface |

| | |
|---|---|
| | • 32-bit/64-bit and multi-word Flash programming function |
| **SRAM** | • Up to 160 KB on-chip SRAM includes:<br>– 32 KB SRAM located in bank 0 that supports hardware parity check and retenion mode; Exception (NMI) generated upon a parity check error<br>– 96/32 KB SRAM located in bank 1<br>– 32 KB SRAM located in bank 2 that can be used as cache for external SPI Flash memory<br>• Byte-, half-word- and word-access<br>• PDMA operation |
| **Cyclic Redundancy Calculation (CRC)** | • Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials<br>• Programmable initial value and seed value<br>• Programmable order reverse setting and one's complement setting for input data and CRC checksum<br>• 8-bit, 16-bit, and 32-bit data width<br>• 8-bit write mode with 1-AHB clock cycle operation<br>• 16-bit write mode with 2-AHB clock cycle operation<br>• 32-bit write mode with 4-AHB clock cycle operation<br>• Uses DMA to write data with performing CRC operation |
| **Peripheral DMA (PDMA)** | • Sixteen independent and configurable channels for automatic data transfer between memories and peripherals<br>• Basic and Scatter-Gather transfer modes<br>• Each channel supports circular buffer management using Scatter-Gather Transfer mode<br>• Stride function for rectangle image data movement<br>• Fixed-priority and Round-robin priorities modes<br>• Single and burst transfer types<br>• Byte-, half-word- and word tranfer unit with count up to 65536<br>• Incremental or fixed source and destination address |
| ***Clocks*** | |
| **External Clock Source** | • 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation<br>• 32.7688 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation<br>• Supports clock failure detection for external crystal oscillators and exception generatation (NMI) |
| **Internal Clock Source** | • 12 MHz High-speed Internal RC oscillator (HIRC) trimmed to 2% accuracy that can optionally be used as a system clock<br>• 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation |

| | |
|---|---|
| | • Up to 480 MHz on-chip PLL, sourced from HIRC or HXT, allows CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal |
| **Real-Time Clock (RTC)** | • Real-Time Clock with a separate power domain<br>• The RTC clock source includes Low-speed external crystal oscillator (LXT)<br>• The RTC block includes 80 bytes backup registers, which can be cleared by tamper pins<br>• Supports 6 static and dynamic tamper pins<br>• Able to wake up CPU from any reduced power mode<br>• Supports ±5ppm within 5 seconds software clock accuracy compensation<br>• Supports Alarm registers (second, minute, hour, day, month, year)<br>• Supports RTC Time Tick and Alarm Match interrupt<br>• Automatic leap year recognition<br>• Supports 1 Hz clock output for calibration |
| ***Timers*** | |
| **32-bit Timer** | **TIMER**<br>• Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source<br>• One-shot, Periodic, Toggle and Continuous Counting operation modes<br>• Supports event counting function to count the event from external pins<br>• Supports external capture pin for interval measurement and resetting 24-bit up counter<br>• Supports chip wake-up function, if a timer interrupt signal is generated<br>**PWM**<br>• Eight 16-bit PWM counters with 12-bit clock prescale<br>• Supports 12-bit deadband (dead time)<br>• Up, down or up-down PWM counter type<br>• Supports brake function<br>• Supports mask function and tri-state output for each PWM channel |
| **Enhanced PWM (EPWM)** | • Twelve 16-bit counters with 12-bit clock prescale for twelve 192 MHz PWM output channels<br>• Up to 12 independent input capture channels with 16-bit resolution counter<br>• Supports dead time with maximum divided 12-bit prescale<br>• Up, down or up-down PWM counter type<br>• Supports complementary mode for 3 complementary paired PWM output channels |

| | |
|---|---|
| | • Synchronous function for phase control<br>• Counter synchronous start function<br>• Brake function with auto recovery mechanism<br>• Mask function and tri-state output for each PWM channel<br>• Able to trigger EADC or DAC to start conversion |
| **Basic PWM (BPWM)** | • Two 16-bit counters with 12-bit clock prescale for twelve 192 MHz PWM output channels.<br>• Up to 6 independent input capture channels with 16-bit resolution counter<br>• Up, down or up-down PWM counter type<br>• Counter synchronous start function<br>• Complementary mode for 3 complementary paired PWM output channels<br>• Mask function and tri-state output for each PWM channel<br>• Able to trigger EADC to start conversion. |
| **Watchdog** | • 18-bit free running up counter for WDT time-out interval<br>• Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period<br>• Able to wake up system from Power-down or Idle mode<br>• Time-out event to trigger interrupt or reset system<br>• Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period<br>• Configured to force WDT enabled on chip power-on or reset. |
| **Window Watchdog** | • Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale<br>• Suspended in Idle/Power-down mode |
| ***Analog Interfaces*** | |
| **Enhanced Analog-to-Digital Converter (EADC)** | • One 12-bit, 19-ch 5 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed.<br>• Three internal channels for band-gap VBG input and Temperature sensor input<br>• Supports external VREF pin or internal reference voltage VREF: 1.6V, 2.0V, 2.5V, and 3.0V.<br>• Two power saving modes: Power-down mode and Standby mode<br>• Supports calibration capability.<br>• Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~3 overflow pulse trigger or PWM trigger.<br>• Configurable EADC sampling time.<br>• Up to 19 sample modules. |

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| | • Double data buffers for sample module 0~3.<br>• PDMA operation. |
| **Digital-to-Analog Converter (DAC)** | • Two 12-bit, 1 MSPS voltage type DAC with 8-bit mode and 8μs rail-to-rail settle time.<br>• Maximum output voltage $AV_{DD}$ -0.2V at buffer mode<br>• Digital-to-Analog conversion triggered by Timer0~3, EPWM0, EPWM1, external trigger pin to start DAC conversion or software.<br>• Supports group mode for synchronized data update of two DACs.<br>• PDMA operation |
| **Analog Comparator (ACMP)** | • Two rail-to-rail Analog Comparators.<br>• Supports four multiplexed I/O pins at positive input.<br>• Supports I/O pins, band-gap, DAC, and 16-level Voltage divider from $AV_{DD}$ or $V_{REF}$ at negative input<br>• Supports four programmable propagation speeds for power saving<br>• Supports wake up from Power-down by interrput<br>• Supports triggers for brake events and cycle-by-cycle control for PWM<br>• Supports window compare mode and window latch mode.<br>• Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV |
| **Operational Amplifier (OPA)** | • Three Operational Amplifiers with 0~$AV_{DD}$ input voltage range.<br>• OPA schmitt trigger buffer output used as the interrupt source of comparator. |
| ***Communication Interfaces*** | |
| **Low-power UART** | • Six sets of UARTs with up to 17.45 MHz baud rate.<br>• Auto-Baud Rate measurement and baud rate compensation function.<br>• Supports low power UART (LPUART): baud rate clock from LXT(32.768 KHz) with 9600bps in Power-down mode even system clock is stopped.<br>• 16-byte FIFOs with programmable level trigger<br>• Auto flow control ( nCTS and nRTS)<br>• Supports IrDA (SIR) function<br>• Supports LIN function on UART0 and UART1<br>• Supports RS-485 9-bit mode and direction control<br>• Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode.<br>• Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction<br>• Supports wake-up function |

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| | • 8-bit receiver FIFO time-out detection function<br>• Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function<br>• PDMA operation. |
| **Smart Card Interface** | • Three sets of ISO-7816-3 which are compliant with ISO-7816-3 T=0, T=1<br>• Supports full duplex UART function.<br>• 4-byte FIFOs with programmable level trigger<br>• Programmable guard time selection (11 ETU ~ 266 ETU)<br>• One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing<br>• Auto inverse convention function<br>• Stop clock level and clock stop (clock keep) function<br>• Transmitter and receiver error retry function<br>• Supports hardware activation, deactivation and warm reset sequence process<br>• Supports hardware auto deactivation sequence after card removal. |
| **$I^2C$** | • Three sets of $I^2C$ devices with Master/Slave mode.<br>• Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)<br>• Supports 10 bits mode<br>• Programmable clocks allowing for versatile rate control<br>• Supports multiple address recognition (four slave address with mask option)<br>• Supports SMBus and PMBus<br>• Supports multi-address power-down wake-up function<br>• PDMA operation |
| **SPI Master (SPI Flash)** | • Maximum 32 MB external SPI Flash memory with standard (1-bit), dual (2-bit) and quad (4-bit) transfer mode.<br>• 32 KB cache memory for enhancing program execution performance.<br>• 64-bit key length for code protection.<br>• DMA mode for code transfer between SPI Flash memory and SRAM.<br>• SPI Master function with 8-, 16-, 24-, and 32-bit length of transaction and burst mode operation, which can transmit/receive data up to four successive transactions in one transfer. |
| **Quad SPI** | • One set of SPI Quad controller with Master/Slave mode, up to 96 MHz at 2.7V~3.6V stsyem voltage.<br>• Supports Dual and Quad I/O Transfer mode<br>• Supports one/two data channel half-duplex transfer<br>• Supports receive-only mode |

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| | • Configurable bit length of a transfer word from 8 to 32-bit<br>• Provides separate 8-level depth transmit and receive FIFO buffers<br>• Supports MSB first or LSB first transfer sequence<br>• Supports the byte reorder function<br>• Supports Byte or Word Suspend mode<br>• Supports 3-wired, no slave select signal, bi-direction interface<br>• PDMA operation. |
| **SPI/I²S** | • Up to four sets of SPI/I²S controllers with Master/Slave mode.<br>• SPI/I²S provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers.<br>**SPI**<br>• SPI can communicate at up to 96 Mbit/s<br>• Configurable bit length of a transfer word from 8 to 32-bit.<br>• MSB first or LSB first transfer sequence.<br>• Byte reorder function.<br>• Supports Byte or Word Suspend mode.<br>• Supports one data channel half-duplex transfer.<br>• Supports receive-only mode.<br>**I²S**<br>• Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes.<br>• Supports PCM mode A, PCM mode B, I²S and MSB justified data format.<br>• PDMA operation. |
| **I²S** | • One set of I²S interface with Master/Slave mode.<br>• Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes.<br>• Two 16-level FIFO data buffers, one for transmitting and the other for receiving.<br>• Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format.<br>• Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format.<br>• PCM protocol supports TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8.<br>• PDMA operation. |
| **Universal Serial Control Interface (USCI)** | • Two sets of USCI,configured as UART, SPI or I²C function.<br>• Supports single byte TX and RX buffer mode<br>**UART**<br>• Supports one transmit buffer and two receive buffers for data |

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| | payload.<br>• Supports hardware auto flow control function and programmable flow control trigger level.<br>• 9-bit Data Transfer.<br>• Baud rate detection by built-in capture event of baud rate generator.<br>• Supports wake-up function.<br>• PDMA operation.<br>**SPI**<br>• Supports Master or Slave mode operation.<br>• Supports one transmit buffer and two receive buffer for data payload.<br>• Supports additional receive/transmit 16 entries FIFO for data payload.<br>• Configurable bit length of a transfer word from 4 to 16-bit (SPI Quad transmission only supports 8 to 16-bit of word length).<br>• Supports MSB first or LSB first transfer sequence.<br>• Supports Word Suspend function.<br>• Supports 3-wire, no slave select signal, bi-direction interface.<br>• Supports wake-up function: input slave select transition.<br>• PDMA operation.<br>**$I^2C$**<br>• Supports master and slave device capability.<br>• Supports one transmit buffer and two receive buffer for data payload.<br>• Communication in standard mode (100 kbps), fast mode (up to 400 kbps), and Fast mode plus (1 Mbps).<br>• Supports 10-bit mode.<br>• Supports 10-bit bus time out capability.<br>• Supports bus monitor mode.<br>• Supports power-down wake-up by data toggle or address match.<br>• Supports multiple address recognition.<br>• Supports device address flag.<br>• Programmable setup/hold time. |
| **Controller Area Network (CAN)** | • Two sets of CAN 2.0B controllers.<br>• Each supports 32 Message Objects; each Message Object has its own identifier mask.<br>• Programmable FIFO mode (concatenation of Message Object).<br>• Disabled Automatic Re-transmission mode for Time Triggered CAN applications.<br>• Supports power-down wake-up function. |
| **Secure Digital Host Controller (SDHC)** | • Two sets of Secure Digital Host Controllers, compliant with SD Memory Card Specification Version 2.0. |

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| | • Supports 50 MHz to achieve 200 Mbps at 3.3V operation.<br>• Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC/SDIO card. |
| **External Bus Interface (EBI)** | • Supports up to three memory banks with individual adjustment of timing parameter.<br>• Each bank supports dedicated external chip select pin with polarity control and up to 1 MB addressing space.<br>• 8-/16-bit data width.<br>• Supports byte write in 16-bit data width mode.<br>• Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R).<br>• Supports Address/Data multiplexed mode.<br>• Supports address bus and data bus separate mode.<br>• Supports LCD interface i80 mode.<br>• PDMA operation. |
| **GPIO** | • Supports three I/O modes: Push-Pull output, Open-Drain output and Input only with high impendence mode.<br>• Selectable TTL/Schmitt trigger input.<br>• Configured as interrupt source with edge/level trigger setting.<br>• Supports independent pull-up/pull-down control.<br>• Supports high driver and high sink current I/O.<br>• Supports software selectable slew rate control.<br>• Supports 5V-tolerance function except analog I/O. |
| ***Control Interfaces*** | |
| **Quadrature Encoder Interface (QEI)** | • Two QEI phase inputs (QEI_A, QEI_B) and one Index input (QEI_INDEX).<br>• Supports 2/4 times free-counting mode and 2/4 compare-counting mode.<br>• Supports encoder pulse width measurement mode with ECAP. |
| **Enhanced Capture (ECAP)** | **Input Capture Timer/Counter**<br>• Supports three input channels with independent capture counter hold register.<br>• 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter.<br>• Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports.<br>• Supports compare-match function. |
| ***Advanced Connectivity*** | |

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| **USB 2.0 Full Speed with on-chip transceiver** | **USB 2.0 Full Speed OTG (On-The-Go)**<br>• On-chip USB 2.0 full speed OTG transceiver.<br>• Compliant with USB OTG Supplement 2.0<br>• Configurable as host-only, device-only or ID-dependent<br>**USB 2.0 Full Speed Host Controller**<br>• Compliant with USB Revision 1.1 Specification.<br>• Compatible with OHCI (Open Host Controller Interface) Revision 1.0.<br>• Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.<br>• Supports Control, Bulk, Interrupt, Isochronous and Split transfers.<br>• Integrated a port routing logic to route full/low speed device to OHCI controller.<br>• Supports an integrated Root Hub.<br>• Supports port power control and port over current detection.<br>• Built-in DMA.<br>**USB 2.0 Full Speed Device Controller**<br>• Compliant with USB Revision 2.0 Specification.<br>• Supports suspend function when no bus activity existing for 3 ms.<br>• 12 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types.<br>• 1024 bytes configurable RAM for endpoint buffer.<br>• Remote wake-up capability. |
| **USB 2.0 High Speed with on-chip transceiver** | **USB 2.0 High Speed OTG (On-The-Go)**<br>• On-chip USB 2.0 high speed OTG transceiver.<br>• Compliant with USB OTG Supplement 2.0.<br>• Configurable as host-only, device-only or ID-dependent.<br>**USB 2.0 High Speed Host Controller**<br>• Compliant with USB Revision 2.0 Specification.<br>• Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0.<br>• Compatible with OHCI (Open Host Controller Interface) Revision 1.0.<br>• Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.<br>• Integrated a port routing logic to route full/low speed device to OHCI controller.<br>• Supports an integrated Root Hub.<br>• Built-in DMA.<br>**USB 2.0 High Speed Device Controller**<br>• Compliant with USB Revision 2.0 Specification.<br>• Supports one dedicate control endpoint and 12 configurable |

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| | endpoints; each can be Isochronous, Bulk or Interrupt and either IN or OUT direction.<br>• 4096 bytes configurable RAM for endpoint buffer and up to 1024 bytes maximum packet size.<br>• Three different operation modes of an in-endpoint: Auto Validation mode, Manual Validation mode and Fly mode.<br>• Suspend, resume and remote wake-up capability.<br>• Built-in DMA. |
| **Ethernet MAC** | • IEEE Std. 802.3 CSMA/CD protocol.<br>• Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol.<br>• Supports both half and full duplex for 10 Mbps or 100 Mbps operation.<br>• RMII (Reduced Media Independent Interface) and serial management interface (MDC/MDIO).<br>• Pause and remote pause function for flow control.<br>• Long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception.<br>• CAM function for Ethernet MAC address recognition.<br>• Supports Magic Packet recognition to wake system up from Power-down mode.<br>• Built-in DMA. |
| ***Cryptography Accelerator*** | |
| **Elliptic Curve Cryptography (ECC)** | • Hardware ECC accelerator.<br>• Supports 192-bit and 256-bit key length.<br>• Supports both prime field GF(p) and binary field GF(2m).<br>• Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes.<br>• Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes.<br>• Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes.<br>• Supports point multiplication, addition and doubling operations in GF(p) and GF(2m).<br>• Supports modulus division, multiplication, addition and subtraction operations in GF(p). |
| **Advanced Encryption Standard (AES)** | • Hardware AES accelerator.<br>• Supports 128-bit, 192-bit and 256-bit key length and key expander, and is compliant with FIPS 197.<br>• Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes<br>• Compliant with NIST SP800-38A and addendum. |
| **Data Encryption Standard (DES)** | • Hardware DES accelerator.<br>• Supports ECB, CBC, CFB, OFB, and CTR block cipher mode. |

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| | • Compliant with FIPS 46-3. |
| **Triple Data Encryption Standard (3DES)** | • Hardware Triple DES accelerator.<br>• Supports two or three different keys in each round.<br>• Supports ECB, CBC, CFB, OFB, and CTR block cipher mode.<br>• Implemented based on X9.52 standard and compliant with FIPS SP 800-67. |
| **Secure Hash Algorithm (SHA)** | • Hardware SHA accelerator.<br>• Supports SHA-160, SHA-224, SHA-256, SHA-384 and SHA-512.<br>• Compliant with FIPS 180/180-2. |
| **keyed-Hash Message Authentication Code (HMAC)** | • Hardware HMAC accelerator.<br>• Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512.<br>• Compliant with FIPS 180/180-2. |

# 3 PARTS INFORMATION

## 3.1 Summary

| Part No. | USB FS | USB HS | CAN | Crypto | Ethernet |
|---|---|---|---|---|---|
| **M481** | – | – | – | – | – |
| **M482** | √ | – | – | – | – |
| **M483** | √ | √ | √ | – | – |
| **M484** | √ | √ | – | – | – |
| **M485** | √ | √ | – | √ | – |
| **M487** | √ | √ | √ | √ | √ |

## 3.2 Package Type

| Part No. | QFN33 | LQFP48 | LQFP64 | LQFP128 | LQFP144 |
|---|---|---|---|---|---|
| **M481** | M481ZGAAE<br>M481ZIDAE | M481LGAAE<br>M481LIDAE | M481SGAAE<br>M481SIDAE | | |
| **M482** | M482ZIDAE | M482LGAAE<br>M482LIDAE | M482SGAAE<br>M482SIDAE | M482KGAAE<br>M482KIDAE | |
| **M483** | | | M483SGAAE<br>M483SIDAE | M483KIDAE | |
| **M484** | | | M484SGAAE<br>M484SIDAE<br>M484SGAAE2U<br>M484SIDAE2U | M484KIDAE | |
| **M485** | M485ZIDAE | M485LIDAE | M485SIDAE | M485KIDAE | |
| **M487** | | | M487SIDAE | M487KIDAE | M487JIDAE |

## 3.3 NuMicro® M481 Base Series

| PART NUMBER | | M481 | | | | | |
|---|---|---|---|---|---|---|---|
| | | ZGAAE | ZIDAE | LGAAE | LIDAE | SGAAE | SIDAE |
| Flash (KB) | | 256 | 512 | 256 | 512 | 256 | 512 |
| SRAM (KB) | | 96 | 160 | 96 | 160 | 96 | 160 |
| ISP Loader ROM (KB) | | 4 | | | | | |
| I/O | | 26 | | 41 | | 52 | |
| 32-bit Timer | | 4 | | | | | |
| Tamper | | - | | - | | 1 | |
| Connectivity | LPUART | 6 | | | | | |
| | ISO-7816 | 3 | | | | | |
| | SPI Master | 1 | | | | | |
| | Quad SPI | 1 | | | | | |
| | SPI/I$^2$S | 3 | | 3 | | 4 | |
| | I$^2$S | 1 | | | | | |
| | I$^2$C | 3 | | | | | |
| | USCI | 2 | | | | | |
| | CAN | - | | | | | |
| | LIN | 2 | | | | | |
| | SDHC | 1 | | 2 | | 2 | |
| 16-bit PWM | | 24 | | | | | |
| QEI | | 1 | | 2 | | 2 | |
| ECAP | | - | | 1 | | 1 | |
| USB 2.0 FS OTG | | - | | | | | |
| USB 2.0 HS OTG | | - | | | | | |
| 12-bit ADC | | 10 | | 12 | | 16 | |
| 12-bit DAC | | 2 | | | | | |
| Analog Comparator | | 2 | | | | | |
| Operational Amplifier | | 1 | | 2 | | 2 | |
| Ethernet | | - | | | | | |
| Cryptography | | - | | | | | |
| LCD Parallel Data Bus (External Bus Interface) | | - | | 8 | | 16 | |
| Package | | QFN 33 | | LQFP 48 | | LQFP 64 | |

## 3.4 NuMicro® M482 USB FS OTG Series

| PART NUMBER | | M482 | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | ZIDAE | LGAAE | LIDAE | SGAAE | SIDAE | KGAAE | KIDAE |
| Flash (KB) | | 512 | 256 | 512 | 256 | 512 | 256 | 512 |
| SRAM (KB) | | 160 | 96 | 160 | 96 | 160 | 96 | 160 |
| ISP Loader ROM (KB) | | 4 | | | | | | |
| I/O | | 26 | 41 | | 52 | | 100 | |
| 32-bit Timer | | 4 | | | | | | |
| Tamper | | - | - | | 1 | | 6 | |
| Connectivity | LPUART | 6 | | | | | | |
| | ISO-7816 | 3 | | | | | | |
| | SPI Master | 1 | | | | | | |
| | Quad SPI | 1 | | | | | | |
| | SPI/I$^2$S | 3 | 3 | | 4 | | 4 | |
| | I$^2$S | 1 | | | | | | |
| | I$^2$C | 3 | | | | | | |
| | USCI | 2 | | | | | | |
| | CAN | - | | | | | | |
| | LIN | 2 | | | | | | |
| | SDHC | 2 | | | | | | |
| 16-bit PWM | | 24 | | | | | | |
| QEI | | 1 | 2 | | 2 | | 2 | |
| ECAP | | - | 1 | | 1 | | 2 | |
| USB 2.0 FS OTG | | √ | | | | | | |
| USB 2.0 HS OTG | | - | | | | | | |
| 12-bit ADC | | 10 | 12 | | 16 | | 16 | |
| 12-bit DAC | | 2 | | | | | | |
| Analog Comparator | | 2 | | | | | | |
| Operational Amplifier | | 1 | 2 | | 2 | | 3 | |
| Ethernet | | - | | | | | | |
| Cryptography | | - | | | | | | |
| LCD Parallel Data Bus (External Bus Interface) | | - | 8 | | 16 | | 16 | |
| Package | | QFN33 | LQFP 48 | | LQFP 64 | | LQFP 128 | |

## 3.5 NuMicro® M483 CAN Series

| PART NUMBER | | M483 | | |
|---|---|---|---|---|
| | | SGAAE | SIDAE | KIDAE |
| Flash (KB) | | 256 | 512 | 512 |
| SRAM (KB) | | 96 | 160 | 160 |
| ISP Loader ROM (KB) | | 4 | | |
| I/O | | 44 | | 100 |
| 32-bit Timer | | 4 | | |
| Tamper | | 1 | | 6 |
| Connectivity | LPUART | 6 | | |
| | ISO-7816 | 3 | | |
| | SPI Master | 1 | | |
| | Quad SPI | 1 | | |
| | SPI/I$^2$S | 4 | | |
| | I$^2$S | 1 | | |
| | I$^2$C | 3 | | |
| | USCI | 2 | | |
| | CAN | 2 | | |
| | LIN | 2 | | |
| | SDHC | 2 | | |
| 16-bit PWM | | 24 | | |
| QEI | | 2 | | |
| ECAP | | 1 | | 2 |
| USB 2.0 FS OTG | | - | | √ |
| USB 2.0 HS OTG | | √ | | |
| 12-bit ADC | | 16 | | |
| 12-bit DAC | | 2 | | |
| Analog Comparator | | 2 | | |
| Operational Amplifier | | 2 | | 3 |
| Ethernet | | - | | |
| Cryptography | | - | | |
| LCD Parallel Data Bus (External Bus Interface) | | 8 | | 16 |
| Package | | LQFP 64 | | LQFP 128 |

## 3.6 NuMicro® M484 USB HS OTG Series

| PART NUMBER | | M484 | | | | |
|---|---|---|---|---|---|---|
| | | SGAAE | SIDAE | SGAAE2U | SIDAE2U | KIDAE |
| Flash (KB) | | 256 | 512 | 256 | 512 | 512 |
| SRAM (KB) | | 96 | 160 | 96 | 160 | 160 |
| ISP Loader ROM (KB) | | 4 | | | | |
| I/O | | 44 | | 44 | | 100 |
| 32-bit Timer | | 4 | | | | |
| Tamper | | 1 | | 1 | | 6 |
| Connectivity | LPUART | 6 | | | | |
| | ISO-7816 | 3 | | | | |
| | SPI Master | 1 | | | | |
| | Quad SPI | 1 | | | | |
| | SPI/I$^2$S | 4 | | | | |
| | I$^2$S | 1 | | | | |
| | I$^2$C | 3 | | | | |
| | USCI | 2 | | | | |
| | CAN | - | | | | |
| | LIN | 2 | | | | |
| | SDHC | 2 | | | | |
| 16-bit PWM | | 24 | | | | |
| QEI | | 2 | | | | |
| ECAP | | 1 | | 1 | | 2 |
| USB 2.0 FS OTG | | - | | √ | | √ |
| USB 2.0 HS OTG | | √ | | | | |
| 12-bit ADC | | 16 | | | | |
| 12-bit DAC | | 2 | | | | |
| Analog Comparator | | 2 | | | | |
| Operational Amplifier | | 2 | | 2 | | 3 |
| Ethernet | | - | | | | |
| Cryptography | | - | | | | |
| LCD Parallel Data Bus (External Bus Interface) | | 8 | | 8 | | 16 |
| Package | | LQFP 64 | | LQFP 64 | | LQFP 128 |

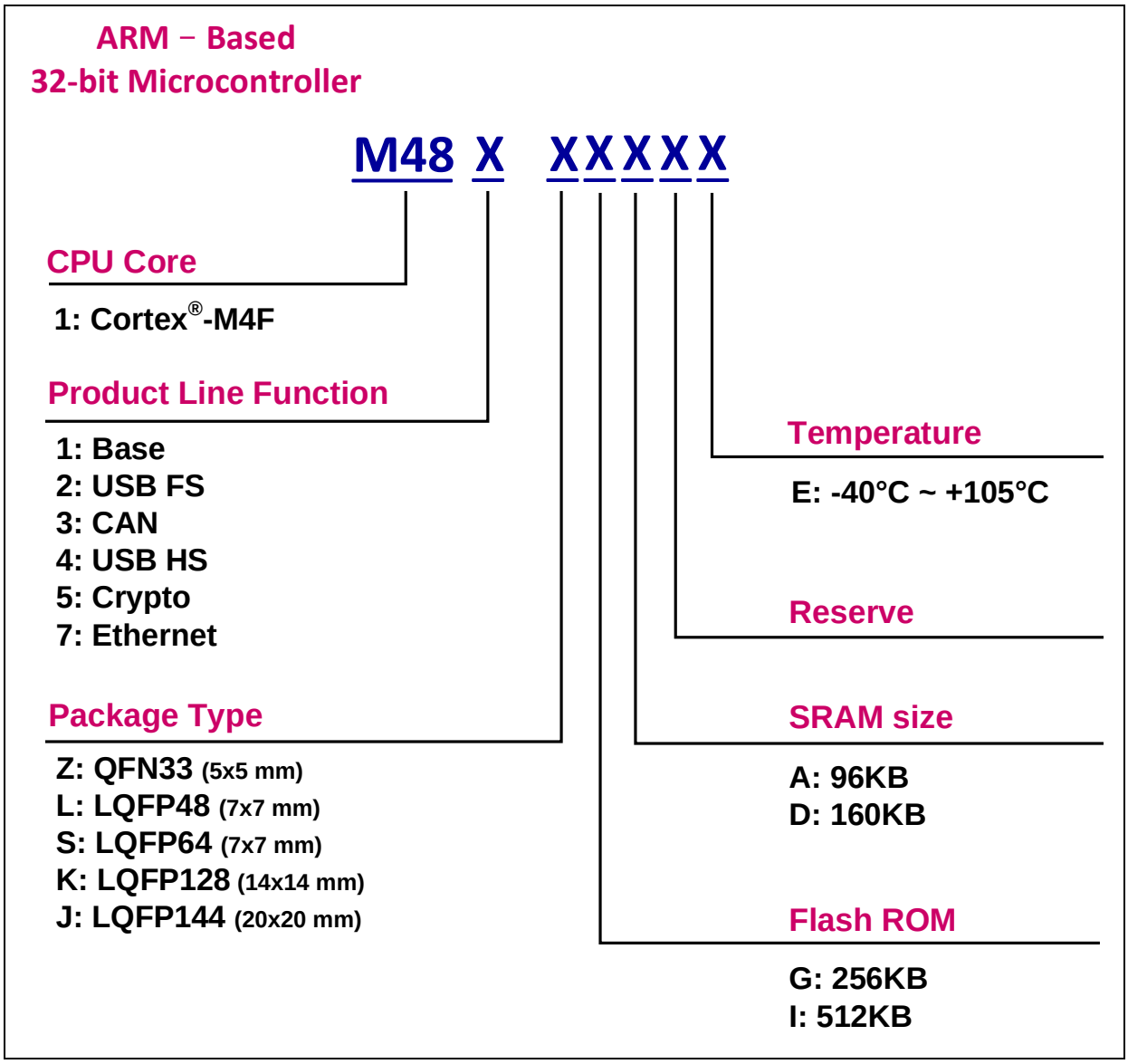
## 3.7 NuMicro® M485 Crypto Series

| PART NUMBER | | M485 | | | |
|---|---|---|---|---|---|
| | | ZIDAE | LIDAE | SIDAE | KIDAE |
| Flash (KB) | | 512 | | | |
| SRAM (KB) | | 160 | | | |
| ISP Loader ROM (KB) | | 4 | | | |
| I/O | | 26 | 41 | 44 | 100 |
| 32-bit Timer | | 4 | | | |
| Tamper | | - | - | 1 | 6 |
| Connectivity | LPUART | 6 | | | |
| | ISO-7816 | 3 | | | |
| | SPI Master | 1 | | | |
| | Quad SPI | 1 | | | |
| | SPI/I$^2$S | 3 | 3 | 4 | 4 |
| | I$^2$S | 1 | | | |
| | I$^2$C | 3 | | | |
| | USCI | 2 | | | |
| | CAN | - | | | |
| | LIN | 2 | | | |
| | SDHC | 1 | 2 | 2 | 2 |
| 16-bit PWM | | 24 | | | |
| QEI | | 1 | 2 | 2 | 2 |
| ECAP | | - | 1 | 1 | 2 |
| USB 2.0 FS OTG | | √ | √ | - | √ |
| USB 2.0 HS OTG | | - | - | √ | √ |
| 12-bit ADC | | 10 | 12 | 16 | 16 |
| 12-bit DAC | | 2 | | | |
| Analog Comparator | | 2 | | | |
| Operational Amplifier | | 1 | 2 | 2 | 3 |
| Ethernet | | - | | | |
| Cryptography | | √ | | | |
| LCD Parallel Data Bus (External Bus Interface) | | - | 8 | 8 | 16 |
| Package | | QFN33 | LQFP 48 | LQFP 64 | LQFP 128 |

## 3.8 NuMicro® M487 Ethernet Series

| PART NUMBER | | M487 | | |
|---|---|---|---|---|
| | | SIDAE | KIDAE | JIDAE |
| Flash (KB) | | 512 | | |
| SRAM (KB) | | 160 | | |
| ISP Loader ROM (KB) | | 4 | | |
| I/O | | 44 | 100 | 114 |
| 32-bit Timer | | 4 | | |
| Tamper | | 1 | 6 | 6 |
| Connectivity | LPUART | 6 | | |
| | ISO-7816 | 3 | | |
| | SPI Master | 1 | | |
| | Quad SPI | 1 | | |
| | SPI/I$^2$S | 4 | | |
| | I$^2$S | 1 | | |
| | I$^2$C | 3 | | |
| | USCI | 2 | | |
| | CAN | 2 | | |
| | LIN | 2 | | |
| | SDHC | 2 | | |
| 16-bit PWM | | 24 | | |
| QEI | | 2 | | |
| ECAP | | 1 | 2 | 2 |
| USB 2.0 FS OTG | | - | √ | √ |
| USB 2.0 HS OTG | | √ | | |
| 12-bit ADC | | 16 | | |
| 12-bit DAC | | 2 | | |
| Analog Comparator | | 2 | | |
| Operational Amplifier | | 2 | 3 | 3 |
| Ethernet | | √ | | |
| Cryptography | | √ | | |
| LCD Parallel Data Bus (External Bus Interface) | | 8 | 16 | 16 |
| Package | | LQFP 64 | LQFP 128 | LQFP 144 |

### 3.9 NuMicro® M480 Naming Rule



# 4 PIN CONFIGURATION & DESCRIPTION

## 4.1 Pin Configuration

### 4.1.1 NuMicro® M481 Base Series QFN33 Pin Diagram

Corresponding Part Number: M481ZGAAE, M481ZIDAE

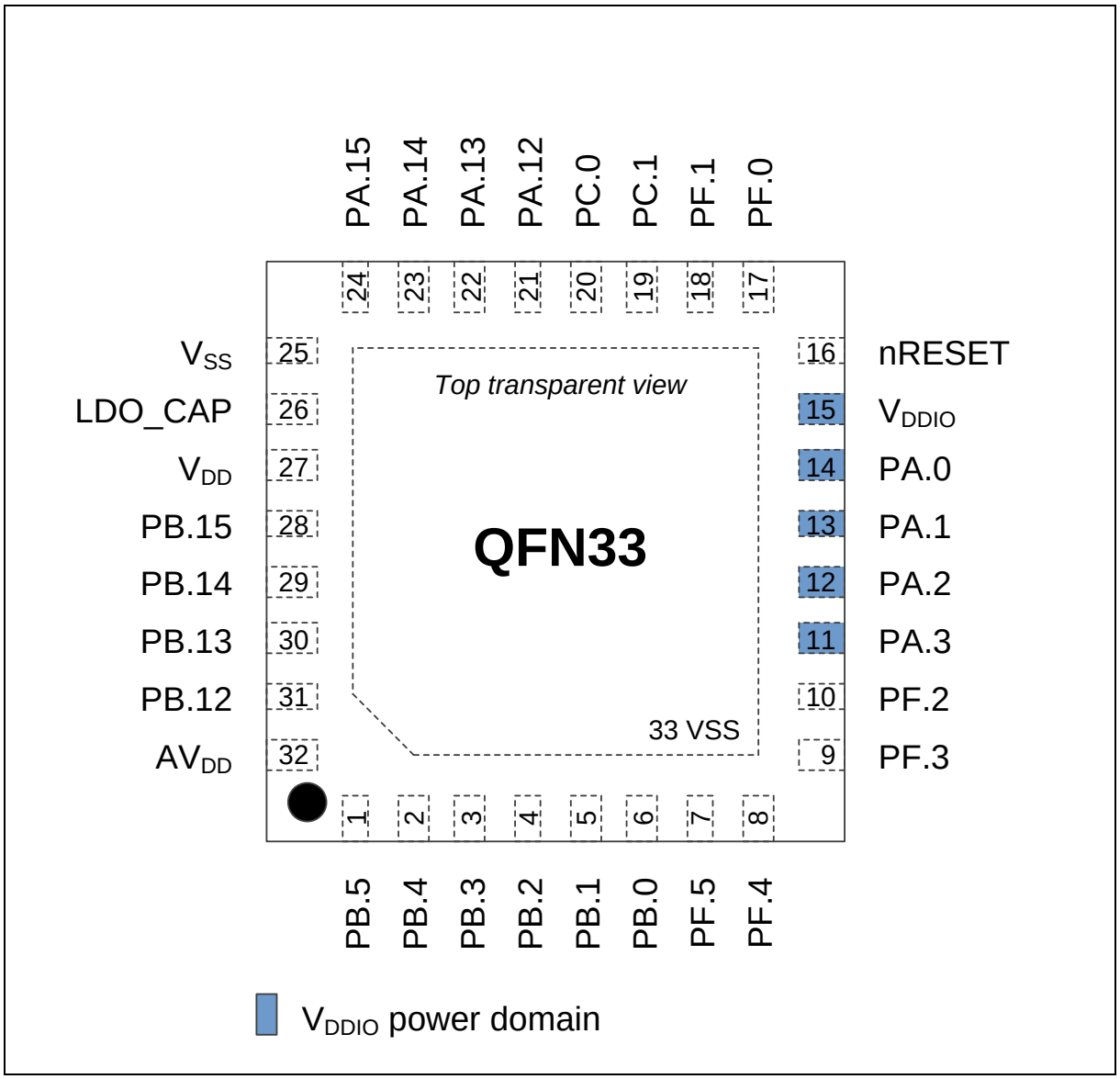



Figure 4.1-1 NuMicro® M481 Base Series QFN 33-pin Diagram

### 4.1.2 NuMicro® M481 Base Series LQFP48 Pin Diagram

Corresponding Part Number: M481LGAAE, M481LIDAE

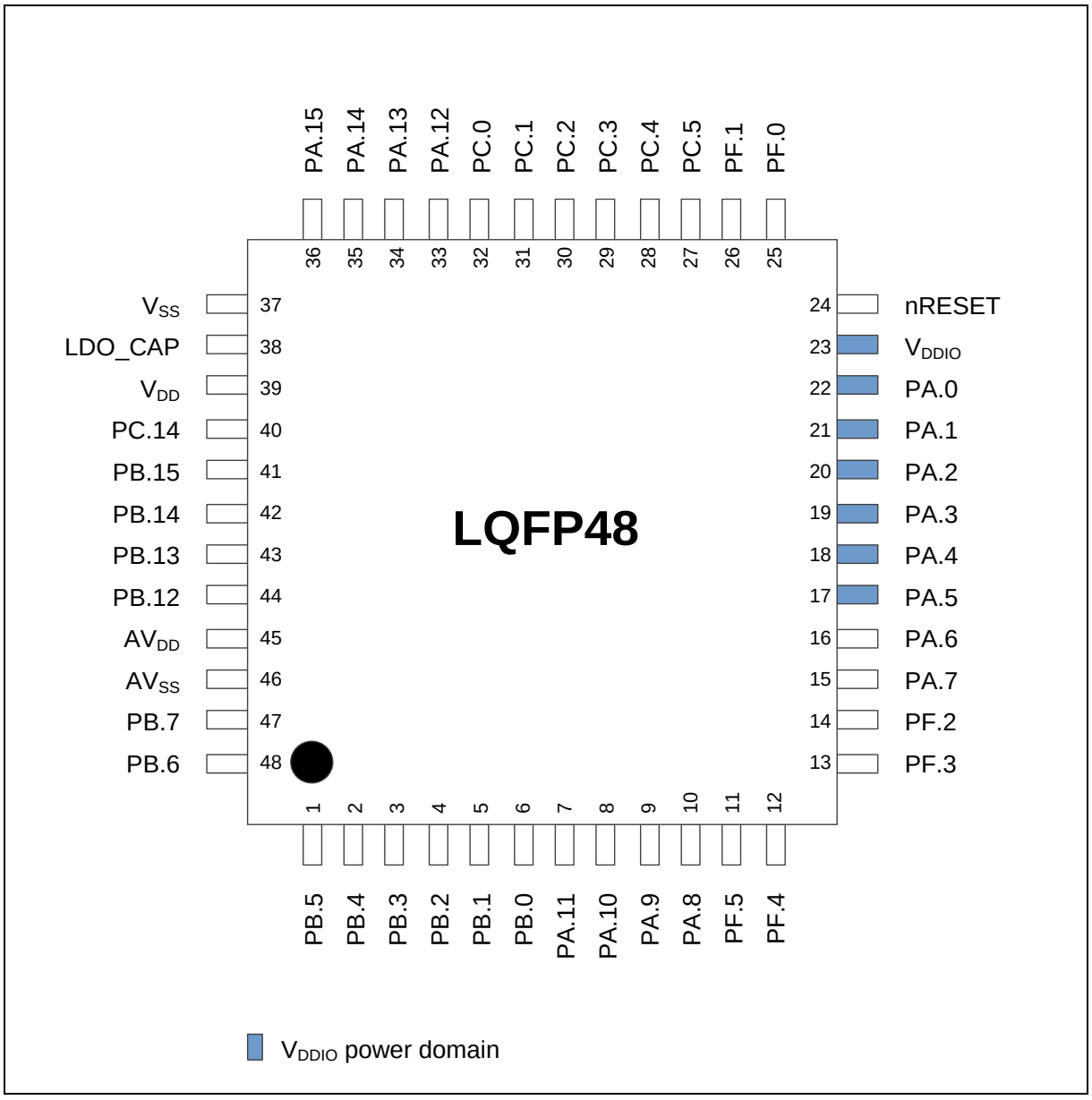



Figure 4.1-2 NuMicro® M481 Base Series LQFP 48-pin Diagram

### 4.1.3 NuMicro® M481 Base Series LQFP64 Pin Diagram

Corresponding Part Number: M481SGAAE, M481SIDAE

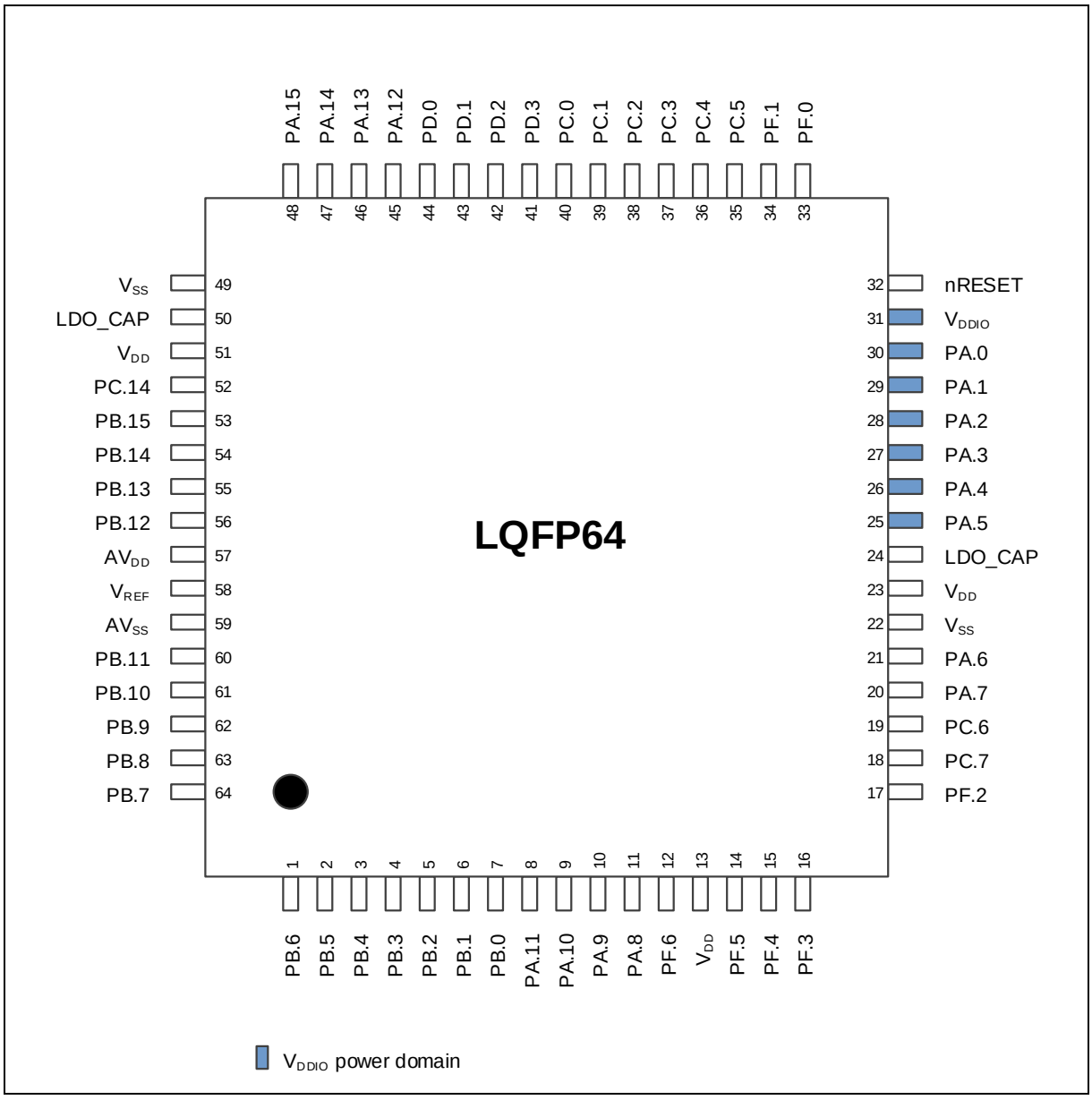



Figure 4.1-3 NuMicro® M481 Base Series LQFP 64-pin Diagram

### 4.1.4 NuMicro® M482 USB FS OTG Series QFN33 Pin Diagram

Corresponding Part Number: M482ZIDAE

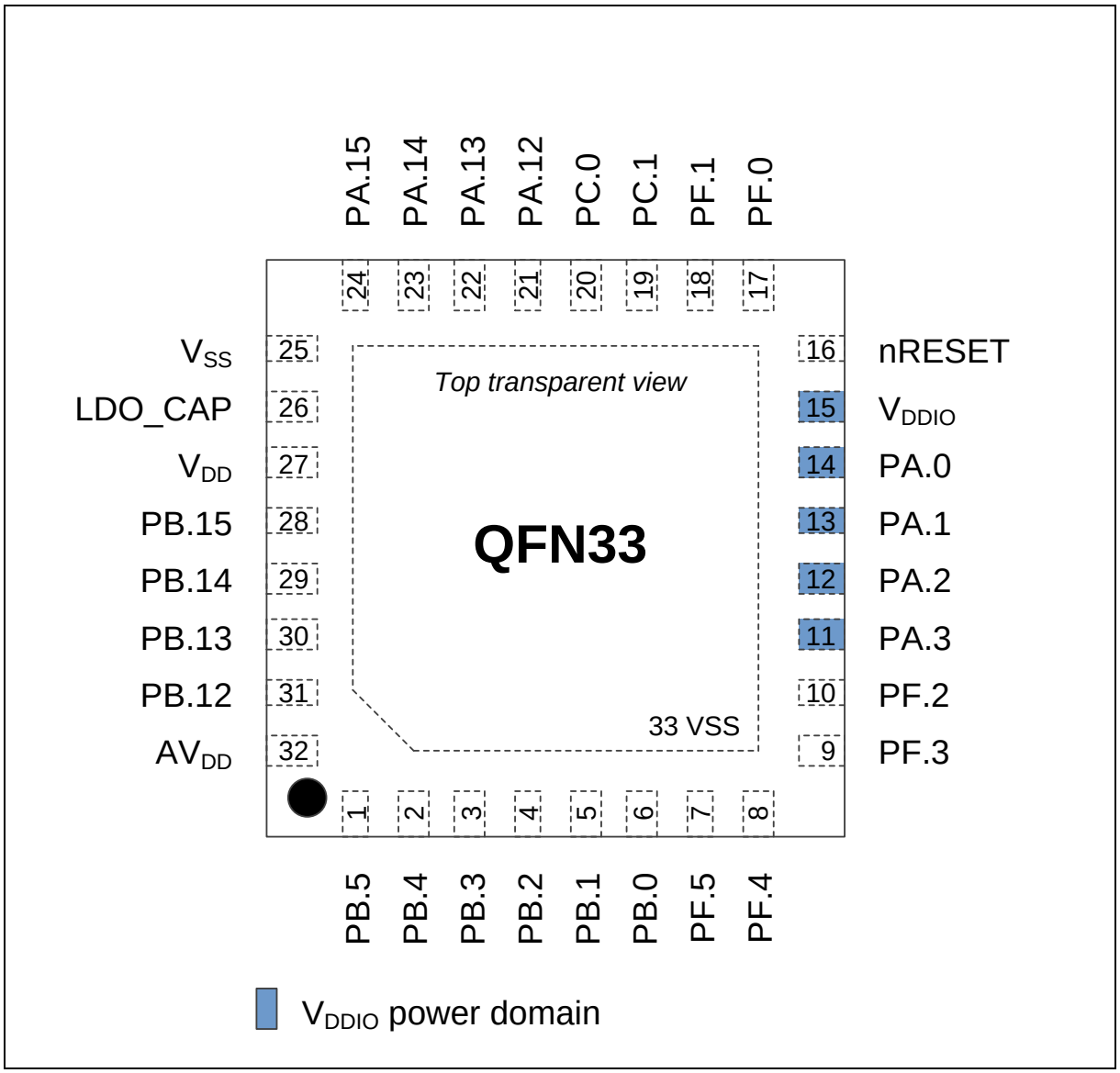



Figure 4.1-4 NuMicro® M482 USB FS OTG Series QFN 33-pin Diagram

### 4.1.5 NuMicro® M482 USB FS OTG Series LQFP48 Pin Diagram

Corresponding Part Number: M482LGAAE, M482LIDAE

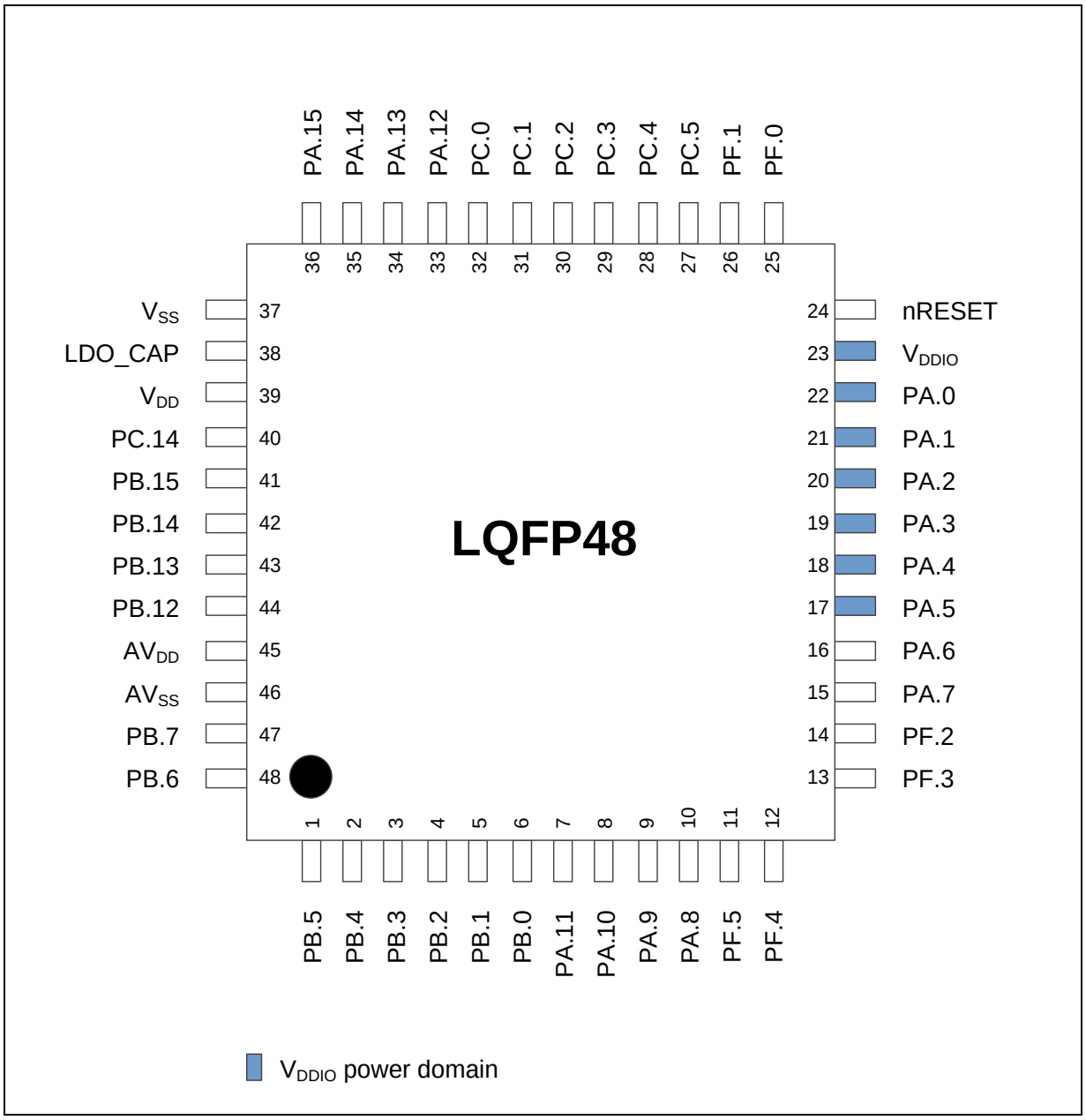



Figure 4.1-5 NuMicro® M482 USB FS OTG Series LQFP 48-pin Diagram

### 4.1.6 NuMicro® M482 USB FS OTG Series LQFP64 Pin Diagram

Corresponding Part Number: M482SGAAE, M482SIDAE

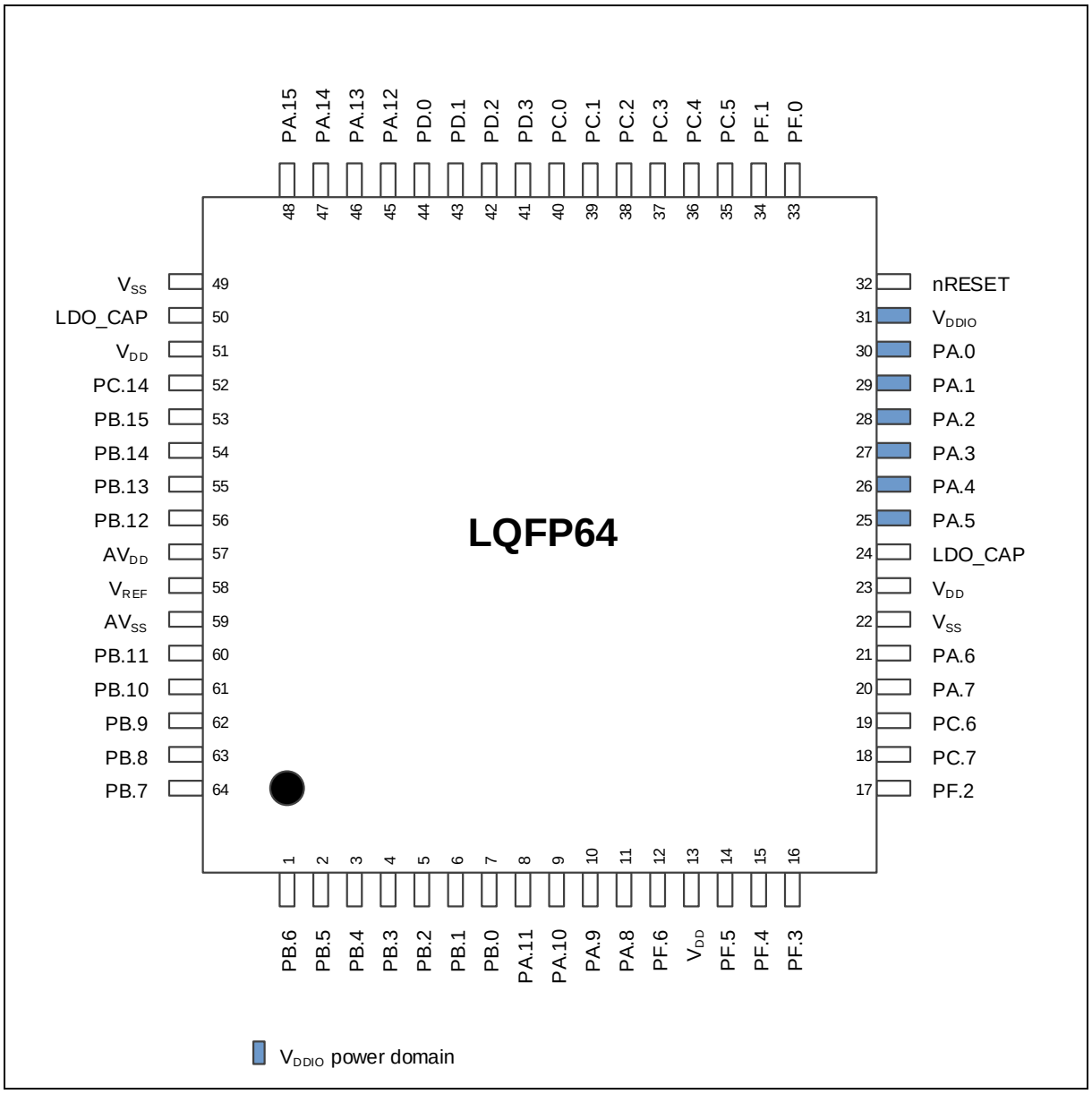



Figure 4.1-6 NuMicro® M482 USB FS OTG Series LQFP 64-pin Diagram

### 4.1.7 NuMicro® M482 USB FS OTG Series LQFP128 Pin Diagram

Corresponding Part Number: M482KGAAE, M482KIDAE

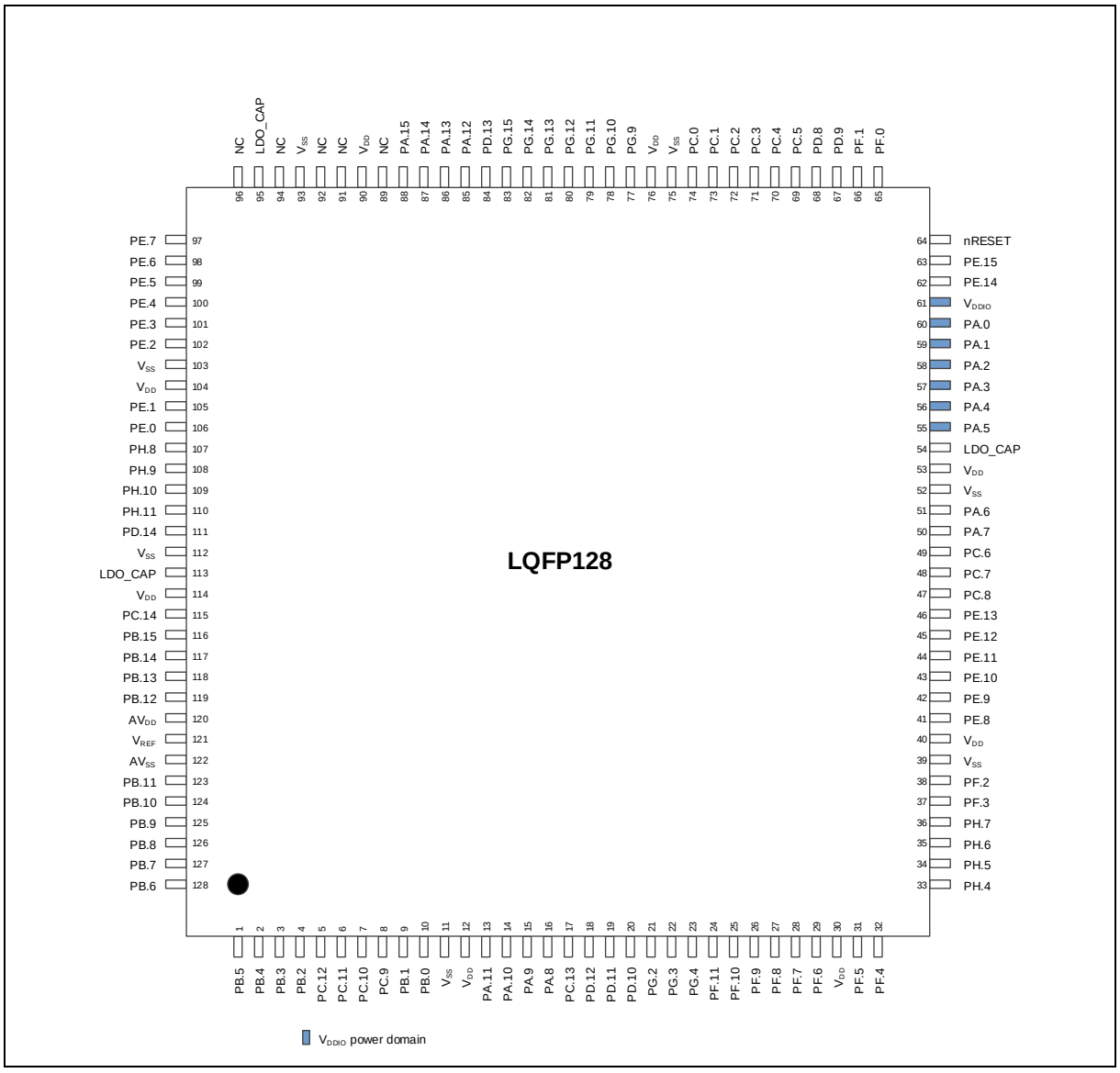



Figure 4.1-7 NuMicro® M482 USB FS OTG Series LQFP 128-pin Diagram

### 4.1.8 NuMicro® M483 CAN Series LQFP64 Pin Diagram

Corresponding Part Number: M483SGAAE, M483SIDAE

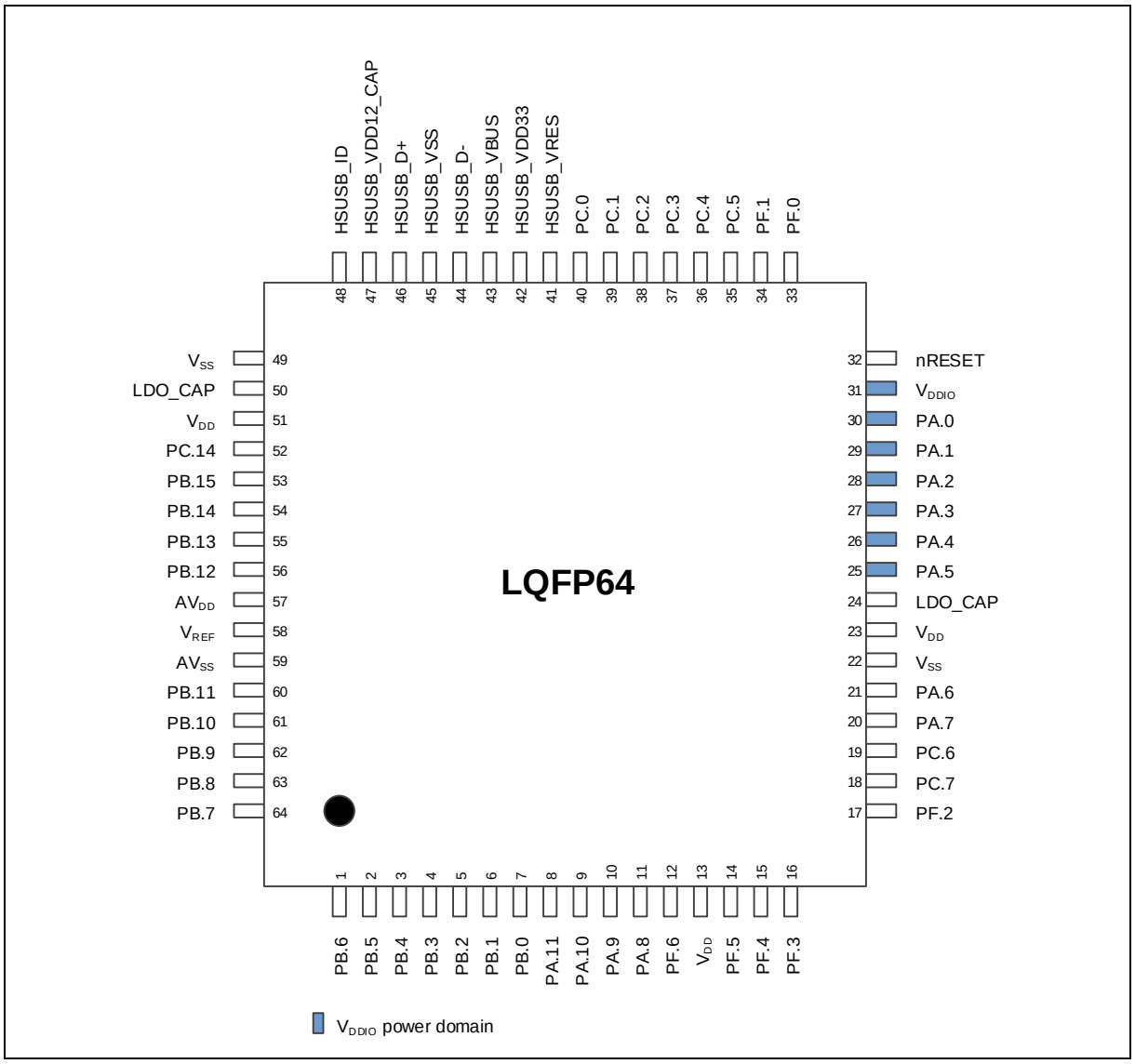



Figure 4.1-8 NuMicro® M483 CAN Series LQFP 64-pin Diagram

### 4.1.9 NuMicro® M483 CAN Series LQFP128 Pin Diagram

Corresponding Part Number: M483KIDAE

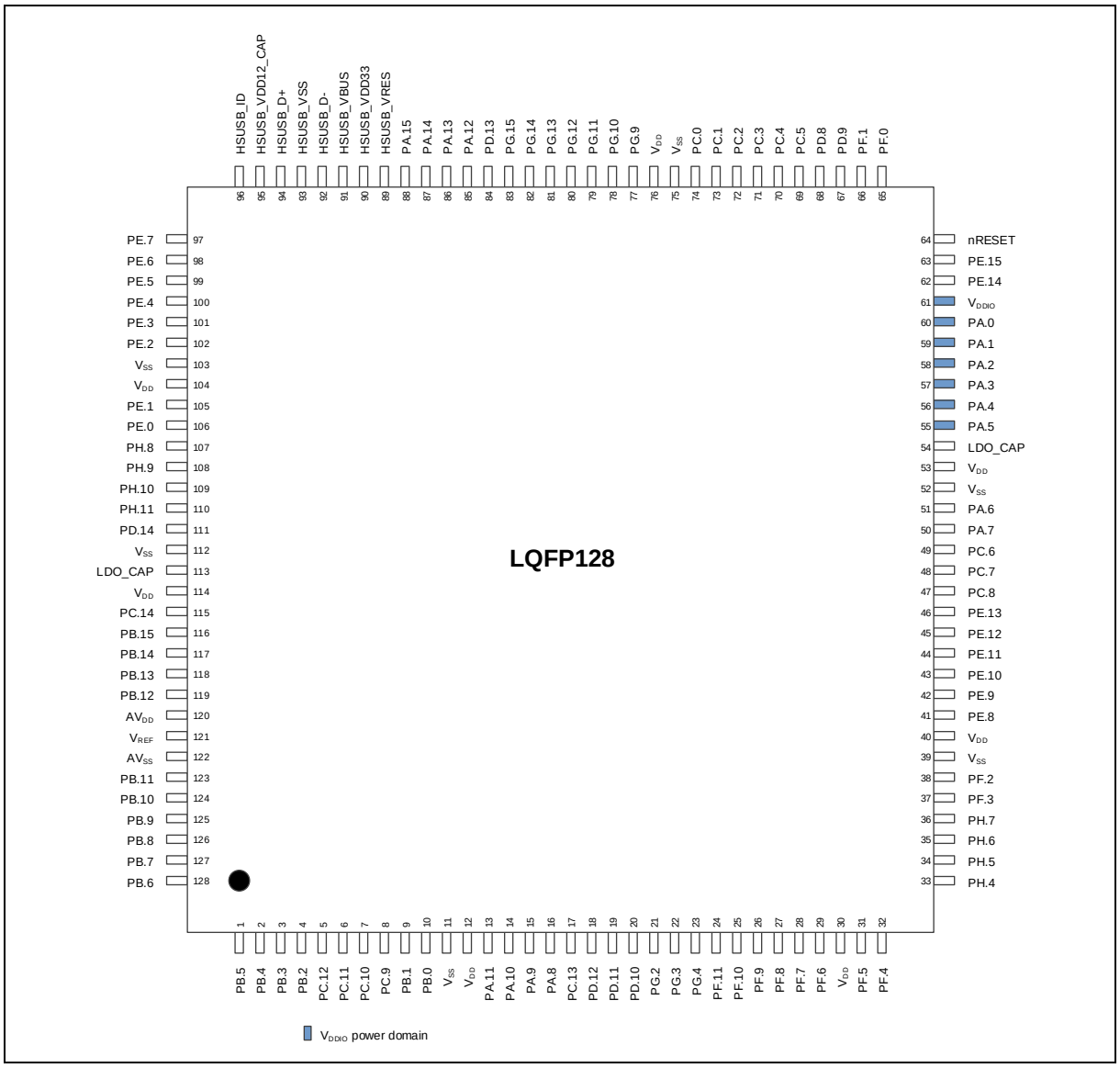



Figure 4.1-9 NuMicro® M483 CAN Series LQFP 128-pin Diagram

### 4.1.10 NuMicro® M484 USB HS OTG Series LQFP64 Pin Diagram

Corresponding Part Number: M484SGAAE, M484SIDAE

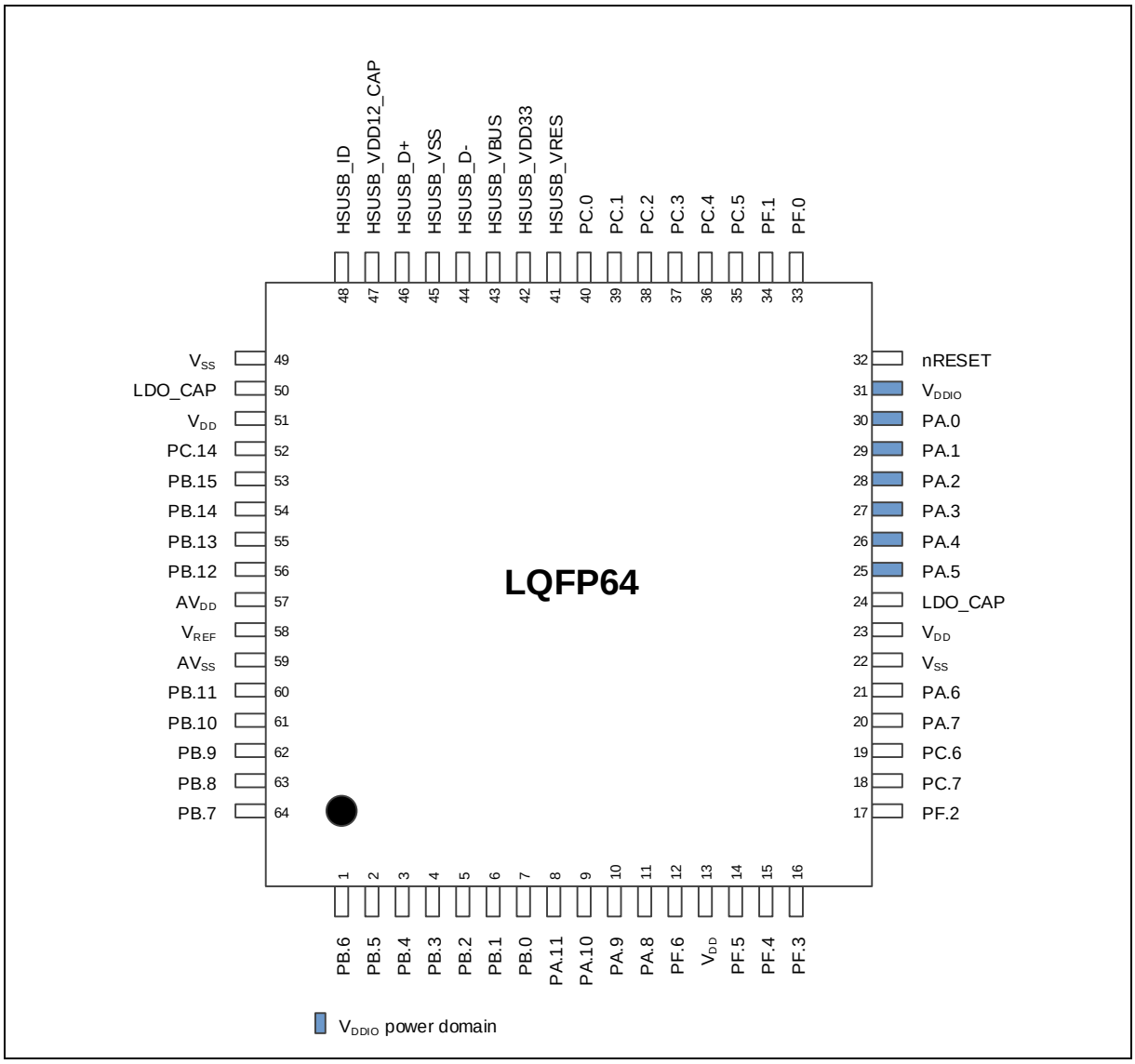



Figure 4.1-10 NuMicro® M484 USB HS OTG Series LQFP 64-pin Diagram

### 4.1.11 NuMicro® M484 USB HS OTG Series with 2 USB LQFP64 Pin Diagram

Corresponding Part Number: M484SGAAE2U, M484SIDAE2U

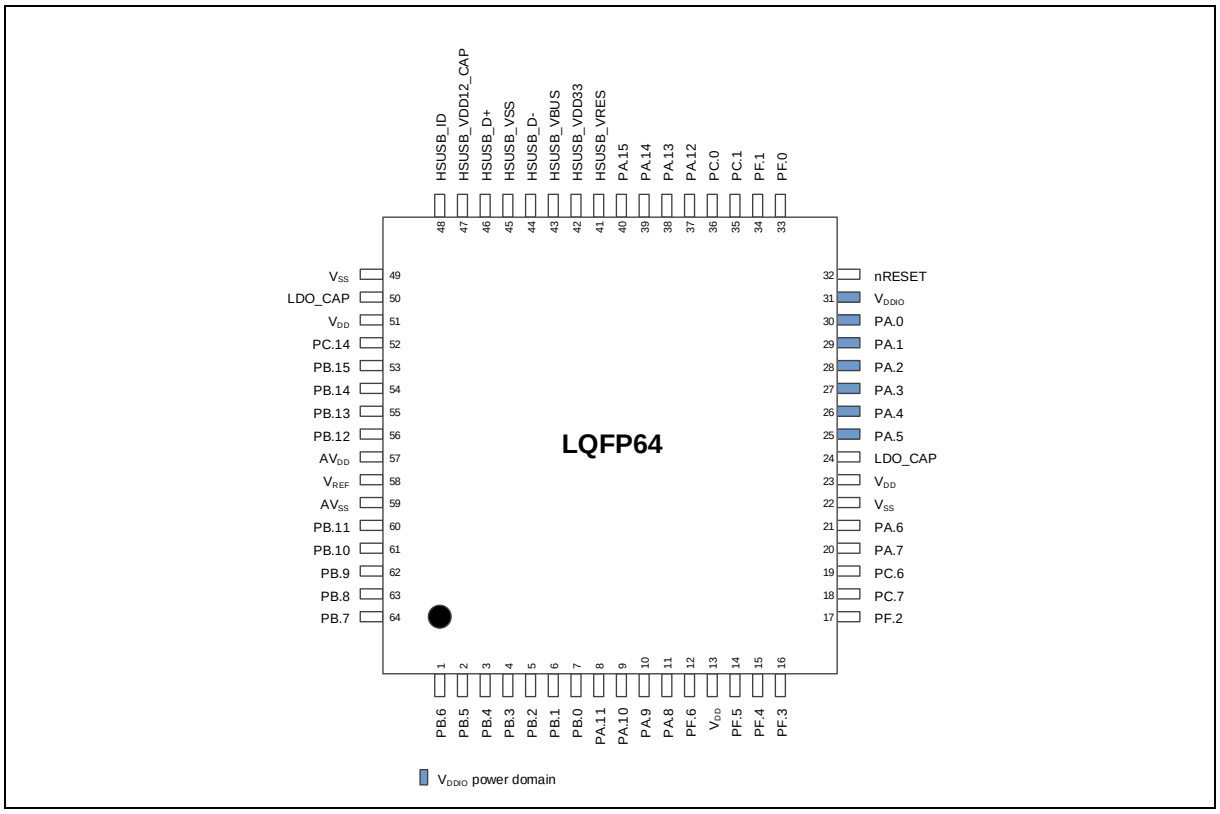



Figure 4.1-11 NuMicro® M484 USB HS OTG Series with 2 USB LQFP 64-pin Diagram

### 4.1.12 NuMicro® M484 USB HS OTG Series LQFP128 Pin Diagram

Corresponding Part Number: M484KIDAE

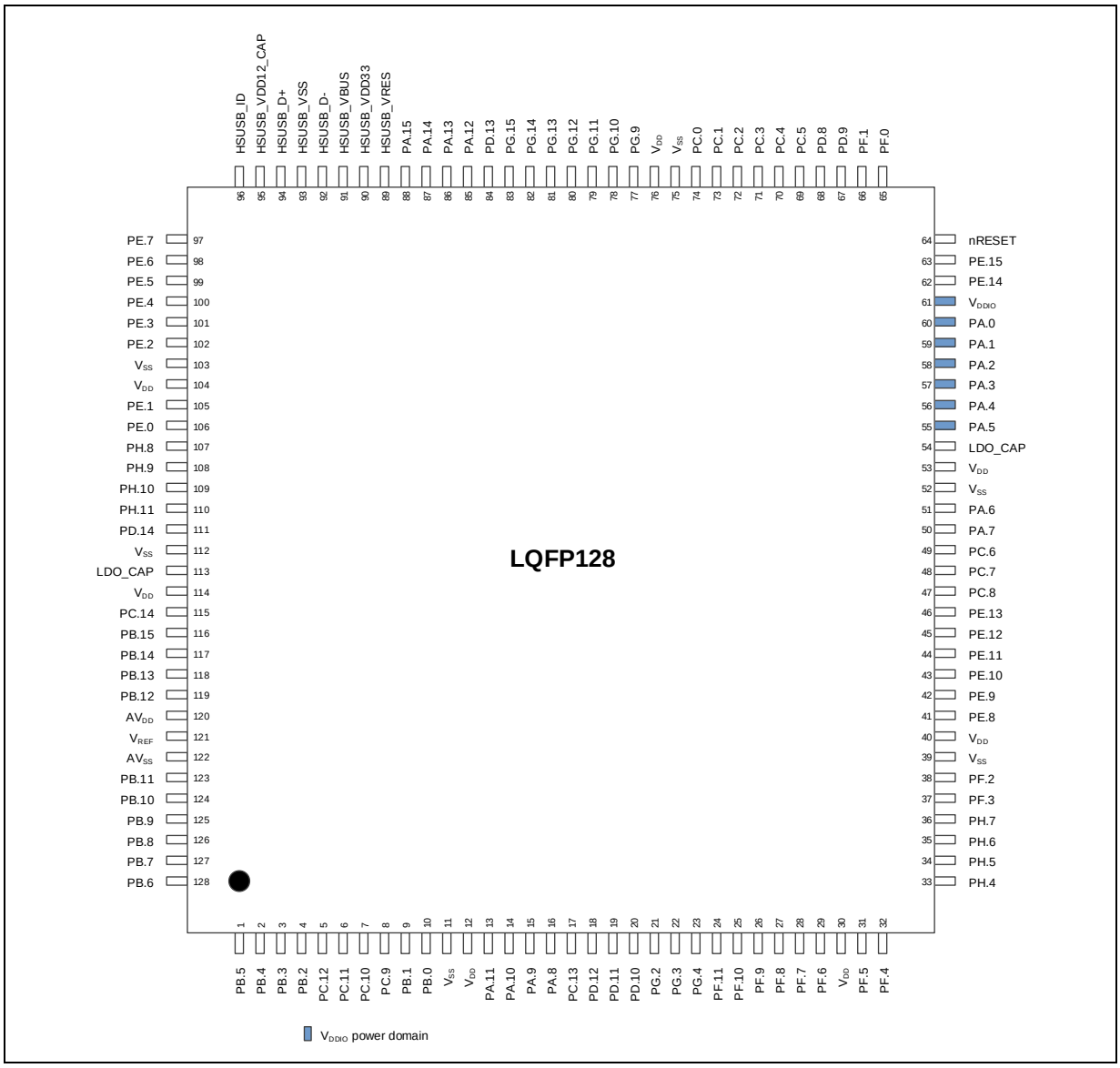



Figure 4.1-12 NuMicro® M484 USB HS OTG Series LQFP 128-pin Diagram

### 4.1.13 NuMicro® M485 Crypto Series QFN33 Pin Diagram

Corresponding Part Number: M485ZIDAE

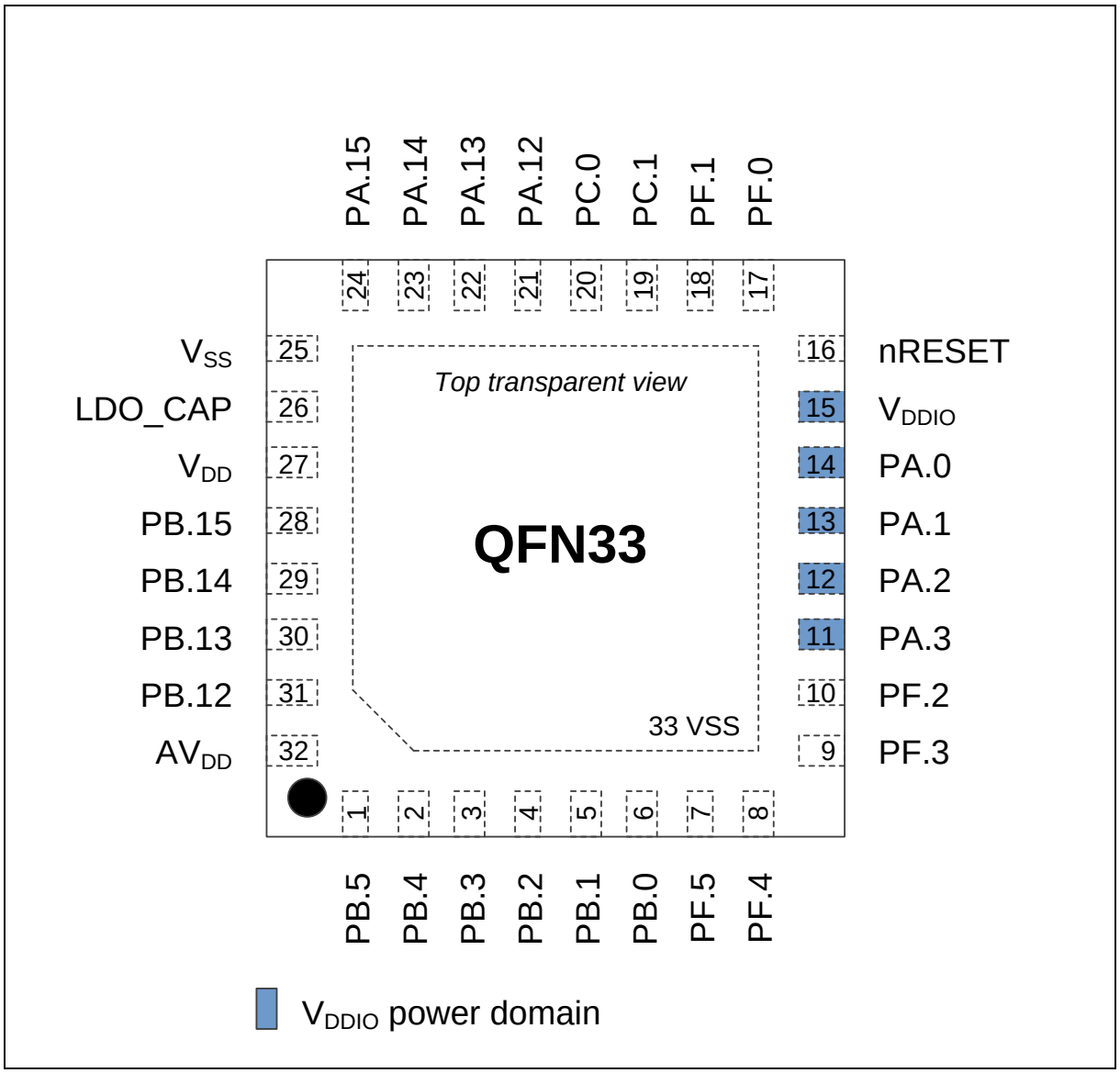



Figure 4.1-13 NuMicro® M485 Crypto Series QFN 33-pin Diagram

### 4.1.14 NuMicro® M485 Crypto Series LQFP48 Pin Diagram

Corresponding Part Number: M485LIDAE

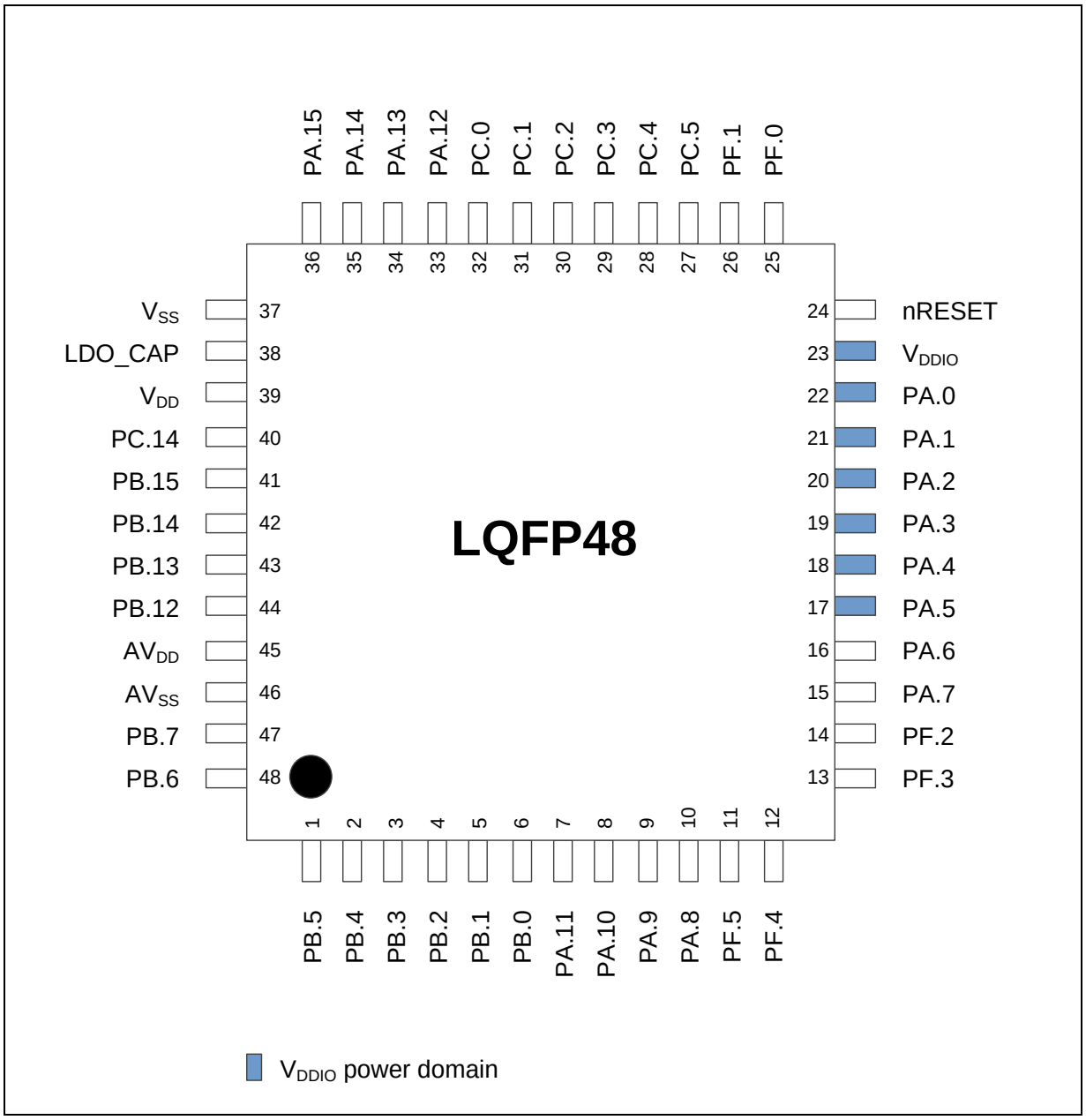



Figure 4.1-14 NuMicro® M485 Crypto Series LQFP 48-pin Diagram

### 4.1.15 NuMicro® M485 Crypto Series LQFP64 Pin Diagram

Corresponding Part Number: M485SIDAE

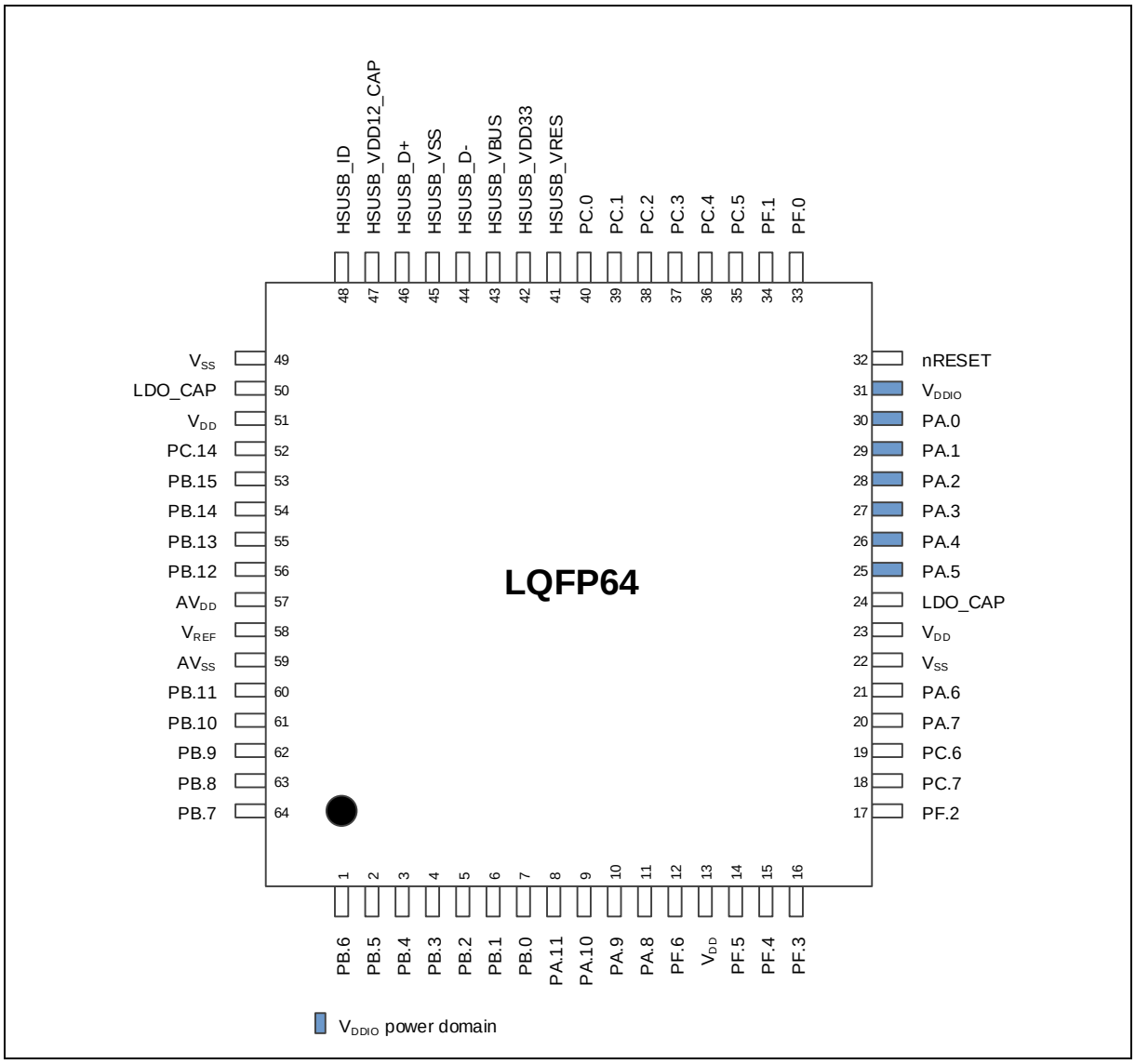



Figure 4.1-15 NuMicro® M485 Crypto Series LQFP 64-pin Diagram

### 4.1.16 NuMicro® M485 Crypto Series LQFP128 Pin Diagram

Corresponding Part Number: M485KIDAE

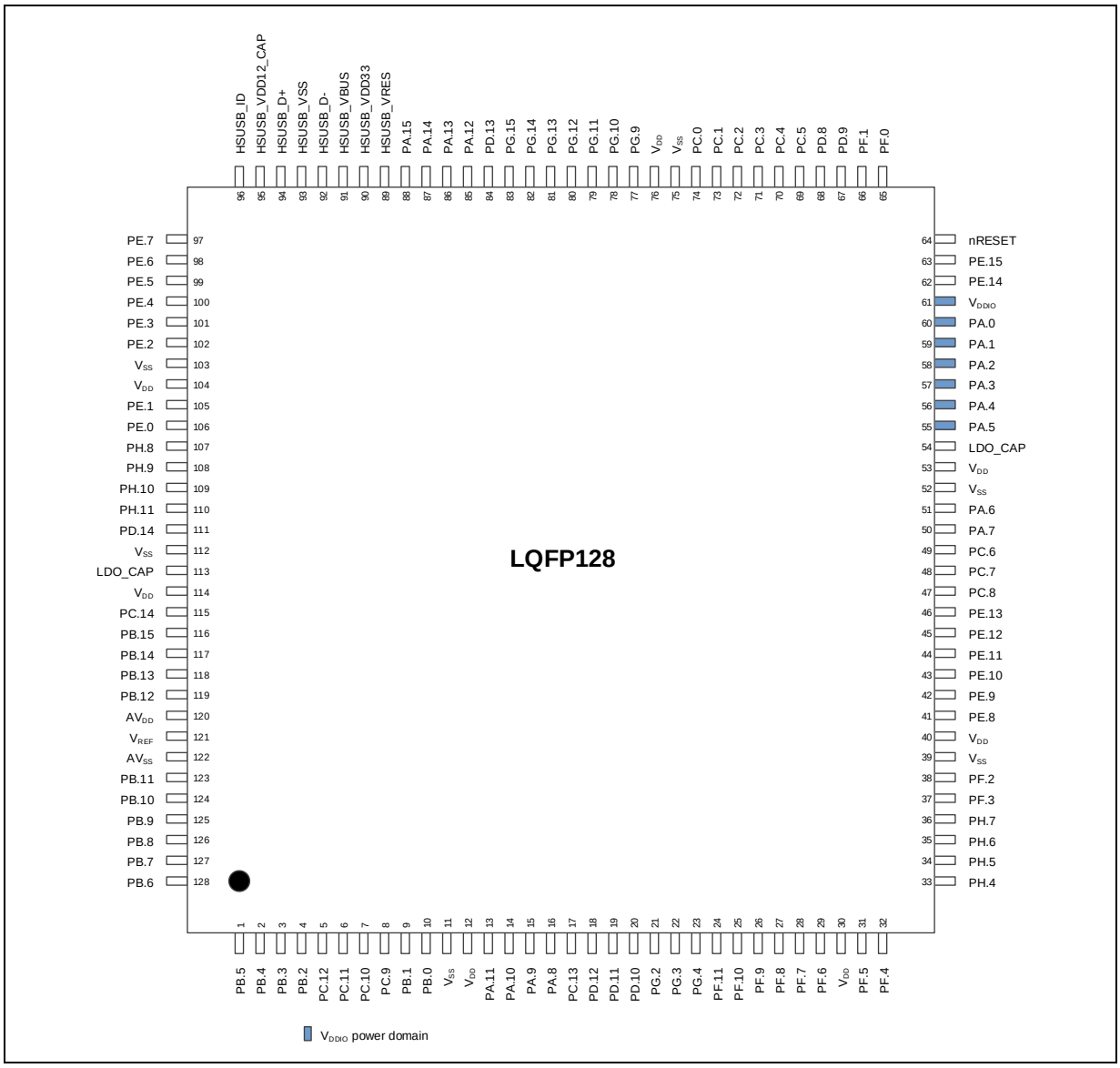



Figure 4.1-16 NuMicro® M485 Crypto Series LQFP 128-pin Diagram

### 4.1.17 NuMicro® M487 Ethernet Series LQFP64 Pin Diagram

Corresponding Part Number: M487SIDAE

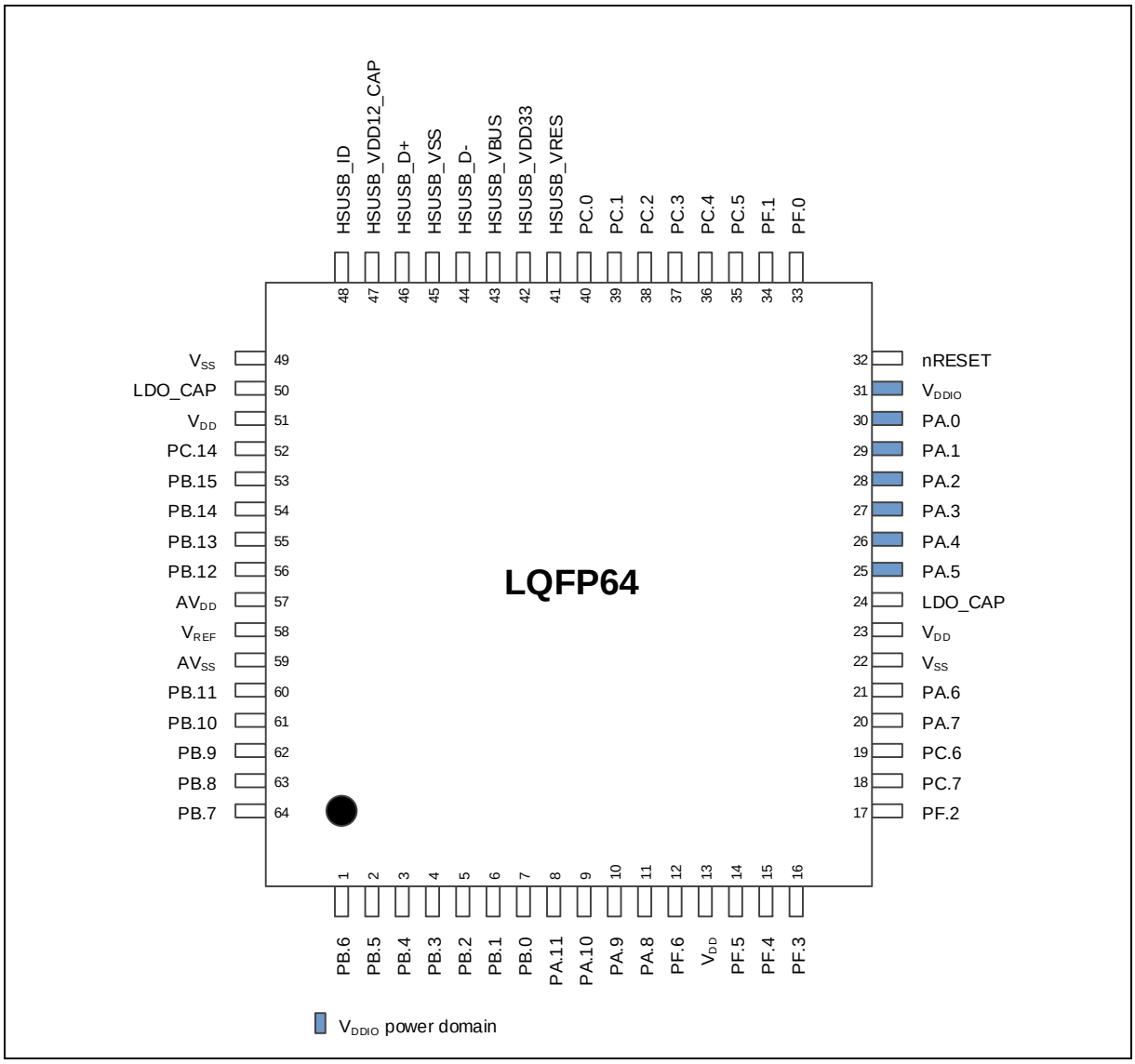



Figure 4.1-17 NuMicro® M487 Ethernet Series LQFP 64-pin Diagram

### 4.1.18 NuMicro® M487 Ethernet Series LQFP128 Pin Diagram

Corresponding Part Number: M487KIDAE

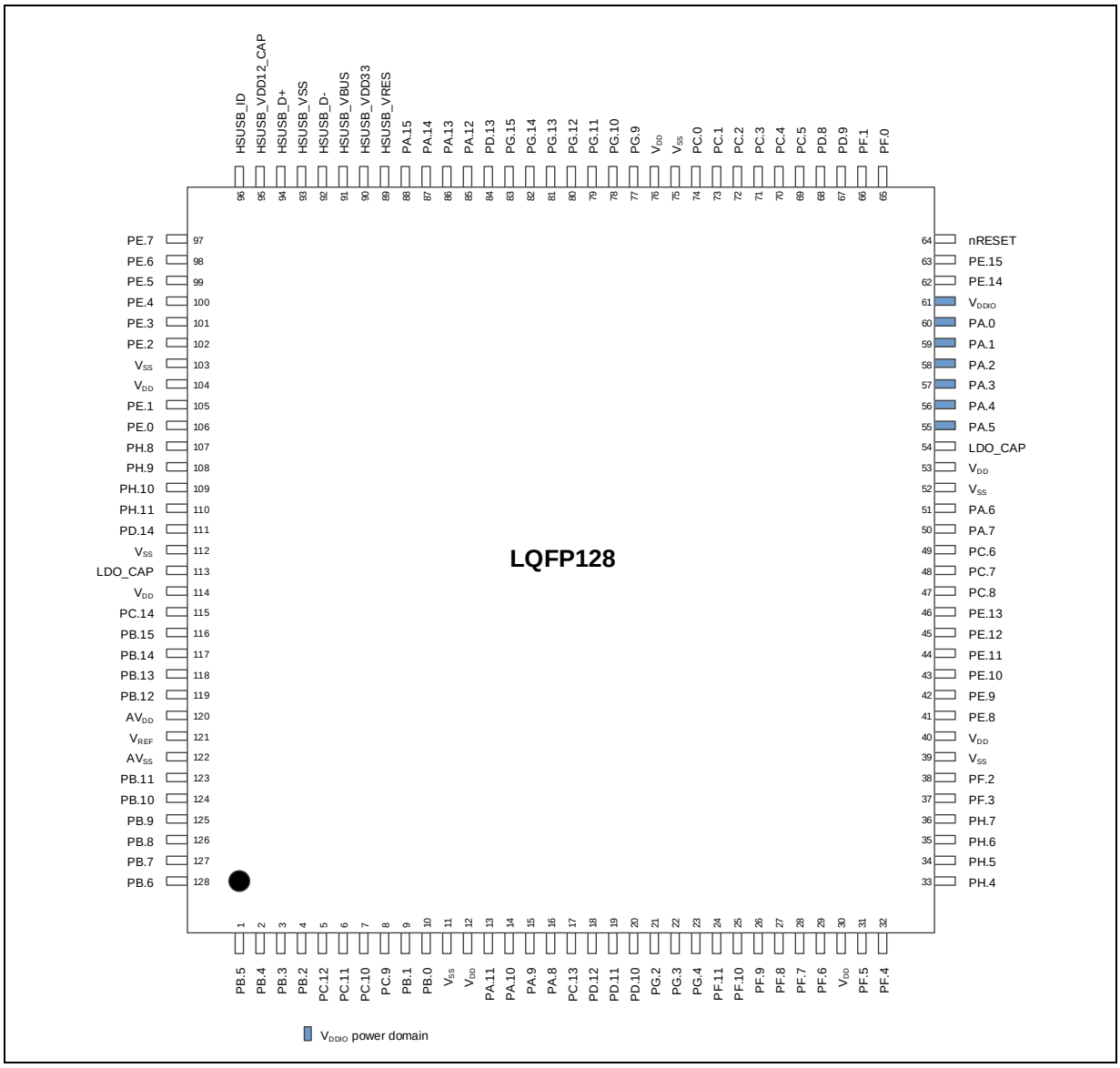



Figure 4.1-18 NuMicro® M487 Ethernet Series LQFP 128-pin Diagram

### 4.1.19 NuMicro® M487 Ethernet Series LQFP144 Pin Diagram

Corresponding Part Number: M487JIDAE

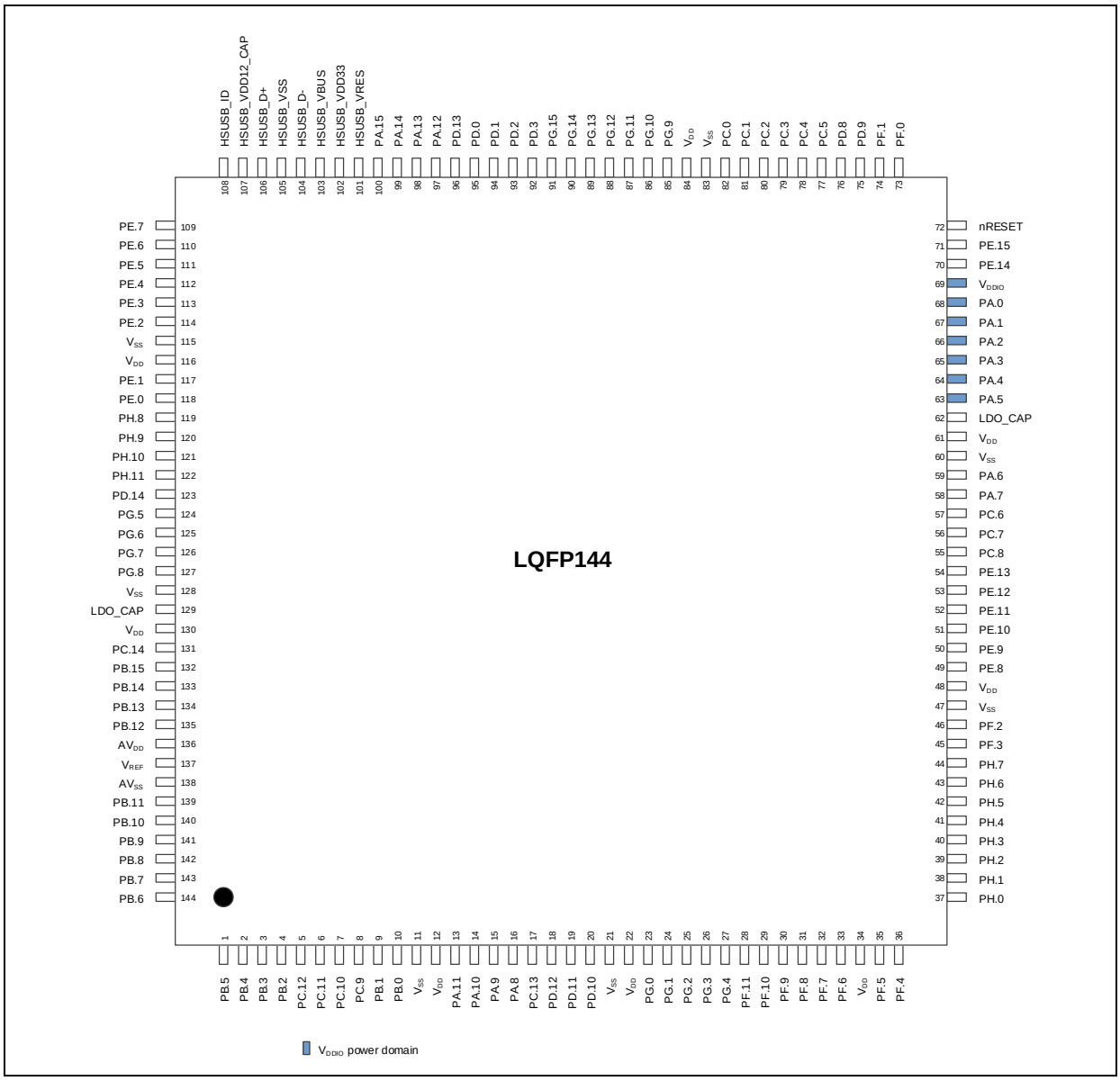



Figure 4.1-19 NuMicro® M487 Ethernet Series LQFP 144-pin Diagram

## 4.2 Pin Description

### 4.2.1 M481 Series Pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[3:0] = 0x0.

PA.9 MFP5 means SYS_GPA_MFPH[7:4] = 0x5.

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | 48 | 1 | PB.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH6 | A | MFP1 | EADC0 channel 6 analog input. |
| | | | EBI_nWRH | O | MFP2 | EBI high byte write enable output pin |
| | | | USCI1_DAT1 | I/O | MFP4 | USCI1 data 1 pin. |
| | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | SD1_CLK | O | MFP7 | SD/SDIO1 clock output pin |
| | | | EBI_nCS1 | O | MFP8 | EBI chip select 1 output pin. |
| | | | BPWM1_CH5 | I/O | MFP10 | BPWM1 channel 5 output/capture input. |
| | | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | INT4 | I | MFP13 | External interrupt 4 input pin. |
| | | | ACMP1_O | O | MFP15 | Analog comparator 1 output pin. |
| 1 | 1 | 2 | PB.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH5 | A | MFP1 | EADC0 channel 5 analog input. |
| | | | ACMP1_N | A | MFP1 | Analog comparator 1 negative input pin. |
| | | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | | SPI1_MISO | I/O | MFP5 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | I2C0_SCL | I/O | MFP6 | I2C0 clock pin. |
| | | | UART5_TXD | O | MFP7 | UART5 data transmitter output pin. |
| | | | USCI1_CTL0 | I/O | MFP8 | USCI1 control 0 pin. |
| | | | SC0_CLK | O | MFP9 | Smart Card 0 clock pin. |
| | | | I2S0_BCLK | O | MFP10 | I2S0 bit clock output pin. |
| | | | EPWM0_CH0 | I/O | MFP11 | EPWM0 channel 0 output/capture input. |
| | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| 2 | 2 | 3 | PB.4 | I/O | MFP0 | General purpose digital I/O pin. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EADC0_CH4 | A | MFP1 | EADC0 channel 4 analog input. |
| | | | ACMP1_P1 | A | MFP1 | Analog comparator 1 positive input 1 pin. |
| | | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | | SPI1_MOSI | I/O | MFP5 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | I2C0_SDA | I/O | MFP6 | I2C0 data input/output pin. |
| | | | UART5_RXD | I | MFP7 | UART5 data receiver input pin. |
| | | | USCI1_CTL1 | I/O | MFP8 | USCI1 control 1 pin. |
| | | | SC0_DAT | I/O | MFP9 | Smart Card 0 data pin. |
| | | | I2S0_MCLK | O | MFP10 | I2S0 master clock output pin. |
| | | | EPWM0_CH1 | I/O | MFP11 | EPWM0 channel 1 output/capture input. |
| | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| 3 | 3 | 4 | PB.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH3 | A | MFP1 | EADC0 channel 3 analog input. |
| | | | ACMP0_N | A | MFP1 | Analog comparator 0 negative input pin. |
| | | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | | | SPI1_CLK | I/O | MFP5 | SPI1 serial clock pin. |
| | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | UART5_nRTS | O | MFP7 | UART5 request to Send output pin. |
| | | | USCI1_DAT1 | I/O | MFP8 | USCI1 data 1 pin. |
| | | | SC0_RST | O | MFP9 | Smart Card 0 reset pin. |
| | | | I2S0_DI | I | MFP10 | I2S0 data input pin. |
| | | | EPWM0_CH2 | I/O | MFP11 | EPWM0 channel 2 output/capture input. |
| | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| 4 | 4 | 5 | PB.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH2 | A | MFP1 | EADC0 channel 2 analog input. |
| | | | ACMP0_P1 | A | MFP1 | Analog comparator 0 positive input 1 pin. |
| | | | OPA0_O | A | MFP1 | Operational amplifier 0 output pin. |
| | | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI1_SS | I/O | MFP5 | SPI1 slave select pin. |
| | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | UART5_nCTS | I | MFP7 | UART5 clear to Send input pin. |
| | | | USCI1_DAT0 | I/O | MFP8 | USCI1 data 0 pin. |
| | | | SC0_PWR | O | MFP9 | Smart Card 0 power pin. |
| | | | I2S0_DO | O | MFP10 | I2S0 data output pin. |
| | | | EPWM0_CH3 | I/O | MFP11 | EPWM0 channel 3 output/capture input. |
| | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| 5 | 5 | 6 | PB.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH1 | A | MFP1 | EADC0 channel 1 analog input. |
| | | | OPA0_N | A | MFP1 | Operational amplifier 0 negative input pin. |
| | | | EBI_ADR8 | O | MFP2 | EBI address bus bit 8. |
| | | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | | SPI3_I2SMCLK | I/O | MFP6 | SPI3 I2S master clock output pin |
| | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | USCI1_CLK | I/O | MFP8 | USCI1 clock pin. |
| | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | I2S0_LRCK | O | MFP10 | I2S0 left right channel clock output pin. |
| | | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | EPWM0_BRAKE0 | I | MFP13 | EPWM0 Brake 0 input pin. |
| 6 | 6 | 7 | PB.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH0 | A | MFP1 | EADC0 channel 0 analog input. |
| | | | OPA0_P | A | MFP1 | Operational amplifier 0 positive input pin. |
| | | | EBI_ADR9 | O | MFP2 | EBI address bus bit 9. |
| | | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | SPI0_I2SMCLK | I/O | MFP8 | SPI0 I2S master clock output pin |
| | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EPWM0_BRAKE1 | I | MFP13 | EPWM0 Brake 1 input pin. |
| | 7 | 8 | PA.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ACMP0_P0 | A | MFP1 | Analog comparator 0 positive input 0 pin. |
| | | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | | SC2_PWR | O | MFP3 | Smart Card 2 power pin. |
| | | | SPI2_SS | I/O | MFP4 | SPI2 slave select pin. |
| | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | USCI0_CLK | I/O | MFP6 | USCI0 clock pin. |
| | | | I2C2_SCL | I/O | MFP7 | I2C2 clock pin. |
| | | | BPWM0_CH0 | I/O | MFP9 | BPWM0 channel 0 output/capture input. |
| | | | EPWM0_SYNC_OUT | O | MFP10 | EPWM0 counter synchronous trigger output pin. |
| | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | | DAC1_ST | I | MFP14 | DAC1 external trigger input. |
| | 8 | 9 | PA.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ACMP1_P0 | A | MFP1 | Analog comparator 1 positive input 0 pin. |
| | | | OPA1_O | A | MFP1 | Operational amplifier 1 output pin. |
| | | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | | SC2_RST | O | MFP3 | Smart Card 2 reset pin. |
| | | | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | | USCI0_DAT0 | I/O | MFP6 | USCI0 data 0 pin. |
| | | | I2C2_SDA | I/O | MFP7 | I2C2 data input/output pin. |
| | | | BPWM0_CH1 | I/O | MFP9 | BPWM0 channel 1 output/capture input. |
| | | | QEI1_INDEX | I | MFP10 | Quadrature encoder 1 index input |
| | | | ECAP0_IC0 | I | MFP11 | Enhanced capture unit 0 input 0 pin. |
| | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | DAC0_ST | I | MFP14 | DAC0 external trigger input. |
| | 9 | 10 | PA.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA1_N | A | MFP1 | Operational amplifier 1 negative input pin. |
| | | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | | SC2_DAT | I/O | MFP3 | Smart Card 2 data pin. |
| | | | SPI2_MISO | I/O | MFP4 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | USCI0_DAT1 | I/O | MFP6 | USCI0 data 1 pin. |
| | | | UART1_TXD | O | MFP7 | UART1 data transmitter output pin. |
| | | | BPWM0_CH2 | I/O | MFP9 | BPWM0 channel 2 output/capture input. |
| | | | QEI1_A | I | MFP10 | Quadrature encoder 1 phase A input |
| | | | ECAP0_IC1 | I | MFP11 | Enhanced capture unit 0 input 1 pin. |
| | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| | 10 | 11 | PA.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA1_P | A | MFP1 | Operational amplifier 1 positive input pin. |
| | | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | | SC2_CLK | O | MFP3 | Smart Card 2 clock pin. |
| | | | SPI2_MOSI | I/O | MFP4 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | | USCI0_CTL1 | I/O | MFP6 | USCI0 control 1 pin. |
| | | | UART1_RXD | I | MFP7 | UART1 data receiver input pin. |
| | | | BPWM0_CH3 | I/O | MFP9 | BPWM0 channel 3 output/capture input. |
| | | | QEI1_B | I | MFP10 | Quadrature encoder 1 phase B input |
| | | | ECAP0_IC2 | I | MFP11 | Enhanced capture unit 0 input 2 pin. |
| | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| | | | INT4 | I | MFP15 | External interrupt 4 input pin. |
| | | 12 | PF.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | | SC0_CLK | O | MFP3 | Smart Card 0 clock pin. |
| | | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | | SPI0_MOSI | I/O | MFP5 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | EBI_nCS0 | O | MFP7 | EBI chip select 0 output pin. |
| | | | TAMPER0 | I/O | MFP10 | TAMPER detector loop pin 0. |
| | | 13 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 7 | 11 | 14 | PF.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART2_RXD | I | MFP2 | UART2 data receiver input pin. |
| | | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | | | BPWM0_CH4 | I/O | MFP8 | BPWM0 channel 4 output/capture input. |
| | | | EPWM0_SYNC_OUT | O | MFP9 | EPWM0 counter synchronous trigger output pin. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | X32_IN | I | MFP10 | External 32.768 kHz crystal input pin. |
| | | | EADC0_ST | I | MFP11 | EADC0 external trigger input. |
| 8 | 12 | 15 | PF.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART2_TXD | O | MFP2 | UART2 data transmitter output pin. |
| | | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| | | | BPWM0_CH5 | I/O | MFP8 | BPWM0 channel 5 output/capture input. |
| | | | X32_OUT | O | MFP10 | External 32.768 kHz crystal output pin. |
| 9 | 13 | 16 | PF.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | XT1_IN | I | MFP10 | External 4~24 MHz (high speed) crystal input pin. |
| | | | BPWM1_CH0 | I/O | MFP11 | BPWM1 channel 0 output/capture input. |
| 10 | 14 | 17 | PF.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | QSPI0_CLK | I/O | MFP5 | Quad SPI0 serial clock pin. |
| | | | XT1_OUT | O | MFP10 | External 4~24 MHz (high speed) crystal output pin. |
| | | | BPWM1_CH1 | I/O | MFP11 | BPWM1 channel 1 output/capture input. |
| | | 18 | PC.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | | SPI1_MISO | I/O | MFP4 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | UART4_TXD | O | MFP5 | UART4 data transmitter output pin. |
| | | | SC2_PWR | O | MFP6 | Smart Card 2 power pin. |
| | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| | | 19 | PC.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI1_MOSI | I/O | MFP4 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | UART4_RXD | I | MFP5 | UART4 data receiver input pin. |
| | | | SC2_RST | O | MFP6 | Smart Card 2 reset pin. |
| | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| | 15 | 20 | PA.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | | SPI1_CLK | I/O | MFP4 | SPI1 serial clock pin. |
| | | | SC2_DAT | I/O | MFP6 | Smart Card 2 data pin. |
| | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | | EPWM1_CH4 | I/O | MFP11 | EPWM1 channel 4 output/capture input. |
| | | | BPWM1_CH2 | I/O | MFP12 | BPWM1 channel 2 output/capture input. |
| | | | ACMP0_WLAT | I | MFP13 | Analog comparator 0 window latch input pin |
| | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| | 16 | 21 | PA.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | | SPI1_SS | I/O | MFP4 | SPI1 slave select pin. |
| | | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | | | SC2_CLK | O | MFP6 | Smart Card 2 clock pin. |
| | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | | EPWM1_CH5 | I/O | MFP11 | EPWM1 channel 5 output/capture input. |
| | | | BPWM1_CH3 | I/O | MFP12 | BPWM1 channel 3 output/capture input. |
| | | | ACMP1_WLAT | I | MFP13 | Analog comparator 1 window latch input pin |
| | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| | | 22 | VSS | P | MFP0 | Ground pin for digital circuit. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | 23 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | 24 | LDO_CAP | A | MFP0 | LDO output pin. |
| | 17 | 25 | PA.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_D2 | I/O | MFP2 | SPIM data 2 pin for Quad Mode I/O. |
| | | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | SPI1_I2SMCLK | I/O | MFP4 | SPI1 I2S master clock output pin |
| | | | SD1_CMD | I/O | MFP5 | SD/SDIO1 command/response pin |
| | | | SC2_nCD | I | MFP6 | Smart Card 2 card detect pin. |
| | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | | | EPWM0_CH0 | I/O | MFP13 | EPWM0 channel 0 output/capture input. |
| | | | QEI0_INDEX | I | MFP14 | Quadrature encoder 0 index input |
| | 18 | 26 | PA.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_D3 | I/O | MFP2 | SPIM data 3 pin for Quad Mode I/O. |
| | | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | SD1_CLK | O | MFP5 | SD/SDIO1 clock output pin |
| | | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | | | EPWM0_CH1 | I/O | MFP13 | EPWM0 channel 1 output/capture input. |
| | | | QEI0_A | I | MFP14 | Quadrature encoder 0 phase A input |
| 11 | 19 | 27 | PA.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_SS | I/O | MFP2 | SPIM slave select pin. |
| | | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | | | EPWM0_CH2 | I/O | MFP13 | EPWM0 channel 2 output/capture input. |
| | | | QEI0_B | I | MFP14 | Quadrature encoder 0 phase B input |
| 12 | 20 | 28 | PA.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_CLK | I/O | MFP2 | SPIM serial clock pin. |
| | | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | | | EPWM0_CH3 | I/O | MFP13 | EPWM0 channel 3 output/capture input. |
| 13 | 21 | 29 | PA.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_MISO | I/O | MFP2 | SPIM MISO (Master In, Slave Out) pin. |
| | | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | | | EPWM0_CH4 | I/O | MFP13 | EPWM0 channel 4 output/capture input. |
| | | | DAC1_ST | I | MFP15 | DAC1 external trigger input. |
| 14 | 22 | 30 | PA.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_MOSI | I/O | MFP2 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | | | EPWM0_CH5 | I/O | MFP13 | EPWM0 channel 5 output/capture input. |
| | | | DAC0_ST | I | MFP15 | DAC0 external trigger input. |
| 15 | 23 | 31 | VDDIO | P | MFP0 | Power supply for PA.0~PA.5. |
| 16 | 24 | 32 | nRESET | I | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 17 | 25 | 33 | PF.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_TXD | O | MFP2 | UART1 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP3 | I2C1 clock pin. |
| | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | ICE_DAT | O | MFP14 | Serial wired debugger data pin. |
| 18 | 26 | 34 | PF.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_RXD | I | MFP2 | UART1 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP3 | I2C1 data input/output pin. |
| | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | ICE_CLK | I | MFP14 | Serial wired debugger clock pin. |
| | 27 | 35 | PC.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | | | SPIM_D2 | I/O | MFP3 | SPIM data 2 pin for Quad Mode I/O. |
| | | | QSPI0_MISO1 | I/O | MFP4 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | UART4_TXD | O | MFP11 | UART4 data transmitter output pin. |
| | | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| | 28 | 36 | PC.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | | SPIM_D3 | I/O | MFP3 | SPIM data 3 pin for Quad Mode I/O. |
| | | | QSPI0_MOSI1 | I/O | MFP4 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | SC1_nCD | I | MFP5 | Smart Card 1 card detect pin. |
| | | | I2S0_BCLK | O | MFP6 | I2S0 bit clock output pin. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI1_I2SMCLK | I/O | MFP7 | SPI1 I2S master clock output pin |
| | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | UART4_RXD | I | MFP11 | UART4 data receiver input pin. |
| | | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| | 29 | 37 | PC.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | | SPIM_SS | I/O | MFP3 | SPIM slave select pin. |
| | | | QSPI0_SS | I/O | MFP4 | Quad SPI0 slave select pin. |
| | | | SC1_PWR | O | MFP5 | Smart Card 1 power pin. |
| | | | I2S0_MCLK | O | MFP6 | I2S0 master clock output pin. |
| | | | SPI1_MISO | I/O | MFP7 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | UART2_nRTS | O | MFP8 | UART2 request to Send output pin. |
| | | | I2C0_SMBAL | O | MFP9 | I2C0 SMBus SMBALTER pin |
| | | | UART3_TXD | O | MFP11 | UART3 data transmitter output pin. |
| | | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| | 30 | 38 | PC.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | | SPIM_CLK | I/O | MFP3 | SPIM serial clock pin. |
| | | | QSPI0_CLK | I/O | MFP4 | Quad SPI0 serial clock pin. |
| | | | SC1_RST | O | MFP5 | Smart Card 1 reset pin. |
| | | | I2S0_DI | I | MFP6 | I2S0 data input pin. |
| | | | SPI1_MOSI | I/O | MFP7 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | UART2_nCTS | I | MFP8 | UART2 clear to Send input pin. |
| | | | I2C0_SMBSUS | O | MFP9 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | UART3_RXD | I | MFP11 | UART3 data receiver input pin. |
| | | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 19 | 31 | 39 | PC.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | | SPIM_MISO | I/O | MFP3 | SPIM MISO (Master In, Slave Out) pin. |
| | | | QSPI0_MISO0 | I/O | MFP4 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | SC1_DAT | I/O | MFP5 | Smart Card 1 data pin. |
| | | | I2S0_DO | O | MFP6 | I2S0 data output pin. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI1_CLK | I/O | MFP7 | SPI1 serial clock pin. |
| | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| 20 | 32 | 40 | PC.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | | SPIM_MOSI | I/O | MFP3 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | QSPI0_MOSI0 | I/O | MFP4 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | SC1_CLK | O | MFP5 | Smart Card 1 clock pin. |
| | | | I2S0_LRCK | O | MFP6 | I2S0 left right channel clock output pin. |
| | | | SPI1_SS | I/O | MFP7 | SPI1 slave select pin. |
| | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | | 41 | PD.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | USCI0_CTL1 | I/O | MFP3 | USCI0 control 1 pin. |
| | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | UART3_nRTS | O | MFP5 | UART3 request to Send output pin. |
| | | | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |
| | | | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | | | SC1_nCD | I | MFP8 | Smart Card 1 card detect pin. |
| | | | UART0_TXD | O | MFP9 | UART0 data transmitter output pin. |
| | | 42 | PD.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | USCI0_DAT1 | I/O | MFP3 | USCI0 data 1 pin. |
| | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | UART3_nCTS | I | MFP5 | UART3 clear to Send input pin. |
| | | | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | | | UART0_RXD | I | MFP9 | UART0 data receiver input pin. |
| | | 43 | PD.1 | I/O | MFP0 | General purpose digital I/O pin. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | USCI0_DAT0 | I/O | MFP3 | USCI0 data 0 pin. |
| | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | UART3_TXD | O | MFP5 | UART3 data transmitter output pin. |
| | | | I2C2_SCL | I/O | MFP6 | I2C2 clock pin. |
| | | | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | | 44 | PD.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | USCI0_CLK | I/O | MFP3 | USCI0 clock pin. |
| | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | UART3_RXD | I | MFP5 | UART3 data receiver input pin. |
| | | | I2C2_SDA | I/O | MFP6 | I2C2 data input/output pin. |
| | | | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| 21 | 33 | 45 | PA.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_BCLK | O | MFP2 | I2S0 bit clock output pin. |
| | | | UART4_TXD | O | MFP3 | UART4 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP4 | I2C1 clock pin. |
| | | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | | | BPWM1_CH2 | I/O | MFP11 | BPWM1 channel 2 output/capture input. |
| | | | QEI1_INDEX | I | MFP12 | Quadrature encoder 1 index input |
| 22 | 34 | 46 | PA.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_MCLK | O | MFP2 | I2S0 master clock output pin. |
| | | | UART4_RXD | I | MFP3 | UART4 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP4 | I2C1 data input/output pin. |
| | | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | | | BPWM1_CH3 | I/O | MFP11 | BPWM1 channel 3 output/capture input. |
| | | | QEI1_A | I | MFP12 | Quadrature encoder 1 phase A input |
| 23 | 35 | 47 | PA.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_DI | I | MFP2 | I2S0 data input pin. |
| | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | I2C2_SCL | I/O | MFP6 | I2C2 clock pin. |
| | | | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | | | BPWM1_CH4 | I/O | MFP11 | BPWM1 channel 4 output/capture input. |
| | | | QEI1_B | I | MFP12 | Quadrature encoder 1 phase B input |
| 24 | 36 | 48 | PA.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_DO | O | MFP2 | I2S0 data output pin. |
| | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | I2C2_SDA | I/O | MFP6 | I2C2 data input/output pin. |
| | | | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | | | BPWM1_CH5 | I/O | MFP11 | BPWM1 channel 5 output/capture input. |
| | | | EPWM0_SYNC_IN | I | MFP12 | EPWM0 counter synchronous trigger input pin. |
| 25 | 37 | 49 | VSS | P | MFP0 | Ground pin for digital circuit. |
| 26 | 38 | 50 | LDO_CAP | A | MFP0 | LDO output pin. |
| 27 | 39 | 51 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 40 | 52 | PC.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | SC1_nCD | I | MFP3 | Smart Card 1 card detect pin. |
| | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | USCI0_CTL0 | I/O | MFP5 | USCI0 control 0 pin. |
| | | | QSPI0_CLK | I/O | MFP6 | Quad SPI0 serial clock pin. |
| | | | EPWM0_SYNC_IN | I | MFP11 | EPWM0 counter synchronous trigger input pin. |
| | | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| 28 | 41 | 53 | PB.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH15 | A | MFP1 | EADC0 channel 15 analog input. |
| | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | SC1_PWR | O | MFP3 | Smart Card 1 power pin. |
| | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | USCI0_CTL1 | I/O | MFP5 | USCI0 control 1 pin. |
| | | | UART0_nCTS | I | MFP6 | UART0 clear to Send input pin. |
| | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | I2C2_SMBAL | O | MFP8 | I2C2 SMBus SMBALTER pin |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| 29 | 42 | 54 | PB.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH14 | A | MFP1 | EADC0 channel 14 analog input. |
| | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | SC1_RST | O | MFP3 | Smart Card 1 reset pin. |
| | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | USCI0_DAT1 | I/O | MFP5 | USCI0 data 1 pin. |
| | | | UART0_nRTS | O | MFP6 | UART0 request to Send output pin. |
| | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | I2C2_SMBSUS | O | MFP8 | I2C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | CLKO | O | MFP14 | Clock Out |
| 30 | 43 | 55 | PB.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH13 | A | MFP1 | EADC0 channel 13 analog input. |
| | | | DAC1_OUT | A | MFP1 | DAC1 channel analog output. |
| | | | ACMP0_P3 | A | MFP1 | Analog comparator 0 positive input 3 pin. |
| | | | ACMP1_P3 | A | MFP1 | Analog comparator 1 positive input 3 pin. |
| | | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | | SC1_DAT | I/O | MFP3 | Smart Card 1 data pin. |
| | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | USCI0_DAT0 | I/O | MFP5 | USCI0 data 0 pin. |
| | | | UART0_TXD | O | MFP6 | UART0 data transmitter output pin. |
| | | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | | I2C2_SCL | I/O | MFP8 | I2C2 clock pin. |
| | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| 31 | 44 | 56 | PB.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH12 | A | MFP1 | EADC0 channel 12 analog input. |
| | | | DAC0_OUT | A | MFP1 | DAC0 channel analog output. |
| | | | ACMP0_P2 | A | MFP1 | Analog comparator 0 positive input 2 pin. |
| | | | ACMP1_P2 | A | MFP1 | Analog comparator 1 positive input 2 pin. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | | | SC1_CLK | O | MFP3 | Smart Card 1 clock pin. |
| | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | USCI0_CLK | I/O | MFP5 | USCI0 clock pin. |
| | | | UART0_RXD | I | MFP6 | UART0 data receiver input pin. |
| | | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | | I2C2_SDA | I/O | MFP8 | I2C2 data input/output pin. |
| | | | SD0_nCD | I | MFP9 | SD/SDIO0 card detect input pin |
| | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| 32 | 45 | 57 | $AV_{DD}$ | P | MFP0 | Power supply for internal analog circuit. |
| | | 58 | $V_{REF}$ | A | MFP0 | ADC reference voltage input.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| | 46 | 59 | AVSS | P | MFP0 | Ground pin for analog circuit. |
| | | 60 | PB.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH11 | A | MFP1 | EADC0 channel 11 analog input. |
| | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | UART0_nCTS | I | MFP5 | UART0 clear to Send input pin. |
| | | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP7 | I2C1 clock pin. |
| | | | SPI0_I2SMCLK | I/O | MFP9 | SPI0 I2S master clock output pin |
| | | | BPWM1_CH0 | I/O | MFP10 | BPWM1 channel 0 output/capture input. |
| | | | SPI3_CLK | I/O | MFP11 | SPI3 serial clock pin. |
| | | 61 | PB.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH10 | A | MFP1 | EADC0 channel 10 analog input. |
| | | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | | USCI1_CTL0 | I/O | MFP4 | USCI1 control 0 pin. |
| | | | UART0_nRTS | O | MFP5 | UART0 request to Send output pin. |
| | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP7 | I2C1 data input/output pin. |
| | | | BPWM1_CH1 | I/O | MFP10 | BPWM1 channel 1 output/capture input. |
| | | | SPI3_SS | I/O | MFP11 | SPI3 slave select pin. |
| | | 62 | PB.9 | I/O | MFP0 | General purpose digital I/O pin. |

| 32 Pin | 48 Pin | 64 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EADC0_CH9 | A | MFP1 | EADC0 channel 9 analog input. |
| | | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | | USCI1_CTL1 | I/O | MFP4 | USCI1 control 1 pin. |
| | | | UART0_TXD | O | MFP5 | UART0 data transmitter output pin. |
| | | | UART1_nCTS | I | MFP6 | UART1 clear to Send input pin. |
| | | | I2C1_SMBAL | O | MFP7 | I2C1 SMBus SMBALTER pin |
| | | | BPWM1_CH2 | I/O | MFP10 | BPWM1 channel 2 output/capture input. |
| | | | SPI3_MISO | I/O | MFP11 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | INT7 | I | MFP13 | External interrupt 7 input pin. |
| | | 63 | PB.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH8 | A | MFP1 | EADC0 channel 8 analog input. |
| | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | | USCI1_CLK | I/O | MFP4 | USCI1 clock pin. |
| | | | UART0_RXD | I | MFP5 | UART0 data receiver input pin. |
| | | | UART1_nRTS | O | MFP6 | UART1 request to Send output pin. |
| | | | I2C1_SMBSUS | O | MFP7 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | BPWM1_CH3 | I/O | MFP10 | BPWM1 channel 3 output/capture input. |
| | | | SPI3_MOSI | I/O | MFP11 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | INT6 | I | MFP13 | External interrupt 6 input pin. |
| | 47 | 64 | PB.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH7 | A | MFP1 | EADC0 channel 7 analog input. |
| | | | EBI_nWRL | O | MFP2 | EBI low byte write enable output pin. |
| | | | USCI1_DAT0 | I/O | MFP4 | USCI1 data 0 pin. |
| | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | SD1_CMD | I/O | MFP7 | SD/SDIO1 command/response pin |
| | | | EBI_nCS0 | O | MFP8 | EBI chip select 0 output pin. |
| | | | BPWM1_CH4 | I/O | MFP10 | BPWM1 channel 4 output/capture input. |
| | | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | INT5 | I | MFP13 | External interrupt 5 input pin. |
| | | | ACMP0_O | O | MFP15 | Analog comparator 0 output pin. |

### 4.2.2 M482 Series Pin Description

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 2 | 1 | PB.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH5 | A | MFP1 | EADC0 channel 5 analog input. |
| | | | | ACMP1_N | A | MFP1 | Analog comparator 1 negative input pin. |
| | | | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | | | SPI1_MISO | I/O | MFP5 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | | I2C0_SCL | I/O | MFP6 | I2C0 clock pin. |
| | | | | UART5_TXD | O | MFP7 | UART5 data transmitter output pin. |
| | | | | USCI1_CTL0 | I/O | MFP8 | USCI1 control 0 pin. |
| | | | | SC0_CLK | O | MFP9 | Smart Card 0 clock pin. |
| | | | | I2S0_BCLK | O | MFP10 | I2S0 bit clock output pin. |
| | | | | EPWM0_CH0 | I/O | MFP11 | EPWM0 channel 0 output/capture input. |
| | | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| 2 | 2 | 3 | 2 | PB.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH4 | A | MFP1 | EADC0 channel 4 analog input. |
| | | | | ACMP1_P1 | A | MFP1 | Analog comparator 1 positive input 1 pin. |
| | | | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | | | SPI1_MOSI | I/O | MFP5 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | | I2C0_SDA | I/O | MFP6 | I2C0 data input/output pin. |
| | | | | UART5_RXD | I | MFP7 | UART5 data receiver input pin. |
| | | | | USCI1_CTL1 | I/O | MFP8 | USCI1 control 1 pin. |
| | | | | SC0_DAT | I/O | MFP9 | Smart Card 0 data pin. |
| | | | | I2S0_MCLK | O | MFP10 | I2S0 master clock output pin. |
| | | | | EPWM0_CH1 | I/O | MFP11 | EPWM0 channel 1 output/capture input. |
| | | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| 3 | 3 | 4 | 3 | PB.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH3 | A | MFP1 | EADC0 channel 3 analog input. |
| | | | | ACMP0_N | A | MFP1 | Analog comparator 0 negative input pin. |
| | | | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | | | | SPI1_CLK | I/O | MFP5 | SPI1 serial clock pin. |
| | | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | | UART5_nRTS | O | MFP7 | UART5 request to Send output pin. |
| | | | | USCI1_DAT1 | I/O | MFP8 | USCI1 data 1 pin. |
| | | | | SC0_RST | O | MFP9 | Smart Card 0 reset pin. |
| | | | | I2S0_DI | I | MFP10 | I2S0 data input pin. |
| | | | | EPWM0_CH2 | I/O | MFP11 | EPWM0 channel 2 output/capture input. |
| | | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| 4 | 4 | 5 | 4 | PB.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH2 | A | MFP1 | EADC0 channel 2 analog input. |
| | | | | ACMP0_P1 | A | MFP1 | Analog comparator 0 positive input 1 pin. |
| | | | | OPA0_O | A | MFP1 | Operational amplifier 0 output pin. |
| | | | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | | | SPI1_SS | I/O | MFP5 | SPI1 slave select pin. |
| | | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | | UART5_nCTS | I | MFP7 | UART5 clear to Send input pin. |
| | | | | USCI1_DAT0 | I/O | MFP8 | USCI1 data 0 pin. |
| | | | | SC0_PWR | O | MFP9 | Smart Card 0 power pin. |
| | | | | I2S0_DO | O | MFP10 | I2S0 data output pin. |
| | | | | EPWM0_CH3 | I/O | MFP11 | EPWM0 channel 3 output/capture input. |
| | | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| | | | 5 | PC.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR4 | O | MFP2 | EBI address bus bit 4. |
| | | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | | SPI3_MISO | I/O | MFP6 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | | SC0_nCD | I | MFP9 | Smart Card 0 card detect pin. |
| | | | | ECAP1_IC2 | I | MFP11 | Enhanced capture unit 1 input 2 pin. |
| | | | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| | | | 6 | PC.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR5 | O | MFP2 | EBI address bus bit 5. |
| | | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | | SPI3_MOSI | I/O | MFP6 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | | ECAP1_IC1 | I | MFP11 | Enhanced capture unit 1 input 1 pin. |
| | | | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| | | | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | | | 7 | PC.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR6 | O | MFP2 | EBI address bus bit 6. |
| | | | | SPI3_CLK | I/O | MFP6 | SPI3 serial clock pin. |
| | | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | | | | ECAP1_IC0 | I | MFP11 | Enhanced capture unit 1 input 0 pin. |
| | | | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| | | | 8 | PC.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR7 | O | MFP2 | EBI address bus bit 7. |
| | | | | SPI3_SS | I/O | MFP6 | SPI3 slave select pin. |
| | | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | | | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 5 | 5 | 6 | 9 | PB.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH1 | A | MFP1 | EADC0 channel 1 analog input. |
| | | | | OPA0_N | A | MFP1 | Operational amplifier 0 negative input pin. |
| | | | | EBI_ADR8 | O | MFP2 | EBI address bus bit 8. |
| | | | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | | | SPI3_I2SMCLK | I/O | MFP6 | SPI3 I2S master clock output pin |
| | | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | | USCI1_CLK | I/O | MFP8 | USCI1 clock pin. |
| | | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | | I2S0_LRCK | O | MFP10 | I2S0 left right channel clock output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| | | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | | EPWM0_BRAKE0 | I | MFP13 | EPWM0 Brake 0 input pin. |
| 6 | 6 | 7 | 10 | PB.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH0 | A | MFP1 | EADC0 channel 0 analog input. |
| | | | | OPA0_P | A | MFP1 | Operational amplifier 0 positive input pin. |
| | | | | EBI_ADR9 | O | MFP2 | EBI address bus bit 9. |
| | | | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | | SPI0_I2SMCLK | I/O | MFP8 | SPI0 I2S master clock output pin |
| | | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | | EPWM0_BRAKE1 | I | MFP13 | EPWM0 Brake 1 input pin. |
| | | | 11 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | | 12 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 7 | 8 | 13 | PA.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | ACMP0_P0 | A | MFP1 | Analog comparator 0 positive input 0 pin. |
| | | | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | | | SC2_PWR | O | MFP3 | Smart Card 2 power pin. |
| | | | | SPI2_SS | I/O | MFP4 | SPI2 slave select pin. |
| | | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | | USCI0_CLK | I/O | MFP6 | USCI0 clock pin. |
| | | | | I2C2_SCL | I/O | MFP7 | I2C2 clock pin. |
| | | | | BPWM0_CH0 | I/O | MFP9 | BPWM0 channel 0 output/capture input. |
| | | | | EPWM0_SYNC_OUT | O | MFP10 | EPWM0 counter synchronous trigger output pin. |
| | | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | | | DAC1_ST | I | MFP14 | DAC1 external trigger input. |
| | 8 | 9 | 14 | PA.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | ACMP1_P0 | A | MFP1 | Analog comparator 1 positive input 0 pin. |
| | | | | OPA1_O | A | MFP1 | Operational amplifier 1 output pin. |
| | | | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | | | SC2_RST | O | MFP3 | Smart Card 2 reset pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| | | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | | | USCI0_DAT0 | I/O | MFP6 | USCI0 data 0 pin. |
| | | | | I2C2_SDA | I/O | MFP7 | I2C2 data input/output pin. |
| | | | | BPWM0_CH1 | I/O | MFP9 | BPWM0 channel 1 output/capture input. |
| | | | | QEI1_INDEX | I | MFP10 | Quadrature encoder 1 index input |
| | | | | ECAP0_IC0 | I | MFP11 | Enhanced capture unit 0 input 0 pin. |
| | | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | | DAC0_ST | I | MFP14 | DAC0 external trigger input. |
| | 9 | 10 | 15 | PA.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA1_N | A | MFP1 | Operational amplifier 1 negative input pin. |
| | | | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | | | SC2_DAT | I/O | MFP3 | Smart Card 2 data pin. |
| | | | | SPI2_MISO | I/O | MFP4 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | | | USCI0_DAT1 | I/O | MFP6 | USCI0 data 1 pin. |
| | | | | UART1_TXD | O | MFP7 | UART1 data transmitter output pin. |
| | | | | BPWM0_CH2 | I/O | MFP9 | BPWM0 channel 2 output/capture input. |
| | | | | QEI1_A | I | MFP10 | Quadrature encoder 1 phase A input |
| | | | | ECAP0_IC1 | I | MFP11 | Enhanced capture unit 0 input 1 pin. |
| | | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| | 10 | 11 | 16 | PA.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA1_P | A | MFP1 | Operational amplifier 1 positive input pin. |
| | | | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | | | SC2_CLK | O | MFP3 | Smart Card 2 clock pin. |
| | | | | SPI2_MOSI | I/O | MFP4 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | | | USCI0_CTL1 | I/O | MFP6 | USCI0 control 1 pin. |
| | | | | UART1_RXD | I | MFP7 | UART1 data receiver input pin. |
| | | | | BPWM0_CH3 | I/O | MFP9 | BPWM0 channel 3 output/capture input. |
| | | | | QEI1_B | I | MFP10 | Quadrature encoder 1 phase B input |
| | | | | ECAP0_IC2 | I | MFP11 | Enhanced capture unit 0 input 2 pin. |
| | | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | INT4 | I | MFP15 | External interrupt 4 input pin. |
| | | | 17 | PC.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | | | SC2_nCD | I | MFP3 | Smart Card 2 card detect pin. |
| | | | | SPI2_I2SMCLK | I/O | MFP4 | SPI2 I2S master clock output pin |
| | | | | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | | | | USCI0_CTL0 | I/O | MFP6 | USCI0 control 0 pin. |
| | | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | | BPWM0_CH4 | I/O | MFP9 | BPWM0 channel 4 output/capture input. |
| | | | | CLKO | O | MFP13 | Clock Out |
| | | | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | | | 18 | PD.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA2_O | A | MFP1 | Operational amplifier 2 output pin. |
| | | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | | BPWM0_CH5 | I/O | MFP9 | BPWM0 channel 5 output/capture input. |
| | | | | QEI0_INDEX | I | MFP10 | Quadrature encoder 0 index input |
| | | | | CLKO | O | MFP13 | Clock Out |
| | | | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | | | | INT5 | I | MFP15 | External interrupt 5 input pin. |
| | | | 19 | PD.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA2_N | A | MFP1 | Operational amplifier 2 negative input pin. |
| | | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | | UART1_TXD | O | MFP3 | UART1 data transmitter output pin. |
| | | | | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | | | | QEI0_A | I | MFP10 | Quadrature encoder 0 phase A input |
| | | | | INT6 | I | MFP15 | External interrupt 6 input pin. |
| | | | 20 | PD.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA2_P | A | MFP1 | Operational amplifier 2 positive input pin. |
| | | | | EBI_nCS2 | O | MFP2 | EBI chip select 2 output pin. |
| | | | | UART1_RXD | I | MFP3 | UART1 data receiver input pin. |
| | | | | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | QEI0_B | I | MFP10 | Quadrature encoder 0 phase B input |
| | | | | INT7 | I | MFP15 | External interrupt 7 input pin. |
| | | | 21 | PG.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | | | SPI2_SS | I/O | MFP3 | SPI2 slave select pin. |
| | | | | I2C0_SMBAL | O | MFP4 | I2C0 SMBus SMBALTER pin |
| | | | | I2C1_SCL | I/O | MFP5 | I2C1 clock pin. |
| | | | | TM0 | I/O | MFP13 | Timer0 event counter input/toggle output pin. |
| | | | 22 | PG.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | | | SPI2_CLK | I/O | MFP3 | SPI2 serial clock pin. |
| | | | | I2C0_SMBSUS | O | MFP4 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | I2C1_SDA | I/O | MFP5 | I2C1 data input/output pin. |
| | | | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | | | 23 | PG.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | | | | SPI2_MISO | I/O | MFP3 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | | TM2 | I/O | MFP13 | Timer2 event counter input/toggle output pin. |
| | | | 24 | PF.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | | | | SPI2_MOSI | I/O | MFP3 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | | TAMPER5 | I/O | MFP10 | TAMPER detector loop pin 5. |
| | | | | TM3 | I/O | MFP13 | Timer3 event counter input/toggle output pin. |
| | | | 25 | PF.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | | | SC0_nCD | I | MFP3 | Smart Card 0 card detect pin. |
| | | | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |
| | | | | SPI0_I2SMCLK | I/O | MFP5 | SPI0 I2S master clock output pin |
| | | | | TAMPER4 | I/O | MFP10 | TAMPER detector loop pin 4. |
| | | | 26 | PF.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | | SC0_PWR | O | MFP3 | Smart Card 0 power pin. |
| | | | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI0_SS | I/O | MFP5 | SPI0 slave select pin. |
| | | | | TAMPER3 | I/O | MFP10 | TAMPER detector loop pin 3. |
| | | | 27 | PF.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | | | SC0_RST | O | MFP3 | Smart Card 0 reset pin. |
| | | | | I2S0_DI | I | MFP4 | I2S0 data input pin. |
| | | | | SPI0_CLK | I/O | MFP5 | SPI0 serial clock pin. |
| | | | | TAMPER2 | I/O | MFP10 | TAMPER detector loop pin 2. |
| | | | 28 | PF.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | | | SC0_DAT | I/O | MFP3 | Smart Card 0 data pin. |
| | | | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | | | SPI0_MISO | I/O | MFP5 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | | | TAMPER1 | I/O | MFP10 | TAMPER detector loop pin 1. |
| | | 12 | 29 | PF.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | | | SC0_CLK | O | MFP3 | Smart Card 0 clock pin. |
| | | | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | | | SPI0_MOSI | I/O | MFP5 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | | EBI_nCS0 | O | MFP7 | EBI chip select 0 output pin. |
| | | | | TAMPER0 | I/O | MFP10 | TAMPER detector loop pin 0. |
| | | 13 | 30 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 7 | 11 | 14 | 31 | PF.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | UART2_RXD | I | MFP2 | UART2 data receiver input pin. |
| | | | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | | | | BPWM0_CH4 | I/O | MFP8 | BPWM0 channel 4 output/capture input. |
| | | | | EPWM0_SYNC_OUT | O | MFP9 | EPWM0 counter synchronous trigger output pin. |
| | | | | X32_IN | I | MFP10 | External 32.768 kHz crystal input pin. |
| | | | | EADC0_ST | I | MFP11 | EADC0 external trigger input. |
| 8 | 12 | 15 | 32 | PF.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | UART2_TXD | O | MFP2 | UART2 data transmitter output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| | | | | BPWM0_CH5 | I/O | MFP8 | BPWM0 channel 5 output/capture input. |
| | | | | X32_OUT | O | MFP10 | External 32.768 kHz crystal output pin. |
| | | | 33 | PH.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | | | SPI1_MISO | I/O | MFP3 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | 34 | PH.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | | | SPI1_MOSI | I/O | MFP3 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | 35 | PH.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | | | SPI1_CLK | I/O | MFP3 | SPI1 serial clock pin. |
| | | | 36 | PH.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | | | SPI1_SS | I/O | MFP3 | SPI1 slave select pin. |
| 9 | 13 | 16 | 37 | PF.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | | XT1_IN | I | MFP10 | External 4~24 MHz (high speed) crystal input pin. |
| | | | | BPWM1_CH0 | I/O | MFP11 | BPWM1 channel 0 output/capture input. |
| 10 | 14 | 17 | 38 | PF.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | | QSPI0_CLK | I/O | MFP5 | Quad SPI0 serial clock pin. |
| | | | | XT1_OUT | O | MFP10 | External 4~24 MHz (high speed) crystal output pin. |
| | | | | BPWM1_CH1 | I/O | MFP11 | BPWM1 channel 1 output/capture input. |
| | | | 39 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | | 40 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | | 41 | PE.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | | | USCI1_CTL1 | I/O | MFP6 | USCI1 control 1 pin. |
| | | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | | EPWM0_CH0 | I/O | MFP10 | EPWM0 channel 0 output/capture input. |
| | | | | EPWM0_BRAKE0 | I | MFP11 | EPWM0 Brake 0 input pin. |
| | | | | ECAP0_IC0 | I | MFP12 | Enhanced capture unit 0 input 0 pin. |
| | | | | TRACE_CLK | O | MFP14 | ETM Trace Clock output pin |
| | | | 42 | PE.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |
| | | | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |
| | | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | | EPWM0_CH1 | I/O | MFP10 | EPWM0 channel 1 output/capture input. |
| | | | | EPWM0_BRAKE1 | I | MFP11 | EPWM0 Brake 1 input pin. |
| | | | | ECAP0_IC1 | I | MFP12 | Enhanced capture unit 0 input 1 pin. |
| | | | | TRACE_DATA0 | O | MFP14 | ETM Trace Data 0 output pin |
| | | | 43 | PE.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | | | I2S0_DI | I | MFP4 | I2S0 data input pin. |
| | | | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | | USCI1_DAT0 | I/O | MFP6 | USCI1 data 0 pin. |
| | | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | | EPWM0_CH2 | I/O | MFP10 | EPWM0 channel 2 output/capture input. |
| | | | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | | | ECAP0_IC2 | I | MFP12 | Enhanced capture unit 0 input 2 pin. |
| | | | | TRACE_DATA1 | O | MFP14 | ETM Trace Data 1 output pin |
| | | | 44 | PE.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | | | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | | | USCI1_DAT1 | I/O | MFP6 | USCI1 data 1 pin. |
| | | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | | | EPWM0_CH3 | I/O | MFP10 | EPWM0 channel 3 output/capture input. |
| | | | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | | | ECAP1_IC2 | I | MFP13 | Enhanced capture unit 1 input 2 pin. |
| | | | | TRACE_DATA2 | O | MFP14 | ETM Trace Data 2 output pin |
| | | | 45 | PE.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | | | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | | | SPI2_I2SMCLK | I/O | MFP5 | SPI2 I2S master clock output pin |
| | | | | USCI1_CLK | I/O | MFP6 | USCI1 clock pin. |
| | | | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | | | EPWM0_CH4 | I/O | MFP10 | EPWM0 channel 4 output/capture input. |
| | | | | ECAP1_IC1 | I | MFP13 | Enhanced capture unit 1 input 1 pin. |
| | | | | TRACE_DATA3 | O | MFP14 | ETM Trace Data 3 output pin |
| | | | 46 | PE.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | | UART4_nRTS | O | MFP5 | UART4 request to Send output pin. |
| | | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | | | EPWM0_CH5 | I/O | MFP10 | EPWM0 channel 5 output/capture input. |
| | | | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | | | BPWM1_CH5 | I/O | MFP12 | BPWM1 channel 5 output/capture input. |
| | | | | ECAP1_IC0 | I | MFP13 | Enhanced capture unit 1 input 0 pin. |
| | | | 47 | PC.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | | UART4_nCTS | I | MFP5 | UART4 clear to Send input pin. |
| | | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | | | BPWM1_CH4 | I/O | MFP12 | BPWM1 channel 4 output/capture input. |
| | | 18 | 48 | PC.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | | | SPI1_MISO | I/O | MFP4 | SPI1 MISO (Master In, Slave Out) pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | UART4_TXD | O | MFP5 | UART4 data transmitter output pin. |
| | | | | SC2_PWR | O | MFP6 | Smart Card 2 power pin. |
| | | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| | | 19 | 49 | PC.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | | | SPI1_MOSI | I/O | MFP4 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | | UART4_RXD | I | MFP5 | UART4 data receiver input pin. |
| | | | | SC2_RST | O | MFP6 | Smart Card 2 reset pin. |
| | | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| | 15 | 20 | 50 | PA.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | | | SPI1_CLK | I/O | MFP4 | SPI1 serial clock pin. |
| | | | | SC2_DAT | I/O | MFP6 | Smart Card 2 data pin. |
| | | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | | | EPWM1_CH4 | I/O | MFP11 | EPWM1 channel 4 output/capture input. |
| | | | | BPWM1_CH2 | I/O | MFP12 | BPWM1 channel 2 output/capture input. |
| | | | | ACMP0_WLAT | I | MFP13 | Analog comparator 0 window latch input pin |
| | | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| | 16 | 21 | 51 | PA.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | | | SPI1_SS | I/O | MFP4 | SPI1 slave select pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | | | | SC2_CLK | O | MFP6 | Smart Card 2 clock pin. |
| | | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | | | EPWM1_CH5 | I/O | MFP11 | EPWM1 channel 5 output/capture input. |
| | | | | BPWM1_CH3 | I/O | MFP12 | BPWM1 channel 3 output/capture input. |
| | | | | ACMP1_WLAT | I | MFP13 | Analog comparator 1 window latch input pin |
| | | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| | | 22 | 52 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | 23 | 53 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | 24 | 54 | LDO_CAP | A | MFP0 | LDO output pin. |
| | 17 | 25 | 55 | PA.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_D2 | I/O | MFP2 | SPIM data 2 pin for Quad Mode I/O. |
| | | | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | | SPI1_I2SMCLK | I/O | MFP4 | SPI1 I2S master clock output pin |
| | | | | SD1_CMD | I/O | MFP5 | SD/SDIO1 command/response pin |
| | | | | SC2_nCD | I | MFP6 | Smart Card 2 card detect pin. |
| | | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | | | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | | | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | | | | EPWM0_CH0 | I/O | MFP13 | EPWM0 channel 0 output/capture input. |
| | | | | QEI0_INDEX | I | MFP14 | Quadrature encoder 0 index input |
| | 18 | 26 | 56 | PA.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_D3 | I/O | MFP2 | SPIM data 3 pin for Quad Mode I/O. |
| | | | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | | SD1_CLK | O | MFP5 | SD/SDIO1 clock output pin |
| | | | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | | | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | | | | EPWM0_CH1 | I/O | MFP13 | EPWM0 channel 1 output/capture input. |
| | | | | QEI0_A | I | MFP14 | Quadrature encoder 0 phase A input |
| 11 | 19 | 27 | 57 | PA.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_SS | I/O | MFP2 | SPIM slave select pin. |
| | | | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | | | | EPWM0_CH2 | I/O | MFP13 | EPWM0 channel 2 output/capture input. |
| | | | | QEI0_B | I | MFP14 | Quadrature encoder 0 phase B input |
| 12 | 20 | 28 | 58 | PA.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_CLK | I/O | MFP2 | SPIM serial clock pin. |
| | | | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | | | | EPWM0_CH3 | I/O | MFP13 | EPWM0 channel 3 output/capture input. |
| 13 | 21 | 29 | 59 | PA.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_MISO | I/O | MFP2 | SPIM MISO (Master In, Slave Out) pin. |
| | | | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | | | | EPWM0_CH4 | I/O | MFP13 | EPWM0 channel 4 output/capture input. |
| | | | | DAC1_ST | I | MFP15 | DAC1 external trigger input. |
| 14 | 22 | 30 | 60 | PA.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_MOSI | I/O | MFP2 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | | | | EPWM0_CH5 | I/O | MFP13 | EPWM0 channel 5 output/capture input. |
| | | | | DAC0_ST | I | MFP15 | DAC0 external trigger input. |
| 15 | 23 | 31 | 61 | $V_{DDIO}$ | P | MFP0 | Power supply for PA.0~PA.5. |
| | | | 62 | PE.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | | | UART2_TXD | O | MFP3 | UART2 data transmitter output pin. |
| | | | | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | | | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | | | 63 | PE.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | | | UART2_RXD | I | MFP3 | UART2 data receiver input pin. |
| | | | | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |
| 16 | 24 | 32 | 64 | nRESET | I | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 17 | 25 | 33 | 65 | PF.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | UART1_TXD | O | MFP2 | UART1 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP3 | I2C1 clock pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | | ICE_DAT | O | MFP14 | Serial wired debugger data pin. |
| 18 | 26 | 34 | 66 | PF.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | UART1_RXD | I | MFP2 | UART1 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP3 | I2C1 data input/output pin. |
| | | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | | ICE_CLK | I | MFP14 | Serial wired debugger clock pin. |
| | | | 67 | PD.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | | | I2C2_SCL | I/O | MFP3 | I2C2 clock pin. |
| | | | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | | | 68 | PD.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | | | I2C2_SDA | I/O | MFP3 | I2C2 data input/output pin. |
| | | | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| | 27 | 35 | 69 | PC.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | | | | SPIM_D2 | I/O | MFP3 | SPIM data 2 pin for Quad Mode I/O. |
| | | | | QSPI0_MISO1 | I/O | MFP4 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | | | | UART4_TXD | O | MFP11 | UART4 data transmitter output pin. |
| | | | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| | 28 | 36 | 70 | PC.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | | | SPIM_D3 | I/O | MFP3 | SPIM data 3 pin for Quad Mode I/O. |
| | | | | QSPI0_MOSI1 | I/O | MFP4 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | | SC1_nCD | I | MFP5 | Smart Card 1 card detect pin. |
| | | | | I2S0_BCLK | O | MFP6 | I2S0 bit clock output pin. |
| | | | | SPI1_I2SMCLK | I/O | MFP7 | SPI1 I2S master clock output pin |
| | | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | | | | UART4_RXD | I | MFP11 | UART4 data receiver input pin. |
| | | | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| | 29 | 37 | 71 | PC.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | | | SPIM_SS | I/O | MFP3 | SPIM slave select pin. |
| | | | | QSPI0_SS | I/O | MFP4 | Quad SPI0 slave select pin. |
| | | | | SC1_PWR | O | MFP5 | Smart Card 1 power pin. |
| | | | | I2S0_MCLK | O | MFP6 | I2S0 master clock output pin. |
| | | | | SPI1_MISO | I/O | MFP7 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | | UART2_nRTS | O | MFP8 | UART2 request to Send output pin. |
| | | | | I2C0_SMBAL | O | MFP9 | I2C0 SMBus SMBALTER pin |
| | | | | CAN1_TXD | O | MFP10 | CAN1 bus transmitter output. |
| | | | | UART3_TXD | O | MFP11 | UART3 data transmitter output pin. |
| | | | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| | 30 | 38 | 72 | PC.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | | | SPIM_CLK | I/O | MFP3 | SPIM serial clock pin. |
| | | | | QSPI0_CLK | I/O | MFP4 | Quad SPI0 serial clock pin. |
| | | | | SC1_RST | O | MFP5 | Smart Card 1 reset pin. |
| | | | | I2S0_DI | I | MFP6 | I2S0 data input pin. |
| | | | | SPI1_MOSI | I/O | MFP7 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | | UART2_nCTS | I | MFP8 | UART2 clear to Send input pin. |
| | | | | I2C0_SMBSUS | O | MFP9 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | CAN1_RXD | I | MFP10 | CAN1 bus receiver input. |
| | | | | UART3_RXD | I | MFP11 | UART3 data receiver input pin. |
| | | | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 19 | 31 | 39 | 73 | PC.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | | | SPIM_MISO | I/O | MFP3 | SPIM MISO (Master In, Slave Out) pin. |
| | | | | QSPI0_MISO0 | I/O | MFP4 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | | SC1_DAT | I/O | MFP5 | Smart Card 1 data pin. |
| | | | | I2S0_DO | O | MFP6 | I2S0 data output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI1_CLK | I/O | MFP7 | SPI1 serial clock pin. |
| | | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| 20 | 32 | 40 | 74 | PC.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | | | SPIM_MOSI | I/O | MFP3 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | | QSPI0_MOSI0 | I/O | MFP4 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | | SC1_CLK | O | MFP5 | Smart Card 1 clock pin. |
| | | | | I2S0_LRCK | O | MFP6 | I2S0 left right channel clock output pin. |
| | | | | SPI1_SS | I/O | MFP7 | SPI1 slave select pin. |
| | | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | | | 75 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | | 76 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | | 77 | PG.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | | | SD1_DAT3 | I/O | MFP3 | SD/SDIO1 data line bit 3. |
| | | | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | | | 78 | PG.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | | | SD1_DAT2 | I/O | MFP3 | SD/SDIO1 data line bit 2. |
| | | | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | | | 79 | PG.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | | | SD1_DAT1 | I/O | MFP3 | SD/SDIO1 data line bit 1. |
| | | | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | | | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | 80 | PG.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | | | SD1_DAT0 | I/O | MFP3 | SD/SDIO1 data line bit 0. |
| | | | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | | | 81 | PG.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | | | SD1_CMD | I/O | MFP3 | SD/SDIO1 command/response pin |
| | | | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | | | 82 | PG.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | | | | SD1_CLK | O | MFP3 | SD/SDIO1 clock output pin |
| | | | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | | | 83 | PG.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SD1_nCD | I | MFP3 | SD/SDIO1 card detect input pin |
| | | | | CLKO | O | MFP14 | Clock Out |
| | | | | EADC0_ST | I | MFP15 | EADC0 external trigger input. |
| | | 41 | | PD.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | | USCI0_CTL1 | I/O | MFP3 | USCI0 control 1 pin. |
| | | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | | UART3_nRTS | O | MFP5 | UART3 request to Send output pin. |
| | | | | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |
| | | | | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | | | | SC1_nCD | I | MFP8 | Smart Card 1 card detect pin. |
| | | | | UART0_TXD | O | MFP9 | UART0 data transmitter output pin. |
| | | 42 | | PD.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | | USCI0_DAT1 | I/O | MFP3 | USCI0 data 1 pin. |
| | | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | | UART3_nCTS | I | MFP5 | UART3 clear to Send input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | | | | UART0_RXD | I | MFP9 | UART0 data receiver input pin. |
| | | 43 | | PD.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | | USCI0_DAT0 | I/O | MFP3 | USCI0 data 0 pin. |
| | | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | | UART3_TXD | O | MFP5 | UART3 data transmitter output pin. |
| | | | | I2C2_SCL | I/O | MFP6 | I2C2 clock pin. |
| | | | | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | | 44 | | PD.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | | USCI0_CLK | I/O | MFP3 | USCI0 clock pin. |
| | | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | | UART3_RXD | I | MFP5 | UART3 data receiver input pin. |
| | | | | I2C2_SDA | I/O | MFP6 | I2C2 data input/output pin. |
| | | | | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | 84 | PD.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | | SD0_nCD | I | MFP3 | SD/SDIO0 card detect input pin |
| | | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | | | SC2_nCD | I | MFP7 | Smart Card 2 card detect pin. |
| 21 | 33 | 45 | 85 | PA.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | I2S0_BCLK | O | MFP2 | I2S0 bit clock output pin. |
| | | | | UART4_TXD | O | MFP3 | UART4 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP4 | I2C1 clock pin. |
| | | | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | | | CAN0_TXD | O | MFP6 | CAN0 bus transmitter output. |
| | | | | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | | | | BPWM1_CH2 | I/O | MFP11 | BPWM1 channel 2 output/capture input. |
| | | | | QEI1_INDEX | I | MFP12 | Quadrature encoder 1 index input |
| | | | | USB_VBUS | P | MFP14 | Power supply from USB host or HUB. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| 22 | 34 | 46 | 86 | PA.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | I2S0_MCLK | O | MFP2 | I2S0 master clock output pin. |
| | | | | UART4_RXD | I | MFP3 | UART4 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP4 | I2C1 data input/output pin. |
| | | | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | | | CAN0_RXD | I | MFP6 | CAN0 bus receiver input. |
| | | | | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | | | | BPWM1_CH3 | I/O | MFP11 | BPWM1 channel 3 output/capture input. |
| | | | | QEI1_A | I | MFP12 | Quadrature encoder 1 phase A input |
| | | | | USB_D- | A | MFP14 | USB differential signal D-. |
| 23 | 35 | 47 | 87 | PA.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | I2S0_DI | I | MFP2 | I2S0 data input pin. |
| | | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | | I2C2_SCL | I/O | MFP6 | I2C2 clock pin. |
| | | | | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | | | | BPWM1_CH4 | I/O | MFP11 | BPWM1 channel 4 output/capture input. |
| | | | | QEI1_B | I | MFP12 | Quadrature encoder 1 phase B input |
| | | | | USB_D+ | A | MFP14 | USB differential signal D+. |
| 24 | 36 | 48 | 88 | PA.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | I2S0_DO | O | MFP2 | I2S0 data output pin. |
| | | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | | I2C2_SDA | I/O | MFP6 | I2C2 data input/output pin. |
| | | | | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | | | | BPWM1_CH5 | I/O | MFP11 | BPWM1 channel 5 output/capture input. |
| | | | | EPWM0_SYNC_IN | I | MFP12 | EPWM0 counter synchronous trigger input pin. |
| | | | | USB_OTG_ID | I | MFP14 | USB_ identification. |
| | | | 89 | NC | | | |
| | | | 90 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | | 91 | NC | | | |
| | | | 92 | NC | | | |
| | | | 93 | VSS | P | MFP0 | Ground pin for digital circuit. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | 94 | NC | | | |
| | | | 95 | LDO_CAP | A | MFP0 | LDO output pin.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| | | | 96 | NC | | | |
| | | | 97 | PE.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | | | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | | | | QEI1_INDEX | I | MFP11 | Quadrature encoder 1 index input |
| | | | | EPWM0_CH0 | I/O | MFP12 | EPWM0 channel 0 output/capture input. |
| | | | | BPWM0_CH5 | I/O | MFP13 | BPWM0 channel 5 output/capture input. |
| | | | 98 | PE.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | | | SPI3_I2SMCLK | I/O | MFP5 | SPI3 I2S master clock output pin |
| | | | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | | | USCI0_CTL0 | I/O | MFP7 | USCI0 control 0 pin. |
| | | | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | | | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | | | | QEI1_A | I | MFP11 | Quadrature encoder 1 phase A input |
| | | | | EPWM0_CH1 | I/O | MFP12 | EPWM0 channel 1 output/capture input. |
| | | | | BPWM0_CH4 | I/O | MFP13 | BPWM0 channel 4 output/capture input. |
| | | | 99 | PE.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | | | | SPI3_SS | I/O | MFP5 | SPI3 slave select pin. |
| | | | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | | | USCI0_CTL1 | I/O | MFP7 | USCI0 control 1 pin. |
| | | | | QEI1_B | I | MFP11 | Quadrature encoder 1 phase B input |
| | | | | EPWM0_CH2 | I/O | MFP12 | EPWM0 channel 2 output/capture input. |
| | | | | BPWM0_CH3 | I/O | MFP13 | BPWM0 channel 3 output/capture input. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | 100 | PE.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | | | SPI3_CLK | I/O | MFP5 | SPI3 serial clock pin. |
| | | | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | | | USCI0_DAT1 | I/O | MFP7 | USCI0 data 1 pin. |
| | | | | QEI0_INDEX | I | MFP11 | Quadrature encoder 0 index input |
| | | | | EPWM0_CH3 | I/O | MFP12 | EPWM0 channel 3 output/capture input. |
| | | | | BPWM0_CH2 | I/O | MFP13 | BPWM0 channel 2 output/capture input. |
| | | | 101 | PE.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | | | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | | | SPI3_MISO | I/O | MFP5 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | | | USCI0_DAT0 | I/O | MFP7 | USCI0 data 0 pin. |
| | | | | QEI0_A | I | MFP11 | Quadrature encoder 0 phase A input |
| | | | | EPWM0_CH4 | I/O | MFP12 | EPWM0 channel 4 output/capture input. |
| | | | | BPWM0_CH1 | I/O | MFP13 | BPWM0 channel 1 output/capture input. |
| | | | 102 | PE.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | | SPI3_MOSI | I/O | MFP5 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | | | USCI0_CLK | I/O | MFP7 | USCI0 clock pin. |
| | | | | QEI0_B | I | MFP11 | Quadrature encoder 0 phase B input |
| | | | | EPWM0_CH5 | I/O | MFP12 | EPWM0 channel 5 output/capture input. |
| | | | | BPWM0_CH0 | I/O | MFP13 | BPWM0 channel 0 output/capture input. |
| | | | 103 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | | 104 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | | 105 | PE.1 | I/O | MFP0 | General purpose digital I/O pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | | SC2_DAT | I/O | MFP4 | Smart Card 2 data pin. |
| | | | | I2S0_BCLK | O | MFP5 | I2S0 bit clock output pin. |
| | | | | SPI1_MISO | I/O | MFP6 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | | | UART4_nCTS | I | MFP9 | UART4 clear to Send input pin. |
| | | | 106 | PE.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | | SC2_CLK | O | MFP4 | Smart Card 2 clock pin. |
| | | | | I2S0_MCLK | O | MFP5 | I2S0 master clock output pin. |
| | | | | SPI1_MOSI | I/O | MFP6 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | | | UART4_nRTS | O | MFP9 | UART4 request to Send output pin. |
| | | | 107 | PH.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | | | SC2_PWR | O | MFP4 | Smart Card 2 power pin. |
| | | | | I2S0_DI | I | MFP5 | I2S0 data input pin. |
| | | | | SPI1_CLK | I/O | MFP6 | SPI1 serial clock pin. |
| | | | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | | | UART1_TXD | O | MFP10 | UART1 data transmitter output pin. |
| | | | 108 | PH.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | | | SC2_RST | O | MFP4 | Smart Card 2 reset pin. |
| | | | | I2S0_DO | O | MFP5 | I2S0 data output pin. |
| | | | | SPI1_SS | I/O | MFP6 | SPI1 slave select pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | | | UART1_RXD | I | MFP10 | UART1 data receiver input pin. |
| | | | 109 | PH.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | | SC2_nCD | I | MFP4 | Smart Card 2 card detect pin. |
| | | | | I2S0_LRCK | O | MFP5 | I2S0 left right channel clock output pin. |
| | | | | SPI1_I2SMCLK | I/O | MFP6 | SPI1 I2S master clock output pin |
| | | | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | | | UART0_TXD | O | MFP8 | UART0 data transmitter output pin. |
| | | | 110 | PH.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | | | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | | | UART0_RXD | I | MFP8 | UART0 data receiver input pin. |
| | | | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | | | 111 | PD.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | | SPI3_I2SMCLK | I/O | MFP3 | SPI3 I2S master clock output pin |
| | | | | SC1_nCD | I | MFP4 | Smart Card 1 card detect pin. |
| | | | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| 25 | 37 | 49 | 112 | VSS | P | MFP0 | Ground pin for digital circuit. |
| 26 | 38 | 50 | 113 | LDO_CAP | A | MFP0 | LDO output pin. |
| 27 | 39 | 51 | 114 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 40 | 52 | 115 | PC.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | | SC1_nCD | I | MFP3 | Smart Card 1 card detect pin. |
| | | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | | USCI0_CTL0 | I/O | MFP5 | USCI0 control 0 pin. |
| | | | | QSPI0_CLK | I/O | MFP6 | Quad SPI0 serial clock pin. |
| | | | | EPWM0_SYNC_IN | I | MFP11 | EPWM0 counter synchronous trigger input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | | | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| 28 | 41 | 53 | 116 | PB.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH15 | A | MFP1 | EADC0 channel 15 analog input. |
| | | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | | SC1_PWR | O | MFP3 | Smart Card 1 power pin. |
| | | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | | USCI0_CTL1 | I/O | MFP5 | USCI0 control 1 pin. |
| | | | | UART0_nCTS | I | MFP6 | UART0 clear to Send input pin. |
| | | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | | I2C2_SMBAL | O | MFP8 | I2C2 SMBus SMBALTER pin |
| | | | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| 29 | 42 | 54 | 117 | PB.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH14 | A | MFP1 | EADC0 channel 14 analog input. |
| | | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | | SC1_RST | O | MFP3 | Smart Card 1 reset pin. |
| | | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | | USCI0_DAT1 | I/O | MFP5 | USCI0 data 1 pin. |
| | | | | UART0_nRTS | O | MFP6 | UART0 request to Send output pin. |
| | | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | | I2C2_SMBSUS | O | MFP8 | I2C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | | CLKO | O | MFP14 | Clock Out |
| 30 | 43 | 55 | 118 | PB.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH13 | A | MFP1 | EADC0 channel 13 analog input. |
| | | | | DAC1_OUT | A | MFP1 | DAC1 channel analog output. |
| | | | | ACMP0_P3 | A | MFP1 | Analog comparator 0 positive input 3 pin. |
| | | | | ACMP1_P3 | A | MFP1 | Analog comparator 1 positive input 3 pin. |
| | | | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | | | SC1_DAT | I/O | MFP3 | Smart Card 1 data pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | | USCI0_DAT0 | I/O | MFP5 | USCI0 data 0 pin. |
| | | | | UART0_TXD | O | MFP6 | UART0 data transmitter output pin. |
| | | | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | | | I2C2_SCL | I/O | MFP8 | I2C2 clock pin. |
| | | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| 31 | 44 | 56 | 119 | PB.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH12 | A | MFP1 | EADC0 channel 12 analog input. |
| | | | | DAC0_OUT | A | MFP1 | DAC0 channel analog output. |
| | | | | ACMP0_P2 | A | MFP1 | Analog comparator 0 positive input 2 pin. |
| | | | | ACMP1_P2 | A | MFP1 | Analog comparator 1 positive input 2 pin. |
| | | | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | | | | SC1_CLK | O | MFP3 | Smart Card 1 clock pin. |
| | | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | | USCI0_CLK | I/O | MFP5 | USCI0 clock pin. |
| | | | | UART0_RXD | I | MFP6 | UART0 data receiver input pin. |
| | | | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | | | I2C2_SDA | I/O | MFP8 | I2C2 data input/output pin. |
| | | | | SD0_nCD | I | MFP9 | SD/SDIO0 card detect input pin |
| | | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| 32 | 45 | 57 | 120 | $AV_{DD}$ | P | MFP0 | Power supply for internal analog circuit. |
| | | 58 | 121 | $V_{REF}$ | A | MFP0 | ADC reference voltage input.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| | 46 | 59 | 122 | AVSS | P | MFP0 | Ground pin for analog circuit. |
| | | 60 | 123 | PB.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH11 | A | MFP1 | EADC0 channel 11 analog input. |
| | | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | | UART0_nCTS | I | MFP5 | UART0 clear to Send input pin. |
| | | | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP7 | I2C1 clock pin. |
| | | | | CAN0_TXD | O | MFP8 | CAN0 bus transmitter output. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI0_I2SMCLK | I/O | MFP9 | SPI0 I2S master clock output pin |
| | | | | BPWM1_CH0 | I/O | MFP10 | BPWM1 channel 0 output/capture input. |
| | | | | SPI3_CLK | I/O | MFP11 | SPI3 serial clock pin. |
| | | 61 | 124 | PB.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH10 | A | MFP1 | EADC0 channel 10 analog input. |
| | | | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | | | USCI1_CTL0 | I/O | MFP4 | USCI1 control 0 pin. |
| | | | | UART0_nRTS | O | MFP5 | UART0 request to Send output pin. |
| | | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP7 | I2C1 data input/output pin. |
| | | | | CAN0_RXD | I | MFP8 | CAN0 bus receiver input. |
| | | | | BPWM1_CH1 | I/O | MFP10 | BPWM1 channel 1 output/capture input. |
| | | | | SPI3_SS | I/O | MFP11 | SPI3 slave select pin. |
| | | 62 | 125 | PB.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH9 | A | MFP1 | EADC0 channel 9 analog input. |
| | | | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | | | USCI1_CTL1 | I/O | MFP4 | USCI1 control 1 pin. |
| | | | | UART0_TXD | O | MFP5 | UART0 data transmitter output pin. |
| | | | | UART1_nCTS | I | MFP6 | UART1 clear to Send input pin. |
| | | | | I2C1_SMBAL | O | MFP7 | I2C1 SMBus SMBALTER pin |
| | | | | BPWM1_CH2 | I/O | MFP10 | BPWM1 channel 2 output/capture input. |
| | | | | SPI3_MISO | I/O | MFP11 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | | INT7 | I | MFP13 | External interrupt 7 input pin. |
| | | 63 | 126 | PB.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH8 | A | MFP1 | EADC0 channel 8 analog input. |
| | | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | | | USCI1_CLK | I/O | MFP4 | USCI1 clock pin. |
| | | | | UART0_RXD | I | MFP5 | UART0 data receiver input pin. |
| | | | | UART1_nRTS | O | MFP6 | UART1 request to Send output pin. |
| | | | | I2C1_SMBSUS | O | MFP7 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | BPWM1_CH3 | I/O | MFP10 | BPWM1 channel 3 output/capture input. |
| | | | | SPI3_MOSI | I/O | MFP11 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | | INT6 | I | MFP13 | External interrupt 6 input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | 47 | 64 | 127 | PB.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH7 | A | MFP1 | EADC0 channel 7 analog input. |
| | | | | EBI_nWRL | O | MFP2 | EBI low byte write enable output pin. |
| | | | | USCI1_DAT0 | I/O | MFP4 | USCI1 data 0 pin. |
| | | | | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | | SD1_CMD | I/O | MFP7 | SD/SDIO1 command/response pin |
| | | | | EBI_nCS0 | O | MFP8 | EBI chip select 0 output pin. |
| | | | | BPWM1_CH4 | I/O | MFP10 | BPWM1 channel 4 output/capture input. |
| | | | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | | INT5 | I | MFP13 | External interrupt 5 input pin. |
| | | | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | | | | ACMP0_O | O | MFP15 | Analog comparator 0 output pin. |
| | 48 | 1 | 128 | PB.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH6 | A | MFP1 | EADC0 channel 6 analog input. |
| | | | | EBI_nWRH | O | MFP2 | EBI high byte write enable output pin |
| | | | | USCI1_DAT1 | I/O | MFP4 | USCI1 data 1 pin. |
| | | | | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | | SD1_CLK | O | MFP7 | SD/SDIO1 clock output pin |
| | | | | EBI_nCS1 | O | MFP8 | EBI chip select 1 output pin. |
| | | | | BPWM1_CH5 | I/O | MFP10 | BPWM1 channel 5 output/capture input. |
| | | | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | | INT4 | I | MFP13 | External interrupt 4 input pin. |
| | | | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | | | | ACMP1_O | O | MFP15 | Analog comparator 1 output pin. |

### 4.2.3 M483 Series Pin Description

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| 2 | 1 | PB.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH5 | A | MFP1 | EADC0 channel 5 analog input. |
| | | ACMP1_N | A | MFP1 | Analog comparator 1 negative input pin. |
| | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | SPI1_MISO | I/O | MFP5 | SPI1 MISO (Master In, Slave Out) pin. |
| | | I2C0_SCL | I/O | MFP6 | I2C0 clock pin. |
| | | UART5_TXD | O | MFP7 | UART5 data transmitter output pin. |
| | | USCI1_CTL0 | I/O | MFP8 | USCI1 control 0 pin. |
| | | SC0_CLK | O | MFP9 | Smart Card 0 clock pin. |
| | | I2S0_BCLK | O | MFP10 | I2S0 bit clock output pin. |
| | | EPWM0_CH0 | I/O | MFP11 | EPWM0 channel 0 output/capture input. |
| | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| 3 | 2 | PB.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH4 | A | MFP1 | EADC0 channel 4 analog input. |
| | | ACMP1_P1 | A | MFP1 | Analog comparator 1 positive input 1 pin. |
| | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | SPI1_MOSI | I/O | MFP5 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | I2C0_SDA | I/O | MFP6 | I2C0 data input/output pin. |
| | | UART5_RXD | I | MFP7 | UART5 data receiver input pin. |
| | | USCI1_CTL1 | I/O | MFP8 | USCI1 control 1 pin. |
| | | SC0_DAT | I/O | MFP9 | Smart Card 0 data pin. |
| | | I2S0_MCLK | O | MFP10 | I2S0 master clock output pin. |
| | | EPWM0_CH1 | I/O | MFP11 | EPWM0 channel 1 output/capture input. |
| | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| 4 | 3 | PB.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH3 | A | MFP1 | EADC0 channel 3 analog input. |
| | | ACMP0_N | A | MFP1 | Analog comparator 0 negative input pin. |
| | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | SPI1_CLK | I/O | MFP5 | SPI1 serial clock pin. |
| | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | UART5_nRTS | O | MFP7 | UART5 request to Send output pin. |
| | | USCI1_DAT1 | I/O | MFP8 | USCI1 data 1 pin. |
| | | SC0_RST | O | MFP9 | Smart Card 0 reset pin. |
| | | I2S0_DI | I | MFP10 | I2S0 data input pin. |
| | | EPWM0_CH2 | I/O | MFP11 | EPWM0 channel 2 output/capture input. |
| | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| 5 | 4 | PB.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH2 | A | MFP1 | EADC0 channel 2 analog input. |
| | | ACMP0_P1 | A | MFP1 | Analog comparator 0 positive input 1 pin. |
| | | OPA0_O | A | MFP1 | Operational amplifier 0 output pin. |
| | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | SPI1_SS | I/O | MFP5 | SPI1 slave select pin. |
| | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | UART5_nCTS | I | MFP7 | UART5 clear to Send input pin. |
| | | USCI1_DAT0 | I/O | MFP8 | USCI1 data 0 pin. |
| | | SC0_PWR | O | MFP9 | Smart Card 0 power pin. |
| | | I2S0_DO | O | MFP10 | I2S0 data output pin. |
| | | EPWM0_CH3 | I/O | MFP11 | EPWM0 channel 3 output/capture input. |
| | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| | 5 | PC.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR4 | O | MFP2 | EBI address bus bit 4. |
| | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | SPI3_MISO | I/O | MFP6 | SPI3 MISO (Master In, Slave Out) pin. |
| | | SC0_nCD | I | MFP9 | Smart Card 0 card detect pin. |
| | | ECAP1_IC2 | I | MFP11 | Enhanced capture unit 1 input 2 pin. |
| | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| | 6 | PC.11 | I/O | MFP0 | General purpose digital I/O pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | EBI_ADR5 | O | MFP2 | EBI address bus bit 5. |
| | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | SPI3_MOSI | I/O | MFP6 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | ECAP1_IC1 | I | MFP11 | Enhanced capture unit 1 input 1 pin. |
| | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | 7 | PC.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR6 | O | MFP2 | EBI address bus bit 6. |
| | | SPI3_CLK | I/O | MFP6 | SPI3 serial clock pin. |
| | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | | ECAP1_IC0 | I | MFP11 | Enhanced capture unit 1 input 0 pin. |
| | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| | 8 | PC.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR7 | O | MFP2 | EBI address bus bit 7. |
| | | SPI3_SS | I/O | MFP6 | SPI3 slave select pin. |
| | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 6 | 9 | PB.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH1 | A | MFP1 | EADC0 channel 1 analog input. |
| | | OPA0_N | A | MFP1 | Operational amplifier 0 negative input pin. |
| | | EBI_ADR8 | O | MFP2 | EBI address bus bit 8. |
| | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | SPI3_I2SMCLK | I/O | MFP6 | SPI3 I2S master clock output pin |
| | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | USCI1_CLK | I/O | MFP8 | USCI1 clock pin. |
| | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | I2S0_LRCK | O | MFP10 | I2S0 left right channel clock output pin. |
| | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | EPWM0_BRAKE0 | I | MFP13 | EPWM0 Brake 0 input pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| 7 | 10 | PB.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH0 | A | MFP1 | EADC0 channel 0 analog input. |
| | | OPA0_P | A | MFP1 | Operational amplifier 0 positive input pin. |
| | | EBI_ADR9 | O | MFP2 | EBI address bus bit 9. |
| | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | SPI0_I2SMCLK | I/O | MFP8 | SPI0 I2S master clock output pin |
| | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | EPWM0_BRAKE1 | I | MFP13 | EPWM0 Brake 1 input pin. |
| | 11 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | 12 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 8 | 13 | PA.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | ACMP0_P0 | A | MFP1 | Analog comparator 0 positive input 0 pin. |
| | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | SC2_PWR | O | MFP3 | Smart Card 2 power pin. |
| | | SPI2_SS | I/O | MFP4 | SPI2 slave select pin. |
| | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | USCI0_CLK | I/O | MFP6 | USCI0 clock pin. |
| | | I2C2_SCL | I/O | MFP7 | I2C2 clock pin. |
| | | BPWM0_CH0 | I/O | MFP9 | BPWM0 channel 0 output/capture input. |
| | | EPWM0_SYNC_OUT | O | MFP10 | EPWM0 counter synchronous trigger output pin. |
| | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | DAC1_ST | I | MFP14 | DAC1 external trigger input. |
| 9 | 14 | PA.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | ACMP1_P0 | A | MFP1 | Analog comparator 1 positive input 0 pin. |
| | | OPA1_O | A | MFP1 | Operational amplifier 1 output pin. |
| | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | SC2_RST | O | MFP3 | Smart Card 2 reset pin. |
| | | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | USCI0_DAT0 | I/O | MFP6 | USCI0 data 0 pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | I2C2_SDA | I/O | MFP7 | I2C2 data input/output pin. |
| | | BPWM0_CH1 | I/O | MFP9 | BPWM0 channel 1 output/capture input. |
| | | QEI1_INDEX | I | MFP10 | Quadrature encoder 1 index input |
| | | ECAP0_IC0 | I | MFP11 | Enhanced capture unit 0 input 0 pin. |
| | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | DAC0_ST | I | MFP14 | DAC0 external trigger input. |
| 10 | 15 | PA.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | OPA1_N | A | MFP1 | Operational amplifier 1 negative input pin. |
| | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | SC2_DAT | I/O | MFP3 | Smart Card 2 data pin. |
| | | SPI2_MISO | I/O | MFP4 | SPI2 MISO (Master In, Slave Out) pin. |
| | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | USCI0_DAT1 | I/O | MFP6 | USCI0 data 1 pin. |
| | | UART1_TXD | O | MFP7 | UART1 data transmitter output pin. |
| | | BPWM0_CH2 | I/O | MFP9 | BPWM0 channel 2 output/capture input. |
| | | QEI1_A | I | MFP10 | Quadrature encoder 1 phase A input |
| | | ECAP0_IC1 | I | MFP11 | Enhanced capture unit 0 input 1 pin. |
| | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| 11 | 16 | PA.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | OPA1_P | A | MFP1 | Operational amplifier 1 positive input pin. |
| | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | SC2_CLK | O | MFP3 | Smart Card 2 clock pin. |
| | | SPI2_MOSI | I/O | MFP4 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | USCI0_CTL1 | I/O | MFP6 | USCI0 control 1 pin. |
| | | UART1_RXD | I | MFP7 | UART1 data receiver input pin. |
| | | BPWM0_CH3 | I/O | MFP9 | BPWM0 channel 3 output/capture input. |
| | | QEI1_B | I | MFP10 | Quadrature encoder 1 phase B input |
| | | ECAP0_IC2 | I | MFP11 | Enhanced capture unit 0 input 2 pin. |
| | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| | | INT4 | I | MFP15 | External interrupt 4 input pin. |
| | 17 | PC.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | SC2_nCD | I | MFP3 | Smart Card 2 card detect pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | SPI2_I2SMCLK | I/O | MFP4 | SPI2 I2S master clock output pin |
| | | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | | USCI0_CTL0 | I/O | MFP6 | USCI0 control 0 pin. |
| | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | BPWM0_CH4 | I/O | MFP9 | BPWM0 channel 4 output/capture input. |
| | | CLKO | O | MFP13 | Clock Out |
| | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | 18 | PD.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | OPA2_O | A | MFP1 | Operational amplifier 2 output pin. |
| | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | BPWM0_CH5 | I/O | MFP9 | BPWM0 channel 5 output/capture input. |
| | | QEI0_INDEX | I | MFP10 | Quadrature encoder 0 index input |
| | | CLKO | O | MFP13 | Clock Out |
| | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | | INT5 | I | MFP15 | External interrupt 5 input pin. |
| | 19 | PD.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | OPA2_N | A | MFP1 | Operational amplifier 2 negative input pin. |
| | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | UART1_TXD | O | MFP3 | UART1 data transmitter output pin. |
| | | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | | QEI0_A | I | MFP10 | Quadrature encoder 0 phase A input |
| | | INT6 | I | MFP15 | External interrupt 6 input pin. |
| | 20 | PD.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | OPA2_P | A | MFP1 | Operational amplifier 2 positive input pin. |
| | | EBI_nCS2 | O | MFP2 | EBI chip select 2 output pin. |
| | | UART1_RXD | I | MFP3 | UART1 data receiver input pin. |
| | | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |
| | | QEI0_B | I | MFP10 | Quadrature encoder 0 phase B input |
| | | INT7 | I | MFP15 | External interrupt 7 input pin. |
| | 21 | PG.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | SPI2_SS | I/O | MFP3 | SPI2 slave select pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | I2C0_SMBAL | O | MFP4 | I2C0 SMBus SMBALTER pin |
| | | I2C1_SCL | I/O | MFP5 | I2C1 clock pin. |
| | | TM0 | I/O | MFP13 | Timer0 event counter input/toggle output pin. |
| | 22 | PG.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | SPI2_CLK | I/O | MFP3 | SPI2 serial clock pin. |
| | | I2C0_SMBSUS | O | MFP4 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | I2C1_SDA | I/O | MFP5 | I2C1 data input/output pin. |
| | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | 23 | PG.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | | SPI2_MISO | I/O | MFP3 | SPI2 MISO (Master In, Slave Out) pin. |
| | | TM2 | I/O | MFP13 | Timer2 event counter input/toggle output pin. |
| | 24 | PF.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | | SPI2_MOSI | I/O | MFP3 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | TAMPER5 | I/O | MFP10 | TAMPER detector loop pin 5. |
| | | TM3 | I/O | MFP13 | Timer3 event counter input/toggle output pin. |
| | 25 | PF.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | SC0_nCD | I | MFP3 | Smart Card 0 card detect pin. |
| | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |
| | | SPI0_I2SMCLK | I/O | MFP5 | SPI0 I2S master clock output pin |
| | | TAMPER4 | I/O | MFP10 | TAMPER detector loop pin 4. |
| | 26 | PF.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | SC0_PWR | O | MFP3 | Smart Card 0 power pin. |
| | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |
| | | SPI0_SS | I/O | MFP5 | SPI0 slave select pin. |
| | | TAMPER3 | I/O | MFP10 | TAMPER detector loop pin 3. |
| | 27 | PF.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | SC0_RST | O | MFP3 | Smart Card 0 reset pin. |
| | | I2S0_DI | I | MFP4 | I2S0 data input pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | SPI0_CLK | I/O | MFP5 | SPI0 serial clock pin. |
| | | TAMPER2 | I/O | MFP10 | TAMPER detector loop pin 2. |
| | 28 | PF.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | SC0_DAT | I/O | MFP3 | Smart Card 0 data pin. |
| | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | SPI0_MISO | I/O | MFP5 | SPI0 MISO (Master In, Slave Out) pin. |
| | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | TAMPER1 | I/O | MFP10 | TAMPER detector loop pin 1. |
| 12 | 29 | PF.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | SC0_CLK | O | MFP3 | Smart Card 0 clock pin. |
| | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | SPI0_MOSI | I/O | MFP5 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | EBI_nCS0 | O | MFP7 | EBI chip select 0 output pin. |
| | | TAMPER0 | I/O | MFP10 | TAMPER detector loop pin 0. |
| 13 | 30 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 14 | 31 | PF.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | UART2_RXD | I | MFP2 | UART2 data receiver input pin. |
| | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | | BPWM0_CH4 | I/O | MFP8 | BPWM0 channel 4 output/capture input. |
| | | EPWM0_SYNC_OUT | O | MFP9 | EPWM0 counter synchronous trigger output pin. |
| | | X32_IN | I | MFP10 | External 32.768 kHz crystal input pin. |
| | | EADC0_ST | I | MFP11 | EADC0 external trigger input. |
| 15 | 32 | PF.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | UART2_TXD | O | MFP2 | UART2 data transmitter output pin. |
| | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| | | BPWM0_CH5 | I/O | MFP8 | BPWM0 channel 5 output/capture input. |
| | | X32_OUT | O | MFP10 | External 32.768 kHz crystal output pin. |
| | 33 | PH.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | SPI1_MISO | I/O | MFP3 | SPI1 MISO (Master In, Slave Out) pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | 34 | PH.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | SPI1_MOSI | I/O | MFP3 | SPI1 MOSI (Master Out, Slave In) pin. |
| | 35 | PH.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | SPI1_CLK | I/O | MFP3 | SPI1 serial clock pin. |
| | 36 | PH.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | SPI1_SS | I/O | MFP3 | SPI1 slave select pin. |
| 16 | 37 | PF.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | XT1_IN | I | MFP10 | External 4~24 MHz (high speed) crystal input pin. |
| | | BPWM1_CH0 | I/O | MFP11 | BPWM1 channel 0 output/capture input. |
| 17 | 38 | PF.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | QSPI0_CLK | I/O | MFP5 | Quad SPI0 serial clock pin. |
| | | XT1_OUT | O | MFP10 | External 4~24 MHz (high speed) crystal output pin. |
| | | BPWM1_CH1 | I/O | MFP11 | BPWM1 channel 1 output/capture input. |
| | 39 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | 40 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 41 | PE.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |
| | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | USCI1_CTL1 | I/O | MFP6 | USCI1 control 1 pin. |
| | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | EPWM0_CH0 | I/O | MFP10 | EPWM0 channel 0 output/capture input. |
| | | EPWM0_BRAKE0 | I | MFP11 | EPWM0 Brake 0 input pin. |
| | | ECAP0_IC0 | I | MFP12 | Enhanced capture unit 0 input 0 pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | TRACE_CLK | O | MFP14 | ETM Trace Clock output pin |
| | 42 | PE.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |
| | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |
| | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | EPWM0_CH1 | I/O | MFP10 | EPWM0 channel 1 output/capture input. |
| | | EPWM0_BRAKE1 | I | MFP11 | EPWM0 Brake 1 input pin. |
| | | ECAP0_IC1 | I | MFP12 | Enhanced capture unit 0 input 1 pin. |
| | | TRACE_DATA0 | O | MFP14 | ETM Trace Data 0 output pin |
| | 43 | PE.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | I2S0_DI | I | MFP4 | I2S0 data input pin. |
| | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | USCI1_DAT0 | I/O | MFP6 | USCI1 data 0 pin. |
| | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | EPWM0_CH2 | I/O | MFP10 | EPWM0 channel 2 output/capture input. |
| | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | ECAP0_IC2 | I | MFP12 | Enhanced capture unit 0 input 2 pin. |
| | | TRACE_DATA1 | O | MFP14 | ETM Trace Data 1 output pin |
| | 44 | PE.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | USCI1_DAT1 | I/O | MFP6 | USCI1 data 1 pin. |
| | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | EPWM0_CH3 | I/O | MFP10 | EPWM0 channel 3 output/capture input. |
| | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | ECAP1_IC2 | I | MFP13 | Enhanced capture unit 1 input 2 pin. |
| | | TRACE_DATA2 | O | MFP14 | ETM Trace Data 2 output pin |
| | 45 | PE.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | SPI2_I2SMCLK | I/O | MFP5 | SPI2 I2S master clock output pin |
| | | USCI1_CLK | I/O | MFP6 | USCI1 clock pin. |
| | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | EPWM0_CH4 | I/O | MFP10 | EPWM0 channel 4 output/capture input. |
| | | ECAP1_IC1 | I | MFP13 | Enhanced capture unit 1 input 1 pin. |
| | | TRACE_DATA3 | O | MFP14 | ETM Trace Data 3 output pin |
| | 46 | PE.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | UART4_nRTS | O | MFP5 | UART4 request to Send output pin. |
| | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | EPWM0_CH5 | I/O | MFP10 | EPWM0 channel 5 output/capture input. |
| | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | BPWM1_CH5 | I/O | MFP12 | BPWM1 channel 5 output/capture input. |
| | | ECAP1_IC0 | I | MFP13 | Enhanced capture unit 1 input 0 pin. |
| | 47 | PC.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | UART4_nCTS | I | MFP5 | UART4 clear to Send input pin. |
| | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | BPWM1_CH4 | I/O | MFP12 | BPWM1 channel 4 output/capture input. |
| 18 | 48 | PC.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | SPI1_MISO | I/O | MFP4 | SPI1 MISO (Master In, Slave Out) pin. |
| | | UART4_TXD | O | MFP5 | UART4 data transmitter output pin. |
| | | SC2_PWR | O | MFP6 | Smart Card 2 power pin. |
| | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | INT3 | I | MFP15 | External interrupt 3 input pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| 19 | 49 | PC.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | SPI1_MOSI | I/O | MFP4 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | UART4_RXD | I | MFP5 | UART4 data receiver input pin. |
| | | SC2_RST | O | MFP6 | Smart Card 2 reset pin. |
| | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| 20 | 50 | PA.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | SPI1_CLK | I/O | MFP4 | SPI1 serial clock pin. |
| | | SC2_DAT | I/O | MFP6 | Smart Card 2 data pin. |
| | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | EPWM1_CH4 | I/O | MFP11 | EPWM1 channel 4 output/capture input. |
| | | BPWM1_CH2 | I/O | MFP12 | BPWM1 channel 2 output/capture input. |
| | | ACMP0_WLAT | I | MFP13 | Analog comparator 0 window latch input pin |
| | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| 21 | 51 | PA.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | SPI1_SS | I/O | MFP4 | SPI1 slave select pin. |
| | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | | SC2_CLK | O | MFP6 | Smart Card 2 clock pin. |
| | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | EPWM1_CH5 | I/O | MFP11 | EPWM1 channel 5 output/capture input. |
| | | BPWM1_CH3 | I/O | MFP12 | BPWM1 channel 3 output/capture input. |
| | | ACMP1_WLAT | I | MFP13 | Analog comparator 1 window latch input pin |
| | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | INT0 | I | MFP15 | External interrupt 0 input pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| 22 | 52 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| 23 | 53 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 24 | 54 | LDO_CAP | A | MFP0 | LDO output pin. |
| 25 | 55 | PA.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | SPIM_D2 | I/O | MFP2 | SPIM data 2 pin for Quad Mode I/O. |
| | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | SPI1_I2SMCLK | I/O | MFP4 | SPI1 I2S master clock output pin |
| | | SD1_CMD | I/O | MFP5 | SD/SDIO1 command/response pin |
| | | SC2_nCD | I | MFP6 | Smart Card 2 card detect pin. |
| | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | | EPWM0_CH0 | I/O | MFP13 | EPWM0 channel 0 output/capture input. |
| | | QEI0_INDEX | I | MFP14 | Quadrature encoder 0 index input |
| 26 | 56 | PA.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | SPIM_D3 | I/O | MFP2 | SPIM data 3 pin for Quad Mode I/O. |
| | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | SD1_CLK | O | MFP5 | SD/SDIO1 clock output pin |
| | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | | EPWM0_CH1 | I/O | MFP13 | EPWM0 channel 1 output/capture input. |
| | | QEI0_A | I | MFP14 | Quadrature encoder 0 phase A input |
| 27 | 57 | PA.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | SPIM_SS | I/O | MFP2 | SPIM slave select pin. |
| | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | | EPWM0_CH2 | I/O | MFP13 | EPWM0 channel 2 output/capture input. |
| | | QEI0_B | I | MFP14 | Quadrature encoder 0 phase B input |
| 28 | 58 | PA.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | SPIM_CLK | I/O | MFP2 | SPIM serial clock pin. |
| | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | | EPWM0_CH3 | I/O | MFP13 | EPWM0 channel 3 output/capture input. |
| 29 | 59 | PA.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | SPIM_MISO | I/O | MFP2 | SPIM MISO (Master In, Slave Out) pin. |
| | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | | EPWM0_CH4 | I/O | MFP13 | EPWM0 channel 4 output/capture input. |
| | | DAC1_ST | I | MFP15 | DAC1 external trigger input. |
| 30 | 60 | PA.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | SPIM_MOSI | I/O | MFP2 | SPIM MOSI (Master Out, Slave In) pin. |
| | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | | EPWM0_CH5 | I/O | MFP13 | EPWM0 channel 5 output/capture input. |
| | | DAC0_ST | I | MFP15 | DAC0 external trigger input. |
| 31 | 61 | $V_{DDIO}$ | P | MFP0 | Power supply for PA.0~PA.5. |
| | 62 | PE.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | UART2_TXD | O | MFP3 | UART2 data transmitter output pin. |
| | | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | 63 | PE.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | UART2_RXD | I | MFP3 | UART2 data receiver input pin. |
| | | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |
| 32 | 64 | nRESET | I | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 33 | 65 | PF.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | UART1_TXD | O | MFP2 | UART1 data transmitter output pin. |
| | | I2C1_SCL | I/O | MFP3 | I2C1 clock pin. |
| | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | ICE_DAT | O | MFP14 | Serial wired debugger data pin. |
| 34 | 66 | PF.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | UART1_RXD | I | MFP2 | UART1 data receiver input pin. |
| | | I2C1_SDA | I/O | MFP3 | I2C1 data input/output pin. |
| | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | ICE_CLK | I | MFP14 | Serial wired debugger clock pin. |
| | 67 | PD.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | I2C2_SCL | I/O | MFP3 | I2C2 clock pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | 68 | PD.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | I2C2_SDA | I/O | MFP3 | I2C2 data input/output pin. |
| | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| 35 | 69 | PC.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | | SPIM_D2 | I/O | MFP3 | SPIM data 2 pin for Quad Mode I/O. |
| | | QSPI0_MISO1 | I/O | MFP4 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | | UART4_TXD | O | MFP11 | UART4 data transmitter output pin. |
| | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| 36 | 70 | PC.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | SPIM_D3 | I/O | MFP3 | SPIM data 3 pin for Quad Mode I/O. |
| | | QSPI0_MOSI1 | I/O | MFP4 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | SC1_nCD | I | MFP5 | Smart Card 1 card detect pin. |
| | | I2S0_BCLK | O | MFP6 | I2S0 bit clock output pin. |
| | | SPI1_I2SMCLK | I/O | MFP7 | SPI1 I2S master clock output pin |
| | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | | UART4_RXD | I | MFP11 | UART4 data receiver input pin. |
| | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| 37 | 71 | PC.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | SPIM_SS | I/O | MFP3 | SPIM slave select pin. |
| | | QSPI0_SS | I/O | MFP4 | Quad SPI0 slave select pin. |
| | | SC1_PWR | O | MFP5 | Smart Card 1 power pin. |
| | | I2S0_MCLK | O | MFP6 | I2S0 master clock output pin. |
| | | SPI1_MISO | I/O | MFP7 | SPI1 MISO (Master In, Slave Out) pin. |
| | | UART2_nRTS | O | MFP8 | UART2 request to Send output pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | I2C0_SMBAL | O | MFP9 | I2C0 SMBus SMBALTER pin |
| | | CAN1_TXD | O | MFP10 | CAN1 bus transmitter output. |
| | | UART3_TXD | O | MFP11 | UART3 data transmitter output pin. |
| | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| 38 | 72 | PC.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | SPIM_CLK | I/O | MFP3 | SPIM serial clock pin. |
| | | QSPI0_CLK | I/O | MFP4 | Quad SPI0 serial clock pin. |
| | | SC1_RST | O | MFP5 | Smart Card 1 reset pin. |
| | | I2S0_DI | I | MFP6 | I2S0 data input pin. |
| | | SPI1_MOSI | I/O | MFP7 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | UART2_nCTS | I | MFP8 | UART2 clear to Send input pin. |
| | | I2C0_SMBSUS | O | MFP9 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | CAN1_RXD | I | MFP10 | CAN1 bus receiver input. |
| | | UART3_RXD | I | MFP11 | UART3 data receiver input pin. |
| | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 39 | 73 | PC.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | SPIM_MISO | I/O | MFP3 | SPIM MISO (Master In, Slave Out) pin. |
| | | QSPI0_MISO0 | I/O | MFP4 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | SC1_DAT | I/O | MFP5 | Smart Card 1 data pin. |
| | | I2S0_DO | O | MFP6 | I2S0 data output pin. |
| | | SPI1_CLK | I/O | MFP7 | SPI1 serial clock pin. |
| | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| 40 | 74 | PC.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | SPIM_MOSI | I/O | MFP3 | SPIM MOSI (Master Out, Slave In) pin. |
| | | QSPI0_MOSI0 | I/O | MFP4 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | SC1_CLK | O | MFP5 | Smart Card 1 clock pin. |
| | | I2S0_LRCK | O | MFP6 | I2S0 left right channel clock output pin. |
| | | SPI1_SS | I/O | MFP7 | SPI1 slave select pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | 75 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | 76 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 77 | PG.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | SD1_DAT3 | I/O | MFP3 | SD/SDIO1 data line bit 3. |
| | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | 78 | PG.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | SD1_DAT2 | I/O | MFP3 | SD/SDIO1 data line bit 2. |
| | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | 79 | PG.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | SD1_DAT1 | I/O | MFP3 | SD/SDIO1 data line bit 1. |
| | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | 80 | PG.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | SD1_DAT0 | I/O | MFP3 | SD/SDIO1 data line bit 0. |
| | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | 81 | PG.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | SD1_CMD | I/O | MFP3 | SD/SDIO1 command/response pin |
| | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | 82 | PG.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | SD1_CLK | O | MFP3 | SD/SDIO1 clock output pin |
| | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | 83 | PG.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | SD1_nCD | I | MFP3 | SD/SDIO1 card detect input pin |
| | | CLKO | O | MFP14 | Clock Out |
| | | EADC0_ST | I | MFP15 | EADC0 external trigger input. |
| | 84 | PD.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | SD0_nCD | I | MFP3 | SD/SDIO0 card detect input pin |
| | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | SC2_nCD | I | MFP7 | Smart Card 2 card detect pin. |
| | 85 | PA.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | I2S0_BCLK | O | MFP2 | I2S0 bit clock output pin. |
| | | UART4_TXD | O | MFP3 | UART4 data transmitter output pin. |
| | | I2C1_SCL | I/O | MFP4 | I2C1 clock pin. |
| | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | CAN0_TXD | O | MFP6 | CAN0 bus transmitter output. |
| | | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | | BPWM1_CH2 | I/O | MFP11 | BPWM1 channel 2 output/capture input. |
| | | QEI1_INDEX | I | MFP12 | Quadrature encoder 1 index input |
| | | USB_VBUS | P | MFP14 | Power supply from USB host or HUB. |
| | 86 | PA.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | I2S0_MCLK | O | MFP2 | I2S0 master clock output pin. |
| | | UART4_RXD | I | MFP3 | UART4 data receiver input pin. |
| | | I2C1_SDA | I/O | MFP4 | I2C1 data input/output pin. |
| | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | CAN0_RXD | I | MFP6 | CAN0 bus receiver input. |
| | | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | | BPWM1_CH3 | I/O | MFP11 | BPWM1 channel 3 output/capture input. |
| | | QEI1_A | I | MFP12 | Quadrature encoder 1 phase A input |
| | | USB_D- | A | MFP14 | USB differential signal D-. |
| | 87 | PA.14 | I/O | MFP0 | General purpose digital I/O pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | I2S0_DI | I | MFP2 | I2S0 data input pin. |
| | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | I2C2_SCL | I/O | MFP6 | I2C2 clock pin. |
| | | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | | BPWM1_CH4 | I/O | MFP11 | BPWM1 channel 4 output/capture input. |
| | | QEI1_B | I | MFP12 | Quadrature encoder 1 phase B input |
| | | USB_D+ | A | MFP14 | USB differential signal D+. |
| | 88 | PA.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | I2S0_DO | O | MFP2 | I2S0 data output pin. |
| | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | I2C2_SDA | I/O | MFP6 | I2C2 data input/output pin. |
| | | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | | BPWM1_CH5 | I/O | MFP11 | BPWM1 channel 5 output/capture input. |
| | | EPWM0_SYNC_IN | I | MFP12 | EPWM0 counter synchronous trigger input pin. |
| | | USB_OTG_ID | I | MFP14 | USB_ identification. |
| 41 | 89 | HSUSB_VRES | A | MFP0 | HSUSB module reference resister |
| 42 | 90 | HSUSB_VDD33 | P | MFP0 | Power supply for HSUSB VDD33 |
| 43 | 91 | HSUSB_VBUS | P | MFP0 | HSUSB Power supply from USB host or HUB. |
| 44 | 92 | HSUSB_D- | A | MFP0 | HSUSB differential signal D-. |
| 45 | 93 | HSUSB_VSS | P | MFP0 | Ground pin for HSUSB. |
| 46 | 94 | HSUSB_D+ | A | MFP0 | HSUSB differential signal D+. |
| 47 | 95 | HSUSB_VDD12_CAP | A | MFP0 | HSUSB Internal power regulator output 1.2V decoupling pin.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| 48 | 96 | HSUSB_ID | I | MFP0 | HSUSB identification. |
| | 97 | PE.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | | QEI1_INDEX | I | MFP11 | Quadrature encoder 1 index input |
| | | EPWM0_CH0 | I/O | MFP12 | EPWM0 channel 0 output/capture input. |
| | | BPWM0_CH5 | I/O | MFP13 | BPWM0 channel 5 output/capture input. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | 98 | PE.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | SPI3_I2SMCLK | I/O | MFP5 | SPI3 I2S master clock output pin |
| | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | USCI0_CTL0 | I/O | MFP7 | USCI0 control 0 pin. |
| | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | | QEI1_A | I | MFP11 | Quadrature encoder 1 phase A input |
| | | EPWM0_CH1 | I/O | MFP12 | EPWM0 channel 1 output/capture input. |
| | | BPWM0_CH4 | I/O | MFP13 | BPWM0 channel 4 output/capture input. |
| | 99 | PE.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | | SPI3_SS | I/O | MFP5 | SPI3 slave select pin. |
| | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | USCI0_CTL1 | I/O | MFP7 | USCI0 control 1 pin. |
| | | QEI1_B | I | MFP11 | Quadrature encoder 1 phase B input |
| | | EPWM0_CH2 | I/O | MFP12 | EPWM0 channel 2 output/capture input. |
| | | BPWM0_CH3 | I/O | MFP13 | BPWM0 channel 3 output/capture input. |
| | 100 | PE.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | SPI3_CLK | I/O | MFP5 | SPI3 serial clock pin. |
| | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | USCI0_DAT1 | I/O | MFP7 | USCI0 data 1 pin. |
| | | QEI0_INDEX | I | MFP11 | Quadrature encoder 0 index input |
| | | EPWM0_CH3 | I/O | MFP12 | EPWM0 channel 3 output/capture input. |
| | | BPWM0_CH2 | I/O | MFP13 | BPWM0 channel 2 output/capture input. |
| | 101 | PE.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | SPI3_MISO | I/O | MFP5 | SPI3 MISO (Master In, Slave Out) pin. |
| | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | USCI0_DAT0 | I/O | MFP7 | USCI0 data 0 pin. |
| | | QEI0_A | I | MFP11 | Quadrature encoder 0 phase A input |
| | | EPWM0_CH4 | I/O | MFP12 | EPWM0 channel 4 output/capture input. |
| | | BPWM0_CH1 | I/O | MFP13 | BPWM0 channel 1 output/capture input. |
| | 102 | PE.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | SPI3_MOSI | I/O | MFP5 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | USCI0_CLK | I/O | MFP7 | USCI0 clock pin. |
| | | QEI0_B | I | MFP11 | Quadrature encoder 0 phase B input |
| | | EPWM0_CH5 | I/O | MFP12 | EPWM0 channel 5 output/capture input. |
| | | BPWM0_CH0 | I/O | MFP13 | BPWM0 channel 0 output/capture input. |
| | 103 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | 104 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 105 | PE.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | SC2_DAT | I/O | MFP4 | Smart Card 2 data pin. |
| | | I2S0_BCLK | O | MFP5 | I2S0 bit clock output pin. |
| | | SPI1_MISO | I/O | MFP6 | SPI1 MISO (Master In, Slave Out) pin. |
| | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | UART4_nCTS | I | MFP9 | UART4 clear to Send input pin. |
| | 106 | PE.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | SC2_CLK | O | MFP4 | Smart Card 2 clock pin. |
| | | I2S0_MCLK | O | MFP5 | I2S0 master clock output pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | SPI1_MOSI | I/O | MFP6 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | UART4_nRTS | O | MFP9 | UART4 request to Send output pin. |
| | 107 | PH.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | SC2_PWR | O | MFP4 | Smart Card 2 power pin. |
| | | I2S0_DI | I | MFP5 | I2S0 data input pin. |
| | | SPI1_CLK | I/O | MFP6 | SPI1 serial clock pin. |
| | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | UART1_TXD | O | MFP10 | UART1 data transmitter output pin. |
| | 108 | PH.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | SC2_RST | O | MFP4 | Smart Card 2 reset pin. |
| | | I2S0_DO | O | MFP5 | I2S0 data output pin. |
| | | SPI1_SS | I/O | MFP6 | SPI1 slave select pin. |
| | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | UART1_RXD | I | MFP10 | UART1 data receiver input pin. |
| | 109 | PH.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | SC2_nCD | I | MFP4 | Smart Card 2 card detect pin. |
| | | I2S0_LRCK | O | MFP5 | I2S0 left right channel clock output pin. |
| | | SPI1_I2SMCLK | I/O | MFP6 | SPI1 I2S master clock output pin |
| | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | UART0_TXD | O | MFP8 | UART0 data transmitter output pin. |
| | 110 | PH.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | UART0_RXD | I | MFP8 | UART0 data receiver input pin. |
| | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | 111 | PD.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | SPI3_I2SMCLK | I/O | MFP3 | SPI3 I2S master clock output pin |
| | | SC1_nCD | I | MFP4 | Smart Card 1 card detect pin. |
| | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| 49 | 112 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| 50 | 113 | LDO_CAP | A | MFP0 | LDO output pin. |
| 51 | 114 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 52 | 115 | PC.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | SC1_nCD | I | MFP3 | Smart Card 1 card detect pin. |
| | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | USCI0_CTL0 | I/O | MFP5 | USCI0 control 0 pin. |
| | | QSPI0_CLK | I/O | MFP6 | Quad SPI0 serial clock pin. |
| | | EPWM0_SYNC_IN | I | MFP11 | EPWM0 counter synchronous trigger input pin. |
| | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | | HSUSB_VBUS_ST | I | MFP15 | HSUSB external VBUS regulator status pin. |
| 53 | 116 | PB.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH15 | A | MFP1 | EADC0 channel 15 analog input. |
| | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | SC1_PWR | O | MFP3 | Smart Card 1 power pin. |
| | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | USCI0_CTL1 | I/O | MFP5 | USCI0 control 1 pin. |
| | | UART0_nCTS | I | MFP6 | UART0 clear to Send input pin. |
| | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | I2C2_SMBAL | O | MFP8 | I2C2 SMBus SMBALTER pin |
| | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | | HSUSB_VBUS_EN | O | MFP15 | HSUSB external VBUS regulator enable pin. |
| 54 | 117 | PB.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH14 | A | MFP1 | EADC0 channel 14 analog input. |
| | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | SC1_RST | O | MFP3 | Smart Card 1 reset pin. |
| | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | USCI0_DAT1 | I/O | MFP5 | USCI0 data 1 pin. |
| | | UART0_nRTS | O | MFP6 | UART0 request to Send output pin. |
| | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | I2C2_SMBSUS | O | MFP8 | I2C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | CLKO | O | MFP14 | Clock Out |
| 55 | 118 | PB.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH13 | A | MFP1 | EADC0 channel 13 analog input. |
| | | DAC1_OUT | A | MFP1 | DAC1 channel analog output. |
| | | ACMP0_P3 | A | MFP1 | Analog comparator 0 positive input 3 pin. |
| | | ACMP1_P3 | A | MFP1 | Analog comparator 1 positive input 3 pin. |
| | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | SC1_DAT | I/O | MFP3 | Smart Card 1 data pin. |
| | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | USCI0_DAT0 | I/O | MFP5 | USCI0 data 0 pin. |
| | | UART0_TXD | O | MFP6 | UART0 data transmitter output pin. |
| | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | I2C2_SCL | I/O | MFP8 | I2C2 clock pin. |
| | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| 56 | 119 | PB.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH12 | A | MFP1 | EADC0 channel 12 analog input. |
| | | DAC0_OUT | A | MFP1 | DAC0 channel analog output. |
| | | ACMP0_P2 | A | MFP1 | Analog comparator 0 positive input 2 pin. |
| | | ACMP1_P2 | A | MFP1 | Analog comparator 1 positive input 2 pin. |
| | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | SC1_CLK | O | MFP3 | Smart Card 1 clock pin. |
| | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | USCI0_CLK | I/O | MFP5 | USCI0 clock pin. |
| | | UART0_RXD | I | MFP6 | UART0 data receiver input pin. |
| | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | I2C2_SDA | I/O | MFP8 | I2C2 data input/output pin. |
| | | SD0_nCD | I | MFP9 | SD/SDIO0 card detect input pin |
| | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| 57 | 120 | $AV_{DD}$ | P | MFP0 | Power supply for internal analog circuit. |
| 58 | 121 | $V_{REF}$ | A | MFP0 | ADC reference voltage input.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| 59 | 122 | $AV_{SS}$ | P | MFP0 | Ground pin for analog circuit. |
| 60 | 123 | PB.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH11 | A | MFP1 | EADC0 channel 11 analog input. |
| | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | UART0_nCTS | I | MFP5 | UART0 clear to Send input pin. |
| | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | I2C1_SCL | I/O | MFP7 | I2C1 clock pin. |
| | | CAN0_TXD | O | MFP8 | CAN0 bus transmitter output. |
| | | SPI0_I2SMCLK | I/O | MFP9 | SPI0 I2S master clock output pin |
| | | BPWM1_CH0 | I/O | MFP10 | BPWM1 channel 0 output/capture input. |
| | | SPI3_CLK | I/O | MFP11 | SPI3 serial clock pin. |
| | | HSUSB_VBUS_ST | I | MFP14 | HSUSB external VBUS regulator status pin. |
| 61 | 124 | PB.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH10 | A | MFP1 | EADC0 channel 10 analog input. |
| | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | USCI1_CTL0 | I/O | MFP4 | USCI1 control 0 pin. |
| | | UART0_nRTS | O | MFP5 | UART0 request to Send output pin. |
| | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | I2C1_SDA | I/O | MFP7 | I2C1 data input/output pin. |
| | | CAN0_RXD | I | MFP8 | CAN0 bus receiver input. |
| | | BPWM1_CH1 | I/O | MFP10 | BPWM1 channel 1 output/capture input. |
| | | SPI3_SS | I/O | MFP11 | SPI3 slave select pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | HSUSB_VBUS_EN | O | MFP14 | HSUSB external VBUS regulator enable pin. |
| 62 | 125 | PB.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH9 | A | MFP1 | EADC0 channel 9 analog input. |
| | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | USCI1_CTL1 | I/O | MFP4 | USCI1 control 1 pin. |
| | | UART0_TXD | O | MFP5 | UART0 data transmitter output pin. |
| | | UART1_nCTS | I | MFP6 | UART1 clear to Send input pin. |
| | | I2C1_SMBAL | O | MFP7 | I2C1 SMBus SMBALTER pin |
| | | BPWM1_CH2 | I/O | MFP10 | BPWM1 channel 2 output/capture input. |
| | | SPI3_MISO | I/O | MFP11 | SPI3 MISO (Master In, Slave Out) pin. |
| | | INT7 | I | MFP13 | External interrupt 7 input pin. |
| 63 | 126 | PB.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH8 | A | MFP1 | EADC0 channel 8 analog input. |
| | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | USCI1_CLK | I/O | MFP4 | USCI1 clock pin. |
| | | UART0_RXD | I | MFP5 | UART0 data receiver input pin. |
| | | UART1_nRTS | O | MFP6 | UART1 request to Send output pin. |
| | | I2C1_SMBSUS | O | MFP7 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | BPWM1_CH3 | I/O | MFP10 | BPWM1 channel 3 output/capture input. |
| | | SPI3_MOSI | I/O | MFP11 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | INT6 | I | MFP13 | External interrupt 6 input pin. |
| 64 | 127 | PB.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH7 | A | MFP1 | EADC0 channel 7 analog input. |
| | | EBI_nWRL | O | MFP2 | EBI low byte write enable output pin. |
| | | USCI1_DAT0 | I/O | MFP4 | USCI1 data 0 pin. |
| | | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | SD1_CMD | I/O | MFP7 | SD/SDIO1 command/response pin |
| | | EBI_nCS0 | O | MFP8 | EBI chip select 0 output pin. |
| | | BPWM1_CH4 | I/O | MFP10 | BPWM1 channel 4 output/capture input. |
| | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | INT5 | I | MFP13 | External interrupt 5 input pin. |
| | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |

| 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|
| | | ACMP0_O | O | MFP15 | Analog comparator 0 output pin. |
| 1 | 128 | PB.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | EADC0_CH6 | A | MFP1 | EADC0 channel 6 analog input. |
| | | EBI_nWRH | O | MFP2 | EBI high byte write enable output pin |
| | | USCI1_DAT1 | I/O | MFP4 | USCI1 data 1 pin. |
| | | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | SD1_CLK | O | MFP7 | SD/SDIO1 clock output pin |
| | | EBI_nCS1 | O | MFP8 | EBI chip select 1 output pin. |
| | | BPWM1_CH5 | I/O | MFP10 | BPWM1 channel 5 output/capture input. |
| | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | INT4 | I | MFP13 | External interrupt 4 input pin. |
| | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | | ACMP1_O | O | MFP15 | Analog comparator 1 output pin. |

### 4.2.4 M484 Series Pin Description

64 Pin: M484SGAAE, M484SIDAE

64 Pin 2 USB: M484SGAAE2U, M484SIDAE2U

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| 2 | 2 | 1 | PB.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH5 | A | MFP1 | EADC0 channel 5 analog input. |
| | | | ACMP1_N | A | MFP1 | Analog comparator 1 negative input pin. |
| | | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | | SPI1_MISO | I/O | MFP5 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | I2C0_SCL | I/O | MFP6 | I2C0 clock pin. |
| | | | UART5_TXD | O | MFP7 | UART5 data transmitter output pin. |
| | | | USCI1_CTL0 | I/O | MFP8 | USCI1 control 0 pin. |
| | | | SC0_CLK | O | MFP9 | Smart Card 0 clock pin. |
| | | | I2S0_BCLK | O | MFP10 | I2S0 bit clock output pin. |
| | | | EPWM0_CH0 | I/O | MFP11 | EPWM0 channel 0 output/capture input. |
| | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| 3 | 3 | 2 | PB.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH4 | A | MFP1 | EADC0 channel 4 analog input. |
| | | | ACMP1_P1 | A | MFP1 | Analog comparator 1 positive input 1 pin. |
| | | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | | SPI1_MOSI | I/O | MFP5 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | I2C0_SDA | I/O | MFP6 | I2C0 data input/output pin. |
| | | | UART5_RXD | I | MFP7 | UART5 data receiver input pin. |
| | | | USCI1_CTL1 | I/O | MFP8 | USCI1 control 1 pin. |
| | | | SC0_DAT | I/O | MFP9 | Smart Card 0 data pin. |
| | | | I2S0_MCLK | O | MFP10 | I2S0 master clock output pin. |
| | | | EPWM0_CH1 | I/O | MFP11 | EPWM0 channel 1 output/capture input. |
| | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| 4 | 4 | 3 | PB.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH3 | A | MFP1 | EADC0 channel 3 analog input. |
| | | | ACMP0_N | A | MFP1 | Analog comparator 0 negative input pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | | | SPI1_CLK | I/O | MFP5 | SPI1 serial clock pin. |
| | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | UART5_nRTS | O | MFP7 | UART5 request to Send output pin. |
| | | | USCI1_DAT1 | I/O | MFP8 | USCI1 data 1 pin. |
| | | | SC0_RST | O | MFP9 | Smart Card 0 reset pin. |
| | | | I2S0_DI | I | MFP10 | I2S0 data input pin. |
| | | | EPWM0_CH2 | I/O | MFP11 | EPWM0 channel 2 output/capture input. |
| | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| 5 | 5 | 4 | PB.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH2 | A | MFP1 | EADC0 channel 2 analog input. |
| | | | ACMP0_P1 | A | MFP1 | Analog comparator 0 positive input 1 pin. |
| | | | OPA0_O | A | MFP1 | Operational amplifier 0 output pin. |
| | | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | | SPI1_SS | I/O | MFP5 | SPI1 slave select pin. |
| | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | UART5_nCTS | I | MFP7 | UART5 clear to Send input pin. |
| | | | USCI1_DAT0 | I/O | MFP8 | USCI1 data 0 pin. |
| | | | SC0_PWR | O | MFP9 | Smart Card 0 power pin. |
| | | | I2S0_DO | O | MFP10 | I2S0 data output pin. |
| | | | EPWM0_CH3 | I/O | MFP11 | EPWM0 channel 3 output/capture input. |
| | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| | | 5 | PC.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR4 | O | MFP2 | EBI address bus bit 4. |
| | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | SPI3_MISO | I/O | MFP6 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | SC0_nCD | I | MFP9 | Smart Card 0 card detect pin. |
| | | | ECAP1_IC2 | I | MFP11 | Enhanced capture unit 1 input 2 pin. |
| | | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| | | 6 | PC.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR5 | O | MFP2 | EBI address bus bit 5. |
| | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | SPI3_MOSI | I/O | MFP6 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | ECAP1_IC1 | I | MFP11 | Enhanced capture unit 1 input 1 pin. |
| | | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| | | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | | 7 | PC.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR6 | O | MFP2 | EBI address bus bit 6. |
| | | | SPI3_CLK | I/O | MFP6 | SPI3 serial clock pin. |
| | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | ECAP1_IC0 | I | MFP11 | Enhanced capture unit 1 input 0 pin. |
| | | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| | | 8 | PC.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR7 | O | MFP2 | EBI address bus bit 7. |
| | | | SPI3_SS | I/O | MFP6 | SPI3 slave select pin. |
| | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 6 | 6 | 9 | PB.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH1 | A | MFP1 | EADC0 channel 1 analog input. |
| | | | OPA0_N | A | MFP1 | Operational amplifier 0 negative input pin. |
| | | | EBI_ADR8 | O | MFP2 | EBI address bus bit 8. |
| | | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | | SPI3_I2SMCLK | I/O | MFP6 | SPI3 I2S master clock output pin |
| | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | USCI1_CLK | I/O | MFP8 | USCI1 clock pin. |
| | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | I2S0_LRCK | O | MFP10 | I2S0 left right channel clock output pin. |
| | | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | EPWM0_BRAKE0 | I | MFP13 | EPWM0 Brake 0 input pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| 7 | 7 | 10 | PB.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH0 | A | MFP1 | EADC0 channel 0 analog input. |
| | | | OPA0_P | A | MFP1 | Operational amplifier 0 positive input pin. |
| | | | EBI_ADR9 | O | MFP2 | EBI address bus bit 9. |
| | | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | SPI0_I2SMCLK | I/O | MFP8 | SPI0 I2S master clock output pin |
| | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | EPWM0_BRAKE1 | I | MFP13 | EPWM0 Brake 1 input pin. |
| | | 11 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | | 12 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 8 | 8 | 13 | PA.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ACMP0_P0 | A | MFP1 | Analog comparator 0 positive input 0 pin. |
| | | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | | SC2_PWR | O | MFP3 | Smart Card 2 power pin. |
| | | | SPI2_SS | I/O | MFP4 | SPI2 slave select pin. |
| | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | USCI0_CLK | I/O | MFP6 | USCI0 clock pin. |
| | | | I2C2_SCL | I/O | MFP7 | I2C2 clock pin. |
| | | | BPWM0_CH0 | I/O | MFP9 | BPWM0 channel 0 output/capture input. |
| | | | EPWM0_SYNC_OUT | O | MFP10 | EPWM0 counter synchronous trigger output pin. |
| | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | | DAC1_ST | I | MFP14 | DAC1 external trigger input. |
| 9 | 9 | 14 | PA.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ACMP1_P0 | A | MFP1 | Analog comparator 1 positive input 0 pin. |
| | | | OPA1_O | A | MFP1 | Operational amplifier 1 output pin. |
| | | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | | SC2_RST | O | MFP3 | Smart Card 2 reset pin. |
| | | | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | | USCI0_DAT0 | I/O | MFP6 | USCI0 data 0 pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | I2C2_SDA | I/O | MFP7 | I2C2 data input/output pin. |
| | | | BPWM0_CH1 | I/O | MFP9 | BPWM0 channel 1 output/capture input. |
| | | | QEI1_INDEX | I | MFP10 | Quadrature encoder 1 index input |
| | | | ECAP0_IC0 | I | MFP11 | Enhanced capture unit 0 input 0 pin. |
| | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | DAC0_ST | I | MFP14 | DAC0 external trigger input. |
| 10 | 10 | 15 | PA.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA1_N | A | MFP1 | Operational amplifier 1 negative input pin. |
| | | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | | SC2_DAT | I/O | MFP3 | Smart Card 2 data pin. |
| | | | SPI2_MISO | I/O | MFP4 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | | USCI0_DAT1 | I/O | MFP6 | USCI0 data 1 pin. |
| | | | UART1_TXD | O | MFP7 | UART1 data transmitter output pin. |
| | | | BPWM0_CH2 | I/O | MFP9 | BPWM0 channel 2 output/capture input. |
| | | | QEI1_A | I | MFP10 | Quadrature encoder 1 phase A input |
| | | | ECAP0_IC1 | I | MFP11 | Enhanced capture unit 0 input 1 pin. |
| | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| 11 | 11 | 16 | PA.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA1_P | A | MFP1 | Operational amplifier 1 positive input pin. |
| | | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | | SC2_CLK | O | MFP3 | Smart Card 2 clock pin. |
| | | | SPI2_MOSI | I/O | MFP4 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | | USCI0_CTL1 | I/O | MFP6 | USCI0 control 1 pin. |
| | | | UART1_RXD | I | MFP7 | UART1 data receiver input pin. |
| | | | BPWM0_CH3 | I/O | MFP9 | BPWM0 channel 3 output/capture input. |
| | | | QEI1_B | I | MFP10 | Quadrature encoder 1 phase B input |
| | | | ECAP0_IC2 | I | MFP11 | Enhanced capture unit 0 input 2 pin. |
| | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| | | | INT4 | I | MFP15 | External interrupt 4 input pin. |
| | | 17 | PC.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | | SC2_nCD | I | MFP3 | Smart Card 2 card detect pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI2_I2SMCLK | I/O | MFP4 | SPI2 I2S master clock output pin |
| | | | USCI0_CTL0 | I/O | MFP6 | USCI0 control 0 pin. |
| | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | BPWM0_CH4 | I/O | MFP9 | BPWM0 channel 4 output/capture input. |
| | | | CLKO | O | MFP13 | Clock Out |
| | | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | | 18 | PD.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA2_O | A | MFP1 | Operational amplifier 2 output pin. |
| | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | BPWM0_CH5 | I/O | MFP9 | BPWM0 channel 5 output/capture input. |
| | | | QEI0_INDEX | I | MFP10 | Quadrature encoder 0 index input |
| | | | CLKO | O | MFP13 | Clock Out |
| | | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | | | INT5 | I | MFP15 | External interrupt 5 input pin. |
| | | 19 | PD.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA2_N | A | MFP1 | Operational amplifier 2 negative input pin. |
| | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | UART1_TXD | O | MFP3 | UART1 data transmitter output pin. |
| | | | QEI0_A | I | MFP10 | Quadrature encoder 0 phase A input |
| | | | INT6 | I | MFP15 | External interrupt 6 input pin. |
| | | 20 | PD.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA2_P | A | MFP1 | Operational amplifier 2 positive input pin. |
| | | | EBI_nCS2 | O | MFP2 | EBI chip select 2 output pin. |
| | | | UART1_RXD | I | MFP3 | UART1 data receiver input pin. |
| | | | QEI0_B | I | MFP10 | Quadrature encoder 0 phase B input |
| | | | INT7 | I | MFP15 | External interrupt 7 input pin. |
| | | 21 | PG.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | | SPI2_SS | I/O | MFP3 | SPI2 slave select pin. |
| | | | I2C0_SMBAL | O | MFP4 | I2C0 SMBus SMBALTER pin |
| | | | I2C1_SCL | I/O | MFP5 | I2C1 clock pin. |
| | | | TM0 | I/O | MFP13 | Timer0 event counter input/toggle output pin. |
| | | 22 | PG.3 | I/O | MFP0 | General purpose digital I/O pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | | SPI2_CLK | I/O | MFP3 | SPI2 serial clock pin. |
| | | | I2C0_SMBSUS | O | MFP4 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | I2C1_SDA | I/O | MFP5 | I2C1 data input/output pin. |
| | | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | | 23 | PG.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | | | SPI2_MISO | I/O | MFP3 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | TM2 | I/O | MFP13 | Timer2 event counter input/toggle output pin. |
| | | 24 | PF.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | | | SPI2_MOSI | I/O | MFP3 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | TAMPER5 | I/O | MFP10 | TAMPER detector loop pin 5. |
| | | | TM3 | I/O | MFP13 | Timer3 event counter input/toggle output pin. |
| | | 25 | PF.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | | SC0_nCD | I | MFP3 | Smart Card 0 card detect pin. |
| | | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |
| | | | SPI0_I2SMCLK | I/O | MFP5 | SPI0 I2S master clock output pin |
| | | | TAMPER4 | I/O | MFP10 | TAMPER detector loop pin 4. |
| | | 26 | PF.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | SC0_PWR | O | MFP3 | Smart Card 0 power pin. |
| | | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |
| | | | SPI0_SS | I/O | MFP5 | SPI0 slave select pin. |
| | | | TAMPER3 | I/O | MFP10 | TAMPER detector loop pin 3. |
| | | 27 | PF.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | | SC0_RST | O | MFP3 | Smart Card 0 reset pin. |
| | | | I2S0_DI | I | MFP4 | I2S0 data input pin. |
| | | | SPI0_CLK | I/O | MFP5 | SPI0 serial clock pin. |
| | | | TAMPER2 | I/O | MFP10 | TAMPER detector loop pin 2. |
| | | 28 | PF.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC0_DAT | I/O | MFP3 | Smart Card 0 data pin. |
| | | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | | SPI0_MISO | I/O | MFP5 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | | TAMPER1 | I/O | MFP10 | TAMPER detector loop pin 1. |
| 12 | 12 | 29 | PF.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | | SC0_CLK | O | MFP3 | Smart Card 0 clock pin. |
| | | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | | SPI0_MOSI | I/O | MFP5 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | EBI_nCS0 | O | MFP7 | EBI chip select 0 output pin. |
| | | | TAMPER0 | I/O | MFP10 | TAMPER detector loop pin 0. |
| 13 | 13 | 30 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 14 | 14 | 31 | PF.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART2_RXD | I | MFP2 | UART2 data receiver input pin. |
| | | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | | | BPWM0_CH4 | I/O | MFP8 | BPWM0 channel 4 output/capture input. |
| | | | EPWM0_SYNC_OUT | O | MFP9 | EPWM0 counter synchronous trigger output pin. |
| | | | X32_IN | I | MFP10 | External 32.768 kHz crystal input pin. |
| | | | EADC0_ST | I | MFP11 | EADC0 external trigger input. |
| 15 | 15 | 32 | PF.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART2_TXD | O | MFP2 | UART2 data transmitter output pin. |
| | | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| | | | BPWM0_CH5 | I/O | MFP8 | BPWM0 channel 5 output/capture input. |
| | | | X32_OUT | O | MFP10 | External 32.768 kHz crystal output pin. |
| | | 33 | PH.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | | SPI1_MISO | I/O | MFP3 | SPI1 MISO (Master In, Slave Out) pin. |
| | | 34 | PH.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | | SPI1_MOSI | I/O | MFP3 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | 35 | PH.6 | I/O | MFP0 | General purpose digital I/O pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | | SPI1_CLK | I/O | MFP3 | SPI1 serial clock pin. |
| | | 36 | PH.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | | SPI1_SS | I/O | MFP3 | SPI1 slave select pin. |
| 16 | 16 | 37 | PF.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | XT1_IN | I | MFP10 | External 4~24 MHz (high speed) crystal input pin. |
| | | | BPWM1_CH0 | I/O | MFP11 | BPWM1 channel 0 output/capture input. |
| 17 | 17 | 38 | PF.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | QSPI0_CLK | I/O | MFP5 | Quad SPI0 serial clock pin. |
| | | | XT1_OUT | O | MFP10 | External 4~24 MHz (high speed) crystal output pin. |
| | | | BPWM1_CH1 | I/O | MFP11 | BPWM1 channel 1 output/capture input. |
| | | 39 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | | 40 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | 41 | PE.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |
| | | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | | USCI1_CTL1 | I/O | MFP6 | USCI1 control 1 pin. |
| | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | EPWM0_CH0 | I/O | MFP10 | EPWM0 channel 0 output/capture input. |
| | | | EPWM0_BRAKE0 | I | MFP11 | EPWM0 Brake 0 input pin. |
| | | | ECAP0_IC0 | I | MFP12 | Enhanced capture unit 0 input 0 pin. |
| | | | TRACE_CLK | O | MFP14 | ETM Trace Clock output pin |
| | | 42 | PE.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |
| | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | EPWM0_CH1 | I/O | MFP10 | EPWM0 channel 1 output/capture input. |
| | | | EPWM0_BRAKE1 | I | MFP11 | EPWM0 Brake 1 input pin. |
| | | | ECAP0_IC1 | I | MFP12 | Enhanced capture unit 0 input 1 pin. |
| | | | TRACE_DATA0 | O | MFP14 | ETM Trace Data 0 output pin |
| | | 43 | PE.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | | I2S0_DI | I | MFP4 | I2S0 data input pin. |
| | | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | USCI1_DAT0 | I/O | MFP6 | USCI1 data 0 pin. |
| | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | EPWM0_CH2 | I/O | MFP10 | EPWM0 channel 2 output/capture input. |
| | | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | | ECAP0_IC2 | I | MFP12 | Enhanced capture unit 0 input 2 pin. |
| | | | TRACE_DATA1 | O | MFP14 | ETM Trace Data 1 output pin |
| | | 44 | PE.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | | USCI1_DAT1 | I/O | MFP6 | USCI1 data 1 pin. |
| | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | | EPWM0_CH3 | I/O | MFP10 | EPWM0 channel 3 output/capture input. |
| | | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | | ECAP1_IC2 | I | MFP13 | Enhanced capture unit 1 input 2 pin. |
| | | | TRACE_DATA2 | O | MFP14 | ETM Trace Data 2 output pin |
| | | 45 | PE.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | | SPI2_I2SMCLK | I/O | MFP5 | SPI2 I2S master clock output pin |
| | | | USCI1_CLK | I/O | MFP6 | USCI1 clock pin. |
| | | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EPWM0_CH4 | I/O | MFP10 | EPWM0 channel 4 output/capture input. |
| | | | ECAP1_IC1 | I | MFP13 | Enhanced capture unit 1 input 1 pin. |
| | | | TRACE_DATA3 | O | MFP14 | ETM Trace Data 3 output pin |
| | | 46 | PE.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | UART4_nRTS | O | MFP5 | UART4 request to Send output pin. |
| | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | | EPWM0_CH5 | I/O | MFP10 | EPWM0 channel 5 output/capture input. |
| | | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | | BPWM1_CH5 | I/O | MFP12 | BPWM1 channel 5 output/capture input. |
| | | | ECAP1_IC0 | I | MFP13 | Enhanced capture unit 1 input 0 pin. |
| | | 47 | PC.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | UART4_nCTS | I | MFP5 | UART4 clear to Send input pin. |
| | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | | BPWM1_CH4 | I/O | MFP12 | BPWM1 channel 4 output/capture input. |
| 18 | 18 | 48 | PC.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | | SPI1_MISO | I/O | MFP4 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | UART4_TXD | O | MFP5 | UART4 data transmitter output pin. |
| | | | SC2_PWR | O | MFP6 | Smart Card 2 power pin. |
| | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| 19 | 19 | 49 | PC.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | | SPI1_MOSI | I/O | MFP4 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | UART4_RXD | I | MFP5 | UART4 data receiver input pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC2_RST | O | MFP6 | Smart Card 2 reset pin. |
| | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| 20 | 20 | 50 | PA.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | | SPI1_CLK | I/O | MFP4 | SPI1 serial clock pin. |
| | | | SC2_DAT | I/O | MFP6 | Smart Card 2 data pin. |
| | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | | EPWM1_CH4 | I/O | MFP11 | EPWM1 channel 4 output/capture input. |
| | | | BPWM1_CH2 | I/O | MFP12 | BPWM1 channel 2 output/capture input. |
| | | | ACMP0_WLAT | I | MFP13 | Analog comparator 0 window latch input pin |
| | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| 21 | 21 | 51 | PA.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | | SPI1_SS | I/O | MFP4 | SPI1 slave select pin. |
| | | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | | | SC2_CLK | O | MFP6 | Smart Card 2 clock pin. |
| | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | | EPWM1_CH5 | I/O | MFP11 | EPWM1 channel 5 output/capture input. |
| | | | BPWM1_CH3 | I/O | MFP12 | BPWM1 channel 3 output/capture input. |
| | | | ACMP1_WLAT | I | MFP13 | Analog comparator 1 window latch input pin |
| | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| 22 | 22 | 52 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| 23 | 23 | 53 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 24 | 24 | 54 | LDO_CAP | A | MFP0 | LDO output pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| 25 | 25 | 55 | PA.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_D2 | I/O | MFP2 | SPIM data 2 pin for Quad Mode I/O. |
| | | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | SPI1_I2SMCLK | I/O | MFP4 | SPI1 I2S master clock output pin |
| | | | SD1_CMD | I/O | MFP5 | SD/SDIO1 command/response pin |
| | | | SC2_nCD | I | MFP6 | Smart Card 2 card detect pin. |
| | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | | | EPWM0_CH0 | I/O | MFP13 | EPWM0 channel 0 output/capture input. |
| | | | QEI0_INDEX | I | MFP14 | Quadrature encoder 0 index input |
| 26 | 26 | 56 | PA.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_D3 | I/O | MFP2 | SPIM data 3 pin for Quad Mode I/O. |
| | | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | SD1_CLK | O | MFP5 | SD/SDIO1 clock output pin |
| | | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | | | EPWM0_CH1 | I/O | MFP13 | EPWM0 channel 1 output/capture input. |
| | | | QEI0_A | I | MFP14 | Quadrature encoder 0 phase A input |
| 27 | 27 | 57 | PA.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_SS | I/O | MFP2 | SPIM slave select pin. |
| | | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EPWM0_CH2 | I/O | MFP13 | EPWM0 channel 2 output/capture input. |
| | | | QEI0_B | I | MFP14 | Quadrature encoder 0 phase B input |
| 28 | 28 | 58 | PA.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_CLK | I/O | MFP2 | SPIM serial clock pin. |
| | | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | | | EPWM0_CH3 | I/O | MFP13 | EPWM0 channel 3 output/capture input. |
| 29 | 29 | 59 | PA.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_MISO | I/O | MFP2 | SPIM MISO (Master In, Slave Out) pin. |
| | | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | | | EPWM0_CH4 | I/O | MFP13 | EPWM0 channel 4 output/capture input. |
| | | | DAC1_ST | I | MFP15 | DAC1 external trigger input. |
| 30 | 30 | 60 | PA.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_MOSI | I/O | MFP2 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | | | EPWM0_CH5 | I/O | MFP13 | EPWM0 channel 5 output/capture input. |
| | | | DAC0_ST | I | MFP15 | DAC0 external trigger input. |
| 31 | 31 | 61 | $V_{DDIO}$ | P | MFP0 | Power supply for PA.0~PA.5. |
| | | 62 | PE.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | | UART2_TXD | O | MFP3 | UART2 data transmitter output pin. |
| | | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | | 63 | PE.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | | UART2_RXD | I | MFP3 | UART2 data receiver input pin. |
| 32 | 32 | 64 | nRESET | I | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 33 | 33 | 65 | PF.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_TXD | O | MFP2 | UART1 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP3 | I2C1 clock pin. |
| | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | ICE_DAT | O | MFP14 | Serial wired debugger data pin. |
| 34 | 34 | 66 | PF.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_RXD | I | MFP2 | UART1 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP3 | I2C1 data input/output pin. |
| | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | ICE_CLK | I | MFP14 | Serial wired debugger clock pin. |
| | | 67 | PD.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | | I2C2_SCL | I/O | MFP3 | I2C2 clock pin. |
| | | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | | 68 | PD.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | | I2C2_SDA | I/O | MFP3 | I2C2 data input/output pin. |
| | | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| 35 | | 69 | PC.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | | | SPIM_D2 | I/O | MFP3 | SPIM data 2 pin for Quad Mode I/O. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | QSPI0_MISO1 | I/O | MFP4 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | UART4_TXD | O | MFP11 | UART4 data transmitter output pin. |
| | | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| 36 | | 70 | PC.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | | SPIM_D3 | I/O | MFP3 | SPIM data 3 pin for Quad Mode I/O. |
| | | | QSPI0_MOSI1 | I/O | MFP4 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | SC1_nCD | I | MFP5 | Smart Card 1 card detect pin. |
| | | | I2S0_BCLK | O | MFP6 | I2S0 bit clock output pin. |
| | | | SPI1_I2SMCLK | I/O | MFP7 | SPI1 I2S master clock output pin |
| | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | UART4_RXD | I | MFP11 | UART4 data receiver input pin. |
| | | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| 37 | | 71 | PC.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | | SPIM_SS | I/O | MFP3 | SPIM slave select pin. |
| | | | QSPI0_SS | I/O | MFP4 | Quad SPI0 slave select pin. |
| | | | SC1_PWR | O | MFP5 | Smart Card 1 power pin. |
| | | | I2S0_MCLK | O | MFP6 | I2S0 master clock output pin. |
| | | | SPI1_MISO | I/O | MFP7 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | UART2_nRTS | O | MFP8 | UART2 request to Send output pin. |
| | | | I2C0_SMBAL | O | MFP9 | I2C0 SMBus SMBALTER pin |
| | | | UART3_TXD | O | MFP11 | UART3 data transmitter output pin. |
| | | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| 38 | | 72 | PC.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | | SPIM_CLK | I/O | MFP3 | SPIM serial clock pin. |
| | | | QSPI0_CLK | I/O | MFP4 | Quad SPI0 serial clock pin. |
| | | | SC1_RST | O | MFP5 | Smart Card 1 reset pin. |
| | | | I2S0_DI | I | MFP6 | I2S0 data input pin. |
| | | | SPI1_MOSI | I/O | MFP7 | SPI1 MOSI (Master Out, Slave In) pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | UART2_nCTS | I | MFP8 | UART2 clear to Send input pin. |
| | | | I2C0_SMBSUS | O | MFP9 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | UART3_RXD | I | MFP11 | UART3 data receiver input pin. |
| | | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 39 | 35 | 73 | PC.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | | SPIM_MISO | I/O | MFP3 | SPIM MISO (Master In, Slave Out) pin. |
| | | | QSPI0_MISO0 | I/O | MFP4 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | SC1_DAT | I/O | MFP5 | Smart Card 1 data pin. |
| | | | I2S0_DO | O | MFP6 | I2S0 data output pin. |
| | | | SPI1_CLK | I/O | MFP7 | SPI1 serial clock pin. |
| | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| 40 | 36 | 74 | PC.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | | SPIM_MOSI | I/O | MFP3 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | QSPI0_MOSI0 | I/O | MFP4 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | SC1_CLK | O | MFP5 | Smart Card 1 clock pin. |
| | | | I2S0_LRCK | O | MFP6 | I2S0 left right channel clock output pin. |
| | | | SPI1_SS | I/O | MFP7 | SPI1 slave select pin. |
| | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | | 75 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | | 76 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | 77 | PG.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | | SD1_DAT3 | I/O | MFP3 | SD/SDIO1 data line bit 3. |
| | | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | 78 | PG.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | | SD1_DAT2 | I/O | MFP3 | SD/SDIO1 data line bit 2. |
| | | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | | 79 | PG.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | | SD1_DAT1 | I/O | MFP3 | SD/SDIO1 data line bit 1. |
| | | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | | 80 | PG.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | | SD1_DAT0 | I/O | MFP3 | SD/SDIO1 data line bit 0. |
| | | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | | 81 | PG.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | | SD1_CMD | I/O | MFP3 | SD/SDIO1 command/response pin |
| | | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | | 82 | PG.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | | | SD1_CLK | O | MFP3 | SD/SDIO1 clock output pin |
| | | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | | 83 | PG.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SD1_nCD | I | MFP3 | SD/SDIO1 card detect input pin |
| | | | CLKO | O | MFP14 | Clock Out |
| | | | EADC0_ST | I | MFP15 | EADC0 external trigger input. |
| | | 84 | PD.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | SD0_nCD | I | MFP3 | SD/SDIO0 card detect input pin |
| | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC2_nCD | I | MFP7 | Smart Card 2 card detect pin. |
| | 37 | 85 | PA.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_BCLK | O | MFP2 | I2S0 bit clock output pin. |
| | | | UART4_TXD | O | MFP3 | UART4 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP4 | I2C1 clock pin. |
| | | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | | | BPWM1_CH2 | I/O | MFP11 | BPWM1 channel 2 output/capture input. |
| | | | QEI1_INDEX | I | MFP12 | Quadrature encoder 1 index input |
| | | | USB_VBUS | P | MFP14 | Power supply from USB host or HUB. |
| | 38 | 86 | PA.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_MCLK | O | MFP2 | I2S0 master clock output pin. |
| | | | UART4_RXD | I | MFP3 | UART4 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP4 | I2C1 data input/output pin. |
| | | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | | | BPWM1_CH3 | I/O | MFP11 | BPWM1 channel 3 output/capture input. |
| | | | QEI1_A | I | MFP12 | Quadrature encoder 1 phase A input |
| | | | USB_D- | A | MFP14 | USB differential signal D-. |
| | 39 | 87 | PA.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_DI | I | MFP2 | I2S0 data input pin. |
| | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | I2C2_SCL | I/O | MFP6 | I2C2 clock pin. |
| | | | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | | | BPWM1_CH4 | I/O | MFP11 | BPWM1 channel 4 output/capture input. |
| | | | QEI1_B | I | MFP12 | Quadrature encoder 1 phase B input |
| | | | USB_D+ | A | MFP14 | USB differential signal D+. |
| | 40 | 88 | PA.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_DO | O | MFP2 | I2S0 data output pin. |
| | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | I2C2_SDA | I/O | MFP6 | I2C2 data input/output pin. |
| | | | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | BPWM1_CH5 | I/O | MFP11 | BPWM1 channel 5 output/capture input. |
| | | | EPWM0_SYNC_IN | I | MFP12 | EPWM0 counter synchronous trigger input pin. |
| | | | USB_OTG_ID | I | MFP14 | USB_ identification. |
| 41 | 41 | 89 | HSUSB_VRES | A | MFP0 | HSUSB module reference resister |
| 42 | 42 | 90 | HSUSB_VDD33 | P | MFP0 | Power supply for HSUSB VDD33 |
| 43 | 43 | 91 | HSUSB_VBUS | P | MFP0 | HSUSB Power supply from USB host or HUB. |
| 44 | 44 | 92 | HSUSB_D- | A | MFP0 | HSUSB differential signal D-. |
| 45 | 45 | 93 | HSUSB_VSS | P | MFP0 | Ground pin for HSUSB. |
| 46 | 46 | 94 | HSUSB_D+ | A | MFP0 | HSUSB differential signal D+. |
| 47 | 47 | 95 | HSUSB_VDD12_CAP | A | MFP0 | HSUSB Internal power regulator output 1.2V decoupling pin.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| 48 | 48 | 96 | HSUSB_ID | I | MFP0 | HSUSB identification. |
| | | 97 | PE.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | | QEI1_INDEX | I | MFP11 | Quadrature encoder 1 index input |
| | | | EPWM0_CH0 | I/O | MFP12 | EPWM0 channel 0 output/capture input. |
| | | | BPWM0_CH5 | I/O | MFP13 | BPWM0 channel 5 output/capture input. |
| | | 98 | PE.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | | SPI3_I2SMCLK | I/O | MFP5 | SPI3 I2S master clock output pin |
| | | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | | USCI0_CTL0 | I/O | MFP7 | USCI0 control 0 pin. |
| | | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | | QEI1_A | I | MFP11 | Quadrature encoder 1 phase A input |
| | | | EPWM0_CH1 | I/O | MFP12 | EPWM0 channel 1 output/capture input. |
| | | | BPWM0_CH4 | I/O | MFP13 | BPWM0 channel 4 output/capture input. |
| | | 99 | PE.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI3_SS | I/O | MFP5 | SPI3 slave select pin. |
| | | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | | USCI0_CTL1 | I/O | MFP7 | USCI0 control 1 pin. |
| | | | QEI1_B | I | MFP11 | Quadrature encoder 1 phase B input |
| | | | EPWM0_CH2 | I/O | MFP12 | EPWM0 channel 2 output/capture input. |
| | | | BPWM0_CH3 | I/O | MFP13 | BPWM0 channel 3 output/capture input. |
| | | 100 | PE.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | | SPI3_CLK | I/O | MFP5 | SPI3 serial clock pin. |
| | | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | | USCI0_DAT1 | I/O | MFP7 | USCI0 data 1 pin. |
| | | | QEI0_INDEX | I | MFP11 | Quadrature encoder 0 index input |
| | | | EPWM0_CH3 | I/O | MFP12 | EPWM0 channel 3 output/capture input. |
| | | | BPWM0_CH2 | I/O | MFP13 | BPWM0 channel 2 output/capture input. |
| | | 101 | PE.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | | SPI3_MISO | I/O | MFP5 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | | USCI0_DAT0 | I/O | MFP7 | USCI0 data 0 pin. |
| | | | QEI0_A | I | MFP11 | Quadrature encoder 0 phase A input |
| | | | EPWM0_CH4 | I/O | MFP12 | EPWM0 channel 4 output/capture input. |
| | | | BPWM0_CH1 | I/O | MFP13 | BPWM0 channel 1 output/capture input. |
| | | 102 | PE.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | SPI3_MOSI | I/O | MFP5 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | | USCI0_CLK | I/O | MFP7 | USCI0 clock pin. |
| | | | QEI0_B | I | MFP11 | Quadrature encoder 0 phase B input |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EPWM0_CH5 | I/O | MFP12 | EPWM0 channel 5 output/capture input. |
| | | | BPWM0_CH0 | I/O | MFP13 | BPWM0 channel 0 output/capture input. |
| | | 103 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | | 104 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | 105 | PE.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | SC2_DAT | I/O | MFP4 | Smart Card 2 data pin. |
| | | | I2S0_BCLK | O | MFP5 | I2S0 bit clock output pin. |
| | | | SPI1_MISO | I/O | MFP6 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | | UART4_nCTS | I | MFP9 | UART4 clear to Send input pin. |
| | | 106 | PE.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | SC2_CLK | O | MFP4 | Smart Card 2 clock pin. |
| | | | I2S0_MCLK | O | MFP5 | I2S0 master clock output pin. |
| | | | SPI1_MOSI | I/O | MFP6 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | | UART4_nRTS | O | MFP9 | UART4 request to Send output pin. |
| | | 107 | PH.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | | SC2_PWR | O | MFP4 | Smart Card 2 power pin. |
| | | | I2S0_DI | I | MFP5 | I2S0 data input pin. |
| | | | SPI1_CLK | I/O | MFP6 | SPI1 serial clock pin. |
| | | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | | UART1_TXD | O | MFP10 | UART1 data transmitter output pin. |
| | | 108 | PH.9 | I/O | MFP0 | General purpose digital I/O pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | | SC2_RST | O | MFP4 | Smart Card 2 reset pin. |
| | | | I2S0_DO | O | MFP5 | I2S0 data output pin. |
| | | | SPI1_SS | I/O | MFP6 | SPI1 slave select pin. |
| | | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | | UART1_RXD | I | MFP10 | UART1 data receiver input pin. |
| | | 109 | PH.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | SC2_nCD | I | MFP4 | Smart Card 2 card detect pin. |
| | | | I2S0_LRCK | O | MFP5 | I2S0 left right channel clock output pin. |
| | | | SPI1_I2SMCLK | I/O | MFP6 | SPI1 I2S master clock output pin |
| | | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | | UART0_TXD | O | MFP8 | UART0 data transmitter output pin. |
| | | 110 | PH.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | | UART0_RXD | I | MFP8 | UART0 data receiver input pin. |
| | | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | | 111 | PD.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | SPI3_I2SMCLK | I/O | MFP3 | SPI3 I2S master clock output pin |
| | | | SC1_nCD | I | MFP4 | Smart Card 1 card detect pin. |
| | | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| 49 | 49 | 112 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| 50 | 50 | 113 | LDO_CAP | A | MFP0 | LDO output pin. |
| 51 | 51 | 114 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 52 | 52 | 115 | PC.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC1_nCD | I | MFP3 | Smart Card 1 card detect pin. |
| | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | USCI0_CTL0 | I/O | MFP5 | USCI0 control 0 pin. |
| | | | QSPI0_CLK | I/O | MFP6 | Quad SPI0 serial clock pin. |
| | | | EPWM0_SYNC_IN | I | MFP11 | EPWM0 counter synchronous trigger input pin. |
| | | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | | | HSUSB_VBUS_ST | I | MFP15 | HSUSB external VBUS regulator status pin. |
| 53 | 53 | 116 | PB.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH15 | A | MFP1 | EADC0 channel 15 analog input. |
| | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | SC1_PWR | O | MFP3 | Smart Card 1 power pin. |
| | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | USCI0_CTL1 | I/O | MFP5 | USCI0 control 1 pin. |
| | | | UART0_nCTS | I | MFP6 | UART0 clear to Send input pin. |
| | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | I2C2_SMBAL | O | MFP8 | I2C2 SMBus SMBALTER pin |
| | | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | | | HSUSB_VBUS_EN | O | MFP15 | HSUSB external VBUS regulator enable pin. |
| 54 | 54 | 117 | PB.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH14 | A | MFP1 | EADC0 channel 14 analog input. |
| | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | SC1_RST | O | MFP3 | Smart Card 1 reset pin. |
| | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | USCI0_DAT1 | I/O | MFP5 | USCI0 data 1 pin. |
| | | | UART0_nRTS | O | MFP6 | UART0 request to Send output pin. |
| | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | I2C2_SMBSUS | O | MFP8 | I2C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | CLKO | O | MFP14 | Clock Out |
| 55 | 55 | 118 | PB.13 | I/O | MFP0 | General purpose digital I/O pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EADC0_CH13 | A | MFP1 | EADC0 channel 13 analog input. |
| | | | DAC1_OUT | A | MFP1 | DAC1 channel analog output. |
| | | | ACMP0_P3 | A | MFP1 | Analog comparator 0 positive input 3 pin. |
| | | | ACMP1_P3 | A | MFP1 | Analog comparator 1 positive input 3 pin. |
| | | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | | SC1_DAT | I/O | MFP3 | Smart Card 1 data pin. |
| | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | USCI0_DAT0 | I/O | MFP5 | USCI0 data 0 pin. |
| | | | UART0_TXD | O | MFP6 | UART0 data transmitter output pin. |
| | | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | | I2C2_SCL | I/O | MFP8 | I2C2 clock pin. |
| | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| 56 | 56 | 119 | PB.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH12 | A | MFP1 | EADC0 channel 12 analog input. |
| | | | DAC0_OUT | A | MFP1 | DAC0 channel analog output. |
| | | | ACMP0_P2 | A | MFP1 | Analog comparator 0 positive input 2 pin. |
| | | | ACMP1_P2 | A | MFP1 | Analog comparator 1 positive input 2 pin. |
| | | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | | | SC1_CLK | O | MFP3 | Smart Card 1 clock pin. |
| | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | USCI0_CLK | I/O | MFP5 | USCI0 clock pin. |
| | | | UART0_RXD | I | MFP6 | UART0 data receiver input pin. |
| | | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | | I2C2_SDA | I/O | MFP8 | I2C2 data input/output pin. |
| | | | SD0_nCD | I | MFP9 | SD/SDIO0 card detect input pin |
| | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| 57 | 57 | 120 | $AV_{DD}$ | P | MFP0 | Power supply for internal analog circuit. |
| 58 | 58 | 121 | $V_{REF}$ | A | MFP0 | ADC reference voltage input.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| 59 | 59 | 122 | $AV_{SS}$ | P | MFP0 | Ground pin for analog circuit. |
| 60 | 60 | 123 | PB.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH11 | A | MFP1 | EADC0 channel 11 analog input. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | UART0_nCTS | I | MFP5 | UART0 clear to Send input pin. |
| | | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP7 | I2C1 clock pin. |
| | | | SPI0_I2SMCLK | I/O | MFP9 | SPI0 I2S master clock output pin |
| | | | BPWM1_CH0 | I/O | MFP10 | BPWM1 channel 0 output/capture input. |
| | | | SPI3_CLK | I/O | MFP11 | SPI3 serial clock pin. |
| | | | HSUSB_VBUS_ST | I | MFP14 | HSUSB external VBUS regulator status pin. |
| 61 | 61 | 124 | PB.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH10 | A | MFP1 | EADC0 channel 10 analog input. |
| | | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | | USCI1_CTL0 | I/O | MFP4 | USCI1 control 0 pin. |
| | | | UART0_nRTS | O | MFP5 | UART0 request to Send output pin. |
| | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP7 | I2C1 data input/output pin. |
| | | | BPWM1_CH1 | I/O | MFP10 | BPWM1 channel 1 output/capture input. |
| | | | SPI3_SS | I/O | MFP11 | SPI3 slave select pin. |
| | | | HSUSB_VBUS_EN | O | MFP14 | HSUSB external VBUS regulator enable pin. |
| 62 | 62 | 125 | PB.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH9 | A | MFP1 | EADC0 channel 9 analog input. |
| | | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | | USCI1_CTL1 | I/O | MFP4 | USCI1 control 1 pin. |
| | | | UART0_TXD | O | MFP5 | UART0 data transmitter output pin. |
| | | | UART1_nCTS | I | MFP6 | UART1 clear to Send input pin. |
| | | | I2C1_SMBAL | O | MFP7 | I2C1 SMBus SMBALTER pin |
| | | | BPWM1_CH2 | I/O | MFP10 | BPWM1 channel 2 output/capture input. |
| | | | SPI3_MISO | I/O | MFP11 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | INT7 | I | MFP13 | External interrupt 7 input pin. |
| 63 | 63 | 126 | PB.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH8 | A | MFP1 | EADC0 channel 8 analog input. |
| | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | | USCI1_CLK | I/O | MFP4 | USCI1 clock pin. |
| | | | UART0_RXD | I | MFP5 | UART0 data receiver input pin. |
| | | | UART1_nRTS | O | MFP6 | UART1 request to Send output pin. |

| 64 Pin | 64 Pin 2 USB | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | I2C1_SMBSUS | O | MFP7 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | BPWM1_CH3 | I/O | MFP10 | BPWM1 channel 3 output/capture input. |
| | | | SPI3_MOSI | I/O | MFP11 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | INT6 | I | MFP13 | External interrupt 6 input pin. |
| 64 | 64 | 127 | PB.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH7 | A | MFP1 | EADC0 channel 7 analog input. |
| | | | EBI_nWRL | O | MFP2 | EBI low byte write enable output pin. |
| | | | USCI1_DAT0 | I/O | MFP4 | USCI1 data 0 pin. |
| | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | SD1_CMD | I/O | MFP7 | SD/SDIO1 command/response pin |
| | | | EBI_nCS0 | O | MFP8 | EBI chip select 0 output pin. |
| | | | BPWM1_CH4 | I/O | MFP10 | BPWM1 channel 4 output/capture input. |
| | | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | INT5 | I | MFP13 | External interrupt 5 input pin. |
| | | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | | | ACMP0_O | O | MFP15 | Analog comparator 0 output pin. |
| 1 | 1 | 128 | PB.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH6 | A | MFP1 | EADC0 channel 6 analog input. |
| | | | EBI_nWRH | O | MFP2 | EBI high byte write enable output pin |
| | | | USCI1_DAT1 | I/O | MFP4 | USCI1 data 1 pin. |
| | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | SD1_CLK | O | MFP7 | SD/SDIO1 clock output pin |
| | | | EBI_nCS1 | O | MFP8 | EBI chip select 1 output pin. |
| | | | BPWM1_CH5 | I/O | MFP10 | BPWM1 channel 5 output/capture input. |
| | | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | INT4 | I | MFP13 | External interrupt 4 input pin. |
| | | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | | | ACMP1_O | O | MFP15 | Analog comparator 1 output pin. |

### 4.2.5 M485 Series Pin Description

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 2 | 1 | PB.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH5 | A | MFP1 | EADC0 channel 5 analog input. |
| | | | | ACMP1_N | A | MFP1 | Analog comparator 1 negative input pin. |
| | | | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | | | SPI1_MISO | I/O | MFP5 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | | I2C0_SCL | I/O | MFP6 | I2C0 clock pin. |
| | | | | UART5_TXD | O | MFP7 | UART5 data transmitter output pin. |
| | | | | USCI1_CTL0 | I/O | MFP8 | USCI1 control 0 pin. |
| | | | | SC0_CLK | O | MFP9 | Smart Card 0 clock pin. |
| | | | | I2S0_BCLK | O | MFP10 | I2S0 bit clock output pin. |
| | | | | EPWM0_CH0 | I/O | MFP11 | EPWM0 channel 0 output/capture input. |
| | | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| 2 | 2 | 3 | 2 | PB.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH4 | A | MFP1 | EADC0 channel 4 analog input. |
| | | | | ACMP1_P1 | A | MFP1 | Analog comparator 1 positive input 1 pin. |
| | | | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | | | SPI1_MOSI | I/O | MFP5 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | | I2C0_SDA | I/O | MFP6 | I2C0 data input/output pin. |
| | | | | UART5_RXD | I | MFP7 | UART5 data receiver input pin. |
| | | | | USCI1_CTL1 | I/O | MFP8 | USCI1 control 1 pin. |
| | | | | SC0_DAT | I/O | MFP9 | Smart Card 0 data pin. |
| | | | | I2S0_MCLK | O | MFP10 | I2S0 master clock output pin. |
| | | | | EPWM0_CH1 | I/O | MFP11 | EPWM0 channel 1 output/capture input. |
| | | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| 3 | 3 | 4 | 3 | PB.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH3 | A | MFP1 | EADC0 channel 3 analog input. |
| | | | | ACMP0_N | A | MFP1 | Analog comparator 0 negative input pin. |
| | | | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI1_CLK | I/O | MFP5 | SPI1 serial clock pin. |
| | | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | | UART5_nRTS | O | MFP7 | UART5 request to Send output pin. |
| | | | | USCI1_DAT1 | I/O | MFP8 | USCI1 data 1 pin. |
| | | | | SC0_RST | O | MFP9 | Smart Card 0 reset pin. |
| | | | | I2S0_DI | I | MFP10 | I2S0 data input pin. |
| | | | | EPWM0_CH2 | I/O | MFP11 | EPWM0 channel 2 output/capture input. |
| | | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| 4 | 4 | 5 | 4 | PB.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH2 | A | MFP1 | EADC0 channel 2 analog input. |
| | | | | ACMP0_P1 | A | MFP1 | Analog comparator 0 positive input 1 pin. |
| | | | | OPA0_O | A | MFP1 | Operational amplifier 0 output pin. |
| | | | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | | | SPI1_SS | I/O | MFP5 | SPI1 slave select pin. |
| | | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | | UART5_nCTS | I | MFP7 | UART5 clear to Send input pin. |
| | | | | USCI1_DAT0 | I/O | MFP8 | USCI1 data 0 pin. |
| | | | | SC0_PWR | O | MFP9 | Smart Card 0 power pin. |
| | | | | I2S0_DO | O | MFP10 | I2S0 data output pin. |
| | | | | EPWM0_CH3 | I/O | MFP11 | EPWM0 channel 3 output/capture input. |
| | | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| | | | 5 | PC.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR4 | O | MFP2 | EBI address bus bit 4. |
| | | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | | SPI3_MISO | I/O | MFP6 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | | SC0_nCD | I | MFP9 | Smart Card 0 card detect pin. |
| | | | | ECAP1_IC2 | I | MFP11 | Enhanced capture unit 1 input 2 pin. |
| | | | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| | | | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| | | | 6 | PC.11 | I/O | MFP0 | General purpose digital I/O pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | EBI_ADR5 | O | MFP2 | EBI address bus bit 5. |
| | | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | | SPI3_MOSI | I/O | MFP6 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | | ECAP1_IC1 | I | MFP11 | Enhanced capture unit 1 input 1 pin. |
| | | | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| | | | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | | | 7 | PC.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR6 | O | MFP2 | EBI address bus bit 6. |
| | | | | SPI3_CLK | I/O | MFP6 | SPI3 serial clock pin. |
| | | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | | | | ECAP1_IC0 | I | MFP11 | Enhanced capture unit 1 input 0 pin. |
| | | | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| | | | 8 | PC.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR7 | O | MFP2 | EBI address bus bit 7. |
| | | | | SPI3_SS | I/O | MFP6 | SPI3 slave select pin. |
| | | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | | | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 5 | 5 | 6 | 9 | PB.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH1 | A | MFP1 | EADC0 channel 1 analog input. |
| | | | | OPA0_N | A | MFP1 | Operational amplifier 0 negative input pin. |
| | | | | EBI_ADR8 | O | MFP2 | EBI address bus bit 8. |
| | | | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | | | SPI3_I2SMCLK | I/O | MFP6 | SPI3 I2S master clock output pin |
| | | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | | USCI1_CLK | I/O | MFP8 | USCI1 clock pin. |
| | | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | | I2S0_LRCK | O | MFP10 | I2S0 left right channel clock output pin. |
| | | | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| | | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | | EPWM0_BRAKE0 | I | MFP13 | EPWM0 Brake 0 input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| 6 | 6 | 7 | 10 | PB.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH0 | A | MFP1 | EADC0 channel 0 analog input. |
| | | | | OPA0_P | A | MFP1 | Operational amplifier 0 positive input pin. |
| | | | | EBI_ADR9 | O | MFP2 | EBI address bus bit 9. |
| | | | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | | SPI0_I2SMCLK | I/O | MFP8 | SPI0 I2S master clock output pin |
| | | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | | EPWM0_BRAKE1 | I | MFP13 | EPWM0 Brake 1 input pin. |
| | | | 11 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | | 12 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 7 | 8 | 13 | PA.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | ACMP0_P0 | A | MFP1 | Analog comparator 0 positive input 0 pin. |
| | | | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | | | SC2_PWR | O | MFP3 | Smart Card 2 power pin. |
| | | | | SPI2_SS | I/O | MFP4 | SPI2 slave select pin. |
| | | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | | USCI0_CLK | I/O | MFP6 | USCI0 clock pin. |
| | | | | I2C2_SCL | I/O | MFP7 | I2C2 clock pin. |
| | | | | BPWM0_CH0 | I/O | MFP9 | BPWM0 channel 0 output/capture input. |
| | | | | EPWM0_SYNC_OUT | O | MFP10 | EPWM0 counter synchronous trigger output pin. |
| | | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | | | DAC1_ST | I | MFP14 | DAC1 external trigger input. |
| | 8 | 9 | 14 | PA.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | ACMP1_P0 | A | MFP1 | Analog comparator 1 positive input 0 pin. |
| | | | | OPA1_O | A | MFP1 | Operational amplifier 1 output pin. |
| | | | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | | | SC2_RST | O | MFP3 | Smart Card 2 reset pin. |
| | | | | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| | | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | | | USCI0_DAT0 | I/O | MFP6 | USCI0 data 0 pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | I2C2_SDA | I/O | MFP7 | I2C2 data input/output pin. |
| | | | | BPWM0_CH1 | I/O | MFP9 | BPWM0 channel 1 output/capture input. |
| | | | | QEI1_INDEX | I | MFP10 | Quadrature encoder 1 index input |
| | | | | ECAP0_IC0 | I | MFP11 | Enhanced capture unit 0 input 0 pin. |
| | | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | | DAC0_ST | I | MFP14 | DAC0 external trigger input. |
| | 9 | 10 | 15 | PA.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA1_N | A | MFP1 | Operational amplifier 1 negative input pin. |
| | | | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | | | SC2_DAT | I/O | MFP3 | Smart Card 2 data pin. |
| | | | | SPI2_MISO | I/O | MFP4 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | | | USCI0_DAT1 | I/O | MFP6 | USCI0 data 1 pin. |
| | | | | UART1_TXD | O | MFP7 | UART1 data transmitter output pin. |
| | | | | BPWM0_CH2 | I/O | MFP9 | BPWM0 channel 2 output/capture input. |
| | | | | QEI1_A | I | MFP10 | Quadrature encoder 1 phase A input |
| | | | | ECAP0_IC1 | I | MFP11 | Enhanced capture unit 0 input 1 pin. |
| | | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| | 10 | 11 | 16 | PA.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA1_P | A | MFP1 | Operational amplifier 1 positive input pin. |
| | | | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | | | SC2_CLK | O | MFP3 | Smart Card 2 clock pin. |
| | | | | SPI2_MOSI | I/O | MFP4 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | | | USCI0_CTL1 | I/O | MFP6 | USCI0 control 1 pin. |
| | | | | UART1_RXD | I | MFP7 | UART1 data receiver input pin. |
| | | | | BPWM0_CH3 | I/O | MFP9 | BPWM0 channel 3 output/capture input. |
| | | | | QEI1_B | I | MFP10 | Quadrature encoder 1 phase B input |
| | | | | ECAP0_IC2 | I | MFP11 | Enhanced capture unit 0 input 2 pin. |
| | | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| | | | | INT4 | I | MFP15 | External interrupt 4 input pin. |
| | | | 17 | PC.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | | | SC2_nCD | I | MFP3 | Smart Card 2 card detect pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI2_I2SMCLK | I/O | MFP4 | SPI2 I2S master clock output pin |
| | | | | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | | | | USCI0_CTL0 | I/O | MFP6 | USCI0 control 0 pin. |
| | | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | | BPWM0_CH4 | I/O | MFP9 | BPWM0 channel 4 output/capture input. |
| | | | | CLKO | O | MFP13 | Clock Out |
| | | | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | | | 18 | PD.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA2_O | A | MFP1 | Operational amplifier 2 output pin. |
| | | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | | BPWM0_CH5 | I/O | MFP9 | BPWM0 channel 5 output/capture input. |
| | | | | QEI0_INDEX | I | MFP10 | Quadrature encoder 0 index input |
| | | | | CLKO | O | MFP13 | Clock Out |
| | | | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | | | | INT5 | I | MFP15 | External interrupt 5 input pin. |
| | | | 19 | PD.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA2_N | A | MFP1 | Operational amplifier 2 negative input pin. |
| | | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | | UART1_TXD | O | MFP3 | UART1 data transmitter output pin. |
| | | | | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | | | | QEI0_A | I | MFP10 | Quadrature encoder 0 phase A input |
| | | | | INT6 | I | MFP15 | External interrupt 6 input pin. |
| | | | 20 | PD.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | OPA2_P | A | MFP1 | Operational amplifier 2 positive input pin. |
| | | | | EBI_nCS2 | O | MFP2 | EBI chip select 2 output pin. |
| | | | | UART1_RXD | I | MFP3 | UART1 data receiver input pin. |
| | | | | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |
| | | | | QEI0_B | I | MFP10 | Quadrature encoder 0 phase B input |
| | | | | INT7 | I | MFP15 | External interrupt 7 input pin. |
| | | | 21 | PG.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | | | SPI2_SS | I/O | MFP3 | SPI2 slave select pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | I2C0_SMBAL | O | MFP4 | I2C0 SMBus SMBALTER pin |
| | | | | I2C1_SCL | I/O | MFP5 | I2C1 clock pin. |
| | | | | TM0 | I/O | MFP13 | Timer0 event counter input/toggle output pin. |
| | | | 22 | PG.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | | | SPI2_CLK | I/O | MFP3 | SPI2 serial clock pin. |
| | | | | I2C0_SMBSUS | O | MFP4 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | I2C1_SDA | I/O | MFP5 | I2C1 data input/output pin. |
| | | | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | | | 23 | PG.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | | | | SPI2_MISO | I/O | MFP3 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | | TM2 | I/O | MFP13 | Timer2 event counter input/toggle output pin. |
| | | | 24 | PF.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | | | | SPI2_MOSI | I/O | MFP3 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | | TAMPER5 | I/O | MFP10 | TAMPER detector loop pin 5. |
| | | | | TM3 | I/O | MFP13 | Timer3 event counter input/toggle output pin. |
| | | | 25 | PF.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | | | SC0_nCD | I | MFP3 | Smart Card 0 card detect pin. |
| | | | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |
| | | | | SPI0_I2SMCLK | I/O | MFP5 | SPI0 I2S master clock output pin |
| | | | | TAMPER4 | I/O | MFP10 | TAMPER detector loop pin 4. |
| | | | 26 | PF.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | | SC0_PWR | O | MFP3 | Smart Card 0 power pin. |
| | | | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |
| | | | | SPI0_SS | I/O | MFP5 | SPI0 slave select pin. |
| | | | | TAMPER3 | I/O | MFP10 | TAMPER detector loop pin 3. |
| | | | 27 | PF.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | | | SC0_RST | O | MFP3 | Smart Card 0 reset pin. |
| | | | | I2S0_DI | I | MFP4 | I2S0 data input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI0_CLK | I/O | MFP5 | SPI0 serial clock pin. |
| | | | | TAMPER2 | I/O | MFP10 | TAMPER detector loop pin 2. |
| | | | 28 | PF.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | | | SC0_DAT | I/O | MFP3 | Smart Card 0 data pin. |
| | | | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | | | SPI0_MISO | I/O | MFP5 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | | | TAMPER1 | I/O | MFP10 | TAMPER detector loop pin 1. |
| | | 12 | 29 | PF.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | | | SC0_CLK | O | MFP3 | Smart Card 0 clock pin. |
| | | | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | | | SPI0_MOSI | I/O | MFP5 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | | EBI_nCS0 | O | MFP7 | EBI chip select 0 output pin. |
| | | | | TAMPER0 | I/O | MFP10 | TAMPER detector loop pin 0. |
| | | 13 | 30 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 7 | 11 | 14 | 31 | PF.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | UART2_RXD | I | MFP2 | UART2 data receiver input pin. |
| | | | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | | | | BPWM0_CH4 | I/O | MFP8 | BPWM0 channel 4 output/capture input. |
| | | | | EPWM0_SYNC_OUT | O | MFP9 | EPWM0 counter synchronous trigger output pin. |
| | | | | X32_IN | I | MFP10 | External 32.768 kHz crystal input pin. |
| | | | | EADC0_ST | I | MFP11 | EADC0 external trigger input. |
| 8 | 12 | 15 | 32 | PF.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | UART2_TXD | O | MFP2 | UART2 data transmitter output pin. |
| | | | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| | | | | BPWM0_CH5 | I/O | MFP8 | BPWM0 channel 5 output/capture input. |
| | | | | X32_OUT | O | MFP10 | External 32.768 kHz crystal output pin. |
| | | | 33 | PH.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | | | SPI1_MISO | I/O | MFP3 | SPI1 MISO (Master In, Slave Out) pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | 34 | PH.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | | | SPI1_MOSI | I/O | MFP3 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | 35 | PH.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | | | SPI1_CLK | I/O | MFP3 | SPI1 serial clock pin. |
| | | | 36 | PH.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | | | SPI1_SS | I/O | MFP3 | SPI1 slave select pin. |
| 9 | 13 | 16 | 37 | PF.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | | XT1_IN | I | MFP10 | External 4~24 MHz (high speed) crystal input pin. |
| | | | | BPWM1_CH0 | I/O | MFP11 | BPWM1 channel 0 output/capture input. |
| 10 | 14 | 17 | 38 | PF.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | | QSPI0_CLK | I/O | MFP5 | Quad SPI0 serial clock pin. |
| | | | | XT1_OUT | O | MFP10 | External 4~24 MHz (high speed) crystal output pin. |
| | | | | BPWM1_CH1 | I/O | MFP11 | BPWM1 channel 1 output/capture input. |
| | | | 39 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | | 40 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | | 41 | PE.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |
| | | | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | | | USCI1_CTL1 | I/O | MFP6 | USCI1 control 1 pin. |
| | | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | | EPWM0_CH0 | I/O | MFP10 | EPWM0 channel 0 output/capture input. |
| | | | | EPWM0_BRAKE0 | I | MFP11 | EPWM0 Brake 0 input pin. |
| | | | | ECAP0_IC0 | I | MFP12 | Enhanced capture unit 0 input 0 pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | TRACE_CLK | O | MFP14 | ETM Trace Clock output pin |
| | | | 42 | PE.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |
| | | | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |
| | | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | | EPWM0_CH1 | I/O | MFP10 | EPWM0 channel 1 output/capture input. |
| | | | | EPWM0_BRAKE1 | I | MFP11 | EPWM0 Brake 1 input pin. |
| | | | | ECAP0_IC1 | I | MFP12 | Enhanced capture unit 0 input 1 pin. |
| | | | | TRACE_DATA0 | O | MFP14 | ETM Trace Data 0 output pin |
| | | | 43 | PE.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | | | I2S0_DI | I | MFP4 | I2S0 data input pin. |
| | | | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | | USCI1_DAT0 | I/O | MFP6 | USCI1 data 0 pin. |
| | | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | | EPWM0_CH2 | I/O | MFP10 | EPWM0 channel 2 output/capture input. |
| | | | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | | | ECAP0_IC2 | I | MFP12 | Enhanced capture unit 0 input 2 pin. |
| | | | | TRACE_DATA1 | O | MFP14 | ETM Trace Data 1 output pin |
| | | | 44 | PE.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | | | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | | | USCI1_DAT1 | I/O | MFP6 | USCI1 data 1 pin. |
| | | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | | | EPWM0_CH3 | I/O | MFP10 | EPWM0 channel 3 output/capture input. |
| | | | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | | | ECAP1_IC2 | I | MFP13 | Enhanced capture unit 1 input 2 pin. |
| | | | | TRACE_DATA2 | O | MFP14 | ETM Trace Data 2 output pin |
| | | | 45 | PE.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | | | SPI2_I2SMCLK | I/O | MFP5 | SPI2 I2S master clock output pin |
| | | | | USCI1_CLK | I/O | MFP6 | USCI1 clock pin. |
| | | | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | | | EPWM0_CH4 | I/O | MFP10 | EPWM0 channel 4 output/capture input. |
| | | | | ECAP1_IC1 | I | MFP13 | Enhanced capture unit 1 input 1 pin. |
| | | | | TRACE_DATA3 | O | MFP14 | ETM Trace Data 3 output pin |
| | | | 46 | PE.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | | UART4_nRTS | O | MFP5 | UART4 request to Send output pin. |
| | | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | | | EPWM0_CH5 | I/O | MFP10 | EPWM0 channel 5 output/capture input. |
| | | | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | | | BPWM1_CH5 | I/O | MFP12 | BPWM1 channel 5 output/capture input. |
| | | | | ECAP1_IC0 | I | MFP13 | Enhanced capture unit 1 input 0 pin. |
| | | | 47 | PC.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | | UART4_nCTS | I | MFP5 | UART4 clear to Send input pin. |
| | | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | | | BPWM1_CH4 | I/O | MFP12 | BPWM1 channel 4 output/capture input. |
| | | 18 | 48 | PC.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | | | SPI1_MISO | I/O | MFP4 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | | UART4_TXD | O | MFP5 | UART4 data transmitter output pin. |
| | | | | SC2_PWR | O | MFP6 | Smart Card 2 power pin. |
| | | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | | INT3 | I | MFP15 | External interrupt 3 input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | 19 | 49 | PC.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | | | SPI1_MOSI | I/O | MFP4 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | | UART4_RXD | I | MFP5 | UART4 data receiver input pin. |
| | | | | SC2_RST | O | MFP6 | Smart Card 2 reset pin. |
| | | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| | 15 | 20 | 50 | PA.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | | | SPI1_CLK | I/O | MFP4 | SPI1 serial clock pin. |
| | | | | SC2_DAT | I/O | MFP6 | Smart Card 2 data pin. |
| | | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | | | EPWM1_CH4 | I/O | MFP11 | EPWM1 channel 4 output/capture input. |
| | | | | BPWM1_CH2 | I/O | MFP12 | BPWM1 channel 2 output/capture input. |
| | | | | ACMP0_WLAT | I | MFP13 | Analog comparator 0 window latch input pin |
| | | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| | 16 | 21 | 51 | PA.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | | | SPI1_SS | I/O | MFP4 | SPI1 slave select pin. |
| | | | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | | | | SC2_CLK | O | MFP6 | Smart Card 2 clock pin. |
| | | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | | | EPWM1_CH5 | I/O | MFP11 | EPWM1 channel 5 output/capture input. |
| | | | | BPWM1_CH3 | I/O | MFP12 | BPWM1 channel 3 output/capture input. |
| | | | | ACMP1_WLAT | I | MFP13 | Analog comparator 1 window latch input pin |
| | | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | | INT0 | I | MFP15 | External interrupt 0 input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | 22 | 52 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | 23 | 53 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | 24 | 54 | LDO_CAP | A | MFP0 | LDO output pin. |
| | 17 | 25 | 55 | PA.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_D2 | I/O | MFP2 | SPIM data 2 pin for Quad Mode I/O. |
| | | | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | | SPI1_I2SMCLK | I/O | MFP4 | SPI1 I2S master clock output pin |
| | | | | SD1_CMD | I/O | MFP5 | SD/SDIO1 command/response pin |
| | | | | SC2_nCD | I | MFP6 | Smart Card 2 card detect pin. |
| | | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | | | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | | | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | | | | EPWM0_CH0 | I/O | MFP13 | EPWM0 channel 0 output/capture input. |
| | | | | QEI0_INDEX | I | MFP14 | Quadrature encoder 0 index input |
| | 18 | 26 | 56 | PA.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_D3 | I/O | MFP2 | SPIM data 3 pin for Quad Mode I/O. |
| | | | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | | SD1_CLK | O | MFP5 | SD/SDIO1 clock output pin |
| | | | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | | | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | | | | EPWM0_CH1 | I/O | MFP13 | EPWM0 channel 1 output/capture input. |
| | | | | QEI0_A | I | MFP14 | Quadrature encoder 0 phase A input |
| 11 | 19 | 27 | 57 | PA.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_SS | I/O | MFP2 | SPIM slave select pin. |
| | | | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | | | | EPWM0_CH2 | I/O | MFP13 | EPWM0 channel 2 output/capture input. |
| | | | | QEI0_B | I | MFP14 | Quadrature encoder 0 phase B input |
| 12 | 20 | 28 | 58 | PA.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_CLK | I/O | MFP2 | SPIM serial clock pin. |
| | | | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | | | | EPWM0_CH3 | I/O | MFP13 | EPWM0 channel 3 output/capture input. |
| 13 | 21 | 29 | 59 | PA.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_MISO | I/O | MFP2 | SPIM MISO (Master In, Slave Out) pin. |
| | | | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | | | | EPWM0_CH4 | I/O | MFP13 | EPWM0 channel 4 output/capture input. |
| | | | | DAC1_ST | I | MFP15 | DAC1 external trigger input. |
| 14 | 22 | 30 | 60 | PA.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SPIM_MOSI | I/O | MFP2 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | | | | EPWM0_CH5 | I/O | MFP13 | EPWM0 channel 5 output/capture input. |
| | | | | DAC0_ST | I | MFP15 | DAC0 external trigger input. |
| 15 | 23 | 31 | 61 | $V_{DDIO}$ | P | MFP0 | Power supply for PA.0~PA.5. |
| | | | 62 | PE.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | | | UART2_TXD | O | MFP3 | UART2 data transmitter output pin. |
| | | | | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | | | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | | | 63 | PE.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | | | UART2_RXD | I | MFP3 | UART2 data receiver input pin. |
| | | | | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |
| 16 | 24 | 32 | 64 | nRESET | I | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 17 | 25 | 33 | 65 | PF.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | UART1_TXD | O | MFP2 | UART1 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP3 | I2C1 clock pin. |
| | | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | | ICE_DAT | O | MFP14 | Serial wired debugger data pin. |
| 18 | 26 | 34 | 66 | PF.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | UART1_RXD | I | MFP2 | UART1 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP3 | I2C1 data input/output pin. |
| | | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | | ICE_CLK | I | MFP14 | Serial wired debugger clock pin. |
| | | | 67 | PD.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | | | I2C2_SCL | I/O | MFP3 | I2C2 clock pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | | | 68 | PD.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | | | I2C2_SDA | I/O | MFP3 | I2C2 data input/output pin. |
| | | | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| | 27 | 35 | 69 | PC.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | | | | SPIM_D2 | I/O | MFP3 | SPIM data 2 pin for Quad Mode I/O. |
| | | | | QSPI0_MISO1 | I/O | MFP4 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | | | | UART4_TXD | O | MFP11 | UART4 data transmitter output pin. |
| | | | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| | 28 | 36 | 70 | PC.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | | | SPIM_D3 | I/O | MFP3 | SPIM data 3 pin for Quad Mode I/O. |
| | | | | QSPI0_MOSI1 | I/O | MFP4 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | | SC1_nCD | I | MFP5 | Smart Card 1 card detect pin. |
| | | | | I2S0_BCLK | O | MFP6 | I2S0 bit clock output pin. |
| | | | | SPI1_I2SMCLK | I/O | MFP7 | SPI1 I2S master clock output pin |
| | | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | | | | UART4_RXD | I | MFP11 | UART4 data receiver input pin. |
| | | | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| | 29 | 37 | 71 | PC.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | | | SPIM_SS | I/O | MFP3 | SPIM slave select pin. |
| | | | | QSPI0_SS | I/O | MFP4 | Quad SPI0 slave select pin. |
| | | | | SC1_PWR | O | MFP5 | Smart Card 1 power pin. |
| | | | | I2S0_MCLK | O | MFP6 | I2S0 master clock output pin. |
| | | | | SPI1_MISO | I/O | MFP7 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | | UART2_nRTS | O | MFP8 | UART2 request to Send output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | I2C0_SMBAL | O | MFP9 | I2C0 SMBus SMBALTER pin |
| | | | | CAN1_TXD | O | MFP10 | CAN1 bus transmitter output. |
| | | | | UART3_TXD | O | MFP11 | UART3 data transmitter output pin. |
| | | | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| | 30 | 38 | 72 | PC.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | | | SPIM_CLK | I/O | MFP3 | SPIM serial clock pin. |
| | | | | QSPI0_CLK | I/O | MFP4 | Quad SPI0 serial clock pin. |
| | | | | SC1_RST | O | MFP5 | Smart Card 1 reset pin. |
| | | | | I2S0_DI | I | MFP6 | I2S0 data input pin. |
| | | | | SPI1_MOSI | I/O | MFP7 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | | UART2_nCTS | I | MFP8 | UART2 clear to Send input pin. |
| | | | | I2C0_SMBSUS | O | MFP9 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | CAN1_RXD | I | MFP10 | CAN1 bus receiver input. |
| | | | | UART3_RXD | I | MFP11 | UART3 data receiver input pin. |
| | | | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 19 | 31 | 39 | 73 | PC.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | | | SPIM_MISO | I/O | MFP3 | SPIM MISO (Master In, Slave Out) pin. |
| | | | | QSPI0_MISO0 | I/O | MFP4 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | | SC1_DAT | I/O | MFP5 | Smart Card 1 data pin. |
| | | | | I2S0_DO | O | MFP6 | I2S0 data output pin. |
| | | | | SPI1_CLK | I/O | MFP7 | SPI1 serial clock pin. |
| | | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| 20 | 32 | 40 | 74 | PC.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | | | SPIM_MOSI | I/O | MFP3 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | | QSPI0_MOSI0 | I/O | MFP4 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | | SC1_CLK | O | MFP5 | Smart Card 1 clock pin. |
| | | | | I2S0_LRCK | O | MFP6 | I2S0 left right channel clock output pin. |
| | | | | SPI1_SS | I/O | MFP7 | SPI1 slave select pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | | | 75 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | | 76 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | | 77 | PG.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | | | SD1_DAT3 | I/O | MFP3 | SD/SDIO1 data line bit 3. |
| | | | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | | | 78 | PG.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | | | SD1_DAT2 | I/O | MFP3 | SD/SDIO1 data line bit 2. |
| | | | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | | | 79 | PG.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | | | SD1_DAT1 | I/O | MFP3 | SD/SDIO1 data line bit 1. |
| | | | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | | | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | | | 80 | PG.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | | | SD1_DAT0 | I/O | MFP3 | SD/SDIO1 data line bit 0. |
| | | | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | | | 81 | PG.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | | | SD1_CMD | I/O | MFP3 | SD/SDIO1 command/response pin |
| | | | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | | | 82 | PG.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SD1_CLK | O | MFP3 | SD/SDIO1 clock output pin |
| | | | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | | | 83 | PG.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SD1_nCD | I | MFP3 | SD/SDIO1 card detect input pin |
| | | | | CLKO | O | MFP14 | Clock Out |
| | | | | EADC0_ST | I | MFP15 | EADC0 external trigger input. |
| | | | 84 | PD.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | | SD0_nCD | I | MFP3 | SD/SDIO0 card detect input pin |
| | | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | | | SC2_nCD | I | MFP7 | Smart Card 2 card detect pin. |
| 21 | 33 | | 85 | PA.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | I2S0_BCLK | O | MFP2 | I2S0 bit clock output pin. |
| | | | | UART4_TXD | O | MFP3 | UART4 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP4 | I2C1 clock pin. |
| | | | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | | | CAN0_TXD | O | MFP6 | CAN0 bus transmitter output. |
| | | | | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | | | | BPWM1_CH2 | I/O | MFP11 | BPWM1 channel 2 output/capture input. |
| | | | | QEI1_INDEX | I | MFP12 | Quadrature encoder 1 index input |
| | | | | USB_VBUS | P | MFP14 | Power supply from USB host or HUB. |
| 22 | 34 | | 86 | PA.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | I2S0_MCLK | O | MFP2 | I2S0 master clock output pin. |
| | | | | UART4_RXD | I | MFP3 | UART4 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP4 | I2C1 data input/output pin. |
| | | | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | | | CAN0_RXD | I | MFP6 | CAN0 bus receiver input. |
| | | | | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | | | | BPWM1_CH3 | I/O | MFP11 | BPWM1 channel 3 output/capture input. |
| | | | | QEI1_A | I | MFP12 | Quadrature encoder 1 phase A input |
| | | | | USB_D- | A | MFP14 | USB differential signal D-. |
| 23 | 35 | | 87 | PA.14 | I/O | MFP0 | General purpose digital I/O pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | I2S0_DI | I | MFP2 | I2S0 data input pin. |
| | | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | | I2C2_SCL | I/O | MFP6 | I2C2 clock pin. |
| | | | | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | | | | BPWM1_CH4 | I/O | MFP11 | BPWM1 channel 4 output/capture input. |
| | | | | QEI1_B | I | MFP12 | Quadrature encoder 1 phase B input |
| | | | | USB_D+ | A | MFP14 | USB differential signal D+. |
| 24 | 36 | | 88 | PA.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | I2S0_DO | O | MFP2 | I2S0 data output pin. |
| | | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | | I2C2_SDA | I/O | MFP6 | I2C2 data input/output pin. |
| | | | | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | | | | BPWM1_CH5 | I/O | MFP11 | BPWM1 channel 5 output/capture input. |
| | | | | EPWM0_SYNC_IN | I | MFP12 | EPWM0 counter synchronous trigger input pin. |
| | | | | USB_OTG_ID | I | MFP14 | USB_ identification. |
| | | 41 | 89 | HSUSB_VRES | A | MFP0 | HSUSB module reference resister |
| | | 42 | 90 | HSUSB_VDD33 | P | MFP0 | Power supply for HSUSB VDD33 |
| | | 43 | 91 | HSUSB_VBUS | P | MFP0 | HSUSB Power supply from USB host or HUB. |
| | | 44 | 92 | HSUSB_D- | A | MFP0 | HSUSB differential signal D-. |
| | | 45 | 93 | HSUSB_VSS | P | MFP0 | Ground pin for HSUSB. |
| | | 46 | 94 | HSUSB_D+ | A | MFP0 | HSUSB differential signal D+. |
| | | 47 | 95 | HSUSB_VDD12_CAP | A | MFP0 | HSUSB Internal power regulator output 1.2V decoupling pin.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| | | 48 | 96 | HSUSB_ID | I | MFP0 | HSUSB identification. |
| | | | 97 | PE.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | | | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | | | | QEI1_INDEX | I | MFP11 | Quadrature encoder 1 index input |
| | | | | EPWM0_CH0 | I/O | MFP12 | EPWM0 channel 0 output/capture input. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | BPWM0_CH5 | I/O | MFP13 | BPWM0 channel 5 output/capture input. |
| | | | 98 | PE.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | | | SPI3_I2SMCLK | I/O | MFP5 | SPI3 I2S master clock output pin |
| | | | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | | | USCI0_CTL0 | I/O | MFP7 | USCI0 control 0 pin. |
| | | | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | | | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | | | | QEI1_A | I | MFP11 | Quadrature encoder 1 phase A input |
| | | | | EPWM0_CH1 | I/O | MFP12 | EPWM0 channel 1 output/capture input. |
| | | | | BPWM0_CH4 | I/O | MFP13 | BPWM0 channel 4 output/capture input. |
| | | | 99 | PE.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | | | | SPI3_SS | I/O | MFP5 | SPI3 slave select pin. |
| | | | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | | | USCI0_CTL1 | I/O | MFP7 | USCI0 control 1 pin. |
| | | | | QEI1_B | I | MFP11 | Quadrature encoder 1 phase B input |
| | | | | EPWM0_CH2 | I/O | MFP12 | EPWM0 channel 2 output/capture input. |
| | | | | BPWM0_CH3 | I/O | MFP13 | BPWM0 channel 3 output/capture input. |
| | | | 100 | PE.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | | | SPI3_CLK | I/O | MFP5 | SPI3 serial clock pin. |
| | | | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | | | USCI0_DAT1 | I/O | MFP7 | USCI0 data 1 pin. |
| | | | | QEI0_INDEX | I | MFP11 | Quadrature encoder 0 index input |
| | | | | EPWM0_CH3 | I/O | MFP12 | EPWM0 channel 3 output/capture input. |
| | | | | BPWM0_CH2 | I/O | MFP13 | BPWM0 channel 2 output/capture input. |
| | | | 101 | PE.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | | | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | | | SPI3_MISO | I/O | MFP5 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | | | USCI0_DAT0 | I/O | MFP7 | USCI0 data 0 pin. |
| | | | | QEI0_A | I | MFP11 | Quadrature encoder 0 phase A input |
| | | | | EPWM0_CH4 | I/O | MFP12 | EPWM0 channel 4 output/capture input. |
| | | | | BPWM0_CH1 | I/O | MFP13 | BPWM0 channel 1 output/capture input. |
| | | | 102 | PE.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | | SPI3_MOSI | I/O | MFP5 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | | | USCI0_CLK | I/O | MFP7 | USCI0 clock pin. |
| | | | | QEI0_B | I | MFP11 | Quadrature encoder 0 phase B input |
| | | | | EPWM0_CH5 | I/O | MFP12 | EPWM0 channel 5 output/capture input. |
| | | | | BPWM0_CH0 | I/O | MFP13 | BPWM0 channel 0 output/capture input. |
| | | | 103 | VSS | P | MFP0 | Ground pin for digital circuit. |
| | | | 104 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | | 105 | PE.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | | SC2_DAT | I/O | MFP4 | Smart Card 2 data pin. |
| | | | | I2S0_BCLK | O | MFP5 | I2S0 bit clock output pin. |
| | | | | SPI1_MISO | I/O | MFP6 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | | | UART4_nCTS | I | MFP9 | UART4 clear to Send input pin. |
| | | | 106 | PE.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | | SC2_CLK | O | MFP4 | Smart Card 2 clock pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | I2S0_MCLK | O | MFP5 | I2S0 master clock output pin. |
| | | | | SPI1_MOSI | I/O | MFP6 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | | | UART4_nRTS | O | MFP9 | UART4 request to Send output pin. |
| | | | 107 | PH.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | | | SC2_PWR | O | MFP4 | Smart Card 2 power pin. |
| | | | | I2S0_DI | I | MFP5 | I2S0 data input pin. |
| | | | | SPI1_CLK | I/O | MFP6 | SPI1 serial clock pin. |
| | | | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | | | UART1_TXD | O | MFP10 | UART1 data transmitter output pin. |
| | | | 108 | PH.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | | | SC2_RST | O | MFP4 | Smart Card 2 reset pin. |
| | | | | I2S0_DO | O | MFP5 | I2S0 data output pin. |
| | | | | SPI1_SS | I/O | MFP6 | SPI1 slave select pin. |
| | | | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | | | UART1_RXD | I | MFP10 | UART1 data receiver input pin. |
| | | | 109 | PH.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | | SC2_nCD | I | MFP4 | Smart Card 2 card detect pin. |
| | | | | I2S0_LRCK | O | MFP5 | I2S0 left right channel clock output pin. |
| | | | | SPI1_I2SMCLK | I/O | MFP6 | SPI1 I2S master clock output pin |
| | | | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | | | UART0_TXD | O | MFP8 | UART0 data transmitter output pin. |
| | | | 110 | PH.11 | I/O | MFP0 | General purpose digital I/O pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | | | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | | | UART0_RXD | I | MFP8 | UART0 data receiver input pin. |
| | | | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | | | 111 | PD.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | | SPI3_I2SMCLK | I/O | MFP3 | SPI3 I2S master clock output pin |
| | | | | SC1_nCD | I | MFP4 | Smart Card 1 card detect pin. |
| | | | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| 25 | 37 | 49 | 112 | VSS | P | MFP0 | Ground pin for digital circuit. |
| 26 | 38 | 50 | 113 | LDO_CAP | A | MFP0 | LDO output pin. |
| 27 | 39 | 51 | 114 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 40 | 52 | 115 | PC.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | | SC1_nCD | I | MFP3 | Smart Card 1 card detect pin. |
| | | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | | USCI0_CTL0 | I/O | MFP5 | USCI0 control 0 pin. |
| | | | | QSPI0_CLK | I/O | MFP6 | Quad SPI0 serial clock pin. |
| | | | | EPWM0_SYNC_IN | I | MFP11 | EPWM0 counter synchronous trigger input pin. |
| | | | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | | | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | | | | HSUSB_VBUS_ST | I | MFP15 | HSUSB external VBUS regulator status pin. |
| 28 | 41 | 53 | 116 | PB.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH15 | A | MFP1 | EADC0 channel 15 analog input. |
| | | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | | SC1_PWR | O | MFP3 | Smart Card 1 power pin. |
| | | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | | USCI0_CTL1 | I/O | MFP5 | USCI0 control 1 pin. |
| | | | | UART0_nCTS | I | MFP6 | UART0 clear to Send input pin. |
| | | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | | I2C2_SMBAL | O | MFP8 | I2C2 SMBus SMBALTER pin |
| | | | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | | | | HSUSB_VBUS_EN | O | MFP15 | HSUSB external VBUS regulator enable pin. |
| 29 | 42 | 54 | 117 | PB.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH14 | A | MFP1 | EADC0 channel 14 analog input. |
| | | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | | SC1_RST | O | MFP3 | Smart Card 1 reset pin. |
| | | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | | USCI0_DAT1 | I/O | MFP5 | USCI0 data 1 pin. |
| | | | | UART0_nRTS | O | MFP6 | UART0 request to Send output pin. |
| | | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | | I2C2_SMBSUS | O | MFP8 | I2C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | | CLKO | O | MFP14 | Clock Out |
| 30 | 43 | 55 | 118 | PB.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH13 | A | MFP1 | EADC0 channel 13 analog input. |
| | | | | DAC1_OUT | A | MFP1 | DAC1 channel analog output. |
| | | | | ACMP0_P3 | A | MFP1 | Analog comparator 0 positive input 3 pin. |
| | | | | ACMP1_P3 | A | MFP1 | Analog comparator 1 positive input 3 pin. |
| | | | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | | | SC1_DAT | I/O | MFP3 | Smart Card 1 data pin. |
| | | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | | USCI0_DAT0 | I/O | MFP5 | USCI0 data 0 pin. |
| | | | | UART0_TXD | O | MFP6 | UART0 data transmitter output pin. |
| | | | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | | | I2C2_SCL | I/O | MFP8 | I2C2 clock pin. |
| | | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| 31 | 44 | 56 | 119 | PB.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH12 | A | MFP1 | EADC0 channel 12 analog input. |
| | | | | DAC0_OUT | A | MFP1 | DAC0 channel analog output. |
| | | | | ACMP0_P2 | A | MFP1 | Analog comparator 0 positive input 2 pin. |
| | | | | ACMP1_P2 | A | MFP1 | Analog comparator 1 positive input 2 pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | | | | SC1_CLK | O | MFP3 | Smart Card 1 clock pin. |
| | | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | | USCI0_CLK | I/O | MFP5 | USCI0 clock pin. |
| | | | | UART0_RXD | I | MFP6 | UART0 data receiver input pin. |
| | | | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | | | I2C2_SDA | I/O | MFP8 | I2C2 data input/output pin. |
| | | | | SD0_nCD | I | MFP9 | SD/SDIO0 card detect input pin |
| | | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| 32 | 45 | 57 | 120 | $AV_{DD}$ | P | MFP0 | Power supply for internal analog circuit. |
| | | 58 | 121 | $V_{REF}$ | A | MFP0 | ADC reference voltage input.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| | 46 | 59 | 122 | AVSS | P | MFP0 | Ground pin for analog circuit. |
| | | 60 | 123 | PB.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH11 | A | MFP1 | EADC0 channel 11 analog input. |
| | | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | | UART0_nCTS | I | MFP5 | UART0 clear to Send input pin. |
| | | | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | | | I2C1_SCL | I/O | MFP7 | I2C1 clock pin. |
| | | | | CAN0_TXD | O | MFP8 | CAN0 bus transmitter output. |
| | | | | SPI0_I2SMCLK | I/O | MFP9 | SPI0 I2S master clock output pin |
| | | | | BPWM1_CH0 | I/O | MFP10 | BPWM1 channel 0 output/capture input. |
| | | | | SPI3_CLK | I/O | MFP11 | SPI3 serial clock pin. |
| | | | | HSUSB_VBUS_ST | I | MFP14 | HSUSB external VBUS regulator status pin. |
| | | 61 | 124 | PB.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH10 | A | MFP1 | EADC0 channel 10 analog input. |
| | | | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | | | USCI1_CTL0 | I/O | MFP4 | USCI1 control 0 pin. |
| | | | | UART0_nRTS | O | MFP5 | UART0 request to Send output pin. |
| | | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | | I2C1_SDA | I/O | MFP7 | I2C1 data input/output pin. |
| | | | | CAN0_RXD | I | MFP8 | CAN0 bus receiver input. |
| | | | | BPWM1_CH1 | I/O | MFP10 | BPWM1 channel 1 output/capture input. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | SPI3_SS | I/O | MFP11 | SPI3 slave select pin. |
| | | | | HSUSB_VBUS_EN | O | MFP14 | HSUSB external VBUS regulator enable pin. |
| | | 62 | 125 | PB.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH9 | A | MFP1 | EADC0 channel 9 analog input. |
| | | | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | | | USCI1_CTL1 | I/O | MFP4 | USCI1 control 1 pin. |
| | | | | UART0_TXD | O | MFP5 | UART0 data transmitter output pin. |
| | | | | UART1_nCTS | I | MFP6 | UART1 clear to Send input pin. |
| | | | | I2C1_SMBAL | O | MFP7 | I2C1 SMBus SMBALTER pin |
| | | | | BPWM1_CH2 | I/O | MFP10 | BPWM1 channel 2 output/capture input. |
| | | | | SPI3_MISO | I/O | MFP11 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | | INT7 | I | MFP13 | External interrupt 7 input pin. |
| | | 63 | 126 | PB.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH8 | A | MFP1 | EADC0 channel 8 analog input. |
| | | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | | | USCI1_CLK | I/O | MFP4 | USCI1 clock pin. |
| | | | | UART0_RXD | I | MFP5 | UART0 data receiver input pin. |
| | | | | UART1_nRTS | O | MFP6 | UART1 request to Send output pin. |
| | | | | I2C1_SMBSUS | O | MFP7 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | | BPWM1_CH3 | I/O | MFP10 | BPWM1 channel 3 output/capture input. |
| | | | | SPI3_MOSI | I/O | MFP11 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | | INT6 | I | MFP13 | External interrupt 6 input pin. |
| | 47 | 64 | 127 | PB.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH7 | A | MFP1 | EADC0 channel 7 analog input. |
| | | | | EBI_nWRL | O | MFP2 | EBI low byte write enable output pin. |
| | | | | USCI1_DAT0 | I/O | MFP4 | USCI1 data 0 pin. |
| | | | | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | | SD1_CMD | I/O | MFP7 | SD/SDIO1 command/response pin |
| | | | | EBI_nCS0 | O | MFP8 | EBI chip select 0 output pin. |
| | | | | BPWM1_CH4 | I/O | MFP10 | BPWM1 channel 4 output/capture input. |
| | | | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | | INT5 | I | MFP13 | External interrupt 5 input pin. |

| 32 Pin | 48 Pin | 64 Pin | 128 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|---|
| | | | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | | | | ACMP0_O | O | MFP15 | Analog comparator 0 output pin. |
| | 48 | 1 | 128 | PB.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | | EADC0_CH6 | A | MFP1 | EADC0 channel 6 analog input. |
| | | | | EBI_nWRH | O | MFP2 | EBI high byte write enable output pin |
| | | | | USCI1_DAT1 | I/O | MFP4 | USCI1 data 1 pin. |
| | | | | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | | SD1_CLK | O | MFP7 | SD/SDIO1 clock output pin |
| | | | | EBI_nCS1 | O | MFP8 | EBI chip select 1 output pin. |
| | | | | BPWM1_CH5 | I/O | MFP10 | BPWM1 channel 5 output/capture input. |
| | | | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | | INT4 | I | MFP13 | External interrupt 4 input pin. |
| | | | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | | | | ACMP1_O | O | MFP15 | Analog comparator 1 output pin. |

### 4.2.6 M487 Series Pin Description

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| 2 | 1 | 1 | PB.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH5 | A | MFP1 | EADC0 channel 5 analog input. |
| | | | ACMP1_N | A | MFP1 | Analog comparator 1 negative input pin. |
| | | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | | EMAC_RMII_REFCLK | I | MFP4 | EMAC RMII reference clock input pin. |
| | | | SPI1_MISO | I/O | MFP5 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | I2C0_SCL | I/O | MFP6 | I2C0 clock pin. |
| | | | UART5_TXD | O | MFP7 | UART5 data transmitter output pin. |
| | | | USCI1_CTL0 | I/O | MFP8 | USCI1 control 0 pin. |
| | | | SC0_CLK | O | MFP9 | Smart Card 0 clock pin. |
| | | | I2S0_BCLK | O | MFP10 | I2S0 bit clock output pin. |
| | | | EPWM0_CH0 | I/O | MFP11 | EPWM0 channel 0 output/capture input. |
| | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| 3 | 2 | 2 | PB.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH4 | A | MFP1 | EADC0 channel 4 analog input. |
| | | | ACMP1_P1 | A | MFP1 | Analog comparator 1 positive input 1 pin. |
| | | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | | EMAC_RMII_RXD0 | I | MFP4 | EMAC RMII Receive Data bus bit 0. |
| | | | SPI1_MOSI | I/O | MFP5 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | I2C0_SDA | I/O | MFP6 | I2C0 data input/output pin. |
| | | | UART5_RXD | I | MFP7 | UART5 data receiver input pin. |
| | | | USCI1_CTL1 | I/O | MFP8 | USCI1 control 1 pin. |
| | | | SC0_DAT | I/O | MFP9 | Smart Card 0 data pin. |
| | | | I2S0_MCLK | O | MFP10 | I2S0 master clock output pin. |
| | | | EPWM0_CH1 | I/O | MFP11 | EPWM0 channel 1 output/capture input. |
| | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| 4 | 3 | 3 | PB.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH3 | A | MFP1 | EADC0 channel 3 analog input. |
| | | | ACMP0_N | A | MFP1 | Analog comparator 0 negative input pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | | | EMAC_RMII_RXD1 | I | MFP4 | EMAC RMII Receive Data bus bit 1. |
| | | | SPI1_CLK | I/O | MFP5 | SPI1 serial clock pin. |
| | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | UART5_nRTS | O | MFP7 | UART5 request to Send output pin. |
| | | | USCI1_DAT1 | I/O | MFP8 | USCI1 data 1 pin. |
| | | | SC0_RST | O | MFP9 | Smart Card 0 reset pin. |
| | | | I2S0_DI | I | MFP10 | I2S0 data input pin. |
| | | | EPWM0_CH2 | I/O | MFP11 | EPWM0 channel 2 output/capture input. |
| | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| 5 | 4 | 4 | PB.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH2 | A | MFP1 | EADC0 channel 2 analog input. |
| | | | ACMP0_P1 | A | MFP1 | Analog comparator 0 positive input 1 pin. |
| | | | OPA0_O | A | MFP1 | Operational amplifier 0 output pin. |
| | | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | | EMAC_RMII_CRSDV | I | MFP4 | EMAC RMII Carrier Sense/Receive Data input pin. |
| | | | SPI1_SS | I/O | MFP5 | SPI1 slave select pin. |
| | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | UART5_nCTS | I | MFP7 | UART5 clear to Send input pin. |
| | | | USCI1_DAT0 | I/O | MFP8 | USCI1 data 0 pin. |
| | | | SC0_PWR | O | MFP9 | Smart Card 0 power pin. |
| | | | I2S0_DO | O | MFP10 | I2S0 data output pin. |
| | | | EPWM0_CH3 | I/O | MFP11 | EPWM0 channel 3 output/capture input. |
| | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| | 5 | 5 | PC.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR4 | O | MFP2 | EBI address bus bit 4. |
| | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | SPI3_MISO | I/O | MFP6 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | SC0_nCD | I | MFP9 | Smart Card 0 card detect pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | ECAP1_IC2 | I | MFP11 | Enhanced capture unit 1 input 2 pin. |
| | | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| | | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| | 6 | 6 | PC.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR5 | O | MFP2 | EBI address bus bit 5. |
| | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | SPI3_MOSI | I/O | MFP6 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | ECAP1_IC1 | I | MFP11 | Enhanced capture unit 1 input 1 pin. |
| | | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| | | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | 7 | 7 | PC.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR6 | O | MFP2 | EBI address bus bit 6. |
| | | | SPI3_CLK | I/O | MFP6 | SPI3 serial clock pin. |
| | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | | | ECAP1_IC0 | I | MFP11 | Enhanced capture unit 1 input 0 pin. |
| | | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| | 8 | 8 | PC.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR7 | O | MFP2 | EBI address bus bit 7. |
| | | | SPI3_SS | I/O | MFP6 | SPI3 slave select pin. |
| | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 6 | 9 | 9 | PB.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH1 | A | MFP1 | EADC0 channel 1 analog input. |
| | | | OPA0_N | A | MFP1 | Operational amplifier 0 negative input pin. |
| | | | EBI_ADR8 | O | MFP2 | EBI address bus bit 8. |
| | | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | | EMAC_RMII_RXERR | I | MFP4 | EMAC RMII Receive Data Error input pin. |
| | | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | | SPI3_I2SMCLK | I/O | MFP6 | SPI3 I2S master clock output pin |
| | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | USCI1_CLK | I/O | MFP8 | USCI1 clock pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | I2S0_LRCK | O | MFP10 | I2S0 left right channel clock output pin. |
| | | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | EPWM0_BRAKE0 | I | MFP13 | EPWM0 Brake 0 input pin. |
| 7 | 10 | 10 | PB.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH0 | A | MFP1 | EADC0 channel 0 analog input. |
| | | | OPA0_P | A | MFP1 | Operational amplifier 0 positive input pin. |
| | | | EBI_ADR9 | O | MFP2 | EBI address bus bit 9. |
| | | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | SPI0_I2SMCLK | I/O | MFP8 | SPI0 I2S master clock output pin |
| | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | EPWM0_BRAKE1 | I | MFP13 | EPWM0 Brake 1 input pin. |
| | 11 | 11 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | 12 | 12 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 8 | 13 | 13 | PA.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ACMP0_P0 | A | MFP1 | Analog comparator 0 positive input 0 pin. |
| | | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | | SC2_PWR | O | MFP3 | Smart Card 2 power pin. |
| | | | SPI2_SS | I/O | MFP4 | SPI2 slave select pin. |
| | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | USCI0_CLK | I/O | MFP6 | USCI0 clock pin. |
| | | | I2C2_SCL | I/O | MFP7 | I2C2 clock pin. |
| | | | BPWM0_CH0 | I/O | MFP9 | BPWM0 channel 0 output/capture input. |
| | | | EPWM0_SYNC_OUT | O | MFP10 | EPWM0 counter synchronous trigger output pin. |
| | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | | DAC1_ST | I | MFP14 | DAC1 external trigger input. |
| 9 | 14 | 14 | PA.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | ACMP1_P0 | A | MFP1 | Analog comparator 1 positive input 0 pin. |
| | | | OPA1_O | A | MFP1 | Operational amplifier 1 output pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | | SC2_RST | O | MFP3 | Smart Card 2 reset pin. |
| | | | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | | | USCI0_DAT0 | I/O | MFP6 | USCI0 data 0 pin. |
| | | | I2C2_SDA | I/O | MFP7 | I2C2 data input/output pin. |
| | | | BPWM0_CH1 | I/O | MFP9 | BPWM0 channel 1 output/capture input. |
| | | | QEI1_INDEX | I | MFP10 | Quadrature encoder 1 index input |
| | | | ECAP0_IC0 | I | MFP11 | Enhanced capture unit 0 input 0 pin. |
| | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | DAC0_ST | I | MFP14 | DAC0 external trigger input. |
| 10 | 15 | 15 | PA.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA1_N | A | MFP1 | Operational amplifier 1 negative input pin. |
| | | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | | SC2_DAT | I/O | MFP3 | Smart Card 2 data pin. |
| | | | SPI2_MISO | I/O | MFP4 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | | USCI0_DAT1 | I/O | MFP6 | USCI0 data 1 pin. |
| | | | UART1_TXD | O | MFP7 | UART1 data transmitter output pin. |
| | | | BPWM0_CH2 | I/O | MFP9 | BPWM0 channel 2 output/capture input. |
| | | | QEI1_A | I | MFP10 | Quadrature encoder 1 phase A input |
| | | | ECAP0_IC1 | I | MFP11 | Enhanced capture unit 0 input 1 pin. |
| | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| 11 | 16 | 16 | PA.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA1_P | A | MFP1 | Operational amplifier 1 positive input pin. |
| | | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | | SC2_CLK | O | MFP3 | Smart Card 2 clock pin. |
| | | | SPI2_MOSI | I/O | MFP4 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | | USCI0_CTL1 | I/O | MFP6 | USCI0 control 1 pin. |
| | | | UART1_RXD | I | MFP7 | UART1 data receiver input pin. |
| | | | BPWM0_CH3 | I/O | MFP9 | BPWM0 channel 3 output/capture input. |
| | | | QEI1_B | I | MFP10 | Quadrature encoder 1 phase B input |
| | | | ECAP0_IC2 | I | MFP11 | Enhanced capture unit 0 input 2 pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| | | | INT4 | I | MFP15 | External interrupt 4 input pin. |
| | 17 | 17 | PC.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | | SC2_nCD | I | MFP3 | Smart Card 2 card detect pin. |
| | | | SPI2_I2SMCLK | I/O | MFP4 | SPI2 I2S master clock output pin |
| | | | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | | | USCI0_CTL0 | I/O | MFP6 | USCI0 control 0 pin. |
| | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | BPWM0_CH4 | I/O | MFP9 | BPWM0 channel 4 output/capture input. |
| | | | CLKO | O | MFP13 | Clock Out |
| | | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | 18 | 18 | PD.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA2_O | A | MFP1 | Operational amplifier 2 output pin. |
| | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | BPWM0_CH5 | I/O | MFP9 | BPWM0 channel 5 output/capture input. |
| | | | QEI0_INDEX | I | MFP10 | Quadrature encoder 0 index input |
| | | | CLKO | O | MFP13 | Clock Out |
| | | | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | | | INT5 | I | MFP15 | External interrupt 5 input pin. |
| | 19 | 19 | PD.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA2_N | A | MFP1 | Operational amplifier 2 negative input pin. |
| | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | UART1_TXD | O | MFP3 | UART1 data transmitter output pin. |
| | | | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | | | QEI0_A | I | MFP10 | Quadrature encoder 0 phase A input |
| | | | INT6 | I | MFP15 | External interrupt 6 input pin. |
| | 20 | 20 | PD.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | OPA2_P | A | MFP1 | Operational amplifier 2 positive input pin. |
| | | | EBI_nCS2 | O | MFP2 | EBI chip select 2 output pin. |
| | | | UART1_RXD | I | MFP3 | UART1 data receiver input pin. |
| | | | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | QEI0_B | I | MFP10 | Quadrature encoder 0 phase B input |
| | | | INT7 | I | MFP15 | External interrupt 7 input pin. |
| | | 21 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | | 22 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | | 23 | PG.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR8 | O | MFP2 | EBI address bus bit 8. |
| | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | I2C1_SMBAL | O | MFP5 | I2C1 SMBus SMBALTER pin |
| | | | UART2_RXD | I | MFP6 | UART2 data receiver input pin. |
| | | | CAN1_TXD | O | MFP7 | CAN1 bus transmitter output. |
| | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | 24 | PG.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR9 | O | MFP2 | EBI address bus bit 9. |
| | | | SPI2_I2SMCLK | I/O | MFP3 | SPI2 I2S master clock output pin |
| | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | I2C1_SMBSUS | O | MFP5 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | UART2_TXD | O | MFP6 | UART2 data transmitter output pin. |
| | | | CAN1_RXD | I | MFP7 | CAN1 bus receiver input. |
| | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | 21 | 25 | PG.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | | SPI2_SS | I/O | MFP3 | SPI2 slave select pin. |
| | | | I2C0_SMBAL | O | MFP4 | I2C0 SMBus SMBALTER pin |
| | | | I2C1_SCL | I/O | MFP5 | I2C1 clock pin. |
| | | | TM0 | I/O | MFP13 | Timer0 event counter input/toggle output pin. |
| | 22 | 26 | PG.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | | SPI2_CLK | I/O | MFP3 | SPI2 serial clock pin. |
| | | | I2C0_SMBSUS | O | MFP4 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | I2C1_SDA | I/O | MFP5 | I2C1 data input/output pin. |
| | | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | 23 | 27 | PG.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI2_MISO | I/O | MFP3 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | TM2 | I/O | MFP13 | Timer2 event counter input/toggle output pin. |
| | 24 | 28 | PF.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | | | SPI2_MOSI | I/O | MFP3 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | TAMPER5 | I/O | MFP10 | TAMPER detector loop pin 5. |
| | | | TM3 | I/O | MFP13 | Timer3 event counter input/toggle output pin. |
| | 25 | 29 | PF.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | | SC0_nCD | I | MFP3 | Smart Card 0 card detect pin. |
| | | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |
| | | | SPI0_I2SMCLK | I/O | MFP5 | SPI0 I2S master clock output pin |
| | | | TAMPER4 | I/O | MFP10 | TAMPER detector loop pin 4. |
| | 26 | 30 | PF.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | SC0_PWR | O | MFP3 | Smart Card 0 power pin. |
| | | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |
| | | | SPI0_SS | I/O | MFP5 | SPI0 slave select pin. |
| | | | TAMPER3 | I/O | MFP10 | TAMPER detector loop pin 3. |
| | 27 | 31 | PF.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | | SC0_RST | O | MFP3 | Smart Card 0 reset pin. |
| | | | I2S0_DI | I | MFP4 | I2S0 data input pin. |
| | | | SPI0_CLK | I/O | MFP5 | SPI0 serial clock pin. |
| | | | TAMPER2 | I/O | MFP10 | TAMPER detector loop pin 2. |
| | 28 | 32 | PF.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | | SC0_DAT | I/O | MFP3 | Smart Card 0 data pin. |
| | | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | | SPI0_MISO | I/O | MFP5 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | | TAMPER1 | I/O | MFP10 | TAMPER detector loop pin 1. |
| 12 | 29 | 33 | PF.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC0_CLK | O | MFP3 | Smart Card 0 clock pin. |
| | | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | | SPI0_MOSI | I/O | MFP5 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | EBI_nCS0 | O | MFP7 | EBI chip select 0 output pin. |
| | | | TAMPER0 | I/O | MFP10 | TAMPER detector loop pin 0. |
| 13 | 30 | 34 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 14 | 31 | 35 | PF.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART2_RXD | I | MFP2 | UART2 data receiver input pin. |
| | | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | | | BPWM0_CH4 | I/O | MFP8 | BPWM0 channel 4 output/capture input. |
| | | | EPWM0_SYNC_OUT | O | MFP9 | EPWM0 counter synchronous trigger output pin. |
| | | | X32_IN | I | MFP10 | External 32.768 kHz crystal input pin. |
| | | | EADC0_ST | I | MFP11 | EADC0 external trigger input. |
| 15 | 32 | 36 | PF.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART2_TXD | O | MFP2 | UART2 data transmitter output pin. |
| | | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| | | | BPWM0_CH5 | I/O | MFP8 | BPWM0 channel 5 output/capture input. |
| | | | X32_OUT | O | MFP10 | External 32.768 kHz crystal output pin. |
| | | 37 | PH.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR7 | O | MFP2 | EBI address bus bit 7. |
| | | | UART5_TXD | O | MFP4 | UART5 data transmitter output pin. |
| | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | 38 | PH.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR6 | O | MFP2 | EBI address bus bit 6. |
| | | | UART5_RXD | I | MFP4 | UART5 data receiver input pin. |
| | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | 39 | PH.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR5 | O | MFP2 | EBI address bus bit 5. |
| | | | UART5_nRTS | O | MFP4 | UART5 request to Send output pin. |
| | | | UART4_TXD | O | MFP5 | UART4 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP6 | I2C0 clock pin. |
| | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | 40 | PH.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR4 | O | MFP2 | EBI address bus bit 4. |
| | | | SPI1_I2SMCLK | I/O | MFP3 | SPI1 I2S master clock output pin |
| | | | UART5_nCTS | I | MFP4 | UART5 clear to Send input pin. |
| | | | UART4_RXD | I | MFP5 | UART4 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP6 | I2C0 data input/output pin. |
| | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| | 33 | 41 | PH.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | | | SPI1_MISO | I/O | MFP3 | SPI1 MISO (Master In, Slave Out) pin. |
| | 34 | 42 | PH.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | | | SPI1_MOSI | I/O | MFP3 | SPI1 MOSI (Master Out, Slave In) pin. |
| | 35 | 43 | PH.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | | | SPI1_CLK | I/O | MFP3 | SPI1 serial clock pin. |
| | 36 | 44 | PH.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | | | SPI1_SS | I/O | MFP3 | SPI1 slave select pin. |
| 16 | 37 | 45 | PF.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | XT1_IN | I | MFP10 | External 4~24 MHz (high speed) crystal input pin. |
| | | | BPWM1_CH0 | I/O | MFP11 | BPWM1 channel 0 output/capture input. |
| 17 | 38 | 46 | PF.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | QSPI0_CLK | I/O | MFP5 | Quad SPI0 serial clock pin. |
| | | | XT1_OUT | O | MFP10 | External 4~24 MHz (high speed) crystal output pin. |
| | | | BPWM1_CH1 | I/O | MFP11 | BPWM1 channel 1 output/capture input. |
| | 39 | 47 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | 40 | 48 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | | | | and digital circuit. |
| | 41 | 49 | PE.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | | | EMAC_RMII_MDC | O | MFP3 | EMAC RMII PHY Management Clock output pin. |
| | | | I2S0_BCLK | O | MFP4 | I2S0 bit clock output pin. |
| | | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | | USCI1_CTL1 | I/O | MFP6 | USCI1 control 1 pin. |
| | | | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | | | EPWM0_CH0 | I/O | MFP10 | EPWM0 channel 0 output/capture input. |
| | | | EPWM0_BRAKE0 | I | MFP11 | EPWM0 Brake 0 input pin. |
| | | | ECAP0_IC0 | I | MFP12 | Enhanced capture unit 0 input 0 pin. |
| | | | TRACE_CLK | O | MFP14 | ETM Trace Clock output pin |
| | 42 | 50 | PE.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | | | EMAC_RMII_MDIO | I/O | MFP3 | EMAC RMII PHY Management Data pin. |
| | | | I2S0_MCLK | O | MFP4 | I2S0 master clock output pin. |
| | | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |
| | | | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | | | EPWM0_CH1 | I/O | MFP10 | EPWM0 channel 1 output/capture input. |
| | | | EPWM0_BRAKE1 | I | MFP11 | EPWM0 Brake 1 input pin. |
| | | | ECAP0_IC1 | I | MFP12 | Enhanced capture unit 0 input 1 pin. |
| | | | TRACE_DATA0 | O | MFP14 | ETM Trace Data 0 output pin |
| | 43 | 51 | PE.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | | | EMAC_RMII_TXD0 | O | MFP3 | EMAC RMII Transmit Data bus bit 0. |
| | | | I2S0_DI | I | MFP4 | I2S0 data input pin. |
| | | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | USCI1_DAT0 | I/O | MFP6 | USCI1 data 0 pin. |
| | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | EPWM0_CH2 | I/O | MFP10 | EPWM0 channel 2 output/capture input. |
| | | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | | ECAP0_IC2 | I | MFP12 | Enhanced capture unit 0 input 2 pin. |
| | | | TRACE_DATA1 | O | MFP14 | ETM Trace Data 1 output pin |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | 44 | 52 | PE.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | | | EMAC_RMII_TXD1 | O | MFP3 | EMAC RMII Transmit Data bus bit 1. |
| | | | I2S0_DO | O | MFP4 | I2S0 data output pin. |
| | | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | | USCI1_DAT1 | I/O | MFP6 | USCI1 data 1 pin. |
| | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | | EPWM0_CH3 | I/O | MFP10 | EPWM0 channel 3 output/capture input. |
| | | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | | ECAP1_IC2 | I | MFP13 | Enhanced capture unit 1 input 2 pin. |
| | | | TRACE_DATA2 | O | MFP14 | ETM Trace Data 2 output pin |
| | 45 | 53 | PE.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | | | EMAC_RMII_TXEN | O | MFP3 | EMAC RMII Transmit Enable output pin. |
| | | | I2S0_LRCK | O | MFP4 | I2S0 left right channel clock output pin. |
| | | | SPI2_I2SMCLK | I/O | MFP5 | SPI2 I2S master clock output pin |
| | | | USCI1_CLK | I/O | MFP6 | USCI1 clock pin. |
| | | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | | EPWM0_CH4 | I/O | MFP10 | EPWM0 channel 4 output/capture input. |
| | | | ECAP1_IC1 | I | MFP13 | Enhanced capture unit 1 input 1 pin. |
| | | | TRACE_DATA3 | O | MFP14 | ETM Trace Data 3 output pin |
| | 46 | 54 | PE.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | | | EMAC_PPS | O | MFP3 | EMAC Pulse Per Second output pin. |
| | | | I2C0_SCL | I/O | MFP4 | I2C0 clock pin. |
| | | | UART4_nRTS | O | MFP5 | UART4 request to Send output pin. |
| | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | | EPWM0_CH5 | I/O | MFP10 | EPWM0 channel 5 output/capture input. |
| | | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | | BPWM1_CH5 | I/O | MFP12 | BPWM1 channel 5 output/capture input. |
| | | | ECAP1_IC0 | I | MFP13 | Enhanced capture unit 1 input 0 pin. |
| | 47 | 55 | PC.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EMAC_RMII_REFCLK | I | MFP3 | EMAC RMII reference clock input pin. |
| | | | I2C0_SDA | I/O | MFP4 | I2C0 data input/output pin. |
| | | | UART4_nCTS | I | MFP5 | UART4 clear to Send input pin. |
| | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | | BPWM1_CH4 | I/O | MFP12 | BPWM1 channel 4 output/capture input. |
| 18 | 48 | 56 | PC.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | | EMAC_RMII_RXD0 | I | MFP3 | EMAC RMII Receive Data bus bit 0. |
| | | | SPI1_MISO | I/O | MFP4 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | UART4_TXD | O | MFP5 | UART4 data transmitter output pin. |
| | | | SC2_PWR | O | MFP6 | Smart Card 2 power pin. |
| | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | | | INT3 | I | MFP15 | External interrupt 3 input pin. |
| 19 | 49 | 57 | PC.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | | EMAC_RMII_RXD1 | I | MFP3 | EMAC RMII Receive Data bus bit 1. |
| | | | SPI1_MOSI | I/O | MFP4 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | UART4_RXD | I | MFP5 | UART4 data receiver input pin. |
| | | | SC2_RST | O | MFP6 | Smart Card 2 reset pin. |
| | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | | | INT2 | I | MFP15 | External interrupt 2 input pin. |
| 20 | 50 | 58 | PA.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | | EMAC_RMII_CRSDV | I | MFP3 | EMAC RMII Carrier Sense/Receive Data input pin. |
| | | | SPI1_CLK | I/O | MFP4 | SPI1 serial clock pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC2_DAT | I/O | MFP6 | Smart Card 2 data pin. |
| | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | | EPWM1_CH4 | I/O | MFP11 | EPWM1 channel 4 output/capture input. |
| | | | BPWM1_CH2 | I/O | MFP12 | BPWM1 channel 2 output/capture input. |
| | | | ACMP0_WLAT | I | MFP13 | Analog comparator 0 window latch input pin |
| | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | | | INT1 | I | MFP15 | External interrupt 1 input pin. |
| 21 | 51 | 59 | PA.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | | EMAC_RMII_RXERR | I | MFP3 | EMAC RMII Receive Data Error input pin. |
| | | | SPI1_SS | I/O | MFP4 | SPI1 slave select pin. |
| | | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | | | SC2_CLK | O | MFP6 | Smart Card 2 clock pin. |
| | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | | EPWM1_CH5 | I/O | MFP11 | EPWM1 channel 5 output/capture input. |
| | | | BPWM1_CH3 | I/O | MFP12 | BPWM1 channel 3 output/capture input. |
| | | | ACMP1_WLAT | I | MFP13 | Analog comparator 1 window latch input pin |
| | | | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | | | INT0 | I | MFP15 | External interrupt 0 input pin. |
| 22 | 52 | 60 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| 23 | 53 | 61 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 24 | 54 | 62 | LDO_CAP | A | MFP0 | LDO output pin. |
| 25 | 55 | 63 | PA.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_D2 | I/O | MFP2 | SPIM data 2 pin for Quad Mode I/O. |
| | | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | SPI1_I2SMCLK | I/O | MFP4 | SPI1 I2S master clock output pin |
| | | | SD1_CMD | I/O | MFP5 | SD/SDIO1 command/response pin |
| | | | SC2_nCD | I | MFP6 | Smart Card 2 card detect pin. |
| | | | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | | | EPWM0_CH0 | I/O | MFP13 | EPWM0 channel 0 output/capture input. |
| | | | QEI0_INDEX | I | MFP14 | Quadrature encoder 0 index input |
| 26 | 56 | 64 | PA.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_D3 | I/O | MFP2 | SPIM data 3 pin for Quad Mode I/O. |
| | | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | SD1_CLK | O | MFP5 | SD/SDIO1 clock output pin |
| | | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | | | EPWM0_CH1 | I/O | MFP13 | EPWM0 channel 1 output/capture input. |
| | | | QEI0_A | I | MFP14 | Quadrature encoder 0 phase A input |
| 27 | 57 | 65 | PA.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_SS | I/O | MFP2 | SPIM slave select pin. |
| | | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | | | EPWM0_CH2 | I/O | MFP13 | EPWM0 channel 2 output/capture input. |
| | | | QEI0_B | I | MFP14 | Quadrature encoder 0 phase B input |
| 28 | 58 | 66 | PA.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_CLK | I/O | MFP2 | SPIM serial clock pin. |
| | | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | | | EPWM0_CH3 | I/O | MFP13 | EPWM0 channel 3 output/capture input. |
| 29 | 59 | 67 | PA.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_MISO | I/O | MFP2 | SPIM MISO (Master In, Slave Out) pin. |
| | | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | | | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | | | EPWM0_CH4 | I/O | MFP13 | EPWM0 channel 4 output/capture input. |
| | | | DAC1_ST | I | MFP15 | DAC1 external trigger input. |
| 30 | 60 | 68 | PA.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SPIM_MOSI | I/O | MFP2 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | | | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | | | EPWM0_CH5 | I/O | MFP13 | EPWM0 channel 5 output/capture input. |
| | | | DAC0_ST | I | MFP15 | DAC0 external trigger input. |
| 31 | 61 | 69 | $V_{DDIO}$ | P | MFP0 | Power supply for PA.0~PA.5. |
| | 62 | 70 | PE.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | | | UART2_TXD | O | MFP3 | UART2 data transmitter output pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | | | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | 63 | 71 | PE.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | | | UART2_RXD | I | MFP3 | UART2 data receiver input pin. |
| | | | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |
| 32 | 64 | 72 | nRESET | I | MFP0 | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. |
| 33 | 65 | 73 | PF.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_TXD | O | MFP2 | UART1 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP3 | I2C1 clock pin. |
| | | | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | | | ICE_DAT | O | MFP14 | Serial wired debugger data pin. |
| 34 | 66 | 74 | PF.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | UART1_RXD | I | MFP2 | UART1 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP3 | I2C1 data input/output pin. |
| | | | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | | | ICE_CLK | I | MFP14 | Serial wired debugger clock pin. |
| | 67 | 75 | PD.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | | | I2C2_SCL | I/O | MFP3 | I2C2 clock pin. |
| | | | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | 68 | 76 | PD.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | | | I2C2_SDA | I/O | MFP3 | I2C2 data input/output pin. |
| | | | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| 35 | 69 | 77 | PC.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | | | SPIM_D2 | I/O | MFP3 | SPIM data 2 pin for Quad Mode I/O. |
| | | | QSPI0_MISO1 | I/O | MFP4 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP9 | I2C1 clock pin. |
| | | | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | | | UART4_TXD | O | MFP11 | UART4 data transmitter output pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| 36 | 70 | 78 | PC.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | | SPIM_D3 | I/O | MFP3 | SPIM data 3 pin for Quad Mode I/O. |
| | | | QSPI0_MOSI1 | I/O | MFP4 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | SC1_nCD | I | MFP5 | Smart Card 1 card detect pin. |
| | | | I2S0_BCLK | O | MFP6 | I2S0 bit clock output pin. |
| | | | SPI1_I2SMCLK | I/O | MFP7 | SPI1 I2S master clock output pin |
| | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP9 | I2C1 data input/output pin. |
| | | | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | | | UART4_RXD | I | MFP11 | UART4 data receiver input pin. |
| | | | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| 37 | 71 | 79 | PC.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | | SPIM_SS | I/O | MFP3 | SPIM slave select pin. |
| | | | QSPI0_SS | I/O | MFP4 | Quad SPI0 slave select pin. |
| | | | SC1_PWR | O | MFP5 | Smart Card 1 power pin. |
| | | | I2S0_MCLK | O | MFP6 | I2S0 master clock output pin. |
| | | | SPI1_MISO | I/O | MFP7 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | UART2_nRTS | O | MFP8 | UART2 request to Send output pin. |
| | | | I2C0_SMBAL | O | MFP9 | I2C0 SMBus SMBALTER pin |
| | | | CAN1_TXD | O | MFP10 | CAN1 bus transmitter output. |
| | | | UART3_TXD | O | MFP11 | UART3 data transmitter output pin. |
| | | | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| 38 | 72 | 80 | PC.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | | SPIM_CLK | I/O | MFP3 | SPIM serial clock pin. |
| | | | QSPI0_CLK | I/O | MFP4 | Quad SPI0 serial clock pin. |
| | | | SC1_RST | O | MFP5 | Smart Card 1 reset pin. |
| | | | I2S0_DI | I | MFP6 | I2S0 data input pin. |
| | | | SPI1_MOSI | I/O | MFP7 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | UART2_nCTS | I | MFP8 | UART2 clear to Send input pin. |
| | | | I2C0_SMBSUS | O | MFP9 | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | CAN1_RXD | I | MFP10 | CAN1 bus receiver input. |
| | | | UART3_RXD | I | MFP11 | UART3 data receiver input pin. |
| | | | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| 39 | 73 | 81 | PC.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | | SPIM_MISO | I/O | MFP3 | SPIM MISO (Master In, Slave Out) pin. |
| | | | QSPI0_MISO0 | I/O | MFP4 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | SC1_DAT | I/O | MFP5 | Smart Card 1 data pin. |
| | | | I2S0_DO | O | MFP6 | I2S0 data output pin. |
| | | | SPI1_CLK | I/O | MFP7 | SPI1 serial clock pin. |
| | | | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | | | I2C0_SCL | I/O | MFP9 | I2C0 clock pin. |
| | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| 40 | 74 | 82 | PC.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | | SPIM_MOSI | I/O | MFP3 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | QSPI0_MOSI0 | I/O | MFP4 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | SC1_CLK | O | MFP5 | Smart Card 1 clock pin. |
| | | | I2S0_LRCK | O | MFP6 | I2S0 left right channel clock output pin. |
| | | | SPI1_SS | I/O | MFP7 | SPI1 slave select pin. |
| | | | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | | | I2C0_SDA | I/O | MFP9 | I2C0 data input/output pin. |
| | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| | 75 | 83 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | 76 | 84 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 77 | 85 | PG.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | | | SD1_DAT3 | I/O | MFP3 | SD/SDIO1 data line bit 3. |
| | | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | 78 | 86 | PG.10 | I/O | MFP0 | General purpose digital I/O pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | | | SD1_DAT2 | I/O | MFP3 | SD/SDIO1 data line bit 2. |
| | | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | 79 | 87 | PG.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | | | SD1_DAT1 | I/O | MFP3 | SD/SDIO1 data line bit 1. |
| | | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | | | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | 80 | 88 | PG.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | | | SD1_DAT0 | I/O | MFP3 | SD/SDIO1 data line bit 0. |
| | | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | 81 | 89 | PG.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | | | SD1_CMD | I/O | MFP3 | SD/SDIO1 command/response pin |
| | | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | 82 | 90 | PG.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | | | SD1_CLK | O | MFP3 | SD/SDIO1 clock output pin |
| | | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | 83 | 91 | PG.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SD1_nCD | I | MFP3 | SD/SDIO1 card detect input pin |
| | | | CLKO | O | MFP14 | Clock Out |
| | | | EADC0_ST | I | MFP15 | EADC0 external trigger input. |
| | | 92 | PD.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | USCI0_CTL1 | I/O | MFP3 | USCI0 control 1 pin. |
| | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | UART3_nRTS | O | MFP5 | UART3 request to Send output pin. |
| | | | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | | | SC1_nCD | I | MFP8 | Smart Card 1 card detect pin. |
| | | | UART0_TXD | O | MFP9 | UART0 data transmitter output pin. |
| | | 93 | PD.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | USCI0_DAT1 | I/O | MFP3 | USCI0 data 1 pin. |
| | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | UART3_nCTS | I | MFP5 | UART3 clear to Send input pin. |
| | | | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | | | UART0_RXD | I | MFP9 | UART0 data receiver input pin. |
| | | 94 | PD.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | USCI0_DAT0 | I/O | MFP3 | USCI0 data 0 pin. |
| | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | UART3_TXD | O | MFP5 | UART3 data transmitter output pin. |
| | | | I2C2_SCL | I/O | MFP6 | I2C2 clock pin. |
| | | | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | | 95 | PD.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | USCI0_CLK | I/O | MFP3 | USCI0 clock pin. |
| | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | UART3_RXD | I | MFP5 | UART3 data receiver input pin. |
| | | | I2C2_SDA | I/O | MFP6 | I2C2 data input/output pin. |
| | | | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | | | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | 84 | 96 | PD.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | SD0_nCD | I | MFP3 | SD/SDIO0 card detect input pin |
| | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | SPI1_I2SMCLK | I/O | MFP5 | SPI1 I2S master clock output pin |
| | | | SC2_nCD | I | MFP7 | Smart Card 2 card detect pin. |
| | 85 | 97 | PA.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_BCLK | O | MFP2 | I2S0 bit clock output pin. |
| | | | UART4_TXD | O | MFP3 | UART4 data transmitter output pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | I2C1_SCL | I/O | MFP4 | I2C1 clock pin. |
| | | | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | | | CAN0_TXD | O | MFP6 | CAN0 bus transmitter output. |
| | | | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | | | BPWM1_CH2 | I/O | MFP11 | BPWM1 channel 2 output/capture input. |
| | | | QEI1_INDEX | I | MFP12 | Quadrature encoder 1 index input |
| | | | USB_VBUS | P | MFP14 | Power supply from USB host or HUB. |
| | 86 | 98 | PA.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_MCLK | O | MFP2 | I2S0 master clock output pin. |
| | | | UART4_RXD | I | MFP3 | UART4 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP4 | I2C1 data input/output pin. |
| | | | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | | | CAN0_RXD | I | MFP6 | CAN0 bus receiver input. |
| | | | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | | | BPWM1_CH3 | I/O | MFP11 | BPWM1 channel 3 output/capture input. |
| | | | QEI1_A | I | MFP12 | Quadrature encoder 1 phase A input |
| | | | USB_D- | A | MFP14 | USB differential signal D-. |
| | 87 | 99 | PA.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_DI | I | MFP2 | I2S0 data input pin. |
| | | | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | | | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | | | I2C2_SCL | I/O | MFP6 | I2C2 clock pin. |
| | | | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | | | BPWM1_CH4 | I/O | MFP11 | BPWM1 channel 4 output/capture input. |
| | | | QEI1_B | I | MFP12 | Quadrature encoder 1 phase B input |
| | | | USB_D+ | A | MFP14 | USB differential signal D+. |
| | 88 | 100 | PA.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | I2S0_DO | O | MFP2 | I2S0 data output pin. |
| | | | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | | | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | | | I2C2_SDA | I/O | MFP6 | I2C2 data input/output pin. |
| | | | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | | | BPWM1_CH5 | I/O | MFP11 | BPWM1 channel 5 output/capture input. |
| | | | EPWM0_SYNC_IN | I | MFP12 | EPWM0 counter synchronous trigger input pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | USB_OTG_ID | I | MFP14 | USB_ identification. |
| 41 | 89 | 101 | HSUSB_VRES | A | MFP0 | HSUSB module reference resister |
| 42 | 90 | 102 | HSUSB_VDD33 | P | MFP0 | Power supply for HSUSB VDD33 |
| 43 | 91 | 103 | HSUSB_VBUS | P | MFP0 | HSUSB Power supply from USB host or HUB. |
| 44 | 92 | 104 | HSUSB_D- | A | MFP0 | HSUSB differential signal D-. |
| 45 | 93 | 105 | HSUSB_VSS | P | MFP0 | Ground pin for HSUSB. |
| 46 | 94 | 106 | HSUSB_D+ | A | MFP0 | HSUSB differential signal D+. |
| 47 | 95 | 107 | HSUSB_VDD12_CAP | A | MFP0 | HSUSB Internal power regulator output 1.2V decoupling pin. Note: This pin needs to be connected with a 1uF capacitor. |
| 48 | 96 | 108 | HSUSB_ID | I | MFP0 | HSUSB identification. |
| | 97 | 109 | PE.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | | | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | | | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | | | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | | | QEI1_INDEX | I | MFP11 | Quadrature encoder 1 index input |
| | | | EPWM0_CH0 | I/O | MFP12 | EPWM0 channel 0 output/capture input. |
| | | | BPWM0_CH5 | I/O | MFP13 | BPWM0 channel 5 output/capture input. |
| | 98 | 110 | PE.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | | | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | | | SPI3_I2SMCLK | I/O | MFP5 | SPI3 I2S master clock output pin |
| | | | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | | | USCI0_CTL0 | I/O | MFP7 | USCI0 control 0 pin. |
| | | | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | | | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | | | QEI1_A | I | MFP11 | Quadrature encoder 1 phase A input |
| | | | EPWM0_CH1 | I/O | MFP12 | EPWM0 channel 1 output/capture input. |
| | | | BPWM0_CH4 | I/O | MFP13 | BPWM0 channel 4 output/capture input. |
| | 99 | 111 | PE.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | | | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | | | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | | | SPI3_SS | I/O | MFP5 | SPI3 slave select pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | | | USCI0_CTL1 | I/O | MFP7 | USCI0 control 1 pin. |
| | | | QEI1_B | I | MFP11 | Quadrature encoder 1 phase B input |
| | | | EPWM0_CH2 | I/O | MFP12 | EPWM0 channel 2 output/capture input. |
| | | | BPWM0_CH3 | I/O | MFP13 | BPWM0 channel 3 output/capture input. |
| | 100 | 112 | PE.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | | | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | | | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | | | SPI3_CLK | I/O | MFP5 | SPI3 serial clock pin. |
| | | | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | | | USCI0_DAT1 | I/O | MFP7 | USCI0 data 1 pin. |
| | | | QEI0_INDEX | I | MFP11 | Quadrature encoder 0 index input |
| | | | EPWM0_CH3 | I/O | MFP12 | EPWM0 channel 3 output/capture input. |
| | | | BPWM0_CH2 | I/O | MFP13 | BPWM0 channel 2 output/capture input. |
| | 101 | 113 | PE.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | | | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | | | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | | | SPI3_MISO | I/O | MFP5 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | | | USCI0_DAT0 | I/O | MFP7 | USCI0 data 0 pin. |
| | | | QEI0_A | I | MFP11 | Quadrature encoder 0 phase A input |
| | | | EPWM0_CH4 | I/O | MFP12 | EPWM0 channel 4 output/capture input. |
| | | | BPWM0_CH1 | I/O | MFP13 | BPWM0 channel 1 output/capture input. |
| | 102 | 114 | PE.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | | | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | | | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | | | SPI3_MOSI | I/O | MFP5 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | | | USCI0_CLK | I/O | MFP7 | USCI0 clock pin. |
| | | | QEI0_B | I | MFP11 | Quadrature encoder 0 phase B input |
| | | | EPWM0_CH5 | I/O | MFP12 | EPWM0 channel 5 output/capture input. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | BPWM0_CH0 | I/O | MFP13 | BPWM0 channel 0 output/capture input. |
| | 103 | 115 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| | 104 | 116 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | 105 | 117 | PE.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | | | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | | SC2_DAT | I/O | MFP4 | Smart Card 2 data pin. |
| | | | I2S0_BCLK | O | MFP5 | I2S0 bit clock output pin. |
| | | | SPI1_MISO | I/O | MFP6 | SPI1 MISO (Master In, Slave Out) pin. |
| | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP8 | I2C1 clock pin. |
| | | | UART4_nCTS | I | MFP9 | UART4 clear to Send input pin. |
| | 106 | 118 | PE.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | | SC2_CLK | O | MFP4 | Smart Card 2 clock pin. |
| | | | I2S0_MCLK | O | MFP5 | I2S0 master clock output pin. |
| | | | SPI1_MOSI | I/O | MFP6 | SPI1 MOSI (Master Out, Slave In) pin. |
| | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP8 | I2C1 data input/output pin. |
| | | | UART4_nRTS | O | MFP9 | UART4 request to Send output pin. |
| | 107 | 119 | PH.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | | | SC2_PWR | O | MFP4 | Smart Card 2 power pin. |
| | | | I2S0_DI | I | MFP5 | I2S0 data input pin. |
| | | | SPI1_CLK | I/O | MFP6 | SPI1 serial clock pin. |
| | | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | | I2C1_SMBAL | O | MFP8 | I2C1 SMBus SMBALTER pin |
| | | | I2C2_SCL | I/O | MFP9 | I2C2 clock pin. |
| | | | UART1_TXD | O | MFP10 | UART1 data transmitter output pin. |
| | 108 | 120 | PH.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | | | SC2_RST | O | MFP4 | Smart Card 2 reset pin. |
| | | | I2S0_DO | O | MFP5 | I2S0 data output pin. |
| | | | SPI1_SS | I/O | MFP6 | SPI1 slave select pin. |
| | | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | | I2C1_SMBSUS | O | MFP8 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | I2C2_SDA | I/O | MFP9 | I2C2 data input/output pin. |
| | | | UART1_RXD | I | MFP10 | UART1 data receiver input pin. |
| | 109 | 121 | PH.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | | SC2_nCD | I | MFP4 | Smart Card 2 card detect pin. |
| | | | I2S0_LRCK | O | MFP5 | I2S0 left right channel clock output pin. |
| | | | SPI1_I2SMCLK | I/O | MFP6 | SPI1 I2S master clock output pin |
| | | | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | | | UART0_TXD | O | MFP8 | UART0 data transmitter output pin. |
| | 110 | 122 | PH.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | | | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | | | UART0_RXD | I | MFP8 | UART0 data receiver input pin. |
| | | | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | 111 | 123 | PD.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | | | SPI3_I2SMCLK | I/O | MFP3 | SPI3 I2S master clock output pin |
| | | | SC1_nCD | I | MFP4 | Smart Card 1 card detect pin. |
| | | | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| | | 124 | PG.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | | | SPI3_SS | I/O | MFP3 | SPI3 slave select pin. |
| | | | SC1_PWR | O | MFP4 | Smart Card 1 power pin. |
| | | | EPWM0_CH3 | I/O | MFP11 | EPWM0 channel 3 output/capture input. |
| | | 125 | PG.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nCS2 | O | MFP2 | EBI chip select 2 output pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | SPI3_CLK | I/O | MFP3 | SPI3 serial clock pin. |
| | | | SC1_RST | O | MFP4 | Smart Card 1 reset pin. |
| | | | EPWM0_CH2 | I/O | MFP11 | EPWM0 channel 2 output/capture input. |
| | | 126 | PG.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nWRL | O | MFP2 | EBI low byte write enable output pin. |
| | | | SPI3_MISO | I/O | MFP3 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | SC1_DAT | I/O | MFP4 | Smart Card 1 data pin. |
| | | | EPWM0_CH1 | I/O | MFP11 | EPWM0 channel 1 output/capture input. |
| | | 127 | PG.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_nWRH | O | MFP2 | EBI high byte write enable output pin |
| | | | SPI3_MOSI | I/O | MFP3 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | SC1_CLK | O | MFP4 | Smart Card 1 clock pin. |
| | | | EPWM0_CH0 | I/O | MFP11 | EPWM0 channel 0 output/capture input. |
| 49 | 112 | 128 | $V_{SS}$ | P | MFP0 | Ground pin for digital circuit. |
| 50 | 113 | 129 | LDO_CAP | A | MFP0 | LDO output pin. |
| 51 | 114 | 130 | $V_{DD}$ | P | MFP0 | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| 52 | 115 | 131 | PC.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | | | SC1_nCD | I | MFP3 | Smart Card 1 card detect pin. |
| | | | SPI0_I2SMCLK | I/O | MFP4 | SPI0 I2S master clock output pin |
| | | | USCI0_CTL0 | I/O | MFP5 | USCI0 control 0 pin. |
| | | | QSPI0_CLK | I/O | MFP6 | Quad SPI0 serial clock pin. |
| | | | EPWM0_SYNC_IN | I | MFP11 | EPWM0 counter synchronous trigger input pin. |
| | | | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | | | HSUSB_VBUS_ST | I | MFP15 | HSUSB external VBUS regulator status pin. |
| 53 | 116 | 132 | PB.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH15 | A | MFP1 | EADC0 channel 15 analog input. |
| | | | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | | | SC1_PWR | O | MFP3 | Smart Card 1 power pin. |
| | | | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | | | USCI0_CTL1 | I/O | MFP5 | USCI0 control 1 pin. |
| | | | UART0_nCTS | I | MFP6 | UART0 clear to Send input pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | | | I2C2_SMBAL | O | MFP8 | I2C2 SMBus SMBALTER pin |
| | | | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | | | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | | | HSUSB_VBUS_EN | O | MFP15 | HSUSB external VBUS regulator enable pin. |
| 54 | 117 | 133 | PB.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH14 | A | MFP1 | EADC0 channel 14 analog input. |
| | | | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | | | SC1_RST | O | MFP3 | Smart Card 1 reset pin. |
| | | | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | | | USCI0_DAT1 | I/O | MFP5 | USCI0 data 1 pin. |
| | | | UART0_nRTS | O | MFP6 | UART0 request to Send output pin. |
| | | | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | | | I2C2_SMBSUS | O | MFP8 | I2C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | | | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | | | CLKO | O | MFP14 | Clock Out |
| 55 | 118 | 134 | PB.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH13 | A | MFP1 | EADC0 channel 13 analog input. |
| | | | DAC1_OUT | A | MFP1 | DAC1 channel analog output. |
| | | | ACMP0_P3 | A | MFP1 | Analog comparator 0 positive input 3 pin. |
| | | | ACMP1_P3 | A | MFP1 | Analog comparator 1 positive input 3 pin. |
| | | | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | | | SC1_DAT | I/O | MFP3 | Smart Card 1 data pin. |
| | | | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | | | USCI0_DAT0 | I/O | MFP5 | USCI0 data 0 pin. |
| | | | UART0_TXD | O | MFP6 | UART0 data transmitter output pin. |
| | | | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | | | I2C2_SCL | I/O | MFP8 | I2C2 clock pin. |
| | | | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | | | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| 56 | 119 | 135 | PB.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH12 | A | MFP1 | EADC0 channel 12 analog input. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | DAC0_OUT | A | MFP1 | DAC0 channel analog output. |
| | | | ACMP0_P2 | A | MFP1 | Analog comparator 0 positive input 2 pin. |
| | | | ACMP1_P2 | A | MFP1 | Analog comparator 1 positive input 2 pin. |
| | | | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | | | SC1_CLK | O | MFP3 | Smart Card 1 clock pin. |
| | | | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | | | USCI0_CLK | I/O | MFP5 | USCI0 clock pin. |
| | | | UART0_RXD | I | MFP6 | UART0 data receiver input pin. |
| | | | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | | | I2C2_SDA | I/O | MFP8 | I2C2 data input/output pin. |
| | | | SD0_nCD | I | MFP9 | SD/SDIO0 card detect input pin |
| | | | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | | | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| 57 | 120 | 136 | $AV_{DD}$ | P | MFP0 | Power supply for internal analog circuit. |
| 58 | 121 | 137 | $V_{REF}$ | A | MFP0 | ADC reference voltage input.<br>Note: This pin needs to be connected with a 1uF capacitor. |
| 59 | 122 | 138 | $AV_{SS}$ | P | MFP0 | Ground pin for analog circuit. |
| 60 | 123 | 139 | PB.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH11 | A | MFP1 | EADC0 channel 11 analog input. |
| | | | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | | | EMAC_RMII_MDC | O | MFP3 | EMAC RMII PHY Management Clock output pin. |
| | | | UART0_nCTS | I | MFP5 | UART0 clear to Send input pin. |
| | | | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | | | I2C1_SCL | I/O | MFP7 | I2C1 clock pin. |
| | | | CAN0_TXD | O | MFP8 | CAN0 bus transmitter output. |
| | | | SPI0_I2SMCLK | I/O | MFP9 | SPI0 I2S master clock output pin |
| | | | BPWM1_CH0 | I/O | MFP10 | BPWM1 channel 0 output/capture input. |
| | | | SPI3_CLK | I/O | MFP11 | SPI3 serial clock pin. |
| | | | HSUSB_VBUS_ST | I | MFP14 | HSUSB external VBUS regulator status pin. |
| 61 | 124 | 140 | PB.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH10 | A | MFP1 | EADC0 channel 10 analog input. |
| | | | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | | | EMAC_RMII_MDIO | I/O | MFP3 | EMAC RMII PHY Management Data pin. |
| | | | USCI1_CTL0 | I/O | MFP4 | USCI1 control 0 pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | UART0_nRTS | O | MFP5 | UART0 request to Send output pin. |
| | | | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | | | I2C1_SDA | I/O | MFP7 | I2C1 data input/output pin. |
| | | | CAN0_RXD | I | MFP8 | CAN0 bus receiver input. |
| | | | BPWM1_CH1 | I/O | MFP10 | BPWM1 channel 1 output/capture input. |
| | | | SPI3_SS | I/O | MFP11 | SPI3 slave select pin. |
| | | | HSUSB_VBUS_EN | O | MFP14 | HSUSB external VBUS regulator enable pin. |
| 62 | 125 | 141 | PB.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH9 | A | MFP1 | EADC0 channel 9 analog input. |
| | | | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | | | EMAC_RMII_TXD0 | O | MFP3 | EMAC RMII Transmit Data bus bit 0. |
| | | | USCI1_CTL1 | I/O | MFP4 | USCI1 control 1 pin. |
| | | | UART0_TXD | O | MFP5 | UART0 data transmitter output pin. |
| | | | UART1_nCTS | I | MFP6 | UART1 clear to Send input pin. |
| | | | I2C1_SMBAL | O | MFP7 | I2C1 SMBus SMBALTER pin |
| | | | BPWM1_CH2 | I/O | MFP10 | BPWM1 channel 2 output/capture input. |
| | | | SPI3_MISO | I/O | MFP11 | SPI3 MISO (Master In, Slave Out) pin. |
| | | | INT7 | I | MFP13 | External interrupt 7 input pin. |
| 63 | 126 | 142 | PB.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH8 | A | MFP1 | EADC0 channel 8 analog input. |
| | | | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | | | EMAC_RMII_TXD1 | O | MFP3 | EMAC RMII Transmit Data bus bit 1. |
| | | | USCI1_CLK | I/O | MFP4 | USCI1 clock pin. |
| | | | UART0_RXD | I | MFP5 | UART0 data receiver input pin. |
| | | | UART1_nRTS | O | MFP6 | UART1 request to Send output pin. |
| | | | I2C1_SMBSUS | O | MFP7 | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | | BPWM1_CH3 | I/O | MFP10 | BPWM1 channel 3 output/capture input. |
| | | | SPI3_MOSI | I/O | MFP11 | SPI3 MOSI (Master Out, Slave In) pin. |
| | | | INT6 | I | MFP13 | External interrupt 6 input pin. |
| 64 | 127 | 143 | PB.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH7 | A | MFP1 | EADC0 channel 7 analog input. |
| | | | EBI_nWRL | O | MFP2 | EBI low byte write enable output pin. |
| | | | EMAC_RMII_TXEN | O | MFP3 | EMAC RMII Transmit Enable output pin. |
| | | | USCI1_DAT0 | I/O | MFP4 | USCI1 data 0 pin. |

| 64 Pin | 128 Pin | 144 Pin | Pin Name | Type | MFP | Description |
|---|---|---|---|---|---|---|
| | | | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | | | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | | | SD1_CMD | I/O | MFP7 | SD/SDIO1 command/response pin |
| | | | EBI_nCS0 | O | MFP8 | EBI chip select 0 output pin. |
| | | | BPWM1_CH4 | I/O | MFP10 | BPWM1 channel 4 output/capture input. |
| | | | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | | | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | | | INT5 | I | MFP13 | External interrupt 5 input pin. |
| | | | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | | | ACMP0_O | O | MFP15 | Analog comparator 0 output pin. |
| 1 | 128 | 144 | PB.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | | | EADC0_CH6 | A | MFP1 | EADC0 channel 6 analog input. |
| | | | EBI_nWRH | O | MFP2 | EBI high byte write enable output pin |
| | | | EMAC_PPS | O | MFP3 | EMAC Pulse Per Second output pin. |
| | | | USCI1_DAT1 | I/O | MFP4 | USCI1 data 1 pin. |
| | | | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | | | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | | | SD1_CLK | O | MFP7 | SD/SDIO1 clock output pin |
| | | | EBI_nCS1 | O | MFP8 | EBI chip select 1 output pin. |
| | | | BPWM1_CH5 | I/O | MFP10 | BPWM1 channel 5 output/capture input. |
| | | | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | | | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | | | INT4 | I | MFP13 | External interrupt 4 input pin. |
| | | | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | | | ACMP1_O | O | MFP15 | Analog comparator 1 output pin. |

### 4.2.7 M480 Multi-function Summary Table

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| ACMP0 | ACMP0_N | PB.3 | MFP1 | A | Analog comparator 0 negative input pin. |
| | ACMP0_O | PC.12 | MFP14 | O | Analog comparator 0 output pin. |
| | | PC.1 | MFP14 | O | |
| | | PB.7 | MFP15 | O | |
| | ACMP0_P0 | PA.11 | MFP1 | A | Analog comparator 0 positive input 0 pin. |
| | ACMP0_P1 | PB.2 | MFP1 | A | Analog comparator 0 positive input 1 pin. |
| | ACMP0_P2 | PB.12 | MFP1 | A | Analog comparator 0 positive input 2 pin. |
| | ACMP0_P3 | PB.13 | MFP1 | A | Analog comparator 0 positive input 3 pin. |
| | ACMP0_WLAT | PA.7 | MFP13 | I | Analog comparator 0 window latch input pin |
| ACMP1 | ACMP1_N | PB.5 | MFP1 | A | Analog comparator 1 negative input pin. |
| | ACMP1_O | PC.11 | MFP14 | O | Analog comparator 1 output pin. |
| | | PC.0 | MFP14 | O | |
| | | PB.6 | MFP15 | O | |
| | ACMP1_P0 | PA.10 | MFP1 | A | Analog comparator 1 positive input 0 pin. |
| | ACMP1_P1 | PB.4 | MFP1 | A | Analog comparator 1 positive input 1 pin. |
| | ACMP1_P2 | PB.12 | MFP1 | A | Analog comparator 1 positive input 2 pin. |
| | ACMP1_P3 | PB.13 | MFP1 | A | Analog comparator 1 positive input 3 pin. |
| | ACMP1_WLAT | PA.6 | MFP13 | I | Analog comparator 1 window latch input pin |
| BPWM0 | BPWM0_CH0 | PA.11 | MFP9 | I/O | BPWM0 channel 0 output/capture input. |
| | | PA.0 | MFP12 | I/O | |
| | | PG.14 | MFP12 | I/O | |
| | | PE.2 | MFP13 | I/O | |
| | BPWM0_CH1 | PA.10 | MFP9 | I/O | BPWM0 channel 1 output/capture input. |
| | | PA.1 | MFP12 | I/O | |
| | | PG.13 | MFP12 | I/O | |
| | | PE.3 | MFP13 | I/O | |
| | BPWM0_CH2 | PA.9 | MFP9 | I/O | BPWM0 channel 2 output/capture input. |
| | | PA.2 | MFP12 | I/O | |
| | | PG.12 | MFP12 | I/O | |
| | | PE.4 | MFP13 | I/O | |
| | BPWM0_CH3 | PA.8 | MFP9 | I/O | BPWM0 channel 3 output/capture input. |
| | | PA.3 | MFP12 | I/O | |
| | | PG.11 | MFP12 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PE.5 | MFP13 | I/O | |
| | BPWM0_CH4 | PC.13 | MFP9 | I/O | BPWM0 channel 4 output/capture input. |
| | | PF.5 | MFP8 | I/O | |
| | | PA.4 | MFP12 | I/O | |
| | | PG.10 | MFP12 | I/O | |
| | | PE.6 | MFP13 | I/O | |
| | BPWM0_CH5 | PD.12 | MFP9 | I/O | BPWM0 channel 5 output/capture input. |
| | | PF.4 | MFP8 | I/O | |
| | | PA.5 | MFP12 | I/O | |
| | | PG.9 | MFP12 | I/O | |
| | | PE.7 | MFP13 | I/O | |
| BPWM1 | BPWM1_CH0 | PF.3 | MFP11 | I/O | BPWM1 channel 0 output/capture input. |
| | | PC.7 | MFP12 | I/O | |
| | | PF.0 | MFP12 | I/O | |
| | | PB.11 | MFP10 | I/O | |
| | BPWM1_CH1 | PF.2 | MFP11 | I/O | BPWM1 channel 1 output/capture input. |
| | | PC.6 | MFP12 | I/O | |
| | | PF.1 | MFP12 | I/O | |
| | | PB.10 | MFP10 | I/O | |
| | BPWM1_CH2 | PA.7 | MFP12 | I/O | BPWM1 channel 2 output/capture input. |
| | | PA.12 | MFP11 | I/O | |
| | | PB.9 | MFP10 | I/O | |
| | BPWM1_CH3 | PA.6 | MFP12 | I/O | BPWM1 channel 3 output/capture input. |
| | | PA.13 | MFP11 | I/O | |
| | | PB.8 | MFP10 | I/O | |
| | BPWM1_CH4 | PC.8 | MFP12 | I/O | BPWM1 channel 4 output/capture input. |
| | | PA.14 | MFP11 | I/O | |
| | | PB.7 | MFP10 | I/O | |
| | BPWM1_CH5 | PE.13 | MFP12 | I/O | BPWM1 channel 5 output/capture input. |
| | | PA.15 | MFP11 | I/O | |
| | | PB.6 | MFP10 | I/O | |
| CAN0 | CAN0_RXD | PD.10 | MFP4 | I | CAN0 bus receiver input. |
| | | PA.4 | MFP10 | I | |
| | | PE.15 | MFP4 | I | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PC.4 | MFP10 | I | |
| | | PA.13 | MFP6 | I | |
| | | PB.10 | MFP8 | I | |
| | CAN0_TXD | PD.11 | MFP4 | O | CAN0 bus transmitter output. |
| | | PA.5 | MFP10 | O | |
| | | PE.14 | MFP4 | O | |
| | | PC.5 | MFP10 | O | |
| | | PA.12 | MFP6 | O | |
| | | PB.11 | MFP8 | O | |
| CAN1 | CAN1_RXD | PC.9 | MFP9 | I | CAN1 bus receiver input. |
| | | PD.12 | MFP5 | I | |
| | | PG.1 | MFP7 | I | |
| | | PC.2 | MFP10 | I | |
| | | PE.6 | MFP9 | I | |
| | | PB.6 | MFP5 | I | |
| | CAN1_TXD | PC.10 | MFP9 | O | CAN1 bus transmitter output. |
| | | PC.13 | MFP5 | O | |
| | | PG.0 | MFP7 | O | |
| | | PC.3 | MFP10 | O | |
| | | PE.7 | MFP9 | O | |
| | | PB.7 | MFP5 | O | |
| CLKO | CLKO | PC.13 | MFP13 | O | Clock Out |
| | | PD.12 | MFP13 | O | |
| | | PG.15 | MFP14 | O | |
| | | PB.14 | MFP14 | O | |
| DAC0 | DAC0_OUT | PB.12 | MFP1 | A | DAC0 channel analog output. |
| | DAC0_ST | PA.10 | MFP14 | I | DAC0 external trigger input. |
| | | PA.0 | MFP15 | I | |
| DAC1 | DAC1_OUT | PB.13 | MFP1 | A | DAC1 channel analog output. |
| | DAC1_ST | PA.11 | MFP14 | I | DAC1 external trigger input. |
| | | PA.1 | MFP15 | I | |
| EADC0 | EADC0_CH0 | PB.0 | MFP1 | A | EADC0 channel 0 analog input. |
| | EADC0_CH1 | PB.1 | MFP1 | A | EADC0 channel 1 analog input. |
| | EADC0_CH2 | PB.2 | MFP1 | A | EADC0 channel 2 analog input. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | EADC0_CH3 | PB.3 | MFP1 | A | EADC0 channel 3 analog input. |
| | EADC0_CH4 | PB.4 | MFP1 | A | EADC0 channel 4 analog input. |
| | EADC0_CH5 | PB.5 | MFP1 | A | EADC0 channel 5 analog input. |
| | EADC0_CH6 | PB.6 | MFP1 | A | EADC0 channel 6 analog input. |
| | EADC0_CH7 | PB.7 | MFP1 | A | EADC0 channel 7 analog input. |
| | EADC0_CH8 | PB.8 | MFP1 | A | EADC0 channel 8 analog input. |
| | EADC0_CH9 | PB.9 | MFP1 | A | EADC0 channel 9 analog input. |
| | EADC0_CH10 | PB.10 | MFP1 | A | EADC0 channel 10 analog input. |
| | EADC0_CH11 | PB.11 | MFP1 | A | EADC0 channel 11 analog input. |
| | EADC0_CH12 | PB.12 | MFP1 | A | EADC0 channel 12 analog input. |
| | EADC0_CH13 | PB.13 | MFP1 | A | EADC0 channel 13 analog input. |
| | EADC0_CH14 | PB.14 | MFP1 | A | EADC0 channel 14 analog input. |
| | EADC0_CH15 | PB.15 | MFP1 | A | EADC0 channel 15 analog input. |
| | EADC0_ST | PC.13 | MFP14 | I | EADC0 external trigger input. |
| | | PD.12 | MFP14 | I | |
| | | PF.5 | MFP11 | I | |
| | | PG.15 | MFP15 | I | |
| EBI | EBI_AD0 | PC.0 | MFP2 | I/O | EBI address/data bus bit 0. |
| | | PG.9 | MFP2 | I/O | |
| | EBI_AD1 | PC.1 | MFP2 | I/O | EBI address/data bus bit 1. |
| | | PG.10 | MFP2 | I/O | |
| | EBI_AD2 | PC.2 | MFP2 | I/O | EBI address/data bus bit 2. |
| | | PG.11 | MFP2 | I/O | |
| | EBI_AD3 | PC.3 | MFP2 | I/O | EBI address/data bus bit 3. |
| | | PG.12 | MFP2 | I/O | |
| | EBI_AD4 | PC.4 | MFP2 | I/O | EBI address/data bus bit 4. |
| | | PG.13 | MFP2 | I/O | |
| | EBI_AD5 | PC.5 | MFP2 | I/O | EBI address/data bus bit 5. |
| | | PG.14 | MFP2 | I/O | |
| | EBI_AD6 | PA.6 | MFP2 | I/O | EBI address/data bus bit 6. |
| | | PD.8 | MFP2 | I/O | |
| | EBI_AD7 | PA.7 | MFP2 | I/O | EBI address/data bus bit 7. |
| | | PD.9 | MFP2 | I/O | |
| | EBI_AD8 | PC.6 | MFP2 | I/O | EBI address/data bus bit 8. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PE.14 | MFP2 | I/O | |
| | EBI_AD9 | PC.7 | MFP2 | I/O | EBI address/data bus bit 9. |
| | | PE.15 | MFP2 | I/O | |
| | EBI_AD10 | PD.3 | MFP2 | I/O | EBI address/data bus bit 10. |
| | | PD.13 | MFP2 | I/O | |
| | | PE.1 | MFP2 | I/O | |
| | EBI_AD11 | PD.2 | MFP2 | I/O | EBI address/data bus bit 11. |
| | | PE.0 | MFP2 | I/O | |
| | | PC.14 | MFP2 | I/O | |
| | EBI_AD12 | PD.1 | MFP2 | I/O | EBI address/data bus bit 12. |
| | | PH.8 | MFP2 | I/O | |
| | | PB.15 | MFP2 | I/O | |
| | EBI_AD13 | PD.0 | MFP2 | I/O | EBI address/data bus bit 13. |
| | | PH.9 | MFP2 | I/O | |
| | | PB.14 | MFP2 | I/O | |
| | EBI_AD14 | PH.10 | MFP2 | I/O | EBI address/data bus bit 14. |
| | | PB.13 | MFP2 | I/O | |
| | EBI_AD15 | PH.11 | MFP2 | I/O | EBI address/data bus bit 15. |
| | | PB.12 | MFP2 | I/O | |
| | EBI_ADR0 | PB.5 | MFP2 | O | EBI address bus bit 0. |
| | | PH.7 | MFP2 | O | |
| | EBI_ADR1 | PB.4 | MFP2 | O | EBI address bus bit 1. |
| | | PH.6 | MFP2 | O | |
| | EBI_ADR2 | PB.3 | MFP2 | O | EBI address bus bit 2. |
| | | PH.5 | MFP2 | O | |
| | EBI_ADR3 | PB.2 | MFP2 | O | EBI address bus bit 3. |
| | | PH.4 | MFP2 | O | |
| | EBI_ADR4 | PC.12 | MFP2 | O | EBI address bus bit 4. |
| | | PH.3 | MFP2 | O | |
| | EBI_ADR5 | PC.11 | MFP2 | O | EBI address bus bit 5. |
| | | PH.2 | MFP2 | O | |
| | EBI_ADR6 | PC.10 | MFP2 | O | EBI address bus bit 6. |
| | | PH.1 | MFP2 | O | |
| | EBI_ADR7 | PC.9 | MFP2 | O | EBI address bus bit 7. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PH.0 | MFP2 | O | |
| | EBI_ADR8 | PB.1 | MFP2 | O | EBI address bus bit 8. |
| | | PG.0 | MFP2 | O | |
| | EBI_ADR9 | PB.0 | MFP2 | O | EBI address bus bit 9. |
| | | PG.1 | MFP2 | O | |
| | EBI_ADR10 | PC.13 | MFP2 | O | EBI address bus bit 10. |
| | | PE.8 | MFP2 | O | |
| | EBI_ADR11 | PG.2 | MFP2 | O | EBI address bus bit 11. |
| | | PE.9 | MFP2 | O | |
| | EBI_ADR12 | PG.3 | MFP2 | O | EBI address bus bit 12. |
| | | PE.10 | MFP2 | O | |
| | EBI_ADR13 | PG.4 | MFP2 | O | EBI address bus bit 13. |
| | | PE.11 | MFP2 | O | |
| | EBI_ADR14 | PF.11 | MFP2 | O | EBI address bus bit 14. |
| | | PE.12 | MFP2 | O | |
| | EBI_ADR15 | PF.10 | MFP2 | O | EBI address bus bit 15. |
| | | PE.13 | MFP2 | O | |
| | EBI_ADR16 | PF.9 | MFP2 | O | EBI address bus bit 16. |
| | | PC.8 | MFP2 | O | |
| | | PB.11 | MFP2 | O | |
| | EBI_ADR17 | PF.8 | MFP2 | O | EBI address bus bit 17. |
| | | PB.10 | MFP2 | O | |
| | EBI_ADR18 | PF.7 | MFP2 | O | EBI address bus bit 18. |
| | | PB.9 | MFP2 | O | |
| | EBI_ADR19 | PF.6 | MFP2 | O | EBI address bus bit 19. |
| | | PB.8 | MFP2 | O | |
| | EBI_ALE | PA.8 | MFP2 | O | EBI address latch enable output pin. |
| | | PE.2 | MFP2 | O | |
| | EBI_MCLK | PA.9 | MFP2 | O | EBI external clock output pin. |
| | | PE.3 | MFP2 | O | |
| | EBI_nCS0 | PD.12 | MFP2 | O | EBI chip select 0 output pin. |
| | | PF.6 | MFP7 | O | |
| | | PF.3 | MFP2 | O | |
| | | PD.14 | MFP2 | O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PB.7 | MFP8 | O | |
| | EBI_nCS1 | PD.11 | MFP2 | O | EBI chip select 1 output pin. |
| | | PF.2 | MFP2 | O | |
| | | PG.5 | MFP2 | O | |
| | | PB.6 | MFP8 | O | |
| | EBI_nCS2 | PD.10 | MFP2 | O | EBI chip select 2 output pin. |
| | | PG.6 | MFP2 | O | |
| | EBI_nRD | PA.11 | MFP2 | O | EBI read enable output pin. |
| | | PE.5 | MFP2 | O | |
| | EBI_nWR | PA.10 | MFP2 | O | EBI write enable output pin. |
| | | PE.4 | MFP2 | O | |
| | EBI_nWRH | PG.8 | MFP2 | O | EBI high byte write enable output pin |
| | | PB.6 | MFP2 | O | |
| | EBI_nWRL | PG.7 | MFP2 | O | EBI low byte write enable output pin. |
| | | PB.7 | MFP2 | O | |
| ECAP0 | ECAP0_IC0 | PA.10 | MFP11 | I | Enhanced capture unit 0 input 0 pin. |
| | | PE.8 | MFP12 | I | |
| | ECAP0_IC1 | PA.9 | MFP11 | I | Enhanced capture unit 0 input 1 pin. |
| | | PE.9 | MFP12 | I | |
| | ECAP0_IC2 | PA.8 | MFP11 | I | Enhanced capture unit 0 input 2 pin. |
| | | PE.10 | MFP12 | I | |
| ECAP1 | ECAP1_IC0 | PC.10 | MFP11 | I | Enhanced capture unit 1 input 0 pin. |
| | | PE.13 | MFP13 | I | |
| | ECAP1_IC1 | PC.11 | MFP11 | I | Enhanced capture unit 1 input 1 pin. |
| | | PE.12 | MFP13 | I | |
| | ECAP1_IC2 | PC.12 | MFP11 | I | Enhanced capture unit 1 input 2 pin. |
| | | PE.11 | MFP13 | I | |
| EMAC | EMAC_RMII_MDC | PE.8 | MFP3 | O | EMAC RMII PHY Management Clock output pin. |
| | | PB.11 | MFP3 | O | |
| | EMAC_RMII_MDIO | PE.9 | MFP3 | I/O | EMAC RMII PHY Management Data pin. |
| | | PB.10 | MFP3 | I/O | |
| | EMAC_RMII_RXD0 | PB.4 | MFP4 | I | EMAC RMII Receive Data bus bit 0. |
| | | PC.7 | MFP3 | I | |
| | EMAC_RMII_RXD1 | PB.3 | MFP4 | I | EMAC RMII Receive Data bus bit 1. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PC.6 | MFP3 | I | |
| | EMAC_RMII_CRSDV | PB.2 | MFP4 | I | EMAC RMII Carrier Sense/Receive Data input pin. |
| | | PA.7 | MFP3 | I | |
| | EMAC_RMII_RXERR | PB.1 | MFP4 | I | EMAC RMII Receive Data Error input pin. |
| | | PA.6 | MFP3 | I | |
| | EMAC_RMII_TXD0 | PE.10 | MFP3 | O | EMAC RMII Transmit Data bus bit 0. |
| | | PB.9 | MFP3 | O | |
| | EMAC_RMII_TXD1 | PE.11 | MFP3 | O | EMAC RMII Transmit Data bus bit 1. |
| | | PB.8 | MFP3 | O | |
| | EMAC_RMII_TXEN | PE.12 | MFP3 | O | EMAC RMII Transmit Enable output pin. |
| | | PB.7 | MFP3 | O | |
| | EMAC_PPS | PE.13 | MFP3 | O | EMAC Pulse Per Second output pin. |
| | | PB.6 | MFP3 | O | |
| | EMAC_RMII_REFCLK | PB.5 | MFP4 | I | EMAC RMII reference clock input pin. |
| | | PC.8 | MFP3 | I | |
| EPWM0 | EPWM0_BRAKE0 | PB.1 | MFP13 | I | EPWM0 Brake 0 input pin. |
| | | PE.8 | MFP11 | I | |
| | EPWM0_BRAKE1 | PB.0 | MFP13 | I | EPWM0 Brake 1 input pin. |
| | | PE.9 | MFP11 | I | |
| | EPWM0_CH0 | PB.5 | MFP11 | I/O | EPWM0 channel 0 output/capture input. |
| | | PE.8 | MFP10 | I/O | |
| | | PA.5 | MFP13 | I/O | |
| | | PE.7 | MFP12 | I/O | |
| | | PG.8 | MFP11 | I/O | |
| | EPWM0_CH1 | PB.4 | MFP11 | I/O | EPWM0 channel 1 output/capture input. |
| | | PE.9 | MFP10 | I/O | |
| | | PA.4 | MFP13 | I/O | |
| | | PE.6 | MFP12 | I/O | |
| | | PG.7 | MFP11 | I/O | |
| | EPWM0_CH2 | PB.3 | MFP11 | I/O | EPWM0 channel 2 output/capture input. |
| | | PE.10 | MFP10 | I/O | |
| | | PA.3 | MFP13 | I/O | |
| | | PE.5 | MFP12 | I/O | |
| | | PG.6 | MFP11 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | EPWM0_CH3 | PB.2 | MFP11 | I/O | EPWM0 channel 3 output/capture input. |
| | | PE.11 | MFP10 | I/O | |
| | | PA.2 | MFP13 | I/O | |
| | | PE.4 | MFP12 | I/O | |
| | | PG.5 | MFP11 | I/O | |
| | EPWM0_CH4 | PB.1 | MFP11 | I/O | EPWM0 channel 4 output/capture input. |
| | | PE.12 | MFP10 | I/O | |
| | | PA.1 | MFP13 | I/O | |
| | | PE.3 | MFP12 | I/O | |
| | | PD.14 | MFP11 | I/O | |
| | EPWM0_CH5 | PB.0 | MFP11 | I/O | EPWM0 channel 5 output/capture input. |
| | | PE.13 | MFP10 | I/O | |
| | | PA.0 | MFP13 | I/O | |
| | | PE.2 | MFP12 | I/O | |
| | | PH.11 | MFP11 | I/O | |
| | EPWM0_SYNC_IN | PA.15 | MFP12 | I | EPWM0 counter synchronous trigger input pin. |
| | | PC.14 | MFP11 | I | |
| | EPWM0_SYNC_OUT | PA.11 | MFP10 | O | EPWM0 counter synchronous trigger output pin. |
| | | PF.5 | MFP9 | O | |
| EPWM1 | EPWM1_BRAKE0 | PE.10 | MFP11 | I | EPWM1 Brake 0 input pin. |
| | | PB.7 | MFP11 | I | |
| | EPWM1_BRAKE1 | PE.11 | MFP11 | I | EPWM1 Brake 1 input pin. |
| | | PB.6 | MFP11 | I | |
| | EPWM1_CH0 | PC.12 | MFP12 | I/O | EPWM1 channel 0 output/capture input. |
| | | PE.13 | MFP11 | I/O | |
| | | PC.5 | MFP12 | I/O | |
| | | PB.15 | MFP11 | I/O | |
| | EPWM1_CH1 | PC.11 | MFP12 | I/O | EPWM1 channel 1 output/capture input. |
| | | PC.8 | MFP11 | I/O | |
| | | PC.4 | MFP12 | I/O | |
| | | PB.14 | MFP11 | I/O | |
| | EPWM1_CH2 | PC.10 | MFP12 | I/O | EPWM1 channel 2 output/capture input. |
| | | PC.7 | MFP11 | I/O | |
| | | PC.3 | MFP12 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PB.13 | MFP11 | I/O | |
| | EPWM1_CH3 | PC.9 | MFP12 | I/O | EPWM1 channel 3 output/capture input. |
| | | PC.6 | MFP11 | I/O | |
| | | PC.2 | MFP12 | I/O | |
| | | PB.12 | MFP11 | I/O | |
| | EPWM1_CH4 | PB.1 | MFP12 | I/O | EPWM1 channel 4 output/capture input. |
| | | PA.7 | MFP11 | I/O | |
| | | PC.1 | MFP12 | I/O | |
| | | PB.7 | MFP12 | I/O | |
| | EPWM1_CH5 | PB.0 | MFP12 | I/O | EPWM1 channel 5 output/capture input. |
| | | PA.6 | MFP11 | I/O | |
| | | PC.0 | MFP12 | I/O | |
| | | PB.6 | MFP12 | I/O | |
| HSUSB | HSUSB_VBUS_EN | PB.15 | MFP15 | O | HSUSB external VBUS regulator enable pin. |
| | | PB.10 | MFP14 | O | |
| | HSUSB_VBUS_ST | PC.14 | MFP15 | I | HSUSB external VBUS regulator status pin. |
| | | PB.11 | MFP14 | I | |
| I2C0 | I2C0_SCL | PB.5 | MFP6 | I/O | I2C0 clock pin. |
| | | PC.12 | MFP4 | I/O | |
| | | PG.0 | MFP4 | I/O | |
| | | PH.2 | MFP6 | I/O | |
| | | PF.3 | MFP4 | I/O | |
| | | PE.13 | MFP4 | I/O | |
| | | PA.5 | MFP9 | I/O | |
| | | PC.1 | MFP9 | I/O | |
| | | PD.7 | MFP4 | I/O | |
| | I2C0_SDA | PB.4 | MFP6 | I/O | I2C0 data input/output pin. |
| | | PC.11 | MFP4 | I/O | |
| | | PG.1 | MFP4 | I/O | |
| | | PH.3 | MFP6 | I/O | |
| | | PF.2 | MFP4 | I/O | |
| | | PC.8 | MFP4 | I/O | |
| | | PA.4 | MFP9 | I/O | |
| | | PC.0 | MFP9 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PD.6 | MFP4 | I/O | |
| | I2C0_SMBAL | PG.2 | MFP4 | O | I2C0 SMBus SMBALTER pin |
| | | PC.3 | MFP9 | O | |
| | I2C0_SMBSUS | PG.3 | MFP4 | O | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | PC.2 | MFP9 | O | |
| I2C1 | I2C1_SCL | PB.1 | MFP9 | I/O | I2C1 clock pin. |
| | | PG.2 | MFP5 | I/O | |
| | | PA.7 | MFP8 | I/O | |
| | | PA.3 | MFP9 | I/O | |
| | | PF.0 | MFP3 | I/O | |
| | | PC.5 | MFP9 | I/O | |
| | | PD.5 | MFP4 | I/O | |
| | | PA.12 | MFP4 | I/O | |
| | | PE.1 | MFP8 | I/O | |
| | | PB.11 | MFP7 | I/O | |
| | I2C1_SDA | PB.0 | MFP9 | I/O | I2C1 data input/output pin. |
| | | PG.3 | MFP5 | I/O | |
| | | PA.6 | MFP8 | I/O | |
| | | PA.2 | MFP9 | I/O | |
| | | PF.1 | MFP3 | I/O | |
| | | PC.4 | MFP9 | I/O | |
| | | PD.4 | MFP4 | I/O | |
| | | PA.13 | MFP4 | I/O | |
| | | PE.0 | MFP8 | I/O | |
| | | PB.10 | MFP7 | I/O | |
| | I2C1_SMBAL | PG.0 | MFP5 | O | I2C1 SMBus SMBALTER pin |
| | | PC.7 | MFP8 | O | |
| | | PH.8 | MFP8 | O | |
| | | PB.9 | MFP7 | O | |
| | I2C1_SMBSUS | PG.1 | MFP5 | O | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | | PC.6 | MFP8 | O | |
| | | PH.9 | MFP8 | O | |
| | | PB.8 | MFP7 | O | |
| I2C2 | I2C2_SCL | PA.11 | MFP7 | I/O | I2C2 clock pin. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PA.1 | MFP9 | I/O | |
| | | PD.9 | MFP3 | I/O | |
| | | PD.1 | MFP6 | I/O | |
| | | PA.14 | MFP6 | I/O | |
| | | PH.8 | MFP9 | I/O | |
| | | PB.13 | MFP8 | I/O | |
| | I2C2_SDA | PA.10 | MFP7 | I/O | I2C2 data input/output pin. |
| | | PA.0 | MFP9 | I/O | |
| | | PD.8 | MFP3 | I/O | |
| | | PD.0 | MFP6 | I/O | |
| | | PA.15 | MFP6 | I/O | |
| | | PH.9 | MFP9 | I/O | |
| | | PB.12 | MFP8 | I/O | |
| | I2C2_SMBAL | PB.15 | MFP8 | O | I2C2 SMBus SMBALTER pin |
| | I2C2_SMBSUS | PB.14 | MFP8 | O | I2C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
| I2S0 | I2S0_BCLK | PB.5 | MFP10 | O | I2S0 bit clock output pin. |
| | | PF.10 | MFP4 | O | |
| | | PE.8 | MFP4 | O | |
| | | PC.4 | MFP6 | O | |
| | | PA.12 | MFP2 | O | |
| | | PE.1 | MFP5 | O | |
| | I2S0_DI | PB.3 | MFP10 | I | I2S0 data input pin. |
| | | PF.8 | MFP4 | I | |
| | | PE.10 | MFP4 | I | |
| | | PC.2 | MFP6 | I | |
| | | PA.14 | MFP2 | I | |
| | | PH.8 | MFP5 | I | |
| | I2S0_DO | PB.2 | MFP10 | O | I2S0 data output pin. |
| | | PF.7 | MFP4 | O | |
| | | PE.11 | MFP4 | O | |
| | | PC.1 | MFP6 | O | |
| | | PA.15 | MFP2 | O | |
| | | PH.9 | MFP5 | O | |
| | I2S0_LRCK | PB.1 | MFP10 | O | I2S0 left right channel clock output pin. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PF.6 | MFP4 | O | |
| | | PE.12 | MFP4 | O | |
| | | PC.0 | MFP6 | O | |
| | | PH.10 | MFP5 | O | |
| | I2S0_MCLK | PB.4 | MFP10 | O | I2S0 master clock output pin. |
| | | PF.9 | MFP4 | O | |
| | | PE.9 | MFP4 | O | |
| | | PC.3 | MFP6 | O | |
| | | PA.13 | MFP2 | O | |
| | | PE.0 | MFP5 | O | |
| ICE | ICE_CLK | PF.1 | MFP14 | I | Serial wired debugger clock pin. |
| | ICE_DAT | PF.0 | MFP14 | O | Serial wired debugger data pin. |
| INT0 | INT0 | PB.5 | MFP15 | I | External interrupt 0 input pin. |
| | | PA.6 | MFP15 | I | |
| INT1 | INT1 | PB.4 | MFP15 | I | External interrupt 1 input pin. |
| | | PA.7 | MFP15 | I | |
| INT2 | INT2 | PB.3 | MFP15 | I | External interrupt 2 input pin. |
| | | PC.6 | MFP15 | I | |
| INT3 | INT3 | PB.2 | MFP15 | I | External interrupt 3 input pin. |
| | | PC.7 | MFP15 | I | |
| INT4 | INT4 | PA.8 | MFP15 | I | External interrupt 4 input pin. |
| | | PB.6 | MFP13 | I | |
| INT5 | INT5 | PD.12 | MFP15 | I | External interrupt 5 input pin. |
| | | PB.7 | MFP13 | I | |
| INT6 | INT6 | PD.11 | MFP15 | I | External interrupt 6 input pin. |
| | | PB.8 | MFP13 | I | |
| INT7 | INT7 | PD.10 | MFP15 | I | External interrupt 7 input pin. |
| | | PB.9 | MFP13 | I | |
| OPA0 | OPA0_N | PB.1 | MFP1 | A | Operational amplifier 0 negative input pin. |
| | OPA0_O | PB.2 | MFP1 | A | Operational amplifier 0 output pin. |
| | OPA0_P | PB.0 | MFP1 | A | Operational amplifier 0 positive input pin. |
| OPA1 | OPA1_N | PA.9 | MFP1 | A | Operational amplifier 1 negative input pin. |
| | OPA1_O | PA.10 | MFP1 | A | Operational amplifier 1 output pin. |
| | OPA1_P | PA.8 | MFP1 | A | Operational amplifier 1 positive input pin. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| OPA2 | OPA2_N | PD.11 | MFP1 | A | Operational amplifier 2 negative input pin. |
| | OPA2_O | PD.12 | MFP1 | A | Operational amplifier 2 output pin. |
| | OPA2_P | PD.10 | MFP1 | A | Operational amplifier 2 positive input pin. |
| QEI0 | QEI0_A | PD.11 | MFP10 | I | Quadrature encoder 0 phase A input |
| | | PA.4 | MFP14 | I | |
| | | PE.3 | MFP11 | I | |
| | QEI0_B | PD.10 | MFP10 | I | Quadrature encoder 0 phase B input |
| | | PA.3 | MFP14 | I | |
| | | PE.2 | MFP11 | I | |
| | QEI0_INDEX | PD.12 | MFP10 | I | Quadrature encoder 0 index input |
| | | PA.5 | MFP14 | I | |
| | | PE.4 | MFP11 | I | |
| QEI1 | QEI1_A | PA.9 | MFP10 | I | Quadrature encoder 1 phase A input |
| | | PA.13 | MFP12 | I | |
| | | PE.6 | MFP11 | I | |
| | QEI1_B | PA.8 | MFP10 | I | Quadrature encoder 1 phase B input |
| | | PA.14 | MFP12 | I | |
| | | PE.5 | MFP11 | I | |
| | QEI1_INDEX | PA.10 | MFP10 | I | Quadrature encoder 1 index input |
| | | PA.12 | MFP12 | I | |
| | | PE.7 | MFP11 | I | |
| QSPI0 | QSPI0_CLK | PF.2 | MFP5 | I/O | Quad SPI0 serial clock pin. |
| | | PA.2 | MFP3 | I/O | |
| | | PC.2 | MFP4 | I/O | |
| | | PH.8 | MFP3 | I/O | |
| | | PC.14 | MFP6 | I/O | |
| | QSPI0_MISO0 | PA.1 | MFP3 | I/O | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | | PC.1 | MFP4 | I/O | |
| | | PE.1 | MFP3 | I/O | |
| | QSPI0_MISO1 | PA.5 | MFP3 | I/O | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | | PC.5 | MFP4 | I/O | |
| | | PH.10 | MFP3 | I/O | |
| | QSPI0_MOSI0 | PA.0 | MFP3 | I/O | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | | PC.0 | MFP4 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PE.0 | MFP3 | I/O | |
| | QSPI0_MOSI1 | PA.4 | MFP3 | I/O | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | PC.4 | MFP4 | I/O | |
| | | PH.11 | MFP3 | I/O | |
| | QSPI0_SS | PA.3 | MFP3 | I/O | Quad SPI0 slave select pin. |
| | | PC.3 | MFP4 | I/O | |
| | | PH.9 | MFP3 | I/O | |
| SC0 | SC0_CLK | PB.5 | MFP9 | O | Smart Card 0 clock pin. |
| | | PF.6 | MFP3 | O | |
| | | PA.0 | MFP6 | O | |
| | | PE.2 | MFP6 | O | |
| | SC0_DAT | PB.4 | MFP9 | I/O | Smart Card 0 data pin. |
| | | PF.7 | MFP3 | I/O | |
| | | PA.1 | MFP6 | I/O | |
| | | PE.3 | MFP6 | I/O | |
| | SC0_PWR | PB.2 | MFP9 | O | Smart Card 0 power pin. |
| | | PF.9 | MFP3 | O | |
| | | PA.3 | MFP6 | O | |
| | | PE.5 | MFP6 | O | |
| | SC0_RST | PB.3 | MFP9 | O | Smart Card 0 reset pin. |
| | | PF.8 | MFP3 | O | |
| | | PA.2 | MFP6 | O | |
| | | PE.4 | MFP6 | O | |
| | SC0_nCD | PC.12 | MFP9 | I | Smart Card 0 card detect pin. |
| | | PF.10 | MFP3 | I | |
| | | PA.4 | MFP6 | I | |
| | | PE.6 | MFP6 | I | |
| SC1 | SC1_CLK | PC.0 | MFP5 | O | Smart Card 1 clock pin. |
| | | PD.4 | MFP8 | O | |
| | | PG.8 | MFP4 | O | |
| | | PB.12 | MFP3 | O | |
| | SC1_DAT | PC.1 | MFP5 | I/O | Smart Card 1 data pin. |
| | | PD.5 | MFP8 | I/O | |
| | | PG.7 | MFP4 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PB.13 | MFP3 | I/O | |
| | SC1_PWR | PC.3 | MFP5 | O | Smart Card 1 power pin. |
| | | PD.7 | MFP8 | O | |
| | | PG.5 | MFP4 | O | |
| | | PB.15 | MFP3 | O | |
| | SC1_RST | PC.2 | MFP5 | O | Smart Card 1 reset pin. |
| | | PD.6 | MFP8 | O | |
| | | PG.6 | MFP4 | O | |
| | | PB.14 | MFP3 | O | |
| | SC1_nCD | PC.4 | MFP5 | I | Smart Card 1 card detect pin. |
| | | PD.3 | MFP8 | I | |
| | | PD.14 | MFP4 | I | |
| | | PC.14 | MFP3 | I | |
| SC2 | SC2_CLK | PA.8 | MFP3 | O | Smart Card 2 clock pin. |
| | | PA.6 | MFP6 | O | |
| | | PD.0 | MFP7 | O | |
| | | PA.15 | MFP7 | O | |
| | | PE.0 | MFP4 | O | |
| | SC2_DAT | PA.9 | MFP3 | I/O | Smart Card 2 data pin. |
| | | PA.7 | MFP6 | I/O | |
| | | PD.1 | MFP7 | I/O | |
| | | PA.14 | MFP7 | I/O | |
| | | PE.1 | MFP4 | I/O | |
| | SC2_PWR | PA.11 | MFP3 | O | Smart Card 2 power pin. |
| | | PC.7 | MFP6 | O | |
| | | PD.3 | MFP7 | O | |
| | | PA.12 | MFP7 | O | |
| | | PH.8 | MFP4 | O | |
| | SC2_RST | PA.10 | MFP3 | O | Smart Card 2 reset pin. |
| | | PC.6 | MFP6 | O | |
| | | PD.2 | MFP7 | O | |
| | | PA.13 | MFP7 | O | |
| | | PH.9 | MFP4 | O | |
| | SC2_nCD | PC.13 | MFP3 | I | Smart Card 2 card detect pin. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PA.5 | MFP6 | I | |
| | | PD.13 | MFP7 | I | |
| | | PH.10 | MFP4 | I | |
| SD0 | SD0_CLK | PB.1 | MFP3 | O | SD/SDIO0 clock output pin |
| | | PE.6 | MFP3 | O | |
| | SD0_CMD | PB.0 | MFP3 | I/O | SD/SDIO0 command/response pin |
| | | PE.7 | MFP3 | I/O | |
| | SD0_DAT0 | PB.2 | MFP3 | I/O | SD/SDIO0 data line bit 0. |
| | | PE.2 | MFP3 | I/O | |
| | SD0_DAT1 | PB.3 | MFP3 | I/O | SD/SDIO0 data line bit 1. |
| | | PE.3 | MFP3 | I/O | |
| | SD0_DAT2 | PB.4 | MFP3 | I/O | SD/SDIO0 data line bit 2. |
| | | PE.4 | MFP3 | I/O | |
| | SD0_DAT3 | PB.5 | MFP3 | I/O | SD/SDIO0 data line bit 3. |
| | | PE.5 | MFP3 | I/O | |
| | SD0_nCD | PD.13 | MFP3 | I | SD/SDIO0 card detect input pin |
| | | PB.12 | MFP9 | I | |
| SD1 | SD1_CLK | PA.4 | MFP5 | O | SD/SDIO1 clock output pin |
| | | PG.14 | MFP3 | O | |
| | | PB.6 | MFP7 | O | |
| | SD1_CMD | PA.5 | MFP5 | I/O | SD/SDIO1 command/response pin |
| | | PG.13 | MFP3 | I/O | |
| | | PB.7 | MFP7 | I/O | |
| | SD1_DAT0 | PA.8 | MFP5 | I/O | SD/SDIO1 data line bit 0. |
| | | PA.0 | MFP5 | I/O | |
| | | PG.12 | MFP3 | I/O | |
| | SD1_DAT1 | PA.9 | MFP5 | I/O | SD/SDIO1 data line bit 1. |
| | | PA.1 | MFP5 | I/O | |
| | | PG.11 | MFP3 | I/O | |
| | SD1_DAT2 | PA.10 | MFP5 | I/O | SD/SDIO1 data line bit 2. |
| | | PA.2 | MFP5 | I/O | |
| | | PG.10 | MFP3 | I/O | |
| | SD1_DAT3 | PA.11 | MFP5 | I/O | SD/SDIO1 data line bit 3. |
| | | PA.3 | MFP5 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PG.9 | MFP3 | I/O | |
| | SD1_nCD | PA.6 | MFP5 | I | SD/SDIO1 card detect input pin |
| | | PE.14 | MFP5 | I | |
| | | PG.15 | MFP3 | I | |
| SPI0 | SPI0_CLK | PF.8 | MFP5 | I/O | SPI0 serial clock pin. |
| | | PA.2 | MFP4 | I/O | |
| | | PD.2 | MFP4 | I/O | |
| | | PB.14 | MFP4 | I/O | |
| | SPI0_I2SMCLK | PB.0 | MFP8 | I/O | SPI0 I2S master clock output pin |
| | | PF.10 | MFP5 | I/O | |
| | | PA.4 | MFP4 | I/O | |
| | | PD.13 | MFP4 | I/O | |
| | | PC.14 | MFP4 | I/O | |
| | | PB.11 | MFP9 | I/O | |
| | SPI0_MISO | PF.7 | MFP5 | I/O | SPI0 MISO (Master In, Slave Out) pin. |
| | | PA.1 | MFP4 | I/O | |
| | | PD.1 | MFP4 | I/O | |
| | | PB.13 | MFP4 | I/O | |
| | SPI0_MOSI | PF.6 | MFP5 | I/O | SPI0 MOSI (Master Out, Slave In) pin. |
| | | PA.0 | MFP4 | I/O | |
| | | PD.0 | MFP4 | I/O | |
| | | PB.12 | MFP4 | I/O | |
| | SPI0_SS | PF.9 | MFP5 | I/O | SPI0 slave select pin. |
| | | PA.3 | MFP4 | I/O | |
| | | PD.3 | MFP4 | I/O | |
| | | PB.15 | MFP4 | I/O | |
| SPI1 | SPI1_CLK | PB.3 | MFP5 | I/O | SPI1 serial clock pin. |
| | | PH.6 | MFP3 | I/O | |
| | | PA.7 | MFP4 | I/O | |
| | | PC.1 | MFP7 | I/O | |
| | | PD.5 | MFP5 | I/O | |
| | | PH.8 | MFP6 | I/O | |
| | SPI1_I2SMCLK | PB.1 | MFP5 | I/O | SPI1 I2S master clock output pin |
| | | PH.3 | MFP3 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PA.5 | MFP4 | I/O | |
| | | PC.4 | MFP7 | I/O | |
| | | PD.13 | MFP5 | I/O | |
| | | PH.10 | MFP6 | I/O | |
| | SPI1_MISO | PB.5 | MFP5 | I/O | SPI1 MISO (Master In, Slave Out) pin. |
| | | PH.4 | MFP3 | I/O | |
| | | PC.7 | MFP4 | I/O | |
| | | PC.3 | MFP7 | I/O | |
| | | PD.7 | MFP5 | I/O | |
| | | PE.1 | MFP6 | I/O | |
| | SPI1_MOSI | PB.4 | MFP5 | I/O | SPI1 MOSI (Master Out, Slave In) pin. |
| | | PH.5 | MFP3 | I/O | |
| | | PC.6 | MFP4 | I/O | |
| | | PC.2 | MFP7 | I/O | |
| | | PD.6 | MFP5 | I/O | |
| | | PE.0 | MFP6 | I/O | |
| | SPI1_SS | PB.2 | MFP5 | I/O | SPI1 slave select pin. |
| | | PH.7 | MFP3 | I/O | |
| | | PA.6 | MFP4 | I/O | |
| | | PC.0 | MFP7 | I/O | |
| | | PD.4 | MFP5 | I/O | |
| | | PH.9 | MFP6 | I/O | |
| SPI2 | SPI2_CLK | PA.10 | MFP4 | I/O | SPI2 serial clock pin. |
| | | PG.3 | MFP3 | I/O | |
| | | PE.8 | MFP5 | I/O | |
| | | PA.13 | MFP5 | I/O | |
| | SPI2_I2SMCLK | PC.13 | MFP4 | I/O | SPI2 I2S master clock output pin |
| | | PG.1 | MFP3 | I/O | |
| | | PE.12 | MFP5 | I/O | |
| | SPI2_MISO | PA.9 | MFP4 | I/O | SPI2 MISO (Master In, Slave Out) pin. |
| | | PG.4 | MFP3 | I/O | |
| | | PE.9 | MFP5 | I/O | |
| | | PA.14 | MFP5 | I/O | |
| | SPI2_MOSI | PA.8 | MFP4 | I/O | SPI2 MOSI (Master Out, Slave In) pin. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PF.11 | MFP3 | I/O | |
| | | PE.10 | MFP5 | I/O | |
| | | PA.15 | MFP5 | I/O | |
| | SPI2_SS | PA.11 | MFP4 | I/O | SPI2 slave select pin. |
| | | PG.2 | MFP3 | I/O | |
| | | PE.11 | MFP5 | I/O | |
| | | PA.12 | MFP5 | I/O | |
| SPI3 | SPI3_CLK | PC.10 | MFP6 | I/O | SPI3 serial clock pin. |
| | | PE.4 | MFP5 | I/O | |
| | | PG.6 | MFP3 | I/O | |
| | | PB.11 | MFP11 | I/O | |
| | SPI3_I2SMCLK | PB.1 | MFP6 | I/O | SPI3 I2S master clock output pin |
| | | PE.6 | MFP5 | I/O | |
| | | PD.14 | MFP3 | I/O | |
| | SPI3_MISO | PC.12 | MFP6 | I/O | SPI3 MISO (Master In, Slave Out) pin. |
| | | PE.3 | MFP5 | I/O | |
| | | PG.7 | MFP3 | I/O | |
| | | PB.9 | MFP11 | I/O | |
| | SPI3_MOSI | PC.11 | MFP6 | I/O | SPI3 MOSI (Master Out, Slave In) pin. |
| | | PE.2 | MFP5 | I/O | |
| | | PG.8 | MFP3 | I/O | |
| | | PB.8 | MFP11 | I/O | |
| | SPI3_SS | PC.9 | MFP6 | I/O | SPI3 slave select pin. |
| | | PE.5 | MFP5 | I/O | |
| | | PG.5 | MFP3 | I/O | |
| | | PB.10 | MFP11 | I/O | |
| SPIM | SPIM_CLK | PA.2 | MFP2 | I/O | SPIM serial clock pin. |
| | | PC.2 | MFP3 | I/O | |
| | | PG.12 | MFP4 | I/O | |
| | | PE.4 | MFP4 | I/O | |
| | SPIM_D2 | PA.5 | MFP2 | I/O | SPIM data 2 pin for Quad Mode I/O. |
| | | PC.5 | MFP3 | I/O | |
| | | PG.9 | MFP4 | I/O | |
| | | PE.7 | MFP4 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | SPIM_D3 | PA.4 | MFP2 | I/O | SPIM data 3 pin for Quad Mode I/O. |
| | | PC.4 | MFP3 | I/O | |
| | | PG.10 | MFP4 | I/O | |
| | | PE.6 | MFP4 | I/O | |
| | SPIM_MISO | PA.1 | MFP2 | I/O | SPIM MISO (Master In, Slave Out) pin. |
| | | PC.1 | MFP3 | I/O | |
| | | PG.13 | MFP4 | I/O | |
| | | PE.3 | MFP4 | I/O | |
| | SPIM_MOSI | PA.0 | MFP2 | I/O | SPIM MOSI (Master Out, Slave In) pin. |
| | | PC.0 | MFP3 | I/O | |
| | | PG.14 | MFP4 | I/O | |
| | | PE.2 | MFP4 | I/O | |
| | SPIM_SS | PA.3 | MFP2 | I/O | SPIM slave select pin. |
| | | PC.3 | MFP3 | I/O | |
| | | PG.11 | MFP4 | I/O | |
| | | PE.5 | MFP4 | I/O | |
| TAMPER0 | TAMPER0 | PF.6 | MFP10 | I/O | TAMPER detector loop pin 0. |
| TAMPER1 | TAMPER1 | PF.7 | MFP10 | I/O | TAMPER detector loop pin 1. |
| TAMPER2 | TAMPER2 | PF.8 | MFP10 | I/O | TAMPER detector loop pin 2. |
| TAMPER3 | TAMPER3 | PF.9 | MFP10 | I/O | TAMPER detector loop pin 3. |
| TAMPER4 | TAMPER4 | PF.10 | MFP10 | I/O | TAMPER detector loop pin 4. |
| TAMPER5 | TAMPER5 | PF.11 | MFP10 | I/O | TAMPER detector loop pin 5. |
| TM0 | TM0 | PB.5 | MFP14 | I/O | Timer0 event counter input/toggle output pin. |
| | | PG.2 | MFP13 | I/O | |
| | | PC.7 | MFP14 | I/O | |
| | TM0_EXT | PA.11 | MFP13 | I/O | Timer0 external capture input/toggle output pin. |
| | | PH.0 | MFP13 | I/O | |
| | | PB.15 | MFP13 | I/O | |
| TM1 | TM1 | PB.4 | MFP14 | I/O | Timer1 event counter input/toggle output pin. |
| | | PG.3 | MFP13 | I/O | |
| | | PC.6 | MFP14 | I/O | |
| | | PC.14 | MFP13 | I/O | |
| | TM1_EXT | PA.10 | MFP13 | I/O | Timer1 external capture input/toggle output pin. |
| | | PH.1 | MFP13 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PB.14 | MFP13 | I/O | |
| TM2 | TM2 | PB.3 | MFP14 | I/O | Timer2 event counter input/toggle output pin. |
| | | PG.4 | MFP13 | I/O | |
| | | PA.7 | MFP14 | I/O | |
| | | PD.0 | MFP14 | I/O | |
| | TM2_EXT | PA.9 | MFP13 | I/O | Timer2 external capture input/toggle output pin. |
| | | PH.2 | MFP13 | I/O | |
| | | PB.13 | MFP13 | I/O | |
| TM3 | TM3 | PB.2 | MFP14 | I/O | Timer3 event counter input/toggle output pin. |
| | | PF.11 | MFP13 | I/O | |
| | | PA.6 | MFP14 | I/O | |
| | TM3_EXT | PA.8 | MFP13 | I/O | Timer3 external capture input/toggle output pin. |
| | | PH.3 | MFP13 | I/O | |
| | | PB.12 | MFP13 | I/O | |
| TRACE | TRACE_CLK | PE.8 | MFP14 | O | ETM Trace Clock output pin |
| | TRACE_DATA0 | PE.9 | MFP14 | O | ETM Trace Data 0 output pin |
| | TRACE_DATA1 | PE.10 | MFP14 | O | ETM Trace Data 1 output pin |
| | TRACE_DATA2 | PE.11 | MFP14 | O | ETM Trace Data 2 output pin |
| | TRACE_DATA3 | PE.12 | MFP14 | O | ETM Trace Data 3 output pin |
| UART0 | UART0_RXD | PC.11 | MFP3 | I | UART0 data receiver input pin. |
| | | PF.2 | MFP3 | I | |
| | | PA.6 | MFP7 | I | |
| | | PA.0 | MFP7 | I | |
| | | PD.2 | MFP9 | I | |
| | | PA.15 | MFP3 | I | |
| | | PH.11 | MFP8 | I | |
| | | PB.12 | MFP6 | I | |
| | | PB.8 | MFP5 | I | |
| | UART0_TXD | PC.12 | MFP3 | O | UART0 data transmitter output pin. |
| | | PF.3 | MFP3 | O | |
| | | PA.7 | MFP7 | O | |
| | | PA.1 | MFP7 | O | |
| | | PD.3 | MFP9 | O | |
| | | PA.14 | MFP3 | O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PH.10 | MFP8 | O | |
| | | PB.13 | MFP6 | O | |
| | | PB.9 | MFP5 | O | |
| | UART0_nCTS | PC.7 | MFP7 | I | UART0 clear to Send input pin. |
| | | PA.5 | MFP7 | I | |
| | | PB.15 | MFP6 | I | |
| | | PB.11 | MFP5 | I | |
| | UART0_nRTS | PC.6 | MFP7 | O | UART0 request to Send output pin. |
| | | PA.4 | MFP7 | O | |
| | | PB.14 | MFP6 | O | |
| | | PB.10 | MFP5 | O | |
| UART1 | UART1_RXD | PB.2 | MFP6 | I | UART1 data receiver input pin. |
| | | PA.8 | MFP7 | I | |
| | | PD.10 | MFP3 | I | |
| | | PG.1 | MFP8 | I | |
| | | PC.8 | MFP8 | I | |
| | | PA.2 | MFP8 | I | |
| | | PF.1 | MFP2 | I | |
| | | PD.6 | MFP3 | I | |
| | | PH.9 | MFP10 | I | |
| | | PB.6 | MFP6 | I | |
| | UART1_TXD | PB.3 | MFP6 | O | UART1 data transmitter output pin. |
| | | PA.9 | MFP7 | O | |
| | | PD.11 | MFP3 | O | |
| | | PG.0 | MFP8 | O | |
| | | PE.13 | MFP8 | O | |
| | | PA.3 | MFP8 | O | |
| | | PF.0 | MFP2 | O | |
| | | PD.7 | MFP3 | O | |
| | | PH.8 | MFP10 | O | |
| | | PB.7 | MFP6 | O | |
| | UART1_nCTS | PE.11 | MFP8 | I | UART1 clear to Send input pin. |
| | | PA.1 | MFP8 | I | |
| | | PB.9 | MFP6 | I | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | UART1_nRTS | PE.12 | MFP8 | O | UART1 request to Send output pin. |
| | | PA.0 | MFP8 | O | |
| | | PB.8 | MFP6 | O | |
| UART2 | UART2_RXD | PB.0 | MFP7 | I | UART2 data receiver input pin. |
| | | PD.12 | MFP7 | I | |
| | | PG.0 | MFP6 | I | |
| | | PF.5 | MFP2 | I | |
| | | PE.9 | MFP7 | I | |
| | | PE.15 | MFP3 | I | |
| | | PC.4 | MFP8 | I | |
| | | PC.0 | MFP8 | I | |
| | UART2_TXD | PB.1 | MFP7 | O | UART2 data transmitter output pin. |
| | | PC.13 | MFP7 | O | |
| | | PG.1 | MFP6 | O | |
| | | PF.4 | MFP2 | O | |
| | | PE.8 | MFP7 | O | |
| | | PE.14 | MFP3 | O | |
| | | PC.5 | MFP8 | O | |
| | | PC.1 | MFP8 | O | |
| | UART2_nCTS | PF.5 | MFP4 | I | UART2 clear to Send input pin. |
| | | PD.9 | MFP4 | I | |
| | | PC.2 | MFP8 | I | |
| | UART2_nRTS | PF.4 | MFP4 | O | UART2 request to Send output pin. |
| | | PD.8 | MFP4 | O | |
| | | PC.3 | MFP8 | O | |
| UART3 | UART3_RXD | PC.9 | MFP7 | I | UART3 data receiver input pin. |
| | | PE.11 | MFP7 | I | |
| | | PC.2 | MFP11 | I | |
| | | PD.0 | MFP5 | I | |
| | | PE.0 | MFP7 | I | |
| | | PB.14 | MFP7 | I | |
| | UART3_TXD | PC.10 | MFP7 | O | UART3 data transmitter output pin. |
| | | PE.10 | MFP7 | O | |
| | | PC.3 | MFP11 | O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PD.1 | MFP5 | O | |
| | | PE.1 | MFP7 | O | |
| | | PB.15 | MFP7 | O | |
| | UART3_nCTS | PD.2 | MFP5 | I | UART3 clear to Send input pin. |
| | | PH.9 | MFP7 | I | |
| | | PB.12 | MFP7 | I | |
| | UART3_nRTS | PD.3 | MFP5 | O | UART3 request to Send output pin. |
| | | PH.8 | MFP7 | O | |
| | | PB.13 | MFP7 | O | |
| UART4 | UART4_RXD | PF.6 | MFP6 | I | UART4 data receiver input pin. |
| | | PH.3 | MFP5 | I | |
| | | PC.6 | MFP5 | I | |
| | | PA.2 | MFP7 | I | |
| | | PC.4 | MFP11 | I | |
| | | PA.13 | MFP3 | I | |
| | | PH.11 | MFP7 | I | |
| | | PB.10 | MFP6 | I | |
| | UART4_TXD | PF.7 | MFP6 | O | UART4 data transmitter output pin. |
| | | PH.2 | MFP5 | O | |
| | | PC.7 | MFP5 | O | |
| | | PA.3 | MFP7 | O | |
| | | PC.5 | MFP11 | O | |
| | | PA.12 | MFP3 | O | |
| | | PH.10 | MFP7 | O | |
| | | PB.11 | MFP6 | O | |
| | UART4_nCTS | PC.8 | MFP5 | I | UART4 clear to Send input pin. |
| | | PE.1 | MFP9 | I | |
| | UART4_nRTS | PE.13 | MFP5 | O | UART4 request to Send output pin. |
| | | PE.0 | MFP9 | O | |
| UART5 | UART5_RXD | PB.4 | MFP7 | I | UART5 data receiver input pin. |
| | | PH.1 | MFP4 | I | |
| | | PA.4 | MFP8 | I | |
| | | PE.6 | MFP8 | I | |
| | UART5_TXD | PB.5 | MFP7 | O | UART5 data transmitter output pin. |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PH.0 | MFP4 | O | |
| | | PA.5 | MFP8 | O | |
| | | PE.7 | MFP8 | O | |
| | UART5_nCTS | PB.2 | MFP7 | I | UART5 clear to Send input pin. |
| | | PH.3 | MFP4 | I | |
| | UART5_nRTS | PB.3 | MFP7 | O | UART5 request to Send output pin. |
| | | PH.2 | MFP4 | O | |
| USB | USB_D+ | PA.14 | MFP14 | A | USB differential signal D+. |
| | USB_D- | PA.13 | MFP14 | A | USB differential signal D-. |
| | USB_OTG_ID | PA.15 | MFP14 | I | USB_ identification. |
| | USB_VBUS | PA.12 | MFP14 | P | Power supply from USB host or HUB. |
| | USB_VBUS_EN | PB.15 | MFP14 | O | USB external VBUS regulator enable pin. |
| | | PB.6 | MFP14 | O | |
| | USB_VBUS_ST | PD.4 | MFP14 | I | USB external VBUS regulator status pin. |
| | | PC.14 | MFP14 | I | |
| | | PB.7 | MFP14 | I | |
| USCI0 | USCI0_CLK | PA.11 | MFP6 | I/O | USCI0 clock pin. |
| | | PD.0 | MFP3 | I/O | |
| | | PE.2 | MFP7 | I/O | |
| | | PB.12 | MFP5 | I/O | |
| | USCI0_CTL0 | PC.13 | MFP6 | I/O | USCI0 control 0 pin. |
| | | PD.4 | MFP3 | I/O | |
| | | PE.6 | MFP7 | I/O | |
| | | PC.14 | MFP5 | I/O | |
| | USCI0_CTL1 | PA.8 | MFP6 | I/O | USCI0 control 1 pin. |
| | | PD.3 | MFP3 | I/O | |
| | | PE.5 | MFP7 | I/O | |
| | | PB.15 | MFP5 | I/O | |
| | USCI0_DAT0 | PA.10 | MFP6 | I/O | USCI0 data 0 pin. |
| | | PD.1 | MFP3 | I/O | |
| | | PE.3 | MFP7 | I/O | |
| | | PB.13 | MFP5 | I/O | |
| | USCI0_DAT1 | PA.9 | MFP6 | I/O | USCI0 data 1 pin. |
| | | PD.2 | MFP3 | I/O | |

| Group | Pin Name | GPIO | MFP | Type | Description |
|---|---|---|---|---|---|
| | | PE.4 | MFP7 | I/O | |
| | | PB.14 | MFP5 | I/O | |
| USCI1 | USCI1_CLK | PB.1 | MFP8 | I/O | USCI1 clock pin. |
| | | PE.12 | MFP6 | I/O | |
| | | PD.7 | MFP6 | I/O | |
| | | PB.8 | MFP4 | I/O | |
| | USCI1_CTL0 | PB.5 | MFP8 | I/O | USCI1 control 0 pin. |
| | | PE.9 | MFP6 | I/O | |
| | | PD.3 | MFP6 | I/O | |
| | | PB.10 | MFP4 | I/O | |
| | USCI1_CTL1 | PB.4 | MFP8 | I/O | USCI1 control 1 pin. |
| | | PE.8 | MFP6 | I/O | |
| | | PD.4 | MFP6 | I/O | |
| | | PB.9 | MFP4 | I/O | |
| | USCI1_DAT0 | PB.2 | MFP8 | I/O | USCI1 data 0 pin. |
| | | PE.10 | MFP6 | I/O | |
| | | PD.5 | MFP6 | I/O | |
| | | PB.7 | MFP4 | I/O | |
| | USCI1_DAT1 | PB.3 | MFP8 | I/O | USCI1 data 1 pin. |
| | | PE.11 | MFP6 | I/O | |
| | | PD.6 | MFP6 | I/O | |
| | | PB.6 | MFP4 | I/O | |
| X32 | X32_IN | PF.5 | MFP10 | I | External 32.768 kHz crystal input pin. |
| | X32_OUT | PF.4 | MFP10 | O | External 32.768 kHz crystal output pin. |
| XT1 | XT1_IN | PF.3 | MFP10 | I | External 4~24 MHz (high speed) crystal input pin. |
| | XT1_OUT | PF.2 | MFP10 | O | External 4~24 MHz (high speed) crystal output pin. |

### 4.2.8 M480 Multi-function Summary Table Sorted by GPIO

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| PA.0 | PA.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | SPIM_MOSI | I/O | MFP2 | SPIM MOSI (Master Out, Slave In) pin. |
| | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | I2C2_SDA | I/O | MFP9 | $I^2C2$ data input/output pin. |
| | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| | EPWM0_CH5 | I/O | MFP13 | EPWM0 channel 5 output/capture input. |
| | DAC0_ST | I | MFP15 | DAC0 external trigger input. |
| PA.1 | PA.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | SPIM_MISO | I/O | MFP2 | SPIM MISO (Master In, Slave Out) pin. |
| | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | I2C2_SCL | I/O | MFP9 | $I^2C2$ clock pin. |
| | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |
| | EPWM0_CH4 | I/O | MFP13 | EPWM0 channel 4 output/capture input. |
| | DAC1_ST | I | MFP15 | DAC1 external trigger input. |
| PA.2 | PA.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | SPIM_CLK | I/O | MFP2 | SPIM serial clock pin. |
| | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | I2C1_SDA | I/O | MFP9 | $I^2C1$ data input/output pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| | EPWM0_CH3 | I/O | MFP13 | EPWM0 channel 3 output/capture input. |
| PA.3 | PA.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | SPIM_SS | I/O | MFP2 | SPIM slave select pin. |
| | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | I2C1_SCL | I/O | MFP9 | $I^2C1$ clock pin. |
| | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| | EPWM0_CH2 | I/O | MFP13 | EPWM0 channel 2 output/capture input. |
| | QEI0_B | I | MFP14 | Quadrature encoder 0 phase B input |
| PA.4 | PA.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | SPIM_D3 | I/O | MFP2 | SPIM data 3 pin for Quad Mode I/O. |
| | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | SPI0_I2SMCLK | I/O | MFP4 | SPI0 $I^2S$ master clock output pin |
| | SD1_CLK | O | MFP5 | SD/SDIO1 clock output pin |
| | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | I2C0_SDA | I/O | MFP9 | $I^2C0$ data input/output pin. |
| | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| | EPWM0_CH1 | I/O | MFP13 | EPWM0 channel 1 output/capture input. |
| | QEI0_A | I | MFP14 | Quadrature encoder 0 phase A input |
| PA.5 | PA.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | SPIM_D2 | I/O | MFP2 | SPIM data 2 pin for Quad Mode I/O. |
| | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | SPI1_I2SMCLK | I/O | MFP4 | SPI1 $I^2S$ master clock output pin |
| | SD1_CMD | I/O | MFP5 | SD/SDIO1 command/response pin |
| | SC2_nCD | I | MFP6 | Smart Card 2 card detect pin. |
| | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | I2C0_SCL | I/O | MFP9 | I²C0 clock pin. |
| | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| | EPWM0_CH0 | I/O | MFP13 | EPWM0 channel 0 output/capture input. |
| | QEI0_INDEX | I | MFP14 | Quadrature encoder 0 index input |
| PA.6 | PA.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | EMAC_RMII_RXERR | I | MFP3 | EMAC RMII Receive Data Error input pin. |
| | SPI1_SS | I/O | MFP4 | SPI1 slave select pin. |
| | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| | SC2_CLK | O | MFP6 | Smart Card 2 clock pin. |
| | UART0_RXD | I | MFP7 | UART0 data receiver input pin. |
| | I2C1_SDA | I/O | MFP8 | I²C1 data input/output pin. |
| | EPWM1_CH5 | I/O | MFP11 | EPWM1 channel 5 output/capture input. |
| | BPWM1_CH3 | I/O | MFP12 | BPWM1 channel 3 output/capture input. |
| | ACMP1_WLAT | I | MFP13 | Analog comparator 1 window latch input pin |
| | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | INT0 | I | MFP15 | External interrupt 0 input pin. |
| PA.7 | PA.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | EMAC_RMII_CRSDV | I | MFP3 | EMAC RMII Carrier Sense/Receive Data input pin. |
| | SPI1_CLK | I/O | MFP4 | SPI1 serial clock pin. |
| | SC2_DAT | I/O | MFP6 | Smart Card 2 data pin. |
| | UART0_TXD | O | MFP7 | UART0 data transmitter output pin. |
| | I2C1_SCL | I/O | MFP8 | I²C1 clock pin. |
| | EPWM1_CH4 | I/O | MFP11 | EPWM1 channel 4 output/capture input. |
| | BPWM1_CH2 | I/O | MFP12 | BPWM1 channel 2 output/capture input. |
| | ACMP0_WLAT | I | MFP13 | Analog comparator 0 window latch input pin |
| | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | INT1 | I | MFP15 | External interrupt 1 input pin. |
| PA.8 | PA.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | OPA1_P | A | MFP1 | Operational amplifier 1 positive input pin. |
| | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | SC2_CLK | O | MFP3 | Smart Card 2 clock pin. |
| | SPI2_MOSI | I/O | MFP4 | SPI2 MOSI (Master Out, Slave In) pin. |
| | SD1_DAT0 | I/O | MFP5 | SD/SDIO1 data line bit 0. |
| | USCI0_CTL1 | I/O | MFP6 | USCI0 control 1 pin. |
| | UART1_RXD | I | MFP7 | UART1 data receiver input pin. |
| | BPWM0_CH3 | I/O | MFP9 | BPWM0 channel 3 output/capture input. |
| | QEI1_B | I | MFP10 | Quadrature encoder 1 phase B input |
| | ECAP0_IC2 | I | MFP11 | Enhanced capture unit 0 input 2 pin. |
| | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| | INT4 | I | MFP15 | External interrupt 4 input pin. |
| PA.9 | PA.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | OPA1_N | A | MFP1 | Operational amplifier 1 negative input pin. |
| | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | SC2_DAT | I/O | MFP3 | Smart Card 2 data pin. |
| | SPI2_MISO | I/O | MFP4 | SPI2 MISO (Master In, Slave Out) pin. |
| | SD1_DAT1 | I/O | MFP5 | SD/SDIO1 data line bit 1. |
| | USCI0_DAT1 | I/O | MFP6 | USCI0 data 1 pin. |
| | UART1_TXD | O | MFP7 | UART1 data transmitter output pin. |
| | BPWM0_CH2 | I/O | MFP9 | BPWM0 channel 2 output/capture input. |
| | QEI1_A | I | MFP10 | Quadrature encoder 1 phase A input |
| | ECAP0_IC1 | I | MFP11 | Enhanced capture unit 0 input 1 pin. |
| | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| PA.10 | PA.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | ACMP1_P0 | A | MFP1 | Analog comparator 1 positive input 0 pin. |
| | OPA1_O | A | MFP1 | Operational amplifier 1 output pin. |
| | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | SC2_RST | O | MFP3 | Smart Card 2 reset pin. |
| | SPI2_CLK | I/O | MFP4 | SPI2 serial clock pin. |
| | SD1_DAT2 | I/O | MFP5 | SD/SDIO1 data line bit 2. |
| | USCI0_DAT0 | I/O | MFP6 | USCI0 data 0 pin. |
| | I2C2_SDA | I/O | MFP7 | $I^2C2$ data input/output pin. |
| | BPWM0_CH1 | I/O | MFP9 | BPWM0 channel 1 output/capture input. |
| | QEI1_INDEX | I | MFP10 | Quadrature encoder 1 index input |
| | ECAP0_IC0 | I | MFP11 | Enhanced capture unit 0 input 0 pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | DAC0_ST | I | MFP14 | DAC0 external trigger input. |
| PA.11 | PA.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | ACMP0_P0 | A | MFP1 | Analog comparator 0 positive input 0 pin. |
| | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | SC2_PWR | O | MFP3 | Smart Card 2 power pin. |
| | SPI2_SS | I/O | MFP4 | SPI2 slave select pin. |
| | SD1_DAT3 | I/O | MFP5 | SD/SDIO1 data line bit 3. |
| | USCI0_CLK | I/O | MFP6 | USCI0 clock pin. |
| | I2C2_SCL | I/O | MFP7 | $I^2C2$ clock pin. |
| | BPWM0_CH0 | I/O | MFP9 | BPWM0 channel 0 output/capture input. |
| | EPWM0_SYNC_OUT | O | MFP10 | EPWM0 counter synchronous trigger output pin. |
| | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | DAC1_ST | I | MFP14 | DAC1 external trigger input. |
| PA.12 | PA.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | I2S0_BCLK | O | MFP2 | $I^2S0$ bit clock output pin. |
| | UART4_TXD | O | MFP3 | UART4 data transmitter output pin. |
| | I2C1_SCL | I/O | MFP4 | $I^2C1$ clock pin. |
| | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | CAN0_TXD | O | MFP6 | CAN0 bus transmitter output. |
| | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | BPWM1_CH2 | I/O | MFP11 | BPWM1 channel 2 output/capture input. |
| | QEI1_INDEX | I | MFP12 | Quadrature encoder 1 index input |
| | USB_VBUS | P | MFP14 | Power supply from USB host or HUB. |
| PA.13 | PA.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | I2S0_MCLK | O | MFP2 | $I^2S0$ master clock output pin. |
| | UART4_RXD | I | MFP3 | UART4 data receiver input pin. |
| | I2C1_SDA | I/O | MFP4 | $I^2C1$ data input/output pin. |
| | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | CAN0_RXD | I | MFP6 | CAN0 bus receiver input. |
| | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | BPWM1_CH3 | I/O | MFP11 | BPWM1 channel 3 output/capture input. |
| | QEI1_A | I | MFP12 | Quadrature encoder 1 phase A input |
| | USB_D- | A | MFP14 | USB differential signal D-. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| PA.14 | PA.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | I2S0_DI | I | MFP2 | I²S0 data input pin. |
| | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | I2C2_SCL | I/O | MFP6 | I²C2 clock pin. |
| | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| | BPWM1_CH4 | I/O | MFP11 | BPWM1 channel 4 output/capture input. |
| | QEI1_B | I | MFP12 | Quadrature encoder 1 phase B input |
| | USB_D+ | A | MFP14 | USB differential signal D+. |
| PA.15 | PA.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | I2S0_DO | O | MFP2 | I²S0 data output pin. |
| | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | I2C2_SDA | I/O | MFP6 | I²C2 data input/output pin. |
| | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | BPWM1_CH5 | I/O | MFP11 | BPWM1 channel 5 output/capture input. |
| | EPWM0_SYNC_IN | I | MFP12 | EPWM0 counter synchronous trigger input pin. |
| | USB_OTG_ID | I | MFP14 | USB_ identification. |
| PB.0 | PB.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH0 | A | MFP1 | EADC0 channel 0 analog input. |
| | OPA0_P | A | MFP1 | Operational amplifier 0 positive input pin. |
| | EBI_ADR9 | O | MFP2 | EBI address bus bit 9. |
| | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | SPI0_I2SMCLK | I/O | MFP8 | SPI0 I²S master clock output pin |
| | I2C1_SDA | I/O | MFP9 | I²C1 data input/output pin. |
| | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |
| | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | EPWM0_BRAKE1 | I | MFP13 | EPWM0 Brake 1 input pin. |
| PB.1 | PB.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH1 | A | MFP1 | EADC0 channel 1 analog input. |
| | OPA0_N | A | MFP1 | Operational amplifier 0 negative input pin. |
| | EBI_ADR8 | O | MFP2 | EBI address bus bit 8. |
| | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | EMAC_RMII_RXERR | I | MFP4 | EMAC RMII Receive Data Error input pin. |
| | SPI1_I2SMCLK | I/O | MFP5 | SPI1 $I^2S$ master clock output pin |
| | SPI3_I2SMCLK | I/O | MFP6 | SPI3 $I^2S$ master clock output pin |
| | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | USCI1_CLK | I/O | MFP8 | USCI1 clock pin. |
| | I2C1_SCL | I/O | MFP9 | $I^2C1$ clock pin. |
| | I2S0_LRCK | O | MFP10 | $I^2S0$ left right channel clock output pin. |
| | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | EPWM0_BRAKE0 | I | MFP13 | EPWM0 Brake 0 input pin. |
| PB.2 | PB.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH2 | A | MFP1 | EADC0 channel 2 analog input. |
| | ACMP0_P1 | A | MFP1 | Analog comparator 0 positive input 1 pin. |
| | OPA0_O | A | MFP1 | Operational amplifier 0 output pin. |
| | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | EMAC_RMII_CRSDV | I | MFP4 | EMAC RMII Carrier Sense/Receive Data input pin. |
| | SPI1_SS | I/O | MFP5 | SPI1 slave select pin. |
| | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | UART5_nCTS | I | MFP7 | UART5 clear to Send input pin. |
| | USCI1_DAT0 | I/O | MFP8 | USCI1 data 0 pin. |
| | SC0_PWR | O | MFP9 | Smart Card 0 power pin. |
| | I2S0_DO | O | MFP10 | $I^2S0$ data output pin. |
| | EPWM0_CH3 | I/O | MFP11 | EPWM0 channel 3 output/capture input. |
| | TM3 | I/O | MFP14 | Timer3 event counter input/toggle output pin. |
| | INT3 | I | MFP15 | External interrupt 3 input pin. |
| PB.3 | PB.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH3 | A | MFP1 | EADC0 channel 3 analog input. |
| | ACMP0_N | A | MFP1 | Analog comparator 0 negative input pin. |
| | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | EMAC_RMII_RXD1 | I | MFP4 | EMAC RMII Receive Data bus bit 1. |
| | SPI1_CLK | I/O | MFP5 | SPI1 serial clock pin. |
| | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | UART5_nRTS | O | MFP7 | UART5 request to Send output pin. |
| | USCI1_DAT1 | I/O | MFP8 | USCI1 data 1 pin. |
| | SC0_RST | O | MFP9 | Smart Card 0 reset pin. |
| | I2S0_DI | I | MFP10 | $I^2S0$ data input pin. |
| | EPWM0_CH2 | I/O | MFP11 | EPWM0 channel 2 output/capture input. |
| | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| | INT2 | I | MFP15 | External interrupt 2 input pin. |
| PB.4 | PB.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH4 | A | MFP1 | EADC0 channel 4 analog input. |
| | ACMP1_P1 | A | MFP1 | Analog comparator 1 positive input 1 pin. |
| | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | EMAC_RMII_RXD0 | I | MFP4 | EMAC RMII Receive Data bus bit 0. |
| | SPI1_MOSI | I/O | MFP5 | SPI1 MOSI (Master Out, Slave In) pin. |
| | I2C0_SDA | I/O | MFP6 | $I^2C0$ data input/output pin. |
| | UART5_RXD | I | MFP7 | UART5 data receiver input pin. |
| | USCI1_CTL1 | I/O | MFP8 | USCI1 control 1 pin. |
| | SC0_DAT | I/O | MFP9 | Smart Card 0 data pin. |
| | I2S0_MCLK | O | MFP10 | $I^2S0$ master clock output pin. |
| | EPWM0_CH1 | I/O | MFP11 | EPWM0 channel 1 output/capture input. |
| | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | INT1 | I | MFP15 | External interrupt 1 input pin. |
| PB.5 | PB.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH5 | A | MFP1 | EADC0 channel 5 analog input. |
| | ACMP1_N | A | MFP1 | Analog comparator 1 negative input pin. |
| | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | EMAC_RMII_REFCLK | I | MFP4 | EMAC RMII reference clock input pin. |
| | SPI1_MISO | I/O | MFP5 | SPI1 MISO (Master In, Slave Out) pin. |
| | I2C0_SCL | I/O | MFP6 | $I^2C0$ clock pin. |
| | UART5_TXD | O | MFP7 | UART5 data transmitter output pin. |
| | USCI1_CTL0 | I/O | MFP8 | USCI1 control 0 pin. |
| | SC0_CLK | O | MFP9 | Smart Card 0 clock pin. |
| | I2S0_BCLK | O | MFP10 | $I^2S0$ bit clock output pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | EPWM0_CH0 | I/O | MFP11 | EPWM0 channel 0 output/capture input. |
| | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | INT0 | I | MFP15 | External interrupt 0 input pin. |
| PB.6 | PB.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH6 | A | MFP1 | EADC0 channel 6 analog input. |
| | EBI_nWRH | O | MFP2 | EBI high byte write enable output pin |
| | EMAC_PPS | O | MFP3 | EMAC Pulse Per Second output pin. |
| | USCI1_DAT1 | I/O | MFP4 | USCI1 data 1 pin. |
| | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | UART1_RXD | I | MFP6 | UART1 data receiver input pin. |
| | SD1_CLK | O | MFP7 | SD/SDIO1 clock output pin |
| | EBI_nCS1 | O | MFP8 | EBI chip select 1 output pin. |
| | BPWM1_CH5 | I/O | MFP10 | BPWM1 channel 5 output/capture input. |
| | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | INT4 | I | MFP13 | External interrupt 4 input pin. |
| | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | ACMP1_O | O | MFP15 | Analog comparator 1 output pin. |
| PB.7 | PB.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH7 | A | MFP1 | EADC0 channel 7 analog input. |
| | EBI_nWRL | O | MFP2 | EBI low byte write enable output pin. |
| | EMAC_RMII_TXEN | O | MFP3 | EMAC RMII Transmit Enable output pin. |
| | USCI1_DAT0 | I/O | MFP4 | USCI1 data 0 pin. |
| | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | UART1_TXD | O | MFP6 | UART1 data transmitter output pin. |
| | SD1_CMD | I/O | MFP7 | SD/SDIO1 command/response pin |
| | EBI_nCS0 | O | MFP8 | EBI chip select 0 output pin. |
| | BPWM1_CH4 | I/O | MFP10 | BPWM1 channel 4 output/capture input. |
| | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | INT5 | I | MFP13 | External interrupt 5 input pin. |
| | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | ACMP0_O | O | MFP15 | Analog comparator 0 output pin. |
| PB.8 | PB.8 | I/O | MFP0 | General purpose digital I/O pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | EADC0_CH8 | A | MFP1 | EADC0 channel 8 analog input. |
| | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | EMAC_RMII_TXD1 | O | MFP3 | EMAC RMII Transmit Data bus bit 1. |
| | USCI1_CLK | I/O | MFP4 | USCI1 clock pin. |
| | UART0_RXD | I | MFP5 | UART0 data receiver input pin. |
| | UART1_nRTS | O | MFP6 | UART1 request to Send output pin. |
| | I2C1_SMBSUS | O | MFP7 | $I^2C1$ SMBus SMBSUS pin (PMBus CONTROL pin) |
| | BPWM1_CH3 | I/O | MFP10 | BPWM1 channel 3 output/capture input. |
| | SPI3_MOSI | I/O | MFP11 | SPI3 MOSI (Master Out, Slave In) pin. |
| | INT6 | I | MFP13 | External interrupt 6 input pin. |
| PB.9 | PB.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH9 | A | MFP1 | EADC0 channel 9 analog input. |
| | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | EMAC_RMII_TXD0 | O | MFP3 | EMAC RMII Transmit Data bus bit 0. |
| | USCI1_CTL1 | I/O | MFP4 | USCI1 control 1 pin. |
| | UART0_TXD | O | MFP5 | UART0 data transmitter output pin. |
| | UART1_nCTS | I | MFP6 | UART1 clear to Send input pin. |
| | I2C1_SMBAL | O | MFP7 | $I^2C1$ SMBus SMBALTER pin |
| | BPWM1_CH2 | I/O | MFP10 | BPWM1 channel 2 output/capture input. |
| | SPI3_MISO | I/O | MFP11 | SPI3 MISO (Master In, Slave Out) pin. |
| | INT7 | I | MFP13 | External interrupt 7 input pin. |
| PB.10 | PB.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH10 | A | MFP1 | EADC0 channel 10 analog input. |
| | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | EMAC_RMII_MDIO | I/O | MFP3 | EMAC RMII PHY Management Data pin. |
| | USCI1_CTL0 | I/O | MFP4 | USCI1 control 0 pin. |
| | UART0_nRTS | O | MFP5 | UART0 request to Send output pin. |
| | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | I2C1_SDA | I/O | MFP7 | $I^2C1$ data input/output pin. |
| | CAN0_RXD | I | MFP8 | CAN0 bus receiver input. |
| | BPWM1_CH1 | I/O | MFP10 | BPWM1 channel 1 output/capture input. |
| | SPI3_SS | I/O | MFP11 | SPI3 slave select pin. |
| | HSUSB_VBUS_EN | O | MFP14 | HSUSB external VBUS regulator enable pin. |
| PB.11 | PB.11 | I/O | MFP0 | General purpose digital I/O pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | EADC0_CH11 | A | MFP1 | EADC0 channel 11 analog input. |
| | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | EMAC_RMII_MDC | O | MFP3 | EMAC RMII PHY Management Clock output pin. |
| | UART0_nCTS | I | MFP5 | UART0 clear to Send input pin. |
| | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | I2C1_SCL | I/O | MFP7 | $I^2C1$ clock pin. |
| | CAN0_TXD | O | MFP8 | CAN0 bus transmitter output. |
| | SPI0_I2SMCLK | I/O | MFP9 | SPI0 $I^2S$ master clock output pin |
| | BPWM1_CH0 | I/O | MFP10 | BPWM1 channel 0 output/capture input. |
| | SPI3_CLK | I/O | MFP11 | SPI3 serial clock pin. |
| | HSUSB_VBUS_ST | I | MFP14 | HSUSB external VBUS regulator status pin. |
| PB.12 | PB.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH12 | A | MFP1 | EADC0 channel 12 analog input. |
| | DAC0_OUT | A | MFP1 | DAC0 channel analog output. |
| | ACMP0_P2 | A | MFP1 | Analog comparator 0 positive input 2 pin. |
| | ACMP1_P2 | A | MFP1 | Analog comparator 1 positive input 2 pin. |
| | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | SC1_CLK | O | MFP3 | Smart Card 1 clock pin. |
| | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | USCI0_CLK | I/O | MFP5 | USCI0 clock pin. |
| | UART0_RXD | I | MFP6 | UART0 data receiver input pin. |
| | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | I2C2_SDA | I/O | MFP8 | $I^2C2$ data input/output pin. |
| | SD0_nCD | I | MFP9 | SD/SDIO0 card detect input pin |
| | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| PB.13 | PB.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH13 | A | MFP1 | EADC0 channel 13 analog input. |
| | DAC1_OUT | A | MFP1 | DAC1 channel analog output. |
| | ACMP0_P3 | A | MFP1 | Analog comparator 0 positive input 3 pin. |
| | ACMP1_P3 | A | MFP1 | Analog comparator 1 positive input 3 pin. |
| | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | SC1_DAT | I/O | MFP3 | Smart Card 1 data pin. |
| | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | USCI0_DAT0 | I/O | MFP5 | USCI0 data 0 pin. |
| | UART0_TXD | O | MFP6 | UART0 data transmitter output pin. |
| | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | I2C2_SCL | I/O | MFP8 | I²C2 clock pin. |
| | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| PB.14 | PB.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH14 | A | MFP1 | EADC0 channel 14 analog input. |
| | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | SC1_RST | O | MFP3 | Smart Card 1 reset pin. |
| | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | USCI0_DAT1 | I/O | MFP5 | USCI0 data 1 pin. |
| | UART0_nRTS | O | MFP6 | UART0 request to Send output pin. |
| | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | I2C2_SMBSUS | O | MFP8 | I²C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| | CLKO | O | MFP14 | Clock Out |
| PB.15 | PB.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | EADC0_CH15 | A | MFP1 | EADC0 channel 15 analog input. |
| | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | SC1_PWR | O | MFP3 | Smart Card 1 power pin. |
| | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | USCI0_CTL1 | I/O | MFP5 | USCI0 control 1 pin. |
| | UART0_nCTS | I | MFP6 | UART0 clear to Send input pin. |
| | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | I2C2_SMBAL | O | MFP8 | I²C2 SMBus SMBALTER pin |
| | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| | USB_VBUS_EN | O | MFP14 | USB external VBUS regulator enable pin. |
| | HSUSB_VBUS_EN | O | MFP15 | HSUSB external VBUS regulator enable pin. |
| PC.0 | PC.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | SPIM_MOSI | I/O | MFP3 | SPIM MOSI (Master Out, Slave In) pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | QSPI0_MOSI0 | I/O | MFP4 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | SC1_CLK | O | MFP5 | Smart Card 1 clock pin. |
| | I2S0_LRCK | O | MFP6 | I²S0 left right channel clock output pin. |
| | SPI1_SS | I/O | MFP7 | SPI1 slave select pin. |
| | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | I2C0_SDA | I/O | MFP9 | I²C0 data input/output pin. |
| | EPWM1_CH5 | I/O | MFP12 | EPWM1 channel 5 output/capture input. |
| | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| PC.1 | PC.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | SPIM_MISO | I/O | MFP3 | SPIM MISO (Master In, Slave Out) pin. |
| | QSPI0_MISO0 | I/O | MFP4 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | SC1_DAT | I/O | MFP5 | Smart Card 1 data pin. |
| | I2S0_DO | O | MFP6 | I²S0 data output pin. |
| | SPI1_CLK | I/O | MFP7 | SPI1 serial clock pin. |
| | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | I2C0_SCL | I/O | MFP9 | I²C0 clock pin. |
| | EPWM1_CH4 | I/O | MFP12 | EPWM1 channel 4 output/capture input. |
| | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| PC.2 | PC.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | SPIM_CLK | I/O | MFP3 | SPIM serial clock pin. |
| | QSPI0_CLK | I/O | MFP4 | Quad SPI0 serial clock pin. |
| | SC1_RST | O | MFP5 | Smart Card 1 reset pin. |
| | I2S0_DI | I | MFP6 | I²S0 data input pin. |
| | SPI1_MOSI | I/O | MFP7 | SPI1 MOSI (Master Out, Slave In) pin. |
| | UART2_nCTS | I | MFP8 | UART2 clear to Send input pin. |
| | I2C0_SMBSUS | O | MFP9 | I²C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| | CAN1_RXD | I | MFP10 | CAN1 bus receiver input. |
| | UART3_RXD | I | MFP11 | UART3 data receiver input pin. |
| | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |
| PC.3 | PC.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | SPIM_SS | I/O | MFP3 | SPIM slave select pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | QSPI0_SS | I/O | MFP4 | Quad SPI0 slave select pin. |
| | SC1_PWR | O | MFP5 | Smart Card 1 power pin. |
| | I2S0_MCLK | O | MFP6 | $I^2S$0 master clock output pin. |
| | SPI1_MISO | I/O | MFP7 | SPI1 MISO (Master In, Slave Out) pin. |
| | UART2_nRTS | O | MFP8 | UART2 request to Send output pin. |
| | I2C0_SMBAL | O | MFP9 | $I^2C$0 SMBus SMBALTER pin |
| | CAN1_TXD | O | MFP10 | CAN1 bus transmitter output. |
| | UART3_TXD | O | MFP11 | UART3 data transmitter output pin. |
| | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| PC.4 | PC.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | SPIM_D3 | I/O | MFP3 | SPIM data 3 pin for Quad Mode I/O. |
| | QSPI0_MOSI1 | I/O | MFP4 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | SC1_nCD | I | MFP5 | Smart Card 1 card detect pin. |
| | I2S0_BCLK | O | MFP6 | $I^2S$0 bit clock output pin. |
| | SPI1_I2SMCLK | I/O | MFP7 | SPI1 $I^2S$ master clock output pin |
| | UART2_RXD | I | MFP8 | UART2 data receiver input pin. |
| | I2C1_SDA | I/O | MFP9 | $I^2C$1 data input/output pin. |
| | CAN0_RXD | I | MFP10 | CAN0 bus receiver input. |
| | UART4_RXD | I | MFP11 | UART4 data receiver input pin. |
| | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| PC.5 | PC.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | SPIM_D2 | I/O | MFP3 | SPIM data 2 pin for Quad Mode I/O. |
| | QSPI0_MISO1 | I/O | MFP4 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | UART2_TXD | O | MFP8 | UART2 data transmitter output pin. |
| | I2C1_SCL | I/O | MFP9 | $I^2C$1 clock pin. |
| | CAN0_TXD | O | MFP10 | CAN0 bus transmitter output. |
| | UART4_TXD | O | MFP11 | UART4 data transmitter output pin. |
| | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| PC.6 | PC.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | EMAC_RMII_RXD1 | I | MFP3 | EMAC RMII Receive Data bus bit 1. |
| | SPI1_MOSI | I/O | MFP4 | SPI1 MOSI (Master Out, Slave In) pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | UART4_RXD | I | MFP5 | UART4 data receiver input pin. |
| | SC2_RST | O | MFP6 | Smart Card 2 reset pin. |
| | UART0_nRTS | O | MFP7 | UART0 request to Send output pin. |
| | I2C1_SMBSUS | O | MFP8 | $I^2C1$ SMBus SMBSUS pin (PMBus CONTROL pin) |
| | EPWM1_CH3 | I/O | MFP11 | EPWM1 channel 3 output/capture input. |
| | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | TM1 | I/O | MFP14 | Timer1 event counter input/toggle output pin. |
| | INT2 | I | MFP15 | External interrupt 2 input pin. |
| PC.7 | PC.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | EMAC_RMII_RXD0 | I | MFP3 | EMAC RMII Receive Data bus bit 0. |
| | SPI1_MISO | I/O | MFP4 | SPI1 MISO (Master In, Slave Out) pin. |
| | UART4_TXD | O | MFP5 | UART4 data transmitter output pin. |
| | SC2_PWR | O | MFP6 | Smart Card 2 power pin. |
| | UART0_nCTS | I | MFP7 | UART0 clear to Send input pin. |
| | I2C1_SMBAL | O | MFP8 | $I^2C1$ SMBus SMBALTER pin |
| | EPWM1_CH2 | I/O | MFP11 | EPWM1 channel 2 output/capture input. |
| | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | TM0 | I/O | MFP14 | Timer0 event counter input/toggle output pin. |
| | INT3 | I | MFP15 | External interrupt 3 input pin. |
| PC.8 | PC.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | EMAC_RMII_REFCLK | I | MFP3 | EMAC RMII reference clock input pin. |
| | I2C0_SDA | I/O | MFP4 | $I^2C0$ data input/output pin. |
| | UART4_nCTS | I | MFP5 | UART4 clear to Send input pin. |
| | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| | EPWM1_CH1 | I/O | MFP11 | EPWM1 channel 1 output/capture input. |
| | BPWM1_CH4 | I/O | MFP12 | BPWM1 channel 4 output/capture input. |
| PC.9 | PC.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR7 | O | MFP2 | EBI address bus bit 7. |
| | SPI3_SS | I/O | MFP6 | SPI3 slave select pin. |
| | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | EPWM1_CH3 | I/O | MFP12 | EPWM1 channel 3 output/capture input. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| PC.10 | PC.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR6 | O | MFP2 | EBI address bus bit 6. |
| | SPI3_CLK | I/O | MFP6 | SPI3 serial clock pin. |
| | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | ECAP1_IC0 | I | MFP11 | Enhanced capture unit 1 input 0 pin. |
| | EPWM1_CH2 | I/O | MFP12 | EPWM1 channel 2 output/capture input. |
| PC.11 | PC.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR5 | O | MFP2 | EBI address bus bit 5. |
| | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |
| | I2C0_SDA | I/O | MFP4 | $I^2C0$ data input/output pin. |
| | SPI3_MOSI | I/O | MFP6 | SPI3 MOSI (Master Out, Slave In) pin. |
| | ECAP1_IC1 | I | MFP11 | Enhanced capture unit 1 input 1 pin. |
| | EPWM1_CH1 | I/O | MFP12 | EPWM1 channel 1 output/capture input. |
| | ACMP1_O | O | MFP14 | Analog comparator 1 output pin. |
| PC.12 | PC.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR4 | O | MFP2 | EBI address bus bit 4. |
| | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | I2C0_SCL | I/O | MFP4 | $I^2C0$ clock pin. |
| | SPI3_MISO | I/O | MFP6 | SPI3 MISO (Master In, Slave Out) pin. |
| | SC0_nCD | I | MFP9 | Smart Card 0 card detect pin. |
| | ECAP1_IC2 | I | MFP11 | Enhanced capture unit 1 input 2 pin. |
| | EPWM1_CH0 | I/O | MFP12 | EPWM1 channel 0 output/capture input. |
| | ACMP0_O | O | MFP14 | Analog comparator 0 output pin. |
| PC.13 | PC.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | SC2_nCD | I | MFP3 | Smart Card 2 card detect pin. |
| | SPI2_I2SMCLK | I/O | MFP4 | SPI2 $I^2S$ master clock output pin |
| | CAN1_TXD | O | MFP5 | CAN1 bus transmitter output. |
| | USCI0_CTL0 | I/O | MFP6 | USCI0 control 0 pin. |
| | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | BPWM0_CH4 | I/O | MFP9 | BPWM0 channel 4 output/capture input. |
| | CLKO | O | MFP13 | Clock Out |
| | EADC0_ST | I | MFP14 | EADC0 external trigger input. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| PC.14 | PC.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | SC1_nCD | I | MFP3 | Smart Card 1 card detect pin. |
| | SPI0_I2SMCLK | I/O | MFP4 | SPI0 $I^2S$ master clock output pin |
| | USCI0_CTL0 | I/O | MFP5 | USCI0 control 0 pin. |
| | QSPI0_CLK | I/O | MFP6 | Quad SPI0 serial clock pin. |
| | EPWM0_SYNC_IN | I | MFP11 | EPWM0 counter synchronous trigger input pin. |
| | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| | HSUSB_VBUS_ST | I | MFP15 | HSUSB external VBUS regulator status pin. |
| PD.0 | PD.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | USCI0_CLK | I/O | MFP3 | USCI0 clock pin. |
| | SPI0_MOSI | I/O | MFP4 | SPI0 MOSI (Master Out, Slave In) pin. |
| | UART3_RXD | I | MFP5 | UART3 data receiver input pin. |
| | I2C2_SDA | I/O | MFP6 | $I^2C2$ data input/output pin. |
| | SC2_CLK | O | MFP7 | Smart Card 2 clock pin. |
| | TM2 | I/O | MFP14 | Timer2 event counter input/toggle output pin. |
| PD.1 | PD.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | USCI0_DAT0 | I/O | MFP3 | USCI0 data 0 pin. |
| | SPI0_MISO | I/O | MFP4 | SPI0 MISO (Master In, Slave Out) pin. |
| | UART3_TXD | O | MFP5 | UART3 data transmitter output pin. |
| | I2C2_SCL | I/O | MFP6 | $I^2C2$ clock pin. |
| | SC2_DAT | I/O | MFP7 | Smart Card 2 data pin. |
| PD.2 | PD.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | USCI0_DAT1 | I/O | MFP3 | USCI0 data 1 pin. |
| | SPI0_CLK | I/O | MFP4 | SPI0 serial clock pin. |
| | UART3_nCTS | I | MFP5 | UART3 clear to Send input pin. |
| | SC2_RST | O | MFP7 | Smart Card 2 reset pin. |
| | UART0_RXD | I | MFP9 | UART0 data receiver input pin. |
| PD.3 | PD.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | USCI0_CTL1 | I/O | MFP3 | USCI0 control 1 pin. |
| | SPI0_SS | I/O | MFP4 | SPI0 slave select pin. |
| | UART3_nRTS | O | MFP5 | UART3 request to Send output pin. |
| | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |
| | SC2_PWR | O | MFP7 | Smart Card 2 power pin. |
| | SC1_nCD | I | MFP8 | Smart Card 1 card detect pin. |
| | UART0_TXD | O | MFP9 | UART0 data transmitter output pin. |
| PD.4 | PD.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | USCI0_CTL0 | I/O | MFP3 | USCI0 control 0 pin. |
| | I2C1_SDA | I/O | MFP4 | $I^2C1$ data input/output pin. |
| | SPI1_SS | I/O | MFP5 | SPI1 slave select pin. |
| | USCI1_CTL1 | I/O | MFP6 | USCI1 control 1 pin. |
| | SC1_CLK | O | MFP8 | Smart Card 1 clock pin. |
| | USB_VBUS_ST | I | MFP14 | USB external VBUS regulator status pin. |
| PD.5 | PD.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | I2C1_SCL | I/O | MFP4 | $I^2C1$ clock pin. |
| | SPI1_CLK | I/O | MFP5 | SPI1 serial clock pin. |
| | USCI1_DAT0 | I/O | MFP6 | USCI1 data 0 pin. |
| | SC1_DAT | I/O | MFP8 | Smart Card 1 data pin. |
| PD.6 | PD.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | UART1_RXD | I | MFP3 | UART1 data receiver input pin. |
| | I2C0_SDA | I/O | MFP4 | $I^2C0$ data input/output pin. |
| | SPI1_MOSI | I/O | MFP5 | SPI1 MOSI (Master Out, Slave In) pin. |
| | USCI1_DAT1 | I/O | MFP6 | USCI1 data 1 pin. |
| | SC1_RST | O | MFP8 | Smart Card 1 reset pin. |
| PD.7 | PD.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | UART1_TXD | O | MFP3 | UART1 data transmitter output pin. |
| | I2C0_SCL | I/O | MFP4 | $I^2C0$ clock pin. |
| | SPI1_MISO | I/O | MFP5 | SPI1 MISO (Master In, Slave Out) pin. |
| | USCI1_CLK | I/O | MFP6 | USCI1 clock pin. |
| | SC1_PWR | O | MFP8 | Smart Card 1 power pin. |
| PD.8 | PD.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD6 | I/O | MFP2 | EBI address/data bus bit 6. |
| | I2C2_SDA | I/O | MFP3 | $I^2C2$ data input/output pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| PD.9 | PD.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD7 | I/O | MFP2 | EBI address/data bus bit 7. |
| | I2C2_SCL | I/O | MFP3 | $I^2C2$ clock pin. |
| | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| PD.10 | PD.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | OPA2_P | A | MFP1 | Operational amplifier 2 positive input pin. |
| | EBI_nCS2 | O | MFP2 | EBI chip select 2 output pin. |
| | UART1_RXD | I | MFP3 | UART1 data receiver input pin. |
| | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |
| | QEI0_B | I | MFP10 | Quadrature encoder 0 phase B input |
| | INT7 | I | MFP15 | External interrupt 7 input pin. |
| PD.11 | PD.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | OPA2_N | A | MFP1 | Operational amplifier 2 negative input pin. |
| | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | UART1_TXD | O | MFP3 | UART1 data transmitter output pin. |
| | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | QEI0_A | I | MFP10 | Quadrature encoder 0 phase A input |
| | INT6 | I | MFP15 | External interrupt 6 input pin. |
| PD.12 | PD.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | OPA2_O | A | MFP1 | Operational amplifier 2 output pin. |
| | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | CAN1_RXD | I | MFP5 | CAN1 bus receiver input. |
| | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | BPWM0_CH5 | I/O | MFP9 | BPWM0 channel 5 output/capture input. |
| | QEI0_INDEX | I | MFP10 | Quadrature encoder 0 index input |
| | CLKO | O | MFP13 | Clock Out |
| | EADC0_ST | I | MFP14 | EADC0 external trigger input. |
| | INT5 | I | MFP15 | External interrupt 5 input pin. |
| PD.13 | PD.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | SD0_nCD | I | MFP3 | SD/SDIO0 card detect input pin |
| | SPI0_I2SMCLK | I/O | MFP4 | SPI0 $I^2S$ master clock output pin |
| | SPI1_I2SMCLK | I/O | MFP5 | SPI1 $I^2S$ master clock output pin |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | SC2_nCD | I | MFP7 | Smart Card 2 card detect pin. |
| PD.14 | PD.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | SPI3_I2SMCLK | I/O | MFP3 | SPI3 $I^2S$ master clock output pin |
| | SC1_nCD | I | MFP4 | Smart Card 1 card detect pin. |
| | EPWM0_CH4 | I/O | MFP11 | EPWM0 channel 4 output/capture input. |
| PE.0 | PE.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD11 | I/O | MFP2 | EBI address/data bus bit 11. |
| | QSPI0_MOSI0 | I/O | MFP3 | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | SC2_CLK | O | MFP4 | Smart Card 2 clock pin. |
| | I2S0_MCLK | O | MFP5 | $I^2S0$ master clock output pin. |
| | SPI1_MOSI | I/O | MFP6 | SPI1 MOSI (Master Out, Slave In) pin. |
| | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | I2C1_SDA | I/O | MFP8 | $I^2C1$ data input/output pin. |
| | UART4_nRTS | O | MFP9 | UART4 request to Send output pin. |
| PE.1 | PE.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD10 | I/O | MFP2 | EBI address/data bus bit 10. |
| | QSPI0_MISO0 | I/O | MFP3 | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | SC2_DAT | I/O | MFP4 | Smart Card 2 data pin. |
| | I2S0_BCLK | O | MFP5 | $I^2S0$ bit clock output pin. |
| | SPI1_MISO | I/O | MFP6 | SPI1 MISO (Master In, Slave Out) pin. |
| | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | I2C1_SCL | I/O | MFP8 | $I^2C1$ clock pin. |
| | UART4_nCTS | I | MFP9 | UART4 clear to Send input pin. |
| PE.2 | PE.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ALE | O | MFP2 | EBI address latch enable output pin. |
| | SD0_DAT0 | I/O | MFP3 | SD/SDIO0 data line bit 0. |
| | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | SPI3_MOSI | I/O | MFP5 | SPI3 MOSI (Master Out, Slave In) pin. |
| | SC0_CLK | O | MFP6 | Smart Card 0 clock pin. |
| | USCI0_CLK | I/O | MFP7 | USCI0 clock pin. |
| | QEI0_B | I | MFP11 | Quadrature encoder 0 phase B input |
| | EPWM0_CH5 | I/O | MFP12 | EPWM0 channel 5 output/capture input. |
| | BPWM0_CH0 | I/O | MFP13 | BPWM0 channel 0 output/capture input. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| PE.3 | PE.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_MCLK | O | MFP2 | EBI external clock output pin. |
| | SD0_DAT1 | I/O | MFP3 | SD/SDIO0 data line bit 1. |
| | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | SPI3_MISO | I/O | MFP5 | SPI3 MISO (Master In, Slave Out) pin. |
| | SC0_DAT | I/O | MFP6 | Smart Card 0 data pin. |
| | USCI0_DAT0 | I/O | MFP7 | USCI0 data 0 pin. |
| | QEI0_A | I | MFP11 | Quadrature encoder 0 phase A input |
| | EPWM0_CH4 | I/O | MFP12 | EPWM0 channel 4 output/capture input. |
| | BPWM0_CH1 | I/O | MFP13 | BPWM0 channel 1 output/capture input. |
| PE.4 | PE.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_nWR | O | MFP2 | EBI write enable output pin. |
| | SD0_DAT2 | I/O | MFP3 | SD/SDIO0 data line bit 2. |
| | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | SPI3_CLK | I/O | MFP5 | SPI3 serial clock pin. |
| | SC0_RST | O | MFP6 | Smart Card 0 reset pin. |
| | USCI0_DAT1 | I/O | MFP7 | USCI0 data 1 pin. |
| | QEI0_INDEX | I | MFP11 | Quadrature encoder 0 index input |
| | EPWM0_CH3 | I/O | MFP12 | EPWM0 channel 3 output/capture input. |
| | BPWM0_CH2 | I/O | MFP13 | BPWM0 channel 2 output/capture input. |
| PE.5 | PE.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_nRD | O | MFP2 | EBI read enable output pin. |
| | SD0_DAT3 | I/O | MFP3 | SD/SDIO0 data line bit 3. |
| | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | SPI3_SS | I/O | MFP5 | SPI3 slave select pin. |
| | SC0_PWR | O | MFP6 | Smart Card 0 power pin. |
| | USCI0_CTL1 | I/O | MFP7 | USCI0 control 1 pin. |
| | QEI1_B | I | MFP11 | Quadrature encoder 1 phase B input |
| | EPWM0_CH2 | I/O | MFP12 | EPWM0 channel 2 output/capture input. |
| | BPWM0_CH3 | I/O | MFP13 | BPWM0 channel 3 output/capture input. |
| PE.6 | PE.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | SD0_CLK | O | MFP3 | SD/SDIO0 clock output pin |
| | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | SPI3_I2SMCLK | I/O | MFP5 | SPI3 $I^2S$ master clock output pin |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | SC0_nCD | I | MFP6 | Smart Card 0 card detect pin. |
| | USCI0_CTL0 | I/O | MFP7 | USCI0 control 0 pin. |
| | UART5_RXD | I | MFP8 | UART5 data receiver input pin. |
| | CAN1_RXD | I | MFP9 | CAN1 bus receiver input. |
| | QEI1_A | I | MFP11 | Quadrature encoder 1 phase A input |
| | EPWM0_CH1 | I/O | MFP12 | EPWM0 channel 1 output/capture input. |
| | BPWM0_CH4 | I/O | MFP13 | BPWM0 channel 4 output/capture input. |
| PE.7 | PE.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | SD0_CMD | I/O | MFP3 | SD/SDIO0 command/response pin |
| | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | UART5_TXD | O | MFP8 | UART5 data transmitter output pin. |
| | CAN1_TXD | O | MFP9 | CAN1 bus transmitter output. |
| | QEI1_INDEX | I | MFP11 | Quadrature encoder 1 index input |
| | EPWM0_CH0 | I/O | MFP12 | EPWM0 channel 0 output/capture input. |
| | BPWM0_CH5 | I/O | MFP13 | BPWM0 channel 5 output/capture input. |
| PE.8 | PE.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR10 | O | MFP2 | EBI address bus bit 10. |
| | EMAC_RMII_MDC | O | MFP3 | EMAC RMII PHY Management Clock output pin. |
| | I2S0_BCLK | O | MFP4 | $I^2S$0 bit clock output pin. |
| | SPI2_CLK | I/O | MFP5 | SPI2 serial clock pin. |
| | USCI1_CTL1 | I/O | MFP6 | USCI1 control 1 pin. |
| | UART2_TXD | O | MFP7 | UART2 data transmitter output pin. |
| | EPWM0_CH0 | I/O | MFP10 | EPWM0 channel 0 output/capture input. |
| | EPWM0_BRAKE0 | I | MFP11 | EPWM0 Brake 0 input pin. |
| | ECAP0_IC0 | I | MFP12 | Enhanced capture unit 0 input 0 pin. |
| | TRACE_CLK | O | MFP14 | ETM Trace Clock output pin |
| PE.9 | PE.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | EMAC_RMII_MDIO | I/O | MFP3 | EMAC RMII PHY Management Data pin. |
| | I2S0_MCLK | O | MFP4 | $I^2S$0 master clock output pin. |
| | SPI2_MISO | I/O | MFP5 | SPI2 MISO (Master In, Slave Out) pin. |
| | USCI1_CTL0 | I/O | MFP6 | USCI1 control 0 pin. |
| | UART2_RXD | I | MFP7 | UART2 data receiver input pin. |
| | EPWM0_CH1 | I/O | MFP10 | EPWM0 channel 1 output/capture input. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | EPWM0_BRAKE1 | I | MFP11 | EPWM0 Brake 1 input pin. |
| | ECAP0_IC1 | I | MFP12 | Enhanced capture unit 0 input 1 pin. |
| | TRACE_DATA0 | O | MFP14 | ETM Trace Data 0 output pin |
| PE.10 | PE.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | EMAC_RMII_TXD0 | O | MFP3 | EMAC RMII Transmit Data bus bit 0. |
| | I2S0_DI | I | MFP4 | $I^2S$0 data input pin. |
| | SPI2_MOSI | I/O | MFP5 | SPI2 MOSI (Master Out, Slave In) pin. |
| | USCI1_DAT0 | I/O | MFP6 | USCI1 data 0 pin. |
| | UART3_TXD | O | MFP7 | UART3 data transmitter output pin. |
| | EPWM0_CH2 | I/O | MFP10 | EPWM0 channel 2 output/capture input. |
| | EPWM1_BRAKE0 | I | MFP11 | EPWM1 Brake 0 input pin. |
| | ECAP0_IC2 | I | MFP12 | Enhanced capture unit 0 input 2 pin. |
| | TRACE_DATA1 | O | MFP14 | ETM Trace Data 1 output pin |
| PE.11 | PE.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | EMAC_RMII_TXD1 | O | MFP3 | EMAC RMII Transmit Data bus bit 1. |
| | I2S0_DO | O | MFP4 | $I^2S$0 data output pin. |
| | SPI2_SS | I/O | MFP5 | SPI2 slave select pin. |
| | USCI1_DAT1 | I/O | MFP6 | USCI1 data 1 pin. |
| | UART3_RXD | I | MFP7 | UART3 data receiver input pin. |
| | UART1_nCTS | I | MFP8 | UART1 clear to Send input pin. |
| | EPWM0_CH3 | I/O | MFP10 | EPWM0 channel 3 output/capture input. |
| | EPWM1_BRAKE1 | I | MFP11 | EPWM1 Brake 1 input pin. |
| | ECAP1_IC2 | I | MFP13 | Enhanced capture unit 1 input 2 pin. |
| | TRACE_DATA2 | O | MFP14 | ETM Trace Data 2 output pin |
| PE.12 | PE.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | EMAC_RMII_TXEN | O | MFP3 | EMAC RMII Transmit Enable output pin. |
| | I2S0_LRCK | O | MFP4 | $I^2S$0 left right channel clock output pin. |
| | SPI2_I2SMCLK | I/O | MFP5 | SPI2 $I^2S$ master clock output pin |
| | USCI1_CLK | I/O | MFP6 | USCI1 clock pin. |
| | UART1_nRTS | O | MFP8 | UART1 request to Send output pin. |
| | EPWM0_CH4 | I/O | MFP10 | EPWM0 channel 4 output/capture input. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | ECAP1_IC1 | I | MFP13 | Enhanced capture unit 1 input 1 pin. |
| | TRACE_DATA3 | O | MFP14 | ETM Trace Data 3 output pin |
| PE.13 | PE.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | EMAC_PPS | O | MFP3 | EMAC Pulse Per Second output pin. |
| | I2C0_SCL | I/O | MFP4 | $I^2C0$ clock pin. |
| | UART4_nRTS | O | MFP5 | UART4 request to Send output pin. |
| | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| | EPWM0_CH5 | I/O | MFP10 | EPWM0 channel 5 output/capture input. |
| | EPWM1_CH0 | I/O | MFP11 | EPWM1 channel 0 output/capture input. |
| | BPWM1_CH5 | I/O | MFP12 | BPWM1 channel 5 output/capture input. |
| | ECAP1_IC0 | I | MFP13 | Enhanced capture unit 1 input 0 pin. |
| PE.14 | PE.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD8 | I/O | MFP2 | EBI address/data bus bit 8. |
| | UART2_TXD | O | MFP3 | UART2 data transmitter output pin. |
| | CAN0_TXD | O | MFP4 | CAN0 bus transmitter output. |
| | SD1_nCD | I | MFP5 | SD/SDIO1 card detect input pin |
| PE.15 | PE.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD9 | I/O | MFP2 | EBI address/data bus bit 9. |
| | UART2_RXD | I | MFP3 | UART2 data receiver input pin. |
| | CAN0_RXD | I | MFP4 | CAN0 bus receiver input. |
| PF.0 | PF.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | UART1_TXD | O | MFP2 | UART1 data transmitter output pin. |
| | I2C1_SCL | I/O | MFP3 | $I^2C1$ clock pin. |
| | BPWM1_CH0 | I/O | MFP12 | BPWM1 channel 0 output/capture input. |
| | ICE_DAT | O | MFP14 | Serial wired debugger data pin. |
| PF.1 | PF.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | UART1_RXD | I | MFP2 | UART1 data receiver input pin. |
| | I2C1_SDA | I/O | MFP3 | $I^2C1$ data input/output pin. |
| | BPWM1_CH1 | I/O | MFP12 | BPWM1 channel 1 output/capture input. |
| | ICE_CLK | I | MFP14 | Serial wired debugger clock pin. |
| PF.2 | PF.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | UART0_RXD | I | MFP3 | UART0 data receiver input pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | I2C0_SDA | I/O | MFP4 | I²C0 data input/output pin. |
| | QSPI0_CLK | I/O | MFP5 | Quad SPI0 serial clock pin. |
| | XT1_OUT | O | MFP10 | External 4~24 MHz (high speed) crystal output pin. |
| | BPWM1_CH1 | I/O | MFP11 | BPWM1 channel 1 output/capture input. |
| PF.3 | PF.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_nCS0 | O | MFP2 | EBI chip select 0 output pin. |
| | UART0_TXD | O | MFP3 | UART0 data transmitter output pin. |
| | I2C0_SCL | I/O | MFP4 | I²C0 clock pin. |
| | XT1_IN | I | MFP10 | External 4~24 MHz (high speed) crystal input pin. |
| | BPWM1_CH0 | I/O | MFP11 | BPWM1 channel 0 output/capture input. |
| PF.4 | PF.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | UART2_TXD | O | MFP2 | UART2 data transmitter output pin. |
| | UART2_nRTS | O | MFP4 | UART2 request to Send output pin. |
| | BPWM0_CH5 | I/O | MFP8 | BPWM0 channel 5 output/capture input. |
| | X32_OUT | O | MFP10 | External 32.768 kHz crystal output pin. |
| PF.5 | PF.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | UART2_RXD | I | MFP2 | UART2 data receiver input pin. |
| | UART2_nCTS | I | MFP4 | UART2 clear to Send input pin. |
| | BPWM0_CH4 | I/O | MFP8 | BPWM0 channel 4 output/capture input. |
| | EPWM0_SYNC_OUT | O | MFP9 | EPWM0 counter synchronous trigger output pin. |
| | X32_IN | I | MFP10 | External 32.768 kHz crystal input pin. |
| | EADC0_ST | I | MFP11 | EADC0 external trigger input. |
| PF.6 | PF.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR19 | O | MFP2 | EBI address bus bit 19. |
| | SC0_CLK | O | MFP3 | Smart Card 0 clock pin. |
| | I2S0_LRCK | O | MFP4 | I²S0 left right channel clock output pin. |
| | SPI0_MOSI | I/O | MFP5 | SPI0 MOSI (Master Out, Slave In) pin. |
| | UART4_RXD | I | MFP6 | UART4 data receiver input pin. |
| | EBI_nCS0 | O | MFP7 | EBI chip select 0 output pin. |
| | TAMPER0 | I/O | MFP10 | TAMPER detector loop pin 0. |
| PF.7 | PF.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR18 | O | MFP2 | EBI address bus bit 18. |
| | SC0_DAT | I/O | MFP3 | Smart Card 0 data pin. |
| | I2S0_DO | O | MFP4 | I²S0 data output pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | SPI0_MISO | I/O | MFP5 | SPI0 MISO (Master In, Slave Out) pin. |
| | UART4_TXD | O | MFP6 | UART4 data transmitter output pin. |
| | TAMPER1 | I/O | MFP10 | TAMPER detector loop pin 1. |
| PF.8 | PF.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR17 | O | MFP2 | EBI address bus bit 17. |
| | SC0_RST | O | MFP3 | Smart Card 0 reset pin. |
| | I2S0_DI | I | MFP4 | $I^2S0$ data input pin. |
| | SPI0_CLK | I/O | MFP5 | SPI0 serial clock pin. |
| | TAMPER2 | I/O | MFP10 | TAMPER detector loop pin 2. |
| PF.9 | PF.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR16 | O | MFP2 | EBI address bus bit 16. |
| | SC0_PWR | O | MFP3 | Smart Card 0 power pin. |
| | I2S0_MCLK | O | MFP4 | $I^2S0$ master clock output pin. |
| | SPI0_SS | I/O | MFP5 | SPI0 slave select pin. |
| | TAMPER3 | I/O | MFP10 | TAMPER detector loop pin 3. |
| PF.10 | PF.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR15 | O | MFP2 | EBI address bus bit 15. |
| | SC0_nCD | I | MFP3 | Smart Card 0 card detect pin. |
| | I2S0_BCLK | O | MFP4 | $I^2S0$ bit clock output pin. |
| | SPI0_I2SMCLK | I/O | MFP5 | SPI0 $I^2S$ master clock output pin |
| | TAMPER4 | I/O | MFP10 | TAMPER detector loop pin 4. |
| PF.11 | PF.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR14 | O | MFP2 | EBI address bus bit 14. |
| | SPI2_MOSI | I/O | MFP3 | SPI2 MOSI (Master Out, Slave In) pin. |
| | TAMPER5 | I/O | MFP10 | TAMPER detector loop pin 5. |
| | TM3 | I/O | MFP13 | Timer3 event counter input/toggle output pin. |
| PG.0 | PG.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR8 | O | MFP2 | EBI address bus bit 8. |
| | I2C0_SCL | I/O | MFP4 | $I^2C0$ clock pin. |
| | I2C1_SMBAL | O | MFP5 | $I^2C1$ SMBus SMBALTER pin |
| | UART2_RXD | I | MFP6 | UART2 data receiver input pin. |
| | CAN1_TXD | O | MFP7 | CAN1 bus transmitter output. |
| | UART1_TXD | O | MFP8 | UART1 data transmitter output pin. |
| PG.1 | PG.1 | I/O | MFP0 | General purpose digital I/O pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | EBI_ADR9 | O | MFP2 | EBI address bus bit 9. |
| | SPI2_I2SMCLK | I/O | MFP3 | SPI2 $I^2S$ master clock output pin |
| | I2C0_SDA | I/O | MFP4 | $I^2C0$ data input/output pin. |
| | I2C1_SMBSUS | O | MFP5 | $I^2C1$ SMBus SMBSUS pin (PMBus CONTROL pin) |
| | UART2_TXD | O | MFP6 | UART2 data transmitter output pin. |
| | CAN1_RXD | I | MFP7 | CAN1 bus receiver input. |
| | UART1_RXD | I | MFP8 | UART1 data receiver input pin. |
| PG.2 | PG.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR11 | O | MFP2 | EBI address bus bit 11. |
| | SPI2_SS | I/O | MFP3 | SPI2 slave select pin. |
| | I2C0_SMBAL | O | MFP4 | $I^2C0$ SMBus SMBALTER pin |
| | I2C1_SCL | I/O | MFP5 | $I^2C1$ clock pin. |
| | TM0 | I/O | MFP13 | Timer0 event counter input/toggle output pin. |
| PG.3 | PG.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR12 | O | MFP2 | EBI address bus bit 12. |
| | SPI2_CLK | I/O | MFP3 | SPI2 serial clock pin. |
| | I2C0_SMBSUS | O | MFP4 | $I^2C0$ SMBus SMBSUS pin (PMBus CONTROL pin) |
| | I2C1_SDA | I/O | MFP5 | $I^2C1$ data input/output pin. |
| | TM1 | I/O | MFP13 | Timer1 event counter input/toggle output pin. |
| PG.4 | PG.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR13 | O | MFP2 | EBI address bus bit 13. |
| | SPI2_MISO | I/O | MFP3 | SPI2 MISO (Master In, Slave Out) pin. |
| | TM2 | I/O | MFP13 | Timer2 event counter input/toggle output pin. |
| PG.5 | PG.5 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_nCS1 | O | MFP2 | EBI chip select 1 output pin. |
| | SPI3_SS | I/O | MFP3 | SPI3 slave select pin. |
| | SC1_PWR | O | MFP4 | Smart Card 1 power pin. |
| | EPWM0_CH3 | I/O | MFP11 | EPWM0 channel 3 output/capture input. |
| PG.6 | PG.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_nCS2 | O | MFP2 | EBI chip select 2 output pin. |
| | SPI3_CLK | I/O | MFP3 | SPI3 serial clock pin. |
| | SC1_RST | O | MFP4 | Smart Card 1 reset pin. |
| | EPWM0_CH2 | I/O | MFP11 | EPWM0 channel 2 output/capture input. |
| PG.7 | PG.7 | I/O | MFP0 | General purpose digital I/O pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | EBI_nWRL | O | MFP2 | EBI low byte write enable output pin. |
| | SPI3_MISO | I/O | MFP3 | SPI3 MISO (Master In, Slave Out) pin. |
| | SC1_DAT | I/O | MFP4 | Smart Card 1 data pin. |
| | EPWM0_CH1 | I/O | MFP11 | EPWM0 channel 1 output/capture input. |
| PG.8 | PG.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_nWRH | O | MFP2 | EBI high byte write enable output pin |
| | SPI3_MOSI | I/O | MFP3 | SPI3 MOSI (Master Out, Slave In) pin. |
| | SC1_CLK | O | MFP4 | Smart Card 1 clock pin. |
| | EPWM0_CH0 | I/O | MFP11 | EPWM0 channel 0 output/capture input. |
| PG.9 | PG.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD0 | I/O | MFP2 | EBI address/data bus bit 0. |
| | SD1_DAT3 | I/O | MFP3 | SD/SDIO1 data line bit 3. |
| | SPIM_D2 | I/O | MFP4 | SPIM data 2 pin for Quad Mode I/O. |
| | BPWM0_CH5 | I/O | MFP12 | BPWM0 channel 5 output/capture input. |
| PG.10 | PG.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD1 | I/O | MFP2 | EBI address/data bus bit 1. |
| | SD1_DAT2 | I/O | MFP3 | SD/SDIO1 data line bit 2. |
| | SPIM_D3 | I/O | MFP4 | SPIM data 3 pin for Quad Mode I/O. |
| | BPWM0_CH4 | I/O | MFP12 | BPWM0 channel 4 output/capture input. |
| PG.11 | PG.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD2 | I/O | MFP2 | EBI address/data bus bit 2. |
| | SD1_DAT1 | I/O | MFP3 | SD/SDIO1 data line bit 1. |
| | SPIM_SS | I/O | MFP4 | SPIM slave select pin. |
| | BPWM0_CH3 | I/O | MFP12 | BPWM0 channel 3 output/capture input. |
| PG.12 | PG.12 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD3 | I/O | MFP2 | EBI address/data bus bit 3. |
| | SD1_DAT0 | I/O | MFP3 | SD/SDIO1 data line bit 0. |
| | SPIM_CLK | I/O | MFP4 | SPIM serial clock pin. |
| | BPWM0_CH2 | I/O | MFP12 | BPWM0 channel 2 output/capture input. |
| PG.13 | PG.13 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD4 | I/O | MFP2 | EBI address/data bus bit 4. |
| | SD1_CMD | I/O | MFP3 | SD/SDIO1 command/response pin |
| | SPIM_MISO | I/O | MFP4 | SPIM MISO (Master In, Slave Out) pin. |
| | BPWM0_CH1 | I/O | MFP12 | BPWM0 channel 1 output/capture input. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| PG.14 | PG.14 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD5 | I/O | MFP2 | EBI address/data bus bit 5. |
| | SD1_CLK | O | MFP3 | SD/SDIO1 clock output pin |
| | SPIM_MOSI | I/O | MFP4 | SPIM MOSI (Master Out, Slave In) pin. |
| | BPWM0_CH0 | I/O | MFP12 | BPWM0 channel 0 output/capture input. |
| PG.15 | PG.15 | I/O | MFP0 | General purpose digital I/O pin. |
| | SD1_nCD | I | MFP3 | SD/SDIO1 card detect input pin |
| | CLKO | O | MFP14 | Clock Out |
| | EADC0_ST | I | MFP15 | EADC0 external trigger input. |
| PH.0 | PH.0 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR7 | O | MFP2 | EBI address bus bit 7. |
| | UART5_TXD | O | MFP4 | UART5 data transmitter output pin. |
| | TM0_EXT | I/O | MFP13 | Timer0 external capture input/toggle output pin. |
| PH.1 | PH.1 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR6 | O | MFP2 | EBI address bus bit 6. |
| | UART5_RXD | I | MFP4 | UART5 data receiver input pin. |
| | TM1_EXT | I/O | MFP13 | Timer1 external capture input/toggle output pin. |
| PH.2 | PH.2 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR5 | O | MFP2 | EBI address bus bit 5. |
| | UART5_nRTS | O | MFP4 | UART5 request to Send output pin. |
| | UART4_TXD | O | MFP5 | UART4 data transmitter output pin. |
| | I2C0_SCL | I/O | MFP6 | $I^2C0$ clock pin. |
| | TM2_EXT | I/O | MFP13 | Timer2 external capture input/toggle output pin. |
| PH.3 | PH.3 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR4 | O | MFP2 | EBI address bus bit 4. |
| | SPI1_I2SMCLK | I/O | MFP3 | SPI1 $I^2S$ master clock output pin |
| | UART5_nCTS | I | MFP4 | UART5 clear to Send input pin. |
| | UART4_RXD | I | MFP5 | UART4 data receiver input pin. |
| | I2C0_SDA | I/O | MFP6 | $I^2C0$ data input/output pin. |
| | TM3_EXT | I/O | MFP13 | Timer3 external capture input/toggle output pin. |
| PH.4 | PH.4 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR3 | O | MFP2 | EBI address bus bit 3. |
| | SPI1_MISO | I/O | MFP3 | SPI1 MISO (Master In, Slave Out) pin. |
| PH.5 | PH.5 | I/O | MFP0 | General purpose digital I/O pin. |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | EBI_ADR2 | O | MFP2 | EBI address bus bit 2. |
| | SPI1_MOSI | I/O | MFP3 | SPI1 MOSI (Master Out, Slave In) pin. |
| PH.6 | PH.6 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR1 | O | MFP2 | EBI address bus bit 1. |
| | SPI1_CLK | I/O | MFP3 | SPI1 serial clock pin. |
| PH.7 | PH.7 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_ADR0 | O | MFP2 | EBI address bus bit 0. |
| | SPI1_SS | I/O | MFP3 | SPI1 slave select pin. |
| PH.8 | PH.8 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD12 | I/O | MFP2 | EBI address/data bus bit 12. |
| | QSPI0_CLK | I/O | MFP3 | Quad SPI0 serial clock pin. |
| | SC2_PWR | O | MFP4 | Smart Card 2 power pin. |
| | I2S0_DI | I | MFP5 | $I^2S0$ data input pin. |
| | SPI1_CLK | I/O | MFP6 | SPI1 serial clock pin. |
| | UART3_nRTS | O | MFP7 | UART3 request to Send output pin. |
| | I2C1_SMBAL | O | MFP8 | $I^2C1$ SMBus SMBALTER pin |
| | I2C2_SCL | I/O | MFP9 | $I^2C2$ clock pin. |
| | UART1_TXD | O | MFP10 | UART1 data transmitter output pin. |
| PH.9 | PH.9 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD13 | I/O | MFP2 | EBI address/data bus bit 13. |
| | QSPI0_SS | I/O | MFP3 | Quad SPI0 slave select pin. |
| | SC2_RST | O | MFP4 | Smart Card 2 reset pin. |
| | I2S0_DO | O | MFP5 | $I^2S0$ data output pin. |
| | SPI1_SS | I/O | MFP6 | SPI1 slave select pin. |
| | UART3_nCTS | I | MFP7 | UART3 clear to Send input pin. |
| | I2C1_SMBSUS | O | MFP8 | $I^2C1$ SMBus SMBSUS pin (PMBus CONTROL pin) |
| | I2C2_SDA | I/O | MFP9 | $I^2C2$ data input/output pin. |
| | UART1_RXD | I | MFP10 | UART1 data receiver input pin. |
| PH.10 | PH.10 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD14 | I/O | MFP2 | EBI address/data bus bit 14. |
| | QSPI0_MISO1 | I/O | MFP3 | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | SC2_nCD | I | MFP4 | Smart Card 2 card detect pin. |
| | I2S0_LRCK | O | MFP5 | $I^2S0$ left right channel clock output pin. |
| | SPI1_I2SMCLK | I/O | MFP6 | SPI1 $I^2S$ master clock output pin |

| | Pin Name | Type | MFP | Description |
|---|---|---|---|---|
| | UART4_TXD | O | MFP7 | UART4 data transmitter output pin. |
| | UART0_TXD | O | MFP8 | UART0 data transmitter output pin. |
| PH.11 | PH.11 | I/O | MFP0 | General purpose digital I/O pin. |
| | EBI_AD15 | I/O | MFP2 | EBI address/data bus bit 15. |
| | QSPI0_MOSI1 | I/O | MFP3 | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | UART4_RXD | I | MFP7 | UART4 data receiver input pin. |
| | UART0_RXD | I | MFP8 | UART0 data receiver input pin. |
| | EPWM0_CH5 | I/O | MFP11 | EPWM0 channel 5 output/capture input. |

# 5 BLOCK DIAGRAM

## 5.1 NuMicro® M480 Block Diagram

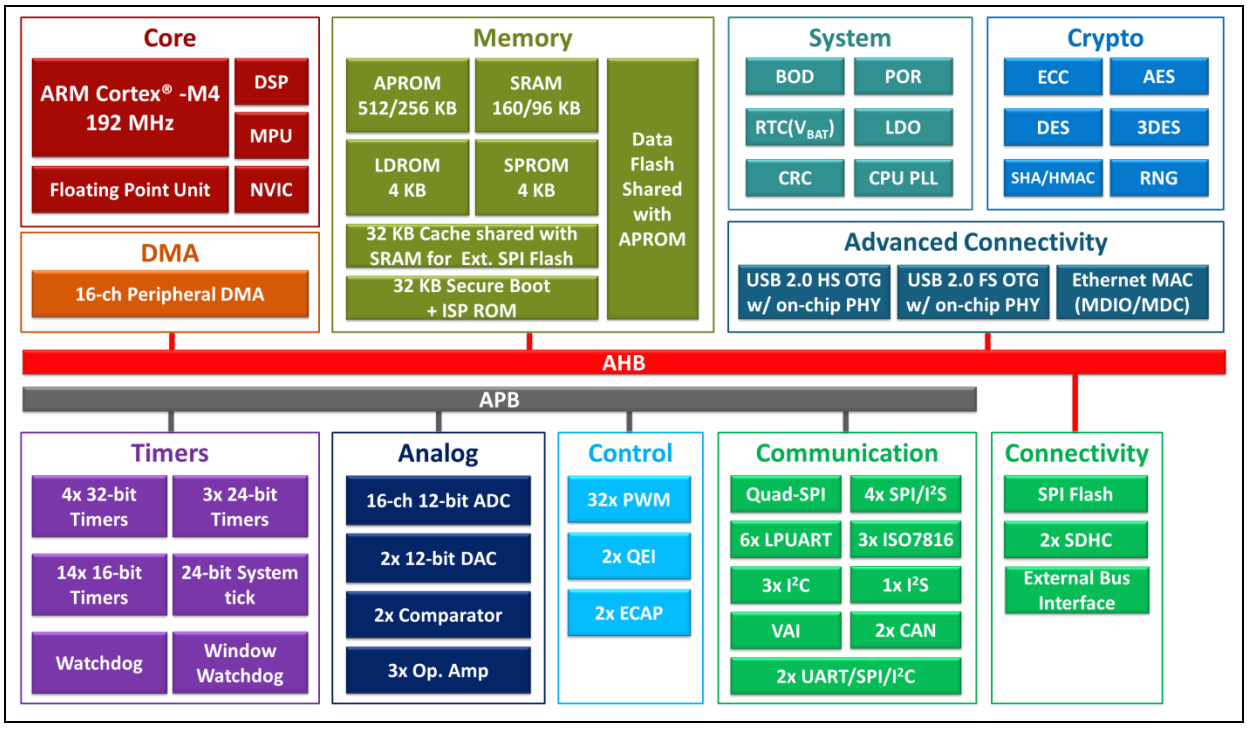



Figure 5.1-1 NuMicro® M480 Block Diagram

# 6 FUNCTIONAL DESCRIPTION

## 6.1 ARM® Cortex®-M4 Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The NuMicro® M480 series is embedded with Cortex®-M4F processor. Throughout this document, the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. Figure 6.1-1 shows the functional controller of the processor.

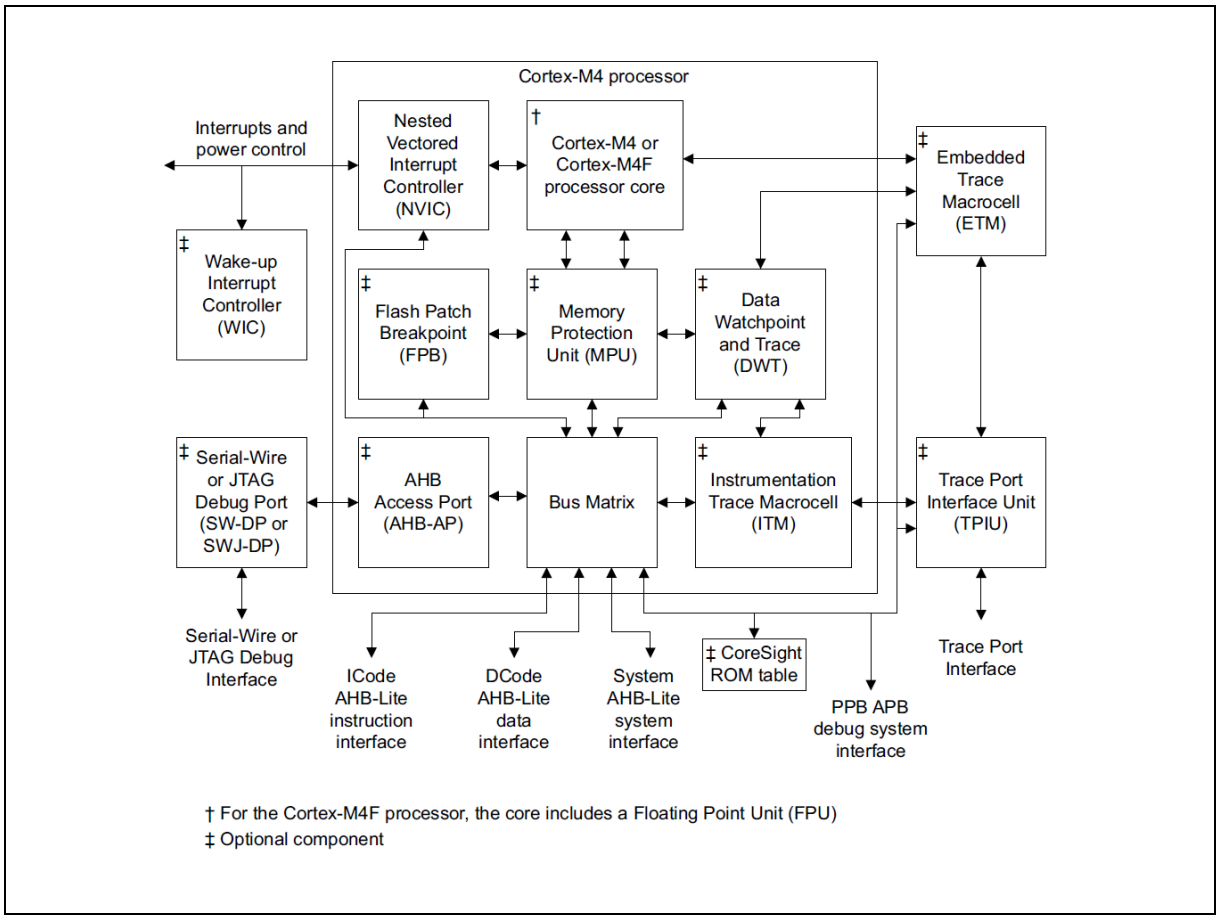



Figure 6.1-1 Cortex®-M4 Block Diagram

**Cortex®-M4 processor features:**

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the *ARMv7-M Architecture Reference Manual*
  - Banked Stack Pointer (SP)
  - Hardware integer divide instructions, SDIV and UDIV
  - Handler and Thread modes

- Thumb and Debug states
- Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
- Automatic processor state saving and restoration for low latency *Interrupt Service Routine (ISR)* entry and exit
- Support for ARMv6 big-endian byte-invariant or little-endian accesses
- Support for ARMv6 unaligned accesses

- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the NuMicro® M480 series configured with 64 interrupts)
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tril-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
  - Serial Wire Debug Port(SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access
  - Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and

code patches

- Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
- Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
- Optional Embedded Trace Macrocell (ETM) for instruction trace.

- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

## 6.2 System Manager

### 6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

### 6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M4 core only by writing 1 to CPURST (SYS_IPRST0[1])

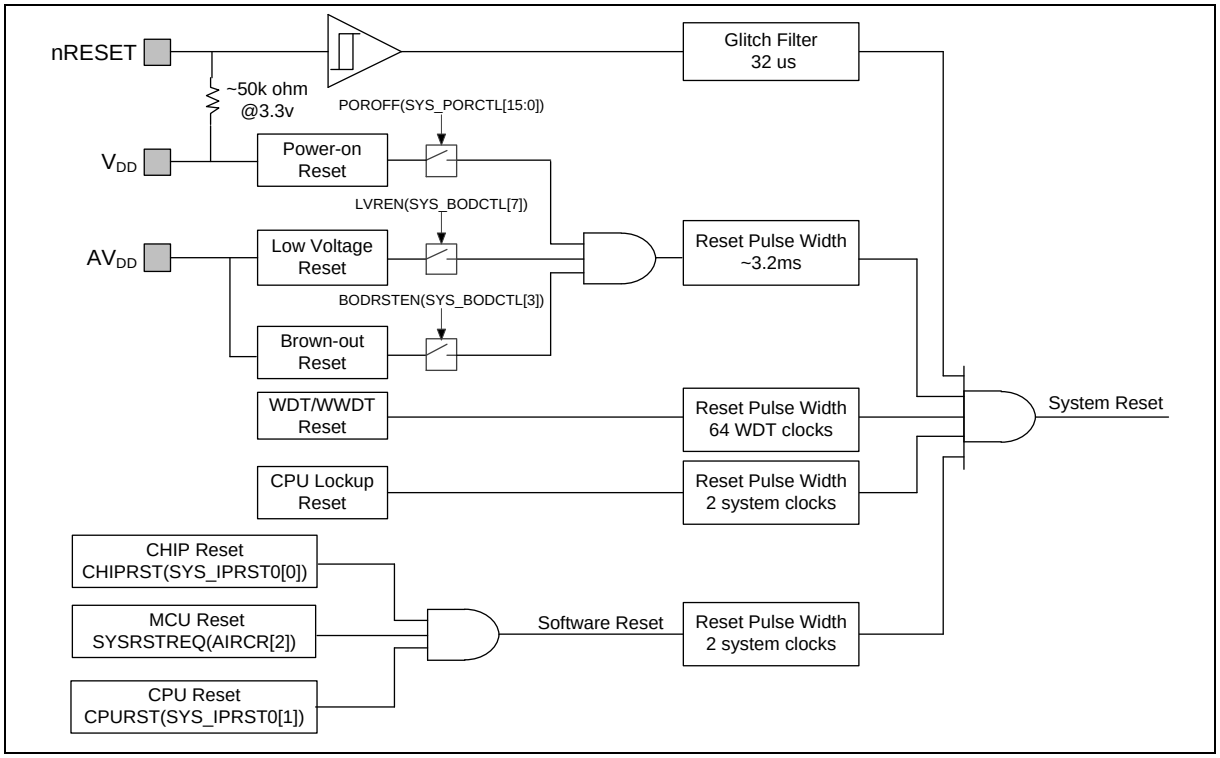



Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M4 only; the other reset sources will reset Cortex®-M4 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1

| Reset Sources<br>Register | POR | NRESET | WDT | LVR | BOD | Lockup | CHIP | MCU | CPU |
|---|---|---|---|---|---|---|---|---|---|
| **SYS_RSTSTS** | Bit 0 = 1 | Bit 1 = 1 | Bit 2 = 1 | Bit 3 = 1 | Bit 4 = 1 | Bit 8 = 1 | Bit 0 = 1 | Bit 5 = 1 | Bit 7 = 1 |
| **CHIPRST**<br>**(SYS_IPRST0[0])** | 0x0 | - | - | - | - | - | - | - | - |
| **BODEN**<br>**(SYS_BODCTL[0])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - |
| **BODVL**<br>**(SYS_BODCTL[2:1])** | | | | | | | | | |
| **BODRSTEN**<br>**(SYS_BODCTL[3])** | | | | | | | | | |
| **HXTEN**<br>**(CLK_PWRCTL[0])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | |
| **LXTEN**<br>**(CLK_PWRCTL[1])** | 0x0 | - | - | - | - | - | - | - | - |
| **WDTCKEN**<br>**(CLK_APBCLK0[0])** | 0x1 | - | 0x1 | - | - | - | 0x1 | - | - |
| **HCLKSEL** | Reload from | Reload from | Reload from | Reload from | Reload from | Reload from | Reload from | Reload from | - |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **(CLK_CLKSEL0[2:0])** | CONFIG0 | CONFIG0 | CONFIG0 | CONFIG0 | CONFIG0 | CONFIG0 | CONFIG0 | CONFIG0 | |
| **WDTSEL (CLK_CLKSEL1[1:0])** | 0x3 | 0x3 | - | - | - | - | - | - | - |
| **HXTSTB (CLK_STATUS[0])** | 0x0 | - | - | - | - | - | - | - | - |
| **LXTSTB (CLK_STATUS[1])** | 0x0 | - | - | - | - | - | - | - | - |
| **PLLSTB (CLK_STATUS[2])** | 0x0 | - | - | - | - | - | - | - | - |
| **HIRCSTB (CLK_STATUS[4])** | 0x0 | - | - | - | - | - | - | - | - |
| **CLKSFAIL (CLK_STATUS[7])** | 0x0 | 0x0 | - | - | - | - | - | - | - |
| **RSTEN (WDT_CTL[1])**<br>**WDTEN (WDT_CTL[7])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | - | - |
| **WDT_CTL except bit 1 and bit 7.** | 0x0700 | 0x0700 | 0x0700 | 0x0700 | 0x0700 | - | 0x0700 | - | - |
| **WDT_ALTCTL** | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | - | 0x0000 | - | - |
| **WWDT_RLDCNT** | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | - | 0x0000 | - | - |
| **WWDT_CTL** | 0x3F0800 | 0x3F0800 | 0x3F0800 | 0x3F0800 | 0x3F0800 | - | 0x3F0800 | - | - |
| **WWDT_STATUS** | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | - | 0x0000 | - | - |
| **WWDT_CNT** | 0x3F | 0x3F | 0x3F | 0x3F | 0x3F | - | 0x3F | - | - |
| **BS (FMC_ISPCTL[1])**<br>**BL (FMC_ISPCTL[16])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | - | - |
| **FMC_DFBA** | Reload from CONFIG1 | Reload from CONFIG1 | Reload from CONFIG1 | Reload from CONFIG1 | Reload from CONFIG1 | - | Reload from CONFIG1 | - | - |
| **CBS (FMC_ISPSTS[2:1])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | - | - |
| **VECMAP (FMC_ISPSTS[23:9])** | Reload base on CONFIG0 | Reload base on CONFIG0 | Reload base on CONFIG0 | Reload base on CONFIG0 | Reload base on CONFIG0 | - | Reload base on CONFIG0 | - | - |
| **Other Peripheral Registers** | Reset Value | | | | | | | | - |
| **FMC Registers** | Reset Value | | | | | | | | |
| **Note:** '-' means that the value of register keeps original setting. | | | | | | | | | |

Table 6.2-1 Reset Value of Registers

#### 6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 $V_{DD}$ and the state keeps longer than 66 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 $V_{DD}$ and the state keeps longer than 66 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

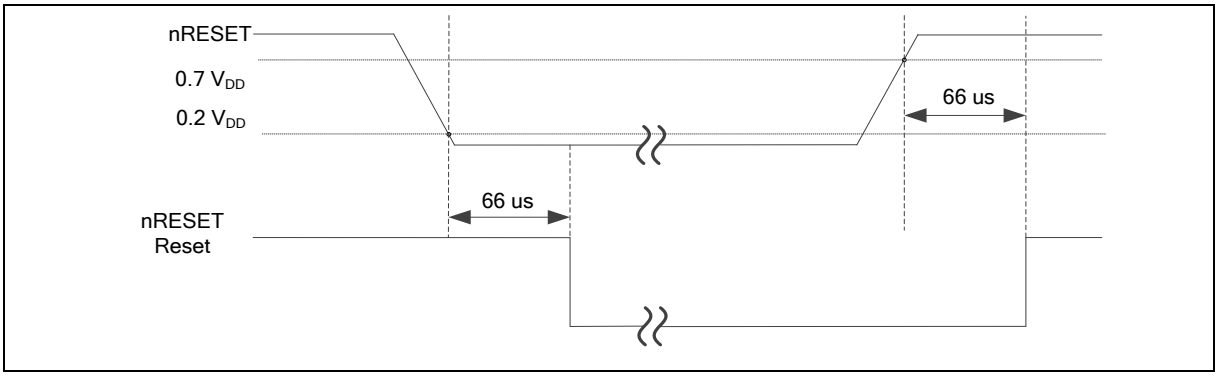



Figure 6.2-2 nRESET Reset Waveform

#### 6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and force the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

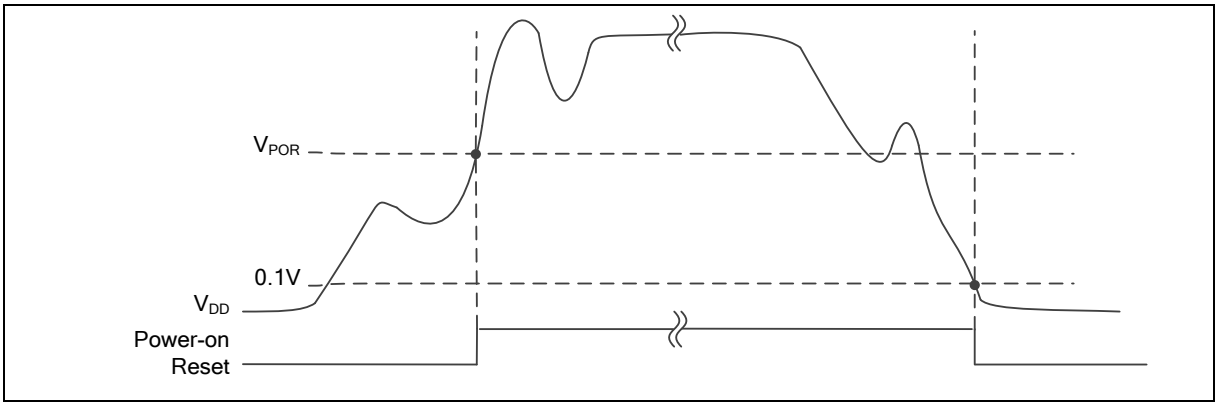



Figure 6.2-3 Power-on Reset (POR) Waveform

#### 6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect $AV_{DD}$ during system operation. When the $AV_{DD}$ voltage is lower than $V_{LVR}$ and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the

$AV_{DD}$ voltage rises above $V_{LVR}$ and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

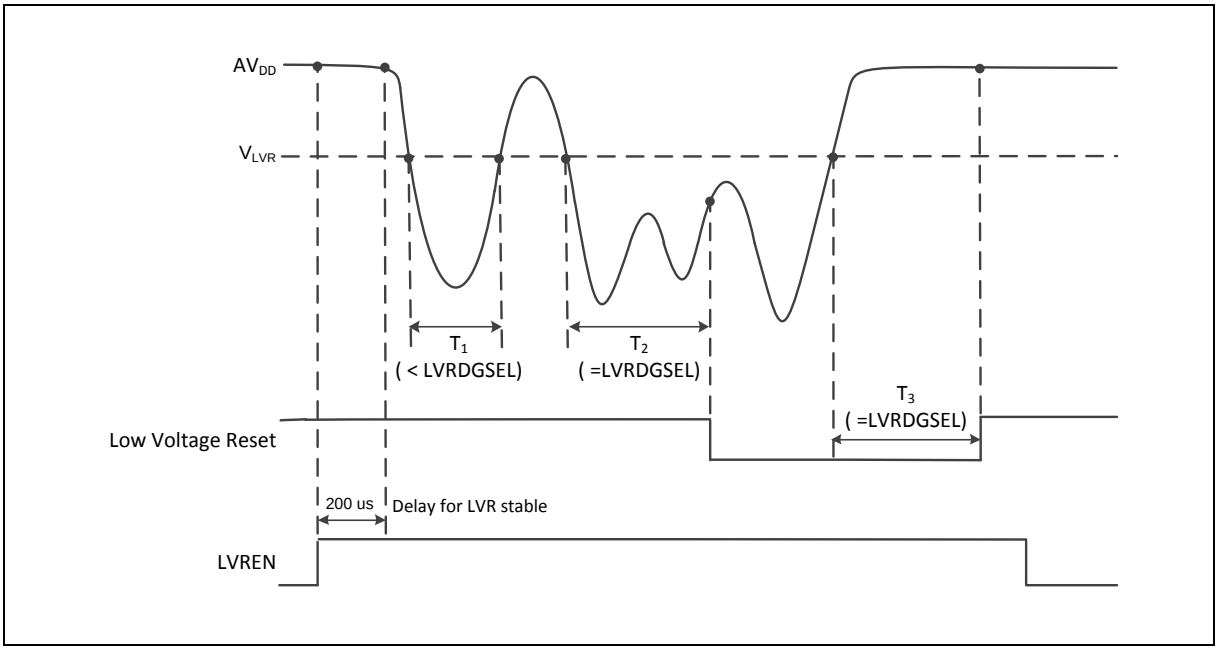



Figure 6.2-4 Low Voltage Reset (LVR) Waveform

#### *6.2.2.4 Brown-out Detector Reset (BOD Reset)*

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect $AV_{DD}$ during system operation. When the $AV_{DD}$ voltage is lower than $V_{BOD}$ which is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the $AV_{DD}$ voltage rises above $V_{BOD}$ and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

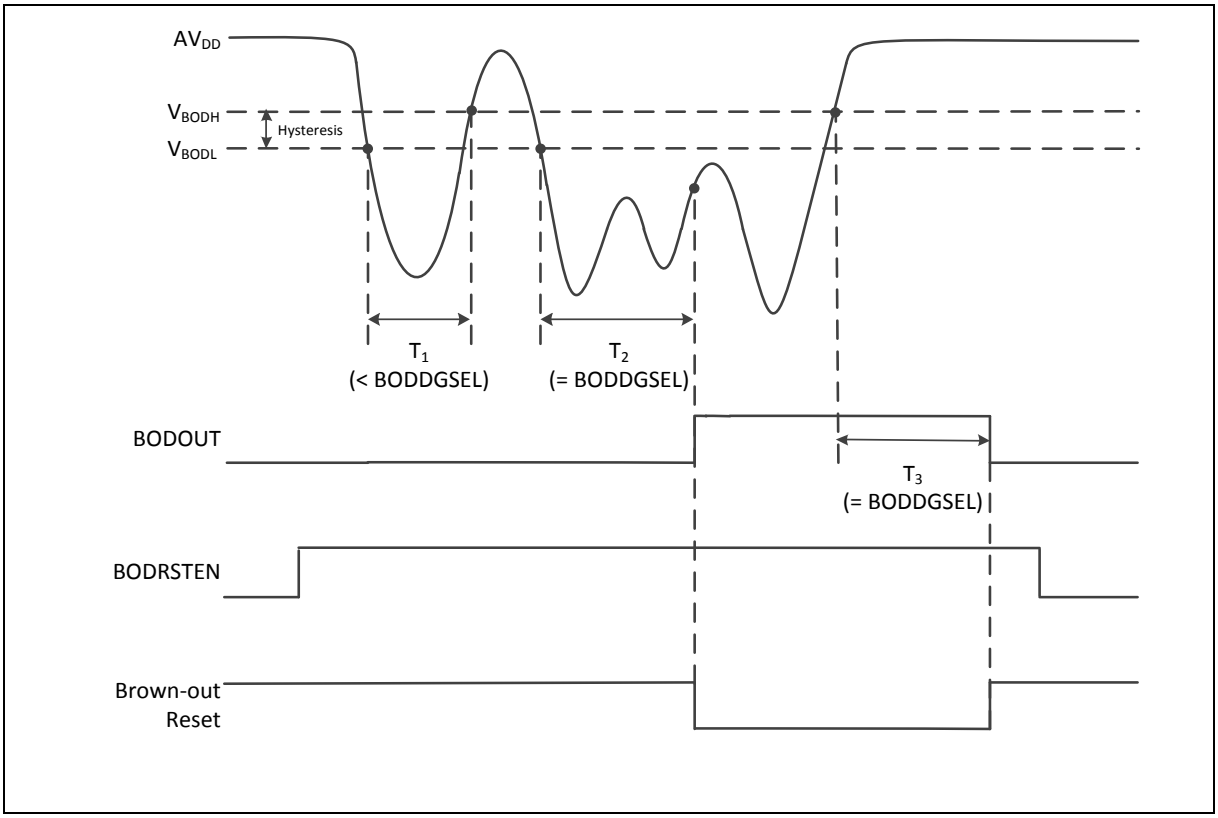



Figure 6.2-5 Brown-out Detector (BOD) Waveform

#### *6.2.2.5 Watchdog Timer Reset (WDT)*

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

#### *6.2.2.6 CPU Lockup Reset*

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built-in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

#### *6.2.2.7 CPU Reset, CHIP Reset and MCU Reset*

The CPU Reset means only Cortex®-M4 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is the same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

### 6.2.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from $AV_{DD}$ and $AV_{SS}$ provides the power for analog components operation.
- Digital power from $V_{DD}$ and $V_{SS}$ supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.
- RTC power from $V_{DD}$ provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power ($AV_{DD}$) should be the same voltage level of the digital power ($V_{DD}$). Figure 6.2-6 shows the NuMicro® M480 power distribution.

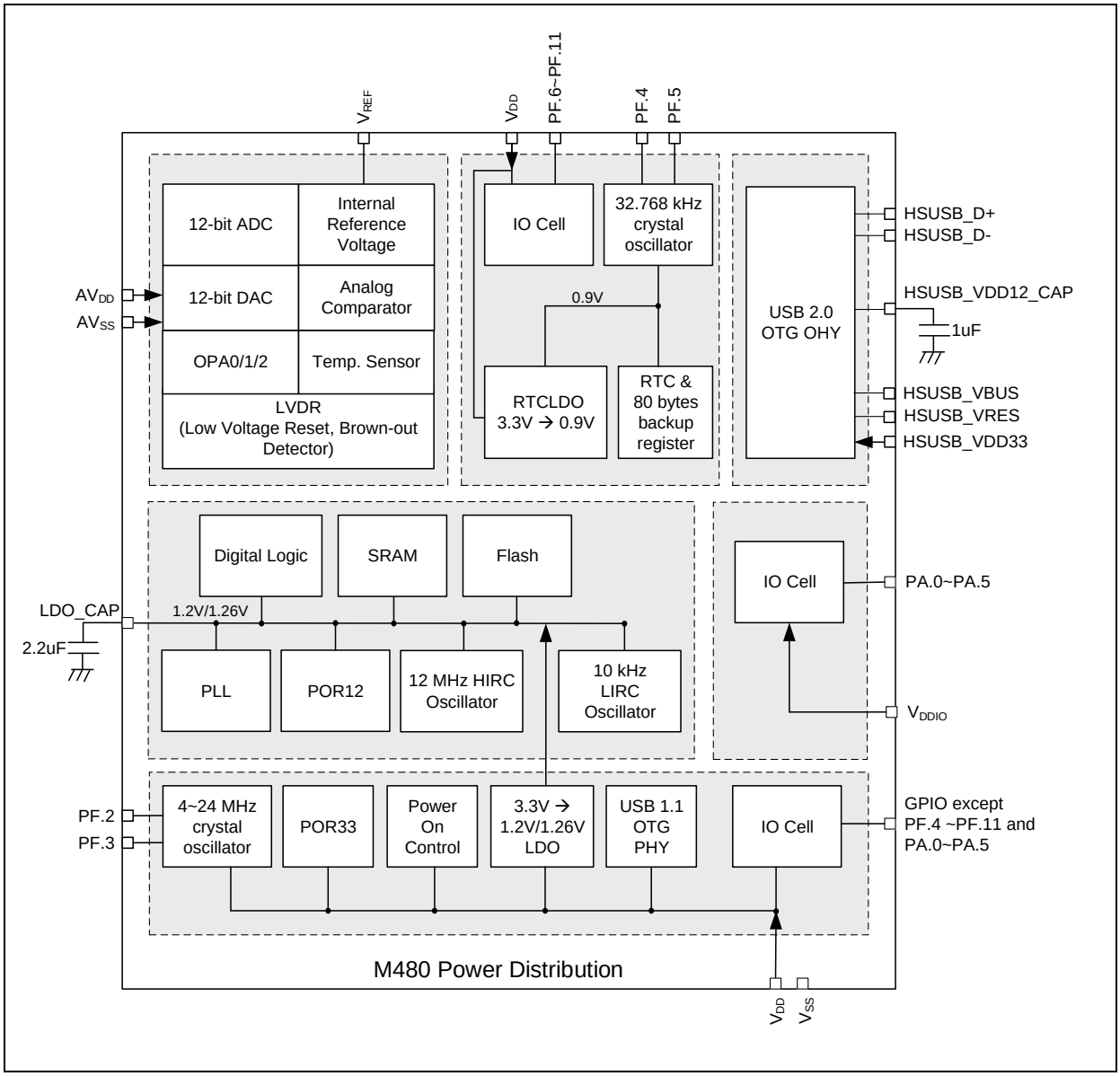



Figure 6.2-6 NuMicro® M480 Power Distribution Diagram

### 6.2.4 Power Modes and Wake-up Sources

The NuMicro® M480 series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power modes in the NuMicro® M480 series.

| Mode | CPU Operating Maximum Speed (MHz) | LDO_CAP (V) | Clock Disable |
|---|---|---|---|
| **Normal mode** | 160 | 1.20 | All clocks are disabled by control register. |
| **Turbo mode** | 192 | 1.26 | All clocks are disabled by control register. |
| **Idle mode** | CPU enter Sleep mode | 1.20/1.26 | Only CPU clock is disabled. |
| **Fast Wakeup Power-down mode (FWPD)** | CPU enters Deep Sleep mode | 1.20/1.26 | Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT. |
| **Normal Power-down mode (NPD)** | CPU enters Deep Sleep mode | 1.20/1.26 | Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT. |
| **Low leakage Power-down mode (LLPD)** | CPU enters Deep Sleep mode | 0.9 | Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT. |
| **Standby Power-down mode 0 (SPD0)** | Power off | Floating | Only LIRC/LXT still enable for RTC function and wake-up timer usage |
| **Standby Power-down mode 1 (SPD1)** | Power off | Floating | Only LIRC/LXT still enable for RTC function and wake-up timer usage |
| **Deep Power-down mode (DPD)** | Power off | Floating | Only LIRC/LXT still enable for RTC function and wake-up timer usage |

Table 6.2-2 Power Mode Table

**Note:**User must turn on LIRC before entering SPD0/1 mode.

There are different power mode entry settings. Each power mode has different entry setting and leaving condition. Table 6.2 3 shows the entry setting for each power mode. When chip power-on, chip is running as normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT:[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction..

| Register/Instruction Mode | SLEEPDEEP (SCR[2]) | PDEN (CLK_PWRCTL[7]) | PDMSEL (CLK_PMUCTL[2:0]) |
|---|---|---|---|
| **Fast Wakeup Power-down mode** | 1 | 1 | 2 |
| **Normal Power-down mode** | 1 | 1 | 0 |
| **Low leakage Power-down mode** | 1 | 1 | 1 |

| | | | |
|---|---|---|---|
| **Standby Power-down mode 0**[1] | 1 | 1 | 4 |
| **Standby Power-down mode 1**[1] | 1 | 1 | 5 |
| **Deep Power-down mode** | 1 | 1 | 6 |

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

| **Power Mode** | **Normal Mode** | **Idle Mode** | **Power-Down Mode** |
|---|---|---|---|
| **Definition** | CPU is in active state | CPU is in sleep state | CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended. |
| **Entry Condition** | Chip is in normal mode after system reset released | CPU executes WFI instruction. | CPU sets sleep mode enable and power down enable and executes WFI instruction. |
| **Wake-up Sources** | N/A | All interrupts | RTC, WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI, USBD, ACMP and BOD. |
| **Available Clocks** | All | All except CPU clock | LXT and LIRC |
| **After Wake-up** | N/A | CPU back to normal mode | CPU back to normal mode |

Table 6.2-4 Power Mode Definition Table

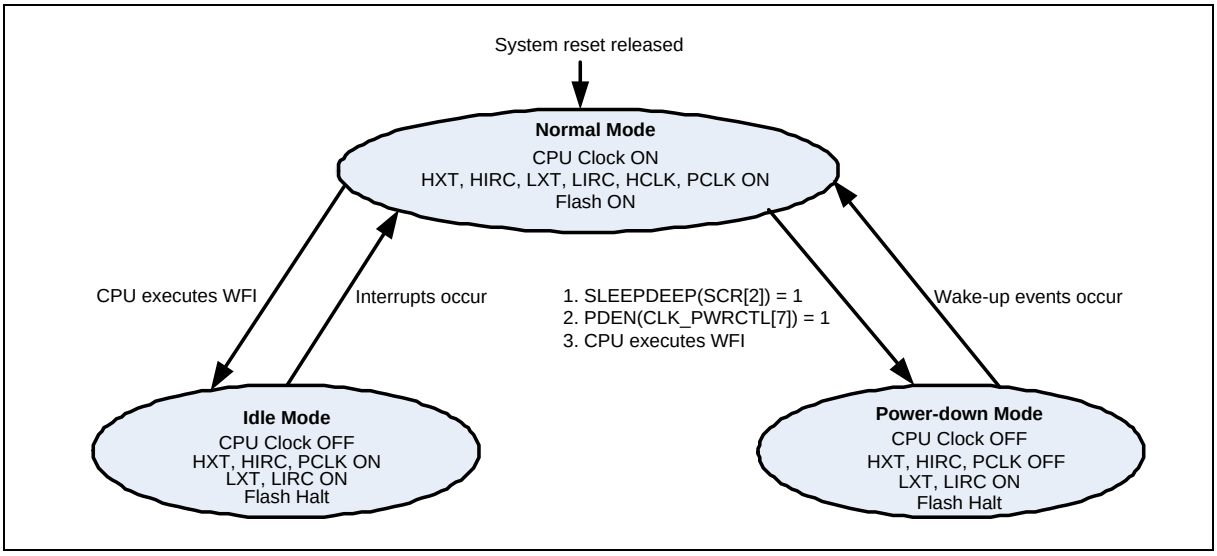



Figure 6.2-7 Power Mode State Machine

| | **Idle Mode** | **NPD, LLPD, FWPD** | **SPD0, SPD1,** | **DPD** |
|---|---|---|---|---|
| HXT | ON | Halt | Halt | Halt |
| HIRC | ON | Halt | Halt | Halt |
| LXT | ON | ON/OFF[1] | ON/OFF[1] | ON/OFF[1] |

| | | | | |
|---|---|---|---|---|
| LIRC | ON | ON/OFF[2] | ON/OFF[2] | ON/OFF[2] |
| PLL | ON | Halt | Halt | Halt |
| HCLK/PCLK | ON | Halt | Halt | Halt |
| CPU | Halt | Halt | Halt | Halt |
| SRAM Retention | ON | ON | Halt | Halt |
| FLASH | ON | Halt | Halt | Halt |
| TIMER | ON | ON/OFF[3] | ON/OFF[3] | Halt |
| WDT | ON | ON/OFF[4] | ON/OFF[4] | Halt |
| RTC | ON | ON/OFF[5] | ON/OFF[5] | Halt |
| UART | ON | ON/OFF[6] | ON/OFF[6] | Halt |
| Others | ON | Halt | Halt | Halt |

Table 6.2-5 Clocks in Power Modes

**Note:**

1. LXT ON or OFF depends on SW setting in normal mode.
2. LIRC ON or OFF depends on S/W setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.

**Wake-up sources in Normal Power-down mode (NPD):**

RTC, WDT, I²C, Timer, UART, USCI, BOD, EBOD, GPIO, USBD, and ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and executing WFI to enter Power-down mode.

| Wake-Up Source | Wake-Up Condition | Power-Down Mode | | | Re-Entering Power-Down Mode Condition |
|---|---|---|---|---|---|
| | | NPD/ FWPD/ LLPD | SPD0/1 | DPD | |
| BOD | Brown-Out Detector Reset / Interrupt | V | - | - | After software writes 1 to clear BODIF (SYS_BODCTL[4]). |
| | Brown-Out Detector Reset | - | V | - | After software writes 1 to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered. |
| LVR | LVR Reset | V | - | - | After software writes 1 to clear LVRF (SYS_RSTSTS[3]) |
| | | - | V | - | After software writes 1 to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered. |
| POR | POR Reset | V | V | - | After software writes 1 to clear PORF (SYS_RSTSTS[0]) |

| | | | | | |
|---|---|---|---|---|---|
| INT | External Interrupt | V | - | - | After software write 1 to clear the Px_INTSRC[n] bit. |
| GPIO | GPIO Interrupt | V | - | - | After software write 1 to clear the Px_INTSRC[n] bit. |
| GPIO(PA~PD) Wake-up pin | rising or falling edge event, 64-pin | - | V | - | After software writes 1 to clear GPxWK (CLK_PMUSTS[11:8]) when SPD mode is entered. |
| GPIO(PC.0) Wake-up pin | rising or falling edge event , 1-pin | - | - | V | After software writes 1 to clear PINWK (CLK_PMUSTS[1]) when DPD mode is entered. |
| TIMER | Timer Interrupt | V | - | - | After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]). |
| Wakeup timer | Wakeup by wake-up timer time-out | - | V | V | After software writes 1 to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered. |
| WDT | WDT Interrupt | V | - | - | After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect). |
| RTC | Alarm Interrupt | V | - | - | After software writes 1 to clear ALMIF (RTC_INTSTS[0]). |
| | Time Tick Interrupt | V | - | - | After software writes 1 to clear TICKIF (RTC_INTSTS[1]). |
| | Wakeup by RTC alarm | - | V | V | After software writes 1 to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered. |
| | Wakeup by RTC tick time | - | V | V | After software writes 1 to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered. |
| | Wakeup by tamper event | - | V | V | After software writes 1 to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered. |
| UART | nCTS wake-up | V | - | - | After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]). |
| | RX Data wake-up | V | - | - | After software writes 1 to clear DATWKF (UARTx_WKSTS[1]). |
| | Received FIFO Threshold Wake-up | V | - | - | After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]). |
| | RS-485 AAD Mode Wake-up | V | - | - | After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]). |
| | Received FIFO Threshold Time-out Wake-up | V | - | - | After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]). |
| USCI UART | CTS Toggle | V | - | - | After software writes 1 to clear WKF (UUART_WKSTS[0]). |
| | Data Toggle | V | - | - | After software writes 1 to clear WKF (UUART_WKSTS[0]). |
| USCI $I^2C$ | Data toggle | V | - | - | After software writes 1 to clear WKF (UI2C_WKSTS[0]). |
| | Address match | V | - | - | After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]). |
| USCI SPI | SS Toggle | V | - | - | After software writes 1 to clear WKF (USPI_WKSTS[0]). |

| | | | | | |
|---|---|---|---|---|---|
| $I^2C$ | Address match wake-up | V | - | - | After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]). |
| USBD | Remote Wake-up | V | - | - | After software writes 1 to clear BUSIF (USBD_INTSTS[0]). |
| ACMP | Comparator Power-Down Wake-Up Interrupt | V | - | - | After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]). |
| ACMP | ACMPO status change | - | V | - | After software writes 1 to clear ACMPWK (CLK_PMUSTS[14]) when SPD mode is entered. |

Table 6.2-6 Re-Entering Power-down Mode Condition

### 6.2.5 Power Modes Transition

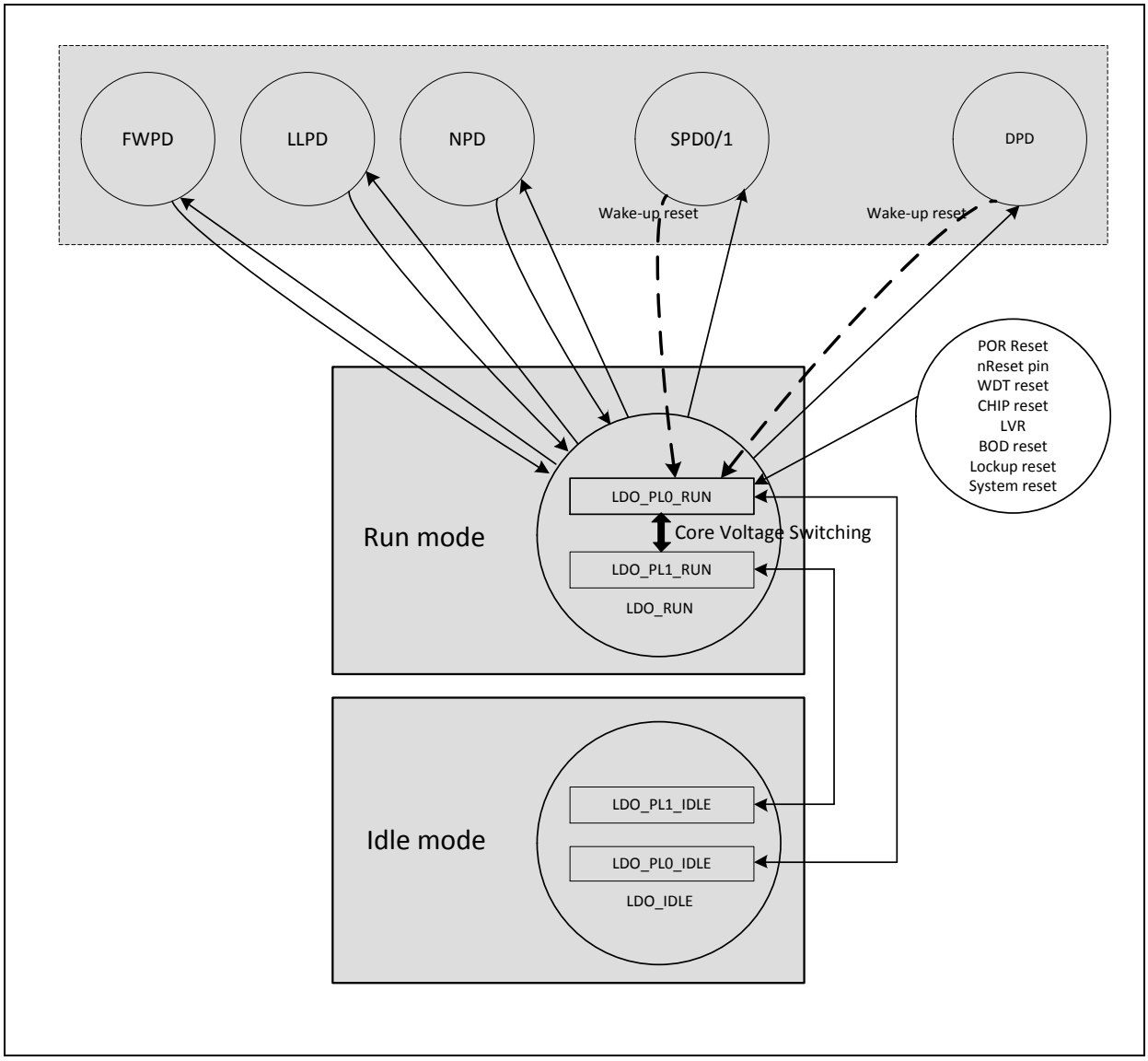



Figure 6.2-8 NuMicro® M480 Power Distribution Diagram

### 6.2.6 System Memory Map

The NuMicro® M480 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NuMicro® M480 series only supports little-endian data format.

| Address Space | Token | Controllers |
|---|---|---|
| **Flash and SRAM Memory Space** | | |
| 0x0000_0000 – 0x0003_FFFF | FLASH_BA | FLASH Memory Space (256KB) |
| 0x0000_0000 – 0x0007_FFFF | FLASH_BA | FLASH Memory Space (512KB) |
| 0x0800_0000 – 0x09FF_FFFF | SPIM_BA | SPIM Memory Space (32MB) |
| 0x2000_0000 – 0x2000_7FFF | SRAM0_BA | SRAM Memory Space (32KB) |
| 0x2000_8000 – 0x2001_FFFF | SRAM1_BA | SRAM Memory Space (96KB) |
| 0x2002_0000 – 0x2002_7FFF | SRAM2_BA | SRAM Memory Space (32KB) for CPU only and share with SPIM cache |
| 0x6000_0000 – 0x6FFF_FFFF | EXTMEM_BA | External Memory Space (256MB) |
| **Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)** | | |
| 0x4000_0000 – 0x4000_01FF | SYS_BA | System Control Registers |
| 0x4000_0200 – 0x4000_02FF | CLK_BA | Clock Control Registers |
| 0x4000_0300 – 0x4000_03FF | NMI_BA | NMI Control Registers |
| 0x4000_4000 – 0x4000_4FFF | GPIO_BA | GPIO Control Registers |
| 0x4000_7000 – 0x4000_7FFF | SPIM_BA | SPIM Control Registers |
| 0x4000_8000 – 0x4000_8FFF | PDMA_BA | Peripheral DMA Control Registers |
| 0x4000_9000 – 0x4000_9FFF | USBH_BA | USB Host Control Registers |
| 0x4000_B000 – 0x4000_BFFF | EMAC_BA | Ethernet MAC Control Registers |
| 0x4000_C000 – 0x4000_CFFF | FMC_BA | Flash Memory Control Registers |
| 0x4000_D000 – 0x4000_DFFF | SDH0_BA | SDHOST0 Control Registers |
| 0x4000_E000 – 0x4000_EFFF | SDH1_BA | SDHOST1 Control Registers |
| 0x4001_0000 – 0x4001_0FFF | EBI_BA | External Bus Interface Control Registers |
| 0x4001_9000 – 0x4001_9FFF | HSUSBD_BA | HSUSBD Control Registers |
| 0x4001_A000 – 0x4001_AFFF | HSUSBH _BA | HSUSBH Host Control Registers |
| 0x4003_1000 – 0x4003_1FFF | CRC_BA | CRC Generator Registers |
| 0x4003_E000 – 0x4003_EFFF | SWDC_BA | SWD Control Registers |
| 0x4003_F000 – 0x4003_FFFF | ETMC_BA | ETM Control Registers |
| 0x5008_0000 – 0x5008_0FFF | CRYP_BA | Cryptographic Accelerator Registers |
| **APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)** | | |
| 0x4004_0000 – 0x4004_0FFF | WDT_BA | Watchdog Timer Control Registers |
| 0x4004_1000 – 0x4004_1FFF | RTC_BA | Real Time Clock (RTC) Control Register |

| | | |
|---|---|---|
| 0x4004_3000 – 0x4004_3FFF | EADC_BA | Enhanced Analog-Digital-Converter (EADC) Control Registers |
| 0x4004_5000 – 0x4004_5FFF | ACMP01_BA | Analog Comparator 0/ 1 Control Registers |
| 0x4004_6000 – 0x4004_6FFF | OPA_BA | OP Amplifier Control Registers |
| 0x4004_7000 – 0x4004_7FFF | DAC_BA | DAC Control Registers |
| 0x4004_8000 – 0x4004_8FFF | I2S0_BA | $I^2S$0 Interface Control Registers |
| 0x4004_D000 – 0x4004_DFFF | OTG_BA | OTG Control Registers |
| 0x4004_F000 – 0x4004_FFFF | HSOTG_BA | HSOTG Control Registers |
| 0x4005_0000 – 0x4005_0FFF | TMR01_BA | Timer0/Timer1 Control Registers |
| 0x4005_1000 – 0x4005_1FFF | TMR23_BA | Timer2/Timer3 Control Registers |
| 0x4005_8000 – 0x4005_8FFF | EPWM0_BA | PWM0 Control Registers |
| 0x4005_9000 – 0x4005_9FFF | EPWM1_BA | PWM1 Control Registers |
| 0x4005_A000 – 0x4005_AFFF | BPWM0_BA | BPWM0 Control Registers |
| 0x4005_B000 – 0x4005_BFFF | BPWM1_BA | BPWM1 Control Registers |
| 0x4006_0000 – 0x4006_0FFF | QSPI0_BA | Quad SPI0 Control Registers |
| 0x4006_1000 – 0x4006_1FFF | SPI0_BA | SPI0 Control Registers |
| 0x4006_2000 – 0x4006_2FFF | SPI1_BA | SPI1 Control Registers |
| 0x4006_3000 – 0x4006_3FFF | SPI2_BA | SPI2 Control Registers |
| 0x4006_4000 – 0x4006_4FFF | SPI3_BA | SPI3 Control Registers |
| 0x4007_0000 – 0x4007_0FFF | UART0_BA | UART0 Control Registers |
| 0x4007_1000 – 0x4007_1FFF | UART1_BA | UART1 Control Registers |
| 0x4007_2000 – 0x4007_2FFF | UART2_BA | UART2 Control Registers |
| 0x4007_3000 – 0x4007_3FFF | UART3_BA | UART3 Control Registers |
| 0x4007_4000 – 0x4007_4FFF | UART4_BA | UART4 Control Registers |
| 0x4007_5000 – 0x4007_5FFF | UART5_BA | UART5 Control Registers |
| 0x4008_0000 – 0x4008_0FFF | I2C0_BA | $I^2C$0 Control Registers |
| 0x4008_1000 – 0x4008_1FFF | I2C1_BA | $I^2C$1 Control Registers |
| 0x4008_2000 – 0x4008_2FFF | I2C2_BA | $I^2C$2 Control Registers |
| 0x4009_0000 – 0x4009_0FFF | SC0_BA | Smartcard Host 0 Control Registers |
| 0x4009_1000 – 0x4009_1FFF | SC1_BA | Smartcard Host 1 Control Registers |
| 0x4009_2000 – 0x4009_2FFF | SC2_BA | Smartcard Host 2 Control Registers |
| 0x4009_3000 – 0x4009_3FFF | SC3_BA | Smartcard Host 3 Control Registers |
| 0x400A_0000 – 0x400A_0FFF | CAN0_BA | CAN0 Bus Control Registers |
| 0x400A_1000 – 0x400A_1FFF | CAN1_BA | CAN1 Bus Control Registers |
| 0x400B_0000 – 0x400B_0FFF | QEI0_BA | QEI0 Control Registers |
| 0x400B_1000 – 0x400B_1FFF | QEI1_BA | QEI1 Control Registers |

| | | |
|---|---|---|
| 0x400B_4000 – 0x400B_4FFF | ECAP0_BA | ECAP0 Control Registers |
| 0x400B_5000 – 0x400B_5FFF | ECAP1_BA | ECAP1 Control Registers |
| 0x400C_0000 – 0x400C_0FFF | USBD_BA | USB Device Control Register |
| 0x400D_0000 – 0x400D_0FFF | USCI0_BA | USCI0 Control Registers |
| 0x400D_1000 – 0x400D_1FFF | USCI1_BA | USCI1 Control Registers |
| **System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)** | | |
| 0xE000_E010 – 0xE000_E0FF | SCS_BA | System Timer Control Registers |
| 0xE000_E100 – 0xE000_ECFF | SCS_BA | External Interrupt Controller Control Registers |
| 0xE000_ED00 – 0xE000_ED8F | SCS_BA | System Control Registers |

Table 6.2-7 Address Space Assignments for On-Chip Controllers

### 6.2.7 SRAM Memory Orginization

The M480 series supports embedded SRAM with total 160 Kbytes and the SRAM organization is separated to two banks: SRAM bank0 and SRAM bank1 and SRAM bank2. The first bank has 32 Kbytes address space, the second bank has 96 Kbyte address space and the third bank has 32Kbyte. These three banks address space can be accessed simultaneously. The SRAM bank0 supports parity error check to make sure chip operating more stable. The SRAM bank2 is shared with SPIM cache, it can switch to external SPI Flash cache memory.

- Supports total 160 Kbytes SRAM
- Supports byte / half word / word write
- Supports fixed 32 Kbytes SRAM bank0 for independent access
- Supports parity error check function for SRAM bank0
- Supports oversize response error
- Supports remap address to 0x1000_0000

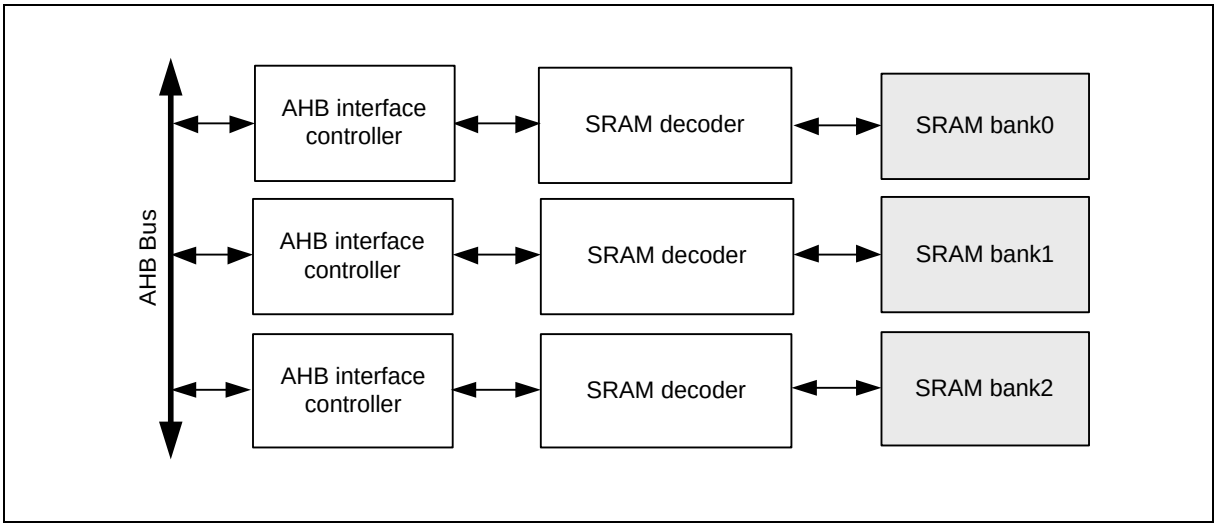



Figure 6.2-9 SRAM Block Diagram

Figure 6.2-9 shows the SRAM organization of M480. There are three SRAM banks in M480. The

bank0 is addressed to 32 Kbytes, the bank1 is addressed to 96 Kbytes and the bank2 is addressed to 32 Kbyte. The bank0 address space is from 0x2000_0000 to 0x2000_7FFF. The bank1 address space is from 0x2000_8000 to 0x2001_FFFF. The bank2 address space is from 0x2002_0000 to 0x2002_7FFF. The address between 0x2002_8000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

The address of each bank is remapping from 0x2000_0000 to 0x1000_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2000_7FFF or 0x1000_0000 to 0x1000_7FFF, and access SRAM bank1 through 0x2000_8000 to 0x2001_FFFF or 0x1000_8000 to 0x1001_FFFF, and access SRAM bank2 through 0x2002_0000 to 0x2002_7FFF or 0x1002_0000 to 0x1002_7FFF.

When setting the control register CCMEN(SPIM_CTL1[2]) to 0, SRAM bank2 is switched to external SPI Flash cache memory. In this case, the SRAM bank2 can't be accessed as gernal SRAM. If user access SRAM bank2 by AHB bus master, the SPI Flash controller will send error response via HRESP AHB bus signal to bus master.

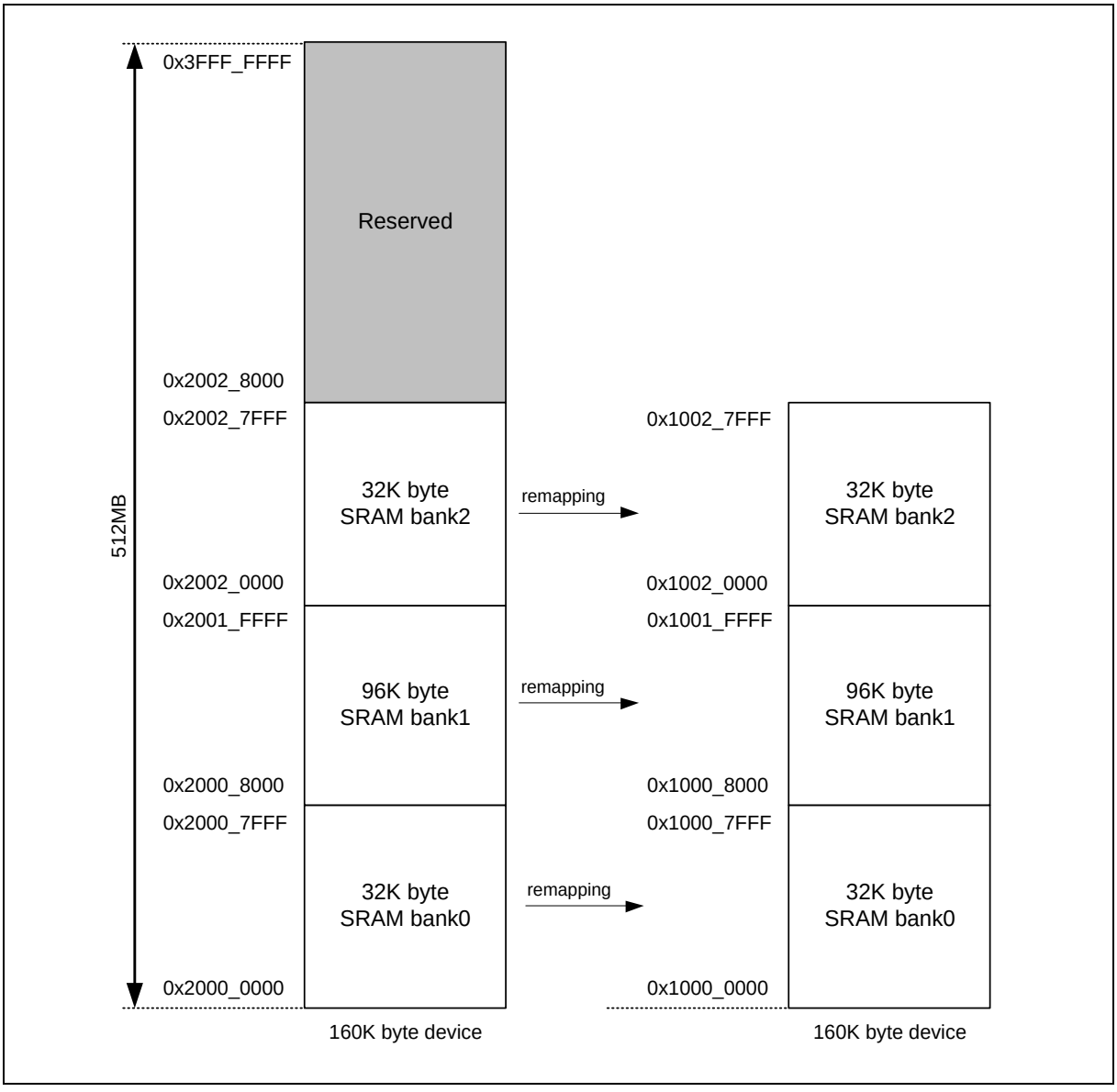



Figure 6.2-10 SRAM Memory Organization

SRAM bank0 has byte parity error check function. When CPU is accessing SRAM bank0, the parity

error checking mechanism is dynamic operating. As parity error occured, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occured, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

### 6.2.8 Bus Matrix

The M480 series supports Bus Matrix to manage the access arbitration between masters. The access arbitration can be selected by INTACTEN (SYS_AHBMCTL[0]) to use round-robin algorithm or set Cortex®-M4 CPU as the highest bus priority.

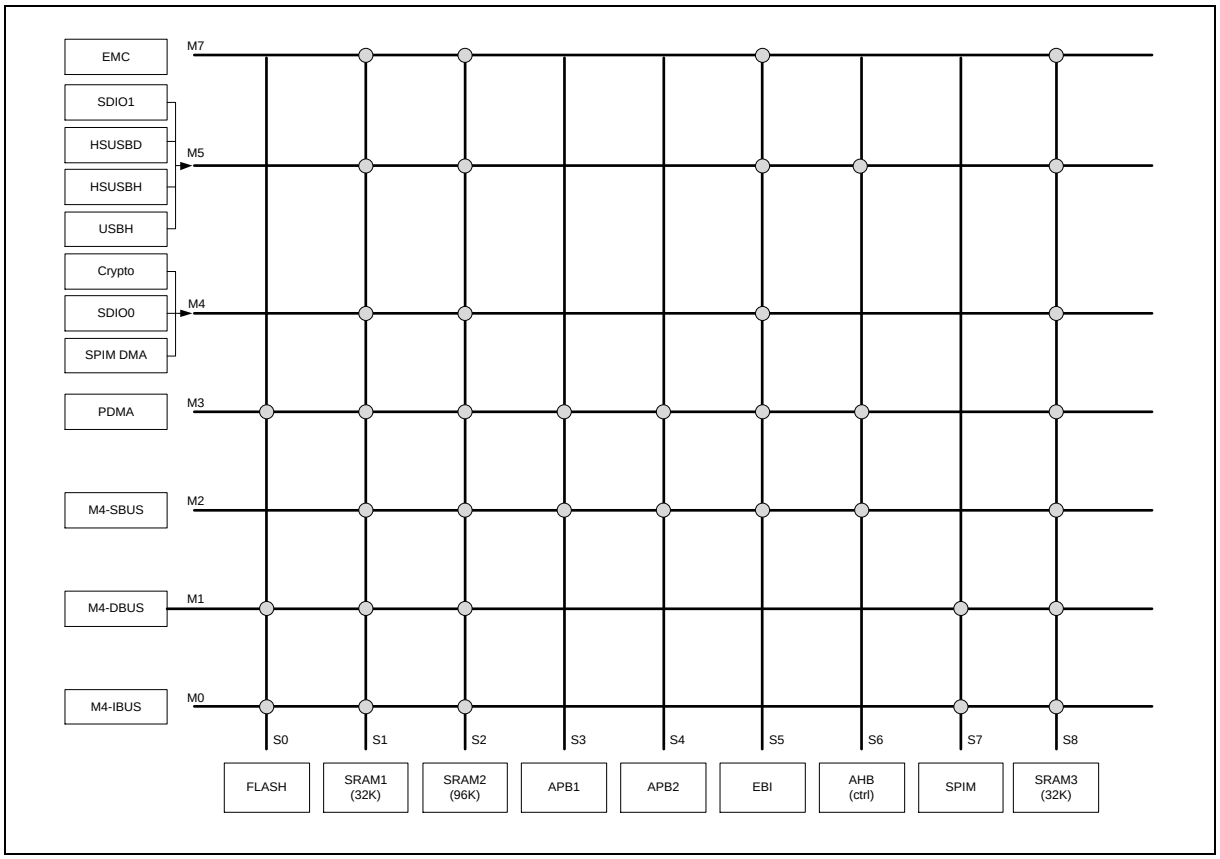



Figure 6.2-11 NuMicro® M480 Bus Matrix Diagram

### 6.2.9 HIRC Auto Trim

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator) or USB SOF (Start-Of-Frame), automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 12 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

### 6.2.10 System Timer (SysTick)

The Cortex®-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "ARM® Cortex®-M4 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

### 6.2.11 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-16 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

## 6.3 Clock Controller

### 6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M4 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 12 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

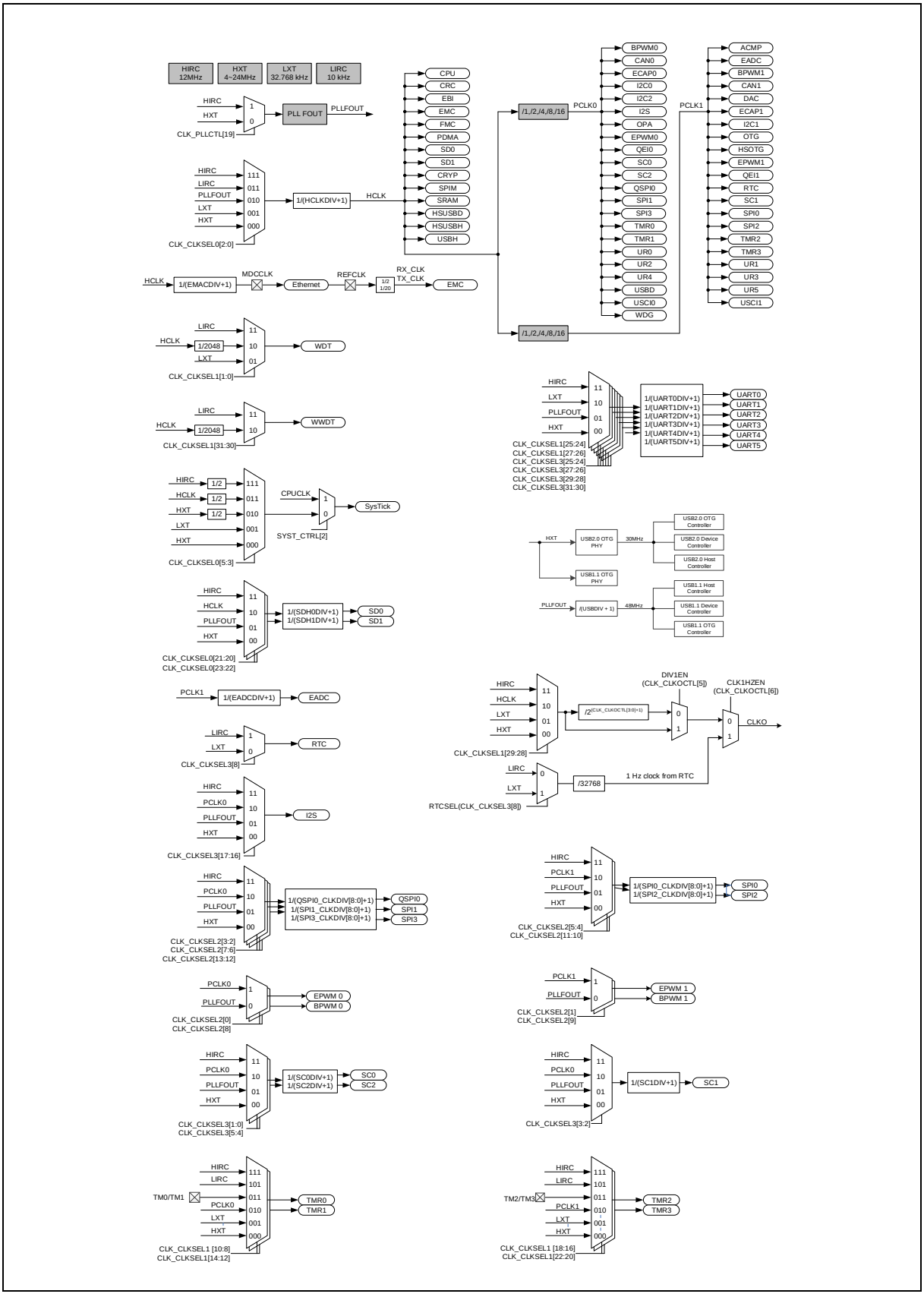



Figure 6.3-1 Clock Generator Global View Diagram

### 6.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)
- 12 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

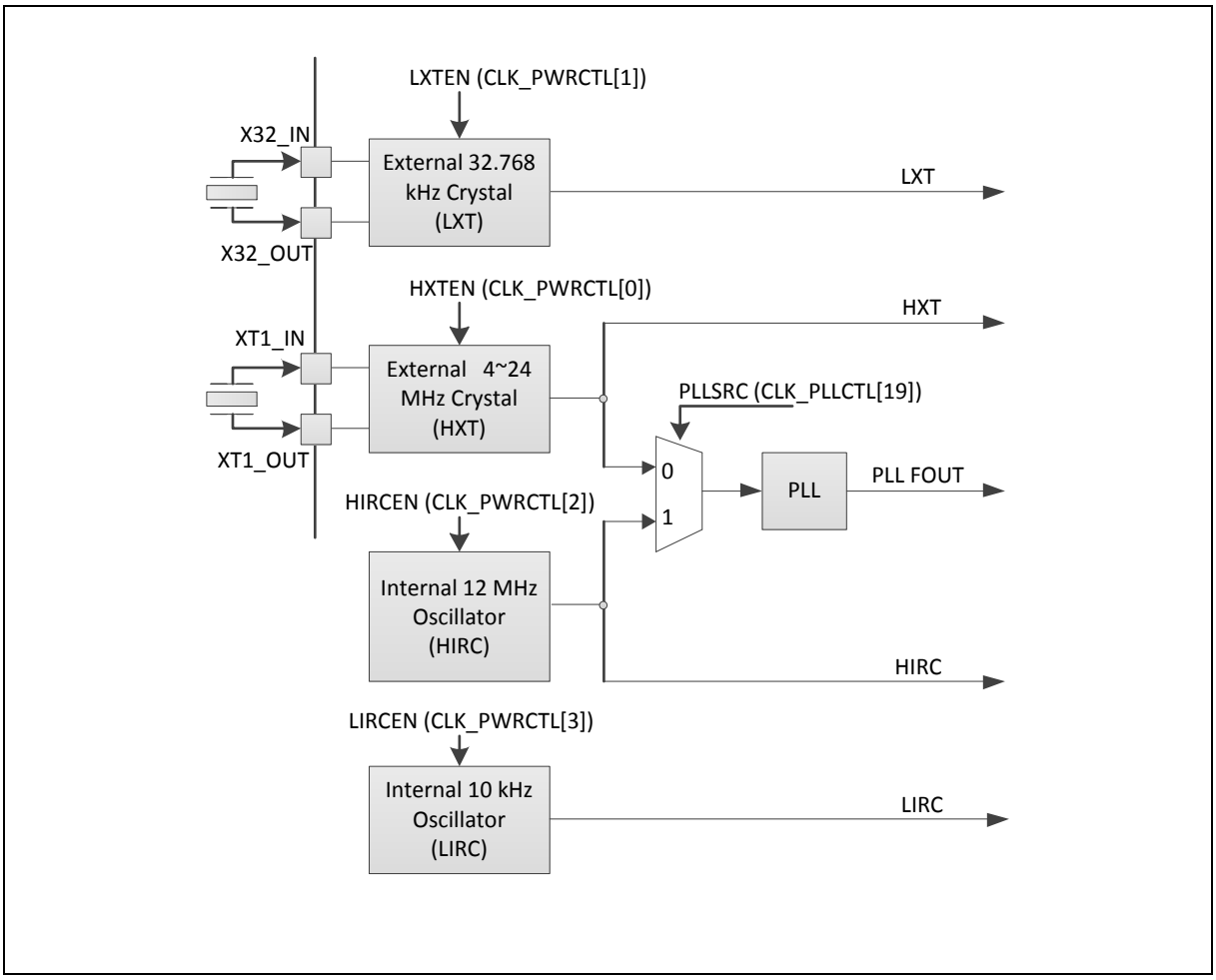



Figure 6.3-2 Clock Generator Block Diagram

### 6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.

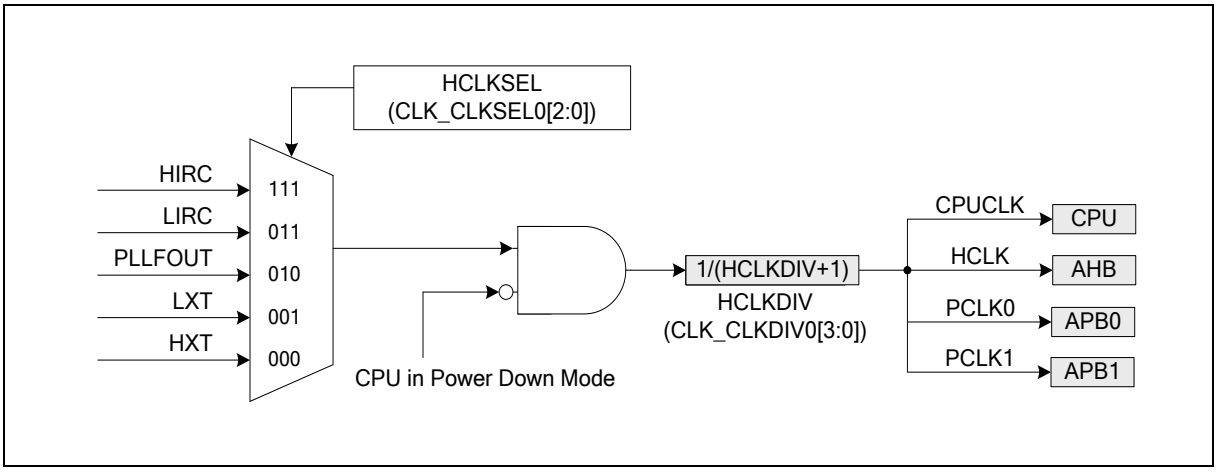



Figure 6.3-3 System Clock Block Diagrams

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 6.3-4 shows the HXT clock stops detection and system clock switches to HIRC procedure.

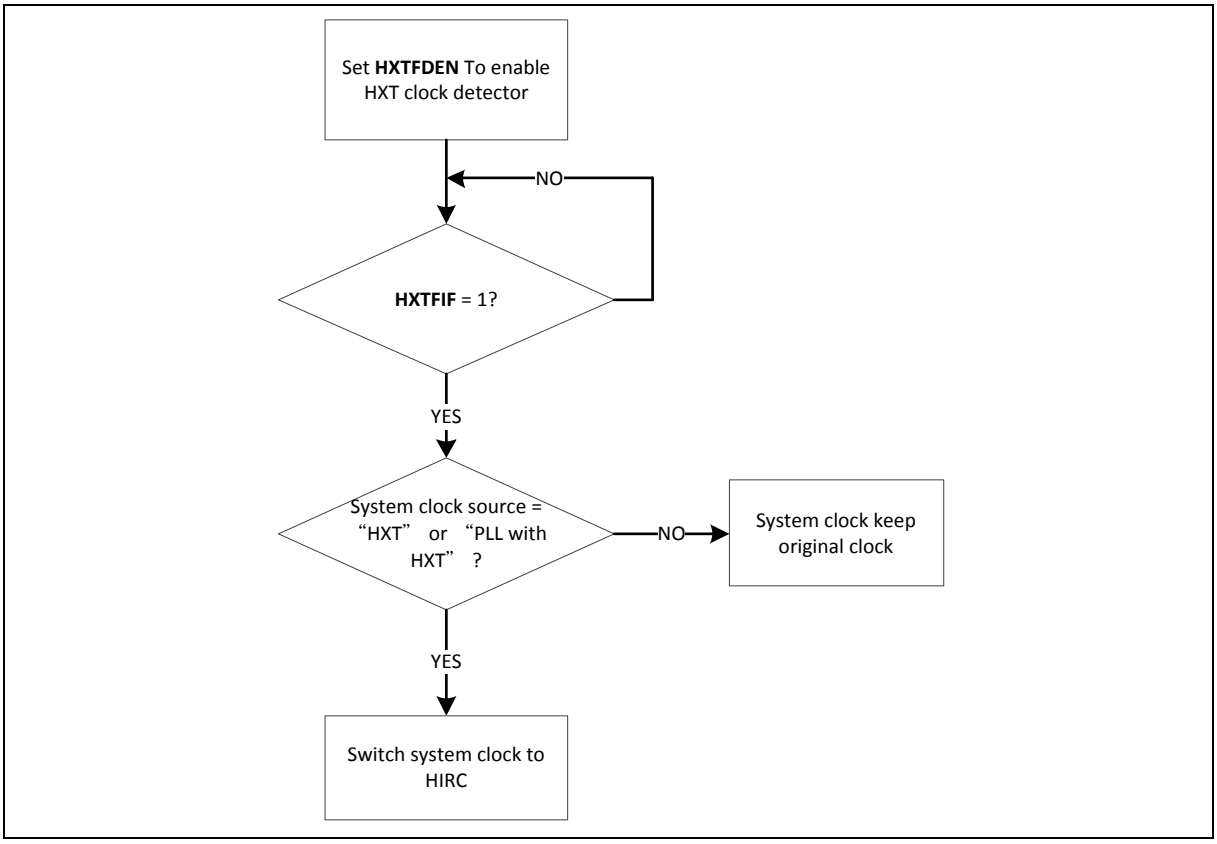



Figure 6.3-4 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M4 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

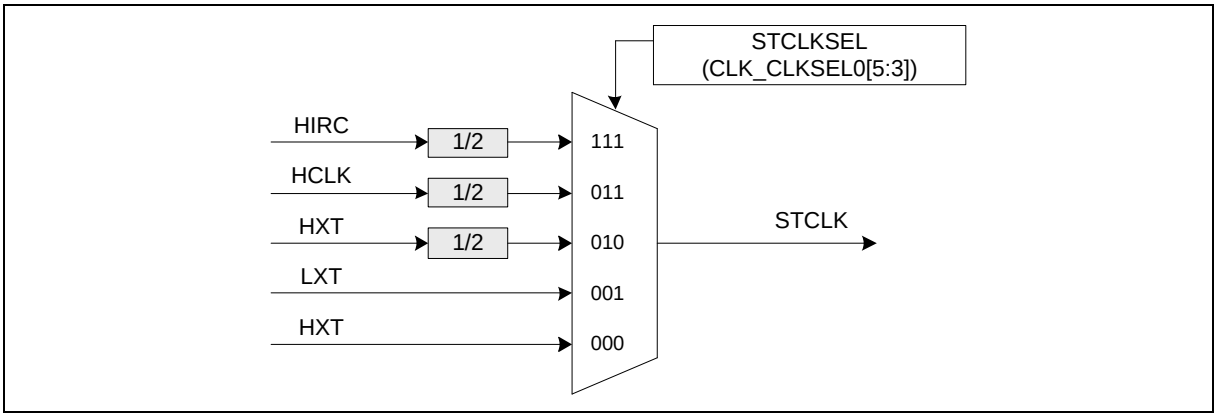



Figure 6.3-5 SysTick Clock Control Block Diagram

### 6.3.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register.

### 6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

### 6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where $F_{in}$ is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where $F_{in}$ is the input clock frequency, $F_{out}$ is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

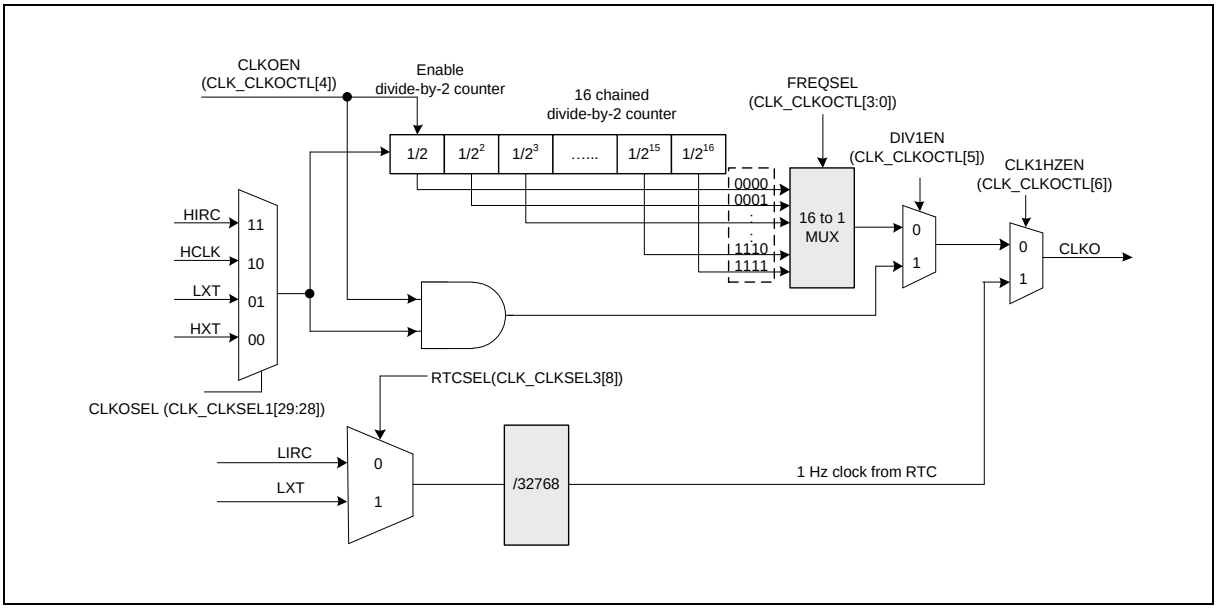



Figure 6.3-6 Clock Output Block Diagram

### 6.3.7 USB Clock Source

The clock sources of USB 1.0 and 2.0 systems are generated from USB2.0 PHY clock or programmable PLL output. The generated clocks are shown in Figure 6.3-7.

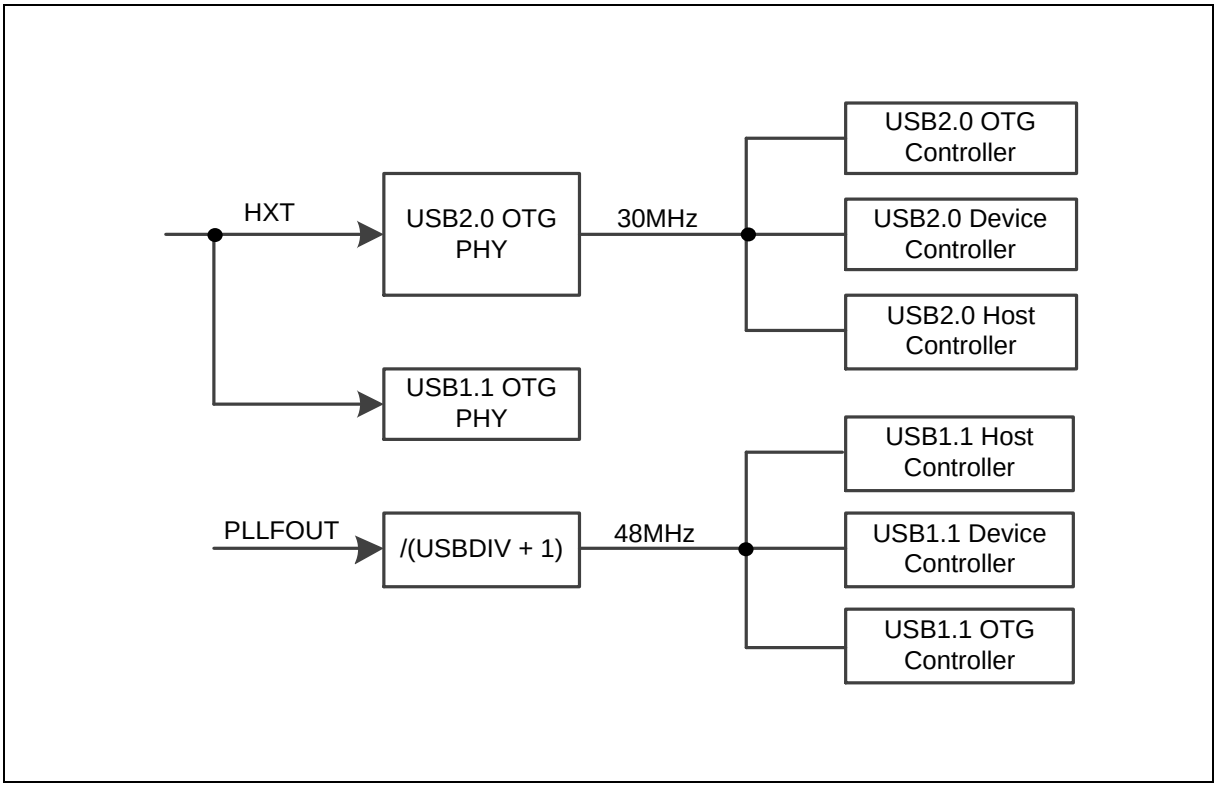



Figure 6.3-7 USB Clock Source

## 6.4 Flash Memeory Controller (FMC)

### 6.4.1 Overview

The FMC is equipped with dual-bank on-chip embedded Flash (BANK0 and BANK1) for application and configurable Data Flash to store some application dependent data. Both BANK0 and BANK1 have 64/128/256 Kbytes space. Thus, the total size of application rom (APROM) is 128K/256K/512K. A User Configuration block provides for system initiation in BANK0. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function in BANK0. A 4 Kbytes security protection ROM (SPROM) can conceal user program. A 2 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data in BANK1. A 32K Boot Loader consists of native ISP functions. A 4KB cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

### 6.4.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports 128/256/512 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports 4 Kbytes security protection ROM (SPROM) to conceal user program
- Supports Data Flash with configurable memory size
- Supports 16 bytes User Configuration block to control system initiation
- Supports 2 Kbytes one-time-program ROM (OTP)
- Supports 4 Kbytes page erase for all embedded Flash
- Supports Boot Loader with native In-System-Programming (ISP) functions
- Supports Security Key protection function for APROM, LDROM, SPROM, User Configuration block and KPROM protection
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption
- Supports auto-tuning Flash access cycle function to optimize the Flash access performance

## 6.5 General Purpose I/O (GPIO)

### 6.5.1 Overview

This chip has up to 118 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 118 pins are arranged in 8 ports named as PA, PB, PC, PD, PE, PF, PG and PH. PA, PB, PE and PG has 16 pins on port. PC, PD has 15 pins on port. PF, PH has 12 pins on port. Each of the 118 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]).

### 6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function

## 6.6 PDMA Controller (PDMA)

### 6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 16 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

### 6.6.2 Features

- Supports 16 independently configurable channels
- Selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, DAC, ADC and PWM request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1
- Supports stride function from channel 0 to channel 5

## 6.7 Timer Controller (TMR)

### 6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

### 6.7.2 Features

#### *6.7.2.1 Timer Function Features*

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, EADC, DAC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode
- Supports event counting source from internal USB SOF signal

#### *6.7.2.2 PWM Function Features*

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed,

Brown-out detection, SRAM parity error and CPU lockup)
- Brake pin noise filter control for brake source
- Edge detect brake source to control brake state until brake status cleared
- Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events

## 6.8 Watchdog Timer (WDT)

### 6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

### 6.8.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (24 ~ 218) and the time-out interval is 1.6 ms ~ 26.214 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 kHz or LXT.

## 6.9 Window Watchdog Timer (WWDT)

### 6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

### 6.9.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

## 6.10 Real Time Clock (RTC)

### 6.10.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

### 6.10.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.
- Supports up 3 pairs dynamic loop tamper pin or 6 individual tamper pin.
- Supports 80 bytes spare registers and tamper pins detection to clear the content of these spare registers.

## 6.11 EPWM Generator and Capture Timer (EPWM)

### 6.11.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC/DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

### 6.11.2 Features

*6.11.2.1 EPWM Function Features*

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter

**Up, down and up/down counter operation type**

- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter match free trigger comparator compared value (only for EADC)

#### *6.11.2.2 Capture Function Features*

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

## 6.12 Basic PWM Generator and Capture Timer (BPWM)

### 6.12.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

### 6.12.2 Features

*6.12.2.1 BPWM Function Features*

- Supports maximum clock frequency up to maximum PLL frequency.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC in the following events:
  - BPWM counter matches 0, period value or compared value

*6.12.2.2 Capture Function Features*

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

## 6.13 Quadrature Encoder Interface (QEI)

### 6.13.1 Overview

There are two QEI controllers in this device. The Quadrature Encoder Interface (QEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

### 6.13.2 Features

*6.13.2.1 Quadrature Encoder Interface (QEI) Features*

- Up to two QEI controllers, QEI0 and QEI1.
- Two QEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (QEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (QEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (QEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (QEI_CNTCMP) with a Pre-set Maximum Count Register (QEI_CNTMAX)
- One QEI control register (QEI_CTL) and one QEI Status Register (QEI_STATUS)
- Four Quadrature encoder pulse counter operation modes
  - Support x4 free-counting mode
  - Support x2 free-counting mode
  - Support x4 compare-counting mode
  - Support x2 compare-counting mode
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clk/8

## 6.14 Enhanced Input Capture Timer (ECAP)

### 6.14.1 Overview

This device provides up to two units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

### 6.14.2 Features

- Up to two Input Capture Timer/Counter units, CAP0 and CAP1.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

## 6.15 UART Interface Controller (UART)

### 6.15.1 Overview

The chip provides six channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN and RS-485 function modes and auto-baud rate measuring function.

### 6.15.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0 /UART1 with LIN function)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function

| UART Feature | UART0/ UART1 | UART2/ UART3/ UART4/ UART5 | SC_UART | USCI-UART |
|---|---|---|---|---|
| FIFO | 16 Bytes | 16 Bytes | 4 Bytes | TX: 1byte<br>RX: 2byte |
| Auto Flow Control (CTS/RTS) | √ | √ | - | √ |
| IrDA | √ | √ | - | - |
| LIN | √ | - | - | - |
| RS-485 Function Mode | √ | √ | - | √ |
| nCTS Wake-up | √ | √ | - | √ |
| Imcoming Data Wake-up | √ | √ | - | √ |
| Received Data FIFO reached threshold Wake-up | √ | √ | - | - |
| RS-485 Address Match (AAD mode) Wake-up | √ | √ | - | - |
| Auto-Baud Rate Measurement | √ | √ | - | √ |
| STOP Bit Length | 1, 1.5, 2 bit | 1, 1.5, 2 bit | 1, 2 bit | 1, 2 bit |
| Word Length | 5, 6, 7, 8 bits | 5, 6, 7, 8 bits | 5, 6, 7, 8 bits | 6~13 bits |
| Even / Odd Parity | √ | √ | √ | √ |
| Stick Bit | √ | √ | - | - |
| **Note:** √= Supported | | | | |

Table 6.15-1 NuMicro® M480 Series UART Features

## 6.16 Ethernet MAC Controller (EMAC)

### 6.16.1 Overview

This chip provides an Ethernet MAC Controller (EMAC) for Network application. The Ethernet MAC controller consists of IEEE 802.3/Ethernet protocol engine with internal CAM function for recognizing Ethernet MAC addresses, Transmit-FIFO, Receive-FIFO, TX/RX state machine controller, time stamping engine for IEEE 1588, Magic Packet parsing engine and status controller. The EMAC supports both the MII and RMII (Reduced MII) interface to connect with external Ethernet PHY.

### 6.16.2 Features

- Supports IEEE Std. 802.3 CSMA/CD protocol
- Supports Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol
- Supports both half and full duplex for 10 Mbps or 100 Mbps operation
- Supports both MII and RMII interface
- Supports MII Management function to control external Ethernet PHY
- Supports pause and remote pause function for flow control
- Supports long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception
- Supports 16 entries CAM function for Ethernet MAC address recognition
- Supports Magic Packet recognition to wake system up from Power-down mode
- Supports 256 bytes transmit FIFO and 256 bytes receive FIFO
- Supports DMA function

## 6.17 Smart Card Host Interface (SC)

### 6.17.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

### 6.17.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Three ISO 7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

## 6.18 I²S Controller (I²S)

### 6.18.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

### 6.18.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

## 6.19 Serial Peripheral Interface (SPI)

### 6.19.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The M480 series contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports $I^2S$ mode to connect external audio CODEC.

### 6.19.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 100 MHz and Slave mode up to 100 MHz (when chip works at $V_{DD}$ = 2.7~3.6V)
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- $I^2S$ Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, $I^2S$ and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

| | QSPIx | SPIx |
|---|---|---|
| Dual/Quad I/O Mode | V | X |
| Two-bit Transfer Mode | V | X |
| FIFO Depth | 8-level | SPI mode 8~16 bits data length: 8-level<br>Otherwise: 4-level |
| Slave Time-out Function | V | X |
| Slave 3-Wired Mode | V | X |

| | | |
|---|---|---|
| I²S Mode | X | V |

## 6.20 Quad Serial Peripheral Interface (QSPI)

### 6.20.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The M480 series contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

### 6.20.2 Features

- Supports Master or Slave mode operation
- Master mode up to 100 MHz and Slave mode up to 100 MHz (when chip works at $V_{DD}$ = 2.7~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports receive-only mode

## 6.21 SPI Synchronous Serial Interface Controller (SPI Master mode)

### 6.21.1 Overview

The SPI Synchronous serial Interface Controller for SPI master mode performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data received from MCU. This SPI controller can drive one external peripheral (External SPI Flash) and it is seen as the SPI master mode. It can generate an interrupt signal when data transfer is finished and can be cleared by writing 1 to the interrupt flag. The active level of device/slave select signal can be chosen to low active or high active, which depends on the peripheral. Writing a divisor into the SPIM_CTL1 register can program the frequency of serial clock output to the peripheral.

In SPI Flash controller, normal I/O mode contains four 32-bit transmit/receive buffers, and can provide 1 to 4 burst mode operation. The number of bits in each transaction can be 8, 16, 24, or 32; data can be transmitted/received up to four successive transactions in one transfer.

By DMA write mode, user can move data from SRAM to external SPI Flash component. In DMA read mode, user can move data from external SPI Flash component to SRAM. In direct memory mapping mode (DMM mode), this SPI Flash controller will translate the AHB bus commands into SPI Flash operations without MCU setting related SPI Flash command. Therefore users can access external SPI Flash as a ROM module.

In direct memory mapping mode with cache off mode, it will pre-fetch 4-word Flash data after a direct memory mapping access. when using direct memory mapping mode with cache on mode, it will use 32 Kbytes cache memory to reduce the number of accessing external SPI Flash component and the performance of SPI Flash access can be improved. To improve the read operation of SPI Flash without increasing the serial clock frequency, this SPI Flash controller supports DTR/DDR (Double Transfer Rate/Double Data Rate) read command codes that support Standard/Dual/Quad SPI modes. The one byte command code is still latched into the device on the rising edge of the serial clock similar to all other SPI commands. Once a DTR/DDR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

In core coupled memory mode (CCM mode), the cache function is disabled by hardware automatically, and MCU can access this 32 Kbytes cache memory as general SRAM. For data protection, this SPI Flash controller supports cipher encryption and decryption circuits to protect data which user places into external SPI Flash when DMA read/write mode and direct memory mapping mode are used.

### 6.21.2 Features

- Supports maximum 32M bytes SPI Flash size
- Supports SPI master mode
- Supports Direct Memory Mapping Mode and Normal I/O Mode
- Supports 8/16/24/32 bits transaction for Normal I/O mode
- Provides burst mode operation in Normal I/O mode, which can transmit/receive data up to four successive transactions in one transfer
- Supports DMA mode read/write
- Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
- Supports Double Transfer Rate (DTR) / Double Data Rate (DDR) transfer mode
- Supports 32 Kbytes cache memory
- Supports 32 Kbytes Core Coupled Memory (CCM) when cache function disable
- Supports Cipher encryption/decryption
- One slave/device select line for external SPI Flash component

## 6.22 I²C Serial Interface Controller (I²C)

### 6.22.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers which support Power-down wake-up function.

### 6.22.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to three I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition ( four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

## 6.23 USCI - Universal Serial Control Interface Controller (USCI)

### 6.23.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or $I^2C$ functional protocol.

### 6.23.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- $I^2C$

## 6.24 USCI – UART Mode

### 6.24.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system.

### 6.24.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wakeup Only)

## 6.25 USCI - SPI Mode

### 6.25.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USCI_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USCI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

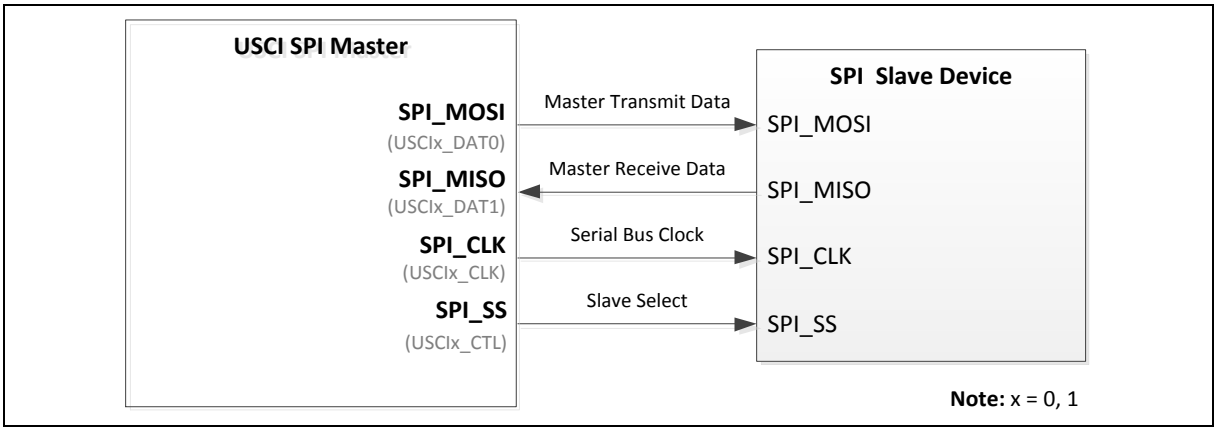



Figure 6.25-1 SPI Master Mode Application Block Diagram

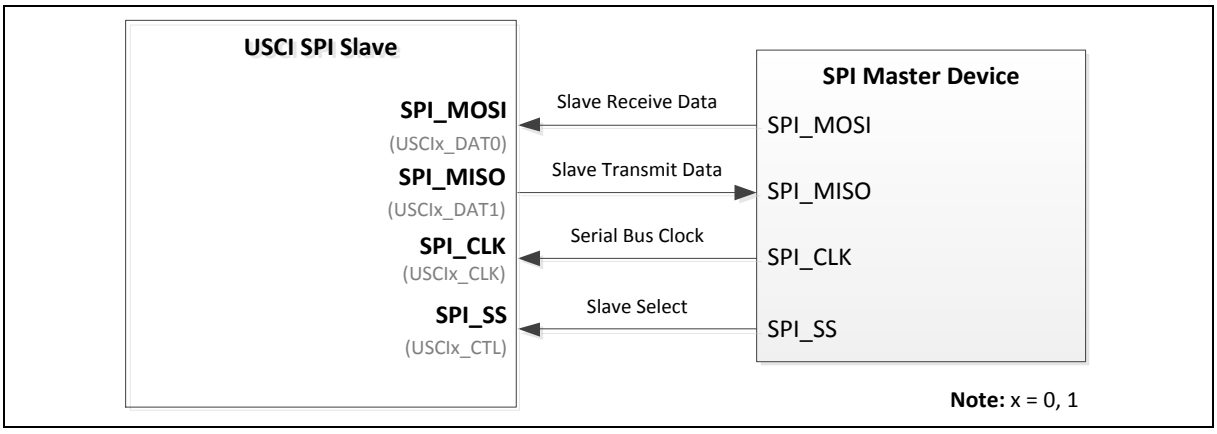



Figure 6.25-2 SPI Slave Mode Application Block Diagram

### 6.25.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = fPCLK / 2, Slave < fPCLK / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence

- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

## 6.26 USCI - I²C Mode

### 6.26.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.26-1 for more detailed I²C BUS Timing.

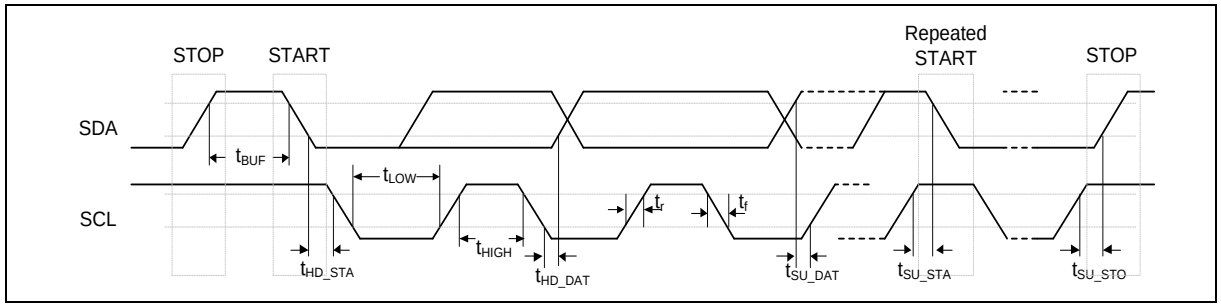



Figure 6.26-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (USCI_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I2C in advance.

**Note:** Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode .

### 6.26.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

## 6.27 Controller Area Network (CAN)

### 6.27.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

### 6.27.2 Features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

## 6.28 Secure Digital Host Controller (SDH)

### 6.28.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SDHOST controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

### 6.28.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function.
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.

## 6.29 External Bus Interface (EBI)

### 6.29.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

### 6.29.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports Address/Data multiplexed Mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)
- Supports address bus and data bus separate mode

## 6.30 USB 1.1 Device Controller (USBD)

### 6.30.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1KBytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

### 6.30.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbyte buffer size
- Provides remote wake-up capability

## 6.31 High Speed USB 2.0 Device Controller (HSUSBD)

### 6.31.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

### 6.31.2 Features

- USB Specification reversion 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint – Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- 4092 Bytes Configurable RAM used as endpoint buffer
- Supports Endpoint Maximum Packet Size up to 1024 bytes

## 6.32 USB 2.0 Host Controller (USBH)

### 6.32.1 Overview

This chip is equipped with a USB 2.0 HS/FS Host Controller (USBH) that supports Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

### 6.32.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Enhanced Host Controller Interface (EHCI) Specification Revision 1.0
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports a port routing logic to route full/low speed device to OHCI controller.
- Supports two USB host port shared with USB device (OTG function).
- Supports port power control and port over current detection.
- Supports DMA for real-time data transfer.

## 6.33 USB On-The-Go (OTG)

### 6.33.1 Overview

The OTG controller interfaces to USB PHY and USB controllers which consist of a USB 1.1 host controller and a USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the "On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 2.0 Specification".

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID-dependent or OTG Device mode defined in USBROLE (SYS_USBPHY[1:0]). In Host-only mode, USB frame acts as USB host. USB frame can support both full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame only supports full-speed transfer. In ID-dependent mode, USB frame can be USB Host or USB device depending on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame only supports full-speed transfer when OTG device acts as a peripheral.

### 6.33.2 Features

- Built-in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID-dependent: The role of USB frame is only dependent on USB_ID pin value--as USB Host (USB_ID pin is low) or USB Device (USB_ID pin is high). Not support HNP or SRP protocol.
  - OTG device: dependent on USB_ID pin status to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). Support HNP and SRP protocols.

## 6.34 High Speed USB On-The-Go (HSOTG)

### 6.34.1 Overview

The HSOTG controller interfaces to USB PHY and USB controllers which consist of a USB 2.0 host controller and a USB 2.0 HS device controller. The OTG controller supports HNP and SRP protocols defined in the "On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 1.3 Specification".

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID-dependent or OTG Device mode defined in HSUSBROLE (SYS_USBPHY[17:16]). In Host-only mode, USB frame acts as USB host. USB frame can support high-speed, full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame supports high-speed and full-speed transfer. In ID-dependent mode, USB frame can be USB Host or USB device depends on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame supports high-speed and full-speed transfer when OTG device acts as a peripheral.

### 6.34.2 Features

- Built in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID-dependent: The role of USB frame is only dependent on USB_ID pin value--as USB Host (USB_ID pin is low) or USB Device (USB_ID pin is high). Not support HNP or SRP protocol.
  - OTG device: dependent on USB_ID pin status to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). Support HNP and SRP protocols.

### 6.34.3 Basic Configuration

The OTG peripheral clock can be enabled by HSOTGCKEN (CLK_APBCLK0[30]). The role of USB frame is determined by HSUSBROLE (SYS_USBPHY[17:16]). These two configurations are write-protection bits. Before writing to these bits, user must disable the register protection function. Refer to the description of SYS_REGLCTL register for details. USB_VBUS_EN and USB_VBUS_ST pin functions are configured in SYS_GPA_MFPL or SYS_GPC_MFPL registers.

## 6.35 CRC Controller (CRC)

### 6.35.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

### 6.35.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

## 6.36 Cryptographic Accelerator (CRYPTO)

### 6.36.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, DES/TDES, SHA and HMAC algorithms.

The PRNG core supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode.

The DES/TDES accelerator is an implementation fully compliant with the DES and Triple DES encryption/decryption algorithm. The DES/TDES accelerator supports ECB, CBC, CFB, OFB, and CTR mode.

The SHA accelerator is an implementation fully compliant with the SHA-160, SHA-224, SHA-256, SHA-384, and SHA-512 and corresponding HMAC algorithms.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime filed.

### 6.36.2 Features

- PRNG
  - Supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode
  - Supports key expander
- DES
  - Supports FIPS 46-3
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- TDES
  - Supports FIPS NIST 800-67
  - Implemented according to the X9.52 standard
  - Supports two keys or three keys mode
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- SHA
  - Supports FIPS NIST 180, 180-2
  - Supports SHA-160, SHA-224, SHA-256, SHA-384, and SHA-512
- HMAC

- Supports FIPS NIST 180, 180-2
- Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512

- ECC
  - Supports both prime field GF(p) and binary filed GF($2^m$)
  - Supports NIST P-192, P-224, P-256, P-384, and P-521
  - Supports NIST B-163, B-233, B-283, B-409, and B-571
  - Supports NIST K-163, K-233, K-283, K-409, and K-571
  - Supports point multiplication, addition and doubling operations in GF(p) and GF($2^m$)
  - Supports modulus division, multiplication, addition and subtraction operations in GF(p)

## 6.37 Enhanced 12-bit Analog-to-Digital Converter (EADC)

### 6.37.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR ADC converter) with 16 external input channels and 3 internal channels. The ADC converter can be started by software trigger, EPWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

### 6.37.2 Features

- Analog input voltage range: 0~ VREF (Max to 3.6V)
- Reference voltage from VREF pin or $AV_{DD}$
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels
- Up to 3 internal channels, they are band-gap voltage (VBG), temperature sensor (VTEMP), and $V_{DD}$ power.
- Four ADC interrupts (ADINT0~3) with individual interrupt vector addresses
- Maximum ADC clock frequency is 72 MHz
- Up to 5.14 MSPS conversion rate
- Configurable ADC internal sampling time.
- 12-bit, 10-bit, 8-bit, 6-bit configurable resolution.
- Supports calibration and load calibration words capability.
- Supports internal reference voltage VREF: 1.6V, 2.0V, 2.5V, and 3.0V.
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode
  - Standby mode
- Up to 19 sample modules
  - Each of sample modules which is configurable for ADC converter channel EADC_CH0~15 and trigger source
  - Sample module 16~18 is fixed for ADC channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and $V_{DD}$ power.
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 19 data registers with valid and overrun indicators
- An ADC conversion can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~18)
  - External pin EADC0_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers

- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

## 6.38 Digital to Analog Converter (DAC)

### 6.38.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

### 6.38.2 Features

- Analog output voltage range: 0~$AV_{DD}$.
- Supports 12- or 8-bit output mode.
- Rail to rail settle time 8us.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), VREF pin or $AV_{DD}$.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

## 6.39 Analog Comparator Controller (ACMP)

### 6.39.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

### 6.39.2 Features

- Analog input voltage range: 0 ~ VDDA (voltage of $AV_{DD}$ pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
- Supports wake-up function
- Supports programmable propagaion speed and low power consumption
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 4 negative sources:
    - ACMP1_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode

## 6.40 OP Amplifier (OPA)

### 6.40.1 Overview

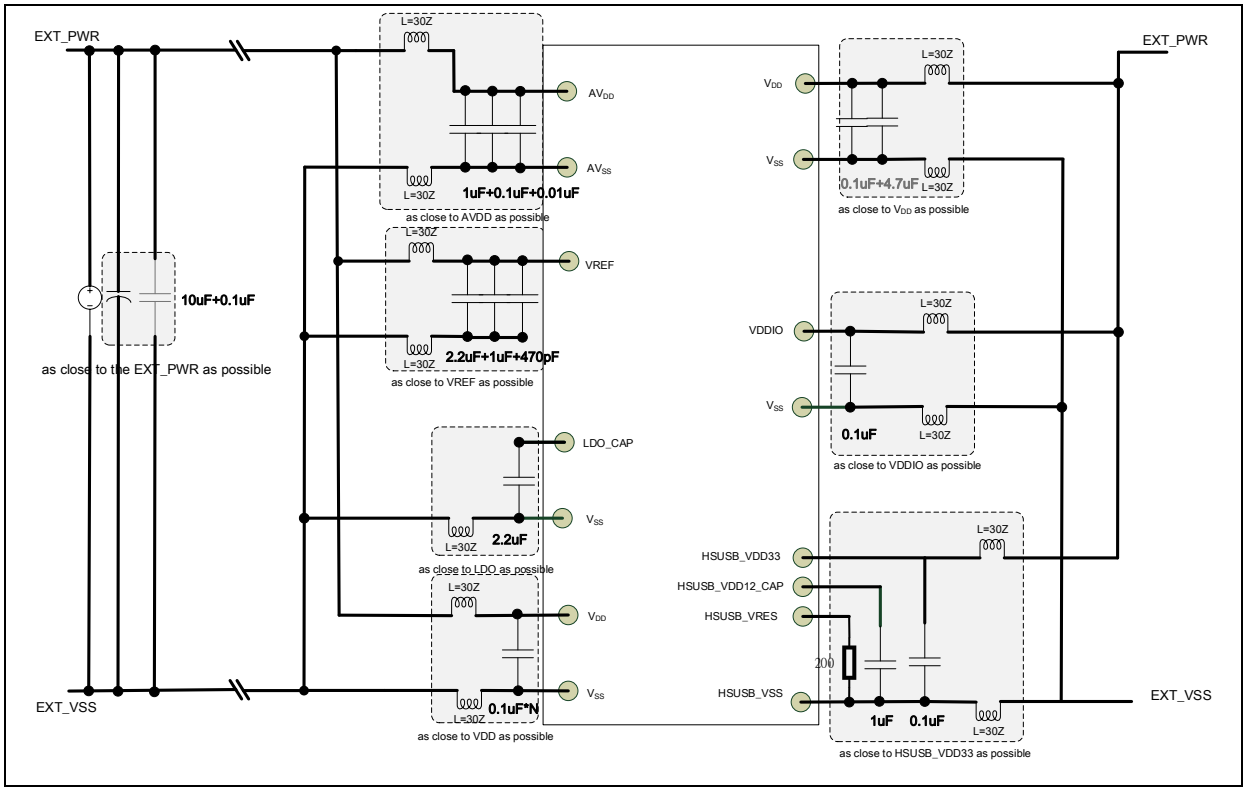
This device is equipped with three operational amplifiers. Users can enable each of them individually, by their application purpose.One of these OP amplifier outputs is connected to ADC channel for measurement requirement.The OP amplifier circuit also can be used in the application of Programmable Gain Amplifier (PGA).

### 6.40.2 Features

- Analog input voltage range: 0~VDD.
- Supports up to 3 operator amplifiers.
- Supports to use Schmitt trigger buffer output for simple comparator function.
- Supports to Schmitt trigger buffer output interrupts.

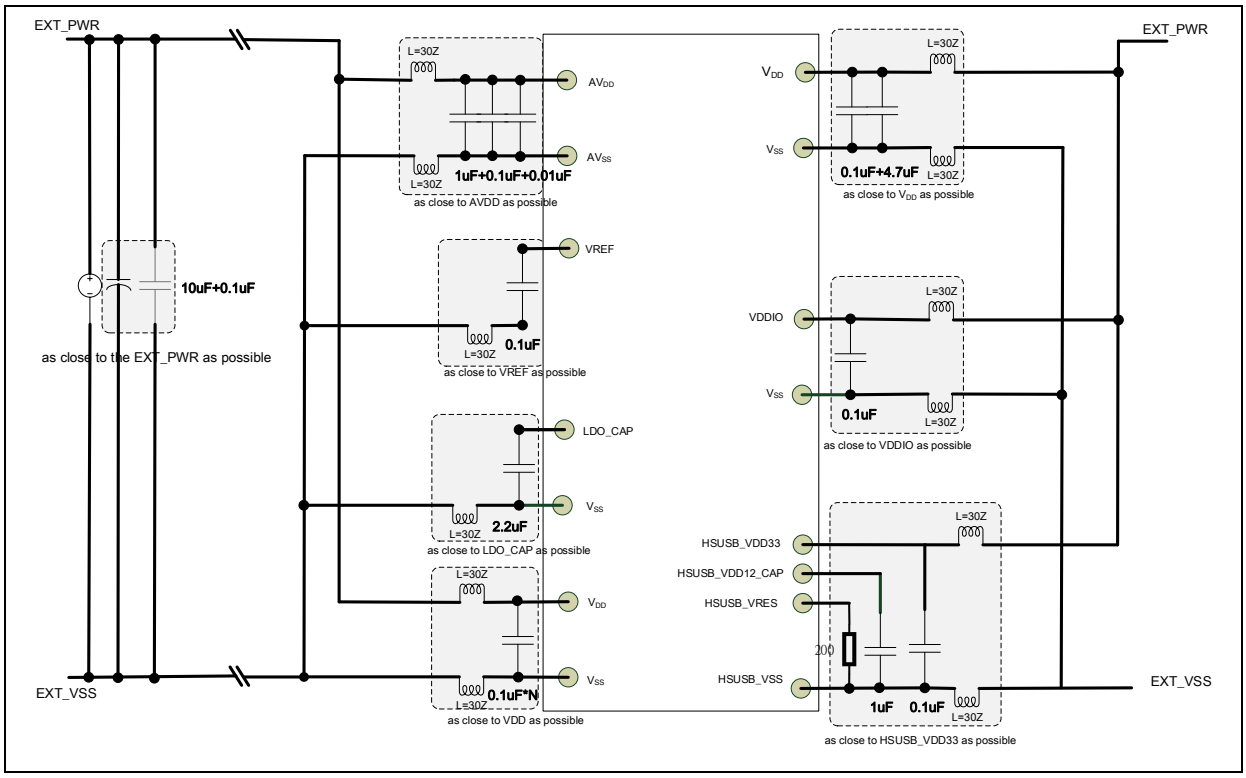
# 7 APPLICATION CIRCUIT

## 7.1 Power Supply Scheme with External Vref



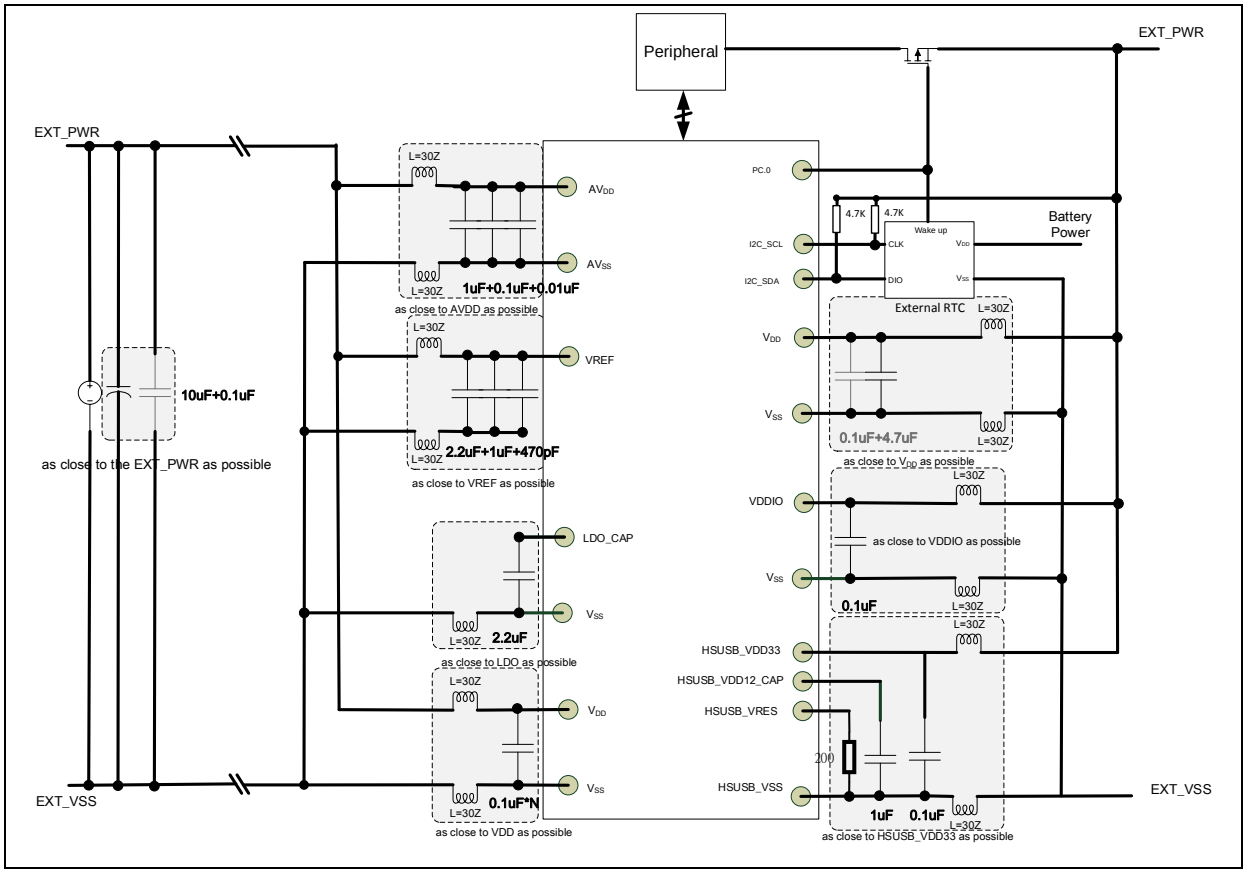

**Note:** Total capacitance of LDO_CAP pin is 2.2uF.

## 7.2 Power Supply Scheme with Internal Vref



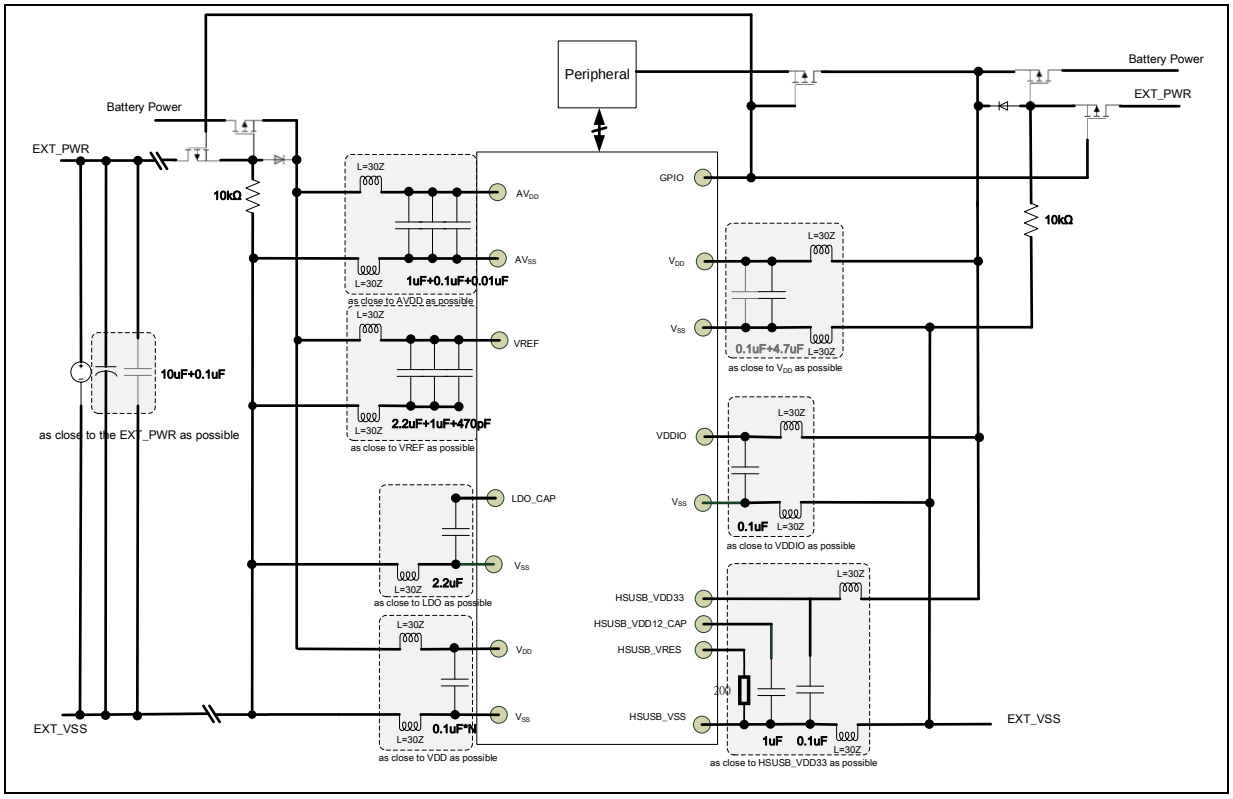

**Note**: Total capacitance of LDO_CAP pin is 2.2uF.

## 7.3 Power Supply Scheme with $V_{REF}$ and External RTC with Battery Power



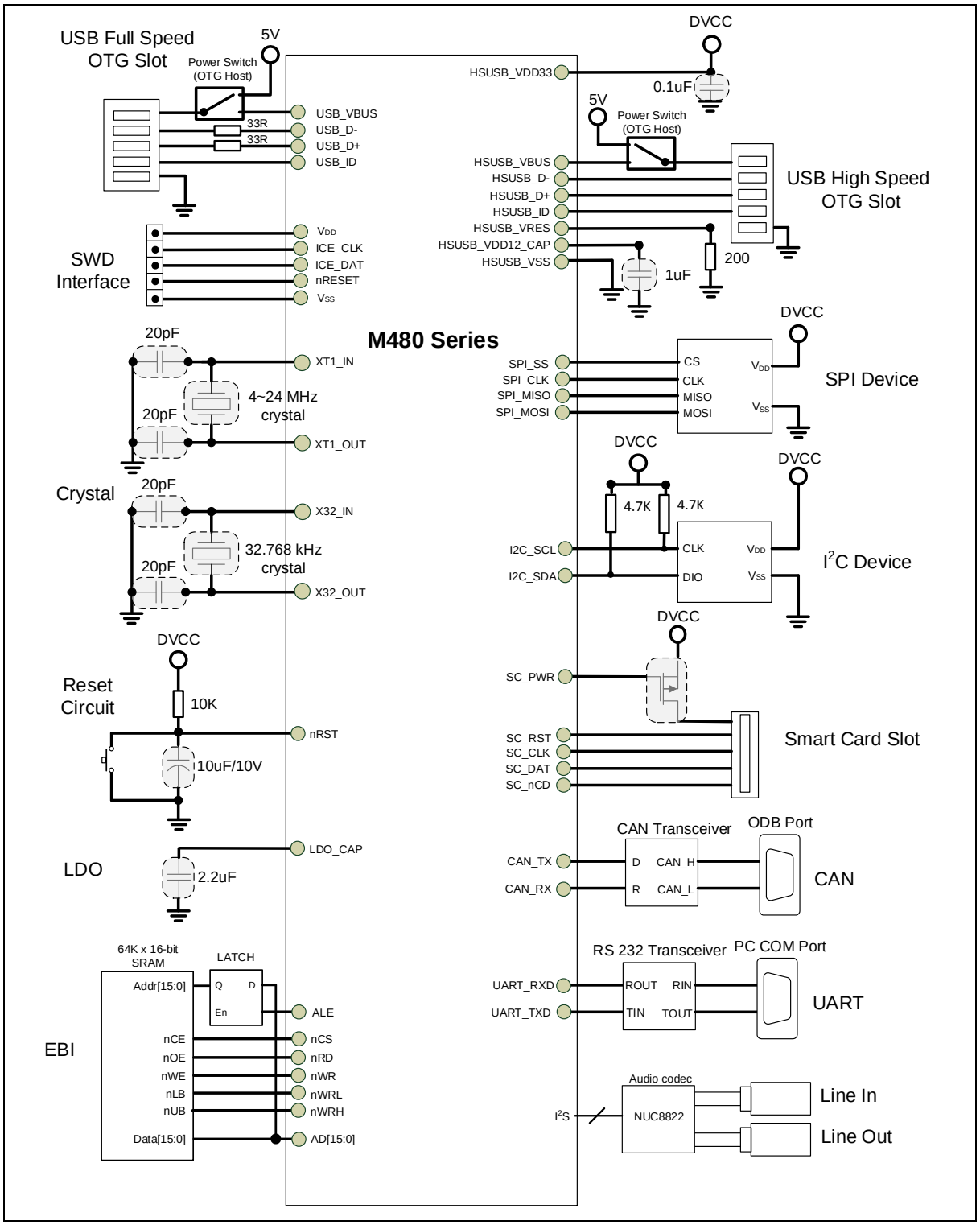

**Note**: Total capacitance of LDO_CAP pin is 2.2uF.

## 7.4 Power Supply Scheme with $V_{REF}$ and Internal RTC with Battery Power




**Note**: Total capacitance of LDO_CAP pin is 2.2uF.

## 7.5 Peripheral Application Scheme




**Note:**

1. USB_ID, HSUSB _ID could be floating using USB or USB HS without OTG.
2. Total capacitance of LDO_CAP pin is 2.2uF.

# 8 ELECTRICAL CHARACTERISTICS

## 8.1 Absolute Maximum Ratings

### 8.1.1 Voltage Characteristics

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$-$V_{SS}$[*1] | DC Power Supply | -0.3 | 4 | V |
| $V_{DDIO}$-$V_{SS}$ | $V_{DDIO}$ Power Supply | -0.3 | 4 | V |
| $\|V_{DDX} – V_{DD}\|$ | Variations between different power pins | | 50 | mV |
| $\|V_{DD} –AV_{DD}\|$ | Allowed voltage difference for $V_{DD}$ and $AV_{DD}$ | | 50 | mV |
| $\|V_{SSX} - V_{SS}\|$ | Variations between different ground pins | | 50 | mV |
| $\|V_{SS} - AV_{SS}\|$ | Allowed voltage difference for $V_{SS}$ and $AV_{SS}$ | | 50 | mV |
| $V_{IN}$ | Input Voltage on 5V-tolerance GPIO | | 5.5 | V |
| | Input Voltage on RTC domain (PF.6 ~ PF.11) | | $V_{DD}$ | V |
| | Input Voltage on any other pin[*2] | | $V_{DD}$ | V |

Table 8.1-1 Voltage Characteristics

**Note:**

1. All main power ($V_{DD}$, $AV_{DD}$) and ground ($V_{SS}$, $AV_{SS}$) pins must always be connected to the external power supply, in the permitted range.
2. Non 5V-tolerance PIN: PA.8 ~ 15; PB.0 ~ 15; PD.10, 11, 12; PF.2, 3, 4, 5; All USB High Speed PIN and nRESET PIN.

### 8.1.2 Current Characteristics

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $I_{DD}$ | Maximum Current into $V_{DD}$ | | 200 | mA |
| $I_{DDIO}$ | Maximum Current into $V_{DDIO}$ | | 100 | |
| $I_{SS}$ | Maximum Current out of $V_{SS}$ | | 100 | |
| $I_{IO}$ | Maximum Current sunk by a I/O Pin | | 20 | |
| | Maximum Current Sourced by a I/O Pin | | 20 | |
| | Maximum Current Sunk by Total I/O Pins | | 100 | |
| | Maximum Current Sourced by Total I/O Pins | | 100 | |

Table 8.1-2 Current Characteristics

### 8.1.3 Thermal Characteristics

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_A$ | Operating Temperature | -40 | 105 | °C |
| $T_J$ | Junction temperature | -40 | 125 | |
| $T_{ST}$ | Storage Temperature | -65 | 150 | |

Table 8.1-3 Thermal Characteristics

### 8.1.4 EMC Characteristics

| Symbol | Parameter | Conditions | Maximum value | Unit |
|---|---|---|---|---|
| $V_{EFTB}$ | 1. Fast transient voltage burst limits to be applied through 100 pF + 47uF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance<br>2. to be applied through 2.2uF on LDO_Pin and VSS pins | $V_{DD}$ = 3.3 V, LQFP144, $T_A$ = +25 °C, $f_{HCLK}$ = 160 MHz | 4.4 | kV |

Table 8.1-4 EMS Characteristics

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +25 °C | 400mA | mA |

Table 8.1-5 Electrical Characteristics

**Note:** Guaranteed by characterization results, not tested in production.

## 8.2 General Operating Conditions

($V_{DD}$-$V_{SS}$ = 1.8 ~ 3.6V, $T_A$ = 25°C, HCLK = 192 MHz unless otherwise specified.)

| SYMBOL | PARAMETER | Conditions | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | | | | 192 | MHz |
| $V_{DD}$ | Operation Voltage | | 1.8 | | 3.6 | V |
| $AV_{DD}$ | Analog Operation Voltage | | $V_{DD}$ | | | |
| $V_{DDIO}$ | Power supply for PA.0 ~ 5 | | 1.8 | | 3.6 | |
| $V_{LDO}$ | LDO Output Voltage | | 1.08 | 1.2 | 1.32 | |
| $V_{BG}$ | Band-gap Voltage | $V_{DD}$ = 1.8 V ~ 3.6 V | 1.18 | | 1.21 | |
| $C_{LDO}$ | LDO Output capacitance on each pin | | | 2.2 | | uF |
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 10 | - | | µs/V |
| | $V_{DD}$ fall time rate | BOD Disabled, LVR Enabled[*1] | 400 | - | | |
| | | BOD Disabled, LVR Enabled[*2] | 500 | | | |
| | | BOD 1.6V Enabled | 80 | | | |
| | | BOD 3.0V Enabled | 80 | | | |

**Note:**

1. LVR in active mode
2. LVR in low power mode

## 8.3 DC Electrical Characteristics

### 8.3.1 Typical Current Consumption

- ALL GPIO pins are in push pull mode, output high.
- LDO = 1.26V
- The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}/2$.
- Program run while(1){} from flash.

| Symbol | Conditions | $f_{HCLK}$ | HXT/LXT | HIRC/LIRC | PLL | Typ $T_A$ = 25 °C | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Normal Run, executed from flash, $V_{DD}$ = 3.3V, all peripherals disable | 192 MHz | 12MHz | - | V | 34.00 | mA |
| | | 160 MHz | 12MHz | - | V | 28.76 | |
| | | 144 MHz | 12MHz | - | V | 26.00 | |
| | | 120 MHz | 12MHz | - | V | 22.21 | |
| | | 12 MHz | 12MHz | - | - | 3.49 | |
| | | 192 MHz | - | 12MHz | V | 33.29 | |
| | | 160 MHz | - | 12MHz | V | 28.11 | |
| | | 144 MHz | - | 12MHz | V | 25.51 | |
| | | 120 MHz | - | 12MHz | V | 21.59 | |
| | | 12 MHz | - | 12MHz | - | 2.98 | |
| | | 32.768 KHz | 32.768 kHz | - | - | 0.57 | |
| | | 10 KHz | - | 10KHz | - | 0.57 | |
| | Normal run, External clock, executed from flash, $V_{DD}$ = 3.3V, all peripherals enabled | 192 MHz | - | 12MHz | V | 70.05 | |
| | | 160 MHz | - | 12MHz | V | 58.99 | |
| | | 144 MHz | - | 12MHz | V | 53.43 | |
| | | 120 MHz | - | 12MHz | V | 45.04 | |
| | | 12 MHz | - | 12MHz | - | 5.60 | |
| | | 192 MHz | 12MHz | - | V | 70.70 | |
| | | 160 MHz | 12MHz | - | V | 60.41 | |
| | | 144 MHz | 12MHz | - | V | 53.75 | |
| | | 120 MHz | 12MHz | - | V | 46.04 | |
| | | 12 MHz | 12MHz | - | - | 5.85 | |
| | | 32.768 KHz | 32.768 kHz | - | - | 0.58 | |
| | | 10 KHz | - | 10KHz | - | 0.57 | |

Table 8.3-1 Current Consumption in Normal Run Mode

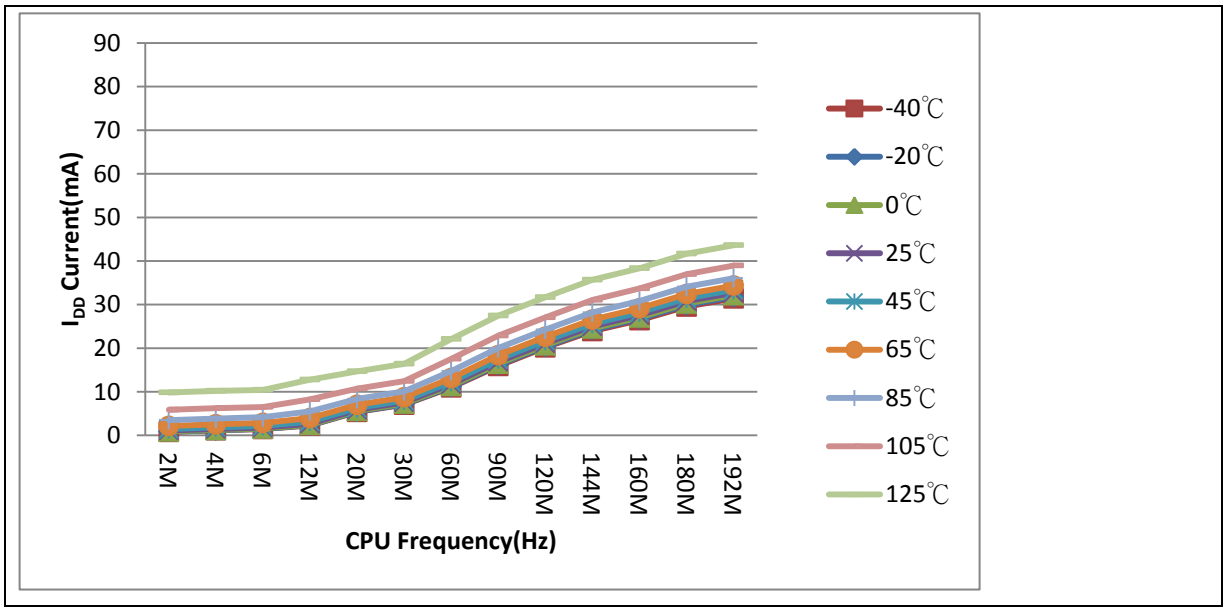



Figure 8.3-1 Current Consumption versus Temperature in Normal Run Mode, $V_{DD}$ = 3.3V , All Peripherals Disabled, PLL Source from HIRC

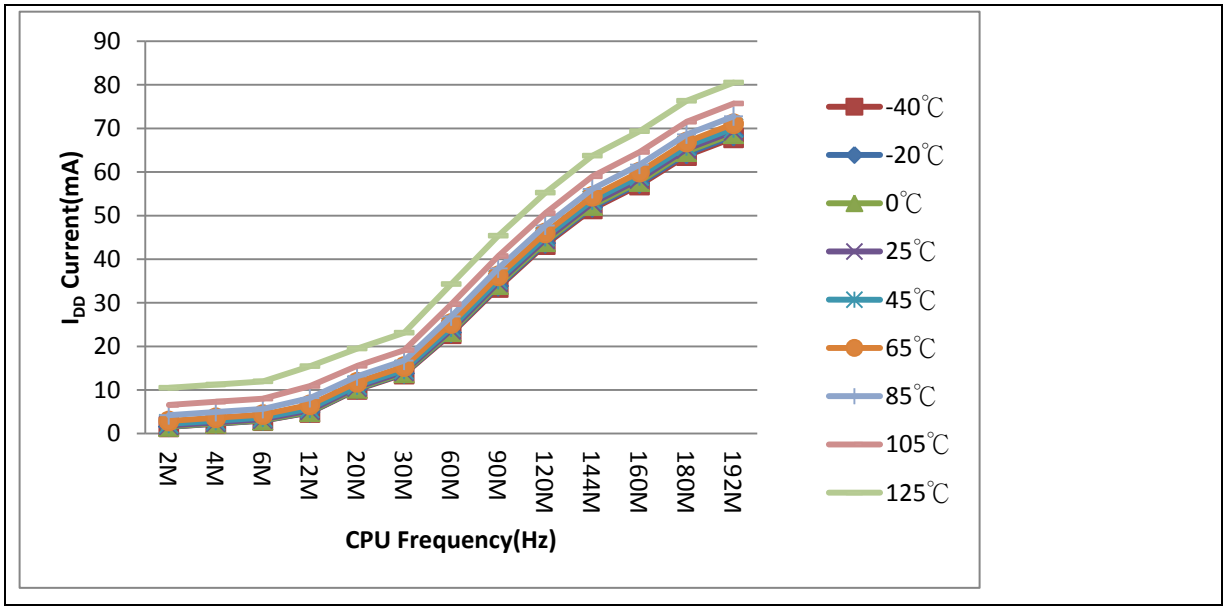



Figure 8.3-2 Current Consumption versus Temperature in Normal Run Mode, $V_{DD}$ = 3.3V , All Peripherals Enabled, PLL Source from HIRC

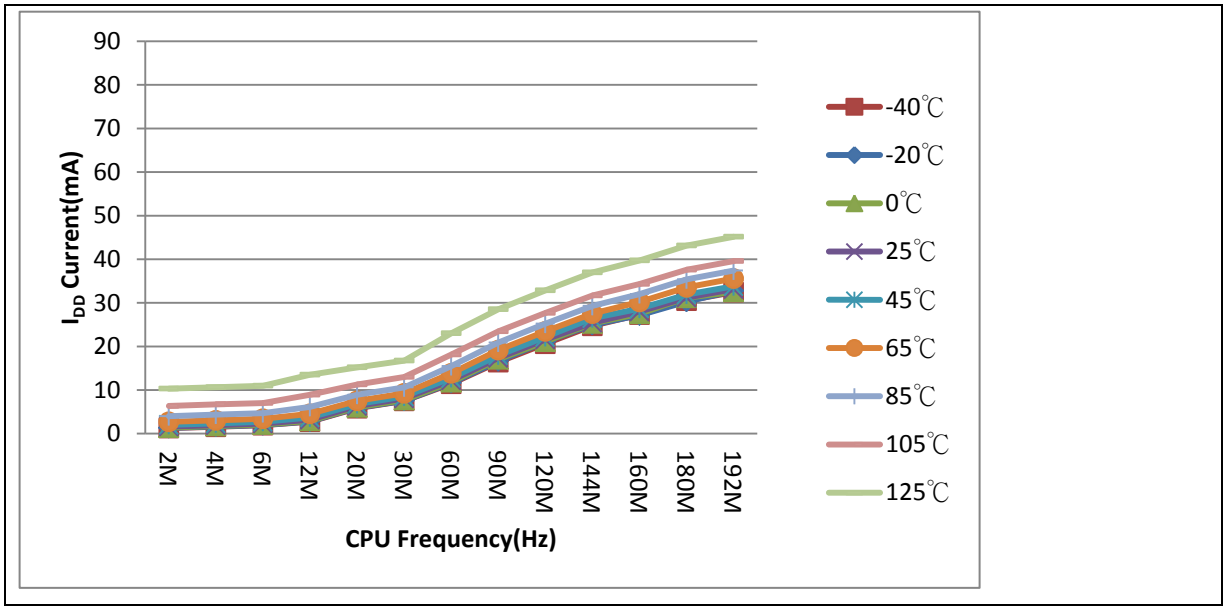



Figure 8.3-3 Current Consumption versus temperature in Normal Run Mode, $V_{DD}$ = 3.3V , All Peripherals Disabled, PLL Source from HXT

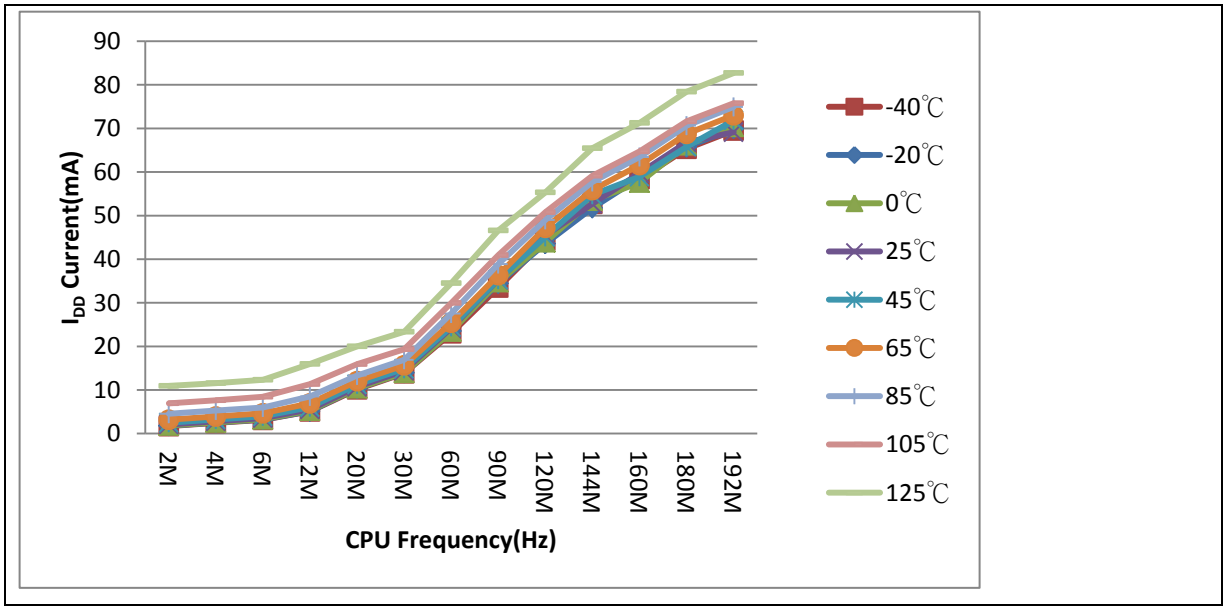



Figure 8.3-4 Current Consumption versus Temperature in Normal Run Mode, $V_{DD}$ = 3.3V , All Peripherals Enabled, PLL Source from HXT

| Symbol | Conditions | $f_{HCLK}$ | HXT/LXT | HIRC/LIRC | PLL | Typ | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | | $T_A$ = 25 °C | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Idle mode, executed from flash, $V_{DD}$ = 3.3V, all peripherals disable | 192 MHz | 12MHz | - | V | 10.32 | mA |
| | | 160 MHz | 12MHz | - | V | 8.95 | |
| | | 144 MHz | 12MHz | - | V | 8.23 | |
| | | 120 MHz | 12MHz | - | V | 7.23 | |
| | | 12 MHz | 12MHz | - | - | 1.98 | |
| | | 192 MHz | - | 12MHz | V | 9.76 | |
| | | 160 MHz | - | 12MHz | V | 8.40 | |
| | | 144 MHz | - | 12MHz | V | 7.72 | |
| | | 120 MHz | - | 12MHz | V | 6.70 | |
| | | 12 MHz | - | 12MHz | - | 1.47 | |
| | | 32.768 KHz | 32.768 kHz | - | - | 0.57 | |
| | | 10 KHz | - | 10KHz | - | 0.57 | |
| | Idle mode, External clock, executed from flash, $V_{DD}$ = 3.3V, all peripherals enabled | 192 MHz | - | 12MHz | V | 49.64 | |
| | | 160 MHz | - | 12MHz | V | 41.82 | |
| | | 144 MHz | - | 12MHz | V | 37.89 | |
| | | 120 MHz | - | 12MHz | V | 31.96 | |
| | | 12 MHz | - | 12MHz | - | 4.03 | |
| | | 192 MHz | 12MHz | - | V | 50.36 | |
| | | 160 MHz | 12MHz | - | V | 42.75 | |
| | | 144 MHz | 12MHz | - | V | 38.29 | |
| | | 120 MHz | 12MHz | - | V | 32.70 | |
| | | 12 MHz | 12MHz | - | - | 4.52 | |
| | | 32.768 KHz | 32.768 kHz | - | - | 0.58 | |
| | | 10 KHz | - | 10KHz | - | 0.57 | |

Table 8.3-2 Current Consumption in Idle Mode

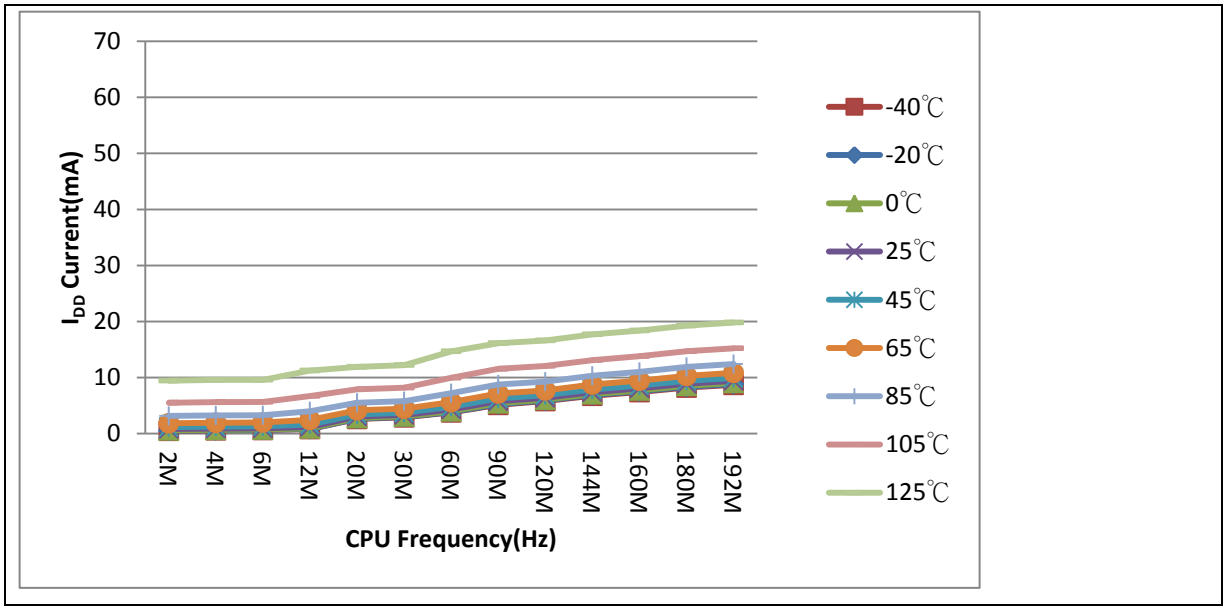



Figure 8.3-5 Current Consumption versus Temperature in Idle Mode, $V_{DD}$ = 3.3V , All Peripherals Disabled, PLL Source from HIRC

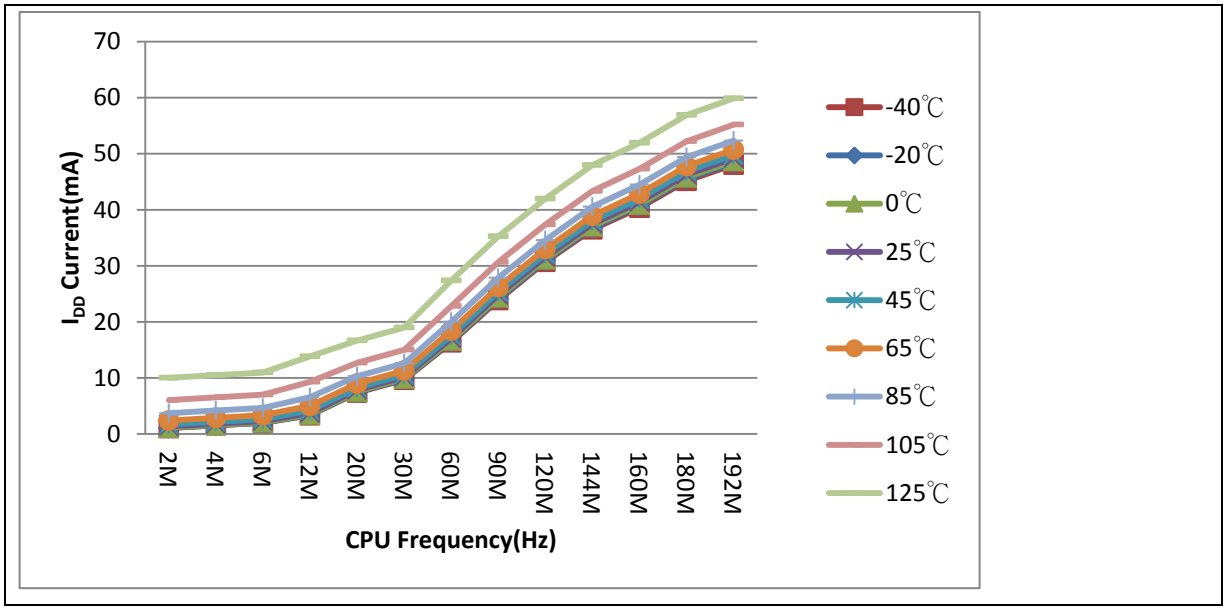



Figure 8.3-6 Current Consumption versus Temperature in Idle Mode, $V_{DD}$ = 3.3V , All Peripherals Enabled, PLL Source from HIRC

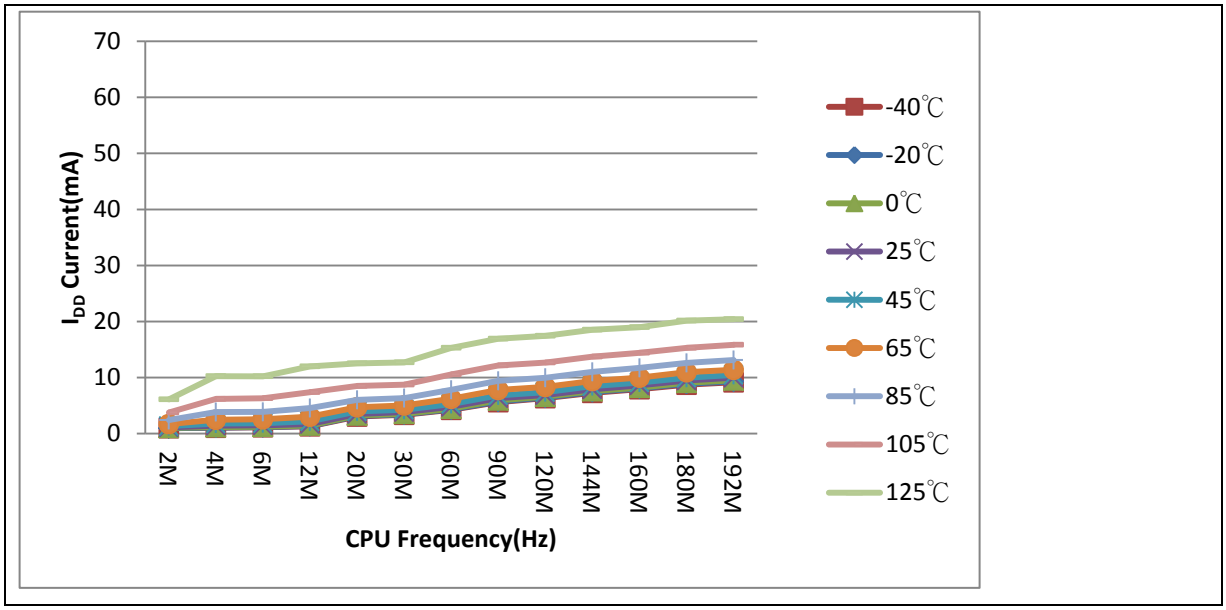



Figure 8.3-7 Current Consumption versus Temperature in Idle Mode, $V_{DD}$ = 3.3V , All Peripherals Disabled, PLL Source from HXT

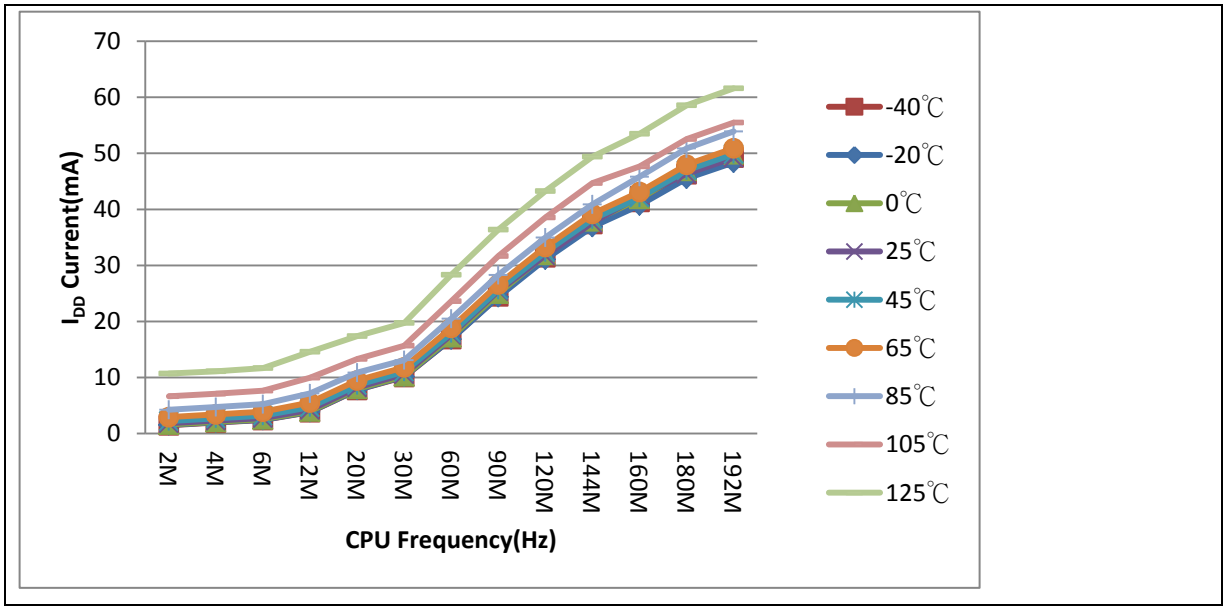



Figure 8.3-8 Current Consumption versus Temperature in Idle Mode, $V_{DD}$ = 3.3V , All Peripherals Enabled, PLL Source from HXT

| Symbol | Conditions | LXT | LIRC | PLL | Typ | Unit |
|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{DD\_FWPD}$ | Fast wake-up Power-down mode, $V_{DD}$ = 3.3V, all peripherals disabled | - | - | - | 0.49 | mA |
| | Fast wake-up Power-down mode, $V_{DD}$ = 3.3V, RTC/WDT/Timer/UART enable | V | - | - | 0.49 | |
| | Fast wake-up Power-down mode, $V_{DD}$ = 3.3V, RTC/WDT/Timer enable | - | V | - | 0.49 | |
| | Fast wake-up Power-down mode, $V_{DD}$ = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT | V | V | - | 0.49 | |
| $I_{DD\_PD}$ | Power-down mode, $V_{DD}$ = 3.3V, all peripherals disabled | - | - | - | 0.37 | mA |
| | Power-down mode, $V_{DD}$ = 3.3V, RTC/WDT/Timer/UART enable | V | - | - | 0.37 | |
| | Power-down mode, $V_{DD}$ = 3.3V, RTC/WDT/Timer use LIRCT | - | V | - | 0.37 | |
| | Power-down mode, $V_{DD}$ = 3.3V, WDT/Timer use LIRC, RTC/UART use LX | V | V | - | 0.37 | |
| $I_{DD\_LLPD}$ | Low leakage Power-down mode, $V_{DD}$ = 3.3V, all peripherals disabled | - | - | - | 0.14 | mA |
| | Low leakage Power-down mode, $V_{DD}$ = 3.3V, RTC/WDT/Timer/UART enable | V | - | - | 0.37 | |
| | Low leakage Power-down mode, $V_{DD}$ = 3.3V, RTC/WDT/Timer enable | - | V | - | 0.37 | |
| | Low leakage Power-down mode, $V_{DD}$ = 3.3V, WDT/Timer use LIRC, RTC/UART use LX | V | V | - | 0.37 | |
| $I_{DD\_SPD0}$ | Standby Power-down mode(SPD0), $V_{DD}$ = 3.3V, all peripherals disabled | - | - | - | 0.04 | mA |
| | Standby Power-down mode(SPD0), $V_{DD}$ = 3.3V, RTC enable | V | - | - | 0.04 | |
| | Standby Power-down mode(SPD0), $V_{DD}$ = 3.3V, RTC enable | - | V | - | 0.04 | |
| $I_{DD\_SPD1}$ | Standby Power-down mode(SPD1), $V_{DD}$ = 3.3V, all peripherals disabled | - | - | - | 0.03 | mA |
| | Standby Power-down mode(SPD1), $V_{DD}$ = 3.3V, RTC enable | V | - | - | 0.03 | |
| | Standby Power-down mode(SPD1), $V_{DD}$ = 3.3V, RTC enable | - | V | - | 0.03 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{DD\_DPD}$ | Deep Power-down mode(DPD), $V_{DD}$ = 3.3V, all peripherals disabled | - | - | - | 0.95 | uA |

Table 8.3-3 Chip Current Consumption in Power-down Mode

**Note:** $V_{DD} = AV_{DD} = V_{DDIO} = 3.3V$

### 8.3.2 On-chip Peripheral Current Consumption

- ALL GPIO pins are in push pull mode, output high.
- LDO = 1.26V
- The typical values for $T_A$= 25 ˚C and $V_{DD} = AV_{DD}$ = 3.3 V unless otherwise specified.
- When the peripherals are enabled HCLK is the system clock, $f_{HCLK}$ = 192 MHz, $f_{PCLK0, 1} = f_{HCLK}/2$.

| Peripheral | $I_{DD}$ | Unit |
|---|---|---|
| DAC | 58.4 | uA |
| ADC | 338.6 | |
| ACMP01 | 85.2 | |
| OPA | 123.3 | |
| QEI0 | 74.2 | |
| QEI1 | 81.9 | |
| ECAP0 | 74.3 | |
| ECAP1 | 69.8 | |
| EPWM0 | 907 | |
| EPWM1 | 896.5 | |
| BPWM0 | 263.8 | |
| BPWM1 | 245.2 | |
| WDT | 49.6 | |
| SD0 | 1416.1 | |
| SD1 | 1263.6 | |
| SC0 | 66.6 | |
| SC1 | 76.6 | |
| SC2 | 73.6 | |
| I2S0 | 102.1 | |
| SPIM | 14681.1 | |
| QSPI0 | 291.1 | |
| SPI0 | 315.5 | |
| SPI1 | 261.2 | |

| | |
|---|---|
| SPI2 | 137.2 |
| SPI3 | 138.7 |
| UART0 | 150.6 |
| UART1 | 209.1 |
| UART2 | 220.0 |
| UART3 | 160.5 |
| UART4 | 186.5 |
| UART5 | 177.5 |
| I2C0 | 34.4 |
| I2C1 | 26.6 |
| I2C2 | 32.7 |
| CAN0 | 280.5 |
| CAN1 | 257.6 |
| USCI0 | 211.9 |
| USCI1 | 205.4 |
| EBI | 209.6 |
| TMR0 | 140.5 |
| TMR1 | 130.1 |
| TMR2 | 127.1 |
| TMR3 | 121.2 |
| USB HS OTG | 248.7 |
| USB FS OTG | 503.1 |
| Crypto | 1550.4 |
| EMAC | 1768.1 |

**Note:** Guaranteed by characterization results, not tested in production.

### 8.3.3 Wakeup Time

- The wakeup times given in Table 8.3-4 is measured on a wakeup phase with a 16 MHz HIRC oscillator. The clock source used to wake up the device depends from the current operating mode:
  - Fast-wakeup, power down, low leakage Power-down mode: the clock source is the RC oscillator
  - Standby and Deep Power-down mode: the clock source is the clock that was set before entering Sleep mode.
- The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
- The clock source is the RC oscillator from HIRC

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $t_{WU\_IDLE}$ | Wakeup from IDLE mode | 5 Cycles | µs |
| $t_{WU\_FWPD}$ | Wakeup from Fast-wakeup power down mode | 6 | |
| $t_{WU\_NPD}$ | Wakeup from normal power down mode | 12 | |
| $t_{WU\_LLPD}$ | Wakeup from low leakage power down mode | 54 | |
| $t_{WU\_SPD0}$ | Wakeup from Standby Power-down mode 0 (SPD0) | 527 | |
| $t_{WU\_SPD1}$ | Wakeup from Standby Power-down mode 1 (SPD1) | 527 | |
| $t_{WU\_DPD}$ | Deep Power-down mode (DPD) | 489 | |

Table 8.3-4 Low-power Mode Wakeup Timings

### 8.3.4 PIN DC Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL1}$ | Input Low Voltage (TTL input) | | | 0.8 | V | $V_{DD} = V_{DDIO} = 3.6$ V |
| | | | | 0.56 | V | $V_{DD} = V_{DDIO} = 1.8$ V |
| $V_{IH1}$ | Input High Voltage (TTL input) | 2 | | | V | $V_{DD} = V_{DDIO} = 3.6$V |
| | | 1.04 | | | V | $V_{DD} = V_{DDIO} = 1.8$V |
| $V_{IL2}$ | Input Low Voltage (Schmitt input) | | | $0.3*V_{DD}$ | V | $V_{DD} = V_{DDIO} = 3.6$V |
| | | | | $0.3*V_{DD}$ | | $V_{DD} = V_{DDIO} = 1.8$V |
| $V_{IH2}$ | Input High Voltage (Schmitt input) | $0.7*V_{DD}$ | | | V | $V_{DD} = V_{DDIO} = 3.6$V |
| | | $0.7*V_{DD}$ | | | | $V_{DD} = V_{DDIO} = 1.8$V |
| $V_{HY}$ | Hysteresis voltage of (Schmitt input) | | $0.2V_{DD}$ | | V | |
| $I_{LK}$ | Input Leakage Current | -1 | | 1 | µA | $V_{DD} = V_{DDIO} = 3.6$V, $0 < V_{IN} < V_{DD}$, Open-drain or input only mode |
| $R_{PU}$ | Input Pull Up Resistor | | 50 | | KΩ | $V_{DD} = V_{DDIO} = 3.3$V |
| | | | 52 | | KΩ | $V_{DD} = V_{DDIO} = 1.8$V |
| $R_{PD}$ | Input Pull down Resistor | | 50 | | KΩ | $V_{DD} = V_{DDIO} = 3.3$V |
| | | | 52 | | KΩ | $V_{DD} = V_{DDIO} = 1.8$V |

Table 8.3-5 PIN Input Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{SR4}$ | Source Current (Push-pull Mode, Set GPIO to output HIGH, Apply GPIO pin VIN=($V_{DD}$-0.4)V for $V_{DD}$ and measure the source current) | | -18 | | mA | $V_{DD} = V_{DDIO} = 3.3$V |
| $I_{SR5}$ | | | -10 | | mA | $V_{DD} = V_{DDIO} = 1.8$V |
| $I_{SR6}$ | | | -8 | | mA | $V_{DD} = V_{DDIO} = 1.8$V |
| $I_{SK1}$ | Sink Current (Push-pull Mode, Set GPIO to output LOW, Apply GPIO pin VIN=(VSS+0.4)V for VSS and measure | | 17 | | mA | $V_{DD} = V_{DDIO} = 3.3$V |
| $I_{SK2}$ | | | 10 | | mA | $V_{DD} = V_{DDIO} = 1.8$V |

| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{SK3}$ | the source current) | | 8 | | mA | $V_{DD}$ = $V_{DDIO}$ = 1.8V |
| $C_{IO}$ | I/O pin capacitance | | 5 | | pF | |

Table 8.3-6 PIN Output Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | unit | **Test Conditions** |
|---|---|---|---|---|---|---|
| $V_{ILR}$ | Negative going threshold (Schmitt input), nRESET | | | 0.3*$V_{DD}$ | V | $V_{DD}$ = 3.3V |
| $V_{IHR}$ | Positive going threshold (Schmitt Input), nRESET | 0.7*$V_{DD}$ | | | V | $V_{DD}$ = 3.3V |
| $R_{RST}$ | Internal nRESET pin pull up resistor | | 50 | | KΩ | |
| $t_{FR1}$ | nRESET input filtered time | | 32 | | uS | |
| $t_{FR2}$ | nRESET input filtered time under SPD and DPD mode | | 300 | | nS | $V_{DD}$ = 3.3V, |

Table 8.3-7 nRESET PIN Characteristics

## 8.4 AC Electrical Characteristics

### 8.4.1 External 4~24 MHz High Speed Crystal (HXT) characteristics

- $T_A$= 25 ˚C and $V_{DD}$ = 3.3 V unless otherwise specified.

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $V_{DD}$ | Operating Voltage | 1.8 | | 3.6 | V | |
| $R_f$ | Feedback resister | | 1000 | | kΩ | |
| $f_{HXT}$ | Oscillator frequency | 4 | | 24 | MHz | $V_{DD}$ = 1.8 ~ 3.6V |
| $T_{HXT}$ | Temperature Range | -40 | | 105 | °C | |
| $I_{HXT\_INV}$ | Current Consumption (INV-type Crystal) | | 650 | | µA | 4MHz |
| | | | 1600 | | | 12MHz |
| | | | 2000 | | | 16MHz |
| | | | 4000 | | | 24MHz |
| $I_{HXT\_GM}$ | Current Consumption (GM-type Crystal) | | 160 | | µA | 4MHz |
| | | | 280 | | | 12MHz |
| | | | 400 | | | 16MHz |
| | | | 600 | | | 24MHz |
| $T_{S\_GM}$ | Stable time (GM-type) | 1545 | | 1752 | µs | 4MHz, -40 ˚C |
| | | 1630 | | 1757 | | 4MHz, 25 ˚C |
| | | 1054 | | 1988 | | 4MHz, 105 ˚C |
| | | 484 | | 512 | | 12MHz, -40 ˚C |
| | | 484 | | 544 | | 12MHz, 25 ˚C |
| | | 386 | | 606 | | 12MHz, 105 ˚C |
| | | 349 | | 375 | | 16MHz, -40 ˚C |
| | | 337 | | 399 | | 16MHz, 25 ˚C |
| | | 281 | | 444 | | 16MHz, 105 ˚C |
| | | 259 | | 303 | | 24MHz, -40 ˚C |
| | | 248 | | 330 | | 24MHz, 25 ˚C |
| | | 210 | | 403 | | 24MHz, 105 ˚C |
| $T_{S\_INV}$ | Stable time (INV-type) | 1490 | | 23432 | µs | 4MHz, -40 ˚C |
| | | 1479 | | 2352 | | 4MHz, 25 ˚C |
| | | 1052 | | 2105 | | 4MHz, 105 ˚C |
| | | 464 | | 558 | | 12MHz, -40 ˚C |

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| | | 481 | | 554 | | 12MHz, 25 ˚C |
| | | 417 | | 663 | | 12MHz, 105 ˚C |
| | | 317 | | 420 | | 16MHz, -40 ˚C |
| | | 326 | | 407 | | 16MHz, 25 ˚C |
| | | 290 | | 472 | | 16MHz, 105 ˚C |
| | | 226 | | 382 | | 24MHz, -40 ˚C |
| | | 228 | | 388 | | 24MHz, 25 ˚C |
| | | 210 | | 441 | | 24MHz, 105 ˚C |
| | Clock Duty | 45 | 50 | 55 | % | |

Table 8.4-1 External 4~24 MHz High Speed Crystal (HXT) Oscillator

#### *8.4.1.1 Typical Crystal Application Circuits*

| CRYSTAL | C1 | C2 | R |
|---|---|---|---|
| 4MHz ~ 24 MHz | 20pF | 20pF | without |

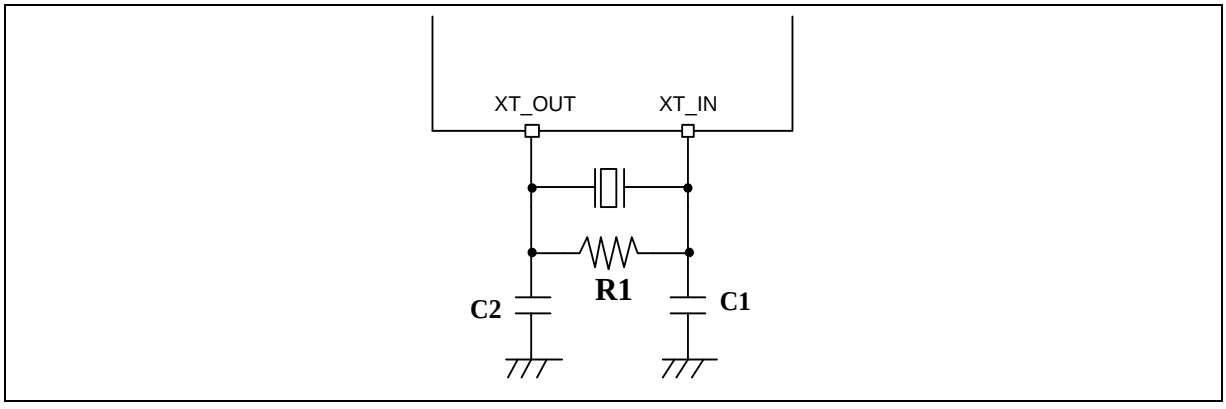
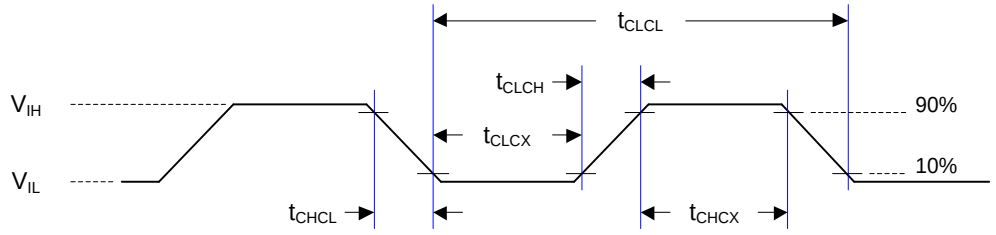



Figure 8.4-1 Typical Crystal Application Circuit

### 8.4.2 External 4~24 MHz High Speed Clock Input (OSC) Characteristics

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $t_{CHCX}$ | Clock High Time | 18 | | | nS | |
| $t_{CLCX}$ | Clock Low Time | 18 | | | nS | |

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $t_{CLCH}$ | Clock Rise Time | | | 10 | nS | |
| $t_{CHCL}$ | Clock Fall Time | | | 10 | nS | |
| $V_{IH}$ | Input High Voltage | | | 0.7*$V_{DD}$ | V | |
| $V_{IL}$ | Input Low Voltage | 0.3*$V_{DD}$ | | | V | |




**Note:** Duty cycle is 50%.

**Notes:** Guaranteed by design, not tested in production

### 8.4.3 External 32.768 kHz Low Speed Crystal (LXT) characteristics

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $V_{DD}$ | Operation Voltage | 1.8 | | 3.6 | V | |
| $f_{LXT}$ | Oscillator frequency | | 32.768 | | kHz | $V_{DD}$ = 1.8 ~ 3.6 V |
| $T_{LXT}$ | Temperature | -40 | | 105 | °C | |
| $I_{LXT}$ | Operating current | | | 0.5 | μA | $V_{DD}$ = 3.3V |
| | Duty cycle | 45 | | 55 | % | |
| $T_S$ | Stable Time | | | 500 | ms | |

Table 8.4-2 External 32.768 kHz Crystal

#### *8.4.3.1 Typical Crystal Application Circuits*

| CRYSTAL | C1 | C2 | R1 |
|---|---|---|---|
| 32.768 kHz | 20pF | 20pF | without |

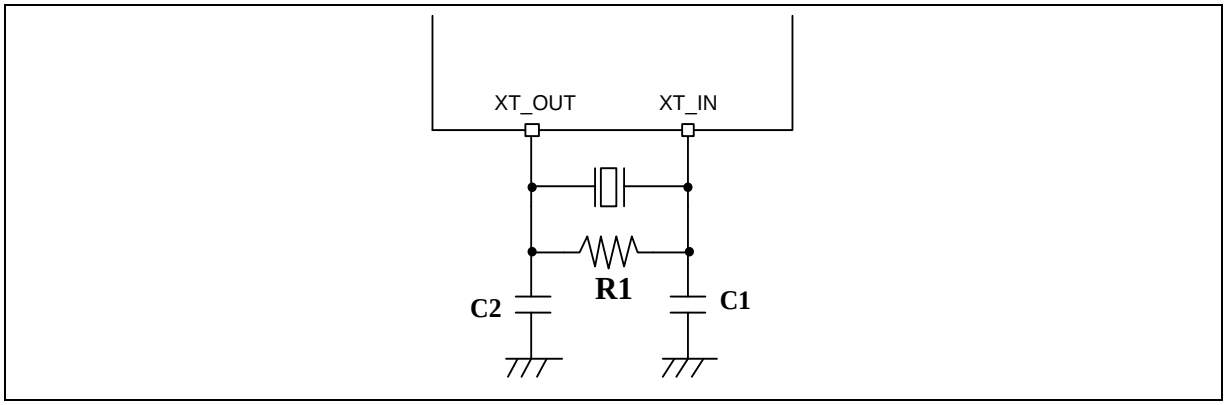
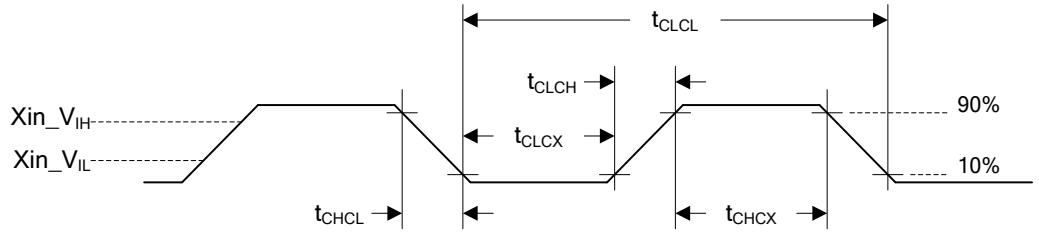



Figure 8.4-2 Typical Crystal Application Circuit

### 8.4.4 External 32.768 kHz Low Speed Clock Input (OSC) Characteristics

| PARAMETER | SYM. | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| Clock High Time | $t_{CHCX}$ | 450 | - | - | nS | |
| Clock Low Time | $t_{CLCX}$ | 450 | - | - | nS | |
| Clock Rise Time | $t_{CLCH}$ | | - | 50 | nS | |
| Clock Fall Time | $t_{CHCL}$ | | - | 50 | nS | |
| LXT Input Pin Input High Voltage | Xin_VIH | | | $0.7*V_{DD}$ | V | |
| LXT Input Pin Input Low Voltage | Xin_VIL | $0.3*V_{DD}$ | | | V | |




***Note:*** *Duty cycle is 50%.*

Note: Duty cycle is 50%.

**Notes:** Guaranteed by design, not tested in production

### 8.4.5 12 MHz Internal High Speed RC Oscillator (HIRC)

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $V_{HRC}$ | Supply voltage | 1.8 | | 3.6 | V | |
| $f_{HRC}$ | Center Frequency | | 12 | | MHz | |

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| | Internal Oscillator Frequency[*1] | -1 | | 1 | % | $T_A$ = 25 °C, $V_{DD}$ = 3.3V |
| | | -2 | | 2 | % | -40°C ~ +105 °C, $V_{DD}$ = 1.8 ~ 3.6V |
| $I_{HRC}$ | Operating current | | 155 | | μA | |
| $T_S$ | Stable time | | | 4 | us | |

**Note:** Guaranteed by characterization, not tested in production

### 8.4.6 10 kHz Internal Low Speed RC Oscillator (LIRC)

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $V_{LRC}$ | Supply voltage | 1.8 | | 3.6 | V | |
| $F_{LRC}$ | Oscillator Frequency[*1] | 5 | | 20 | kHz | $V_{DD}$=1.8V~3.6V, $T_A$=-40~105°C |
| $I_{LRC}$ | Operating current | | | 0.5 | μA | $V_{DD}$ = 3.3V |
| $T_S$ | Stable time | | 200 | | μs | |

**Note:** Guaranteed by characterization, not tested in production

### 8.4.7 PLL Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL\_IN}$ | PLL input clock | | 4 | | 24 | MHz |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | | 50 | | 500 | MHz |
| $T_S$ | PLL stable time[*1] | | 100 | | 200 | μs |
| Jitter | Cycle-to-cycle Jitter[*2] | Peak to peak @ 480M | | 250 | | ps |
| $I_{DD}$ | Power consumption | $V_{DD}$=3.3V@500MHz | | | 3 | mA |

**Note:**

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

### 8.4.8 PIN AC Characteristics

- $C_L$ = 51 pF

| Px_SLEWCTL | Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 00 | $t_{f(IO)out}$ | Output high to low level fall time (90~10%) | $V_{DD}$ = 3.6 V | 4.384 | ns |
| | | | $V_{DD}$ = 1.8 V | 8.532 | |
| | $t_{r(IO)out}$ | output low to high level rise time (10~90%) | $V_{DD}$ = 3.6 V | 4.086 | |
| | | | $V_{DD}$ = 1.8 V | 8.225 | |
| 01 | $t_{f(IO)out}$ | Output high to low level fall time (90~10%) | $V_{DD}$ = 3.6 V | 3.005 | |
| | | | $V_{DD}$ = 1.8 V | 6.153 | |
| | $t_{r(IO)out}$ | output low to high level rise time (10~90%) | $V_{DD}$ = 3.6 V | 3.404 | |
| | | | $V_{DD}$ = 1.8 V | 6.29 | |
| 10 | $t_{f(IO)out}$ | Output high to low level fall time (90~10%) | $V_{DD}$ = 3.6 V | 3.054 | |
| | | | $V_{DD}$ = 1.8 V | 6.152 | |
| | $t_{r(IO)out}$ | output low to high level rise time (10~90%) | $V_{DD}$ = 3.6 V | 3.389 | |
| | | | $V_{DD}$ = 1.8 V | 6.269 | |

Table 8.4-3 I/O AC Characteristics

## 8.5 Analog Electrical Characteristics

### 8.5.1 LDO

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{DD}$ | DC Power Supply | 1.8 | | 3.6 | V | |
| $V_{LDO}$ | Output Voltage | 1.08 | 1.26 | 1.32 | V | |
| $T_A$ | Temperature | -40 | | 105 | ℃ | |

**Note:**

1. It is recommended a 0.1μF bypass capacitor is connected between $V_{DD}$ and the closest $V_{SS}$ pin of the device.
2. For ensuring power stability, a 2.2μF capacitor must be connected between LDO_CAP pin and the closest $V_{SS}$ pin of the device.

### 8.5.2 Low-Voltage Reset

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Supply Voltage | 0 | | 3.6 | V | |
| $T_A$ | Temperature | -40 | | 105 | ℃ | - |
| $I_{LVR}$ | Operating Current | | 0.5 | | uA | $AV_{DD}$ = 3.6V |
| $V_{LVR}$ | Threshold Voltage | 1.40 | 1.48 | 1.56 | V | $T_A$ = 105 ℃ |
| | | 1.40 | 1.48 | 1.56 | V | $T_A$ = 25 ℃ |
| | | 1.40 | 1.48 | 1.56 | V | $T_A$ = -40 ℃ |

### 8.5.3 Brown-out Detector

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Supply Voltage | 0 | | 3.6 | V | - |
| $T_A$ | Temperature | -40 | | 105 | ℃ | - |
| $I_{BOD}$ | Operating Current | | 66 | | μA | $AV_{DD}$ = 3.6V |
| $V_{BOD\_F}$ | Brown-out Voltage (Falling edge) | 2.9 | 3.0 | 3.1 | V | BODVL [2:0] = 111 |
| | | 2.7 | 2.8 | 2.9 | V | BODVL [2:0] = 110 |
| | | 2.5 | 2.6 | 2.7 | V | BODVL [2:0] = 101 |
| | | 2.3 | 2.4 | 2.5 | V | BODVL [2:0] = 100 |
| | | 2.1 | 2.2 | 2.3 | V | BODVL [2:0] = 011 |
| | | 1.9 | 2.0 | 2.1 | V | BODVL [2:0] = 010 |
| | | 1.7 | 1.8 | 1.9 | V | BODVL [2:0] = 001 |
| | | 1.5 | 1.6 | 1.7 | V | BODVL [2:0] = 000 |
| $V_{BOD\_R}$ | Brown-out Voltage (Rising edge) | 3.0 | 3.1 | 3.2 | V | BODVL [2:0] = 111 |
| | | 2.8 | 2.9 | 3.0 | V | BODVL [2:0] = 110 |
| | | 2.6 | 2.7 | 2.8 | V | BODVL [2:0] = 101 |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | 2.4 | 2.5 | 2.6 | V | BODVL [2:0] = 100 |
| | | 2.2 | 2.3 | 2.4 | V | BODVL [2:0] = 011 |
| | | 2.0 | 2.1 | 2.2 | V | BODVL [2:0] = 010 |
| | | 1.8 | 1.9 | 2.0 | V | BODVL [2:0] = 001 |
| | | 1.6 | 1.7 | 1.8 | V | BODVL [2:0] = 000 |
| $T_{BOD\_RE}$ | Respond Time | | 1 | | ms | Respond Time |

### 8.5.4 Power-on Reset

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_A$ | Temperature | -40 | - | +105 | ℃ | - |
| $V_{POR}$ | Reset Voltage | | 1.47 | | V | - |
| $RRV_{DD}$ | $V_{DD}$ Raising Rate to Ensure Power-on Reset[*1] | 10 | | | us/V | |
| $FRV_{DD}$ | $V_{DD}$ Falling Rate to Ensure Power-on Reset[*1] | 320 | | | us/V | |

**Note:** Guaranteed by characterization, not tested in production

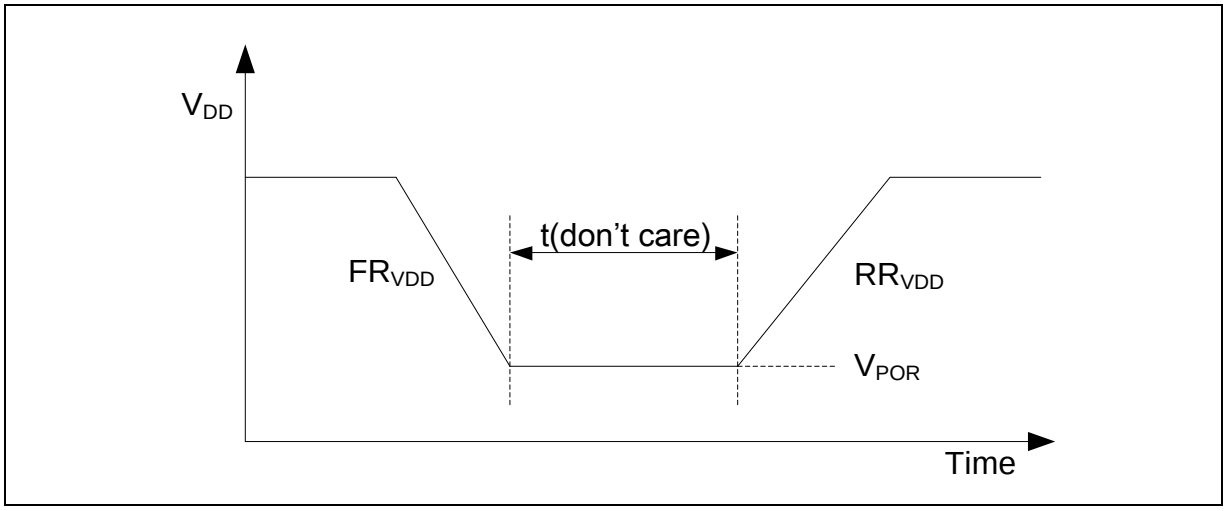



Figure 8.5-1 Power-up Ramp Condition

### 8.5.5 Internal Voltage Reference

- The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 ˚C and $V_{DD}$ = 3.3 V unless otherwise specified.

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{REF\_INT}$ | Internal reference voltage | | 1.6 | | V | |
| | | | 2.0 | | | |
| | | | 2.5 | | | |
| | | | 3.0 | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $AV_{DD\_min}$ | $AV_{DD}$ minimum voltage | 2 | | | V | $V_{REF\_OUT}$ = 1.6 v |
| | | 2.2 | | | | $V_{REF\_OUT}$ = 2.0 v |
| | | 2.7 | | | | $V_{REF\_OUT}$ = 2.5 v |
| | | 3.2 | | | | $V_{REF\_OUT}$ = 3.0 v |
| $T_s$ | Stable time | | 0.7 | 2 | ms | $C_L$ =4.7 uF, $V_{REF}$ initial=0 |
| | | | 35 | 48 | us | $C_L$ =0.1 uF, $V_{REF}$ initial=0 |

**Note:** Guaranteed by characterization, not tested in production

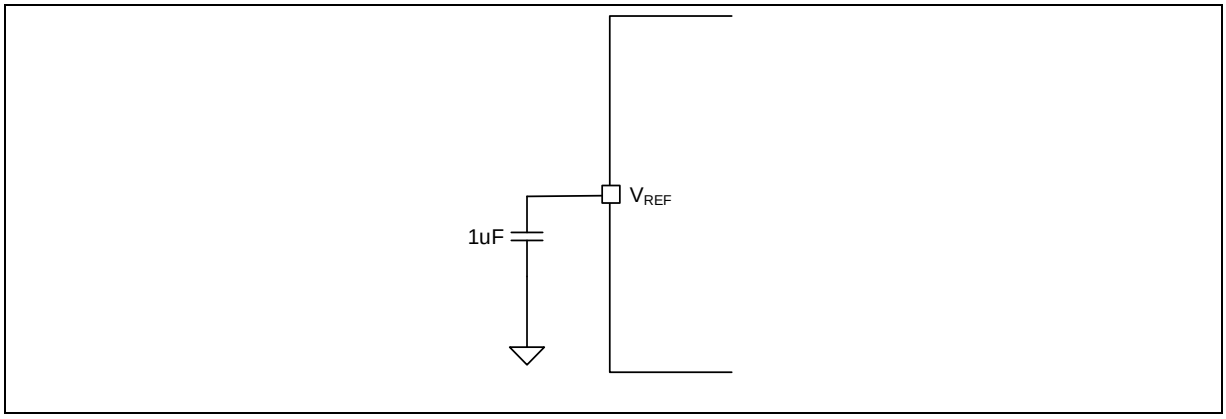



Figure 8.5-2 Typical Connection with Internal Voltage Reference

### 8.5.6 12-bit ADC

*Fast Speed Channel*

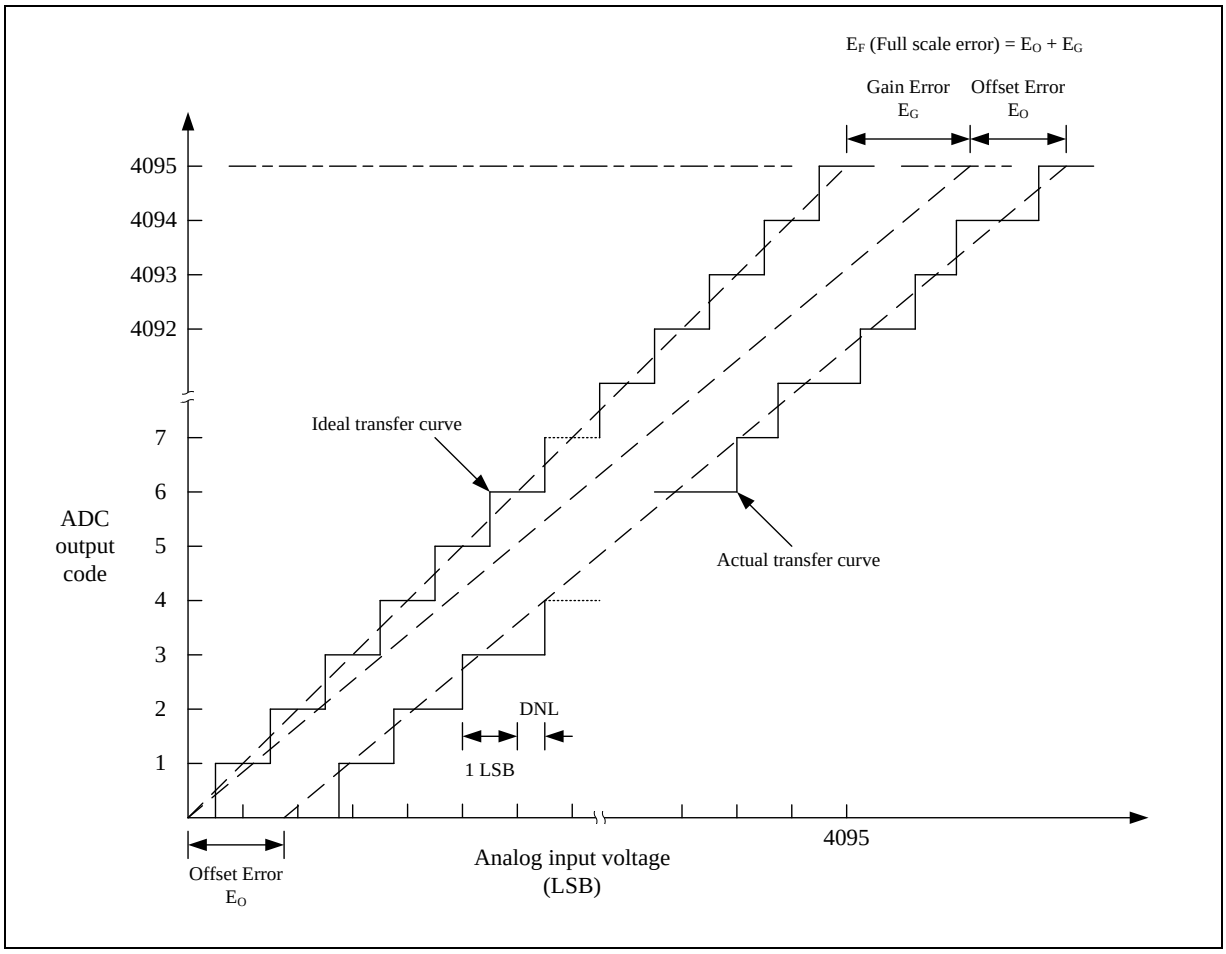
| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $AV_{DD}$ | Operating voltage | 1.8 | | 3.6 | V | $AV_{DD}$ = $V_{DD}$ |
| $V_{REF}$ | Reference voltage | 1.6 | | $AV_{DD}$ | V | |
| $T_A$ | Temperature | -40 | | 105 | ℃ | |
| $I_{ADC}$ | Operating current ($AV_{DD}$ current)<br>(Enable ADC and disable all other analog modules) | 478 | | 523 | uA | $AV_{DD}$ = $V_{DD}$ = $V_{REF}$ = 3.3V<br>ADC Clock Rate = 70 MHz<br>High speed channel |
| | Resolution | | | 12 | Bit | |
| $V_{IN}$ | ADC channel input voltage | 0 | | $V_{REF}$ | V | |
| $F_{ADC}$ | ADC Clock frequency | 0.14 | | 70 | MHz | High speed channel |
| $T_{SMP}$ | Sampling Time | | 2 | | $1/F_{ADC}$ | |
| $T_{CONV}$ | Conversion time | | 14 | | $1/F_{ADC}$ | $T_{CONV}$ = $T_{SMP}$ + 12 |
| $F_{SPS}$ | Sampling Rate ($F_{ADC}/T_{CONV}$) | | | 5 | MSPS | High speed channel |

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $T_{PU}$ | Power-up time | 20 | | | μs | |
| INL | Integral Non-Linearity Error | -4.29 | | -3.71 | LSB | $V_{REF} = AV_{DD}$ |
| DNL | Differential Non-Linearity Error | 3.25 | | 3.28 | LSB | $V_{REF} = AV_{DD}$ |
| $E_G$ | Gain error | 2.25 | | 2.31 | LSB | $V_{REF} = AV_{DD}$ |
| $E_{OFFSET}$ | Offset error | 1.56 | | 2.87 | LSB | $V_{REF} = AV_{DD}$ |
| $E_A$ | Absolute Error | 4.5 | | 4.94 | LSB | $V_{REF} = AV_{DD}$ |
| $C_{IN}$ | Internal Capacitance[*1] | | 5 | | pF | |
| - | Monotonic | Guaranteed | | | - | |

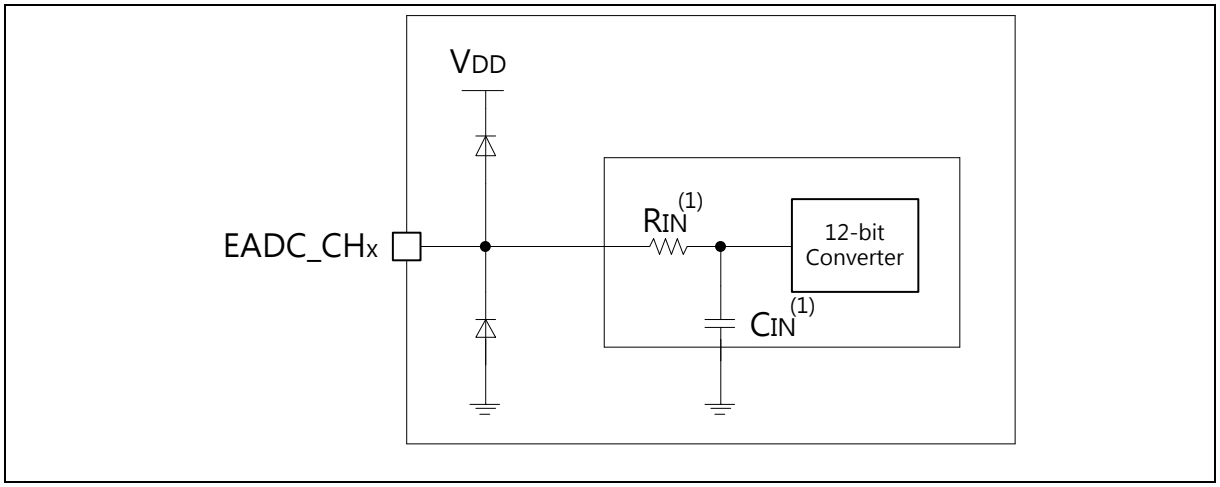
*Low Speed Channel*

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $AV_{DD}$ | Operating voltage | 1.8 | | 3.6 | V | $AV_{DD} = V_{DD}$ |
| $V_{REF}$ | Reference voltage | | $AV_{DD}$ | | V | |
| $T_A$ | Temperature | -40 | | 105 | ℃ | |
| $I_{ADC1}$ | Operating current ($AV_{DD}$ current) (Enable ADC and disable all other analog modules) | 210 | | 231 | uA | $AV_{DD} = V_{DD} = V_{REF}$ = 3.3V<br>ADC Clock Rate = 28 MHz<br>low speed channel |
| | | 131 | | 142 | | $AV_{DD} = V_{DD} = V_{REF}$ = 1.8V<br>ADC Clock Rate = 28 MHz<br>low speed channel |
| $I_{ADC2}$ | | 111 | | 123 | uA | $AV_{DD} = V_{DD} = V_{REF}$ = 3.3V<br>ADC Clock Rate = 14 MHz<br>low speed channel |
| | | 70 | | 78 | | $AV_{DD} = V_{DD} = V_{REF}$ = 1.8V<br>ADC Clock Rate = 14 MHz<br>low speed channel |
| | Resolution | | | 12 | Bit | |
| $V_{IN}$ | ADC channel input voltage | 0 | | $V_{REF}$ | V | |
| $F_{ADC}$ | ADC Clock frequency | 0.14 | | 28 | MHz | Low speed channel |
| $T_{SMP}$ | Sampling Time | | 2 | | $1/F_{ADC}$ | |
| $T_{CONV}$ | Conversion time | | 14 | | $1/F_{ADC}$ | $T_{CONV} = T_{SMP} + 12$ |
| $F_{SPS}$ | Sampling Rate ($F_{ADC}/T_{CONV}$) | | | 2 | MSPS | Low speed channel |
| $T_{PU}$ | Power-up time | 20 | | | μs | |
| INL | Integral Non-Linearity Error | -2.94 | | -1.32 | LSB | $V_{REF} = AV_{DD}$ |
| DNL | Differential Non-Linearity Error | 1.25 | | 2 | LSB | $V_{REF} = AV_{DD}$ |
| $E_G$ | Gain error | 2.5 | | 3.12 | LSB | $V_{REF} = AV_{DD}$ |
| $E_{OFFSET}$ | Offset error | 2.44 | | 3.69 | LSB | $V_{REF} = AV_{DD}$ |

| SYM. | PARAMETER | SPECIFICATIONS | | | | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | UNIT | |
| $E_A$ | Absolute Error | 4.69 | | 6.75 | LSB | $V_{REF} = AV_{DD}$ |
| $C_{IN}$ | Internal Capacitance[*1] | | 5 | | pF | |
| - | Monotonic | Guaranteed | | | - | |




**Note:** The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.




**Note:** GND < EADC_CHx < $V_{REF}$

**(1)** Refer to ADC spec for the values of $R_{IN}$, $C_{IN}$

### 8.5.7 Temperature Sensor

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Operating Voltage | 1.8 | | 3.6 | V |
| $T_A$ | Temperature Range | -40 | | 105 | °C |
| $I_{TEMP}$ | Current Consumption [*3] | | 16 | | µA |
| $T_c$ | Temperature Coefficient [*3] | -1.77 | -1.82 | -1.84 | mV/°C |
| $V_{os}$ | Offset Voltage when $T_A$ = 0°C [*3] | 710.2 | | 716.8 | mV |
| $t_S$ | Stable time[*2] | | 1 | | µs |
| $T_{S\_temp}$ | ADC sampling time when reading the temperature (5pF cap load) [*1] | | 3 | | µs |

**Note:**

1. $V_{TEMP}$ (mV) = $T_c$ (mV/°C) x Temperature (°C) + $V_{os}$ (mV)
2. Guaranteed by design, not tested in production
3. Guaranteed by characteristic, not tested in production

### 8.5.8 Digital to Analog Converter (DAC)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Analog supply voltage | 1.8 | - | 3.6 | V | - |
| $N_R$ | Resolution | | 12 | | bit | - |
| $V_{REF}$ | Reference supply voltage | 1.5 | - | $AV_{DD}$ | V | $V_{REF} \le AV_{DD}$ |
| DNL | Differential non-linearity error[*4] | - | - | ±2 | LSB | 12-bit mode |
| | | - | - | ±0.5 | LSB | 10-bit mode |
| INL | Integral non-linearity error[*4] | - | - | ±4 | LSB | 12-bit mode |
| | | - | - | ±1 | LSB | 10-bit mode |

| | | | | | | |
|---|---|---|---|---|---|---|
| OE | Offset Error[*4] | - | - | ±6 | LSB | 12-bit mode<br>DACOUT buffer ON |
| | | - | - | ±4 | LSB | 12-bit mode<br>DACOUT buffer OFF |
| | | - | - | ±2 | LSB | 10-bit mode |
| GE | Gain Error[*4] | - | - | ±5 | LSB | 12-bit mode<br>DACOUT buffer ON |
| | | - | - | ±4 | LSB | 12-bit mode<br>DACOUT buffer OFF |
| | | - | - | ±2 | LSB | 10-bit mode |
| AE | Absolute Error[*4] | - | - | ±8 | LSB | 12-bit mode<br>DACOUT buffer ON |
| | | - | - | ±4 | LSB | 12-bit mode<br>DACOUT buffer OFF |
| | | - | - | ±2 | LSB | 10-bit mode |
| - | Monotonic | 10-bit guaranteed | | | - | - |
| $V_O$ | Output Voltage | 0.2 | | $AV_{DD}$ - 0.2 | V | DACOUT buffer ON |
| $R_{LOAD}$ | Resistive load[*2] | 7.5 | - | - | kΩ | DACOUT buffer ON |
| Ro | Output impedance[*4] | | 10 | 12 | kΩ | DACOUT buffer OFF |
| $C_{LOAD}$ | Capacitive load[*3] | - | - | 50 | pF | - |
| $I_{AVDD}$ | Current consumption on $AV_{DD}$ supply[*4] | - | - | 180 | µA | $AV_{DD}$ = 3.6V, no load, lowest code (0x000) |
| | | - | - | 420 | | $AV_{DD}$ = 3.6V, no load, middle code (0x800) |
| $I_{REF}$ | Current consumption on $V_{REF}$ supply[*4] | - | 150 | 240 | µA | $V_{REF}$ =3.6V, no load, middle code (0x800) |
| $T_S$ | Settling Time | - | 5 | 6 | µs | Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 7.5k\Omega$ |
| $F_s$ | Update Rate | - | - | 1 | $M_{SPS}$ | Max. frequency for a correct DAC_OUT change from core i to i+1LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 7.5k\Omega$ |
| $T_{WAKEUP}$ | Wake-up Time | - | 9 | 15 | µs | Wakeup time from OFF state. Input code between lowest and highest possible codes.<br>DAC clock source = 1MHz |
| PSRR | Power Supply Rejection Ratio[*1] | - | -60 | -40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50pF |

**Note:**

1. Guaranteed by design, not tested in production.
2. Resistive load between DACOUT and $AV_{SS}$.
3. Capacitive load at DACOUT pin.
4. Guaranteed based on test during characterization.

### 8.5.9 Analog Comparator Controller (ACMP)

- The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Analog supply voltage | 1.8 | | 3.6 | V | |
| $T_A$ | Temperature | -40 | | 105 | ℃ | |
| $I_{DD}$ | Operating current | | 1.2 | | μA | MODESEL[1:0] = 00 |
| | | | 3 | | | MODESEL[1:0] = 01 |
| | | | 10 | | | MODESEL[1:0] = 10 |
| | | | 75 | | | MODESEL[1:0] = 11 |
| $V_{CM}$ | Input common mode voltage range [*2] | 0.1 | 1/2 $AV_{DD}$ | $AV_{DD}$ - 0.1 | | |
| $V_{DI}$ | Differential input voltage sensitivity [*2] | 10 | 20 | | mV | Hysteresis disable |
| $V_{offset}$ | Input offset voltage | | 5 | 10 | mV | Hysteresis disable, |
| $V_{hys}$ | Hysteresis window | | 0 | | mV | HYSSEL[1:0] = 00 |
| | | | 10 | | | HYSSEL[1:0] = 01 |
| | | | 20 | | | HYSSEL[1:0] = 10 |
| | | | 30 | | | HYSSEL[1:0] = 11 |
| $A_v$ | DC voltage Gain[*1] | | 70 | | dB | |
| $T_d$ | Propagation delay[*2] | | | 0.2 | uS | Hysteresis disable MODESEL[1:0] = 00 |
| | | | | 0.6 | | Hysteresis disable MODESEL[1:0] = 01 |
| | | | | 2 | | Hysteresis disable MODESEL[1:0] = 10 |
| | | | | 4.5 | | Hysteresis disable MODESEL[1:0] = 11 |
| $T_{Setup}$ | Setup time[*2] | | | 0.45 | uS | Hysteresis disable MODESEL[1:0] = 00 |
| | | | | 0.85 | | Hysteresis disable MODESEL[1:0] = 01 |
| | | | | 2.25 | | Hysteresis disable MODESEL[1:0] = 10 |
| | | | | 4.75 | | Hysteresis disable MODESEL[1:0] = 11 |

**Note:**

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

### 8.5.10 OP Amplifier (OPA)

- The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$ = 25 ˚C and $V_{DD}$ = 3.3 V unless otherwise specified.

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Analog supply voltage | 2.4 | | 3.6 | V | |
| $T_A$ | Temperature | -40 | | 105 | ℃ | |
| $I_{DD}$ | Consumption current | | 690 | | μA | $A_{VDD}$=3.3V, Temperature=25 ℃ |
| CMIR | Common mode input range | 0 | | $AV_{DD}$ | V | |
| $V_{OFFSET0}$ | Input offset voltage(maximum calibration range) [*2] | | | 4 | mV | Tj = 25°C, No Load |
| | | | | 6 | | $V_{CM}$ = $AV_{DD}$-10mV ~ $AV_{DD}$-0.8V, All Temp. |
| $V_{OFFSET1}$ | Input offset voltage(After offset calibration) [*2] | | | 3.2 | | CALRVS =0: Other $V_{CM}$ |
| | | | | 6.5 | | CALRVS=0: $V_{CM}$ = $AV_{DD}$-10mV ~ $AV_{DD}$-0.8V |
| $V_{OFFSET2}$ | Input offset voltage(After offset calibration) [*2] | | | 3 | | CALRVS =1: Other VCM |
| | | | | 5.2 | | CALRVS =1: $V_{CM}$ = $AV_{DD}$-10mV ~ $AV_{DD}$-0.8V |
| CMRR | Common Mode Rejection Ratio [*1] | | 90 | | dB | |
| PSRR | Power Supply Rejection Ratio [*1] | 73 | 117 | | dB | |
| GBW | Bandwidth [*2] | | 8.2 | | MHz | |
| SR | Slew rate [*2] | | 4.7 | | V/μs | |
| $V_{OHSAT}$ | High saturation voltage [*2] | $AV_{DD}$-0.1 | | | V | Rload=min. INPUT at $AV_{DD}$ |
| | | $AV_{DD}$-0.02 | | | | Rload=20K, INPUT at $AV_{DD}$ |
| $V_{OLSAT}$ | Low saturation voltage [*2] | | | 100 | mV | Rload=min. INPUT at 0 |
| | | | | 20 | | Rload=20K, INPUT at 0 |
| PM | Phase Margin [*1] | | 62 | | degree | |
| $T_{WAKEUP}$ | Wake up time from OFF state [*2] | | 2.8 | 5 | μs | |
| $R_{LOAD}$ | Resistive load | 4 | | | kΩ | |
| $C_{LOAD}$ | Capacitive load | | | 50 | pF | |

**Note:**

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

## 8.6 Flash DC Electrical Characteristic

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{FLA}$[1] | Supply Voltage | 1.08 | | 1.32 | V | $T_A$ = 25℃ |
| $N_{ENDUR}$ | Endurance | 10000 | - | - | cycles[2] | |
| $T_{RET}$ | Data Retention | 10 | - | - | year | |
| $T_{ERASE}$ | Page Erase Time | 92 | - | 160 | mS | |
| $T_{MER}$ | Mass Erase Time | 201 | - | 320 | mS | |
| $T_{PROG}$ | Program Time | 42 | - | 50 | uS | |
| $I_{DD1}$ | Read Current | - | - | 4.12 | mA | |
| $I_{DD2}$ | Program Current | - | - | 5 | mA | |
| $I_{DD3}$ | Erase Current | - | - | 5 | uA | |

**Note:**

1. $V_{FLA}$ is source from chip LDO output voltage.
2. Number of program/erase cycles.
3. This table is guaranteed by design, not test in production.

## 8.7 I²C Dynamic Characteristics

| Symbol | Parameter | Standard Mode[1][2] | | Fast Mode[1][2] | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{LOW}$ | SCL low period | 4.7 | - | 1.2 | - | uS |
| $t_{HIGH}$ | SCL high period | 4 | - | 0.6 | - | uS |
| $t_{SU;\ STA}$ | Repeated START condition setup time | 4.7 | - | 1.2 | - | uS |
| $t_{HD;\ STA}$ | START condition hold time | 4 | - | 0.6 | - | uS |
| $t_{SU;\ STO}$ | STOP condition setup time | 4 | - | 0.6 | - | uS |
| $t_{BUF}$ | Bus free time | 4.7[3] | - | 1.2[3] | - | uS |
| $t_{SU;DAT}$ | Data setup time | 250 | - | 100 | - | nS |
| $t_{HD;DAT}$ | Data hold time | 0[4] | 3.45[5] | 0[4] | 0.8[5] | uS |
| $t_r$ | SCL/SDA rise time | - | 1000 | 20+0.1$C_b$ | 300 | nS |
| $t_f$ | SCL/SDA fall time | - | 300 | - | 300 | nS |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

**Note:**

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

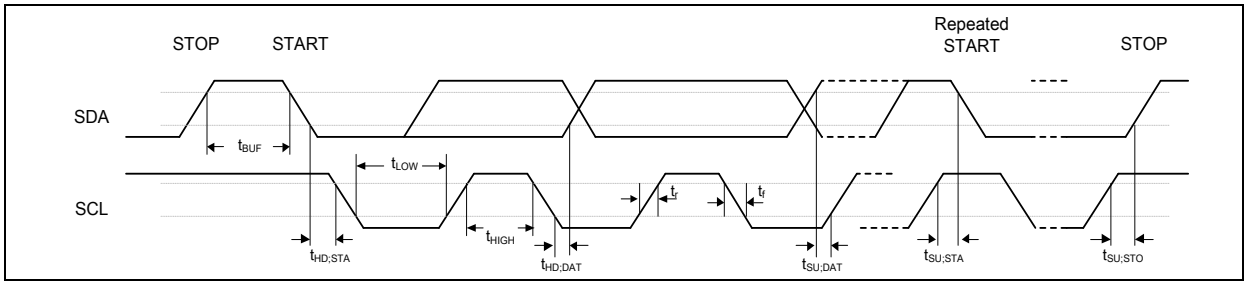



Figure 8.7-1 I²C Timing Diagram

## 8.8 SPI Dynamic Characteristics

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **SPI MASTER MODE ($V_{DD}$ = 3.0~3.6 V, 30 PF LOADING CAPACITOR)** | | | | | |
| $t_{CLKH}$ | Clock output High time [*1] | | | $T_{SPICLK}$ / 2 | ns |
| $t_{CLKL}$ | Clock output Low time [*1] | | | $T_{SPICLK}$ / 2 | ns |
| $t_{DS}$ | Data setup time | 0 | - | - | ns |
| $t_{DH}$ | Data hold time | 2 | - | - | ns |
| $t_V$ | Data output valid time | - | 0 | 1 | ns |
| **SPI MASTER MODE ($V_{DD}$ = 1.8~2.0 V, 30 PF LOADING CAPACITOR)** | | | | | |
| $t_{CLKH}$ | Clock output High time [*1] | | | $T_{SPICLK}$ / 2 | ns |
| $t_{CLKL}$ | Clock output Low time [*1] | | | $T_{SPICLK}$ / 2 | ns |
| $t_{DS}$ | Data setup time | 0 | - | - | ns |
| $t_{DH}$ | Data hold time | 2 | - | - | ns |
| $t_V$ | Data output valid time | - | - | 1 | ns |

**Note:** The minimum clock period for SPICLK is 10.4 ns (96 MHz).

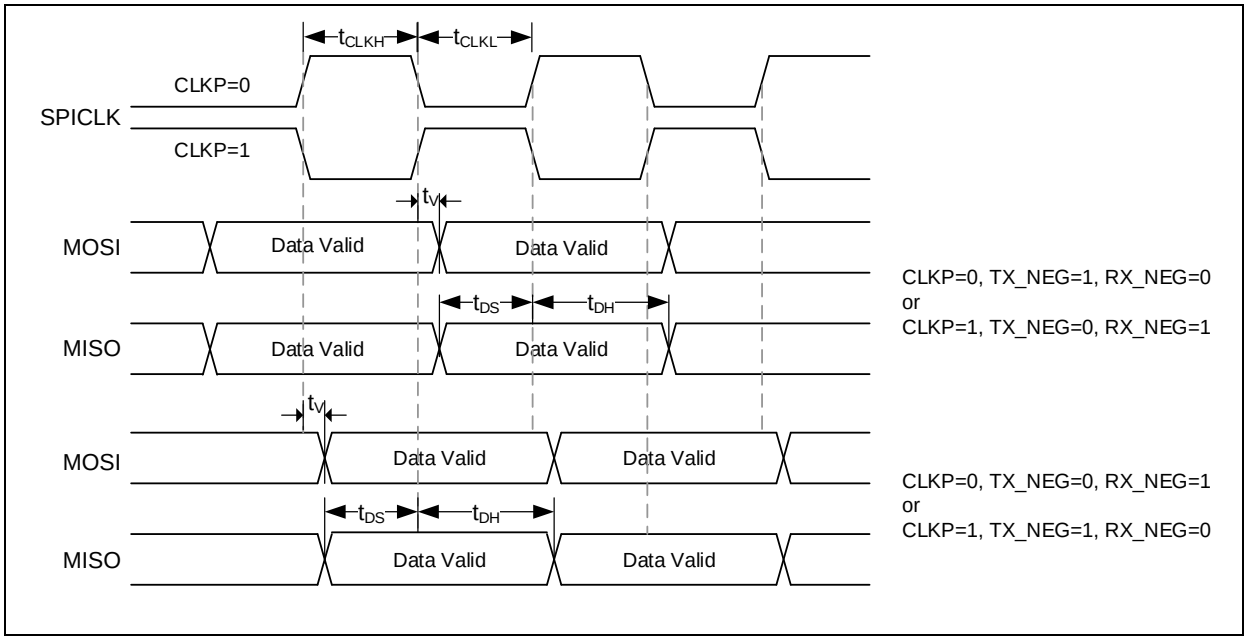



Figure 8.8-1 SPI Master Mode Timing Diagram

| SYMBOL | PARAMETER | MIN. | YP. | MAX. | UNIT |
|---|---|---|---|---|---|

| SPI SLAVE MODE ($V_{DD}$ = 3.0~3.6V, 30 PF LOADING CAPACITOR) | | | | | |
|---|---|---|---|---|---|
| $t_{CLKH}$ | Clock output High time [*1] | - | - | $T_{SPICLK}$ / 2 | ns |
| $t_{CLKL}$ | Clock output Low time [*1] | - | | $T_{SPICLK}$ / 2 | ns |
| $t_{SS}$ | Slave select setup time | 1 $T_{SPICLK}$ + 2ns | - | - | ns |
| $t_{SH}$ | Slave select hold time | 1 $T_{SPICLK}$ | - | - | ns |
| $t_{DS}$ | Data input setup time | 0 | - | - | ns |
| $t_{DH}$ | Data input hold time | 2 | - | - | ns |
| $t_V$ | Data output valid time | - | | 8 | ns |
| $t_{CLKH}$ | Clock output High time [*1] | - | - | $T_{SPICLK}$ / 2 | ns |
| SPI SLAVE MODE ($V_{DD}$ = 1.8 V ~ 2.0 V, 30 PF LOADING CAPACITOR) | | | | | |
| $t_{CLKH}$ | Clock output High time [*1] | - | - | $T_{SPICLK}$ / 2 | ns |
| $t_{CLKL}$ | Clock output Low time [*1] | - | - | $T_{SPICLK}$ / 2 | ns |
| $t_{SS}$ | Slave select setup time | 1 $T_{SPICLK}$ + 3ns | - | - | ns |
| $t_{SH}$ | Slave select hold time | 1 $T_{SPICLK}$ | - | - | ns |
| $t_{DS}$ | Data input setup time | 0 | - | - | ns |
| $t_{DH}$ | Data input hold time | 2 | - | - | ns |
| $t_V$ | Data output valid time | - | | 10 | ns |

**Note:** The minimum clock period for SPICLK is 10.4 ns (96 MHz).

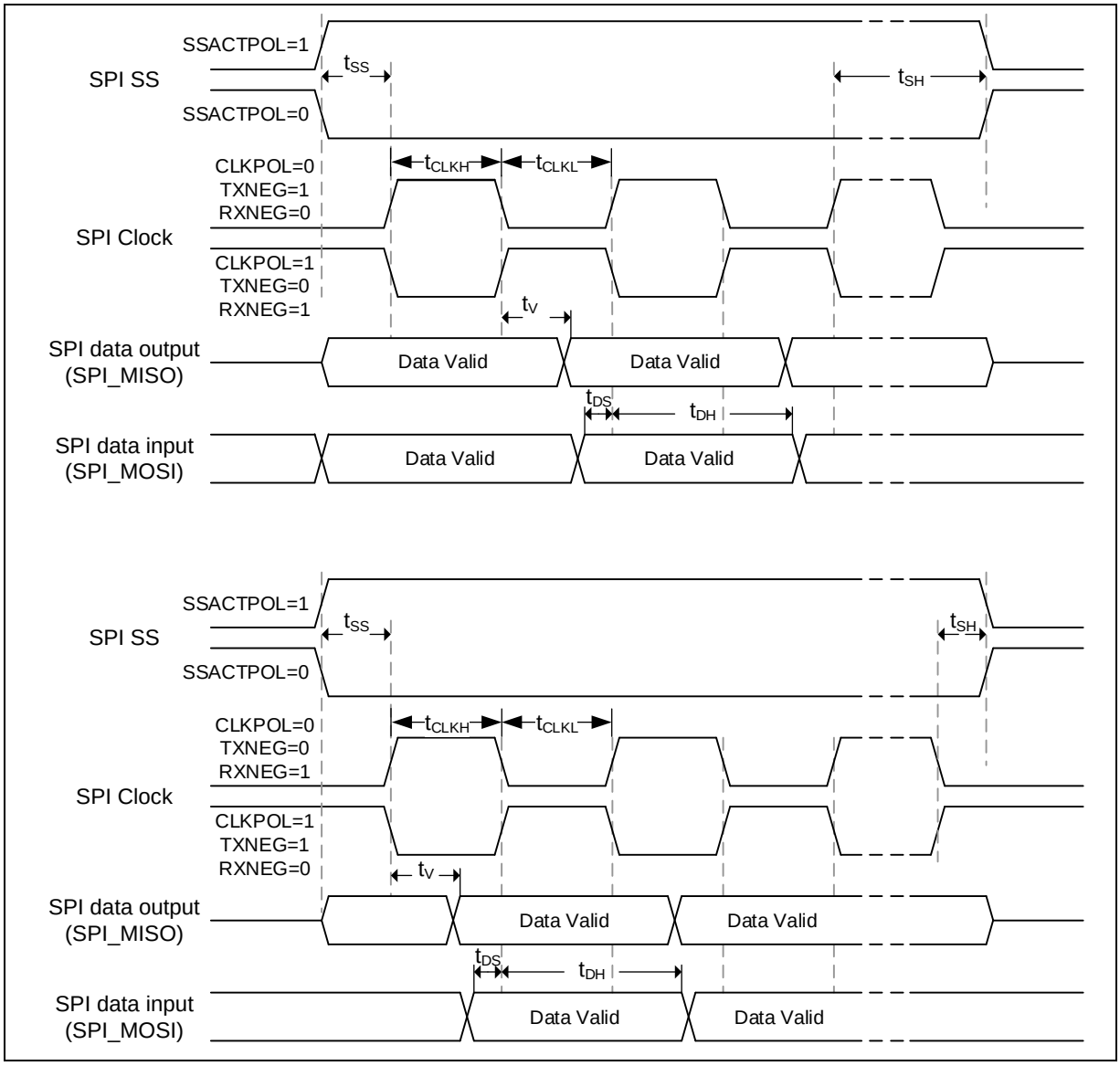



Figure 8.8-2 SPI Slave Mode Timing Diagram

## 8.9 I²S Dynamic Characteristics

| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $t_{w(CKH)}$ | I²S clock high time | 40 | - | ns | Master $f_{PCLK}$ = MHz, data: 24 bits, audio frequency = 256 kHz |
| $t_{w(CKL)}$ | I²S clock low time | 40 | - | | |
| $t_{v(WS)}$ | WS valid time | 4 | 16 | | Master mode |
| $t_{h(WS)}$ | WS hold time | 1 | - | | Master mode |
| $t_{su(WS)}$ | WS setup time | 24 | - | | Slave mode |
| $t_{h(WS)}$ | WS hold time | 0 | - | | Slave mode |
| $DuCy_{(SCK)}$ | I²S slave input clock duty cycle | 30 | 70 | % | Slave mode |
| $t_{su(SD\_MR)}$ | Data input setup time | 10 | - | ns | Master receiver |
| $t_{su(SD\_SR)}$ | | 7 | - | | Slave receiver |
| $t_{h(SD\_MR)}$ | Data input hold time | 7 | - | | Master receiver |
| $t_{h(SD\_SR)}$ | | 4 | - | | Slave receiver |
| $t_{v(SD\_ST)}$ | Data output valid time | - | 10 | | Slave transmitter (after enable edge) |
| $t_{h(SD\_ST)}$ | Data output hold time | 4 | - | | Slave transmitter (after enable edge) |
| $t_{v(SD\_MT)}$ | Data output valid time | - | 4 | | Master transmitter (after enable edge) |
| $t_{h(SD\_MT)}$ | Data output hold time | 0 | - | | Master transmitter (after enable edge) |

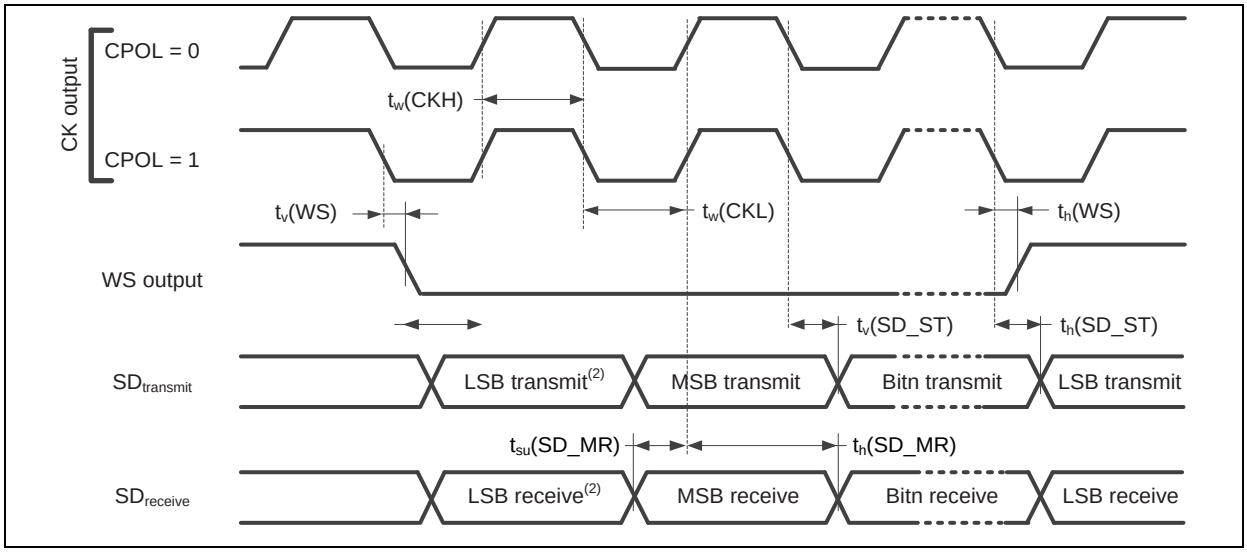



Figure 8.9-1 I²S Master Mode Timing Diagram

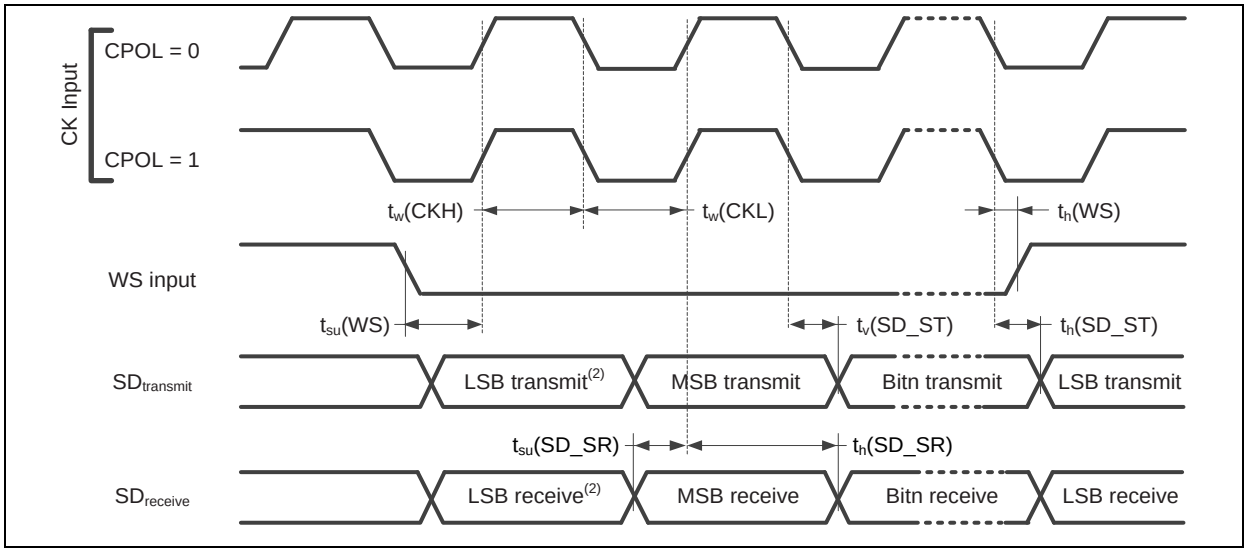



Figure 8.9-2 I²S Slave Mode Timing Diagram

## 8.10 USCI - I²C Dynamic Characteristics

| Symbol | Parameter | Standard Mode[1][2] | | Fast Mode[1][2] | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{LOW}$ | SCL low period | 4.7 | - | 1.2 | - | uS |
| $t_{HIGH}$ | SCL high period | 4 | - | 0.6 | - | uS |
| $t_{SU;\ STA}$ | Repeated START condition setup time | 4.7 | - | 1.2 | - | uS |
| $t_{HD;\ STA}$ | START condition hold time | 4 | - | 0.6 | - | uS |
| $t_{SU;\ STO}$ | STOP condition setup time | 4 | - | 0.6 | - | uS |
| $t_{BUF}$ | Bus free time | 4.7[3] | - | 1.2[3] | - | uS |
| $t_{SU;DAT}$ | Data setup time | 250 | - | 100 | - | nS |
| $t_{HD;DAT}$ | Data hold time | 0[4] | 3.45[5] | 0[4] | 0.8[5] | uS |
| $t_r$ | SCL/SDA rise time | - | 1000 | 20+0.1$C_b$ | 300 | nS |
| $t_f$ | SCL/SDA fall time | - | 300 | - | 300 | nS |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

**Note:**

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

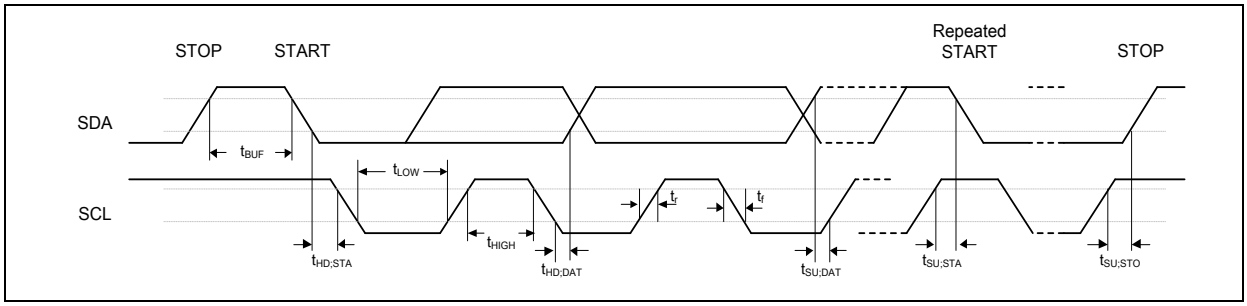



Figure 8.10-1 I²C Timing Diagram

## 8.11 USCI - SPI Dynamic Characteristics

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **SPI MASTER MODE ($V_{DD}$ = 3.0~3.6 V, 30 PF LOADING CAPACITOR)** | | | | | |
| $t_{CLKH}$ | Clock output High time [*1] | | | $T_{SPICLK}$ / 2 | ns |
| $t_{CLKL}$ | Clock output Low time [*1] | | | $T_{SPICLK}$ / 2 | ns |
| $t_{DS}$ | Data setup time | 0 | - | - | ns |
| $t_{DH}$ | Data hold time | 2 | - | - | ns |
| $t_V$ | Data output valid time | - | 0 | 1 | ns |
| **SPI MASTER MODE ($V_{DD}$ = 1.8~2.0 V, 30 PF LOADING CAPACITOR)** | | | | | |
| $t_{CLKH}$ | Clock output High time [*1] | | | $T_{SPICLK}$ / 2 | ns |
| $t_{CLKL}$ | Clock output Low time [*1] | | | $T_{SPICLK}$ / 2 | ns |
| $t_{DS}$ | Data setup time | 0 | - | - | ns |
| $t_{DH}$ | Data hold time | 2 | - | - | ns |
| $t_V$ | Data output valid time | - | - | 1 | ns |

**Note:** The minimum clock period for SPICLK is 10.4 ns (96 MHz).

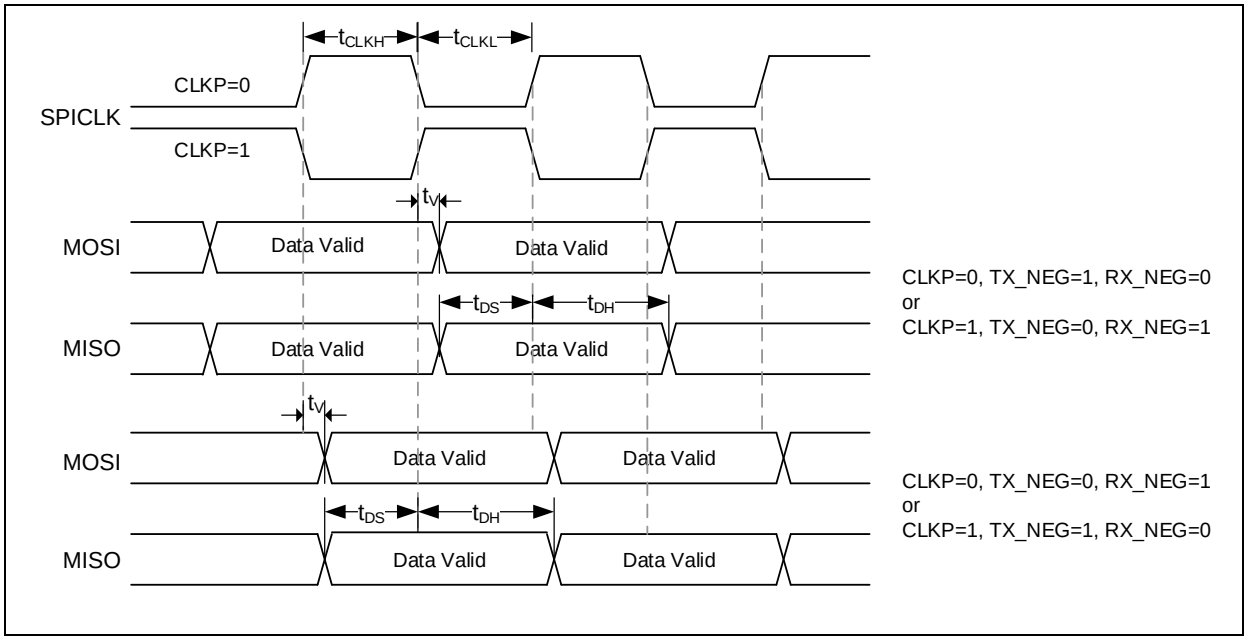



Figure 8.11-1 SPI Master Mode Timing Diagram

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **SPI SLAVE MODE ($V_{DD}$ = 3.0~3.6V, 30 PF LOADING CAPACITOR)** | | | | | |

| | | | | | |
|---|---|---|---|---|---|
| $t_{CLKH}$ | Clock output High time [*1] | - | - | $T_{SPICLK}$ / 2 | ns |
| $t_{CLKL}$ | Clock output Low time [*1] | - | | $T_{SPICLK}$ / 2 | ns |
| $t_{SS}$ | Slave select setup time | 1 $T_{SPICLK}$ + 2ns | - | - | ns |
| $t_{SH}$ | Slave select hold time | 1 $T_{SPICLK}$ | - | - | ns |
| $t_{DS}$ | Data input setup time | 0 | - | - | ns |
| $t_{DH}$ | Data input hold time | 2 | - | - | ns |
| $t_V$ | Data output valid time | - | | 8 | ns |
| $t_{CLKH}$ | Clock output High time [*1] | - | - | $T_{SPICLK}$ / 2 | ns |
| **SPI SLAVE MODE ($V_{DD}$ = 1.8 V ~ 2.0 V, 30 PF LOADING CAPACITOR)** | | | | | |
| $t_{CLKH}$ | Clock output High time [*1] | - | - | $T_{SPICLK}$ / 2 | ns |
| $t_{CLKL}$ | Clock output Low time [*1] | - | - | $T_{SPICLK}$ / 2 | ns |
| $t_{SS}$ | Slave select setup time | 1 $T_{SPICLK}$ + 3ns | - | - | ns |
| $t_{SH}$ | Slave select hold time | 1 $T_{SPICLK}$ | - | - | ns |
| $t_{DS}$ | Data input setup time | 0 | - | - | ns |
| $t_{DH}$ | Data input hold time | 2 | - | - | ns |
| $t_V$ | Data output valid time | - | | 10 | ns |

**Note:** The minimum clock period for SPICLK is 10.4 ns (96 MHz).

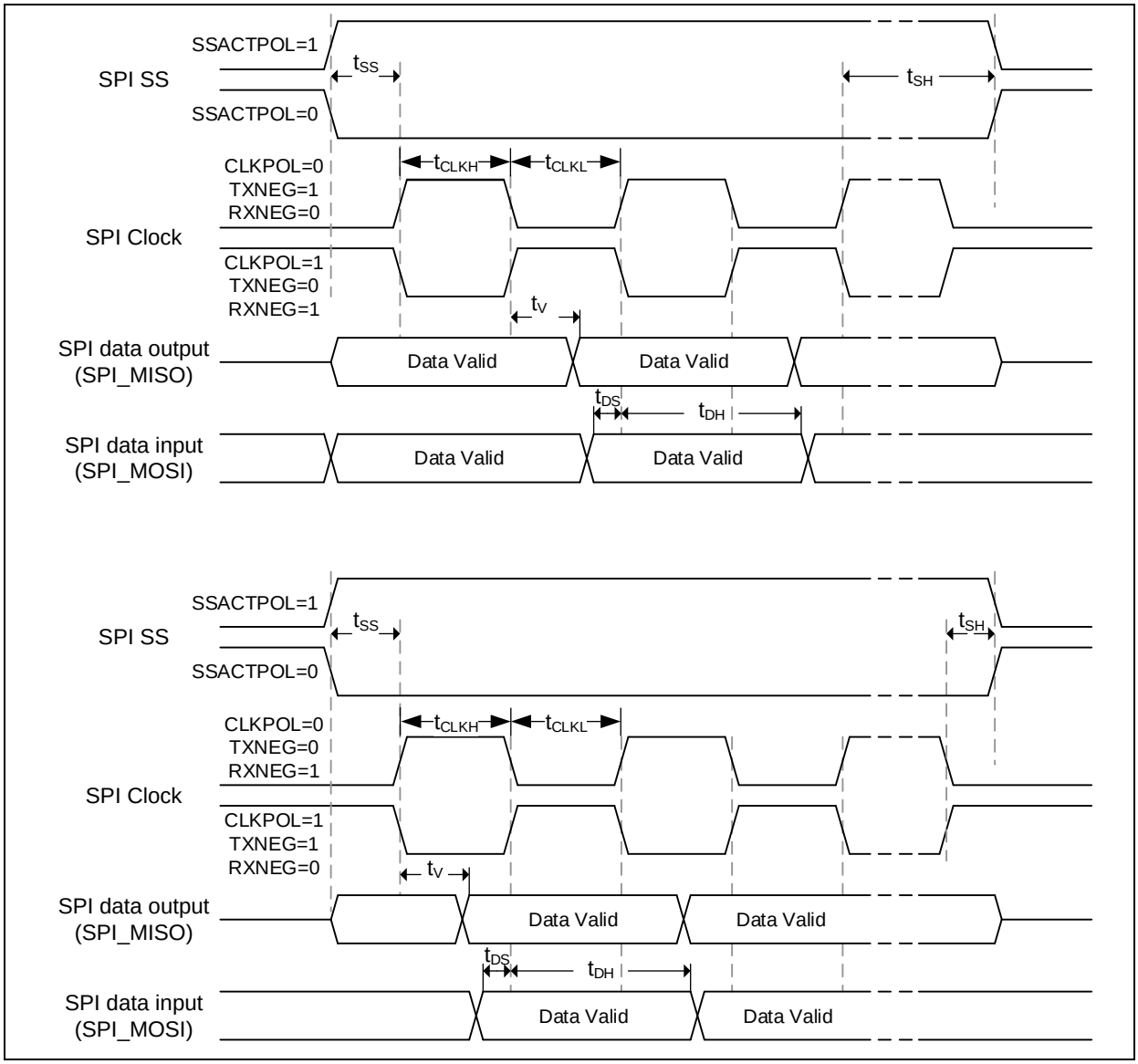



Figure 8.11-2 SPI Slave Mode Timing Diagram

## 8.12 USB Characteristics

### 8.12.1 USB Full-Speed

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High (driven) | 2.0 | - | - | V | - |
| $V_{IL}$ | Input Low | - | - | 0.8 | V | - |
| $V_{DI}$ | Differential Input Sensitivity | 0.2 | - | - | V | \|PADP-PADM\| |
| $V_{CM}$ | Differential Common-mode Range | 0.8 | - | 2.5 | V | Includes $V_{DI}$ range |
| $V_{SE}$ | Single-ended Receiver Threshold | 0.8 | - | 2.0 | V | - |
| | Receiver Hysteresis | - | 200 | - | mV | - |
| $V_{OL}$ | Output Low (driven) | 0 | - | 0.3 | V | - |
| $V_{OH}$ | Output High (driven) | 2.8 | - | 3.6 | V | - |
| $V_{CRS}$ | Output Signal Cross Voltage | 1.3 | - | 2.0 | V | - |
| $R_{PU}$ | Pull-up Resistor | 1.425 | - | 1.575 | kΩ | - |
| $R_{PD}$ | Pull-down Resistor | 14.25 | - | 15.75 | kΩ | |
| $V_{TRM}$ | TERMINATION Voltage for Uptream port pull up (RPU) | 3.0 | - | 3.6 | V | |
| $Z_{DRV}$ | Driver Output Resistance | - | 13 | - | Ω | Steady state drive* |
| $C_{IN}$ | Transceiver Capacitance | - | - | 20 | pF | Pin to GND |

### 8.12.2 USB Full-Speed PHY characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $T_{FR}$ | Rise Time | 4 | - | 20 | ns | $C_L$=50p |
| $T_{FF}$ | Fall Time | 4 | - | 20 | ns | $C_L$=50p |
| $T_{FRFF}$ | Rise and Fall Time Matching | 90 | - | 111.11 | % | $T_{FRFF}=T_{FR}/T_{FF}$ |

### 8.12.3 USB High-Speed characteristics

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_{FR}$ | High Speed Driver Rise Time | 500 | - | | ps | CL=5pF |
| $T_{FF}$ | High Speed Driver Fall Time | 500 | - | | ps | CL=5pF |
| $T_{FRFF}$ | Rise and Fall Time Matching | 90 | | 111.11 | % | $T_{FRFF}=T_{FR}/T_{FF}$ |

## 8.13 Ethernet Characteristics

### 8.13.1 RMII Interface Timing

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_{P\_RMII\_REFCLK}$ | RMII_REFCLK Period | - | 20.0 +/- 50 ppm | - | ns | - |
| $T_{H\_RMII\_REFCLK}$ | RMII_REFCLK High Time | 8.0 | 10.0 | 12.0 | ns | - |
| $T_{L\_RMII\_REFCLK}$ | RMII_REFCLK Low Time | 8.0 | 10.0 | 12.0 | ns | - |
| $T_{DLY\_RMII\_TX}$ | RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay | - | - | 10 | ns | - |
| $T_{SU\_RMII\_RX}$ | RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising | 5 | - | - | ns | - |
| $T_{HD\_RMII\_RX}$ | RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising | 2 | - | - | ns | - |

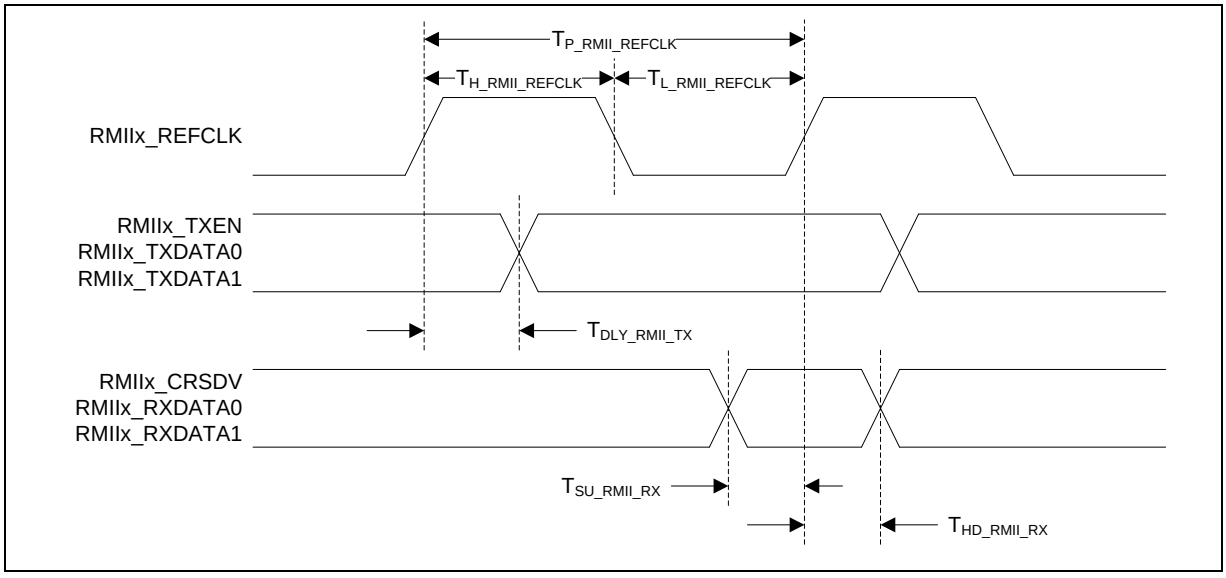



Figure 8.13-1 RMII Interface Timing Diagram

### 8.13.2 Ethernet PHY Management Interface Timing

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_{P\_RMII\_MDC}$ | RMII_MDC Period | 400 | - | - | ns | - |
| $T_{H\_RMII\_MDC}$ | RMII_MDC High Time | 200 | - | - | ns | - |
| $T_{L\_RMII\_MDC}$ | RMII_MDC Low Time | 200 | - | - | ns | - |
| $T_{DLY\_RMII\_MDIOWR}$ | RMII_MDC Falling to Valid RMII_MDIO Delay | - | - | 10 | ns | - |

| | | | | | | |
|---|---|---|---|---|---|---|
| $T_{SU\_RMII\_MDIORD}$ | RMII_MDIO Setup Time to RMII_MDC Rising | 10 | - | - | ns | - |
| $T_{HD\_RMII\_MDIORD}$ | RMII_MDIO Hold Time from RMII_MDC Rising | 10 | - | - | ns | - |

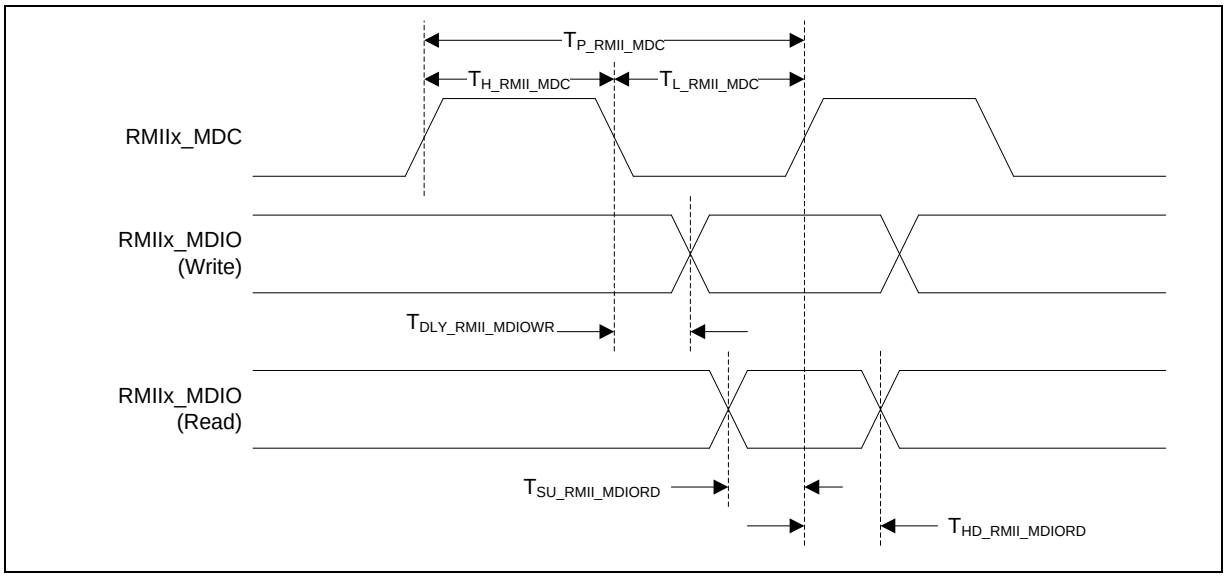



Figure 8.13-2 Ethernet PHY Management Interface Timing Diagram

## 8.14 SDIO Characteristics

### 8.14.1 Default Mode Timing

| 在嗎 | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_{P\_SD\_CLK}$ | SD_CLK Period (Data Transfer Mode) | 40 | - | - | ns | - |
| $T_{P\_SD\_CLK\_ID}$ | SD_CLK Period (Identification Mode) | 2,500 | - | - | ns | |
| $T_{H\_SD\_CLK}$ | SD_CLK High Time | - | 20 | - | ns | - |
| $T_{L\_SD\_CLK}$ | SD_CLK Low Time | - | 20 | - | ns | - |
| $T_{SU\_SD\_IN}$ | SD_DATA Setup Time to SD_CLK Rising | 5 | - | - | ns | - |
| $T_{HD\_SD\_IN}$ | SD_DATA Hold Time from SD_CLK Rising | 5 | - | - | ns | - |
| $T_{DLY\_SD\_OUT}$ | SD_CLK Falling to Valid SD_DATA Delay | - | - | 14 | ns | - |

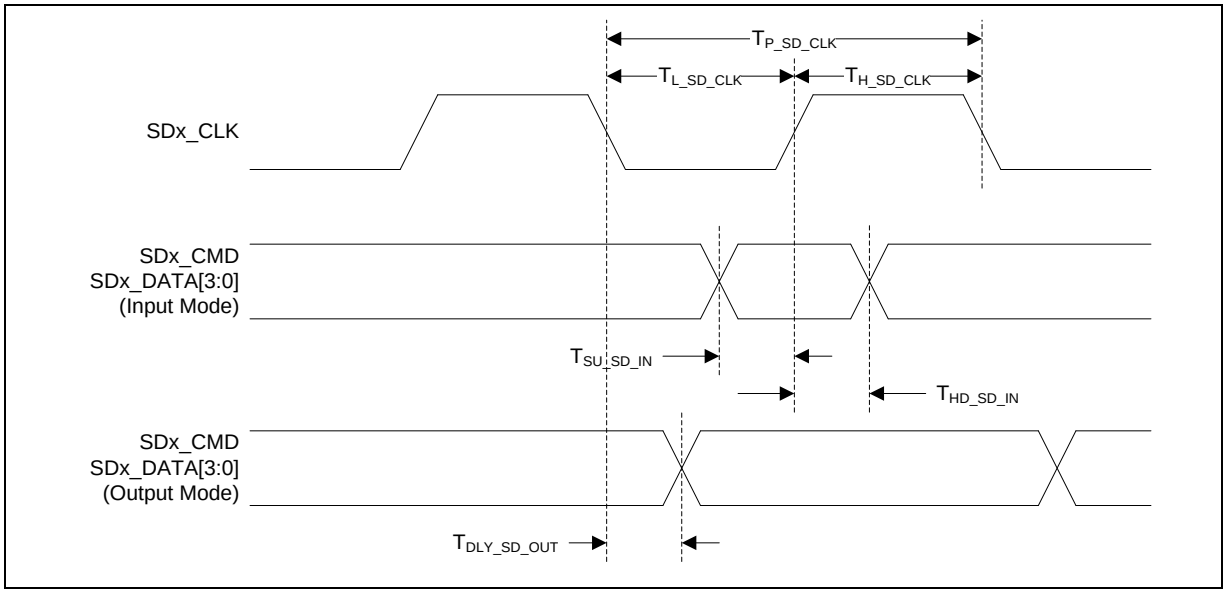



Figure 8.14-1 SDIO Default Mode

### 8.14.2 SDIO Dynamic characteristics

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_{P\_SD\_CLK}$ | SD_CLK Period | 20 | - | - | ns | - |
| $T_{H\_SD\_CLK}$ | SD_CLK High Time | 7 | - | - | ns | - |
| $T_{L\_SD\_CLK}$ | SD_CLK Low Time | 7 | - | - | ns | - |

| | | | | | | |
|---|---|---|---|---|---|---|
| $T_{SU\_SD\_IN}$ | SD_DATA Setup Time to SD_CLK Rising | 6 | - | - | ns | - |
| $T_{HD\_SD\_IN}$ | SD_DATA Hold Time from SD_CLK Rising | 2 | - | - | ns | - |
| $T_{DLY\_SD\_OUT}$ | SD_CLK Falling to Valid SD_DATA Delay | - | - | 14 | ns | - |
| $T_{HD\_SD\_OUT}$ | SD_DATA Hold Time from SD_CLK Rising | 2.5 | - | - | ns | - |

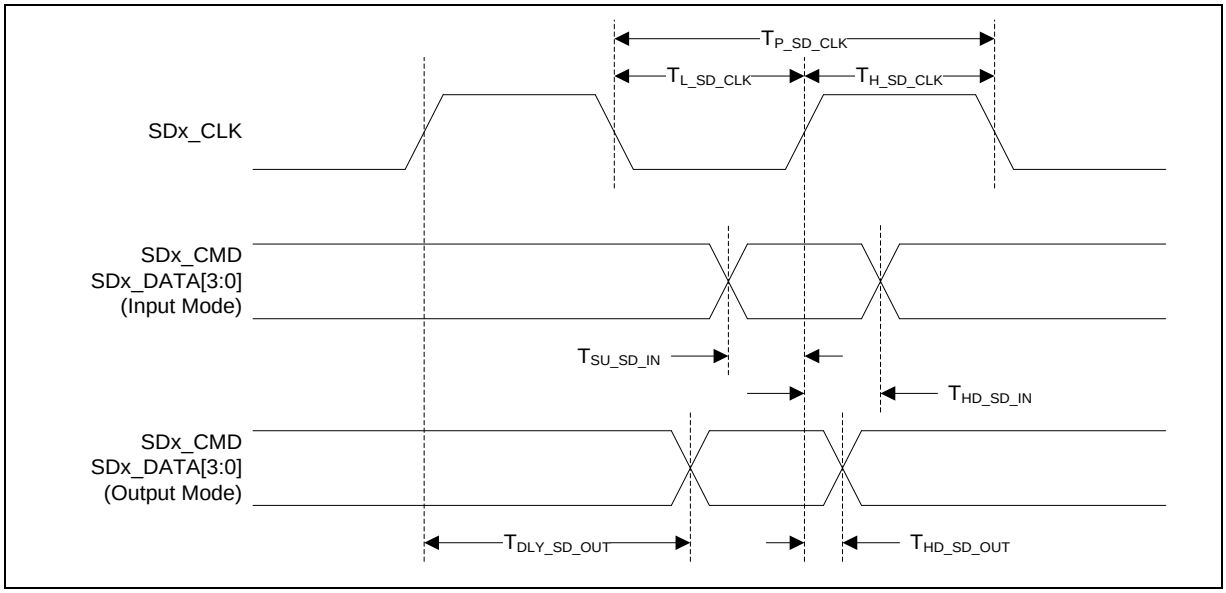
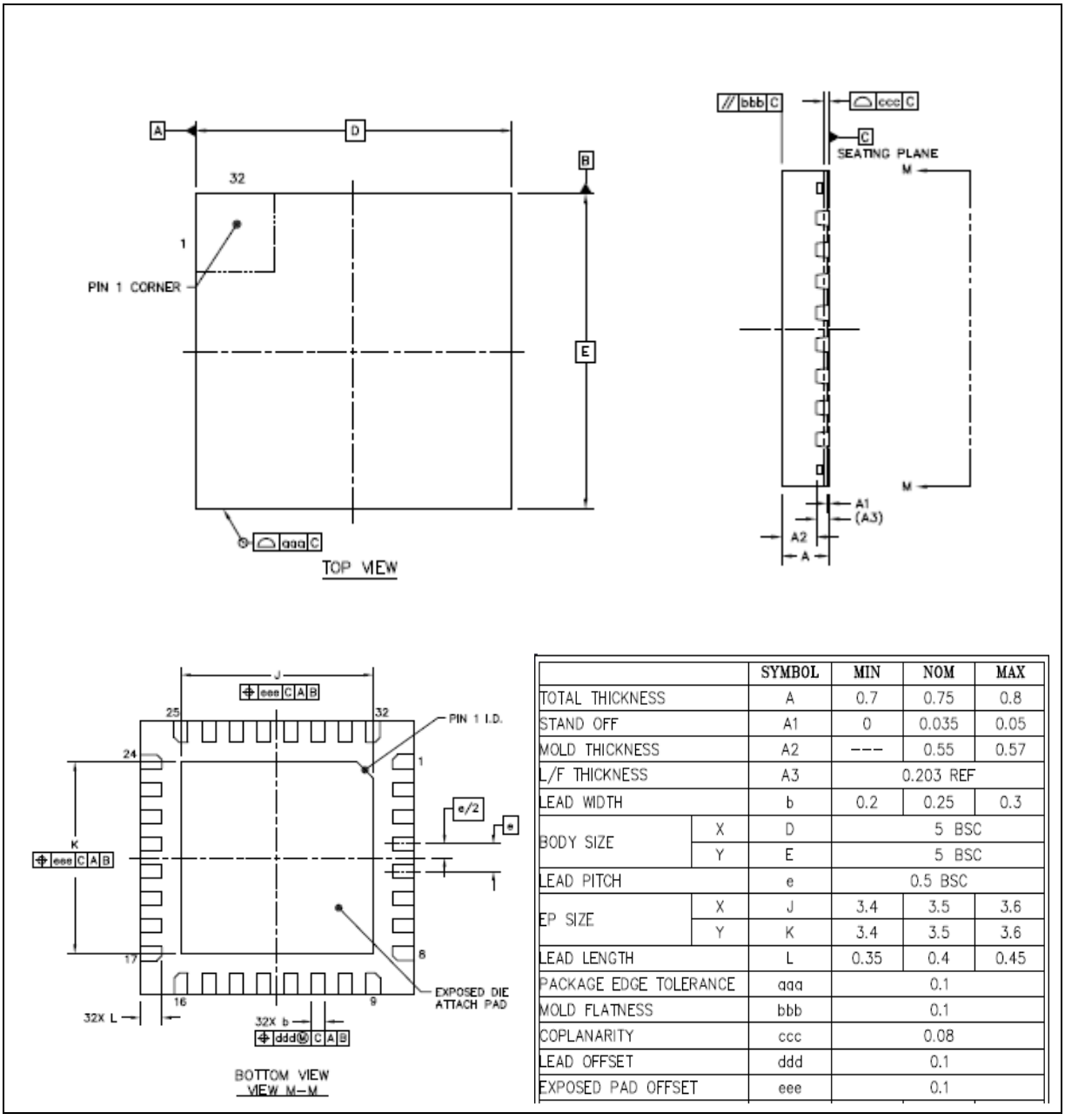



Figure 8.14-2 SDIO High-speed Mode

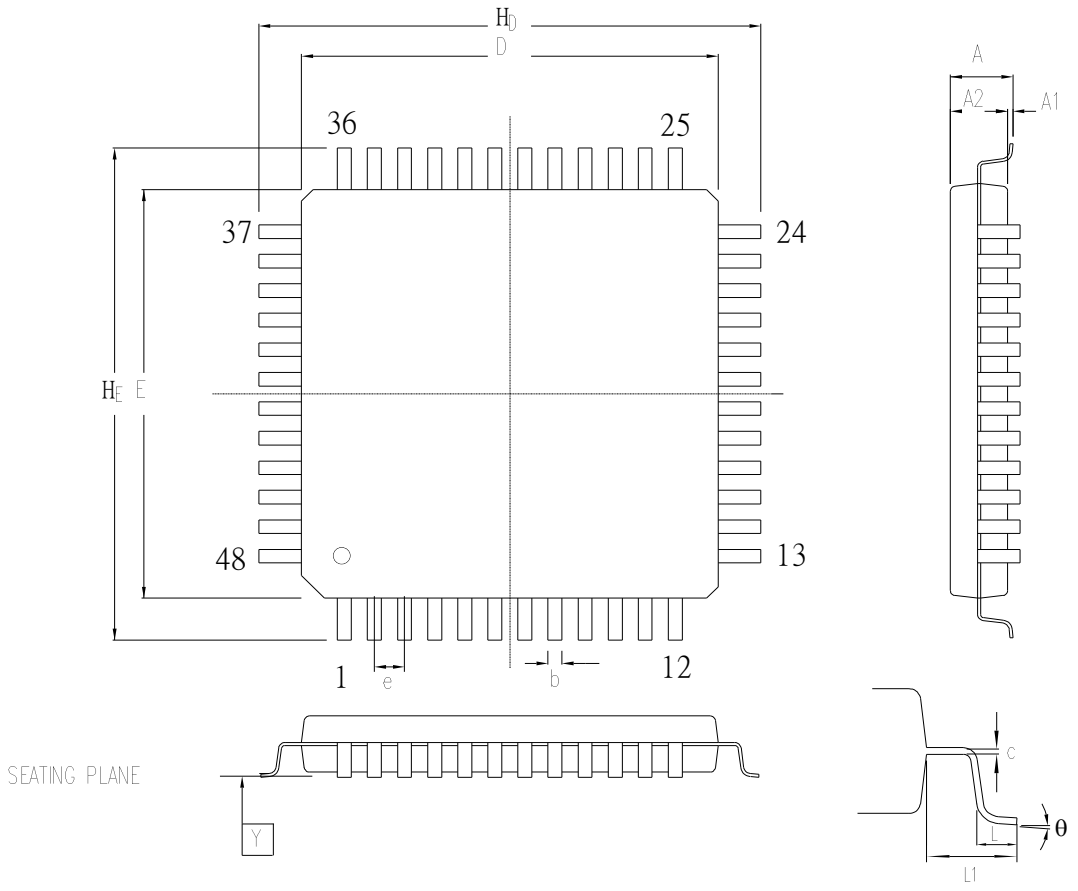
# 9 PACKAGE OUTLINE DRAWING

## 9.1 QFN 33L (5x5x0.8 mm$^3$ Pitch 0.5 mm)




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.7 | 0.75 | 0.8 |
| STAND OFF | | A1 | 0 | 0.035 | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.55 | 0.57 |
| L/F THICKNESS | | A3 | | 0.203 REF | |
| LEAD WIDTH | | b | 0.2 | 0.25 | 0.3 |
| BODY SIZE | X | D | | 5 BSC | |
| | Y | E | | 5 BSC | |
| LEAD PITCH | | e | | 0.5 BSC | |
| EP SIZE | X | J | 3.4 | 3.5 | 3.6 |
| | Y | K | 3.4 | 3.5 | 3.6 |
| LEAD LENGTH | | L | 0.35 | 0.4 | 0.45 |
| PACKAGE EDGE TOLERANCE | | aaa | | 0.1 | |
| MOLD FLATNESS | | bbb | | 0.1 | |
| COPLANARITY | | ccc | | 0.08 | |
| LEAD OFFSET | | ddd | | 0.1 | |
| EXPOSED PAD OFFSET | | eee | | 0.1 | |

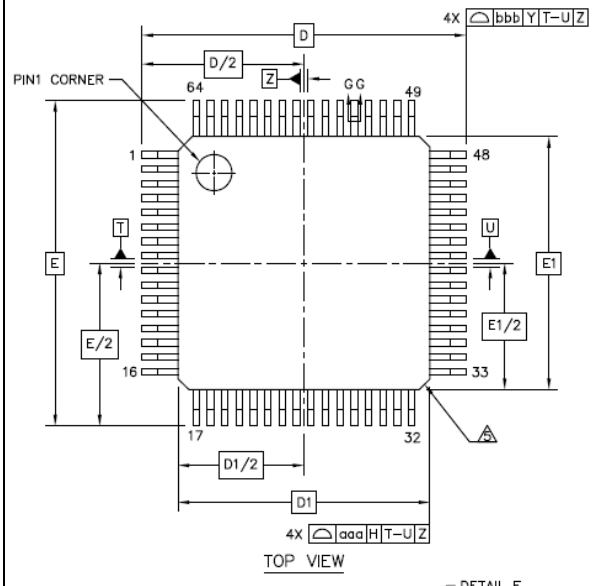
## 9.2 LQFP 48L (7x7x1.4 mm$^3$ Footprint 2.0mm)



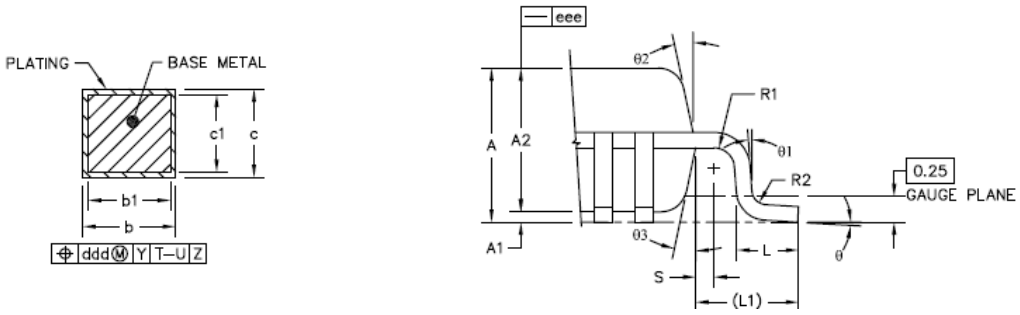

Controlling dimension : Millimeters

| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | — | — | — | — |
| $A_1$ | 0.002 | 0.004 | 0.006 | 0.05 | 0.10 | 0.15 |
| $A_2$ | 0.053 | 0.055 | 0.057 | 1.35 | 1.40 | 1.45 |
| b | 0.006 | 0.008 | 0.010 | 0.15 | 0.20 | 0.25 |
| c | 0.004 | 0.006 | 0.008 | 0.10 | 0.15 | 0.20 |
| D | 0.272 | 0.276 | 0.280 | 6.90 | 7.00 | 7.10 |
| E | 0.272 | 0.276 | 0.280 | 6.90 | 7.00 | 7.10 |
| e | 0.014 | 0.020 | 0.026 | 0.35 | 0.50 | 0.65 |
| $H_D$ | 0.350 | 0.354 | 0.358 | 8.90 | 9.00 | 9.10 |
| $H_E$ | 0.350 | 0.354 | 0.358 | 8.90 | 9.00 | 9.10 |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| $L_1$ | — | 0.039 | — | — | 1.00 | — |
| Y | — | — | 0.004 | — | — | 0.10 |
| θ | 0 | — | 7 | 0 | — | 7 |

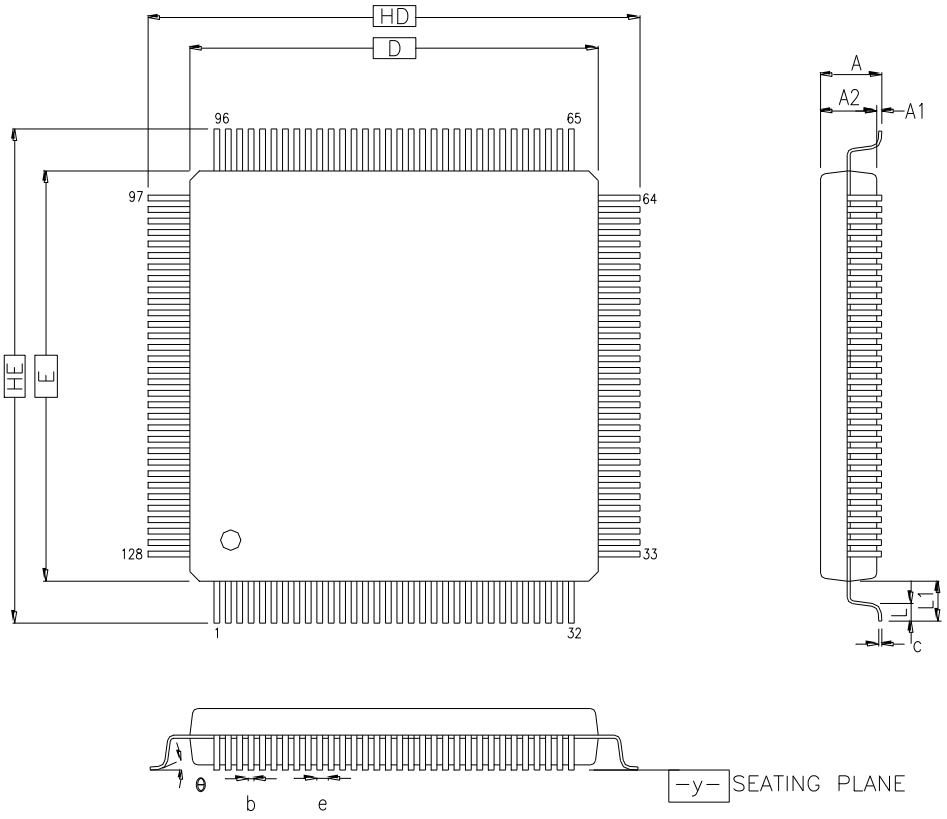
## 9.3 LQFP 64L (7x7x1.4 mm$^3$ footprint 2.0 mm)




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | --- | --- | 1.6 |
| STAND OFF | | A1 | 0.05 | --- | 0.15 |
| MOLD THICKNESS | | A2 | 1.35 | 1.4 | 1.45 |
| LEAD WIDTH(PLATING) | | b | 0.13 | 0.18 | 0.23 |
| LEAD WIDTH | | b1 | 0.13 | 0.16 | 0.19 |
| L/F THICKNESS(PLATING) | | c | 0.09 | --- | 0.2 |
| L/F THICKNESS | | c1 | 0.09 | --- | 0.16 |
| BODY SIZE | X | D | 9 BSC | | |
| | Y | E | 9 BSC | | |
| | X | D1 | 7 BSC | | |
| | Y | E1 | 7 BSC | | |
| LEAD PITCH | | e | 0.4 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| FOOTPRINT | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | --- | --- |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | --- | --- |
| | | R2 | 0.08 | --- | 0.2 |
| | | S | 0.2 | --- | --- |
| PACKAGE EDGE TOLERANCE | | aaa | 0.2 | | |
| LEAD EDGE TOLERANCE | | bbb | 0.2 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.07 | | |
| MOLD FLATNESS | | eee | 0.05 | | |



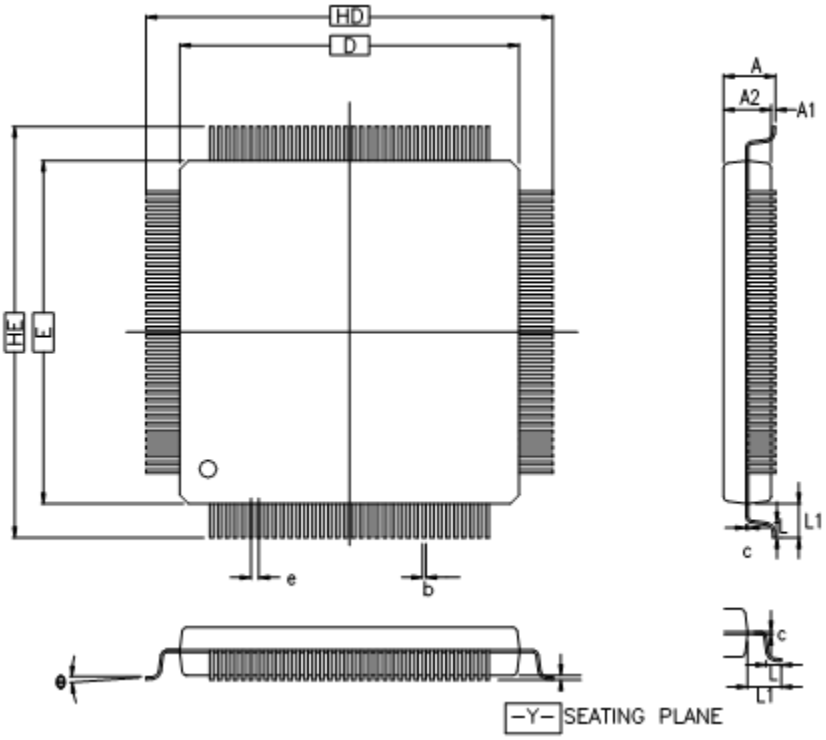
## 9.4 LQFP 128L (14x14x1.4 mm$^3$ footprint 2.0 mm)




COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| HD | 16.00 BSC. | | | 0.630 BSC. | | |
| D | 14.00 BSC. | | | 0.551 BSC. | | |
| HE | 16.00 BSC. | | | 0.630 BSC. | | |
| E | 14.00 BSC. | | | 0.551 BSC. | | |
| b | 0.13 | 0.16 | 0.23 | 0.005 | 0.006 | 0.009 |
| e | 0.40 BSC. | | | 0.016 BSC. | | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| y | – | – | 0.1 | – | – | 0.004 |

## 9.5 LQFP 144L (20x20x1.4 mm$^3$ footprint 2.0 mm)




COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| HD | 22.00 BSC. | | | 0.866 BSC. | | |
| D | 20.00 BSC. | | | 0.787 BSC. | | |
| HE | 22.00 BSC. | | | 0.866 BSC. | | |
| E | 20.00 BSC. | | | 0.787 BSC. | | |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| Y | 0 | — | 0.10 | – | — | 0.004 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |

# 10 ABBREVIATION

## 10.1 Abbreviations

| Acronym | Description |
|---|---|
| ACMP | Analog Comparator Controller |
| ADC | Analog-to-Digital Converter |
| AES | Advanced Encryption Standard |
| APB | Advanced Peripheral Bus |
| AHB | Advanced High-Performance Bus |
| BOD | Brown-out Detection |
| CAN | Controller Area Network |
| DAP | Debug Access Port |
| DES | Data Encryption Standard |
| EADC | Enhanced Analog-to-Digital Converter |
| EBI | External Bus Interface |
| EMAC | Ethernet MAC Controller |
| EPWM | Enhanced Pulse Width Modulation |
| FIFO | First In, First Out |
| FMC | Flash Memory Controller |
| FPU | Floating-point Unit |
| GPIO | General-Purpose Input/Output |
| HCLK | The Clock of Advanced High-Performance Bus |
| HIRC | 12 MHz Internal High Speed RC Oscillator |
| HXT | 4~24 MHz External High Speed Crystal Oscillator |
| IAP | In Application Programming |
| ICP | In Circuit Programming |
| ISP | In System Programming |
| LDO | Low Dropout Regulator |
| LIN | Local Interconnect Network |
| LIRC | 10 kHz internal low speed RC oscillator (LIRC) |
| MPU | Memory Protection Unit |
| NVIC | Nested Vectored Interrupt Controller |
| PCLK | The Clock of Advanced Peripheral Bus |
| PDMA | Peripheral Direct Memory Access |
| PLL | Phase-Locked Loop |
| PWM | Pulse Width Modulation |

| | |
|---|---|
| QEI | Quadrature Encoder Interface |
| SD | Secure Digital |
| SPI | Serial Peripheral Interface |
| SPS | Samples per Second |
| TDES | Triple Data Encryption Standard |
| TK | Touch Key |
| TMR | Timer Controller |
| UART | Universal Asynchronous Receiver/Transmitter |
| UCID | Unique Customer ID |
| USB | Universal Serial Bus |
| WDT | Watchdog Timer |
| WWDT | Window Watchdog Timer |

Table 10.1-1 List of Abbreviations

# 11 REVISION HISTORY

| Date | Revision | Description |
|---|---|---|
| 2018.03.30 | 1.00 | Initial version. |

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