N3290x

Data Sheet

Display Control Application Processor

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1. GENERAL DESCRIPTION

The N3290x seires built on the ARM926EJ-S CPU core and integrated with JPEG codec, CMOS sensor interface, 32-channel SPU (Sound Processing Unit), ADC, DAC, for meeting various kinds of application needs while saving the BOM cost. The combination of ARM926 @ 200MHz, synchronous DRAM, 2D BitBLT accelerator, CMOS image sensor interface, LCD panel interface, USB 1.1 Host & USB2.0 HS Device makes N3290x series the best choice for LCD ELA devices.

Maximum resolution for N3290 series is XVGA (1,024x768) @ TFT LCD panel. The 2D BitBLT accelerator accelerates the graphic compution to make the rendering smooth and off-load CPU to save power consumption.

The N3290x seires is well-positioned in terms of cost/performance for the applications which bitmap graphics is extensively used or CMOS Image Sensor (CIS) interface is required.

The N3290x series is for application under Linux OS and leverage the driver availability of emerging functionalities like Wi-Fi, browser, etc. On the other hand, the open source code environment also give the product development more flexible.

To meet the different requirement of the overall system BOM cost, the different size of DRAM is stacked with N3290x main SoC into one package, that is, multi-chip package (MCP). The N32901x series particularly designed with 1Mbitx16 3.3V SDRAM. The N32903x series particularly designed with 4Mbitx16 1.8V DDR SDRAM. One 16Mbitx16 1.8V DDR2 SDRAM stacked inside the N32905x series to ensure higher performance and minimize the system design efforts, like EMI & noise coupling. Total BOM cost could be reduced by employing 2-layer PCB along with the elimination of damping resistors, EMI prevention components, etc. Advantages including, but not limited to, less PCB space, shorter lead time, and higher / reliable production yield.

1.1 Applications

- ELA (Educational Learning Aid)
- HMI
- Security
- Home Appliance
- Advertisement

2. FEATURES

- CPU
  - ARM926EJ-S 32-bit RISC CPU with 8KB I-Cache & 8KB D-Cache
  - Frequency up to 200MHz@1.8V core power operation voltage
  - JTAG interface supported for development and debugging

- Internal SRAM & ROM
  - 8KB internal SRAM and 16KB IBR internal booting ROM supported
  - IBR booting messages displayed by UART console for debugging supported
  - Different system booting modes supported:
    - Memory card
      - SD card
      - SD-to-NAND flash bridge
    - Raw NAND Flash
    - SPI Flash
    - USB

- EDMA (Enhanced DMA)
  - Totally 5 DMA channels supported
    - 4 peripheral DMA channels for transfer between memory and on-chip peripherals, such as ADC, UART and SPI
    - One dedicated channel for memory-to-memory transfer
  - Byte, half-word and word data width types supported
  - Single and burst transfer modes supported
  - Block transfer supported in memory-to-memory transfer channel
  - Color format transformation supported in memory-to-memory transfer channel
    - Source color format could be RGB555, RGB565 and YCbCr422
    - Destination color format could be RGB555, RGB565 and YCbCr422
  - Auto reload supported for continuous data transfer
  - Interrupt generation supported in the half-of-transfer or end-of-transfer

- Capture (CMOS Sensor I/F)
  - CCIR601 & CCIR656 interfaces supported for connection to CMOS image sensor
  - Resolution up to 2M pixel for Still Image Capture, 640x480 (VGA) resolution for MJPEG Video Streaming
  - YUV422 and RGB565 color format supported for data-in from CMOS sensor
  - YUV422, RGB565, RGB555 and Y-only color format supported for data storing to system memory
  - Planar and packet data formats supported for data storing to system memory
  - Image cropping supported with the cropping window up to 4096x2048
  - Image scaling-down supported
    - Vertical and horizontal scaling-down for preview mode supported
      - The scaling factor is N/M
      - Two pairs of configurable 8-bit N and 8-bit M for vertical and horizontal scaling-down
      - The value of N has to equal to or less than M
    - Frame rate control supported
  - Combines two interlace fields to a single frame supported for data in from TV-decoder

- JPEG Codec
  - Baseline Sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard supported.
  - Planar Format
    - Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
    - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
    - Support to decode YCbCr 4:2:2 transpose format
    - Support arbitrary width and height image encode and decode
    - Support three programmable quantization-tables
    - Support standard default Huffman-table and programmable Huffman-table for decode
    - Support arbitrarily 1X~8X image up-scaling function for encode mode
    - Support down-scaling function for encode and decode modes
    - Support specified window decode mode
    - Support quantization-table adjustment for bit-rate and quality control in encode mode
    - Support rotate function in encode mode
  - Packet Format
    - Support to encode interleaved YUYV format input image, output bitstream 4:2:2 and 4:2:0 format
    - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
    - Support decoded output image RGB555, RGB565 and RGB888 formats.
    - The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
    - Support arbitrary width and height image encode and decode
    - Support three programmable quantization-tables
    - Support standard default Huffman-table and programmable Huffman-table for decode
    - Support arbitrarily 1X~8X image up-scaling function for encode mode
    - Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
    - Support specified window decode mode
    - Support quantization-table adjustment for bit-rate and quality control in encode mode

- 2D Accelerator
  - BitBLT operation
    - 2x2 transform matrix with effects:
      - Scale
      - Translate
      - Rotate
      - Shear
    - Alpha blending and color transformation supported
    - Source format for operations: supported color format of source bitmap
  - Fill
    - Rectangle Fill with single color – ARGB8888
    - Fill with blending effect supported
  - Supported color formats
    - Source
      - 16 bits/pixel – RGB565
      - 32 bits/pixel – ARGB8888
      - 1 bit/pixel, 2 bits/pixel, 4 bits/pixel, 8 bits/pixel with RGB color palette
    - Destination

- 16 bits/pixel – RGB565
- 32 bits/pixel – ARGB8888

- VPOST
  - 8/16/18-bit SYNC type and 8/9/16/18-bit MPU type TFT LCD supported
  - Color format supported:
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data in
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data out
  - XGA (1024x768), SVGA (800x600), WVGA (800x480), D1 (720X480), VGA (640x480), WQVGA (480x272), QVGA (320x240) and HVGA (640x240) resolution supported
    - The maximum resolution is up to D1 (720X480) for TV output
    - The maximum resolution is up to 1024X768 for TFT LCD panel for still image displaying
    - The maximum resolution is up to 480x272 for TFT LCD panel for MJPEG video displaying up to 25fps.
  - Display scaler – to fit different size of LCD panels
    - Horizontal: At most 4.0x scale
    - Vertical: At most 3.0x scale
  - For SYNC type LCD:
    - For 8-bit bus
      - CCIR601 YCbCr422 packet mode (NTSC/PAL) supported
      - CCIR601 RGB Dummy mode (NTSC/PAL) supported
      - CCIR656 interface supported
      - RGB Through mode supported
    - For 16/18-bit bus
      - Parallel pixel data output mode (1-pixel/1-clock)
  - Color format transform supported:
    - Color format transform between YCbCr422 and RGB565
    - Color format transform from YCbCr422 to RGB888
  - Support OSD function to overlap system information like battery life, brightness tuning, volume tuning or muting, etc.

- Frame Switch Controller
  - Frame relation controlled between VPOST and Capture supported
  - 2 modes supported to switch Frame Buffer Base
    - Frame Ratio Mode (16 selectable ratio)
    - Frame sync mode
  - Double/triple buffers supported

- SPU (Sound Processing Unit)
  - 32 stereo channels supported
  - PCM8/PCM16/4-bit MDPCM/TONE source format supported
  - 7-bit volume control supported for each of 32 channels
  - 5-bit pan control supported for each L/R of 32 channels
  - 10-band equalizer supported
  - Special code supported for loop playing and event detection

- Audio DAC
  - 16-bit stereo DAC supported with headphone driver output
  - H/W volume control supported

- I2S Controller

- I2S interface supported to connect external audio codec
- 16/18/20/24-bit data format supported

- Storage Interface Controller
  - Interface to NAND Flash:
    - 8-bit data bus width supported
    - SLC and MLC type NAND Flash supported
    - 512B, 2KB, 4KB, and 8KB page size NAND Flash supported
    - ECC4, ECC8, ECC12 and ECC15 algorithm supported for ECC generation, error detection and error correction
    - PBA-NAND flash supported
  - Interface to SD/MMC/SDIO/SDHC/micro-SD cards supported
    - SD-to-NAND flash bridge supported
  - DMA function supported to accelerate the data transfer between system memory and NAND Flash or SD/MMC/SDIO/SDHC/micro-SD

- USB Device Controller
  - USB2.0 HS (High-Speed) x 1 port
  - 6 configurable endpoints supported
  - Control, Bulk, Interrupt and Isochronous transfers supported
  - Suspend and remote wakeup supported

- USB Host Controller
  - USB1.1 Host one H/W Engine, two pin locations.
  - Fully compliant with USB Revision 1.1 specification
  - Open Host Controller Interface (OHCI) Revision 1.0 compatible
  - Full-speed (12Mbps) and low-speed (1.5Mbps) USB devices supported
  - Control, Bulk, Interrupt and Isochronous transfers supported

- Timer & Watch-Dog Timer
  - Two 32-bit with 8-bit pre-scalar timers supported
  - One programmable 24-bit Watch-Dog Timer supported

- PWM
  - 4 PWM channel outputs supported
  - 16-bit counter supported for each PWM channel
  - Two 8-bit pre-scalars supported and each pre-scalar shared by two PWM channels
  - Two clock-dividers supported and each divider shared by two PWM channels
  - Two Dead-Zone generators supported and each generator shared by two PWM channels
  - Auto reloaded mode and one-shot pulse mode supported
  - Capture function supported

- UART
  - A high speed UART supported:
    - Baud rate is up to 1M bps
    - 4 signals TX, RX, CTS and RTS supported
  - A normal UART supported:
    - Baud rate is up to 115.2K bps
    - 2 signals TX and RX supported only

- SPI

- One SPI controller is supported
  - Both master and slave mode are supported in SPI interface
  - Two chip selection signals for two SPI devices

- I2C
  - One I2C channel supported
  - Compatible with Philips's I^2C standard and only master mode supported
  - Multi-master operation supported

- Advanced Interrupt Controller
  - Total 32 interrupt source supported
  - Configurable interrupt type:
    - Low-active level triggered interrupt
    - High-active level triggered interrupt
    - Low-active edge (falling edge) triggered interrupt
    - High-active edge (rising edge) triggered interrupt
  - Individual interrupt mask bit for each interrupt source
  - 8 different priority levels supported
  - Daisy-chain priority mechanism supported for interrupts with same priority level
  - Low priority interrupt automatic masking supported for interrupt nesting

- RTC
  - Independent power plane supported
  - 32.768 KHz crystal oscillation circuit supported
  - Time counter (second, minute, hour) and Calendar counter (day, month, year) supported
  - Alarm supported (second, minute, hour, day, month and year)
  - 12/24-hour mode and Leap year supported
  - Alarm to wake chip up from Standby mode or from Power-down mode supported
  - Wake chip up from Power-down mode by input pin supported
  - Power-off chip by register setting supported
  - Power-on timeout is supported for low battery protection

- GPIO
  - 80 programmable general purpose I/Os supported and separated into 5 groups
  - Individual configuration supported for each I/O signal
  - Configurable interrupt control functions supported
  - Configurable de-bounce circuit supported for interrupt function

- ADC
  - Multi-channel, 10-bit ADC supported
    - 2 channels dedicated for 4-wire resistive touch sensor inputs
    - 2 channels dedicated for Audio ADC with Microphone pre-Amp & AGC
    - 3 channels reserved for various purposes, like LVD (Low Voltage Detection), keypad input, and light sensor
    - Input voltage range from 0V ~ 3.3V supported
  - Maximum 25MHz input clock supported
  - Maximum 400K/s conversion rate supported
  - LVR (Low Voltage Reset) supported

- Power Management

- Advanced power management including Power Down, Deep Standby, CPU Standby, and Normal Operating modes
  - Normal Operating Mode
    - Core power is 1.8V and chip is in normal operation
  - CPU Standby Mode
    - Core power is 1.8V and only ARM CPU clock is turned OFF
  - Deep Standby Mode
    - Core power is 1.8V and all IP clocks are turned OFF
  - Power Down Mode
    - Only the RTC power is ON. Other 3.3V and 1.8V power are OFF
    - N3290xRxDN series don't support this mode
    - N3290xKxDN don't support RTC wakup function.

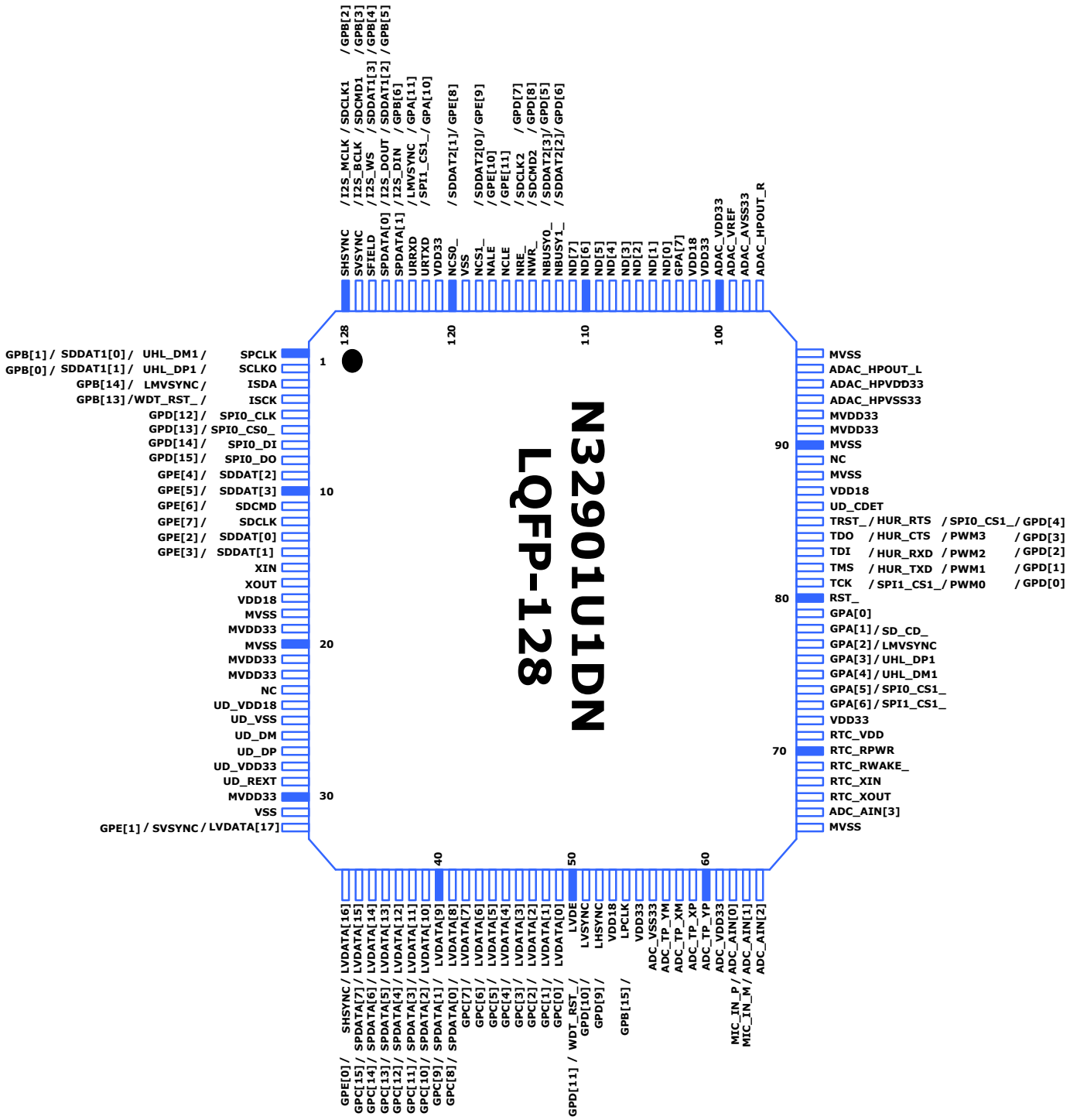
- Software Support
  - Development Tools
    - Bootloader / Diagnostic Program / NAND Writer Program: ADS 1.2 or RVDS 2.x or 3.x
    - Linux Kernel (2.6.17.14) / System Manager: GCC 4.2
    - TurboWriter / Sync Tool: Microsoft VC 6.0
  - NAND Flash File System
    - FAT12, FAT16 and FAT32 with long filename are supported
    - Hidden disk is supported
    - RAM disk is supported
  - S/W audio Library
    - Decoders with ADPCM / MP3 / ACC / OGG / WMA format support
    - 32-polyphony Wavetable MIDI synthesizer
    - Programmable sampling rate and target bit rate
  - USB Driver
    - MS (Mass Storage) Class
    - HID (Human Interface Device) Class

- Operating Voltage
  - I/O: 3.3V
  - Core: 1.8V for 200MHz

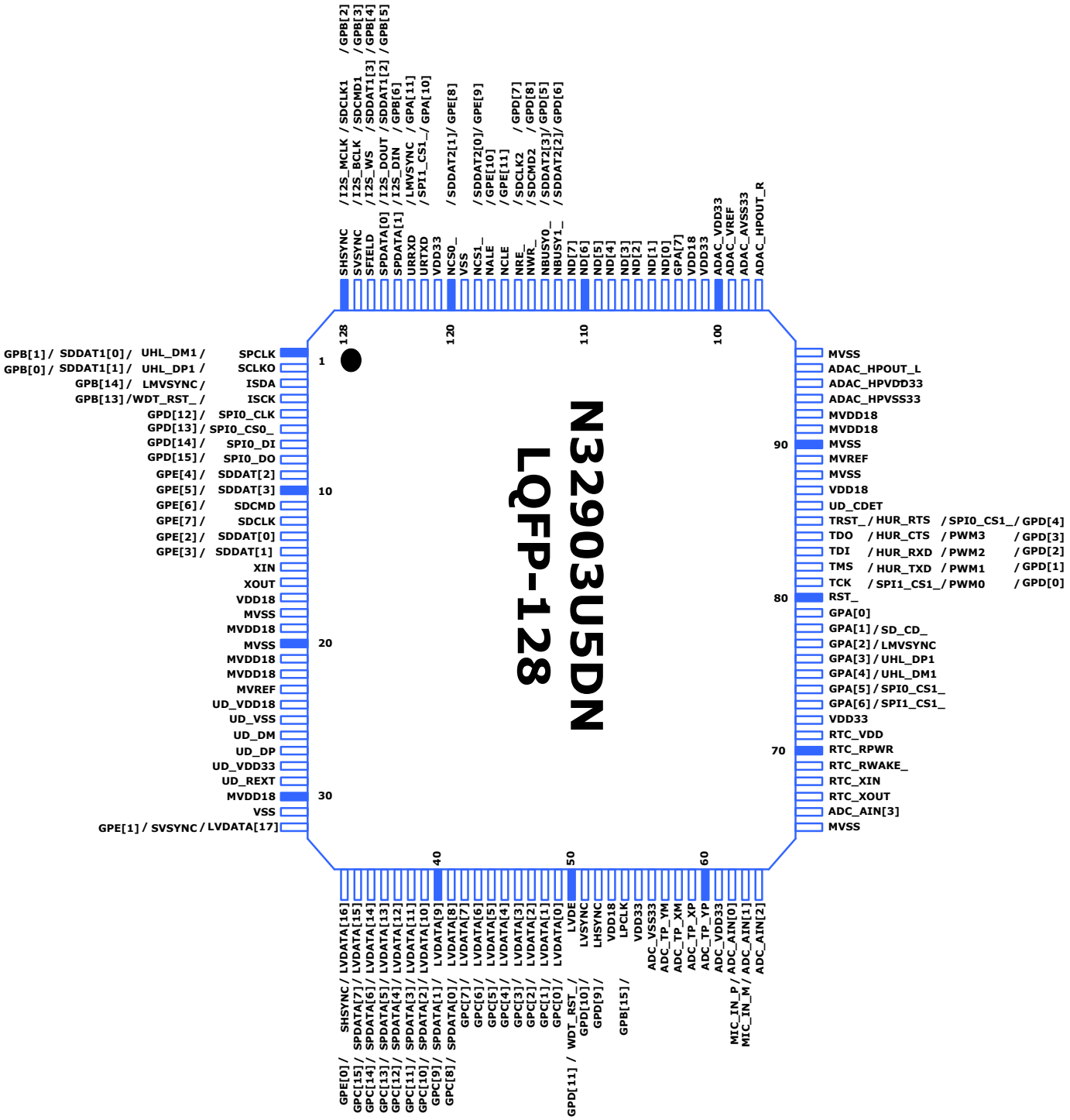
- Package
  - LQFP-128 MCP
  - TPFP-64 MCP with EPAD
  - LQFP-64 MCP

3. PIN DIAGRAM

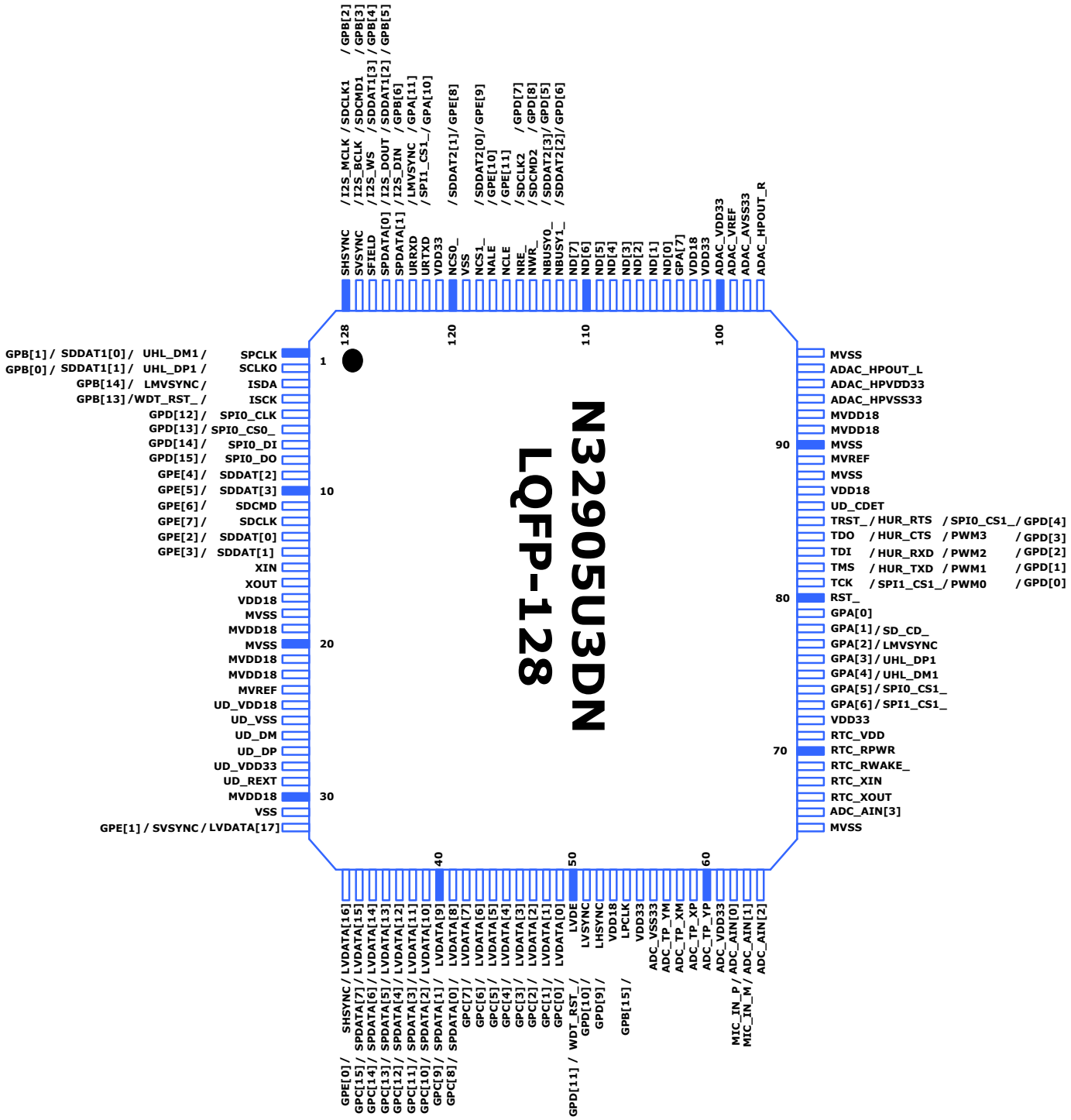
3.1 N32901U1DN (LQFP-128)



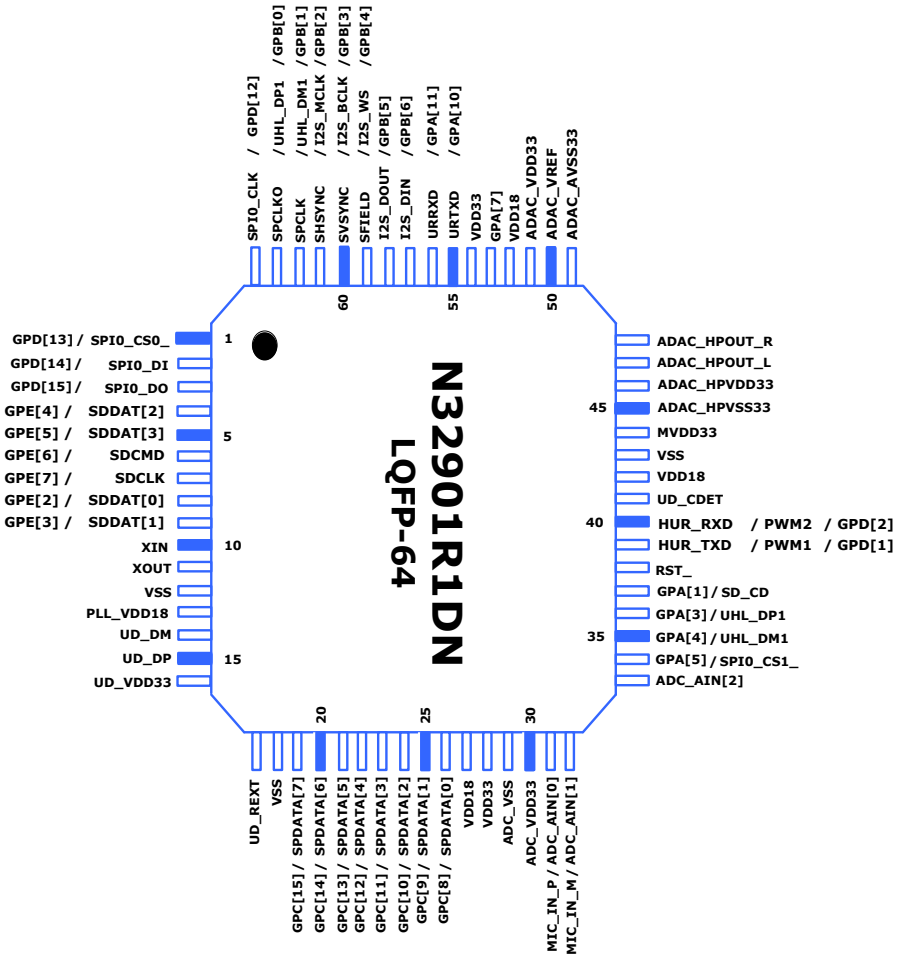
3.2 N32903U5DN (LQFP-128)



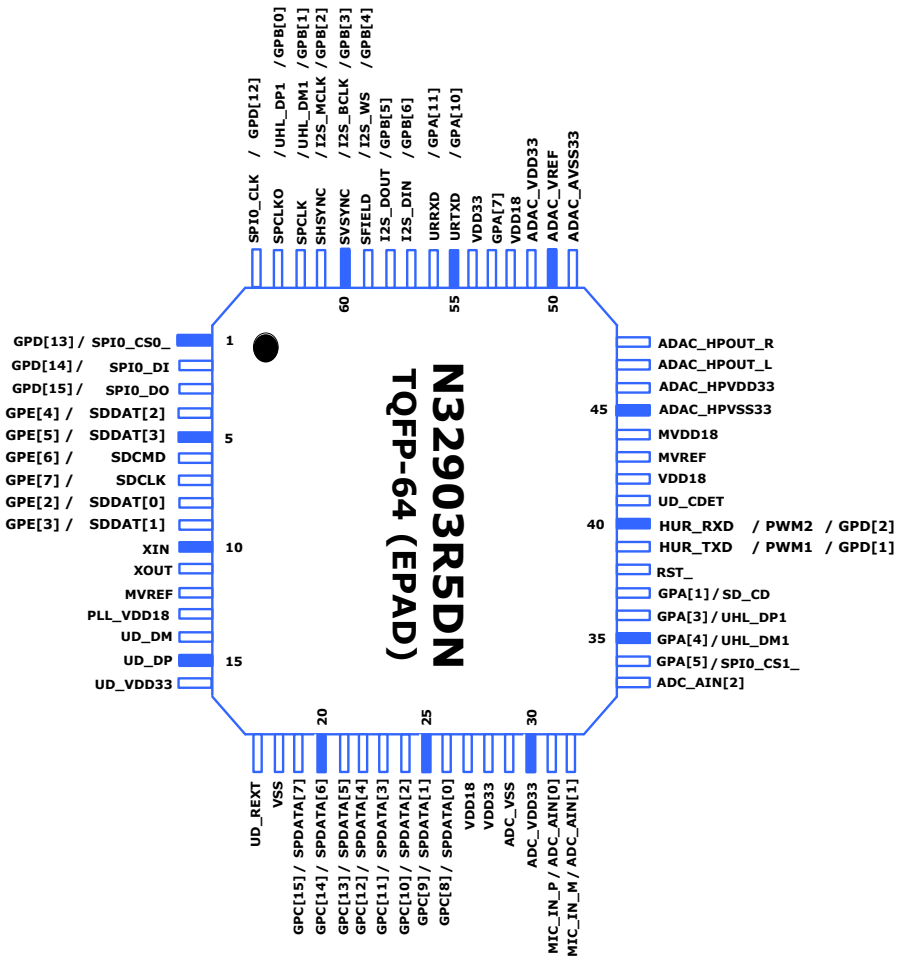
3.3 N32905U3DN (LQFP-128)



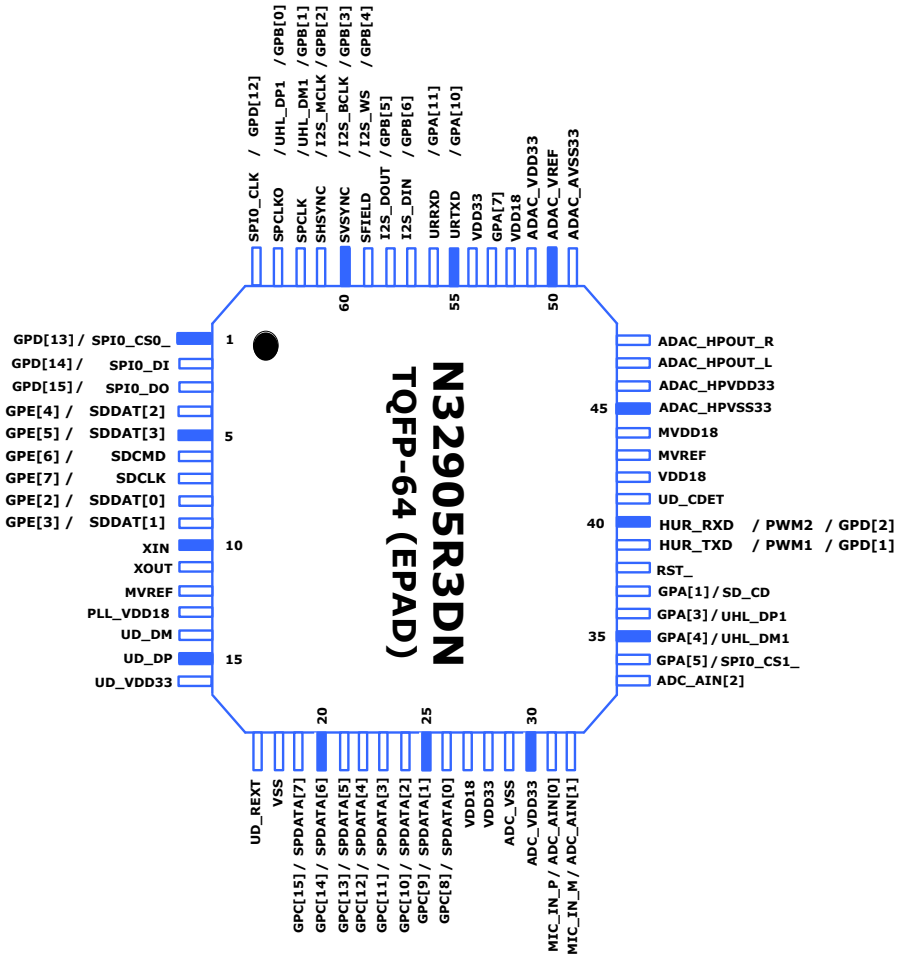
3.4 N32901R1DN (LQFP-64)



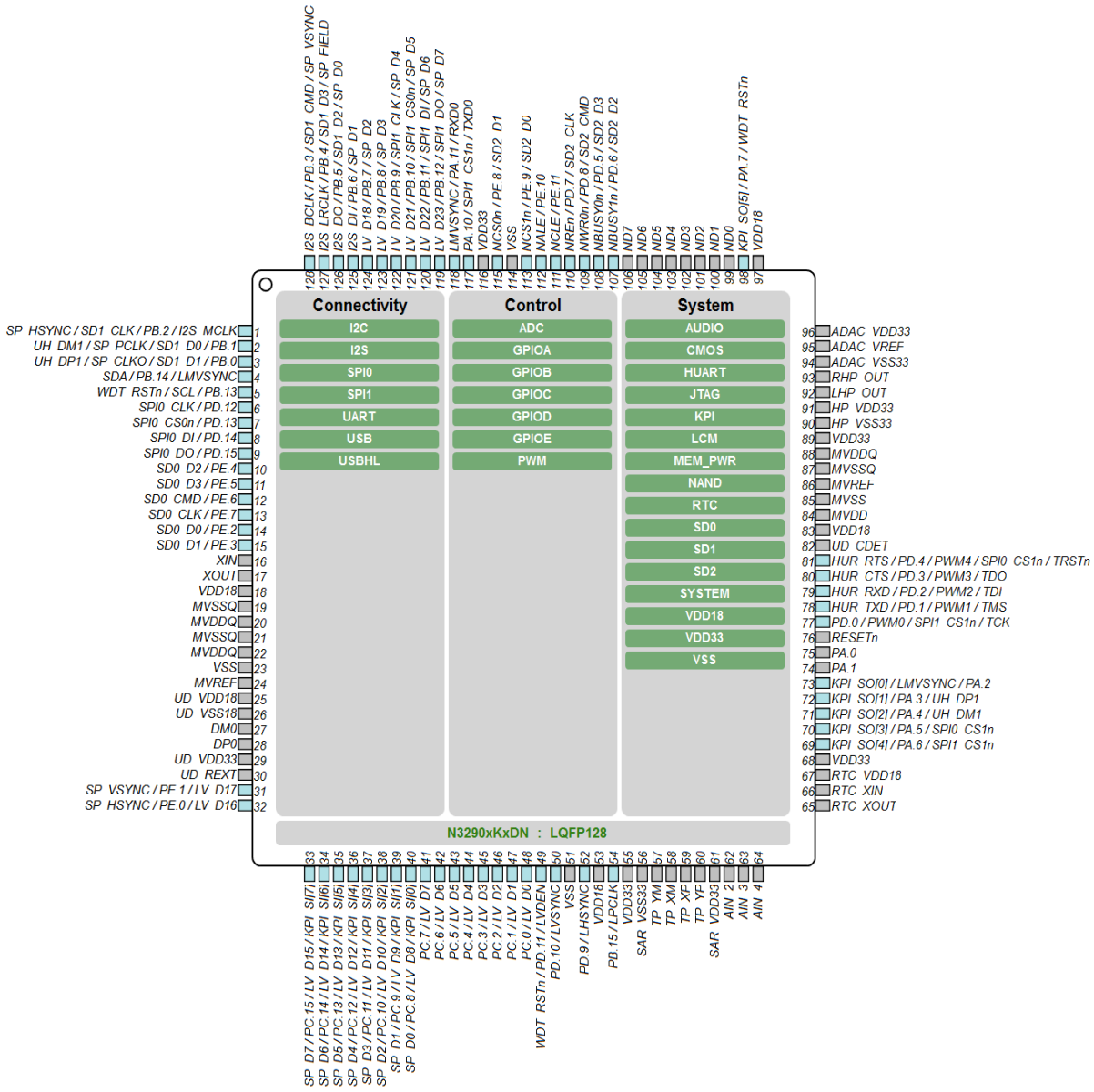
3.5 N32903R5DN (TQFP-64 EPAD)



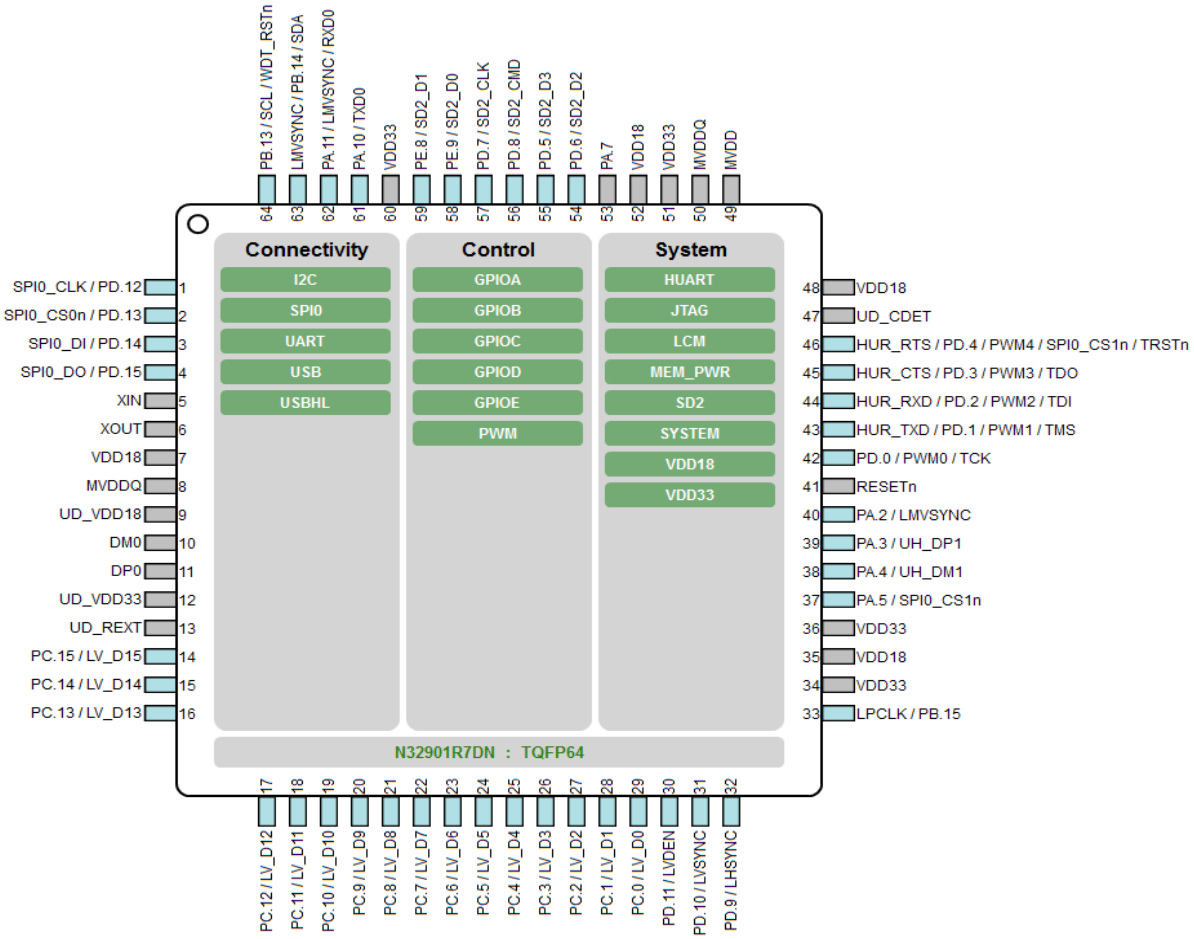
3.6 N32905R3DN (TQFP-64 EPAD)



3.7 N3290xKxDN (LQFP128)



3.8 N32901R7DN (TQFP-64 EPAD)



4. PIN DESCRIPTION

4.1 N3290xUxDN Pin Description

Pin No	Name	Type	Group	Description
1	SPCLK	IOU	CAP	Sensor Interface Pixel Clock, Input
	GPB[1]	IOU	GPIOB	GPIO Port B Bit 1
	SD1_DAT[0]	IOU	SD1	SD Port 1 Data Bit 0
	UHL_DM1	IOU	USB	USB Host 1.0 Lite Port 1, D-E154
2	SCLKO	OU	CAP	Clock to Sensor Module, Output
	GPB[0]	IOU	JTAG	GPIO Port B Bit 0
	SD1_DAT[1]	IOU	SD1	SD Port 1 Data Bit 1
	UHL_DP1	IOU	USB	USB Host 1.0 Lite Port 1, D+
3	ISDA	IOU	I2C	I2C Interface Data
	GPB[14]	IOU	GPIOB	GPIO Port B Bit 14
	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
	LMVSYNC	OU	LCD	MPU LCD Interface Mode VSYNC, Output
4	ISCK	OU	I2C	I2C Interface Clock, Output
	GPB[13]	IOU	GPIOB	GPIO Port B Bit 13
5	SPI0_CLK	IOU	SPI0	SPI Port 0 Clock;Output in Master Mode;Input in Slave Mode
	GPD[12]	IOU	GPIOD	GPIO Port D Bit 12
6	SPI0_CS0_	IOU	SPI0	SPI Port 0 Device Select 0, Low Active;Output in Master Mode;Input in Slave Mode
	GPD[13]	IOU	GPIOD	GPIO Port D Bit 13
7	SPI0_DI	IU	SPI0	SPI Port 0 Data Input
	GPD[14]	IOU	GPIOD	GPIO Port D Bit 14
8	SPI0_DO	OU	SPI0	SPI Port 0 Data Output
	GPD[15]	IOU	GPIOD	GPIO Port D Bit 15
9	SD0_DAT[2]	IOU	SD0	SD Port 0 Data Bit 2
	GPE[4]	IOU	GPIOE	GPIO Port E Bit 4
10	SD0_DAT[3]	IOU	SD0	SD Port 0 Data Bit 3
	GPE[5]	IOU	GPIOE	GPIO Port E Bit 5
11	SD0_CMD	IOU	SD0	SD Port 0 Command/Response
	GPE[6]	IOU	GPIOE	GPIO Port E Bit 6
12	SD0_CLK	OU	SD0	SD Port 0 Clock, Output
	GPE[7]	IOU	GPIOE	GPIO Port E Bit 7
13	SD0_DAT[0]	IOU	SD0	SD Port 0 Data Bit 0

	GPE[2]	IOU	GPIOE	GPIO Port E Bit 2
14	SD0_DAT[1]	IOU	SD0	SD Port 0 Data Bit 1
	GPE[3]	IOU	GPIOE	GPIO Port E Bit 3
15	XIN	I	XTAL	12MHz Crystal Input
16	XOUT	O	XTAL	12MHz Crystal Output
17	VDD18	P	Core	Core Logic Power (1.8V)
18	VSSQ	G	MVDD	SDRAM I/F Ground (0V)
19	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903U5DN or N32905U3DN are installation MVDD=3.3V powered when N32901U1DN is installation
20	VSSQ	G	MVDD	SDRAM Ground (0V)
21	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903U5DN or N32905U3DN are installation MVDD=3.3V powered when N32901U1DN is installation
22	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903U5DN or N32905U3DN are installation MVDD=3.3V powered when N32901U1DN is installation
23	NC	--	NC	when N32901U1DN is installation
	MVREF	P	MVDD	1/2 MVDD (0.9V) for DDR_VREF, when N32903U5DN or N32905U3DN are installation
24	PLL_UD_VDD18	P	PLL & USB	PLL & USB2.0 Device Core Power (1.8V)
25	UD_VSS	G	USB	USB2.0 Device Ground (0V)
26	UD_DM	I/O	USB	USB 2.0 Device D-.
27	UD_DP	I/O	USB	USB 2.0 Device D+.
28	UD_VDD33	P	USB	USB 2.0 Device PHY 3.3V
29	UD_REXT	O	USB	External Resistor 12.1K resistor connected to ground
30	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903U5DN or N32905U3DN are installation MVDD=3.3V powered when N32901U1DN is installation
31	VSS	G	GND	Ground (0V)
32	LVDATA[17]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 17

	SVSYNC	IU	CAP	Sensor Interface VSYNC, Input
	GPE[1]	IOU	GPIOE	GPIO Port E Bit 1
33	LVDATA[16]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 16
	SHSYNC	IU	CAP	Sensor Interface HSYNC, Input
	GPE[0]	IOU	GPIOE	GPIO Port E Bit 0
34	LVDATA[15]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 15
	GPC[15]	IOU	GPIOC	GPIO Port C Bit 15
	SPDATA[7]	IU	CAP	Sensor Interface Data Bit 7, Input
	KPI_SI[7]	IU	KPI	KPI Scan In Bit 7
35	LVDATA[14]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 14
	GPC[14]	IOU	GPIOC	GPIO Port C Bit 14
	SPDATA[6]	IU	CAP	Sensor Interface Data Bit 6, Input
	KPI_SI[6]	IU	KPI	KPI Scan In Bit 6
36	LVDATA[13]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 13
	GPC[13]	IOU	GPIOC	GPIO Port C Bit 13
	SPDATA[5]	IU	CAP	Sensor Interface Data Bit 5, Input
	KPI_SI[5]	IU	KPI	KPI Scan In Bit 5
37	LVDATA[12]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 12
	GPC[12]	IOU	GPIOC	GPIO Port C Bit 12
	SPDATA[4]	IU	CAP	Sensor Interface Data Bit 4, Input
	KPI_SI[4]	IU	KPI	KPI Scan In Bit 4
38	LVDATA[11]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 11
	GPC[11]	IOU	GPIOC	GPIO Port C Bit 11
	SPDATA[3]	IU	CAP	Sensor Interface Data Bit 3, Input
	KPI_SI[3]	IU	KPI	KPI Scan In Bit 3
39	LVDATA[10]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 10
	GPC[10]	IOU	GPIOC	GPIO Port C Bit 10
	SPDATA[2]	IU	CAP	Sensor Interface Data Bit 2, Input
	KPI_SI[2]	IU	KPI	KPI Scan In Bit 2
40	LVDATA[9]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 9
	GPC[9]	IOU	GPIOC	GPIO Port C Bit 9
	SPDATA[1]	IU	CAP	Sensor Interface Data Bit 1, Input
	KPI_SI[1]	IU	KPI	KPI Scan In Bit 1
41	LVDATA[8]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 8
	GPC[8]	IOU	GPIOC	GPIO Port C Bit 8

	SPDATA[0]	IU	CAP	Sensor Interface Data Bit 0, Input
	KPI_SI[0]	IU	KPI	KPI Scan In Bit 0
42	LVDATA[7]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 7
	GPC[7]	IOU	GPIOC	GPIO Port C Bit 7
43	LVDATA[6]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 6
	GPC[6]	IOU	GPIOC	GPIO Port C Bit 6
	CFG[10]	IU	SYSTEM	Chip Power-On Configuration Bit [10], Input
44	LVDATA[5]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 5
	GPC[5]	IOU	GPIOC	GPIO Port C Bit 5
	CFG[9]	IU	SYSTEM	Chip Power-On Configuration Bit [9], Input
45	LVDATA[4]	IOU	LCD	GPIO Port C Bit 4
	GPC[4]	IOU	GPIOC	GPIO Port C Bit 4
	CFG[8]	IU	SYSTEM	Chip Power-On Configuration Bit [8], Input
46	LVDATA[3]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 3
	GPC[3]	IOU	GPIOC	GPIO Port C Bit 3
47	LVDATA[2]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 2
	GPC[2]	IOU	GPIOC	GPIO Port C Bit 2
48	LVDATA[1]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 1
	GPC[1]	IOU	GPIOC	GPIO Port C Bit 1
49	LVDATA[0]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 0
	GPC[0]	IOU	GPIOC	GPIO Port C Bit 0
50	LVDE	OU	LCD	SYNC LCD Interface Data Enable, Output, High Active
	LRS	OU	LCD	MPU LCD Interafec Register Select
	GPD[11]	IOU	GPIOD	GPIO Port D Bit 11
51	LVSYNC	OU	LCD	SYNC LCD Interface VSYNC, Output, High Active
	LRD	OU	LCD	MPU I80 mode LCD Interface Read, active low
	LEN	OU	LCD	MPU M68 mode LCD Interface Read Write Enable/Disable , High Enable
	GPD[10]	IOU	GPIOD	LCD Interface Data Enable, High Active.
52	LHSYNC	OU	LCD	SYNC LCD Interface HSYNC, Output, High Active
	LWR	OU	LCD	MPU I80 mode LCD Interfacer Write, active low
	LR/W	OU	LCD	MPU M68 mode LCD interface R/W, High is read command and Low is write instruction
	GPD[9]	IOU	GPIOD	GPIO Port D Bit 9
53	VDD18	P	Core	Core Logic Power (1.8V)

54	LPCLK	OU	LCD	SYNC LCD Interface Pixel Clock, Output
	LCS	OU	LCD	MPU LCD Interface Chip Enable, active low
	GPB[15]	IOU	GPIOB	GPIO Port B Bit 15
55	VDD33	P	I/O	I/O Power (3.3V)
56	ADC_VSS33	G	ADC	ADC Ground (0V)
57	ADC_TP_YM	I	ADC	Touch Panel YM
58	ADC_TP_XM	I	ADC	Touch Panel XM
59	ADC_TP_XP	I	ADC	Touch Panel XP
60	ADC_TP_YP	I	ADC	Touch Panel YP
61	ADC_VDD33	P	ADC	ADC Power (3.3V)
62	ADC_AIN[0]	I	ADC	ADC MIC+
63	ADC_AIN[1]	I	ADC	ADC MIC-
64	ADC_AIN[2]	I	ADC	ADC Analog Input Channel 2
65	VSS	G	GND	Ground (0V)
66	ADC_AIN[3]	I	ADC	ADC Analog Input Channel 3
67	RTC_XOUT	O	RTC	32768Hz Crystal Output
68	RTC_XIN	I	RTC	32768Hz Crystal Input
69	RTC_RWAKE_	I	RTC	Wakeup Enable or Power switch Input with Low Active (an external pull high resistor is need)
70	RTC_RPWR	O	RTC	Power Enable for external power IC enable pin, Open-Drain output (an external pull high resistor is need)
71	RTC_VDD1.8V	P	RTC	RTC Power (1.8V)
72	VDD33	P	I/O	I/O Power (3.3V)
73	GPA[6]	IOU	GPIOA	GPIO Port A Bit 6
	SPI1_CS1_	OU	SPI1	SPI Port 1 Device Select 1, Output, Low Active
	KPI_SO[4]	OU	KPI	KPI Scan Out Bit 4
74	GPA[5]	IOU	GPIOA	GPIO Port A Bit 5
	SPI0_CS1_	OU	SPI0	SPI Port 0 Device Select 1, Output, Low Active
	KPI_SO[3]	OU	KPI	KPI Scan Out Bit 3
75	GPA[4]	IOU	GPIOA	GPIO Port A Bit 4
	UHL_DM1	IOU	USB	USB Host 1.0 Lite Port 1, D-
	KPI_SO[2]	OU	KPI	KPI Scan Out Bit 2
76	GPA[3]	IOU	GPIOA	GPIO Port A Bit 3
	UHL_DP1	IOU	USB	USB Host 1.0 Lite Port 1, D+
	KPI_SO[1]	OU	KPI	KPI Scan Out Bit 1
77	GPA[2]	IOU	GPIOA	GPIO Port A Bit 2
	LMVSYNC	OU	LCD	MPU LCD Interface VSYNC, Output

	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
	KPI_SO[0]	OU	KPI	KPI Scan Out Bit 0
78	GPA[1]	IOU	GPIOA	GPIO Port A Bit 1
	SD_CD_	IU	SD	SD Card Detect, Input, Low Active
79	GPA[0]	IOU	GPIOA	GPIO Port A Bit 0
80	RST_	IU	SYSTEM	System Reset, Input, Low Active
	WDT_RST_	OU	SYSTEM	Watch-Dog Reset, Output, Low Active
81	TCK	ID	JTAG	JTAG Interface Test Clock, Input
	GPD[0]	IOD	GPIOD	GPIO Port D Bit 0
	SPI1_CS1_	OD	SPI1	SPI Port 1 Device Select 1, Output, Low Active
	PWM0	OD	PWM	PWM Channel 0
82	TMS	IU	JTAG	JTAG Interface Test Mode Select, Input
	GPD[1]	IOU	GPIOD	GPIO Port D Bit 1
	HUR_TXD	OU	UART	High-Speed UART TX Data, Output
	PWM1	OU	PWM	PWM Channel 1
83	TDI	IU	JTAG	JTAG Interface Test Data In, Input
	GPD[2]	IOU	GPIOD	GPIO Port D Bit 2
	HUR_RXD	IU	UART	High-Speed UART RX Data, Input
	PWM2	OU	PWM	PWM Channel 2
84	TDO	OU	JTAG	JTAG Interface Test Data Out, Output
	GPD[3]	IOU	GPIOD	GPIO Port D Bit 3
	HUR_CTS	IU	UART	High-Speed UART Clear-To-Send, Input, Low Active
	PWM3	OU	PWM	PWM Channel 3
85	TRST_	IU	JTAG	JTAG Interface Test Reset, Input, Low Active
	GPD[4]	IOU	GPIOD	GPIO Port D Bit 4
	HUR_RTS	OU	UART	High-Speed UART Reset-To-Send, Output, Low Active
	SPI0_CS1_	OU	SPI0	SPI Port 0 Device Select 1, Output, Low Active
86	UD_CDET	I	USB	USB Device Connect Detect, Input, High Active
87	VDD18	P	Core	Core Logic Power (1.8V)
88	MVSS	G	MVDD	SDRAM I/F Ground (0V)
89	MVREF	P	MVDD	1/2 MVDD (0.9V) for DDR_VREF, when N32903U5DN and N32905U3DN are installation
	NC	--	NC	when N32901U1DN is installation
90	VSSQ	G	MVDD	SDRAM Ground (0V)

91	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903U5DN or N32905U3DN are installation MVDD=3.3V powered when N32901U1DN is installation
92	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903U5DN or N32905U3DN are installation MVDD=3.3V powered when N32901U1DN is installation
93	ADAC_HPVSS33	G	AUDIO	Audio DAC Headphone Driver Ground (0V)
94	ADAC_HPVDD33	P	AUDIO	Audio DAC Headphone Driver Power (3.3V)
95	ADAC_HPOUT_L	O	AUDIO	Audio Headphone Left Channel Output
96	VSS	G	GND	Ground (0V)
97	ADAC_HPOUT_R	O	AUDIO	Audio Headphone Right Channel Output
98	ADAC_AVSS33	G	AUDIO	Audio DAC Ground (0V)
99	ADAC_VREF	O	AUDIO	Audio DAC Reference Voltage Output, please connect 1uF capacitor to DAC ground
100	ADAC_AVDD33	P	AUDIO	Audio DAC Power (3.3V)
101	ADAC_AVDD33	P	AUDIO	Audio DAC Power (3.3V)
102	VDD18	P	Core	Core Logic Power (1.8V)
103	GPA[7]	IOU	GPIOA	GPIO Port A Bit 7
	KPI_SO[5]	OU	KPI	KPI Scan Out Bit 5
104	ND[0]	IOU	NAND	NAND Interface Data Bit [0]
	CFG[0]	IU	SYSTEM	Chip Power-On Configuration Bit [0], Input
105	ND[1]	IOU	NAND	NAND Interface Data Bit [1]
	CFG[1]	IU	SYSTEM	Chip Power-On Configuration Bit [1], Input
106	ND[2]	IOU	NAND	NAND Interface Data Bit [2]
	CFG[2]	IU	SYSTEM	Chip Power-On Configuration Bit [2], Input
107	ND[3]	IOU	NAND	NAND Interface Data Bit [3]
	CFG[3]	IU	SYSTEM	Chip Power-On Configuration Bit [3], Input
108	ND[4]	IOU	NAND	NAND Interface Data Bit [4]
	CFG[4]	IU	SYSTEM	Chip Power-On Configuration Bit [4], Input
109	ND[5]	IOU	NAND	NAND Interface Data Bit [5]
	CFG[5]	IU	SYSTEM	Chip Power-On Configuration Bit [5], Input
110	ND[6]	IOU	NAND	NAND Interface Data Bit [6]
	CFG[6]	IU	SYSTEM	Chip Power-On Configuration Bit [6], Input

111	ND[7]	IOU	NAND	NAND Interface Data Bit [7]
	CFG[7]	IU	SYSTEM	Chip Power-On Configuration Bit [7], Input
112	NBUSY1_	IU	NAND	NAND Interface Busy 1, Input, Low Active
	GPD[6]	IOU	GPIOD	GPIO Port D Bit 6
	SD2_DAT[2]	IOU	SD2	SD Port 2 Data Bit 2
113	NBUSY0_	IU	NAND	NAND Interface Busy 0, Input, Low Active
	GPD[5]	IOU	GPIOD	GPIO Port D Bit 5
	SD2_DAT[3]	IOU	SD2	SD Port 2 Data Bit 3
114	NWR_	OU	NAND	NAND Interface Write Enable, Output, Low Active
	GPD[8]	IOU	GPIOD	GPIO Port D Bit 8
	SD2_CMD	IOU	SD2	SD Port 2 Command/Response
115	NRE_	OU	NAND	NAND Interface Read Enable, Output, Low Active
	GPD[7]	IOU	GPIOD	GPIO Port D Bit 7
	SD2_CLK	OU	SD2	SD Port 2 Clock, Output
116	NCLE	OU	NAND	NAND Interface Command-Latch-Enable, Output, High Active
	GPE[11]	IOU	GPIOE	GPIO Port E Bit 11
117	NALE	OU	NAND	NAND Interface Address-Latch-Enable, Output, High Active
	GPE[10]	IOU	GPIOE	GPIO Port E Bit 10
118	NCS1_	OU	NAND	NAND Interface Chip Select 1, Output, Low Active
	GPE[9]	IOU	GPIOE	GPIO Port E Bit 9
	SD2_DAT[0]	IOU	SD2	SD Port 2 Data Bit 0
119	VSS	G	GND	Ground (0V)
120	NCS0_	IU	NAND	NAND Interface Chip Select 0, Output, Low Active
	GPE[8]	IOU	GPIOE	GPIO Port E Bit 8
	SD2_DAT[1]	IOU	SD2	SD Port 2 Data Bit 1
121	VDD33	P	I/O	I/O Power (3.3V)
122	URTXD	OU	UART	UART TX Data, Output
	GPA[10]	IOU	GPIOA	GPIO Port A Bit 10
	SPI1_CS1_	OU	SPI1	SPI Port 1 Device Select 1, Output, Low Active
123	URRXD	IU	UART	UART RX Data, Input
	GPA[11]	IOU	GPIOA	GPIO Port A Bit 11
	LMVSYNC	OU	LCD	MPU LCD Interface VSYNC, Output
	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
124	SPDATA[1]	IU	CAP	Sensor Interface Data Bit 1, Input
	GPB[6]	IOU	GPIOB	GPIO Port B Bit 6

	I2S_DIN	IU	I²S	I2S Interface Data Input
125	SPDATA[0]	IU	CAP	Sensor Interface Data Bit 0, Input
	GPB[5]	IOU	GPIOB	GPIO Port B Bit 5
	I2S_DOUT	OU	I2S	I2S Interface Data Output
	SD1_DAT[2]	IOU	SD1	SD Port 1 Data Bit 2
126	SFIELD	IU	CAP	Sensor Interface Even/ODD Field Indicator, Input
	GPB[4]	IOU	GPIOB	GPIO Port B Bit 4
	I2S_WS	OU	I²S	I2S Interface Word Select, Output
	SD1_DAT[3]	IOU	SD1	SD Port 1 Data Bit 3
127	SVSYNC	IU	CAP	Sensor Interface VSYNC, Input
	GPB[3]	IOU	GPIOB	GPIO Port B Bit 3
	I2S_BCLK	IU	I²S	I2S Interface Clock, Input
	SD1_CMD	IOU	SD1	SD Port 1 Command/Response
128	SHSYNC	IU	CAP	Sensor Interface HSYNC, Input
	GPB[2]	IOU	GPIOB	GPIO Port B Bit 2
	I2S_MCLK	OU	I²S	Clock to I2S Codec, Output
	SD1_CLK	OU	SD1	SD Port 1 Clock, Output

4.2 N32901R1DN, N32903R5DN and N32905R3DN Pin Description

Pin No	Name	Type	Group	Description
1	SPI0_CS0_	IOU	SPI0	SPI Port 0 Device Select 0, Low Active;Output in Master Mode;Input in Slave Mode
	GPD[13]	IOU	GPIOD	GPIO Port D Bit 13
2	SPI0_DI	IU	SPI0	SPI Port 0 Data Input
	GPD[14]	IOU	GPIOD	GPIO Port D Bit 14
3	SPI0_DO	OU	SPI0	SPI Port 0 Data Output
	GPD[15]	IOU	GPIOD	GPIO Port D Bit 15
4	SD0_DAT[2]	IOU	SD0	SD Port 0 Data Bit 2
	GPE[4]	IOU	GPIOE	GPIO Port E Bit 4
5	SD0_DAT[3]	IOU	SD0	SD Port 0 Data Bit 3
	GPE[5]	IOU	GPIOE	GPIO Port E Bit 5
6	SD0_CMD	IOU	SD0	SD Port 0 Command/Response
	GPE[6]	IOU	GPIOE	GPIO Port E Bit 6
7	SD0_CLK	OU	SD0	SD Port 0 Clock, Output
	GPE[7]	IOU	GPIOE	GPIO Port E Bit 7

8	SD0_DAT[0]	IOU	SD0	SD Port 0 Data Bit 0
	GPE[2]	IOU	GPIOE	GPIO Port E Bit 2
9	SD0_DAT[1]	IOU	SD0	SD Port 0 Data Bit 1
	GPE[3]	IOU	GPIOE	GPIO Port E Bit 3
10	XIN	I	XTAL	12MHz Crystal Input
11	XOUT	O	XTAL	12MHz Crystal Output
12	MVREF	P	MVDD	1/2 MVDD (0.9V) for DDR_VREF, when N32903R5DN or N32905R3 are installation
	VSSQ	G	MVDD	SDRAM I/F Ground (0V), when N32901R1DN is installation
13	PLL_UD_VDD18	P	PLL & USB	PLL & USB2.0 Device Core Power (1.8V)
14	UD_DM	I/O	USB	USB 2.0 Device D-.
15	UD_DP	I/O	USB	USB 2.0 Device D+.
16	UD_VDD33	P	USB	USB 2.0 Device PHY 3.3V
17	UD_REXT	O	USB	External Resistor 12.1K resistor connected to ground
18	VSS	G	GND	Ground (0V)
19	GPC[15]	IOU	GPIOC	GPIO Port C Bit 15
	SPDATA[7]	IU	CAP	Sensor Interface Data Bit 7, Input
20	GPC[14]	IOU	GPIOC	GPIO Port C Bit 14
	SPDATA[6]	IU	CAP	Sensor Interface Data Bit 6, Input
21	GPC[13]	IOU	GPIOC	GPIO Port C Bit 13
	SPDATA[5]	IU	CAP	Sensor Interface Data Bit 5, Input
22	GPC[12]	IOU	GPIOC	GPIO Port C Bit 12
	SPDATA[4]	IU	CAP	Sensor Interface Data Bit 4, Input
23	GPC[11]	IOU	GPIOC	GPIO Port C Bit 11
	SPDATA[3]	IU	CAP	Sensor Interface Data Bit 3, Input
24	GPC[10]	IOU	GPIOC	GPIO Port C Bit 10
	SPDATA[2]	IU	CAP	Sensor Interface Data Bit 2, Input
25	GPC[9]	IOU	GPIOC	GPIO Port C Bit 9
	SPDATA[1]	IU	CAP	Sensor Interface Data Bit 1, Input
26	GPC[8]	IOU	GPIOC	GPIO Port C Bit 8
	SPDATA[0]	IU	CAP	Sensor Interface Data Bit 0, Input
27	VDD18	P	Core	Core Logic Power (1.8V)
28	VDD33	P	I/O	I/O Power (3.3V)
29	ADC_VSS33	G	ADC	ADC Ground (0V)
30	ADC_VDD33	P	ADC	ADC Power (3.3V)

31	ADC_AIN[0]	I	ADC	ADC MIC+
32	ADC_AIN[1]	I	ADC	ADC MIC-
33	ADC_AIN[2]	I	ADC	ADC Analog Input Channel 2
34	GPA[5]	IOU	GPIOA	GPIO Port A Bit 5
	SPI0_CS1_	OU	SPI0	SPI Port 0 Device Select 1, Output, Low Active
35	GPA[4]	IOU	GPIOA	GPIO Port A Bit 4
	UHL_DM1	IOU	USB	USB Host 1.0 Lite Port 1, D-
36	GPA[3]	IOU	GPIOA	GPIO Port A Bit 3
	UHL_DP1	IOU	USB	USB Host 1.0 Lite Port 1, D+
37	GPA[1]	IOU	GPIOA	GPIO Port A Bit 1
	SD_CD_	IU	SD	SD Card Detect, Input, Low Active
38	RST_	IU	SYSTEM	System Reset, Input, Low Active
	WDT_RST_	OU	SYSTEM	Watch-Dog Reset, Output, Low Active
39	GPD[1]	IOU	GPIOD	GPIO Port D Bit 1
	HUR_TXD	OU	UART	High-Speed UART TX Data, Output
	PWM1	OU	PWM	PWM Channel 1
40	GPD[2]	IOU	GPIOD	GPIO Port D Bit 2
	HUR_RXD	IU	UART	High-Speed UART RX Data, Input
	PWM2	OU	PWM	PWM Channel 2
41	UD_CDET	I	USB	USB Device Connect Detect, Input, High Active
42	VDD18	P	Core	Core Logic Power (1.8V)
43	MVREF	P	MVDD	1/2 MVDD (0.9V) for DDR_VREF, when N32903R5DN or N32905R3 are installation
	MVSS	G	MVDD	SDRAM I/F Ground (0V), when N32901R1DN is installation
44	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903R5DN or N32905R3DN are installation MVDD=3.3V powered when N32901R1DN is installation
45	ADAC_HPVSS33	G	AUDIO	Audio DAC Headphone Driver Ground (0V)
46	ADAC_HPVDD33	P	AUDIO	Audio DAC Headphone Driver Power (3.3V)
47	ADAC_HPOUT_L	O	AUDIO	Audio Headphone Left Channel Output
48	ADAC_HPOUT_R	O	AUDIO	Audio Headphone Right Channel Output
49	ADAC_AVSS33	G	AUDIO	Audio DAC Ground (0V)
50	ADAC_VREF	O	AUDIO	Audio DAC Reference Voltage Output, please connect 1uF capacitor to DAC ground

51	ADAC_AVDD33	P	AUDIO	Audio DAC Power (3.3V)
52	VDD18	P	Core	Core Logic Power (1.8V)
53	GPA[7]	IOU	GPIOA	GPIO Port A Bit 7
	CFG[0]	IU	SYSTEM	Chip Power-On Configuration Bit [0], Input
54	VDD33	P	I/O	I/O Power (3.3V)
55	URTXD	OU	UART	UART TX Data, Output
	GPA[10]	IOU	GPIOA	GPIO Port A Bit 10
	SPI1_CS1_	OU	SPI1	SPI Port 1 Device Select 1, Output, Low Active
56	URRXD	IU	UART	UART RX Data, Input
	GPA[11]	IOU	GPIOA	GPIO Port A Bit 11
	LMVSYNC	OU	LCD	MPU LCD Interface VSYNC, Output
	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
57	SPDATA[1]	IU	CAP	Sensor Interface Data Bit 1, Input
	GPB[6]	IOU	GPIOB	GPIO Port B Bit 6
	I2S_DIN	IU	I²S	I2S Interface Data Input
58	SPDATA[0]	IU	CAP	Sensor Interface Data Bit 0, Input
	GPB[5]	IOU	GPIOB	GPIO Port B Bit 5
	I2S_DOUT	OU	I2S	I2S Interface Data Output
	SD1_DAT[2]	IOU	SD1	SD Port 1 Data Bit 2
59	SFIELD	IU	CAP	Sensor Interface Even/ODD Field Indicator, Input
	GPB[4]	IOU	GPIOB	GPIO Port B Bit 4
	I2S_WS	OU	I²S	I2S Interface Word Select, Output
	SD1_DAT[3]	IOU	SD1	SD Port 1 Data Bit 3
60	SVSYNC	IU	CAP	Sensor Interface VSYNC, Input
	GPB[3]	IOU	GPIOB	GPIO Port B Bit 3
	I2S_BCLK	IU	I²S	I2S Interface Clock, Input
	SD1_CMD	IOU	SD1	SD Port 1 Command/Response
61	SHSYNC	IU	CAP	Sensor Interface HSYNC, Input
	GPB[2]	IOU	GPIOB	GPIO Port B Bit 2
	I2S_MCLK	OU	I²S	Clock to I2S Codec, Output
	SD1_CLK	OU	SD1	SD Port 1 Clock, Output
62	SPCLK	IOU	CAP	Sensor Interface Pixel Clock, Input
	GPB[1]	IOU	GPIOB	GPIO Port B Bit 1
	SD1_DAT[0]	IOU	SD1	SD Port 1 Data Bit 0
	UHL_DM1	IOU	USB	USB Host 1.0 Lite Port 1, D-E154

63	SCLKO	OU	CAP	Clock to Sensor Module, Output
	GPB[0]	IOU	JTAG	GPIO Port B Bit 0
	SD1_DAT[1]	IOU	SD1	SD Port 1 Data Bit 1
	UHL_DP1	IOU	USB	USB Host 1.0 Lite Port 1, D+
64	SPI0_CLK	IOU	SPI0	SPI Port 0 Clock;Output in Master Mode;Input in Slave Mode
	GPD[12]	IOU	GPIOD	GPIO Port D Bit 12
EPAD	VSS	G	GND	Ground (0V), EPAD is for TQFP package and used for N32903R5DN & N32905R3DN

4.3 N3290xKxDN series Pin Description

Pin No	Name	Type	Group	Description
1	SHSYNC	IU	CAP	Sensor Interface HSYNC, Input
	GPB[2]	IOU	GPIOB	GPIO Port B Bit 2
	I2S_MCLK	OU	I²S	Clock to I2S Codec, Output
	SD1_CLK	OU	SD1	SD Port 1 Clock, Output
2	SPCLK	IOU	CAP	Sensor Interface Pixel Clock, Input
	GPB[1]	IOU	GPIOB	GPIO Port B Bit 1
	SD1_DAT[0]	IOU	SD1	SD Port 1 Data Bit 0
	UHL_DM1	IOU	USB	USB Host 1.0 Lite Port 1, D-E154
3	SCLKO	OU	CAP	Clock to Sensor Module, Output
	GPB[0]	IOU	JTAG	GPIO Port B Bit 0
	SD1_DAT[1]	IOU	SD1	SD Port 1 Data Bit 1
	UHL_DP1	IOU	USB	USB Host 1.0 Lite Port 1, D+
4	ISDA	IOU	I2C	I2C Interface Data
	GPB[14]	IOU	GPIOB	GPIO Port B Bit 14
	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
	LMVSYNC	OU	LCD	MPU LCD Interface Mode VSYNC, Output
5	ISCK	OU	I2C	I2C Interface Clock, Output
	GPB[13]	IOU	GPIOB	GPIO Port B Bit 13
6	SPI0_CLK	IOU	SPI0	SPI Port 0 Clock;Output in Master Mode;Input in Slave Mode
	GPD[12]	IOU	GPIOD	GPIO Port D Bit 12
7	SPI0_CS0_	IOU	SPI0	SPI Port 0 Device Select 0, Low Active;Output in Master Mode;Input in Slave Mode
	GPD[13]	IOU	GPIOD	GPIO Port D Bit 13
8	SPI0_DI	IU	SPI0	SPI Port 0 Data Input
	GPD[14]	IOU	GPIOD	GPIO Port D Bit 14
9	SPI0_DO	OU	SPI0	SPI Port 0 Data Output
	GPD[15]	IOU	GPIOD	GPIO Port D Bit 15
10	SD0_DAT[2]	IOU	SD0	SD Port 0 Data Bit 2
	GPE[4]	IOU	GPIOE	GPIO Port E Bit 4
11	SD0_DAT[3]	IOU	SD0	SD Port 0 Data Bit 3

	GPE[5]	IOU	GPIOE	GPIO Port E Bit 5
12	SD0_CMD	IOU	SD0	SD Port 0 Command/Response
	GPE[6]	IOU	GPIOE	GPIO Port E Bit 6
13	SD0_CLK	OU	SD0	SD Port 0 Clock, Output
	GPE[7]	IOU	GPIOE	GPIO Port E Bit 7
14	SD0_DAT[0]	IOU	SD0	SD Port 0 Data Bit 0
	GPE[2]	IOU	GPIOE	GPIO Port E Bit 2
15	SD0_DAT[1]	IOU	SD0	SD Port 0 Data Bit 1
	GPE[3]	IOU	GPIOE	GPIO Port E Bit 3
16	XIN	I	XTAL	12MHz Crystal Input
17	XOUT	O	XTAL	12MHz Crystal Output
18	VDD18	P	Core	Core Logic Power (1.8V)
19	VSSQ	G	MVDD	SDRAM I/F Ground (0V)
20	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903K5DN or N32905K5DN are installation MVDD=3.3V powered when N32901K3DN is installation
21	VSSQ	G	MVDD	SDRAM Ground (0V)
22	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903K5DN or N32905K5DN are installation MVDD=3.3V powered when N32901K3DN is installation
23	VSS	G	GND	Ground (0V)
24	NC	--	NC	when N32901K3DN is installation
	MVREF	P	MVDD	1/2 MVDD (0.9V) for DDR_VREF, when N32903K5DN or N32905K5DN are installation
25	PLL_UD_VDD18	P	PLL & USB	PLL & USB2.0 Device Core Power (1.8V)
26	UD_VSS	G	USB	USB2.0 Device Ground (0V)
27	UD_DM	I/O	USB	USB 2.0 Device D-.
28	UD_DP	I/O	USB	USB 2.0 Device D+.
29	UD_VDD33	P	USB	USB 2.0 Device PHY 3.3V
30	UD_REXT	O	USB	External Resistor 12.1K resistor connected to ground

31	LVDATA[17]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 17
	SVSYNC	IU	CAP	Sensor Interface VSYNC, Input
	GPE[1]	IOU	GPIOE	GPIO Port E Bit 1
32	LVDATA[16]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 16
	SHSYNC	IU	CAP	Sensor Interface HSYNC, Input
	GPE[0]	IOU	GPIOE	GPIO Port E Bit 0
33	LVDATA[15]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 15
	GPC[15]	IOU	GPIOC	GPIO Port C Bit 15
	SPDATA[7]	IU	CAP	Sensor Interface Data Bit 7, Input
	KPI_SI[7]	IU	KPI	KPI Scan In Bit 7
34	LVDATA[14]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 14
	GPC[14]	IOU	GPIOC	GPIO Port C Bit 14
	SPDATA[6]	IU	CAP	Sensor Interface Data Bit 6, Input
	KPI_SI[6]	IU	KPI	KPI Scan In Bit 6
35	LVDATA[13]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 13
	GPC[13]	IOU	GPIOC	GPIO Port C Bit 13
	SPDATA[5]	IU	CAP	Sensor Interface Data Bit 5, Input
	KPI_SI[5]	IU	KPI	KPI Scan In Bit 5
36	LVDATA[12]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 12
	GPC[12]	IOU	GPIOC	GPIO Port C Bit 12
	SPDATA[4]	IU	CAP	Sensor Interface Data Bit 4, Input
	KPI_SI[4]	IU	KPI	KPI Scan In Bit 4
37	LVDATA[11]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 11
	GPC[11]	IOU	GPIOC	GPIO Port C Bit 11
	SPDATA[3]	IU	CAP	Sensor Interface Data Bit 3, Input
	KPI_SI[3]	IU	KPI	KPI Scan In Bit 3
38	LVDATA[10]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 10
	GPC[10]	IOU	GPIOC	GPIO Port C Bit 10
	SPDATA[2]	IU	CAP	Sensor Interface Data Bit 2, Input
	KPI_SI[2]	IU	KPI	KPI Scan In Bit 2
39	LVDATA[9]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 9
	GPC[9]	IOU	GPIOC	GPIO Port C Bit 9
	SPDATA[1]	IU	CAP	Sensor Interface Data Bit 1, Input

	KPI_SI[1]	IU	KPI	KPI Scan In Bit 1
40	LVDATA[8]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 8
	GPC[8]	IOU	GPIOC	GPIO Port C Bit 8
	SPDATA[0]	IU	CAP	Sensor Interface Data Bit 0, Input
	KPI_SI[0]	IU	KPI	KPI Scan In Bit 0
41	LVDATA[7]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 7
	GPC[7]	IOU	GPIOC	GPIO Port C Bit 7
42	LVDATA[6]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 6
	GPC[6]	IOU	GPIOC	GPIO Port C Bit 6
	CFG[10]	IU	SYSTEM	Chip Power-On Configuration Bit [10], Input
43	LVDATA[5]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 5
	GPC[5]	IOU	GPIOC	GPIO Port C Bit 5
	CFG[9]	IU	SYSTEM	Chip Power-On Configuration Bit [9], Input
44	LVDATA[4]	IOU	LCD	GPIO Port C Bit 4
	GPC[4]	IOU	GPIOC	GPIO Port C Bit 4
	CFG[8]	IU	SYSTEM	Chip Power-On Configuration Bit [8], Input
45	LVDATA[3]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 3
	GPC[3]	IOU	GPIOC	GPIO Port C Bit 3
46	LVDATA[2]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 2
	GPC[2]	IOU	GPIOC	GPIO Port C Bit 2
47	LVDATA[1]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 1
	GPC[1]	IOU	GPIOC	GPIO Port C Bit 1
48	LVDATA[0]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 0
	GPC[0]	IOU	GPIOC	GPIO Port C Bit 0
49	LVDE	OU	LCD	SYNC LCD Interface Data Enable, Output, High Active
	LRS	OU	LCD	MPU LCD Interface Register Select
	GPD[11]	IOU	GPIOD	GPIO Port D Bit 11 Note. By design limitation, GPD[11] function will be disable when SPI1 is used.
50	LVSYNC	OU	LCD	SYNC LCD Interface VSYNC, Output, High Active
	LRD	OU	LCD	MPU I80 mode LCD Interface Read, active low
	LEN	OU	LCD	MPU M68 mode LCD Interface Read Write Enable/Disable , High Enable
	GPD[10]	IOU	GPIOD	LCD Interface Data Enable, High Active.

51	VSS	G	GND	Ground (0V)
52	LHSYNC	OU	LCD	SYNC LCD Interface HSYNC, Output, High Active
	LWR	OU	LCD	MPU I80 mode LCD Interface Write, active low
	LR/W	OU	LCD	MPU M68 mode LCD interface R/W, High is read command and Low is write instruction
	GPD[9]	IOU	GPIOD	GPIO Port D Bit 9
53	VDD18	P	Core	Core Logic Power (1.8V)
54	LPCLK	OU	LCD	SYNC LCD Interface Pixel Clock, Output
	LCS	OU	LCD	MPU LCD Interface Chip Enable, active low
	GPB[15]	IOU	GPIOB	GPIO Port B Bit 15
55	VDD33	P	I/O	I/O Power (3.3V)
56	ADC_VSS33	G	ADC	ADC Ground (0V)
57	ADC_TP_YM	I	ADC	Touch Panel YM
58	ADC_TP_XM	I	ADC	Touch Panel XM
59	ADC_TP_XP	I	ADC	Touch Panel XP
60	ADC_TP_YP	I	ADC	Touch Panel YP
61	ADC_VDD33	P	ADC	ADC Power (3.3V)
62	ADC_AIN[2]	I	ADC	ADC Analog Input Channel 2
63	ADC_AIN[3]	I	ADC	ADC Analog Input Channel 3
64	ADC_AIN[4]	I	ADC	ADC Analog Input Channel 4
65	RTC_XOUT	O	RTC	32768Hz Crystal Output
66	RTC_XIN	I	RTC	32768Hz Crystal Input
67	RTC_VDD1.8V	P	RTC	RTC Power (1.8V)
68	VDD33	P	I/O	I/O Power (3.3V)
69	GPA[6]	IOU	GPIOA	GPIO Port A Bit 6
	SPI1_CS1_	OU	SPI1	SPI Port 1 Device Select 1, Output, Low Active
	KPI_SO[4]	OU	KPI	KPI Scan Out Bit 4
70	GPA[5]	IOU	GPIOA	GPIO Port A Bit 5
	SPI0_CS1_	OU	SPI0	SPI Port 0 Device Select 1, Output, Low Active
	KPI_SO[3]	OU	KPI	KPI Scan Out Bit 3
71	GPA[4]	IOU	GPIOA	GPIO Port A Bit 4
	UHL_DM1	IOU	USB	USB Host 1.0 Lite Port 1, D-
	KPI_SO[2]	OU	KPI	KPI Scan Out Bit 2

72	GPA[3]	IOU	GPIOA	GPIO Port A Bit 3
	UHL_DP1	IOU	USB	USB Host 1.0 Lite Port 1, D+
	KPI_SO[1]	OU	KPI	KPI Scan Out Bit 1
73	GPA[2]	IOU	GPIOA	GPIO Port A Bit 2
	LMVSYNC	OU	LCD	MPU LCD Interface VSYNC, Output
	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
	KPI_SO[0]	OU	KPI	KPI Scan Out Bit 0
74	GPA[1]	IOU	GPIOA	GPIO Port A Bit 1
	SD_CD_	IU	SD	SD Card Detect, Input, Low Active
75	GPA[0]	IOU	GPIOA	GPIO Port A Bit 0
76	RST_	IU	SYSTEM	System Reset, Input, Low Active
	WDT_RST_	OU	SYSTEM	Watch-Dog Reset, Output, Low Active
77	TCK	ID	JTAG	JTAG Interface Test Clock, Input
	GPD[0]	IOD	GPIOD	GPIO Port D Bit 0
	SPI1_CS1_	OD	SPI1	SPI Port 1 Device Select 1, Output, Low Active
	PWM0	OD	PWM	PWM Channel 0
78	TMS	IU	JTAG	JTAG Interface Test Mode Select, Input
	GPD[1]	IOU	GPIOD	GPIO Port D Bit 1
	HUR_TXD	OU	UART	High-Speed UART TX Data, Output
	PWM1	OU	PWM	PWM Channel 1
79	TDI	IU	JTAG	JTAG Interface Test Data In, Input
	GPD[2]	IOU	GPIOD	GPIO Port D Bit 2
	HUR_RXD	IU	UART	High-Speed UART RX Data, Input
	PWM2	OU	PWM	PWM Channel 2
80	TDO	OU	JTAG	JTAG Interface Test Data Out, Output
	GPD[3]	IOU	GPIOD	GPIO Port D Bit 3
	HUR_CTS	IU	UART	High-Speed UART Clear-To-Send, Input, Low Active
	PWM3	OU	PWM	PWM Channel 3
81	TRST_	IU	JTAG	JTAG Interface Test Reset, Input, Low Active
	GPD[4]	IOU	GPIOD	GPIO Port D Bit 4
	HUR_RTS	OU	UART	High-Speed UART Reset-To-Send, Output, Low Active
	SPI0_CS1_	OU	SPI0	SPI Port 0 Device Select 1, Output, Low Active
82	UD_CDET	I	USB	USB Device Connect Detect, Input, High Active

83	VDD18	P	Core	Core Logic Power (1.8V)
84	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903K5DN or N32905K5DN are installation MVDD=3.3V powered when N32901K3DN is installation
85	MVSS	G	MVDD	SDRAM I/F Ground (0V)
86	MVREF	P	MVDD	1/2 MVDD (0.9V) for DDR_VREF, when N32903K5DN or N32905K5DN are installation
	NC	--	NC	when N32901K3DN is installation
87	VSSQ	G	MVDD	SDRAM Ground (0V)
88	MVDD	P	MVDD	SDRAM Power, please follow that: MVDD=1.8V powered when N32903K5DN or N32905K5DN are installation MVDD=3.3V powered when N32901K3DN is installation
89	VDD33	P	I/O	I/O Power (3.3V)
90	ADAC_HPVSS33	G	AUDIO	Audio DAC Headphone Driver Ground (0V)
91	ADAC_HPVDD33	P	AUDIO	Audio DAC Headphone Driver Power (3.3V)
92	ADAC_HPOUT_L	O	AUDIO	Audio Headphone Left Channel Output
93	ADAC_HPOUT_R	O	AUDIO	Audio Headphone Right Channel Output
94	ADAC_AVSS33	G	AUDIO	Audio DAC Ground (0V)
95	ADAC_VREF	O	AUDIO	Audio DAC Reference Voltage Output, please connect 1uF capacitor to DAC ground
96	ADAC_AVDD33	P	AUDIO	Audio DAC Power (3.3V)
97	VDD18	P	Core	Core Logic Power (1.8V)
98	GPA[7]	IOU	GPIOA	GPIO Port A Bit 7
	KPI_SO[5]	OU	KPI	KPI Scan Out Bit 5
99	ND[0]	IOU	NAND	NAND Interface Data Bit [0]
	CFG[0]	IU	SYSTEM	Chip Power-On Configuration Bit [0], Input
100	ND[1]	IOU	NAND	NAND Interface Data Bit [1]
	CFG[1]	IU	SYSTEM	Chip Power-On Configuration Bit [1], Input
101	ND[2]	IOU	NAND	NAND Interface Data Bit [2]
	CFG[2]	IU	SYSTEM	Chip Power-On Configuration Bit [2], Input

102	ND[3]	IOU	NAND	NAND Interface Data Bit [3]
	CFG[3]	IU	SYSTEM	Chip Power-On Configuration Bit [3], Input
103	ND[4]	IOU	NAND	NAND Interface Data Bit [4]
	CFG[4]	IU	SYSTEM	Chip Power-On Configuration Bit [4], Input
104	ND[5]	IOU	NAND	NAND Interface Data Bit [5]
	CFG[5]	IU	SYSTEM	Chip Power-On Configuration Bit [5], Input
105	ND[6]	IOU	NAND	NAND Interface Data Bit [6]
	CFG[6]	IU	SYSTEM	Chip Power-On Configuration Bit [6], Input
106	ND[7]	IOU	NAND	NAND Interface Data Bit [7]
	CFG[7]	IU	SYSTEM	Chip Power-On Configuration Bit [7], Input
107	NBUSY1_	IU	NAND	NAND Interface Busy 1, Input, Low Active
	GPD[6]	IOU	GPIOD	GPIO Port D Bit 6
	SD2_DAT[2]	IOU	SD2	SD Port 2 Data Bit 2
108	NBUSY0_	IU	NAND	NAND Interface Busy 0, Input, Low Active
	GPD[5]	IOU	GPIOD	GPIO Port D Bit 5
	SD2_DAT[3]	IOU	SD2	SD Port 2 Data Bit 3
109	NWR_	OU	NAND	NAND Interface Write Enable, Output, Low Active
	GPD[8]	IOU	GPIOD	GPIO Port D Bit 8
	SD2_CMD	IOU	SD2	SD Port 2 Command/Response
110	NRE_	OU	NAND	NAND Interface Read Enable, Output, Low Active
	GPD[7]	IOU	GPIOD	GPIO Port D Bit 7
	SD2_CLK	OU	SD2	SD Port 2 Clock, Output
111	NCLE	OU	NAND	NAND Interface Command-Latch-Enable, Output, High Active
	GPE[11]	IOU	GPIOE	GPIO Port E Bit 11
112	NALE	OU	NAND	NAND Interface Address-Latch-Enable, Output, High Active
	GPE[10]	IOU	GPIOE	GPIO Port E Bit 10
113	NCS1_	OU	NAND	NAND Interface Chip Select 1, Output, Low Active
	GPE[9]	IOU	GPIOE	GPIO Port E Bit 9
	SD2_DAT[0]	IOU	SD2	SD Port 2 Data Bit 0
114	VSS	G	GND	Ground (0V)
115	NCS0_	IU	NAND	NAND Interface Chip Select 0, Output, Low Active
	GPE[8]	IOU	GPIOE	GPIO Port E Bit 8
	SD2_DAT[1]	IOU	SD2	SD Port 2 Data Bit 1

116	VDD33	P	I/O	I/O Power (3.3V)
117	URTXD	OU	UART	UART TX Data, Output
	GPA[10]	IOU	GPIOA	GPIO Port A Bit 10
	SPI1_CS1_	OU	SPI1	SPI Port 1 Device Select 1, Output, Low Active
118	URRXD	IU	UART	UART RX Data, Input
	GPA[11]	IOU	GPIOA	GPIO Port A Bit 11
	LMVSYNC	OU	LCD	MPU LCD Interface VSYNC, Output
	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
119	SPDATA[7]	IU	CAP	Sensor Interface Data Bit 7, Input
	GPB[12]	IOU	GPIOB	GPIO Port B Bit 12
	SPI1_DO	OU	SPI1	SPI Port 1 Data Output
	LVDATA[23]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 23
120	SPDATA[6]	IU	CAP	Sensor Interface Data Bit 6, Input
	GPB[11]	IOU	GPIOB	GPIO Port B Bit 11
	SPI1_DI	IU	SPI1	SPI Port 1 Data Input
	LVDATA[22]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 22
121	SPDATA[5]	IU	CAP	Sensor Interface Data Bit 5, Input
	GPB[10]	IOU	GPIOB	GPIO Port B Bit 10
	SPI1_CS0_	IOU	SPI1	SPI Port 1 Device Select 0, Low Active;Output in Master Mode;Input in Slave Mode
	LVDATA[21]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 21
122	SPDATA[4]	IU	CAP	Sensor Interface Data Bit 4, Input
	GPB[9]	IOU	GPIOB	GPIO Port B Bit 9
	SPI1_CLK	IOU	SPI1	SPI Port 1 Clock;Output in Master Mode;Input in Slave Mode
	LVDATA[20]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 20
123	SPDATA[3]	IU	CAP	Sensor Interface Data Bit 3, Input
	GPB[8]	IOU	GPIOB	GPIO Port B Bit 8
	LVDATA[19]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 19
124	SPDATA[2]	IU	CAP	Sensor Interface Data Bit 2, Input
	GPB[7]	IOU	GPIOB	GPIO Port B Bit 7
	LVDATA[18]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 18
125	SPDATA[1]	IU	CAP	Sensor Interface Data Bit 1, Input
	GPB[6]	IOU	GPIOB	GPIO Port B Bit 6

	I2S_DIN	IU	I²S	I2S Interface Data Input
126	SPDATA[0]	IU	CAP	Sensor Interface Data Bit 0, Input
	GPB[5]	IOU	GPIOB	GPIO Port B Bit 5
	I2S_DOUT	OU	I2S	I2S Interface Data Output
	SD1_DAT[2]	IOU	SD1	SD Port 1 Data Bit 2
127	SFIELD	IU	CAP	Sensor Interface Even/ODD Field Indicator, Input
	GPB[4]	IOU	GPIOB	GPIO Port B Bit 4
	I2S_WS	OU	I²S	I2S Interface Word Select, Output
	SD1_DAT[3]	IOU	SD1	SD Port 1 Data Bit 3
128	SVSYNC	IU	CAP	Sensor Interface VSYNC, Input
	GPB[3]	IOU	GPIOB	GPIO Port B Bit 3
	I2S_BCLK	IU	I²S	I2S Interface Clock, Input
	SD1_CMD	IOU	SD1	SD Port 1 Command/Response

4.4 N32901R7DN TQFP64 pin list

Pin No	Name	Type	Group	Description
1	SPI0_CLK	IOU	SPI0	SPI Port 0 Clock;Output in Master Mode;Input in Slave Mode
	GPD[12]	IOU	GPIOD	GPIO Port D Bit 12
2	SPI0_CS0_	IOU	SPI0	SPI Port 0 Device Select 0, Low Active;Output in Master Mode;Input in Slave Mode
	GPD[13]	IOU	GPIOD	GPIO Port D Bit 13
3	SPI0_DI	IU	SPI0	SPI Port 0 Data Input
	GPD[14]	IOU	GPIOD	GPIO Port D Bit 14
4	SPI0_DO	OU	SPI0	SPI Port 0 Data Output
	GPD[15]	IOU	GPIOD	GPIO Port D Bit 15
5	XIN	I	XTAL	12MHz Crystal Input
6	XOUT	O	XTAL	12MHz Crystal Output
7	VDD18	P	Core	Core Logic Power (1.8V)
8	MVDD33	P	MVDD33	SDRAM Power (3.3V)
9	PLL_UD_VDD18	P	PLL & USB	PLL & USB2.0 Device Core Power (1.8V)
10	UD_DM	I/O	USB	USB 2.0 Device D-.
11	UD_DP	I/O	USB	USB 2.0 Device D+.
12	UD_VDD33	P	USB	USB 2.0 Device PHY 3.3V
13	UD_REXT	O	USB	External Resistor 12.1K resistor connected to ground
14	LVDATA[15]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 15
	GPC[15]	IOU	GPIOC	GPIO Port C Bit 15
15	LVDATA[14]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 14
	GPC[14]	IOU	GPIOC	GPIO Port C Bit 14
16	LVDATA[13]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 13
	GPC[13]	IOU	GPIOC	GPIO Port C Bit 13
17	LVDATA[12]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 12
	GPC[12]	IOU	GPIOC	GPIO Port C Bit 12
18	LVDATA[11]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 11
	GPC[11]	IOU	GPIOC	GPIO Port C Bit 11
19	LVDATA[10]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 10
	GPC[10]	IOU	GPIOC	GPIO Port C Bit 10
20	LVDATA[9]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 9
	GPC[9]	IOU	GPIOC	GPIO Port C Bit 9
21	LVDATA[8]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 8

	GPC[8]	IOU	GPIOC	GPIO Port C Bit 8
22	LVDATA[7]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 7
	GPC[7]	IOU	GPIOC	GPIO Port C Bit 7
23	LVDATA[6]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 6
	GPC[6]	IOU	GPIOC	GPIO Port C Bit 6
24	LVDATA[5]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 5
	GPC[5]	IOU	GPIOC	GPIO Port C Bit 5
25	LVDATA[4]	IOU	LCD	GPIO Port C Bit 4
	GPC[4]	IOU	GPIOC	GPIO Port C Bit 4
26	LVDATA[3]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 3
	GPC[3]	IOU	GPIOC	GPIO Port C Bit 3
27	LVDATA[2]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 2
	GPC[2]	IOU	GPIOC	GPIO Port C Bit 2
28	LVDATA[1]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 1
	GPC[1]	IOU	GPIOC	GPIO Port C Bit 1
29	LVDATA[0]	IOU	LCD	SYNC/MPU LCD Interface Data Bit 0
	GPC[0]	IOU	GPIOC	GPIO Port C Bit 0
30	LVDE	OU	LCD	SYNC LCD Interface Data Enable, Output, High Active
	LRS	OU	LCD	MPU LCD Interafec Register Select
	GPD[11]	IOU	GPIOD	GPIO Port D Bit 11
31	LVSYNC	OU	LCD	SYNC LCD Interface VSYNC, Output, High Active
	LRD	OU	LCD	MPU I80 mode LCD Interface Read, active low
	GPD[10]	IOU	GPIOD	LCD Interface Data Enable, High Active.
32	LHSYNC	OU	LCD	SYNC LCD Interface HSYNC, Output, High Active
	LWR	OU	LCD	MPU I80 mode LCD Interface Write, active low
	GPD[9]	IOU	GPIOD	GPIO Port D Bit 9
33	LPCLK	OU	LCD	SYNC LCD Interface Pixel Clock, Output
	LCS	OU	LCD	MPU LCD Interface Chip Enable, active low
	GPB[15]	IOU	GPIOB	GPIO Port B Bit 15
34	ADC_VDD33	P	ADC	ADC Power (3.3V)
35	RTC_VDD1.8V	P	RTC	RTC Power (1.8V)
36	VDD33	P	I/O	I/O Power (3.3V)
37	GPA[5]	IOU	GPIOA	GPIO Port A Bit 5
	SPI0_CS1_	OU	SPI0	SPI Port 0 Device Select 1, Output, Low Active
38	GPA[4]	IOU	GPIOA	GPIO Port A Bit 4

	UHL_DM1	IOU	USB	USB Host 1.0 Lite Port 1, D-
39	GPA[3]	IOU	GPIOA	GPIO Port A Bit 3
	UHL_DP1	IOU	USB	USB Host 1.0 Lite Port 1, D+
40	GPA[2]	IOU	GPIOA	GPIO Port A Bit 2
	LMVSYNC	OU	LCD	MPU LCD Interface VSYNC, Output
	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
41	RST_	IU	SYSTEM	System Reset, Input, Low Active
	WDT_RST_	OU	SYSTEM	Watch-Dog Reset, Output, Low Active
42	TCK	ID	JTAG	JTAG Interface Test Clock, Input
	GPD[0]	IOD	GPIOD	GPIO Port D Bit 0
	SPI1_CS1_	OD	SPI1	SPI Port 1 Device Select 1, Output, Low Active
	PWM0	OD	PWM	PWM Channel 0
43	TMS	IU	JTAG	JTAG Interface Test Mode Select, Input
	GPD[1]	IOU	GPIOD	GPIO Port D Bit 1
	HUR_TXD	OU	UART	High-Speed UART TX Data, Output
	PWM1	OU	PWM	PWM Channel 1
44	TDI	IU	JTAG	JTAG Interface Test Data In, Input
	GPD[2]	IOU	GPIOD	GPIO Port D Bit 2
	HUR_RXD	IU	UART	High-Speed UART RX Data, Input
	PWM2	OU	PWM	PWM Channel 2
45	TDO	OU	JTAG	JTAG Interface Test Data Out, Output
	GPD[3]	IOU	GPIOD	GPIO Port D Bit 3
	PWM3	OU	PWM	PWM Channel 3
46	TRST_	IU	JTAG	JTAG Interface Test Reset, Input, Low Active
	GPD[4]	IOU	GPIOD	GPIO Port D Bit 4
	SPI0_CS1_	OU	SPI0	SPI Port 0 Device Select 1, Output, Low Active
47	UD_CDET	I	USB	USB Device Connect Detect, Input, High Active
48	VDD18	P	Core	Core Logic Power (1.8V)
49	MVDD33	P	MVDD33	SDRAM I/O Power (3.3V)
50	VDDQ	P	MVDD33	SDRAM Power (3.3V)
51	AVDD33	P	AUDIO	Audio DAC Power (3.3V)
52	VDD18	P	Core	Core Logic Power (1.8V)
53	GPA[7]	IOU	GPIOA	GPIO Port A Bit 7
	CFG[0]	OU	SYSTEM	Chip Power-On Configuration Bit [0], Input
54	GPD[6]	IOU	GPIOD	GPIO Port D Bit 6

	SD2_DAT[2]	IOU	SD2	SD Port 2 Data Bit 2
55	GPD[5]	IOU	GPIOD	GPIO Port D Bit 5
	SD2_DAT[3]	IOU	SD2	SD Port 2 Data Bit 3
56	GPD[8]	IOU	GPIOD	GPIO Port D Bit 8
	SD2_CMD	IOU	SD2	SD Port 2 Command/Response
57	GPD[7]	IOU	GPIOD	GPIO Port D Bit 7
	SD2_CLK	OU	SD2	SD Port 2 Clock, Output
58	GPE[9]	IOU	GPIOE	GPIO Port E Bit 9
	SD2_DAT[0]	IOU	SD2	SD Port 2 Data Bit 0
59	GPE[8]	IOU	GPIOE	GPIO Port E Bit 8
	SD2_DAT[1]	IOU	SD2	SD Port 2 Data Bit 1
60	VDD33	P	I/O	I/O Power (3.3V)
61	URTXD	OU	UART	UART TX Data, Output
	GPA[10]	IOU	GPIOA	GPIO Port A Bit 10
	SPI1_CS1_	OU	SPI1	SPI Port 1 Device Select 1, Output, Low Active
62	URRXD	IU	UART	UART RX Data, Input
	GPA[11]	IOU	GPIOA	GPIO Port A Bit 11
	LMVSYNC	OU	LCD	MPU LCD Interface VSYNC, Output
	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
63	ISDA	IOU	I2C	I2C Interface Data
	GPB[14]	IOU	GPIOB	GPIO Port B Bit 14
	LFMARK	IU	LCD	MPU LCD Interface Frame Mark, Input
	LMVSYNC	OU	LCD	MPU LCD Interface Mode VSYNC, Output
64	ISCK	OU	I2C	I2C Interface Clock, Output
	GPB[13]	IOU	GPIOB	GPIO Port B Bit 13
EPAD	VSS	P	GND	Ground (0V)

4.5 Pin Type Description

TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input / Output
IU	Input with internal pull high (50K)
OU	Output with internal pull high (50K)
IOU	Bi-direction with internal pull high (50K)
ID	Input with internal pull low (50K)
OD	Output with internal pull low (50K)
IOD	Bi-direction with internal pull low (50K)
P	Analog Power or Digital Power
G	Analog GND or Digital GND

5. ELECTRICAL SPECIFICATION

5.1 Absolute Maximum Rating

Parameters	Values
Ambient Temperature	-20 °C ~ 85 °C
Storage Temperature	-40 °C ~ 125 °C
Voltage On Any Pin	-0.3V ~ 3.6V
Power Supply Voltage (Core Logic)	-0.5V ~ 2.5V
Power Supply Voltage (I/O Buffer)	-0.5V ~ 4.6V
Injection Current (Latch-Up Testing)	100mA

5.2 DC Characteristics (Normal I/O)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD33	I/O Buffer Post-Driver Voltage		3.0	3.3	3.6	V
VDD18	Core Logic and I/O Buffer Pre-Driver Voltage	CPU=200MHz	1.62	1.8	1.98	V
MVDD33	SDRAM Operation Voltage (only for N32901x series)		3.0	3.3	3.6	V
MVDD18	DDR/DDR2 Operation Voltage (for N32903x/N32905x series)		1.7	1.8	1.9	V
RTC_VDD	RTC Power Supply		1.2	-	1.8	V
I_{RTC_VDD}	RTC Supply Current	RTC_VDD<VDD18	-	4	-	uA
V_{IH}	Input High Voltage		2.0	-	5.5	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
V_T	Threshold Point		1.45	1.58	1.74	V
V_{T+}	Schmitt Trigger Low to High Threshold Point		1.44	1.50	1.56	V
V_{T-}	Schmitt Trigger High to Low Threshold Point		0.89	0.94	0.99	V
I_{CC}	Core Power Supply Current	F_{CPU} = 200MHz, MCLK = 100MHz, VDD18 = 1.8V	-	160	-	mA
I_L	Input Leakage Current		-10	-	10	uA
I_{OZ}	Tri-State Output Leakage		-10	-	10	uA

	Current						
R_{PU}	Pull-Up Resistor			39	65	116	kΩ
R_{PD}	Pull-Down Resistor			40	56	108	kΩ
V_{OL}	Output Low Voltage			-	-	0.4	V
V_{OH}	Output High Voltage			2.4	-	-	V
I_{OL}	Low Level Output Current	4mA I/O	V_{OL} = 0.4V	-	4.0	-	mA
I_{OH}	High Level Output Current	4mA I/O	V_{OH} = 2.4V	-	5.9	-	mA

5.3 Audio DAC Characteristics

Test conditions: RL = 10K / 50pF, BW = 20Hz ~ 20KHz, Freq.= 1KHz, Sample Rate = 48KHz.

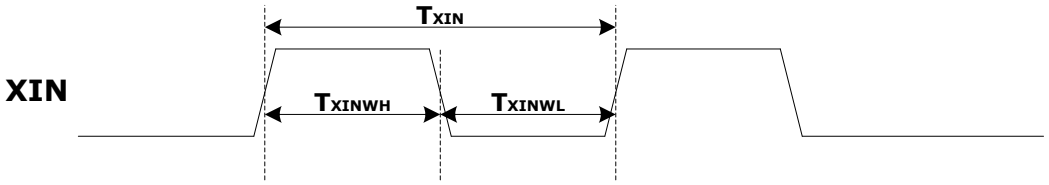
Parameter	Min	Typ	Max	Unit
Operating Voltage	3.0	3.3	3.6	V
Reference Voltage	-	DAC_VDD/2	-	V
Reference Capacitor	-	0.1	-	uF
Full Scale output voltage	-	0.74	-	Vrms
Full Scale output voltage	-	2.08	-	Vpp
Maximum Output Power	-	-	52	mW
Maximum Output Power @ 32ohm load	-	-	46	mW
Maximum Output Power @ 16ohm load	-	-	41	mW
L-Channel SNR	-	86	-	dBV
R-Channel SNR	-	85	-	dBV
L-Channel THD+N	-	-64	-	dB
R-Channel THD+N	-	-64	-	dB
L-Channel THD+N @ 32ohm load	-	-63	-	dB
R-Channel THD+N @ 32ohm load	-	-63	-	dB
L-Channel THD+N @ 16ohm load	-	-62	-	dB
R-Channel THD+N @ 16ohm load	-	-62	-	dB

5.4 ADC Characteristics

Parameter	Min.	Typ.	Max.	Unit
SAR ADC Input Voltage Range	3.0	-	3.6	V
Resolution of ADC	-	-	10	bit
Signal-to-Noise Plus Distortion of ADC from Line In	-	TBD	-	dB
Integral Non-Linearity of ADC	-	±2.0	-	LSB
Differential Non-Linearity of ADC	-	±0.8	-	LSB
No Missing Code	-	10	-	bit
AD Conversion Rate=ADCCLK/16	-	-	400	KHz

5.5 AC Characteristics (Digital Interface)

5.5.1 Clock Input Characteristics

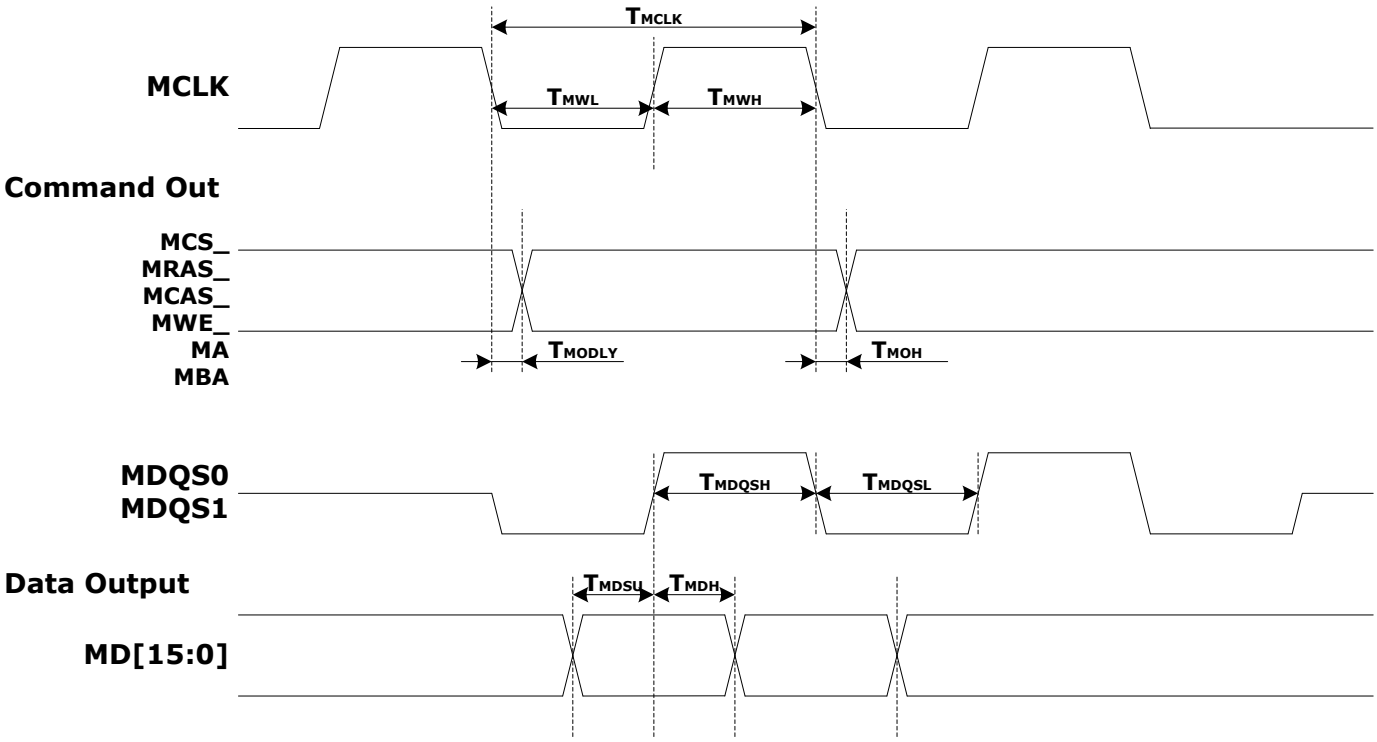


$F_{XIN} = 1 / T_{XIN}$

$XIN_{DUTY} = T_{XINWH} / (T_{XINWH} + T_{XINWL})$

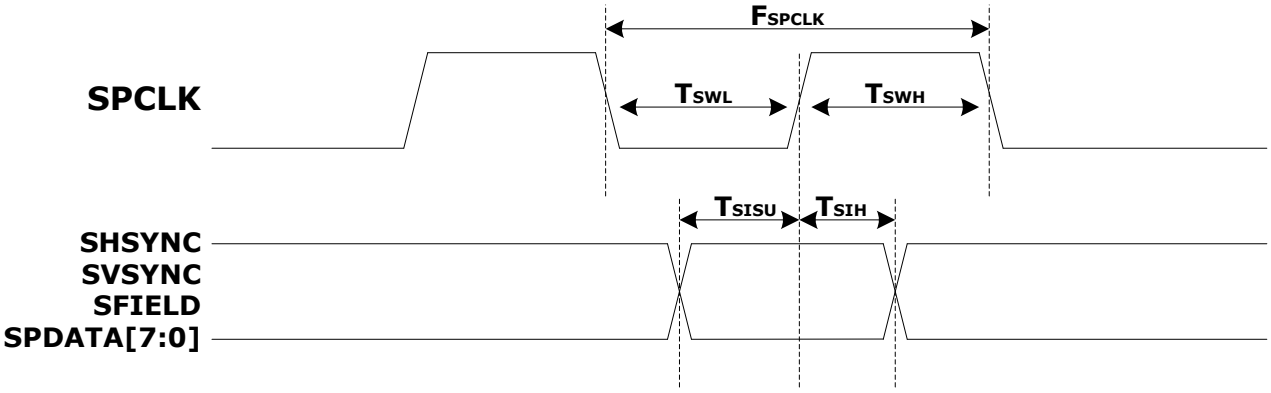
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{XIN}	Clock Input Frequency	-	12	-	MHz
XIN_{DUTY}	Clock Input Duty Cycle	45	50	55	%

5.5.2 SDRAM Interface



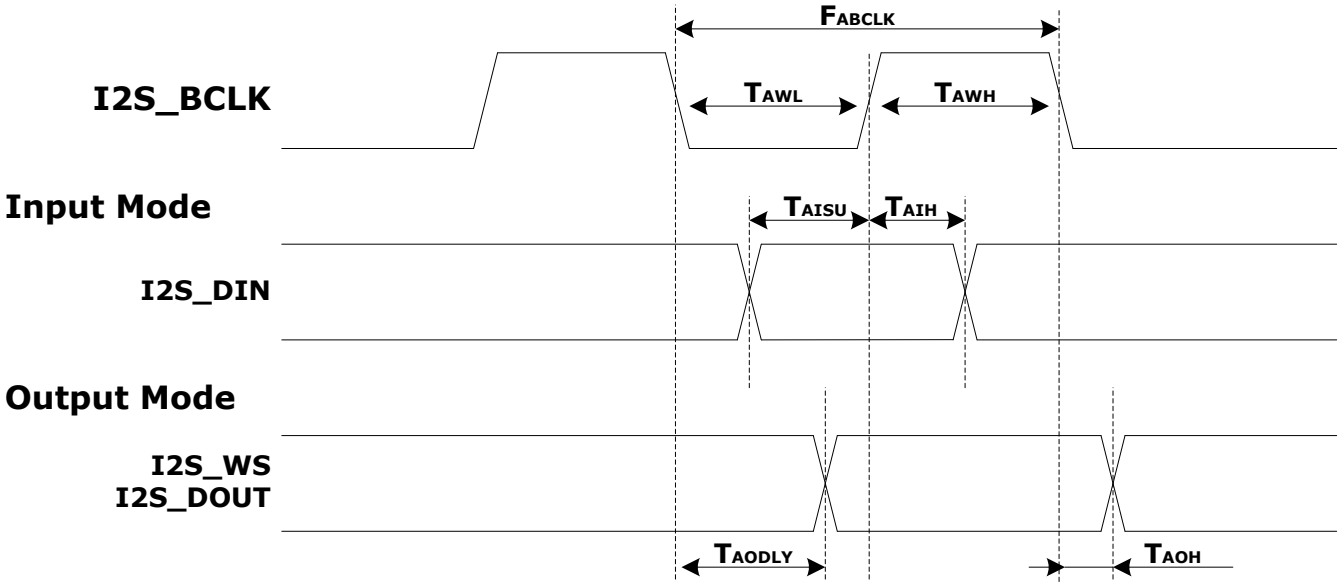
Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{MCLK}	MCLK Clock Cycle Time	6	-	12	ns
T_{MWL}	MCLK Clock Low Time	0.45	-	0.55	T_{MCLK}
T_{SWH}	MCLK Clock High Time	0.45	-	0.55	T_{MCLK}
T_{MODLY}	Command and Address Output Delay Time	-	-	2	ns
T_{MOH}	Command and Address Output Hold Time	2	-	-	ns
T_{MDQSH}	MDQS0/MDQS1 High Time	0.4	-	0.6	T_{MCLK}
T_{MDQSL}	MDQS0/MDQS1 Low Time	0.4	-	0.6	T_{MCLK}
T_{MDSU}	MD to MDQS0/MDQS1 Setup Time	0.6	-	-	ns
T_{MDH}	MD to MDQS0/MDQS1 Hold Time	0.6	-	-	ns
VREF	IO reference voltage	0.49	-	0.51	VDD

5.5.3 Sensor/Video-In Interface



Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPCLK Clock Frequency	-	-	50	MHz
T_{SWL}	SPCLK Clock Low Time	10	-	-	ns
T_{SWH}	SPCLK Clock High Time	10	-	-	ns
T_{SISU}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Setup Time	1.0	-	-	ns
T_{SIH}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Hold Time	1.0	-	-	ns

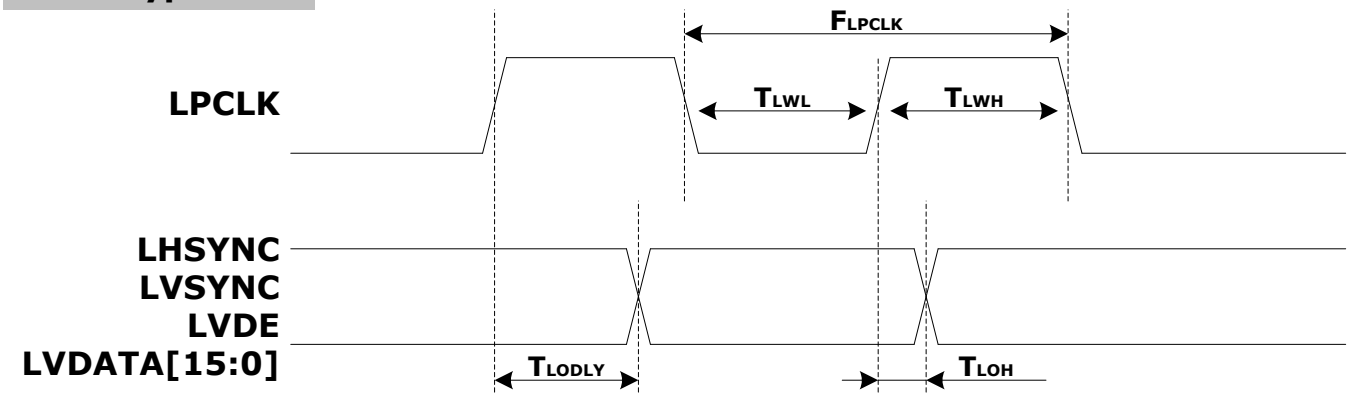
5.5.4 I2S Interface



Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{ABCLK}	I2S_BCLK Clock Frequency	-	-	16	MHz
T_{AWL}	I2S_BCLK Clock Low Time	31.25	-	-	ns
T_{AWH}	I2S_BCLK Clock High Time	31.25	-	-	ns
T_{AISU}	I2S_DIN Setup Time	10	-	-	ns
T_{AIH}	I2S_DIN Hold Time	10	-	-	ns
T_{AODLY}	I2S_DOUT Output Delay Time	-	-	0.5	ns
T_{AOH}	I2S_DOUT Output Hold Time	0.1	-	-	ns

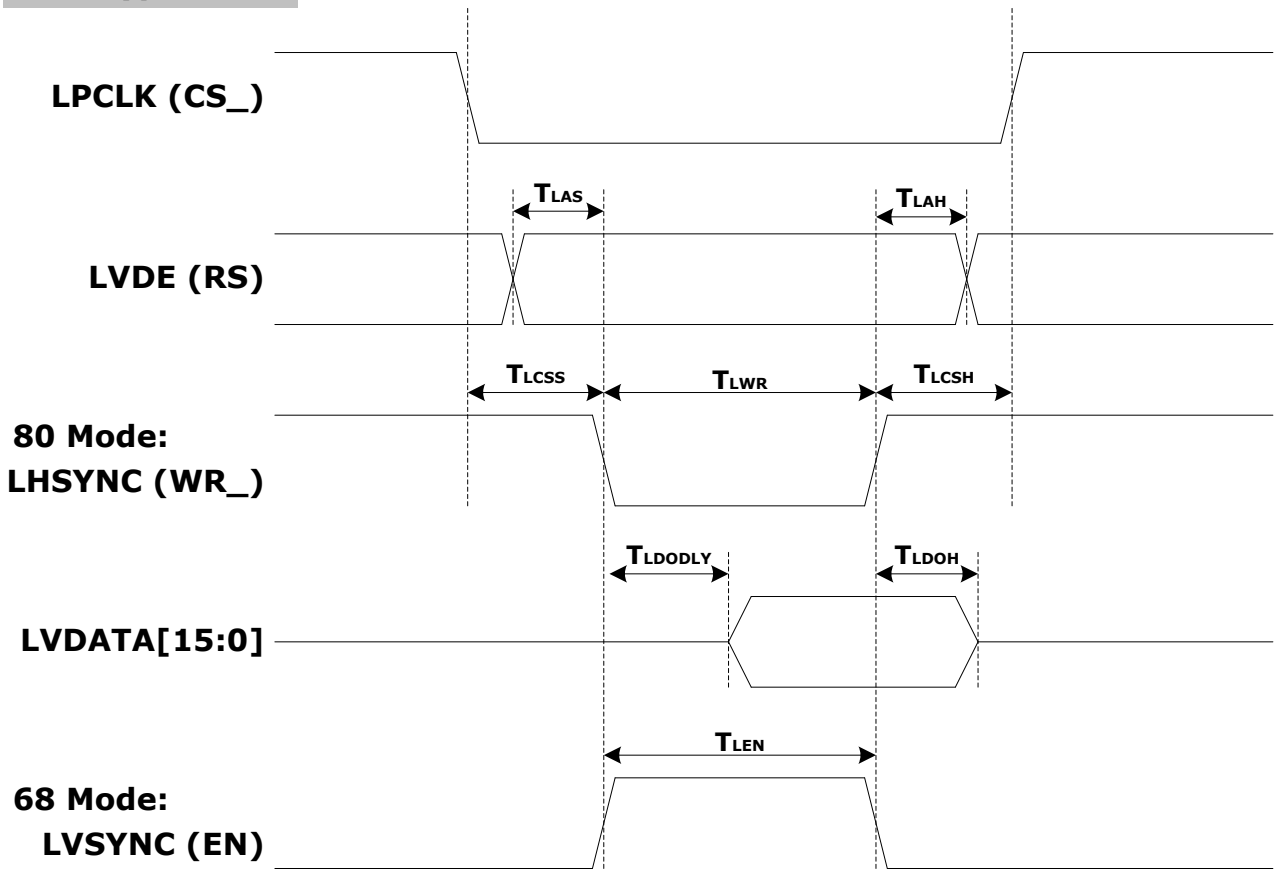
5.5.5 LCD/Display Interface

SYNC Type LCD



Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPCLK}	LPCLK Clock Frequency	-	-	27	MHz
T_{LWL}	LPCLK Clock Low Time	18.5	-	-	ns
T_{LWH}	LPCLK Clock High Time	18.5	-	-	ns
T_{LODLY}	LHSYNC, LVSYNC, LVDE and LVDATA Output Delay Time	-	-	1.3	ns
T_{LOH}	LHSYNC, LVSYNC, LVDE and LVDATA Output Hold Time	0.67	-	-	ns

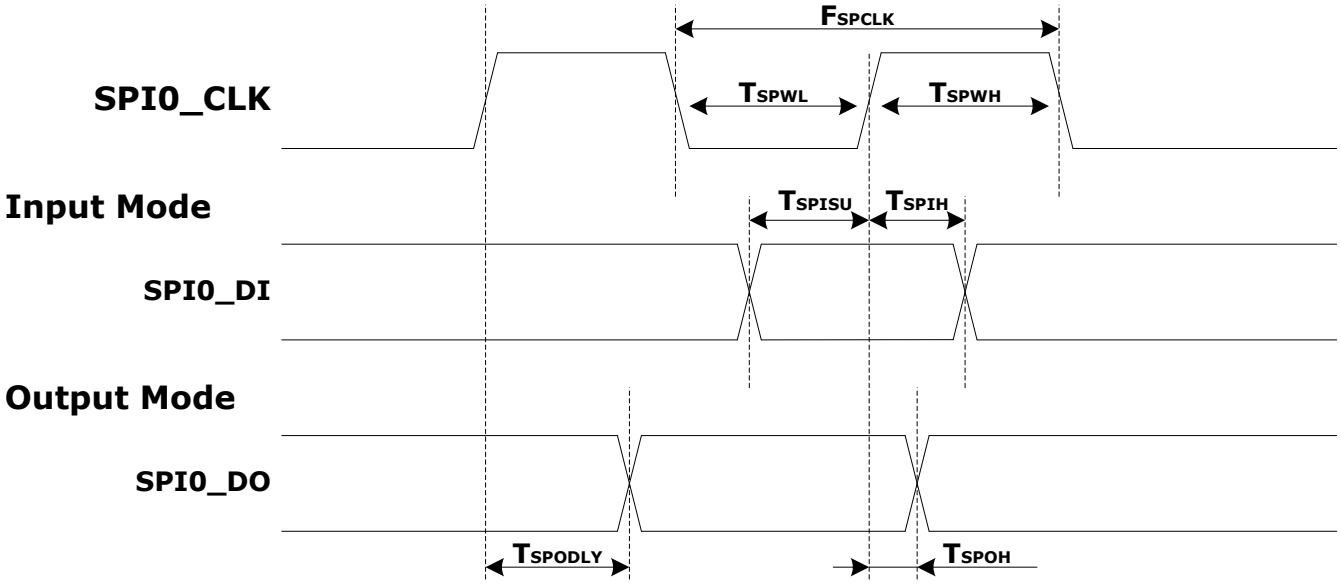
MPU Type LCD



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{LCSS}	CS_ to WR_ Setup Time		2	-	-	PCLK
T_{LCSH}	CS_ to WR_ Hold Time		1	-	-	PCLK
T_{LAS}	RS to WR_ Setup Time		1	-	-	PCLK
T_{LAH}	RS to WR_ Hold Time		1	-	-	PCLK
T_{LDODLY}	LVDATA Output Delay Time		-	-	1	PCLK
T_{LDOH}	LVDATA Output Hold Time		1	-	-	PCLK
T_{LWR}	WR_ Pulse Width	80 Mode	1	-	-	PCLK
T_{LEN}	EN Pulse Width	68 Mode	1	-	-	PCLK

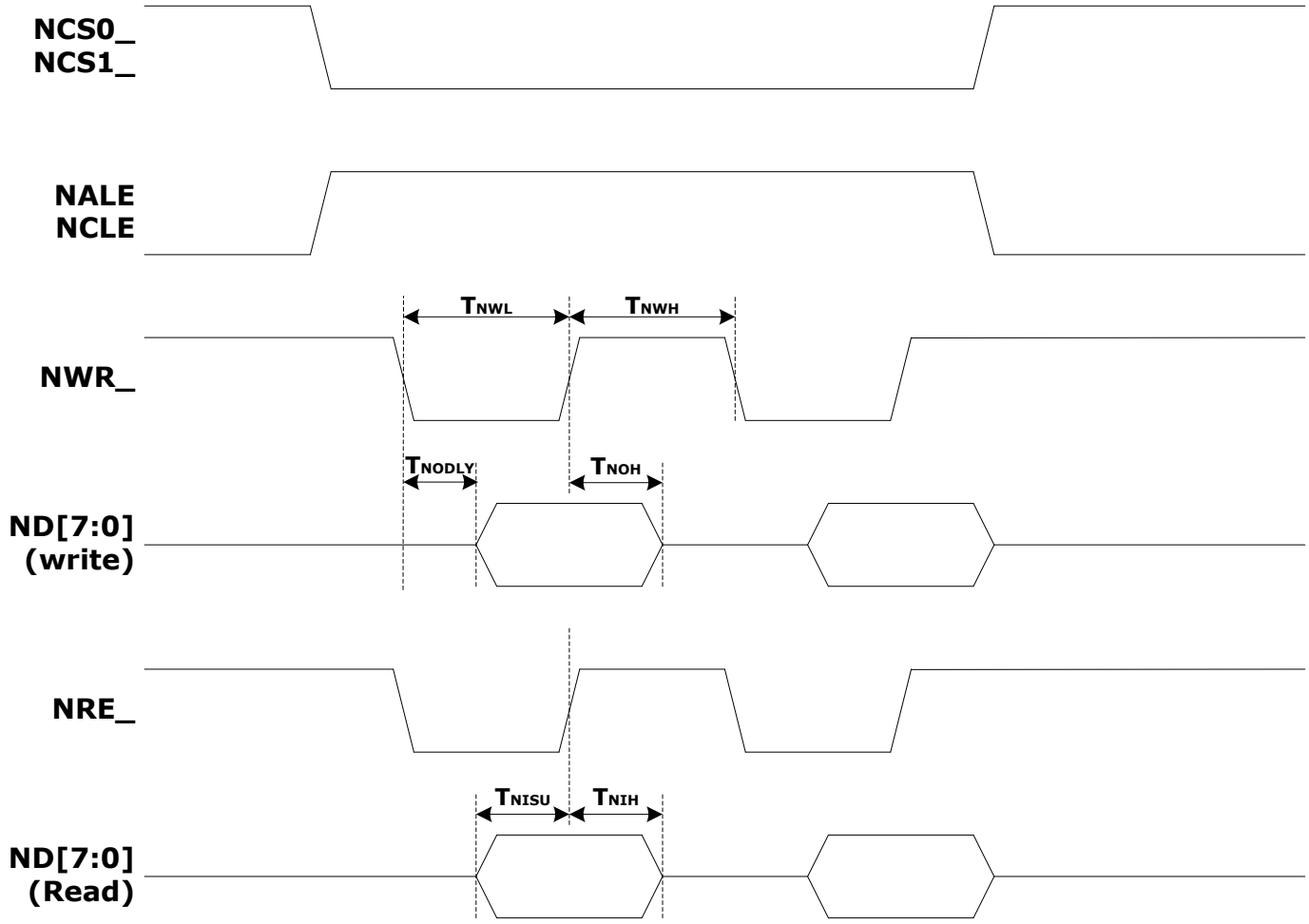
Note: PCLK is the period of one APB bus clock.

5.5.6 SPI Interface



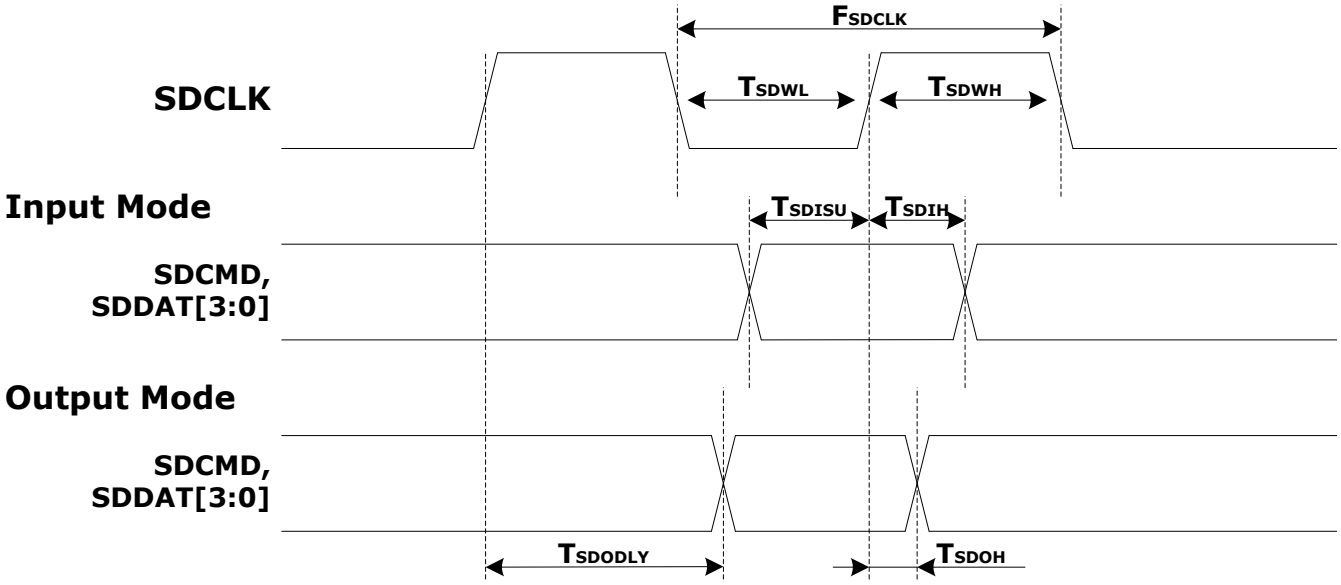
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPI0_CLK Clock Frequency	-	-	25	MHz
T_{SPWL}	SPI0_CLK Clock Low Time	20	-	-	ns
T_{SPWH}	SPI0_CLK Clock High Time	20	-	-	ns
T_{SPISU}	SPI0_DI Setup Time	10	-	-	ns
T_{SPIH}	SPI0_DI Hold Time	10	-	-	ns
T_{SPODLY}	SPI0_DO Output Delay Time	-	-	1	ns
T_{SPOH}	SPI0_DO Output Hold Time	0.2	-	-	ns

5.5.7 NAND Interface



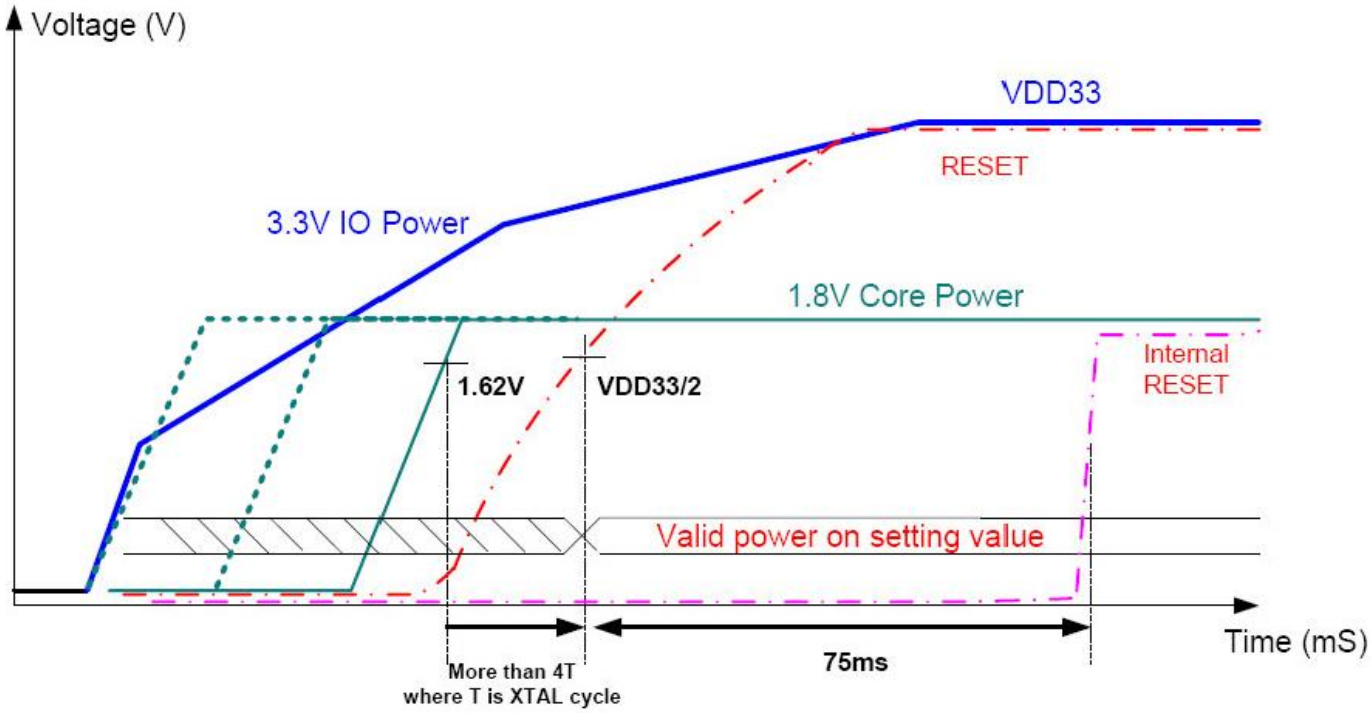
Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{NWL}	Write Pulse Low Width	10	-	-	ns
T_{NWH}	NWR_ High Hold Time	10	-	-	ns
T_{NODLY}	ND[7:0] Output Delay Time	-	-	2.5	ns
T_{NOH}	ND[7:0] Output Hold Time	10	-	-	ns
T_{NISU}	ND[7:0] Data in Setup Time	3.2	-	-	ns
T_{NIH}	ND[7:0] Data in hold time	1	-	-	ns

5.5.8 SD Card Interface

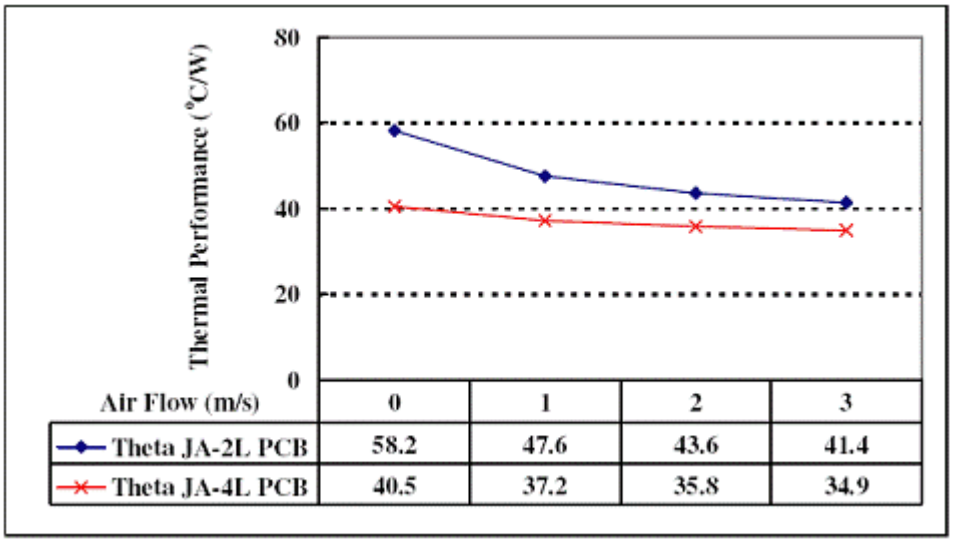


Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock SDCLK					
F_{SDCLK}	Clock Frequency in Data Transfer Mode	-	-	24	MHz
F_{SDCLK}	Clock Frequency in Identification Mode	100	-	400	KHz
T_{SDWL}	Clock Low Time	10	-	-	ns
T_{SDWH}	Clock High Time	10	-	-	ns
Input SDCMD, SDDAT[3:0] (referenced to SDCLK)					
T_{SDISU}	Input Setup Time	6	-	-	ns
T_{SDIH}	Input Hold Time	2	-	-	ns
Output SDCMD, SDDAT[3:0] (referenced to SDCLK)					
T_{SDODLY}	Output Delay Time	-	-	14	ns
T_{SDOH}	Output Hold Time	2.5	-	-	ns

5.6 Power-on Sequence



5.7 Thermal characteristics of LQFP-128 Package



Air Flow (m/s)	0	1	2	3
Theta JA-2L PCB	58.2	47.6	43.6	41.4
Theta JA-4L PCB	40.5	37.2	35.8	34.9

Thermal Performance of LQFP-128 under Forced Convection

6. N3290X SERIES PART SELECTION GUIDE

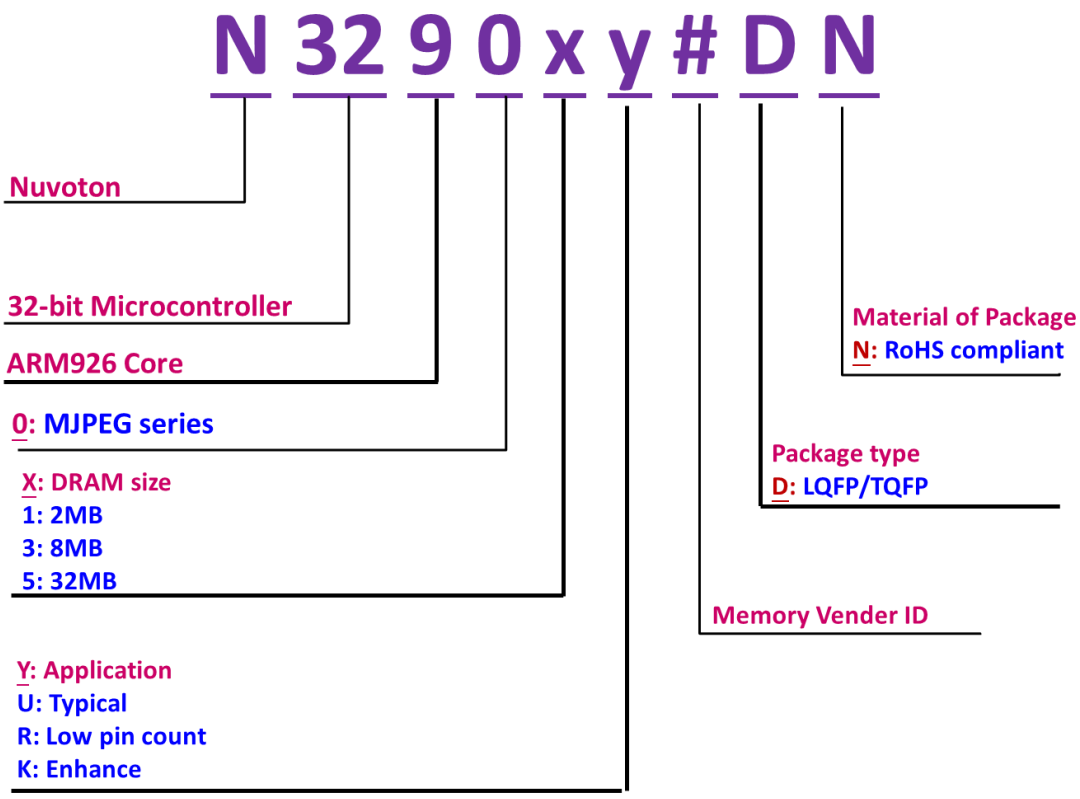
Part No.	Stacked DDR Size (MB)	SPI NOR Boot	NAND Flash Boot	SD / SDIO	USB FS Host (12 Mbps)	USB HS Host	USB Device (FS / HS)	Video Codec	2D Graphics	Parallel RGB LCD Color (bits)	Max. Resolution [3]	SAR ADC	ADC for MIC Input	Touch Panel (Wire)	Stereo DAC (bits)	Ethernet MAC	CMOS Sensor	UART	I²C	SPI	RTC	PWM	I²S	GPIO (Max)	Package	Mass Production
N32901R1DN	2	√	-	2	1	-	HS	MJPEG	-	-	-	1	√	-	16	-	1	2	-	1	-	2	√	34	LQFP64	√
N32903R5DN	8	√	-	2	1	-	HS	MJPEG	-	-	-	1	√	-	16	-	1	2	-	1	-	2	√	34	TQFP64-EP	√
N32905R3DN	32	√	-	2	1	-	HS	MJPEG	-	-	-	1	√	-	16	-	1	2	-	1	-	2	√	34	TQFP64-EP	√
N32901R7DN	2	√	-	1	1	-	HS	MJPEG	√	16	QVGA	-	-	-	-	-	-	2	1	1	-	4	-	44	TQFP64-EP	√
N32901U1DN	2	√	√	3	1	-	HS	MJPEG	√	18	QVGA	2	√	4	16	-	1	2	1	1	√	4	√	64	LQFP128	√
N32903U5DN	8	√	√	3	1	-	HS	MJPEG	√	18	VGA	2	√	4	16	-	1	2	1	1	√	4	√	64	LQFP128	√
N32905U3DN	32	√	√	3	1	-	HS	MJPEG	√	18	VGA	2	√	4	16	-	1	2	1	1	√	4	√	64	LQFP128	√
N32901K3DN	2	√	√	3	1	-	HS	MJPEG	√	24	VGA	3	-	4	16	-	1	2	1	2	√	4	√	70	LQFP128	√
N32903K5DN	8	√	√	3	1	-	HS	MJPEG	√	24	VGA	3	-	4	16	-	1	2	1	2	√	4	√	70	LQFP128	√
N32905K5DN	32	√	√	3	1	-	HS	MJPEG	√	24	VGA	3	-	4	16	-	1	2	1	2	√	4	√	70	LQFP128	√

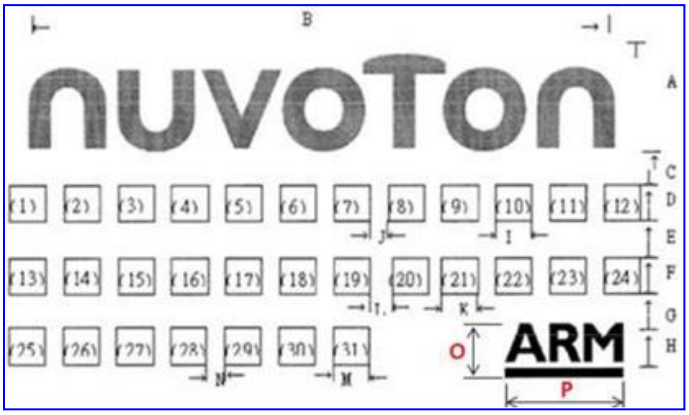
Part no.	Package type	Description	Chip Version
N32901R1DN	LQFP-64,	2MB SDRAM@3.3V with CIS interface	E/H
N32903R5DN	TQFP-64,	8MB LPDDR@1.8V with CIS interface	H
N32905R3DN	TQFP-64,	32MB DDRII@1.8V with CIS interface	F/H
N32901R7DN	TQFP-64,	2MB SDRAM@3.3V with LCD-16bits	H
N32901U1DN	LQFP-128,	2MB SDRAM@3.3V with LCD & CIS interfaces	E/H
N32903U5DN	LQFP-128,	8MB LPDDR@1.8V with LCD & CIS interfaces	H
N32905U3DN	LQFP-128,	32MB DDRII@1.8V with LCD & CIS interfaces	F/H
N32901K3DN	LQFP-128	2MB SDRAM@3.3V with LCD-24bits & SPIx2 interfaces	H
N32903K5DN	LQFP-128	8MB LPDDR@1.8V with LCD-24bits & SPIx2 interfaces	H
N32905K5DN	LQFP128	32MB DDRII@1.8V with LCD-24bits & SPIx2 interfaces	H

Note.

- F version applys to N32905U3DN and N32905R3DN, they must use a specific utility tool of Turbo-Writer version
- N3290xKxDN series is used H version
- F&H version can support DDR2
- F&H version can support eMMC booting
- F&H version can support SPI-NOR size 128Mb or above

6.1 Part Number Definition





Description,

Line-1: NUVOTON LOGO

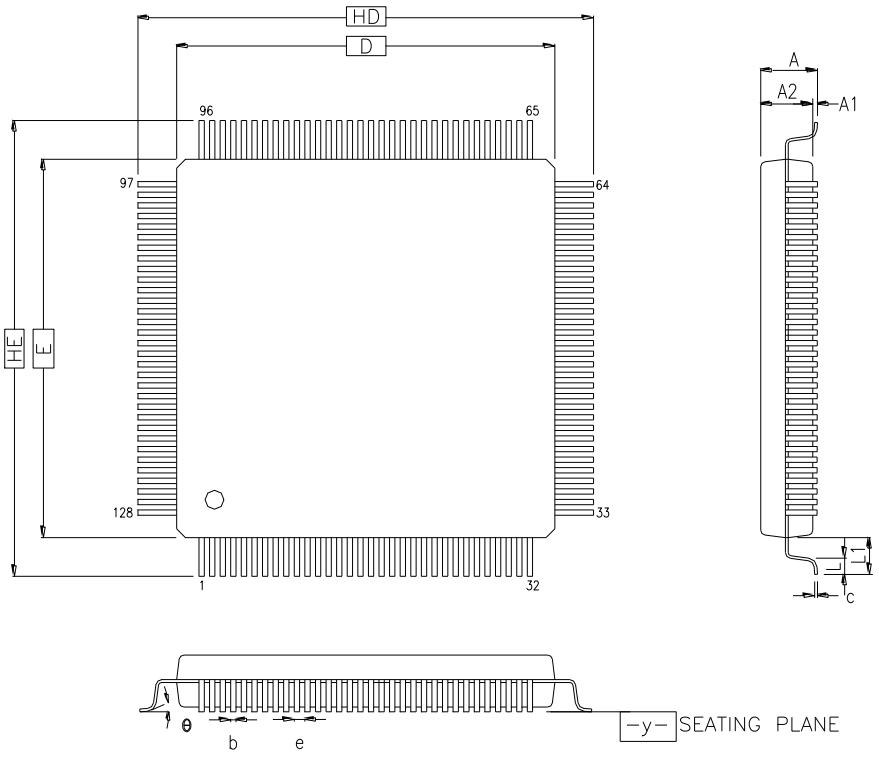
Line-2: Part No.

Line-3: Product lot No.

Line-4: the chip version ID is shown on (29) as the picture.

7. PACKAGE OUTLINE

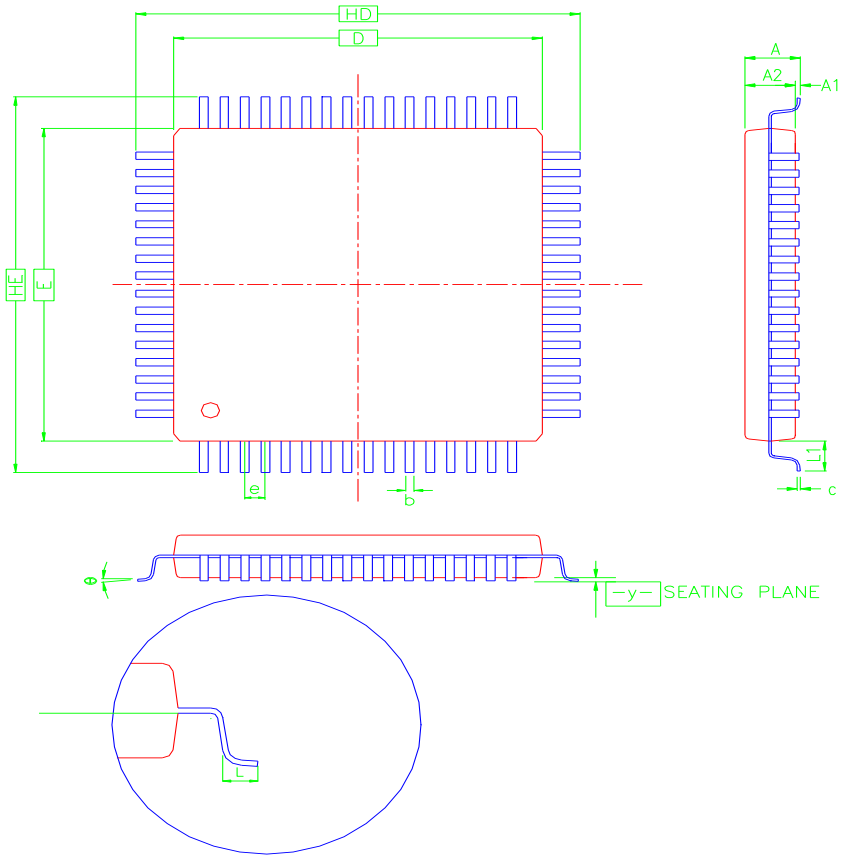
7.1 LQFP-128 (14X14X1.4mm body, 0.4mm pitch)



COTROL DIMENSIONS ARE IN MILLIMETERS.

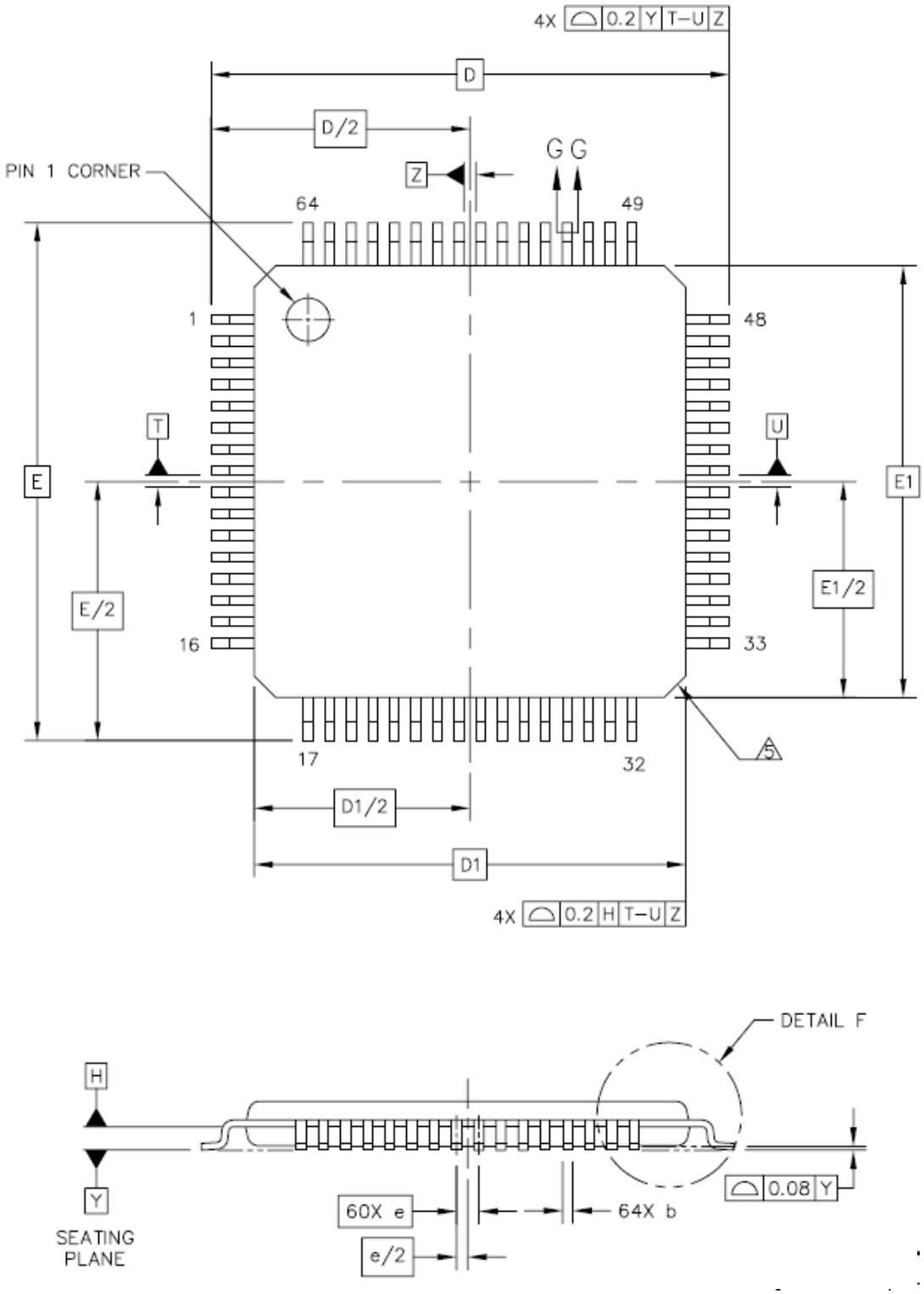
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

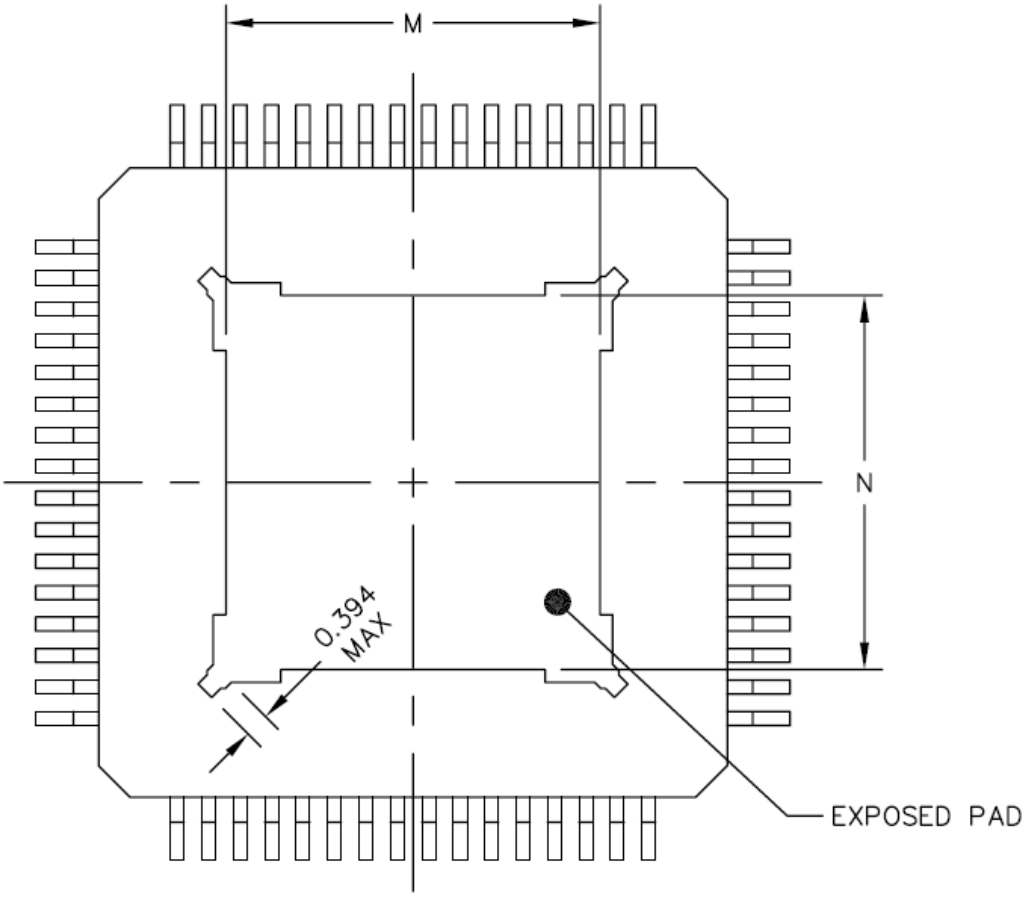
7.2 LQFP-64 (10X10X1.4mm body, 0.5mm pitch)



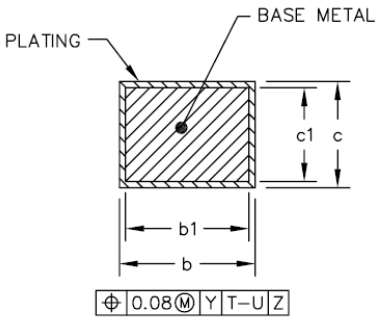
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0	3.5	7	0	3.5	7

7.3 TQFP-64 (10X10X1.0mm body, 0.5mm pitch)

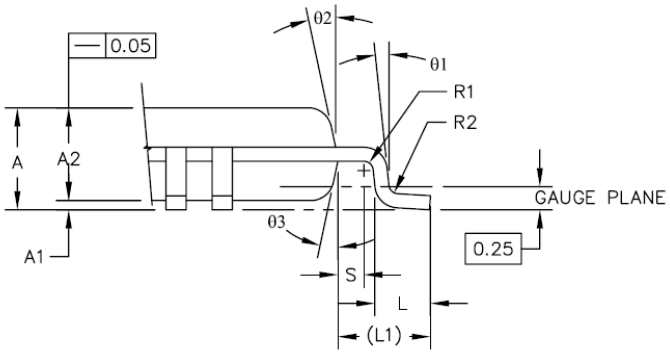




BOTTOM VIEW



SECTION G–G



DETAIL F

DIM	MIN		MAX
A	---		1.2
A1	0.05		0.15
A2	0.95	1	1.05
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		12 BSC	
D1		10 BSC	
e		0.5 BSC	
E		12 BSC	
E1		10 BSC	
L	0.45	0.6	0.75

DIM	MIN		MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S	0.2		---
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°
M	5.85		6.05
N	5.85		6.05

UNIT: mm

COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	—	—	1.60
A_1	0.05	—	0.15
A_2	1.35	1.40	1.45
HD		16.00 BSC.	
D		14.00 BSC.	
HE		16.00 BSC.	
E		14.00 BSC.	
b	0.13	0.16	0.23
e		0.40 BSC.	
θ	0°	3.5°	7°
c	0.09	—	0.20
L	0.45	0.60	0.75
L_1		1.00 REF	
y	–	–	0.1

8. REVISION HISTORY

VERSION	DATE	DESCRIPTION
A0	Jul. 25, 2012	● Initial release.
A1	Aug. 1, 2012	● Add stacked DRAM size into order Information
A2	Aug. 30, 2012	● Add N32901U1DN Information ● Correct the N32905U2DN Pin Diagram
A3	Oct. 15, 2012	● Extend Operation Temperature Range ● Add Parts Feature Difference Table
A3.1	Oct. 26, 2012	● Add Part Number Definition
A3.2	Nov. 8, 2012	● Add CCIR Still Image and Video Recommanded Resolutions. ● Add LCD Display for Still Image and Video Recommanded Resolutions. ● Modify One SPI H/W Engine to Support Two SPI Devices by Two Chip Selection Signals when SPI0 is in Master Mode. For LQFP128 package, only SPI0 is active. ● Add USB 1.1 Host One H/W Controller, Three Different Pin Locations Information.
A3.3	Nov. 10, 2012	● Remove Adobe Flash Feature from Comparision Table.
A3.4	Jan. 21, 2013	● Update the AC characteristics.
A4.0	Mar. 15, 2013	● Add N32903R1DN
A5.0	May 1, 2013	● Add N32901R1DN Information. ● Add N32901U2DN Information.
A5.1	May 3, 2013	● Add SDRAM and DDR Operation Voltage Spec
A5.2	Mar. 17, 2014	● Add N32905U3DN
A5.3	Aug. 13, 2014	● Revise Audio DAC Characteristics of Full Scale output voltage
A5.4	Sept. 10, 2014	● Add N32903U2DN to pin diagram ● Add N32903U2DN, N32901R1DN & N32901U2DN to Ordering Information ● Comparison table for N3290x series
A5.5	Oct. 23, 2014	● Add N32905R3DN ● Removed VPOST supports LCD VSYNC/MPU-24bit BUS
A5.6	Dec. 15, 2015	● Revised pin desciprion.
A5.7	May 17, 2016	● Add N32905U4DN to pin diagram ● Add N32905U4DN to ordering information ● Add the notice with chip F version
A5.8	Jul. 29, 2016	● Add MPU LCD pin description ● Revised DRAM operating voltage 3.3V/1.8V description
A5.9	Sept. 30, 2016	● Updated N32903U2DN part number to pin description.

A6.0	Mar. 26, 2018	● Add part no. N3290xKxDN series
A6.1	May 18, 2018	● Add part no. N32901R7DN
A6.2	Oct. 10, 2018	● N3290x series part no. selection updated in Q4, 2018
A6.3	Mar. 22,2019	● Title renamed: “Displayer Controller Application Pocessor” ● Power management, power-down mode description updated at page 11. ● Adds package ink picture for chip version index at page 62.

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