NAU88L21
Ultra-Low Power Audio CODEC Ground-Referenced Headphone Amplifier

GENERAL DESCRIPTION

The NAU88L21 is an ultra-low power high performance audio codec that supports both analog and digital audio functions. It includes one I2S/PCM interface, one digital microphone interface, one digital mixer, two high quality DACs and ADC's, and one stereo class G headphone amplifier. The advanced on-chip signal processing engine that includes dynamic range compressor (DRC), programmable biquad filter, as well as an integrated frequency locked loop (FLL) to support various input clocks.

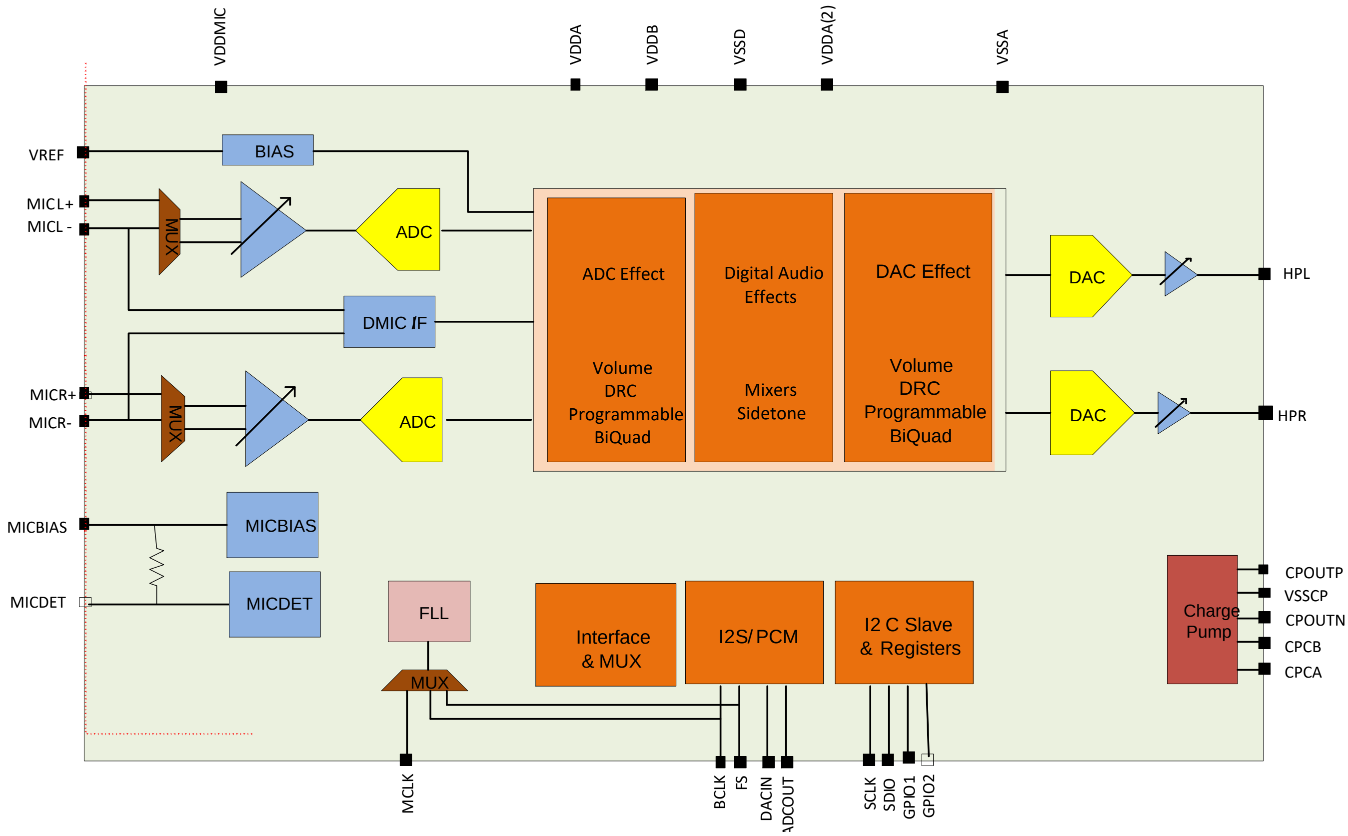
FEATURES

- DAC: 105dB SNR, (A-weighted) @ 0dB gain, 1.8V and -88dB THD @ 20mW and RL= 32Ω, DAC playback to headphone output mode
- ADC: 103dB SNR (A-weighted) @ 0dB MIC gain, 1.8V, Fs = 48kHz and -93dB THD, 1.8V, MIC gain 0dB, OSR 256x
- 1 Digital I2S/PCM I/O port
- Two mono differential or one stereo differential analog microphone inputs, two single-ended microphone inputs or one stereo digital microphone input
- Cap-free Low noise Microphone bias with 7uVrms noise between 20Hz-20kHz, internal pull high resistor for microphone.
- Class G Headphone Amplifier (28mW @ 32Ω, 1% THD+N)
- Sampling rate from 8k to 192 kHz
- Dynamic Range Compressor (DRC)Programmable Biquad filter Integrated DSP with specific functions:Input automatic level control (ALC/AGC)/limiter
- Output dynamic-range-compressor/limiter
- Package: 32 Pin QFN package

Applications

- Gaming controller
- Wireless Headset
- Smart Remote Controller

Block Diagram : QFN32



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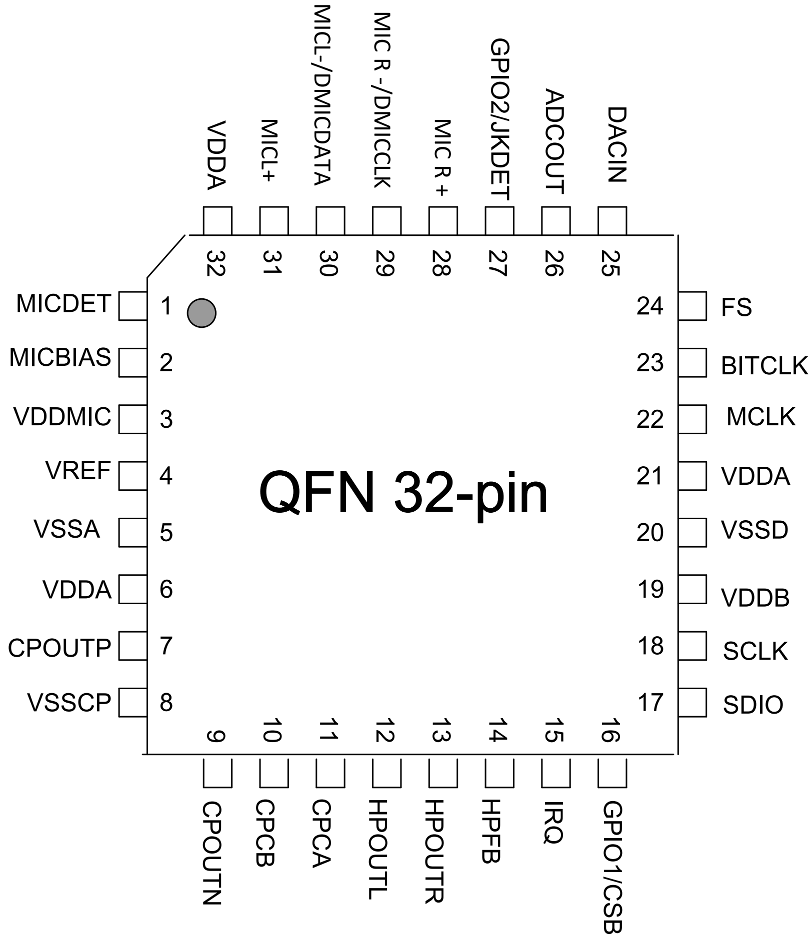

QFN 32-pin
MICDET 1
MICBIAS 2
VDDMIC 3
VREF 4
VSSA 5
VDDA 6
CPOUTP 7
VSSCP 8
9 CPOUTN
10 CPCB
11 CPCA
12 HPOUTL
13 HPOUTR
14 HPFB
15 IRQ
16 GPIO1/CSB
17 SDIO
18 SCLK
19 VDDB
20 VSSD
21 VDDA
22 MCLK
23 BITCLK
24 FS
25 DACIN
26 ADCOUT
27 GPIO2/JKDET
28 MIC R +
29 MIC R -/DMICCLK
30 MICL-/DMICDATA
31 MICL+
32 VDDA

Pin Description

Pin #	Name	Type	Functionality
1	MICDET	Analog IO	Microphone/button detect, 2kOhm between Mic and Mic Bias
2	MICBIAS	Analog Output	Microphone Bias Output
3	VDDMIC	Supply	Microphone supply
4	VREF	Analog I/O	Internal DAC & ADC voltage reference decoupling I/O
5	VSSA	Ground	Analog Ground
6	VDDA	Supply	Analog Supply
7	CPOUTP	Analog I/O	Charge Pump positive voltage
8	VSSCP	Ground	Charge Pump Supply ground
9	CPOUTN	Analog I/O	Charge Pump negative voltage
10	CPCB	Analog I/O	Charge Pump switching capacitor node B
11	CPCA	Analog I/O	Charge Pump switching capacitor node A
12	JKTIP(HPL)	Analog Output	Jack Tip; Headphone left channel output
13	JKR1(HPR)	Analog Output	Jack Ring1; Headphone right channel output
14	HPFB	Ground	Headphone Ground
15	IRQ	Digital I/O	IRQ
16	GPIO1/CSB	Digital I/O	General Purpose IO/CSB
17	SDIO	Digital I/O	Serial Data for I2C
18	SCLK	Digital Input	Serial Data Clock for I2C
19	VDDB	Supply	Digital IO Supply
20	VSSD	Ground	Digital IO ground
21	VDDA	Supply	Analog supply
22	MCLK	Digital Input	CODEC Master clock input
23	BCLK	Digital I/O	Serial data bit clock input or output for I2S or PCM data
24	FS	Digital I/O	Frame Sync input or output for I2S or PCM data
25	DACIN	Digital Input	Serial Audio data input for I2S or PCM data
26	ADCOUT	Digital Output	Serial Audio data Output for I2S or PCM data
27	JKDET	Analog Input	Jack detect input
28	MICR+	Analog Input	PGA MICR+ Analog Input
29	MICR-/DMCLK	Analog/Digital Output	PGA MICR- Analog Input / Digital Microphone Clk output
30	MICL-/DMDATA	Analog Input/Digital Input	PGA MICL- Analog Input / Digital Microphone Data input
31	MICL+	Analog Input	PGA MICL+ Analog Input
32	VDDA	Supply	Analog Supply

Electrical Characteristics

Conditions: $V_{DD}A$ = $V_{DD}B$ = 1.8V; $V_{DD}MIC$= 3.6V.
R_L(Headphone) = 32 Ω, f = 1kHz, MCLK=12.88MHz, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units
ISD	Shutdown Current	$V_{DD}A$	4	16	µA
		$V_{DD}B$	0.2	1	
		$V_{DD}MIC$	0.2	1	
I_{DD}	Headset Detection Standby Mode	MCLK off, Jack Insertion, IRQ enabled		10	µA
	Active Current Normal Playback Mode	f_S = 48kHz, Stereo HP DAC On, HP On, P_{OUT} = 0mW. $R_{L(HP)}$ = 32Ω		5	mA
Headphone Amplifier					
P_O	Output Power	Stereo R_L = 32Ω, DAC Input, CPV_{VDD} = 1.8V, f=1020Hz, 22kHz BW, THD+N = 1% (QFN package),	28		mW
		Stereo R_L = 16Ω, DAC Input, CPV_{VDD} = 1.8V, f=1020Hz, 22kHz BW, THD+N = 1% (QFN Package)	33		mW
THD+N	Total Harmonic Distortion + Noise	R_L = 32Ω, f=1020Hz, P_O = 20mW	-88		dB
SNR	Signal to Noise Ratio	VOUT = 1VRMS, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1020Hz, A-Weighted)	105		dB
		VOUT = 1 V_{RMS}, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1020Hz, A-Weighted, auto attenuate enabled,	108		dB
PSRR	Power Supply Rejection Ratio	f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} Input Referred, HP_GAIN = 0dB DAC Input, DAC_Gain = 0dB Ripple Applied to $V_{DD}A$	90		dB
		Mono_Gain = 0dB Ripple Applied to $V_{DD}A$	90		dB
		Stereo Single Ended Input Terminated, Stereo_Gain = 0dB Ripple Applied to $V_{DD}A$	90		dB
X_{TALK}	Channel Crosstalk	Left Channel to Right Channel, -1dBFS, Gain = 0dB, f = 1020Hz	70		dB
	Interchannel Level Mismatch		+/- 0.1		dB
	Frequency Response	F = 20Hz ~ 20kHz	+0.1/-0.2		dB
	Pop up Noise			1	mVrms
e_{OS}	Output Noise	DAC_Gain = 0dB, HP_Gain = 0dB, f_S=48kHz, OSR_{DAC} = 128, A-Weighted	4.4		uV_{RMS}
	Out of Band Noise Level		-60dB		
V_{OS}	Output Offset Voltage	HP_Gain = 0dB, DAC_Gain= 0dB, DAC Input		±1	mV
	Power Consunption MP3 Mode	No Load, No Signal, Amp on f_S = 48kHz, Stereo DAC On, Amp On, P_{OUT} = 0mW. R_L = 32Ω	6		mW

Symbol	Parameter	Conditions	Typical	Limit	Units
	Fs Accuracy (44.1 / 48 kHz)		+/- 0.02%		
	Pop and Click Noise	plug Into or out of DAC to Headphone	1		mVrms
		ADC			
THD+N	ADC Total Harmonic Distortion + Noise	MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1020Hz, fs = 48KHz, Mono Differential Input	-91		dB
		MIC Input, MIC_GAIN = 30dB, Volume = 0dB, Vin=28.5mVrms, f=1020Hz, Digital Gain = 0dB, Mono Differential Input	-80		dB
SNR	Signal to Noise Ratio	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 48kHz, Mono Differential Input	102		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 48kHz, Mono Differential Input	101		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP} applied to V_{DD}A, f_{RIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input	90		dB
CMRR	Common Mode Rejection Ratio	Differential Input 100mVrms, PGA gain = 20dB, frequency sweep from 20Hz to 20KHz	65		dB
FS_{ADC}	ADC Full Scale Input Level	V_{DD}A= 1.8V	1		V_{RMS}
	Minimum Input Impedance		10		kOhm
	Frequency Response	f = 20Hz ~ 20kHz	+0.1/-0.2		dB
	Pop up Noise	TBD	1		mVrms
	Power Consumption	No Signal, ADC on f_s = 44.1kHz	5		mW
		MICBIAS			
V_{BIAS}	Output Voltage	Programmable 1.8V to 3.0V in 6 steps	2.5		V
I_{OUT}	Output Current			4	mA
e_{os}	Output Noise	Low noise mode, at 1kHz		47	nV/√Hz

Digital I/O

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	V_{DD}B = 1.8V			0.33*V_{DD}B	V
		V_{DD}B = 3.3V			0.37*V_{DD}B	
Input HIGH level	V_{IH}	V_{DD}B = 1.8V		0.67*V_{DD}B		V
		V_{DD}B = 3.3V		0.63*V_{DD}B		
Output HIGH level	V_{OH}	I_{Load}= 1mA	V_{DD}B=1.8V	0.9*V_{DD}B		V
			V_{DD}B = 3.3V	0.95*V_{DD}B		
Output LOW level	V_{OL}	I_{Load}= 1mA	V_{DD}B = 1.8V		0.1*V_{DD}B	V
			V_{DD}B=3.3V		0.05*V_{DD}B	

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital I/O Supply Range	$V_{DD}B$	1.62	3.3	3.6	V
Analog Supply Range	$V_{DD}A$	1.62	1.8	1.98	V
Headphone Supply Range	$V_{DD}A$	1.62	1.8	1.98	V
Microphone Bias Supply Voltage	$V_{DD}MIC$	3.0	3.3	3.6	V
Temperature Range	T_A	-40		+85	°C

Absolute Maximum Ratings

Parameter	Min	Max	Units
Digital Supply Range	-0.3	2.2	V
Digital I/O Supply Range	-0.3	4.0	V
Analog Supply Range	-0.3	2.2	V
Headphone Supply Range	-0.3	2.2	V
Microphone Bias Supply Voltage	-0.3	4.0	V
Voltage Input Digital Range	DGND - 0.3	V_{DD} + 0.3	V
Voltage Input Analog Range	AGND - 0.3	V_{DD} + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

1. General Description

NAU88L21 is an ultra-low power CODECs that has both analog and digital blocks operating at 1.8V. This CODEC includes DSP functions including DRCs (Dynamic Range Compression) and programmable biquad filters. Mic bias supply is upgraded to support voltages up to 3V.

1.1 Inputs

The NAU88L21 provides analog inputs to acquire and process audio signals from microphones with high fidelity and flexibility. There is a stereo input path that can be used to capture signals from single-ended or differential sources. The channel has a fully differential programmable gain amplifier (PGA). The outputs of the PGA connect to the ADC.

The NAU88L21 also has an input for one digital microphone. The NAU88L21 provides a DMCLK, the clock signal for the digital microphones.

The analog and the digital microphone inputs cannot be used simultaneously.

1.2 Outputs

NAU88L21 has one pair of ground-referenced Class G headphone outputs that are fed by two DACs. The headphone amplifier has a gain range of -9dB to 0dB.

The Class G headphone amplifier is powered by the charge pump output voltages CPOUTP and CPOUTN. When there is no loading the CPOUTP is equal to VDDA, and CPOUTN is equal to –VDDA.
This headphone output can also be used as a lineout.

1.3 ADC, DAC and Digital Signal Processing

The NAU88L21 has two independent high quality ADC's and DACs. These are high performance 24-bit sigma-delta converters, which are suitable for a very wide range of applications.

The ADCs and DACs have functions that individually support digital mixing and routing. The ADCs and DACs blocks also support advanced digital signal processing subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize processing artifacts and maximize the audio dynamic range supported by the NAU88L21.

The ADCs and DACs digital signal process can support two-point dynamic range compressors (DRCs), programmable biquad filters configurable for low pass filters, high pass filters, Notch filter, Bell, low shelf, and high shelf filters with various gain, Q, and frequency controls. Two-point DRCs can be programmed to limit the maximum output level and/or boost a low output level. The biquad filters can be configured as high pass filters intended for DC-blocking or low frequency noise reduction, such as reducing unwanted ambient noise or "wind noise" on a microphone inputs.

1.4 Digital Interfaces

Command and control of the device is accomplished by using the I2C interface.

The digital audio I/O data streams transfer separately from command and control using either I2S or PCM audio data protocols

These simple but highly flexible interface protocols are compatible with most commonly used serial data protocols, host drivers, and industry standard I2S and PCM devices.

2. Power Supply

This NAU88L21 has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. Because of this, there are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harming the device. However, pops and clicks may result from some sequences.

2.1 Power on and off reset

The NAU88L21 includes a power on reset circuit on chip. The circuit resets the internal logic control at VDDA supply power up and this reset function is automatically generated internally when power supplies are too low for reliable operation. The reset threshold is approximately 0.55Vdc and 1.0Vdc for VDDA. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

The reset is held on while the power levels for VDDA are below their respective thresholds. Once the power levels rise above their thresholds, the reset is released. Once the reset is released, the registers are ready to be written to. It is also important to note that all the registers should be kept in their reset state for at least 6µs.

An additional internal RC filter based circuit is added which helps the circuit respond for fast ramp rates (~10µs) and generate the desired reset period width (~10µs at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50ns.
For reliable operation, it is recommended to write any value to register upon power up. This will reset all registers to the known default state.

Note that when VDDA are below the power on reset threshold, then the digital IO pins will go into a tri-state condition.

3. Input Path Detailed Descriptions

NAU88L21 has two low noise, high common mode rejection ratio analog microphone differential input. The microphone inputs MICL+/- & MICR+/- which are followed by -1dB to 36dB PGA gain stages that have a fixed 12kOhm input impedance.

Inputs are maintained at a DC bias of approximately ½ of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of external DC blocking capacitors suitable for the device application.

The differential microphone input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital media devices and cell phones. Differential inputs are also very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

3.1 Analog Microphone Inputs

The analog microphone inputs are routed to the FEPGA (Front End Programmable Gain Amplifier). The input stage can be configured in different modes. The FEPGA gain can be varied from -1dB to 36dB in 1dB steps. The gain stage has a fixed 12kOhm input impedance and can be individually enabled or disabled by using register.

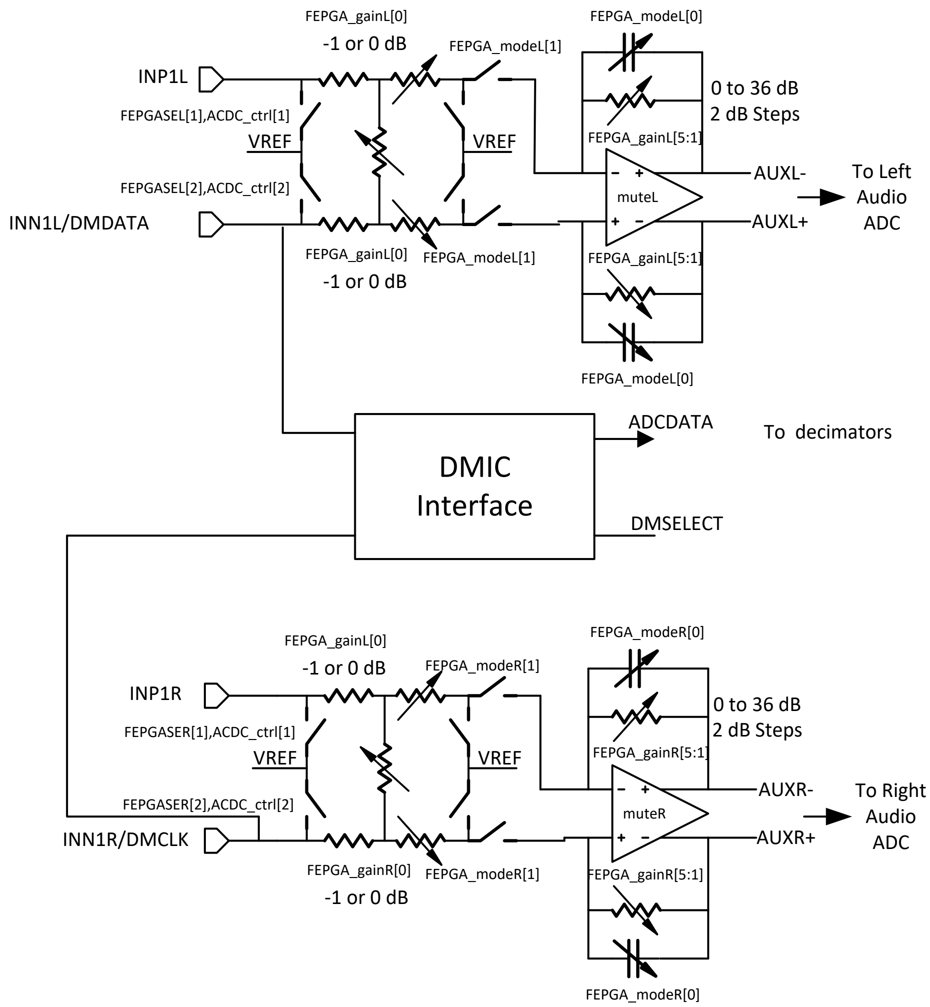


Figure 1: Microphone Input Block Diagram with Registers

3.2 Digital Microphone Input

The MICL- and MICR- pins can be used for the digital microphone input. MICR- is the clock for the digital microphones and the MICL- is the data in.

3.3 VREF

The NAU88L21 includes a mid-supply reference circuit that produces a voltage close to VDDA/2. This “VREF” pin should be decoupled to VSS through an external bypass capacitor. Because VREF is used as a reference voltage inside the NAU88L21, a large capacitance is required to achieve good power supply rejection at low frequency. Typically, a value of 4.7µF should be used. This larger capacitance may introduce longer rise time of VREF and delay the line output signal. However, a pre-charge circuit can be supported to help reduce the rise time. Due to the high impedance of the VREF pin, it is important to use a low leakage capacitor. A pre-charge circuit has been implemented to reduce the VREF rise time. Once charged, this can be disabled using to save power or prevent rapid changes in level due to fluctuations in VDDA. The below Table 1 shows the VREF tie-off resister selection.

VMIDSEL	VREF Resistor Selection	VREF Impedance
00	Open, no resistor selected	Open, no impedance installed
01	50kOhm	25kOhm
10	250kOhm	125kOhm
11	5kOhm	2.5kOhm

Table 1: VREF Impedance Selection

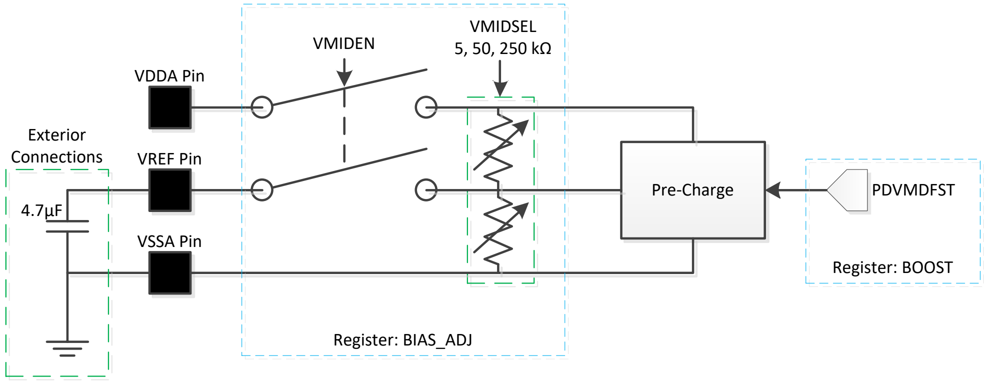


Figure 2: V_{REF} Circuitry

3.4 MIC Bias

The NAU88L21 provides one MIC bias pin, which can be used to power various microphones. The output level of MIC Bias can be set between VDDA and 1.53 X VDDA using register settings.

It is recommended that the microphones do not draw more than 4mA from the MICBIAS pin. There are options for connecting internal 2 Kohm resistor to the microphone and for low noise or low power mode. If MICBIAS is used in low power mode, typically 100nF or 200nF capacitor can be used along with MIC Bias level at VDDA. In the low noise mode, external 1uF or 4.7uF capacitor can be omitted by register settings when MIC Bias is used to power analog microphones.

3.5 MIC detect

The MIC detect block can detect whether a microphone is connected between the MICBIAS output and the MICDET pin. Either the internal 2kOhm resistor or an external 2kOhm resistor can be used to connect the microphone to the MICDET pin and MICBIAS. See Figure 3, where the internal hookup of the MICDET and MICBIAS blocks is shown.

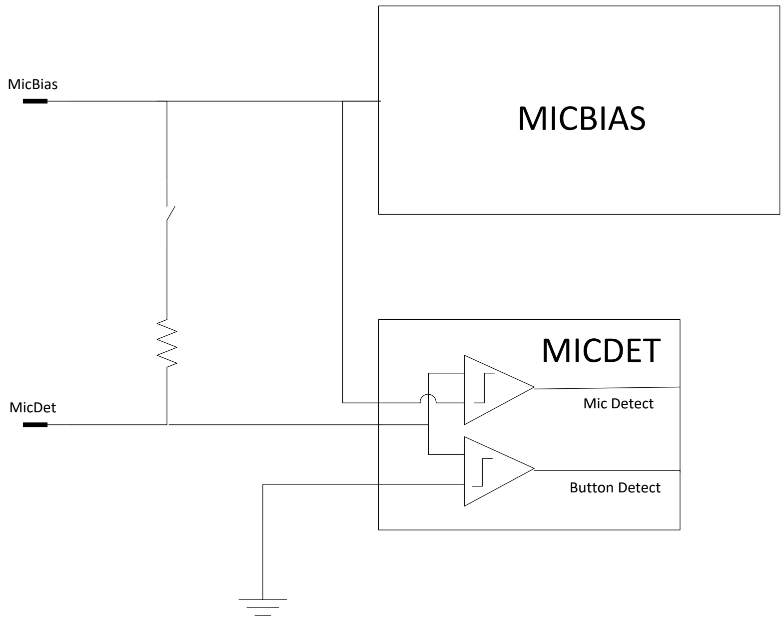


Figure 3. Mic Detect and MICBIAS blocks

Application note: Adding a simple RC on the MICDET pin can help reduce noise coupling. These may be board level related, or component related effects.

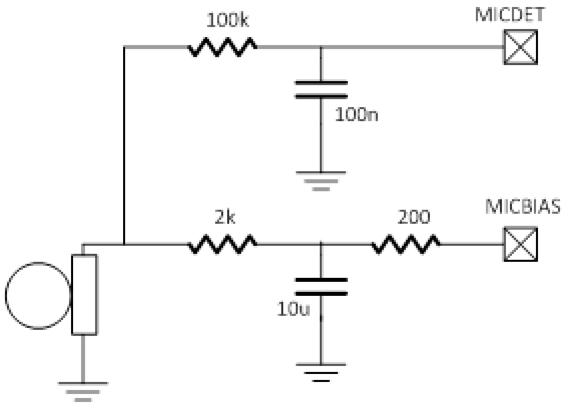


Figure 4. Reducing noise coupling effects

If the optional external 2KOhm resistor is used, then the internal 2K Ohm resistor (Between MICBIAS and MICDET) should be disabled.

3.5.1 Key Release

This feature detects the edge case where the key press interrupt is not followed by a release interrupt until later on in the sequence and clears the x11 register to prepare for further interrupts.

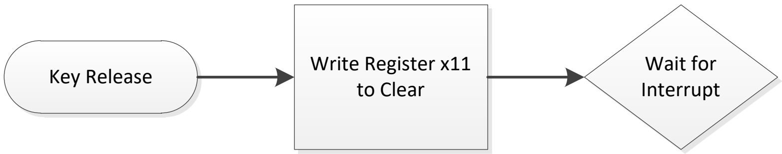


Figure 5. Key Release Flowchart

4. ADC Digital Block

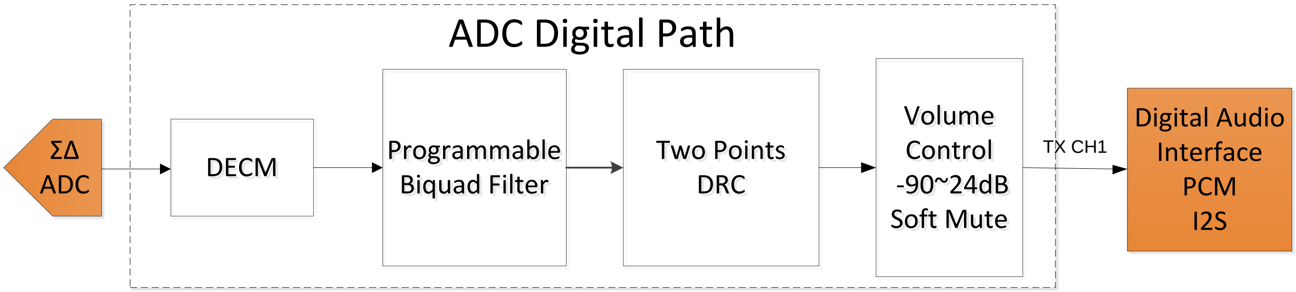


Figure 6: ADC Digital Path

The ADC digital block takes the output of the 24-bit Analog-to-Digital converter and performs signal processing aimed at producing a high quality audio sample stream to the audio path digital interface. The Figure 7 shows the various steps associated with the ADC digital path.

Oversampling is used to improve noise and distortion performance; however this does not affect the final audio sample rate. The oversampling rate configured between 32X and 256X using register settings.
The polarity of either ADC output signal can be changed independently on either ADC logic output as a feature sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data is passed to other stages in the system.

The full-scale input level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0VRMS.

4.1 ADC Dynamic Range Compressors (DRC)

The ADC's in the digital signal path each support a two-point dynamic range compressor (DRC) for advanced signal processing. Each DRC can be programmed to limit the maximum output level and/or boost a low output level signal. The DRC's function consists of level estimation and static curve control.

4.1.1 Level Estimation

The NAU88L21 uses Peak level estimation that depends on the attack and decay time settings, which can be programmable by register settings as shown in the Table 2.

BITS	DRC_PK_COEF1_ADC	DRC_PK_COEF2_ADC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

Table 2: ADC Level Estimation - Attack and Decay Time Register Settings

Please note that Ts is the sampling time given by 1/(Sampling Frequency)

4.1.2 Static Curve

The DRC static curve supports up to five programmable sections as shown in the Figure 6.

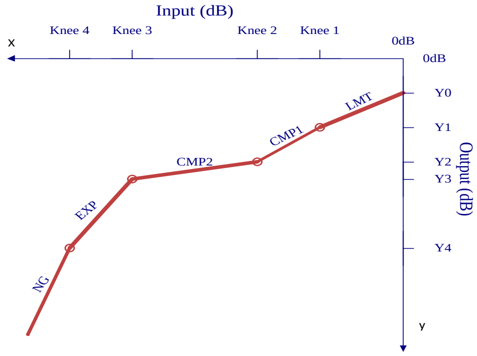


Figure 8: DRC Static Characteristic

Each section on the characteristic (labeled NG, EXP, CMP2, CMP1, and LMT) can be controlled by setting the slope and knee point values, in their respective registers. The table below provides the corresponding register locations.

Static Curve Section	Slope	Knee Point
LMT	0, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1	
CMP1	0, 1/2, 1/4, 1/8, 1/16, 1	0 to -31dB with -1dB step
CMP2	0, 1/2, 1/4, 1/8, 1/16, 1	0 to -63dB with -1dB step
EXP	1, 2, 4	-18 to -81dB with -1dB step
NG	1, 2, 4, 8	-35 to -98dB with -1dB step

Table 3: ADC DRC Static Curve control registers

The output Y values can be determined based on the slopes and knee points selected. Y1 is always equal to Knee 1, as an initial and default condition.

Y1 = Knee 1
Y0 = Y1 - (Knee 1) * (LMT Slope)
Y2 = (Knee 2 - Knee 1) * (CMP1 Slope) + Y1
Y3 = (Knee 3 - Knee 2) * (CMP2 Slope) + Y2
Y4 = (Knee 4 - Knee 3) * (EXP Slope) + Y3

The attack time and decay time is programmable as shown in the Table 4. And the smooth knee filter can be also enabled by register setting.

BITS	DRC_ATK_ADC_CH##	DRC_DCY_ADC_CH##
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4905*Ts
0111	255*Ts	8191*Ts
1000	511*Ts	16383*Ts
1001	1023*Ts	32757*Ts
1010	2047*Ts	65535*Ts
1011	4095*Ts	
1100	8191*Ts	

Table 4: ADC Attack and Decay Time Register Settings

4.2 ADC Digital Volume Control

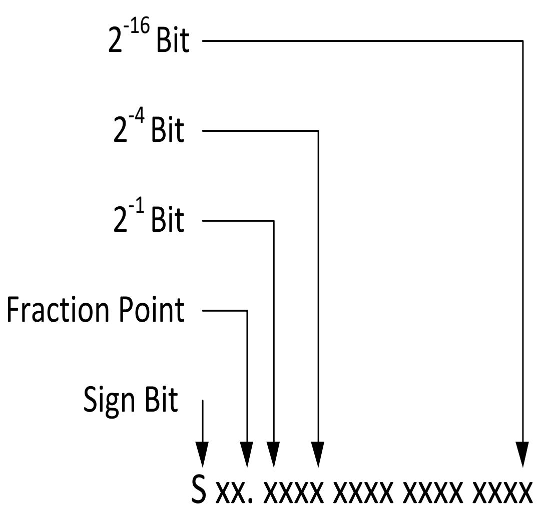
The digital volume control feature allows adjustment of the audio volume coming from ADC using a two-stage volume control. This allows the gain to be adjusted from -103dB to +24dB. Also included is a mute value that will reduce the output signal of the ADCs to zero.

4.3 ADC Programmable Biquad Filter

The NAU88L21 has 4 dedicated digital biquad filters. Two for the ADC path, and two for the DAC path. The biquad filter is a second-order recursive linear filter with two poles and two zeros. Its transfer function is the Z-domain consists of two quadratic functions:

$$H(z) = \frac{B_0 + B_1 Z^{-1} + B_2 Z^{-2}}{1 + A_1 Z^{-1} + A_2 Z^{-2}}$$

The coefficients A_1, A_2, B_0, B_1, B_2 are represented in the 3.16 format described below



Each Biquad Coefficient has 19 bits in Sxx.16 format where

- S is the sign bit (1 bit),
- xx are integers (2bits)
- 16 fractional bits (16 bits)

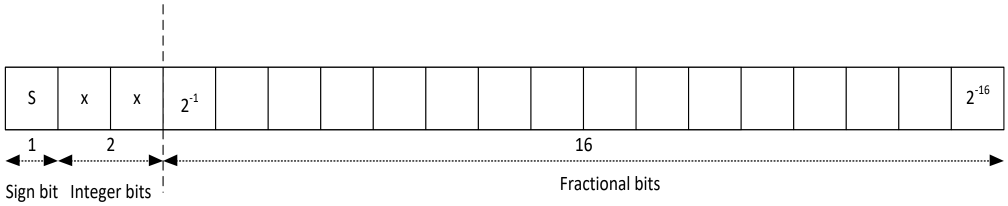


Figure 9: Number format description for biquad filters coefficients.

4.4 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates using non-linear algorithms. The NAU88L21 supports the two main telecommunications companding standards on both transmit and receive sides: A-law and µ-law. The A-law algorithm is primarily used in European communication systems and the µ-law algorithm is primarily used by North America, Japan, and Australia.

4.5 Additional ADC Application Notes

The ADC clock polarity can be inverted if necessary by register setting. It is recommend to match ADC oversampling rate with ADC clock rate as shown in the Table 5.

ADC_RATE	CLK_ADC_SRC
00(OSR=32)	11(CODEC 1/8)
01(OSR=64)	10(CODEC1/4)
10(OSR=128)	01(CODEC 1/2)
11(OSR=256)	00(CODEC CLK)

Table 5: ADC_RATE and CLK_ADC_SRC Pairs

5. DAC Digital Block

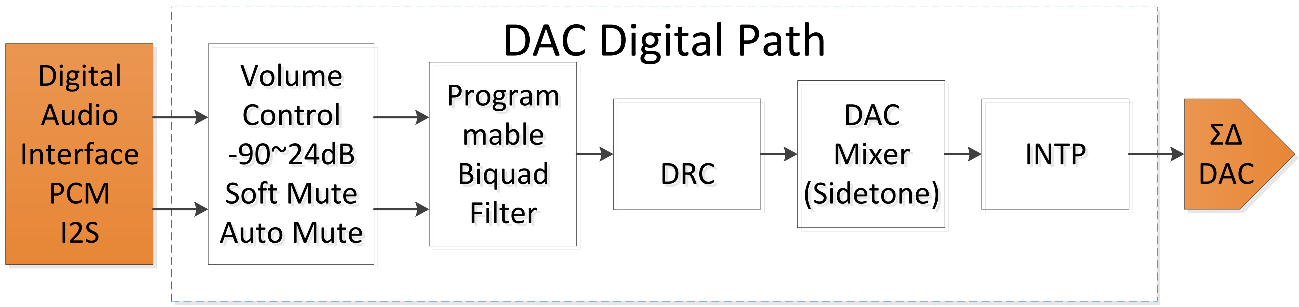


Figure 10: DAC Digital Path

The DAC digital block uses 24-bit signal processing to generate analog audio with a 16-bit digital sample stream input. This block consists of a sigma-delta modulator, digital decimator/filter, programmable biquad filter, and a DRC. The full-scale output level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0 VRMS. The oversampling rate of the DAC can be changed from 32x to 256x for improved audio performance at higher power consumption. The DAC output signal polarity can be changed using register setting. This can help minimize any audio processing that may be required as the data is passed from other stages of the system.

5.1 DAC Dynamic Range Control (DRC)

The DAC DRC functions in the same way as the ADC DRC explained in Section 4.1. However, different control registers are used.

5.1.1 Level Estimation

The Table 6 shows the attack and decay times for the peak level estimation. And, the time constant Ts is the the sampling time given by 1/(Sampling Frequency).

BITS	DRC_PK_COEF1_ADC	DRC_PK_COEF2_ADC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

Table 6: DAC Level Estimation Attack and Decay Time Register Settings

5.1.2 Static Curve

The DRC static curve supports five programmable sections, and slope and knee points can be configured as shown in the Table 7.

Static Curve Section	Slope	Knee Point
LMT	0, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1	
CMP1	0, 1/2, 1/4, 1/8, 1/16, 1	0 to -31dB with -1dB step
CMP2	0, 1/2, 1/4, 1/8, 1/16, 1	0 to -63dB with -1dB step
EXP	1, 2, 4, 8	-18 to -81dB with -1dB step
NG	1, 2, 4, 8	-35 to -98dB with -1dB step

Table 7: DAC DRC Static Curve Control Registers

The Table 8 shows the attack and decay time for DRC. And, it needs to be carefully used combination with cross talk function because DRC is the last blocks in the path after mixer. Small cross-talk signal might be filtered out by DRC. The smooth knee function can be also enabled by register setting.

BITS	DRC_ATK_DAC	DRC_DCY_DAC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts
1000	511*Ts	16383*Ts
1001	1023*Ts	32757*Ts
1010	2047*Ts	65535*Ts
1011	4095*Ts	
1100	8191*Ts	

Table 8: DAC Static Curve Attack and Delay Time Register Settings

5.2 DAC Digital Volume Control, Mute and Channel selection

DACL and DACR both have separate digital volume controls that allow the user to adjust the gain from -103dB to +24dB in 0.5dB steps as well as mutes. Left and Right channels can be adjusted separately and control is accessed through register settings.

5.3 DAC Soft Mute

The soft mute function ramps the DAC digital volume down to zero when enabled. When disabled, the volume increases to the register specified volume level for each channel. This feature provides a tool that is useful for using the DAC without introducing pop and click sounds.

5.4 DAC Auto Attenuate

Auto-attenuate can greatly increase the perceived SNR during playback of silence. The last analog output stage is attenuated such that the noise contribution of the preceding stages is eliminated. The use of auto-attenuate by attenuating the analog output on a DAC path when the digital input represents a zero signal needs to be done gradually in order to avoid audible pops due to sudden offset changes. It is desirable to slowly ramp down the gain of the analog output stage to the maximum attenuation level. This function will be referred to as auto-attenuate. The auto-attenuate feature is used to increase the Signal to Noise Ratio. In addition, the auto attenuate logic can be used to attenuate the analog output manually,saving some software routines and allowing pop-less ramp up and down of the analog outputs with little register writes.

The auto-attenuate function can be enabled manually or automatically. In the automatic mode, if both the left and right channel receive 1024 consecutive samples of „0", then it will read and store the value of the headset driver volume control into internal temporary registers and then attenuate the headset driver output by 1dB for every 128 samples, until -54dB is reached (54 steps maximum). If , at any time, the I2S DACIN signal receives non-zero signal samples, the headset output driver gain is increased by 1dB per step and in 1, 16, 32 or 128 samples per step (programmable by register) until the gain will be stepped up until the original gain setting is reached. In the manual mode, once enabled, it will immediately start saving the volume control into temporary registers and attenuate signals by 1dB for every 128 samples untile -54dB is reached. If the manual attenuate is disabled, the gain will be fully recovered by 1dB step in 1, 16, 32, or 128 samples per step.

5.5 DAC Path Digital Mixer with Side tone

The NAU88L21 implements a channel based digital mixer architecture. Each DAC outputs can be selected between the different inputs. The ADC input channels, I2S channels are capable of being mixed into either output of the DAC. The figure below shows a block diagram of how the mixer works along with the related registers.

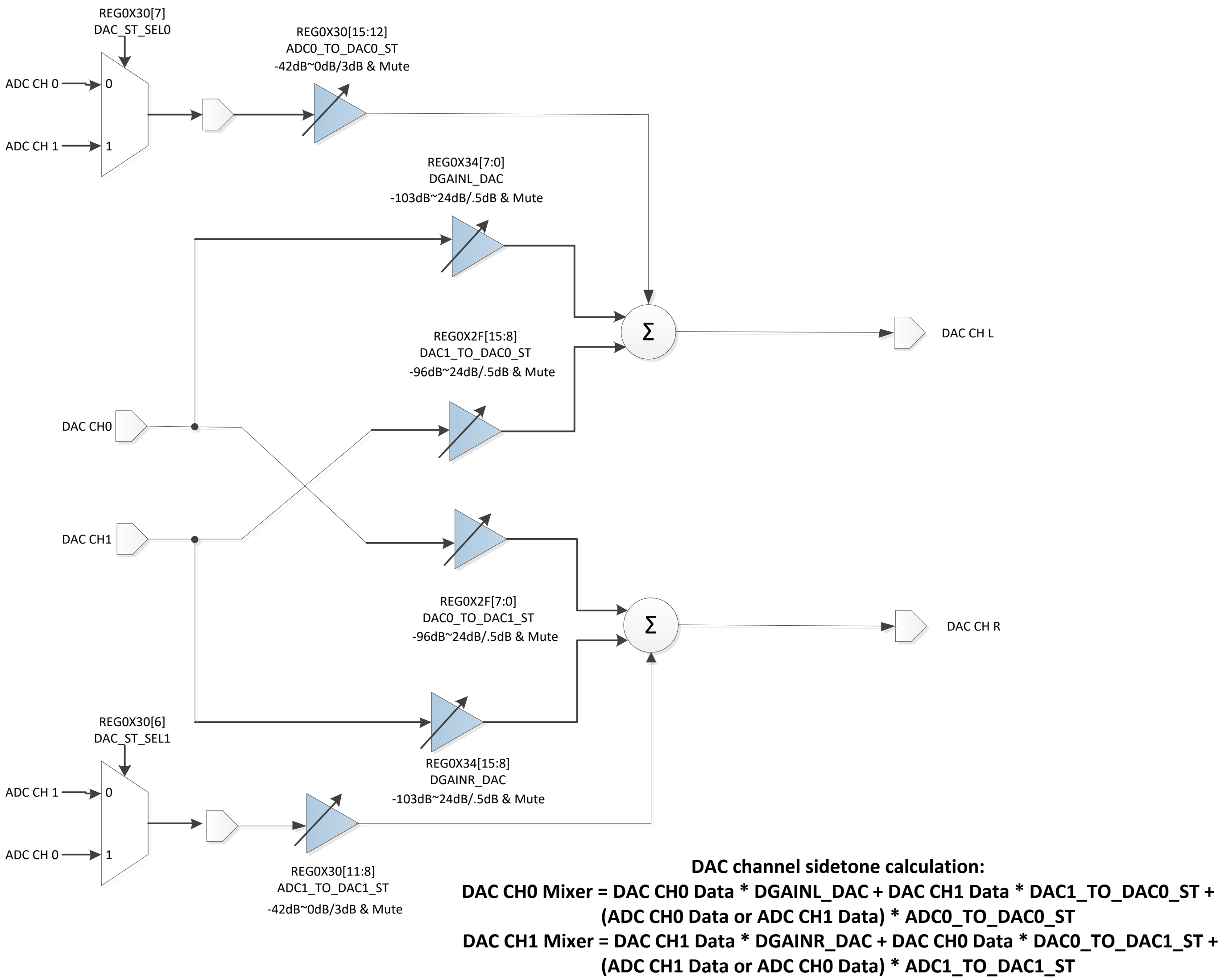


Figure 11: DAC Path Digital Mixer with Side tone.

5.6 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates using non-linear algorithms. The NAU88L21 supports the two main telecommunications companding standards on both transmit and receive sides: A-law and μ-law. The A-law algorithm is primarily used in European communication systems and the μ-law algorithm is primarily used by North America, Japan, and Australia.

Companding converts 14 bits (μ-law) or 13 bits (A-law) to 8 bits using non-linear quantization resulting in 1 sign bit, 3 exponent bits and 4 mantissa bits. When the companding mode is enabled, 8 bit word operation must be enabled.

Sections 5.6.1 and 5.6.2 contain the compression equations set by the ITU-T G.711 standard and implemented in the NAU88L21.

5.6.1 μ-law

$$F(x) = \frac{\ln(1 + \mu \times |x|)}{\ln(1 + \mu)}, \qquad -1 < x < 1$$

$$\mu = 255$$

5.6.2 A-law

$$F(x) = \frac{A \times |x|}{(1 + \ln(A))}, \qquad 0 < x < \frac{1}{A}$$

$$F(x) = \frac{(1 + \ln(A \times |x|)}{(1 + \ln(A))}, \qquad \frac{1}{A} \leq x \leq 1$$

$$A = 87.6$$

6. Clocking and Sample Rates

The internal clocks for the NAU88L21 are derived from a common internal clock source. This master system clock can set directly by the MCLK pin input or it can be generated from a Frequency Locked Loop (FLL) using the MCLK_PIN, BCLK or FS as a reference. While most of the common audio sample rates can be derived directly from typical MCLK frequencies, the FLL provides additional flexibility for a wide range of MCLK inputs or as a free running clock in the absence of an external reference.

The figures below is a block diagram illustrating how the various register settings can be used to adjust/select the MCLK, BCLK, FS, and ADC_CLK clock frequency.

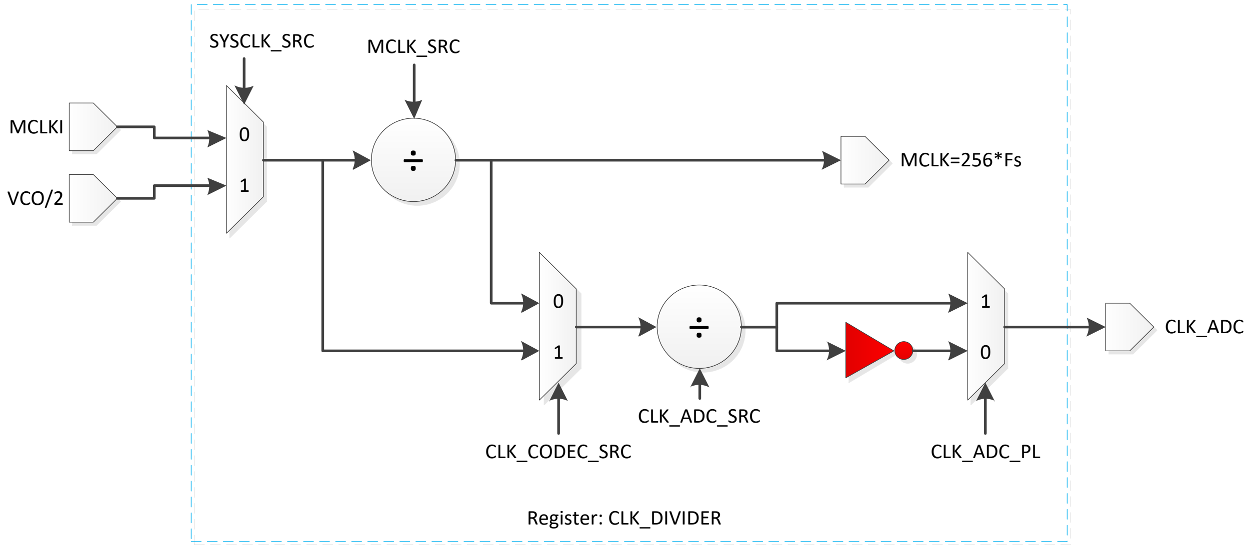


Figure 12: MCLK and ADC_CLK Frequency Selection

Bits	MCLK_SRC
0000	Divide by 1
0001	Invert
0010	Divide by 2
0011	Divide by 4
0100	Divide by 8
0101	Divide by 16
0110	Divide by 32
0111	Divide by 3
1001	Invert
1010	Divide by 6
1011	Divide by 12
1100	Divide by 24
1101	Divide by 48
1110	Divide by 96
1111	Divide by 5

Table 9: Register Settings

Bits	CLK_ADC_SRC
00	Divide by 1
01	Divide by 2
10	Divide by 4
11	Divide by 8

Table 10: Register Settings

The internal clock frequency MCLK must be running at 256*Fs (Fs = sample rate in Hz) in order to achieve the best performance. The internal clock frequency MCLK can also run at 400*Fs or 500*Fs, which may give a slightly lower performance. For example, when targeting 48 kHz sample rate audio, the MCLK must be set to 256*48k = 12.288MHz, 400*48k = 19.2MHz, or 500*48k = 24MHz. When the input clock MCLKI is higher than this speed, register **CLK_DIVIDER.MCLK_SRC REG0x03[3:0]** provides a flexible divider selection to meet this requirement. The FLL can also be used to generate an MCLK that meets this requirement.
The OSR (over sampling rate) is defined as CLK_ADC frequency divided by the audio sample rate.

$$OSR = \frac{CLK\_ADC}{Fs}$$

Available over-sampling rates are 32, 64, 128 or 256 as set in the **ADC_RATE.ADC_RATE REG0X2B[1:0]** register. CLK_ADC frequency is set by **CLK_DIVIDER.CLK_CODEC_SRC REG0X03[13]** and **CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6]** registers.
It should be noted that the OSR and Fs must be selected so that the max frequency of CLK_ADC is less than or equal to 6.144MHz. When CLK_ADC is determined, **ADC_RATE.ADC_RATE REG0X2B[1:0]** should be set to provide appropriate down sampling through digital filters.
There are two special cases in which the OSR will be 100. If MCLK is 400 or 500 times the input sample rate of the DAC or the output sample rate of the ADC, the OSR will be 100. In the first case, set **CLK_DIVIDER.CLK_ADC_SRC_REG0X3[7:6]**=2'b10 (1/4) for ADC path, and DAC path need to set **CLK_DIVIDER.CLK_DAC_SRC_REG0X3[5:4]**=2'b10 (1/4) and **DAC_RATE.DAC_CTRL1_REG0X2C[2:0]**=3b'000 , in the second case the clock to the ADC and DAC will be adjusted automatically.

Example 1:
To configure Fs = 48 kHz, MCLK = (256*Fs) = 12.288MHz, and CLK_ADC = 6.144MHZ
Set:

- SYSCLK_SRC = MCLK
- CLK_ADC_SRC = 1/2
- ADC OSR = 128

Example 2:
To configure Fs = 16 kHz, MCLKI = 12.288MHz, and CLK_ADC = 4.096MHz
Set:

- SYSCLK_SRC = MCLK
- MCLK_SRC = 1/3
- CLK_ADC_SRC = 1
- ADC OSR = 256

6.1 I2S/PCM Clock Generation

In master mode, BCLK can be derived from MCLK via a programmable divider, and the FS can be derived from BCLK via another programmable divider.

To select specific Fs values, both dividers must be set according to the block diagram and the equation below.

$$BCLK = Fs \times data\ \ length \times channels$$

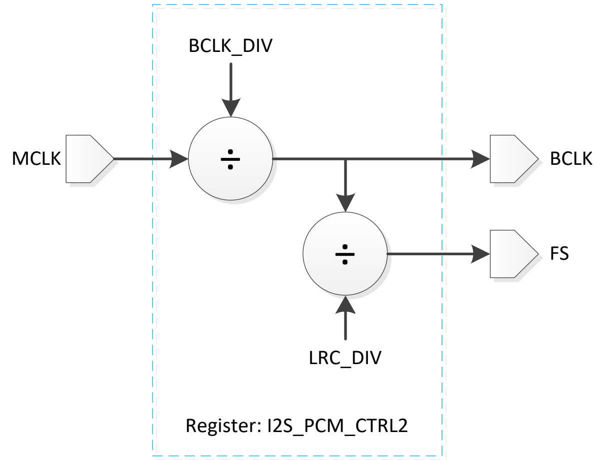


Figure 13: BCLK and FS Frequency Selection

Bits	BCLK_DIV
000	Divide by 1
001	Divide by 2
010	Divide by 4
011	Divide by 8
100	Divide by 16
101	Divide by 32

Table 11: Register Settings

Bits	LRC_DIV
000	Divide by 256
001	Divide by 128
010	Divide by 64
101	Divide by 32

Table 12: Register Settings

Example 1:
If we want an Fs of 48 kHz and 16 bit data is to be sent to the I2S bus (2 channel)

- BCLK = 48000*16*2 = 1.536MHz and MCLK = 48000*256 = 12.288MHz
- Set BCLK_DIV = 1/8
- Set LRC_DIV = 1/32

Or 32 bit data is to be sent

- BCLK = 48000*32*2 = 3.073MHz and MCLK = 48000*256 = 12.288MHz
- Set BCLK_DIV = 1/4
- Set LRC_DIV = 1/64

Example 2:
If we want an Fs of 16 kHz and 16 bit data is to be sent to the I2S bus (2 channel)

- BCLK = 16000*16*2 = 512kHz and MCLK = 16000*256 = 4.096MHz
- Set BCLK_DIV = 1/8
- Set LRC_DIV = 1/32

32 bit data is to be sent,

- BCLK = 16000*32*2 = 1.024MHz and MCLK = 16000*256 = 4.096MHz
- Set BCLK_DIV = 1/4

- Set LRC_DIV = 1/64
-

Example 3:
If we want an Fs of 16 kHz and 32 bit data is to be sent to the I2S TDM bus (4 channels)

- BCLK = 16000*32*4 = 2.048MHz and MCLK = 16000*256 = 4.096MHz
- Set BCLK_DIV = 1/2
- Set LRC_DIV = 1/128

6.2 Frequency Locked Loop(FLL)

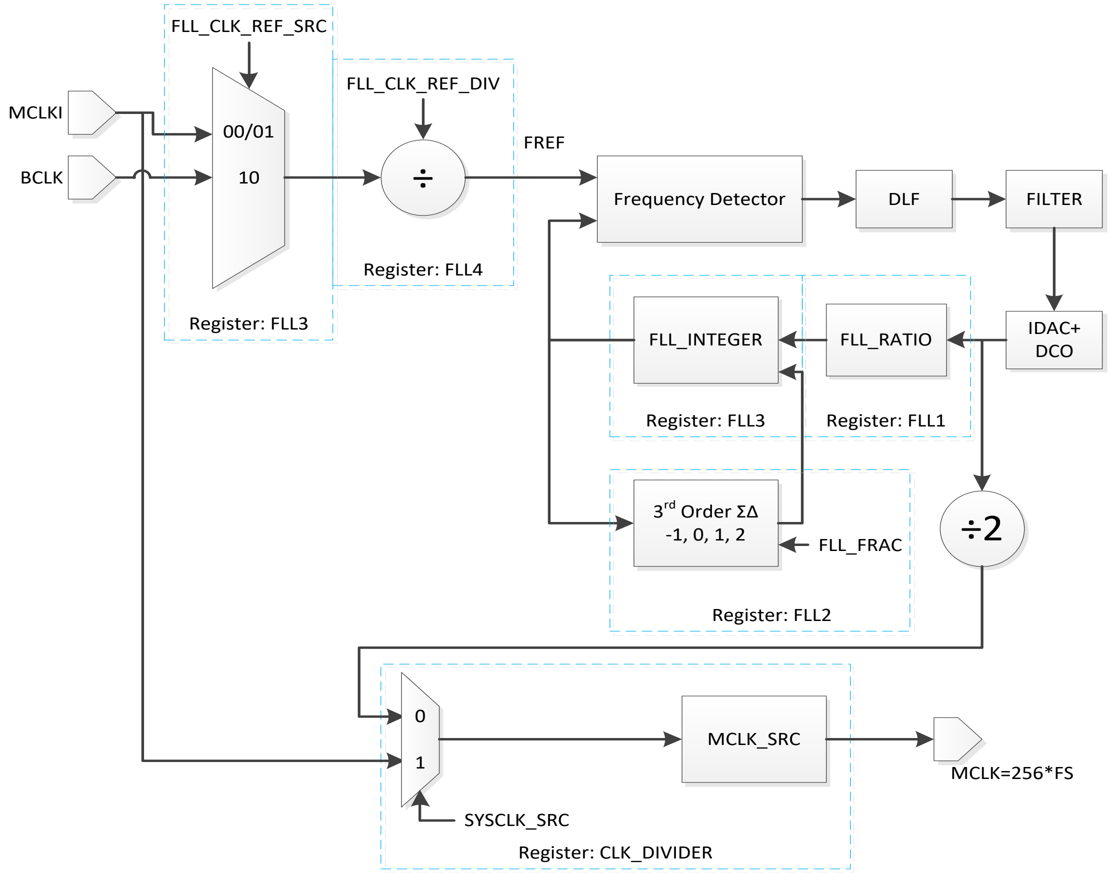


Figure 14: FLL Block diagram

The integrated FLL can be used to generate a SYSMCLK from a wide variety of reference sources such as, MCLK, BCLK, and FS or as a free running clock in the absence of an external reference. It can also create a stable SYSMCLK from less stable sources due to its tolerance of jitter.
The FLL output frequency is determined by the following parameters.

- FLL_RATIO based on input clock frequency
- MCLK_SRC Divider
- FLL_INTEGER: 10 bit Integer Input
- FLL_FRAC: 16 bit Fractional Input
- FLL_CLK_REF_DIV Divider

To determine these settings, the following output frequency equations are used.

1. FDCO = (FREF / FLL_CLK_REF_DIV) X FLL_INTEGER.FLL_FRAC X FLL_RATIO
2. MCLK = (FDCO X MCLK_SRC) / 2

Where FREF is the reference clock frequency for FLL, MCLK is the desired system frequency, and FDCO is the frequency of DCO in decimal.

Example:
If the reference frequency (FREF) is 12MHz, the desired sampling rate (Fs) is 48 kHz, and SYSCLK = 256Fs, what are the output frequency parameters?

Using these requirements, the following can be determined.

- MCLK = 256 × 48kHz = 12.288MHz
- Using Equation 2:
  - FDCO = 2 X MCLK / MCLK_SRC = 2 X 12.288MHz X MCLK_SRC
    - For FDCO to remain between 90MHz – 100MHz, MCLK_SRC must be chosen to be 1/4. This and other values for MCLK_SRC can be seen on the register tables.
  - FDCO = (2 × 12.288MHz) / (1/4) = 98.304MHz
- Using Equation 1:
  - FLL_INTEGER.FLL_FRAC = FDCO X FLL_CLK_REF_DIV / (FREF X FLL_RATIO)
    - FDCO = 98.304MHz
    - FLL_RATIO = 1 because of FREF ≥ 512 kHz.
    - FLL_CLK_REF_DIV = 1 since FREF = MCLKI (12MHz)
  - FLL_INTEGER.FLL_FRAC = 98.304MHz X 1 / (12MHz X 1) = 8.192
- Now retrieve or convert the parameter values into their corresponding HEX values
  - FLL_RATIO = 1 (for input clock frequency ≥ 512Khz)
  - MCLK_SRC = 1/4
  - FLL_INTEGER = 8
  - FLL_FRAC = 0.192 = 12583 (0.192 X 2^16) = 24’h3126

Please Note:

- FLL_CLK_REF_DIV can be used to reduce the reference frequency for SYSMCLK by dividing the input by 1, 2, 4, or 8. Use this to ensure the reference clock frequency is less than or equal to 13.5MHz.
- FDCO must be within the 90MHz – 100MHz or the FLL cannot be guaranteed across the full range of operation.
- FLL_FRAC must be set to 0 for low power mode.

- FLL6.SDM_EN REG0X09[14] to create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not a integer . If the ratio is integer, it still can be on for lower noise output but higher power consumption.
- When FLL uses free running mode, NAU88L21 needs to be set as a master in I2S_PCM_CTRL2.MS0 REG0X1D[3]=1
- Set FLL6.CHB_FILTER_EN REG0X08[14] = ‘1’ to enable FLL Loop Filter. Select filter clock source by FLL6.CHB_FILTER¬_EN REG0X08[13]. Select DCO input by FLL6.FILTER_SW REG0X08[12]. FLL6.CUTOFF500 REG0X09[13] & FLL6.CUTOFF600 REG0X09[12] can be used to define FLL cuttoff frequency at 500KHz or 600KHz. 500KHz will provide the best FLL performance but consume more power.
- set FLL6.FLL_FLTR_DITHER_SEL REG0X09[7:6] = ‘01’ or ‘10’ or ‘11’ as 1LSB / 2LSB / 3LSB random bits to Randomize the number of Filter Output Bits to average out output noise. If ‘00’, there is no dither.

7. Control Interfaces

The NAU88L21 includes a serial control bus that provides access to all the device control registers, it may be configured as a 2-wire interface that conforms to industry standard implementations of the I^2C serial bus protocol.

7.1 2-Wire-Serial Control Mode (I^2C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and any device receiving data as the receiver (or slave). The NAU88L21 can function only as a slave when in the 2-wire interface configuration.

7.2 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

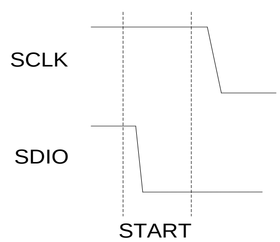


Figure 15: Valid START Condition

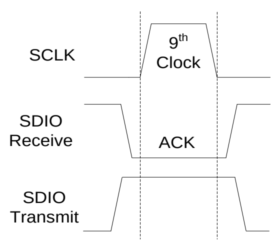


Figure 16: Valid Acknowledge

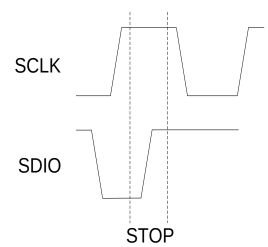


Figure 17: Valid STOP Condition

Please Note:

- Sometimes, I2C needs to use level shifter between different supplies domains. During Acknowledge, such as Figure 16, receiver side (CODEC) will pull low, and transmit side (MCU) is disable and pull high by pull high resistor. Because NAU88L21 SDIO can sink 2mA by default setting (maximum up to 8mA,) shown as below Figure 18, R_{PU1} and R_{PU2} need to be select such that total current VDDB/R_{PU1}+ VDD_MCU/R_{PU2} during Acknowledge should not be too large to exceed SDIO sinking capability.

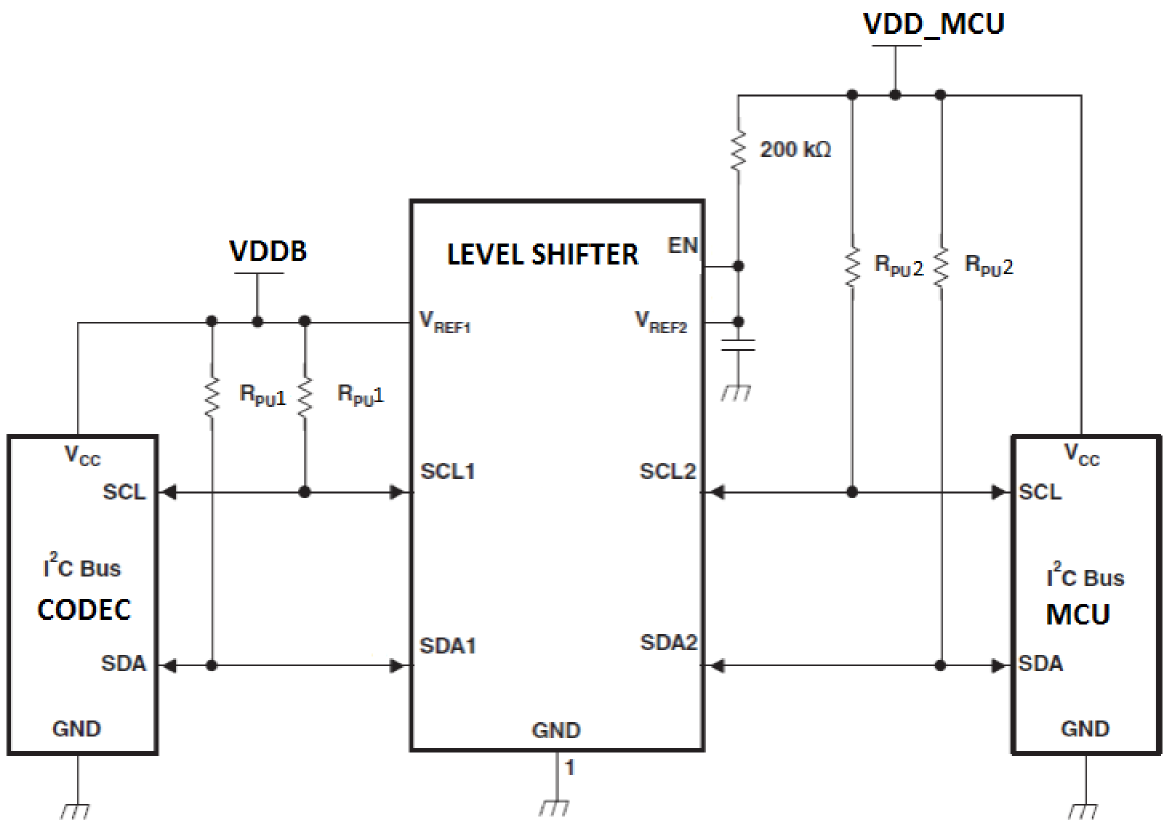


Figure 18: Typical I2C level shifter circuit

7.3 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition.

The Device Address of the NAU88L21 is either 0x1B (CSB=0) or 0x54 (CSB=1). If the Device Address matches this value, the NAU88L21 will respond with the expected ACK signaling as it accepts the data being transmitted to it.

0	0	1	1	0	1	1	R/W	Device Address Byte
A15	A14	A13	A12	A11	A10	A9	A8	Control Address Bytes
A7	A6	A5	A4	A3	A2	A1	A0	
D15	D14	D13	D12	D11	D10	D9	D8	Data Bytes
D7	D6	D5	D4	D3	D2	D1	D0	

Figure 19: Slave Address Byte, Control Address Byte, and Data Byte

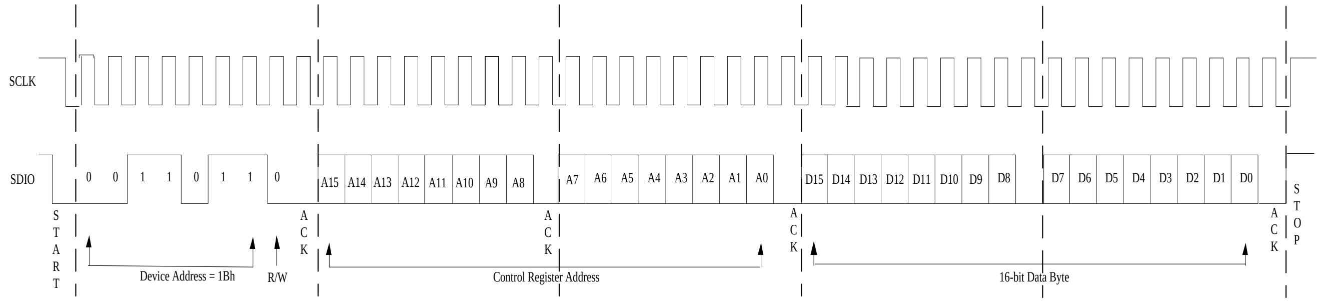


Figure 20:2-Wire Write Sequence

7.4 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

If the device address matches this value, the NAU88L21 will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU88L21 transmits an ACK, followed by a two byte value containing the 16 bits of data from the selected control register inside the NAU88L21.

During this phase, the master generates the ACK signaling with each byte transferred from the NAU85L40. If there is no STOP signal from the master, the NAU88L21 will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU88L21 reaches the value 0xFFFF (hexadecimal) and the value for this register is output, the index will roll over to 0x0000. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

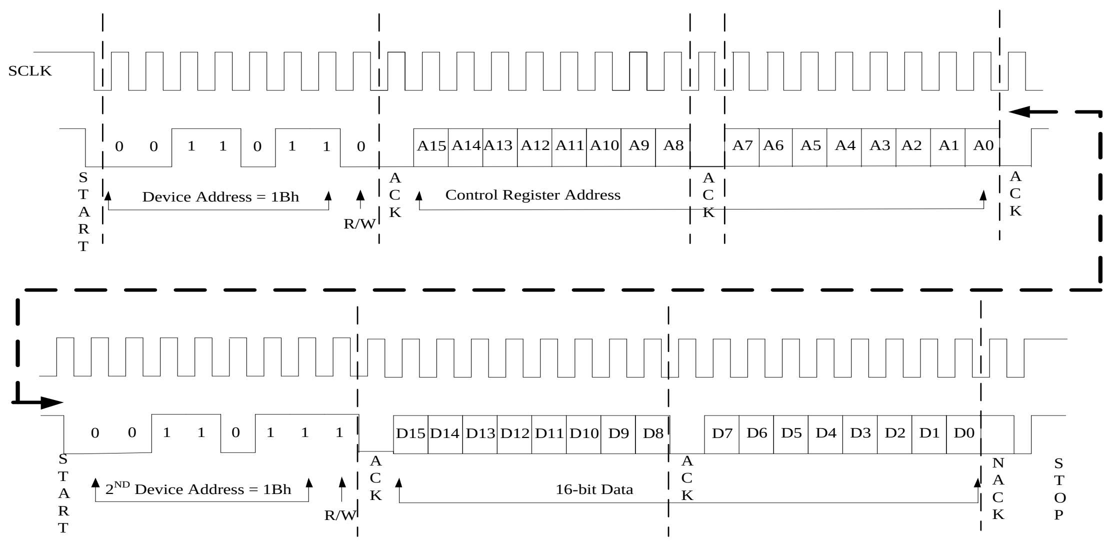


Figure 21:2-Wire Read Sequence

7.5 Digital Serial Interface Timing

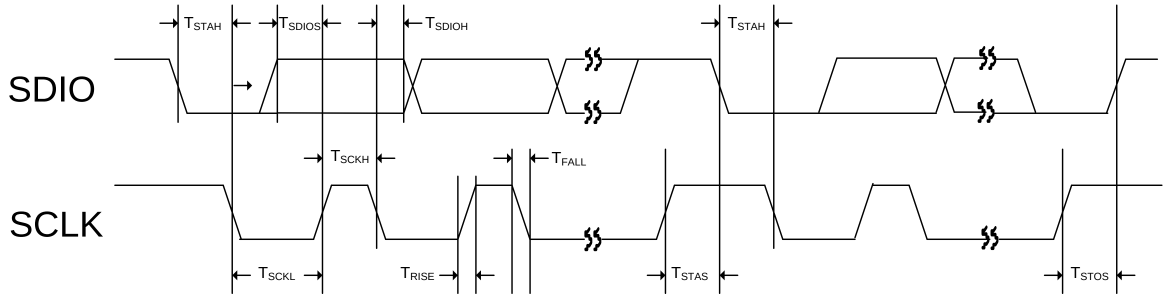


Figure 22: Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{STAH}	SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SCLK rising edge to SDIO falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SCLK rising edge to SDIO rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCLK High Pulse Width	600	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	100	-	-	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

7.6 Software Reset

The NAU88L21 and all of its control registers can be reset to “default”, initial conditions by writing any value to REG0X00 using the two-wire interface mode.

8. Digital Audio Interfaces

The NAU88L21 can be configured as either the master or the slave, and the Slave mode is the default if this bit is not written. In master mode, NAU88L21 outputs both Frame Sync (FS) and the audio data bit clock (BCLK) and has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK; SDO clocks out ADC data, while SDI clocks in data for the DACs.

When not transmitting data, SDO pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. When the time slot function is enabled (see below), there are additional output state modes including controlled tristate capability.
NAU88L21 supports six audio formats; right justified, left justified, I2S, PCMA, PCMB, and PCM Time Slot.

8.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, channel_0 data is transmitted and when FS is LOW, channel_1 data is transmitted. This can be seen in the image below.

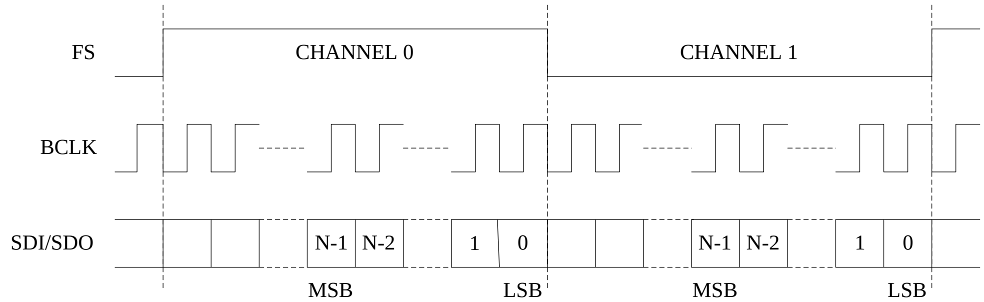


Figure 23: Right-Justified Audio Interface

8.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, channel_0 data is transmitted and when FS is LOW, channel_1 data is transmitted. This can be seen in the figure below.

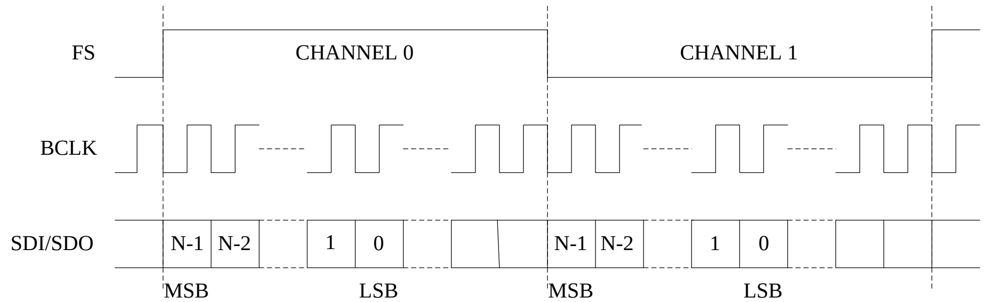


Figure 24: Left-Justified Audio Interface

8.3 I2S Audio Data

In I²S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This can be seen in the figure below.

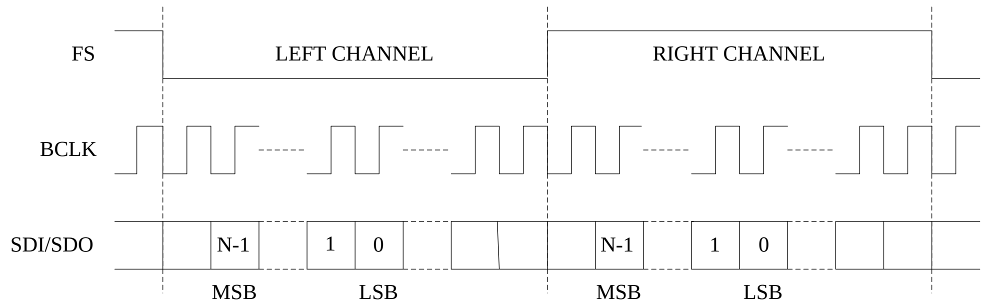


Figure 25: I2S Audio Interface

8.4 PCMA Audio Data

In the PCM A mode, channel 0 data is transmitted first followed immediately by channel 1 data. The channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and channel 1 MSB is clocked on the next BCLK after the left channel LSB. This can be seen in the figure below.

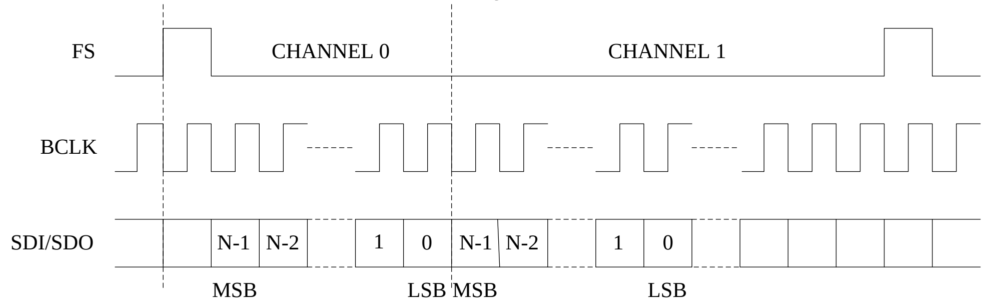


Figure 26: PCMA Audio Interface

8.5 PCMB Audio Data

In the PCMB mode, channel_0 data is transmitted first followed immediately by channel_1 data. Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel_1 MSB is clocked on the next BCLK after channel_0 LSB. This can be seen in the figure below.

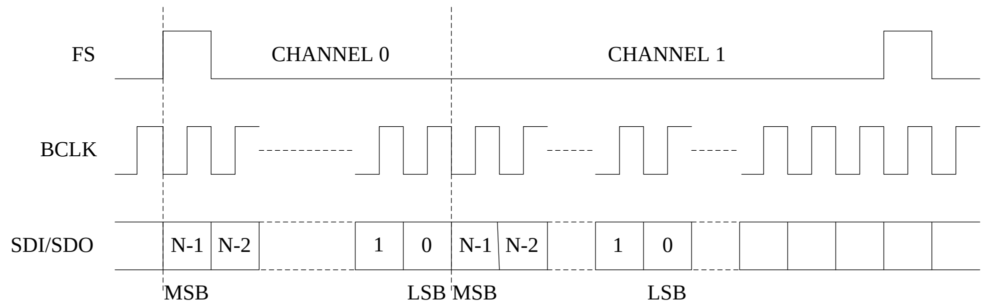


Figure 27: PCMB Audio Interface

8.6 PCM Time Slot Audio Data

The PCM time slot mode is used to allocate different time slots for ADC and DAC data. This can be useful when multiple NAU88L21 chips or other devices are sharing the same audio bus. This will allow each chip‟s audio to be delayed around each other without interference.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS), however, in the PCM time slot mode; the audio data can be delayed by left / right channel PCM time slot start value in the registers.

These delays can be seen before the MSB in the figure below.

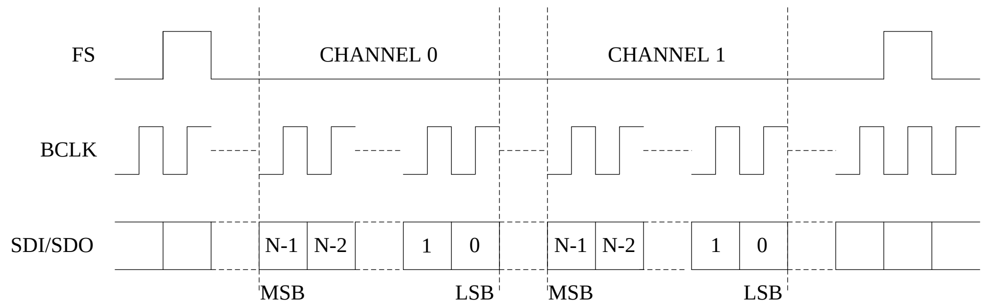


Figure 28: PCM Time Slot Audio Interface

The PMC time slot mode can be also used to swap channel 0 and channel 1 audio or cause both channels to use the same data. When using the NAU88L21 with other driver chips, the SDO pin can be set to pull up or pull down or high impedance during no transmission. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots with reduced risk of bus driver contention.

8.7 TDM I2S Audio Data

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, channel_0 then channel_2 data is transmitted and when FS is HIGH, channel_1 then channel_3 data is transmitted. This is shown in the figure below.

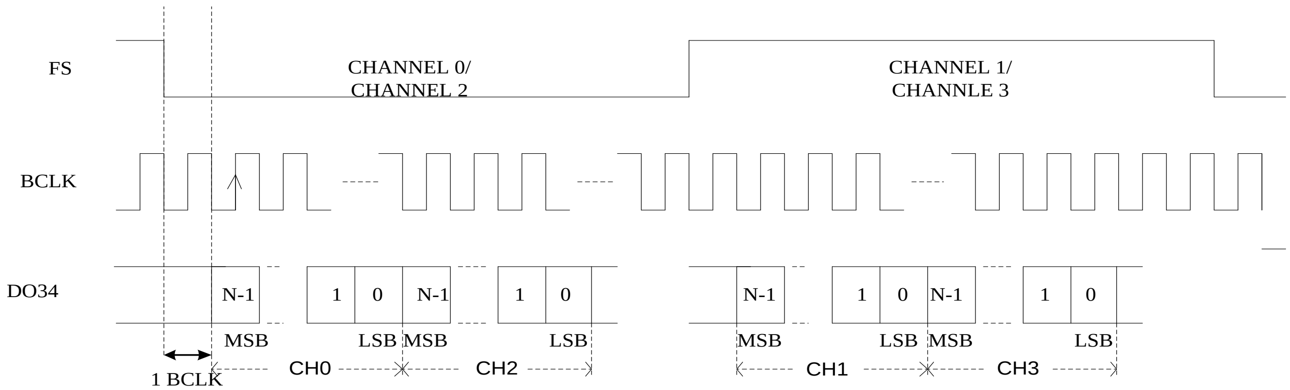


Figure Figure 29: TDM I2S Audio Format

8.8 TDM PCMA Audio Data

In the PCMA mode, channel_0 data is transmitted first followed sequentially by channel_1, 2, and 3 immediately after. The channel_0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel’s MSB is clocked on the next BCLK after the previous channel’s LSB. This is shown in the figure below.

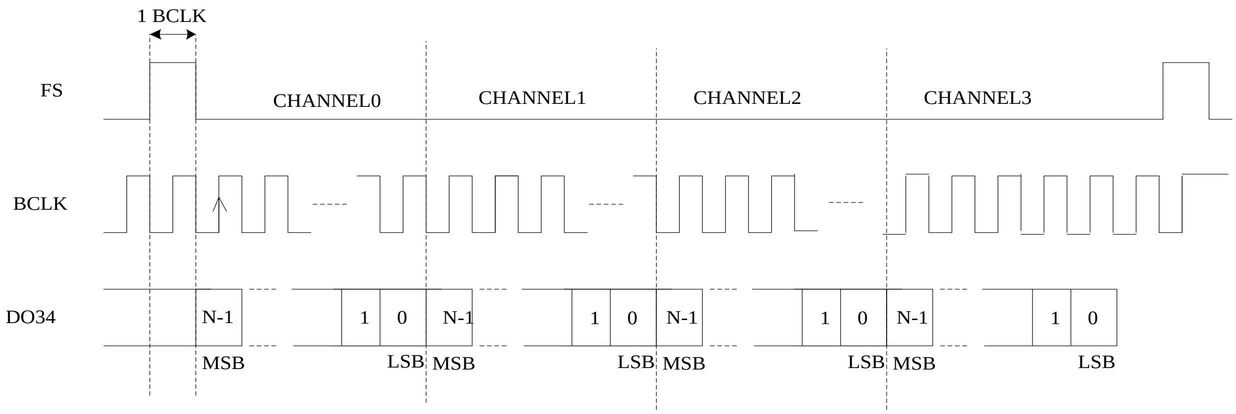


Figure Figure 30: TDM PCMA Audio Format

8.9 TDM PCMB Audio Data

In TDM PCMB mode, channel_0 data is transmitted first followed immediately by channel_1 data. The channel_0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel_1 MSB is clocked on the next SCLK after channel_0 LSB.

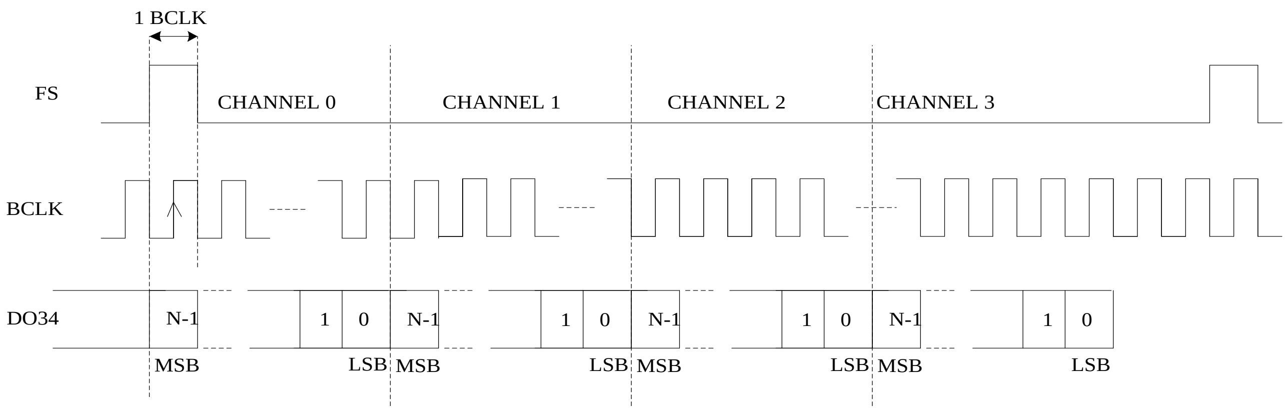
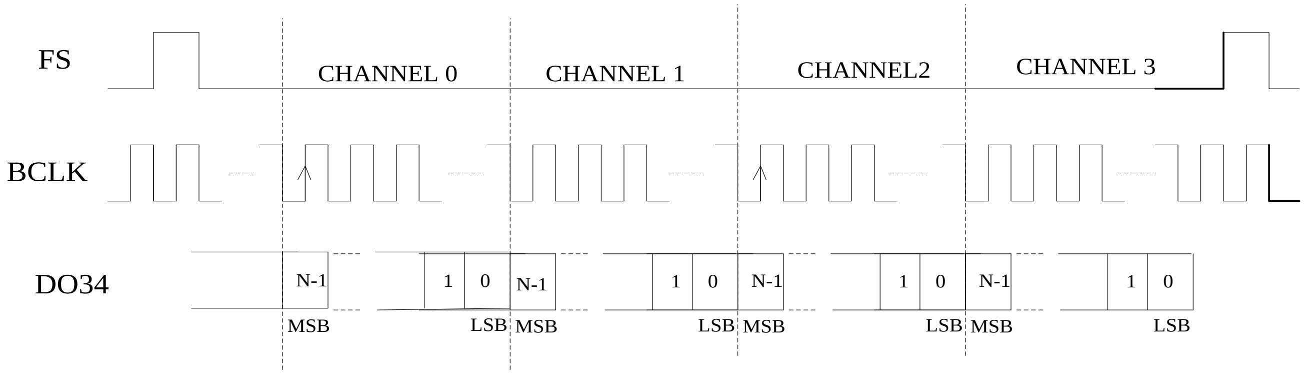


Figure 31: TDM PCMB Audio Format

8.10 TDM PCM Offset Audio Data

The PCM offset mode is used to delay the time at which DAC data is clocked. This increases the flexibility of the NAU88L21 to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU88L21 or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data.

Normally, the DAC data are clocked immediately after the Frame Sync (FS). In this mode audio data is delayed by a delay count specified in the device control registers. The channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in .This can be seen in the figure below.



Figure

Figure 32: TDM PCM Offset Audio Format

9. Outputs

The NAU88L21 provides a pair of Class G ground-reference headphone outputs.

9.1 Class G Headphone Driver and Charge Pump

The NAU88L21 uses Class G speaker drivers powered by a charge pump for the headphones. For typical operation with large and small signals the charge pump provides ±1.8V and ±0.9V, respectively. These output drivers are driven by dedicated left and right DACs and can provide 30mW of power to a 32Ω load (in CSP package).

Three capacitors are needed to generate the negative voltage from the positive 1.8V. Typically, 2μF ceramic capacitors are used.

- The Fly Back capacitor is connected between pins CPCA and CPCB.
- The Positive Output Decoupling capacitor is applied from pin CPVOUTP to ground (VSSCP).
- The Negative Output Decoupling capacitor is applied from pin CPOUTN to ground (VSSCP).

The Class G will be turned on only if DAC signal level is bigger than the threshold in the register settings, and the peak output can be also configured differently by register settings.

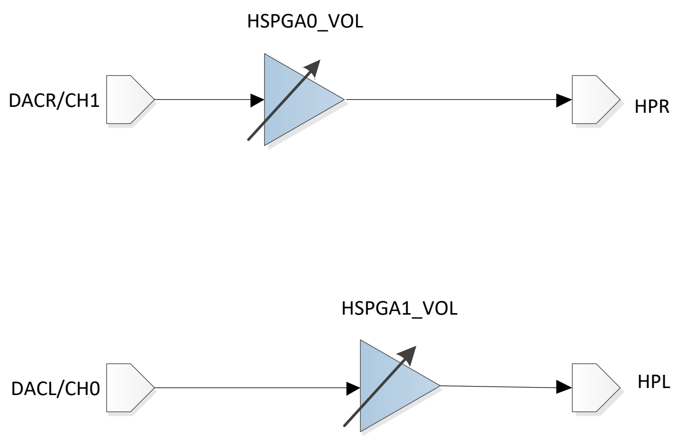


Figure 33: DAC to Headphone out path diagram

10. Control and Status Registers

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
0	HARDWARE_RST	RESET_N1																	Hardware Reset Write any value ***once*** to reset all the registers.
1	ENA_CTRL	CMLCK_ENB																	PGA Common Mode Lock; ‘0’=enabled, ‘1’=disabled
		CLK_DAC_INV																	DAC clock inversion in analog domain 1 = Enable 0 = Disable
		RDACEN																	Right Channel DAC Enable 1 = ON 0 = OFF
		LDACEN																	Left Channel DAC Enable 1 = ON 0 = OFF
		RADCEN																	Right Channel ADC Enable 1 = ON 0 = OFF
		LADCEN																	Left Channel ADC Enable 1 = ON 0 = OFF
		DCLK_ADC_EN																	ADC Clock Enable 1 = ON 0 = OFF
		DCLK_DAC_EN																	DAC Clock Enable 1 = ON 0 = OFF
		CLK_IMM_EN																	IMM Clock Enable 1 = ON 0 = OFF
		CLK_I2S_EN																	I2S Clock Enable 1 = ON 0 = OFF
		CLK_BIST_EN																	BIST Clock Enable 1 = ON 0 = OFF
		CLK_OTP_EN																	OTP Clock Enable 1 = ON 0 = OFF
		CLK_DRC_EN																	DRC Clock Enable 1 = ON 0 = OFF
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0x00ff**
3	CLK_DIVIDER	SYSCLK_SRC																	Master CLOCK sources 1 = ½ VCO_CLK 0 = MCLK_PIN
		CLK_CODEC_SRC																	ADC clock and DAC clock source selection 1 = from MCLK_PIN or ½ VCO_CLK 0 = from internal MCLK
		CLK_DAC_PL																	Invert DAC Clock Polarity in digital domain 1= Invert 0= No change
		CLK_ADC_PL																	Invert ADC Clock Polarity 1= Invert 0= No change
		CLK_GPIO_SRC																	Scaling MCLK for GPIO clock divider 00 = 1/8 01 = MCLK/2 10 = 1/2 11 = 1/4
		CLK_ADC_SRC																	Scaling for ADC clock from CODEC_SRC Output 00 = 1 01 = 1/2 10 = 1/4 11 = 1/8
		CLK_DAC_SRC																	Scaling for DCA clock from CODEC_SRC Output 00 = 1 01 = 1/2 10 = 1/4 11 = 1/8

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		MCLK_SRC																	Scaling for MCLK from SYSCLK_SRC Output 0000 = 1 0001 = Inverted 0010 = 1/2 0011 = 1/4 0100 = 1/8 0101 = 1/16 0110 = 1/32 0111 = 1/3 1000 = 1 1001 = inverted 1010 = 1/6 1011 = 1/12 1100 = 1/24 1101 = 1/48 1110 = 1/96 1111 = 1/5
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0x0050**
4	FLL1	FLLISELDAC																	Recommended default 000 FLL: Increase the drive strength of the FLL DAC.
		ICTRL_LATCH																	FLL Latch drive strength multiplier. When FLL running at high frequency with long decimal number, DSP needs to operate at high speed. By adjusting ICTRL_LATCH, FLL DSP can optimize between performance and power consumption (111 has highest power consumption for FLL DSP.) On the other hand, (DCO frequency)/(FLL input reference frequency)=integer, default setting can be used to reduce power. This register is using thermometer coding. 000 = Default 001 = 1x 011 = 2x 111 = 3x
		ICTRL_V2I																	Amp half bias-current selector. Amp bias current must be reduced to 50% of its nominal value 00 = No Power Reduction 01 = Half Bias Current on FLL_BIAS_AMP2X 10 = Half Bias Current on FLL_BIAS_AMP 11 = Half Current on Both Amps
		FLL_LOCK_BP																	Manually force FLL to lock. 0 - Default Setting 1 - Force Lock Enabled
		FLL_RATIO																	0000001 = for input clock frequency ≥ 512Khz, 0000010 = for input clock frequency ≥ 256Khz 0000100 = for input clock frequency ≥ 128Khz 0001000 = for input clock frequency ≥ 64Khz 0010000 = for input clock frequency ≥ 32Khz 0100000 = for input clock frequency ≥ 8Khz 1000000 = for input clock frequency ≥ 4Khz
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
5	FLL2	DOUT2VCO_RSV																	Set the FLL VCO frequency in free-running mode.
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0x00bc**
6	FLL3	GAIN_ERR																	FLL gain error **;** the threshold is comparison between DCO and target frequency.1111 has the most accurate DCO to target frequency. However, the gain error setting conditionally and inversely depends on FLL input reference clock rate. Higher FLL reference input frequency can only set lower gain error, such as 0000 for input reference from MCLK=12.288MHz. On the other side, if FLL reference input is from Frame sync, 48KHz, higher error gain can apply such as 1111. 0000 = (Rec) 0001 = x1 0010 = x2 0011 = x3 0100 = x4 0101 = x5 0110 = x6 0111 = x8 1000 = x9 1001 = x10 1010 = x12 1011 = x16 1100 = x17 1101 = x18 1110 = x20 1111 = x24
		FLL_CLK_REF_SRC																	FLL Reference CLK Source Select 00 & 01 = MCLK Pin 10 = BCLK_PIN
		FLL_INTEGER																	10-bit integer DCO output frequency divider for FLL filter clock: the value is in orders of 2. When 0x8[13]=1, it selects DCO clock as FLL filter clock. The filter clock rate needs to be less than 1Mhz. With setting proper value, filter clock can be divided down from DCO clock. For example, DCO runs at 96Mhz, by setting value 0x60=96, filter clock becomes 1Mhz

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0x0008
7	FLL4	HIGHBWE																	High Bandwidth enable (0-disable, 1-enable)
		FLL_CLK_REF_DIV_4CHK																	FLL CLK_REF divider for accurate lock detection 000 = 1 (Rec) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32
		FLL_CLK_REF_DIV																	FLL pre-scalar 00 = 1 01 = 1/2 10 = 1/4 11 = 1/8
		FLL_N2																	FLL 10-bit integer VCO divider for FLL Filter Clock
		Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	**0x0010**
8	FLL5	PDB_DACICTRL																	FLL Loop Filter enable to reduce FLL output noise, especially, (DCO frequency)/(FLL input reference frequency) is not a integer 1 = Enable 0 = Disable
		CHB_FILTER_EN																	**Select filter clock source selection** 1 = Select divided VCO clock based on register FLL_N2 0 = Select REFCLK
		CLK_FILTER_SW																	IDAC input selection 1 = Select accumulator output when feedback divider is integer, it can use for saving power but more jitter 0 = Select filter output
		FILTER_SW																	Set FLL Lock-In Length Set the time that FLL must stay within the lock-in range before lock signal goes high
		FLL_LOCK_LENGTH																	FLL Loop Filter enable to reduce FLL output noise, especially, (DCO frequency)/(FLL input reference frequency) is not a integer 1 = Enable 0 = Disable
		Default	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x4000**
9	FLL6	DCO_EN																	FLL free-running mode enable: Need to enable **BIASEN** for FLL Free Running Mode 1 = Enable 0 = Disable
		SDM_EN																	FLL sigma delta modulator enable to create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not a integer . If the ratio is integer, it still can be on for lower noise output but higher power consumption 1 = Enable 0 = Disable
		CUTOFF500																	FLL 500Khz cutoff frequency enable If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give the best FLL performance with highest power consumption 1 = Enable 0 = Disable
		CUTOFF600																	FLL 600Khz cutoff frequency enable If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give a moderate FLL performance with moderate power consumption 1 = Enable 0 = Disable
		VREFSEL																	Vref select 00 = 1.8V, 01 = 1.56V, 10 = 1.65V, 11 = 1.75V
		CHKFS256_EN																	0 = Disable 1 = Enable the function to check for 256 samples/frame sync
		FS8X_SEL																	0 = Total samples per 4 frame sync 1 = Total samples per 8 frame sync
		FLL_FLTR_DITHER_SEL																	Randomize the number of Filter output 00: no dither 01: the LSB is a random bit 10: two LSBs are random bits 11: three LSBs are random bits

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		FLL_SD_DITHER_SEL																	Randomize the number of bits for the input of SD modulator 00: no dither 01: the LSB is a random bit 10: two LSBs are random bits 11: three LSBs are random bits
		DLR																	FLL dynamic lock range. 0000 = recommended
		Default	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x6900**
A	FLL7	FLL_FRAC_H																	MSB potion of FLL 24-bit fractional input FLL_FRAC[23:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0x0031**
B	FLL8	FLL_FRAC_L																	LSB potion of FLL 24-bit fractional input FLL_FRAC[15:0]
		Default	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**0x26e9**
D	JACK_DET_CTRL	MANU_SPKR_DWN1R																	Manual Access SPKR_DWN1R 0 = Pull Down
		MANU_SPKR_DWN1L																	Manual Access SPKR_DWN1L 0 = Pull Down
		JK_1_PL																	Jack Detection Source 1 Configuration 00 = from GPIO2JD1 01 = from Inverted GPIO2JD1 10 = ignore the input and set to 0 11 = ignore the input and set to 1
		JD_RESTART																	Manual Restart Jack Detect de-bounce Toggle this bit to 1 and then to 0 to restart the JACK DETECTION.
		DB_BP_MODE																	Jack Detect de-bounce bypass 1=Bypass the de-bounce circuit 0=Will enable de-bounce circuit (need to set REG4B[0] = 1 to enable the CLK)
		INSERT_DT																	Insertion de-bounce time 2^(INSERT_DT +2) ms
		EJECT_DT																	Ejection de-bounce time 2^(EJECT_DT +2) ms
		JKDET_PL																	Jack Insertion/ Detection Logic polarity 0 = Invert the JACK Detection logic before de-bounce circuit. 1 = Not inverted
		JKDET_LOGIC																	Jack Detection Logic control 1 = AND Gate 0 = OR Gate
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
F	INTERRUPT_MASK	IRQ_PL																	Default IRQ Logic 1 = Active High 0 = Active Low
		IRQ_PS																	IRQ Pin Pull select 0 = Pull Down 1 = Pull Up
		IRQ_PE																	IRQ Pin Pull enable 1 = Enable 0 = Disable
		IRQ_DS																	1 = High drive current 0 = Low drive current
		IRQ_OE																	IRQ Output Enable 1 = Enable 0 = Disable
		APR_EMRGENCY_SHTDWN1_INTP_MASK																	APR Emergency Shutdown Interrupt mask 1 = Mask the interrupt 0 = Unmask
		RMS_INTP_MASK																	RMS Interrupt mask 1 = Mask the interrupt 0 = Unmask
		KEY_RELEASE_INTP_MASK																	Key Release Interrupt mask 1 = Mask the interrupt 0 = Unmask

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		KEY_INTP_MASK																	Key Pressed Interrupt mask 1 = Mask the interrupt 0 = Unmask
		MCLKDET_INTP_MASK																	Missing MCLK Detection Interrupt mask 1 = Mask the interrupt 0 = Unmask
		MIC_DET_INTP_MASK																	MIC Detection Interrupt mask 1 = Mask the interrupt 0 = Unmask
		JK_EJECT_INTP_MASK																	Jack Ejection Interrupt mask 1 = Mask the interrupt 0 = Unmask
		JK_DET_INTP_MASK																	Jack Insertion Interrupt mask 1 = Mask the interrupt 0 = Unmask
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
10	IRQ_STATUS	APR_EMRG_SHTDWN																	APR Emergency Short Circuit Shutdown IRQ
		RMS_INT																	Impedance Measurement Interrupt IRQ Status
		KEY_RELEASE_INT																	Key Release for Key Detection IRQ Status
		KEY_INT																	key Detection IRQ Status
		MCLK_DET_INT																	Missing MCLK Detection IRQ Status
		MIC_DET_INT																	MIC Detection IRQ Status
		JACK_EJCT_IRQ																	Jack Ejection IRQ Status 00 = cleared state 01 = JACK ejection detected 10 = a jack detected was cleared due to a jack insertion before write REG 11[3:2] to clear it. 11 = undefined
		JACK_DET_IRQ																	Jack insertion IRQ status. 00=cleared state 01= Jack insertion detected 10= a jack insertion interrupt was cleared due to jack removal detection before write REG 11[1:0] to clear it. 11 = undefined
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read Only**
11	INT_CLR_KEY_STATUS	INT_CLR_KEY_STATUS																	Write Operation: Write bits[15:0] clear corresponding REG10 [15:0] Write 1s to bits that you want to reset to 0, except Bit0 or Bit1 = clear Jack insertion interrupt Bit2 or Bit3 = clear Jack ejection interrupt
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read/Write**
12	INTERRUPT_DIS_CTRL (Write Mode)	APR_EMRG_SHTDWN_INT_DIS																	APR Emergency Short Circuit Shutdown Interrupt Disable Control 1 = Disable 0 = Enable
		RMS_INT_DIS																	RMS Impedance Measurement Interrupt Disable control 1 = Disable 0 = Enable
		KEY_RELEASE_INT_DIS																	Key Release Interrupt Disable Control 1 = Disable 0 = Enable
		KEY_INT_DIS																	Key Interrupt Disable Control 1 = Disable

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			0 = Enable
		MCLKDET_INT_DIS																	Missing MCLK Detection Interrupt Disable Control 1 = Disable 0 = Enable
		MIC_DET_INT_DIS																	MIC Detection/Headset Configuration interrupt disable control 1 = Disable 0 = Enable
		JACK_EJCT_INT_DIS																	Jack Ejection Interrupt Disable Control 1 = Disable 0 = Enable
		JACK_DET_INT_DIS																	Jack Insertion/Detection Interrupt Disable Control 1 = Disable 0 = Enable
		Default	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0xffff**
13	DMIC_CTRL	DMIC_DS																	DMIC in Driving Select 1 = High drive current 0 = Low drive current
		DMIC_SLEW																	DMMIC Pin Slew Rate Selection
		CLK_DMIC_SRC																	DMIC Clock Speed Selection: 00 = ADC Clock 01 = ADC Clock / 2 10 = ADC Clock / 4 11 = ADC Clock / 8
		DMICEN																	Digital Microphone Mode Enable 1 = Enabled 0 = Disabled
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
1A	GPIO12_CTRL	GPIO2OUT																	Programmable output to GPIO2
		GPIO2_PS																	GPIO2JD1 Pull Select
		GPIO2_DS																	GPIO2JD1 Driving Select 1 = High drive current 0 = Low drive current
		GPIO2_PE																	GPIO2JD1 Pin Pull enable 0 = Enable 1 = Disable
		GPIO2_OE																	GPIO2JD1 Output Enable 1 = Enable 0 = Disable
		GPIO1POL																	GPIO1 polarity inversion control 1 = Inverted logic of the CSB/GPIO1 function output selected by GPIO1SEL 0 = non inverted
		GPIO1SEL																	CSB/GPIO1 function select (input default) 000 = output 0 001 = JACK Status from the AND/OR logic 010 = SCLK_I 011 = SD_I 100 = output divided FLL clock 101 = FLL locked condition (logic 1 = PLL locked) 110 = SD_O 111 = OSC_CLK
		GPIO1_PS																	GPIO1CSB pull select
		GPIO1_DS																	1 = High drive current 0 = Low drive current
		GPIO1_PE																	GPIO1CSB Pin Pull enable 1 = Enable 0 = Disable
		GPIO1_OE																	GPIO1CSB Output Enable 1 = Enable 0 = Disable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
1B	TDM_CTRL	TDM																	TDM Enable 1 = Enable 0 = Disable
		PCM_OFFSET_MODE_CTRL																	PCM Offset Control in TDM 1 = Enable 0 = Disable
		ADCPHS0																	ADC audio data left-right ordering 0 = left ADC data in left phase of LRP

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			1 = left ADC data in right phase of LRP (left-right reversed)
		DACPHS1																	DAC right channel audio data left-right ordering 0 = right DAC data in right phase of LRP 1 = right DAC data in left phase of LRP (left-right reversed)
		DACPHS0																	DAC left channel audio data left-right ordering 0 = left DAC data in left phase of LRP 1 = left DAC data in right phase of LRP (left-right reversed)
		DAC_LEFT_SEL																	DAC left channel source under TDM mode I2S : 000 : from Slot 0 001: from Slot 1 010 : from Slot 2 011: from Slot 3 100 : Reserved 101: Reserved 110 : Reserved 111 : Reserved PCM: 000: from slot 0 001: from slot 1 010: from slot 2 011: from slot 3 100: from slot 4 101: from slot 5 110: from slot 6 111: from slot 7
		DAC_RIGHT_SEL																	DAC right channel source under TDM mode I2S: 000 : from Slot 0 001: from Slot 1 010 : from Slot 2 011: from Slot 3 100 : Reserved 101: Reserved 110 : Reserved 111 : Reserved PCM: 000: from slot 0 001: from slot 1 010: from slot 2 011: from slot 3 100: from slot 4 101: from slot 5 110: from slot 6 111: from slot 7
		ADC_TX_SEL_L																	ADC left channel source under TDM mode 00: from Slot 0 01: from Slot 2 10: from slot 4 11: from slot 6
		ADC_TX_SEL_R																	ADC right channel source under TDM mode I2S: 00: from Slot 1 01: from Slot 3 10: from slot 5 11: from slot 7
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
1C	I2S_PCM_CTRL1	DACCM0																	DAC companding mode control 00 = Off (normal linear operation) 01 = Reserved 10 = U-law companding 11 = A-law companding
		ADCCM0																	ADC companding mode control 00 = Off (normal linear operation) 01 = Reserved 10 = U-law companding 11 = A-law companding
		ADDAP0																	DAC audio data input option to route directly from ADC data stream 0 = No pass through, normal operation 1 = ADC output data stream routed to DAC input data path
		CMB8_0																	8-bit word enable for companding mode of operation 0 = Normal operation (no companding) 1 = 8-bit operation for companding mode
		UA_OFFSET																	uLaw offset 0 = 1's complement 1 = 2's complement
		BCP0																	Bit clock phase inversion option for BCLK 0 = Normal phase 1 = Input logic sense inverted

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		LRP0																	PCMA and PCMB left/right word order control 0 = Right Justified/Left Justified/I2S/PCMA mode 1 = PCMB Mode Enable: MSB is valid on 1st rising edge of BCLK after rising edge of FS
		WLEN0																	Port Word length (24-bits default) of audio data stream 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length 11 = 32-bit word length
		AIFMT0																	Port Audio interface data format (default setting is I2S) 00 = Right justified 01 = Left justified 10 = Standard I2S format 11 = PCMA or PCMB audio data format option
		Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	**0x000a**
1D	I2S_PCM_CTRL2	I2S_TRI																	I2S tri state 0 = Normal mode 1 = Output high Z
		I2S_DRV																	I2S driving enable 0 = Normal mode 1 = Always out
		LRC_DIV																	LRC divide coefficient setting 00 = 1/256 01 = 1/128 10 = 1/64 11 = 1/32
		PCM_TS_EN0																	0 = Only PCM_A_MODE or PCM_B_MODE (STEREO Only) can be used when PCM Mode is selected 1 = Time slot function enable for PCM mode
		TRI0																	Without TDM mode 0 = Drive the full Clock of LSB 1 = Tri-State the 2nd half of LSB
		PCM8BIT0																	0 = Use **I2S_PCM_CTRL.WLEN** to select Word Length 1 = PCM Select 8-bit word length
		PCM_TS_SEL																	Reserved to 0
		ADCDAT0_PE																	ADCDAT IO Pull Enable 1 = Enable 0 = Disable
		ADCDAT0_PS																	ADCDAT IO Pull Up/Down Enable 1 = Pull Up 0 = Pull Down
		ADCDAT0_OE																	0 = ADCDAT is not always out (when no data out, ADCOUT pin becomes high) 1 = ADCDAT always out
		MS0																	Master/Slave Mode Enable 0 = Slave Mode 1 = Master Mode
		BCLKDIV																	BCLK DIVIDE Setting from MCLK frequency 000 = 1 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32
		Default	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	**0x8010**
1E	LEFT_TIME_SLOT	FS_ERR_CMP_SEL																	Triggers short frame sync signal if frame sync is less than 00 = 252 x MCLK 01 = 253 x MCLK 10 = 254 x MCLK 11 = 255 x MCLK
		DIS_FS_SHORT_DET																	Short Gram Sync detection logic Enable 0 = Enable 1 = Disable
		TSLOT_L0																	Left channel PCM time slot start value Or PCM TDM Offset Mode Slot start value
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
1F	RIGHT_TIME_SLOT	TSLOT_R0																	Right channel PCM time slot start value Or unused for PCM TDM Offset Mode
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
21	BIQ0_COF1	BIQ0_A1_L																	Program ADC BIQ_A1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
22	BIQ0_COF2	BIQ0_A1_H																	Program ADC BIQ_A1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
23	BIQ0_COF3	BIQ0_A2_L																	Program ADC BIQ_A2 parameter Bit[15:0]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
24	BIQ0_COF4	BIQ0_A2_H																	Program ADC BIQ_A2 parameter Bit[18:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
25	BIQ0_COF5	BIQ0_B0_L																	Program ADC BIQ_B0 parameter Bit[15:0]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
26	BIQ0_COF6	BIQ0_B0_H																	Program ADC BIQ_B0 parameter Bit[18:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
27	BIQ0_COF7	BIQ0_B1_L																	Program ADC BIQ_B1 parameter Bit[15:0]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
28	BIQ0_COF8	BIQ0_B1_H																	Program ADC BIQ_B1 parameter Bit[18:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
29	BIQ0_COF9	BIQ0_B2_L																	Program ADC BIQ_B2 parameter Bit[15:0]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
2A	BIQ0_COF10	BIQ0_EN																	BIQ ADC Path Enable 1 : Enable 0 : Disable
		BIQ0_B2_H																	Program ADC BIQ_B2 parameter Bit[18:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
2B	ADC_RATE	ADC_L_SRC																	In Non-DMIC Mode: 0 : Latch Left Channel Analog data input into the Left Channel Filter 1: Latch Right Channel Analog data input into the Left Channel Filter In DMIC Mode: 0 = Left Channel in Rising Edge 1 = Left Channel in Falling Edge
		ADC_R_SRC																	In Non-DMIC Mode: 0 : Latch Right Channel Analog data input into the Right Channel Filter 1: Latch Left Channel Analog data input into the Right Channel Filter In DMIC Mode: 0 = Right Channel in Falling Edge 1 = Right Channel in Rising Edge
		SMPL_RATE																	Generating 2.048MKHz based on the Sample Rates 000 = 48k SR(default) 001 = 32k SR 110 = 96k SR 111 = 192 SR
		GAINCMP																	Reserved, always set to zero
		ADC_RATE																	ADC SINC Down selection 00 = Down 32 01 = Down 64 10 = Down 128 11 = Down 256
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0x0002**
2C	DAC_CTRL1	CICCLP_OFF																	Recommended default 1
		CIC_GAIN_ADJ																	For fine tuning the DAC output
		DAC_RATE																	DAC oversample rate selection *000 = 64* 001 = 256 *010 = 128* 100 = 32
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0x0082**
2D	DAC_TRL2	Reserved																	Reserved to 0
		SDMOD_DITHER																	Number of bits of dithering on SD modulator. Each level increments dithering by 1 bit 0000 = No dithering 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 11 1100 = 12 1101 = 13 1110 = 14 1111 = 15
		Reserved																	Reserved to 0
		Reserved																	Reserved to 0
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
2F	DAC_DGAIN_CTRL	DAC1_TO_DAC0_ST																	DAC CH1 to DAC CH0 crosstalk suppression sidetone selection. Step size is 0.5db 0xff = +24dB 0xfe = +23.5dB ▼ 0xcf = 0dB ▼ 0x43 = -70dB 0x42 = Reserved ▼ 0x0f = Reserved 0x0e = Mute 0x00 = Mute
		DAC0_TO_DAC1_ST																	DAC CH0 to DAC CH1 crosstalk suppression sidetone selection. Step size is 0.5db 0xff = +24dB 0xfe = +23.5dB ▼ 0xcf = 0dB ▼ 0x43 = -70dB 0x42 = Reserved ▼ 0x0f = Reserved 0x0e = Mute 0x00 = Mute
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
30	ADC_DGAIN_CTRL	ADC_TO_DAC_ST0																	ADC to DAC CH0 Sidetone selection. Step size is 3db 0000 = mute 0001 = -42db ▼ 1110 = -3dB 1111 = 0dB
		ADC_TO_DAC_ST1																	ADC to DAC CH1 Sidetone Attenuation. Step size is 3db 0000 = mute 0001 = -42db ▼ 1110 = -3dB 1111 = 0dB
		DAC_ST_SEL0																	0 = Select ADC CH0 as the side tone source of the DAC CH0 1 = Select ADC CH1 as the side tone source of the DAC CH0
		DAC_ST_SEL1																	0 = Select ADC CH1 as the side tone source of the DAC CH1 1 = Select ADC CH0 as the side tone source of the DAC CH1
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
31	MUTE_CTRL	PGA_SMUTE_STEP																	Analog Attn Mute Step 00 = 128 sample 01 = 32 sample 10 = 16 sample 11 = 1 sample
		DAC_SLOW_UM																	DAC Slow Soft Unmute Enable 1 = Enable (512 MCLK per step soft unmute) 0 = Disable (16 MCLK per step soft unmute)
		DAC_ZC_UP_EN																	DAC Zero Crossing Enable 1 = Enable 0 = Disable

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		AMUTE_EN																	Auto mute enable Generate null output to analog circuitry when 1024 consecutive zeros are detected. De-assert as soon as first non-zero sample is detected.
		AMUTE_CTRL																	Auto mute control 1 = Either Ch0 or Ch1 must have 1024 consecutive zero samples 0 = Both DAC channels must have 0 values for 1024 samples before AMUTE turns on
		SMUTE_EN																	Soft mute enable 1 = Gradually lower DAC volume to zero 0 = Gradually increase DAC volume to volume register setting
		ADC_ZC_UP_EN																	ADC Zero Crossing Enable 1 = Enable 0 = Disable
		ADC_SMUTE_EN																	ADC Soft mute Enable 1 = Enable 0 = Disable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
32	HSVOL_CTRL	HSPGA_ATTN_EN																	Headphone diver manual attn Enable(Enable HSPGA_ATTN_EN and AMUTE_EN) 1 = Enable 0 = Disable
		HSPGA_ATTN_AUTO_MODE																	Headphone driver Auto attn Enable(Enable HSPGA_ATTN_AUTO_MODE, and AMUTE_EN) 1 = Enable 0 = Disable
		MUTE_HSPGA2																	HSPGA Right Channel Manual Mute 1 = Mute
		MUTE_HSPGA1																	HSPGA Left Channel Manual Mute 1 = Mute
		HSPGA1_VOL																	Left Channel Headphone driver Volume control; 00 = 0dB 01 = -3dB 10 = -6dB 11 = -9dB
		HSPGA2_VOL																	Right Channel Headphone driver Volume control; 00 = 0dB 01 = -3dB 10 = -6dB 11 = -9dB
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
34	DACR_CTRL	DGAINR_DAC																	DAC Right Volume control. Expressed as a gain or attenuation in 0.5db steps 0xff = +24dB 0xfe = +23.5dB ▼ 0xcf = 0dB ▼ 0x4b = -66dB 0x4a = Reserved ▼ 0x0f = Reserved 0x0e = Mute 0x00 = Mute
		DGAINL_DAC																	DAC Left Volume control. Expressed as a gain or attenuation in 0.5db steps 0xff = +24dB 0xfe = +23.5dB ▼ 0xcf = 0dB ▼ 0x4b = -66dB 0x4a = Reserved ▼ 0x0f = Reserved 0x0e = Mute 0x00 = Mute
		Default	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0xcfcf**
35	ADC_DGAIN_CTRL1	DGAINR_ADC																	ADC Right Volume control. Expressed as a gain or attenuation in 0.5db steps 0xff = +24dB 0xfe = +23.5dB ▼ 0xcf = 0dB

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			▼ 0x4b = -66dB 0x4a = Reserved ▼ 0x0f = Reserved 0x0e = Mute 0x00 = Mute
		DGAINL_ADC																	ADC Left Volume control. Expressed as a gain or attenuation in 0.5db steps 0xff = +24dB 0xfe = +23.5dB ▼ 0xcf = 0dB ▼ 0x4b = -66dB 0x4a = Reserved ▼ 0x0f = Reserved 0x0e = Mute 0x00 = Mute
		Default	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	**0xcfcf**
36	ADC_DRC_KNEE_IP12	DRC_ENA_ADC																	ADC channel DRC enable 1 = Enable 0 = Disable
		DRC_KNEE2_IP_ADC																	ADC DRC Knee point 2 setting, increments in -1dB steps 0x00 = 0dB 0x01 = -1dB ▼ 0x3E = -62dB 0x3F = -63dB
		DRC_SMTH_ENA_ADC																	1= ADC Smooth filter enable
		DRC_KNEE1_IP_ADC																	ADC DRC Knee point 1 setting, increments in -1dB steps 0x00 = 0dB 0x01 = 1dB ▼ 0x1E = -30dB 0x1F = -31dB
		Default	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	**0x1486**
37	ADC_DRC_KNEE_IP34	DRC_KNEE4_IP_ADC																	ADC DRC Knee point 4 setting, increments in -1dB steps 0x00 = -35dB 0x01 = -36dB ▼ 0x3E = -97dB 0x3F = -98dB
		DRC_KNEE3_IP_ADC																	ADC DRC Knee point 3 setting, increments in -1dB steps 0x00 = -18dB 0x01 = -19dB ▼ 0x3E = -80dB 0x3F = -81dB
		Default	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	**0x0F12**
38	ADC_DRC_SLOPES	DRC_NG_SLP_ADC																	ADC DRC Noise Gate Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = 8:1
		DRC_EXP_SLP_ADC																	ADC DRC Expansion Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = Reserved
		DRC_CMP2_SLP_ADC																	ADC DRC Compressor Slope (lower region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_CMP1_SLP_ADC																	ADC DRC Compressor Slope (higher region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DRC_LMT_SLP_ADC																	ADC DRC Limiter Slope 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1 (default)
		Default	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0x25FF**
39	ADC_DRC_ATKDCY	DRC_PK_COEF1_ADC																	ADC DRC Peak detection attack time Ts = 1/**SMPL_RATEError! Reference source not found.** 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1xxx reserved
		DRC_PK_COEF2_ADC																	ADC DRC Peak detection release time Ts = 1/**Error! Reference source not found.** 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1xxx reserved
		DRC_ATK_ADC																	ADC DRC Attack time Ts = 1/**Error! Reference source not found.** 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_ADC																	ADC DRC Decay time Ts = 1/**Error! Reference source not found.** 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 =4095*Ts 0111 = 8191*Ts 1000 = 16383*Ts 1001 = 32757*Ts 1010 = 65535*Ts
		Default	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**0x3457**
3A	DAC_DRC_KNEE_IP12	DRC_ENA_DAC																	DAC channel DRC enable 1 = Enable. 0 = Disable
		DRC_KNEE2_IP_DAC																	DRC DAC Knee point 2 setting, increments in -1dB/step 0x00 = 0dB 0x01 = -1dB ▼ 0x3E = -62dB 0x3F = -63dB
		DRC_SMTH_ENA_DAC																	DRC DAC Smooth filter enable 1 = Enable. 0 = Disable
		DRC_KNEE1_IP_DAC																	DRC DAC Knee point 1 setting, increments in -1dB steps 0x00 = 0dB 0x01 = -1dB ▼ 0x1E = -30dB 0x1F = -31dB
		Default	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0x1486**
3B	DAC_DRC_KNEE_IP34	DRC_KNEE4_IP_DAC																	DRC DAC Knee point 4 setting, increments in -1dB steps 0x00 = -35dB 0x01 = -36dB ▼ 0x3E = -97dB 0x3F = -98dB
		DRC_KNEE3_IP_DAC																	DRC DAC Knee point 3 setting, increments in -1dB steps 0x00 = -18dB 0x01 = -19dB ▼ 0x3E = -80dB 0x3F = - 1dB

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		Default	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0x0F12
3C	DAC_DRC _SLOPES	DRC_NG_SLP _DAC																	DAC Noise Gate Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = 8:1
		DRC_EXP_SL P_DAC																	DAC DRC Expansion Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = 8:1
		DRC_CMP2_S LP_DAC																	DAC Compressor Slope (lower region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_CMP1_S LP_DAC																	DAC Compressor Slope (higher region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_LMT_SL P_DAC																	DAC Limiter Slope 000 = 0 001 = 1:2 (default) 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1
		Default	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0x25F9**
3D	DAC_DRC _ATKDCY	DRC_PK_COE F1_DAC																	DAC Peak detection attack time Ts = 1/**Error! Reference source not found.** 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1xxx reserved
		DRC_PK_COE F2_DAC																	DAC Peak detection release time Ts = 1/**Error! Reference source not found.** 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1xxx reserved
		DRC_ATK_DA C																	DAC Attack time Ts = 1/**Error! Reference source not found.** 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_DA C																	DAC Decay time Ts = 1/**Error! Reference source not found.** 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1000 = 16383*Ts 1001 =32757*Ts 1010 = 65535*Ts
		Default	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**0x3457**
41	BIQ1_ COF1	BIQ1_A1_L																	Program DAC BIQ_A1 parameter Bit[15:0]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
42	BIQ1_ COF2	BIQ1_A1_H																	Program DAC BIQ_A1 parameter Bit[18:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
43	BIQ1_ COF3	BIQ1_A2_L																	Program DAC BIQ_A2 parameter Bit[15:0]

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
44	BIQ1_COF4	BIQ1_A2_H																	Program DAC BIQ_A2 parameter Bit[18:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
45	BIQ1_COF5	BIQ1_B0_L																	Program DAC BIQ_B0 parameter Bit[15:0]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
46	BIQ1_COF6	BIQ1_B0_H																	Program DAC BIQ_B0 parameter Bit[18:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
47	BIQ1_COF7	BIQ1_B1_L																	Program DAC BIQ_B1 parameter Bit[15:0]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
48	BIQ1_COF8	BIQ1_B1_H																	Program DAC BIQ_B1 parameter Bit[18:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
49	BIQ1_COF9	BIQ1_B2_L																	Program DAC BIQ_B2 parameter Bit[15:0]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
4A	BIQ1_COF10	BIQ1_EN																	BIQ DAC Path Enable 1 : Enable 0 : Disable
		BIQ1_B2_H																	Program DAC BIQ_B2 parameter Bit[18:16]
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
4B	CLASSG_CTRL	CLASSG_CLK_SRC																	Class G function clock divider 00 = Clock 2Mhz 01 = 1/3 MCLK 10 = MCLK 11 = Disable CLK
		CLASSG_TIMER																	Define the number of milliseconds when a Class G mode signal to go low after it has been below the threshold 000001 = 1ms 000010 = 2ms 000100 = 8ms 001000 = 16ms 010000 = 32ms 100000 = 64ms
		CLASSG_THRSLD																	Threshold for DAC signal level comparison to generate the Class G mode signal 00 = 1/16 Full Scale 01 = 1/8 Full Scale 10 = 3/16 Full Scale 11 = 1/4 Full Scale
		CLASSG_CMP_EN																	Class G Compare path Enable bit. Each Bit enables according DAC path Bit 0 = Left DAC Bit 1 = Right DAC
		CLASSG_EN																	Class G function enable 1 = Enable 0 = Disable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
4C	IMM_MODE_CTRL	Reserved																	Reserved to zero
		IMM_THRESHOLD																	Impedance measurement threshold to avoid false detection. Each increase raises the floor of the ADC requiring higher signal levels before activation. 0x00 = [23:0] Full Range

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			0x01 = [23:1] ▼ 0x14 = [23:20] 0x15 = [23:21]
		IMM_GEN_VOL																	Signal level of the 23Hz sine wave generation for impedance measurement. 00 = 1/2 Full Scale 01 = 1/4 Full Scale 10 = 1/8 Full Scale 11 = 1/16 Full Scale
		IMM_CYCLE_CNT																	Number of MCLK used to calculate the impedance 00 = 1024 01 = 2048 10 = 4096 11 = 8192
		IMM_MODE																	Impedance measurement mode enable 1 = Enable. 0 = Disable
		DACIN_SRC																	DAC Filter Input Source Selection IMM_MODE Enabled, from Built-in Sin Generator 00: from DRC DAC Output 01: from DAC Mixer Output 10: from u/A-law decode output 11: 0
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
4D	IMM_RMS_L																		Left Headset speaker Impedance readout. It is recommended to characterize this before use with known Impedance values
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
4E	FUSE_CTRL2	FUSEIN_L																	The lower 16 bits of the FUSEIN. These register bits are OR ed with the Fuse latches and can be used for test characterization except during reset or after power on reset.
		Default	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
4F	FUSE_CTRL3																		Reseved to ‘0’
		FUSEIN_H																	The higher 2 bits of the FUSEIN. These register bits are OR ed with the Fuse latches and can be used for test characterization except during reset or after power on reset.
		Default	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
51	FUSE_CTRL1	FUSE_PRG_MODE																	Indicated that selected efuse is in the programming mode 1 = In the programming mode 0 = Not in the programming mode
		FUSWBNKIN																	Set the bank of 32 eFuse used for programming the eFuse 1 = bank 1 0 = bank 0
		FUSEPRGBNK																	Set this signal to 1 will instantly program the eFuse that selects the bank of 32 eFuses during a read operation
		FUSEPRGEN																	Set this signal to 1 will program the selected eFuse
		RUSEREAD																	Set this signal to 1 will read the bank of 32 eFuses selected by the fuse bank eFuse
		FUSERESETB																	Set this signalto 0 will reset the 32 eFuse latches. This signal should be 1 after any read cycle.
		FUSESEL																	The eFuse address bus for programming. Only one bit can be programmed at a time.
		Default	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0400**
53	OTPDOUT_1	OTPDOUT_L																	OTP read out data Low 16 bits
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
54	OTPDOUT_2	OTPDOUT_H																	OTP read out data High two bits
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
55	MISC_CTRL	SPI 3-WIRE ENA																	3-wire Mode Control 1 = Enable

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			0 = Disable
		RAM_TEST_START																	Ram Test Control 1 = Enable 0 = Disable
		D2A_LOOP																	1: Use DAC Left Filter Input as ADC decimation filter output
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
58	I2C_DEVICE_ID	I2C_DEVICE_ID[6:1]																	I2C Device ID read in
		KEYDET																	Key Detect Status Bit
		MICDET																	MICDETECT Status Bit
		Silicon Revision ID																	Silicon revision bits
		Software ID																	Software ID 00=NAU88L21
		Default	**X**	**0**	**0**	**1**	**1**	**0**	**1**	**X**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**Read Only**
59	SARDOUT_RAM_STATUS	RATM_TEST_FINISH																	1 = Test is finished 0 = Test is not complete
		RAM_TEST_FAIL																	1 = Test is failed 0 = Test is passed
		ANALOG_MUTE																	Analog mute enable 1 = Enable 0 = Disable
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
5A	SOFTWARE_RST	RESET_N_SOFT_PRE																	Software Reset Write anyvalue ***twice*** to reset all internal states without resetting the config registers.
66	BIAS_ADJ	TESTRL																	Enable Headphone Impedance Test/ IMM_MODE 1 = Enable 0 = Disable
		MUTEL																	Mute Left PGA 1 = Enable 0 = Disable
		MUTER																	Mute Right PGA 1 = Enable 0 = Disable
		TESTDAC																	DAC Right, Left Test only
		Reserved																	Reserved to 0
		VMIDEN																	VMID enable 1 = Enable 0 = Disable
		VMIDSEL																	VMID tie-off selection options 00 = Open (default) 01 = 25k Ohm 10 = 125k Ohm 11 = 2.5k Ohm
		Reserved																	
		Reserved																	
		BIASADJ																	PGA Master bias current power options 00 = normal operation (default) 01 = 9% reduced bias current from default 10 = 17% reduced bias current from default 11 = 11% increased bias current from default
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
68	TRIM_SETTINGS	DRV_IBCTRHS																	HS Output Driver Current trim 1 = Increase current 0 = Default
		DRV_ICUTHS																	HS Output Driver Current trim 1 = Increase current 0 = Default
		INTEG_IBCTRHS																	HS Pre Driver Current trim 1 = Decrease current 0 = Default
		INTEG_ICUTHS																	HS Pre Driver Current trim 1 = Increase current 0 = Default

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DIS_OC																	Disable Offset Trimming on Bit 2 = HS Out Left Bit 1 = HS Out Right 1 = Disable 0 = Enable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
69	ANALOG_CONTROL_1	TESTDACIN																	DAC Test signal;'00' & '11'=gnd;'01','10' high and low
		Pullup_GPIO2																	GPIO2JD1 Pull Up select; '0'=1MOhm, '1'=100kOhm
		GPIO2THL[1:0]																	GPIO2 JKDET1 Threshold Low select 00 = 0.22 x VDDA 10 = 0.40 x VDDA 11 = 0.5 x VDDA
		GPIO2THH[1:0]																	GPIO2 JKDET1 Threshold High select 00 = 0.85 x VDDA 10 = 0.78 x VDDA 11 = 0.6 x VDDA
		Reserved																	
		JD1POL																	JKDETL JD1 Polarity; '0'=default, '1'=inverted
		JKDETLPOL																	JKDETL Output Polarity; '0'=default, '1'=inverted
		ENJKDETL																	Enable Jack Tip insertion detection circuit
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
6A	ANALOG_CONTROL_2	ANALOG_CONTROL2																	Headphone driver Class AB bias current adjust in non-Class-G mode 0 = Default 1 = 2x
		ANALOG_CONTROL2																	Headphone driver bias current adjust in class-G mode 0 = Default 1 = 0.5x
		ANALOG_CONTROL2																	Headphone driver bias current adjust in non-Class-G mode 0 = Default 1 = 2.5x
		ANALOG_CONTROL2																	Headphone Out Boost Driver Bias current adjust2 in Class-G mode 0 = Default 1 = Low
		ANALOG_CONTROL2																	Headphone Out Boost Driver Bias current adjust1 in Class-G mode 0 = Default 1 = Low
		AB_ADJ																	Headphone Driver Class-AB adjust; '0'=default, '1' is increased bias
		Reserved																	
		Reserved																	
		Reserved																	
		Reserved																	
		Reserved																	
		CAP[1]																	DAC Reference Decoupling Capacitor enable msb
		CAP[0]																	DAC Reference Decoupling Capacitor enable lsb
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
6B		MUTENL																	MUTE MICLN Input to PGA when set to '1'
		MUTENR																	MUTE MICRN Input to PGA when set to '1'
		MUTEPL																	MUTE MICLP Input to PGA when set to '1'

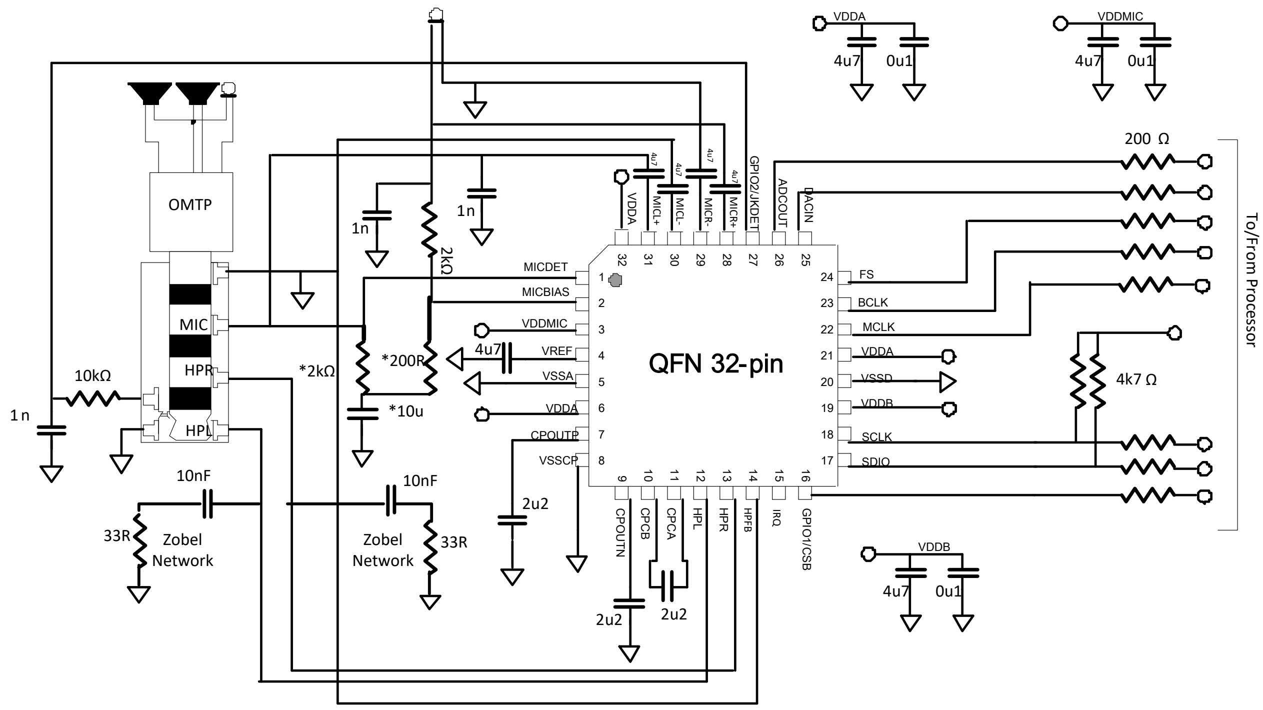
REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		MUTEPR																	MUTE MICRP Input to PGA when set to '1'
		TEST_ANALOG																	Reserved '0'
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
71	ANALOG_ADC_1	Reserved																	
		pdmicdet																	0 = power on mic detection 1 = power down mic detect
		Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	**0x0011**
72	ANALOG_ADC_2	Reserved																	
		Reserved																	
		ADC_UPL																	Left channel PGA bias current increase enable for driving the ADC at high sample rates 1 = Enable 0 = Disable
		ADC_UPR																	Right channel PGA bias current increase enable for driving the ADC at high sample rates 1 = Enable 0 = Disable
		BIAS																	Change bias currents in ADC 00 = Nominal 01 = Double 10 = Half 11 = Quarter
		VREFSEL																	VREF select in ADC 00 = Analog supply 01 = VMID 10 = VMID + 0.5dB 11 = VMID + 1dB
		Reserved																	Reserved '0'
		PDNOTL																	1 = Power on signal left ADC
		PDNOTR																	1 = Power on signal right ADC
		Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	**0x0020**
73	RDAC	DAC_EN																	DAC enable Bit 1 = Right DAC Bit 0 = Left DAC 1 = Enable 0 = Disable
		CLK_DAC_EN																	DAC CLOCK enable Bit 1 = Right DAC Bit 0 = Left DAC 1 = Enable 0 = Disable
		FC_CTR																	DAC Smoothing Filter on HS Output enable 1 = Enable 0 = Disable
		CLK_DAC_DELAY																	DAC clock delay setting
		DACVREFSEL																	DAC Reference voltage setting (default:1.6V)
		Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	**0x0008**
74	MIC_BIAS	INT2KA																	MICBIAS1 internal 2k Ohm resistor for MCGND2 enable 1 = Enable 0 = Disable
		LOWNOISE																	0 = Low power mode 1 = Low noise mode
		POWERUP																	0 = Power down MICBIAS1 1 = Power on MICBIAS1
		MICBIASLVL1																	Set output level for MICBIAS1 000 = VDDA 001 = 1x 010 = 1.1x 011 = 1.2x 100 = 1.3x 101 = 1.4x 110 = 1.53x 111 = 1.53x
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	**0x0006**

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
76	BOOST	CLR_APR_EMRGENCY_SHTDWN																	Clear Headset short circuit shut down IRQ 1 = Reset (momentary) 0 = Default
		STG2_SEL																	PGA in class A mode of operation enable instead of class AB (default) 1 = Enable 0 = Disable
		PDVMDFST																	VMID Pre-charge disable 1 = Disable 0 = Enable
		BIASEN																	Global Analog Bias enable 1 = Enable 0 = Disable
		DISCHRG																	Charges inputs selected by *Error! Reference source not found.* 1 = Enable 0 = Disable
		BYPS_IBCTR																	Bypass PGA current control enable 1 = Enable 0 = Disable
		BOOSTDIS																	Disable HP boost driver 1 = Disable 0 = Enable
		BOOSTGDIS																	Disable HP boost driver in Class-G mode 1 = Disable 0 = Enable
		SHRT_SHTDWN_DIG_EN																	Short Circuit Shut Down Digital Part Enable 1 = Enable 0 = Disable
		EN_SHRT_SHTDWN																	Enable Automatic Short-circuit Shutdown 1:headset driver power down immediately when short detected. No interrupt will be generated. 0&[8]=0: driver shut down after **16.3 usec** debounce when short detected. interrupt generated and 'apr_emrgncy_shtdwn' cleared if the interrupt cleared. 0&[8]=1: same as 0&[8]=0, plus apr_emrgncy_shtdwn cleared **1630 usec after** short removed, but interrupt remains to be cleared by the user
		HS_SHRT_THRESHLD[1:0]																	Headset Short Circuit protection limit 00= at 115mA at +FS(Default) 11= 155mA at +FS
		PAMP_THRSHLD																	Adjust HS boost p-driver bias current 11 = Decrease current 00 = Default
		NAMP_THRSHLD																	Adjust HS boost n-driver bias current 11 = Decrease current 00 = Default
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
77	FEPGA	ACDC_CTRL																	DC state control for Input pins. Action takes effect when DISCHRG=1 ACDC_CTRL[0] charges MICP to VREF ACDC_CTRL[1] charges MICN to VREF 1 = Enable 0 = Disable
		CMLCK_ADJ																	PGA Common mode Threshold lock adjust. It is recommended to leave this in default.
		IB_LOOP_CTR																	PGA: Current Trim. It is recommended to leave this in default.
		IBCTR_CODE																	PGA: Current Trim. It is recommended to leave this in default
		FEPGA_MODEL																	Left PGA mode selection; MODE[0] = Anti-aliasing filter adjust MODE[1] = Disconnects MICP & MICN MODE[2] = No function MODE[3] = Shorts the inputs and terminates with 12kOhm differentially 1 = Enable 0 = Disable

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		FEPGA_MODER																	Right PGA mode selection; MODE[0] = Anti-aliasing filter adjust MODE[1] = Disconnects MICP & MICN MODE[2] = No function MODE[3] = Shorts the inputs and terminates with 12kOhm differentially 1 = Enable 0 = Disable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
7E	PGA_GAIN	PGA_GAIN_L																	Left PGA gain, increments in 1dB steps 000000 = -1dB 000001 = 0dB ▼ 100100 = 35dB 100101 = 36dB
		PGA_GAIN_R																	Right PGA gain, increments in 1dB steps 000000 = -1dB 000001 = 0dB ▼ 100100 = 35dB 100101 = 36dB
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
7F	POWER_UP_CONTROL	PUPGA																	Power Up Left PGA 1 = Enable 0 = Disable
		PUPR																	Power Up Right PGA 1 = Enable 0 = Disable
		PUP_INTEG																	Power Up Output driver 1 = Power up 0 = Power down Bit 0 = Left HP driver Bit 1 = Right HP driver
		PUP_DRV_INSTG																	Power Up Output driver 1 = Power up 0 = Power down Bit 0 = Left HP driver Bit 1 = Right HP driver
		PUP_MAIN_DRV																	Power Up main driver 1 = Power up 0 = Power down Bit 0 = Left HP driver Bit 1 = Right HP driver
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
80	CHARGE_PUMP_AND_POWER_DOWN_CONTROL	Reserved																	Reserved
		BCLK_DS																	BCLK IO Drive Strength 1 = Stronger 0 = Default
		FS_DS																	FS IO Drive Strength 1 = Stronger 0 = Default
		ADCDAT_DS																	ADCDAT IO Drive Strength 1 = Stronger 0 = Default
		SDA_DS																	SDA IO Drive Strength 1 = Stronger 0 = Default
		JAMNODCLOW																	Reserved
		PDB_DAC																	DAC Right, Left Power Down Bar enable 11 = Enable 00 = Disable
		JAMFORCE2																	Register output forces the charge pump clock to not slow 1 = Enable 0 = Disable
		JAMFORCE1																	Register output forces the charge pump clock to not slow down 1 = Enable 0 = Disable

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		RNIN											■						Charge Pump enable 1 = Enable 0 = Disable
		PRECHARGE												■					VPOS Pre-charge enable for faster startup 1 = Enable 0 = Disable
		DISCHARGEVEE													■				VEE pad discharge enable 1 = Enable 0 = Disable
		DISCHARGEVPOS														■			VPOS pad discharge enable 1 = Enable 0 = Disable
		SHCIRSEL2															■		Charge up current limit 0 = Default low 1 = High
		SHCIRSEL1																■	Charge up current limit 0 = Default low 1 = High
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
81	CHARGE_PUMP_INPUT_READ	APR_EMRGNCY_SHTDWN1	■																APR emergency short circuit shutdown IRQ
		MODE1BUF											■						Monitors the MODE1 state of Charge Pump block
		NODCBUF												■					Monitors if the charge pump is drawing DC current 0 = Power drawn 1 = No power drawn
		RN2BUF													■				Monitors charge pump enable status 0 = OFF 1 = ON
		VPOSOK														■			Monitors the high voltage status of VPOS 1 = Max output (OK) 0 = Possible short circuit
		VCOMPBUF															■		Monitors the low voltage and low current status of the charge pump 0 = No current
		FORCE1BUF																■	Monitors charge pump frequency status 1 = Max frequency
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
82	GENERAL_STATUS	JK_EJECT_INTR									■								JACK Ejection Interrupt
		JK_INSERT_INTR										■							JACK Insertion Interrupt
		JKDET_ON											■						Pre-debounce JACK status
		JKDETL												■					JKDETL
		FUSEBNKOUT														■			Fuse Bank Select Output
		GPIO2_IN															■		GPIO2 Input
		GPIO1_IN																■	GPIO1 Input
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**

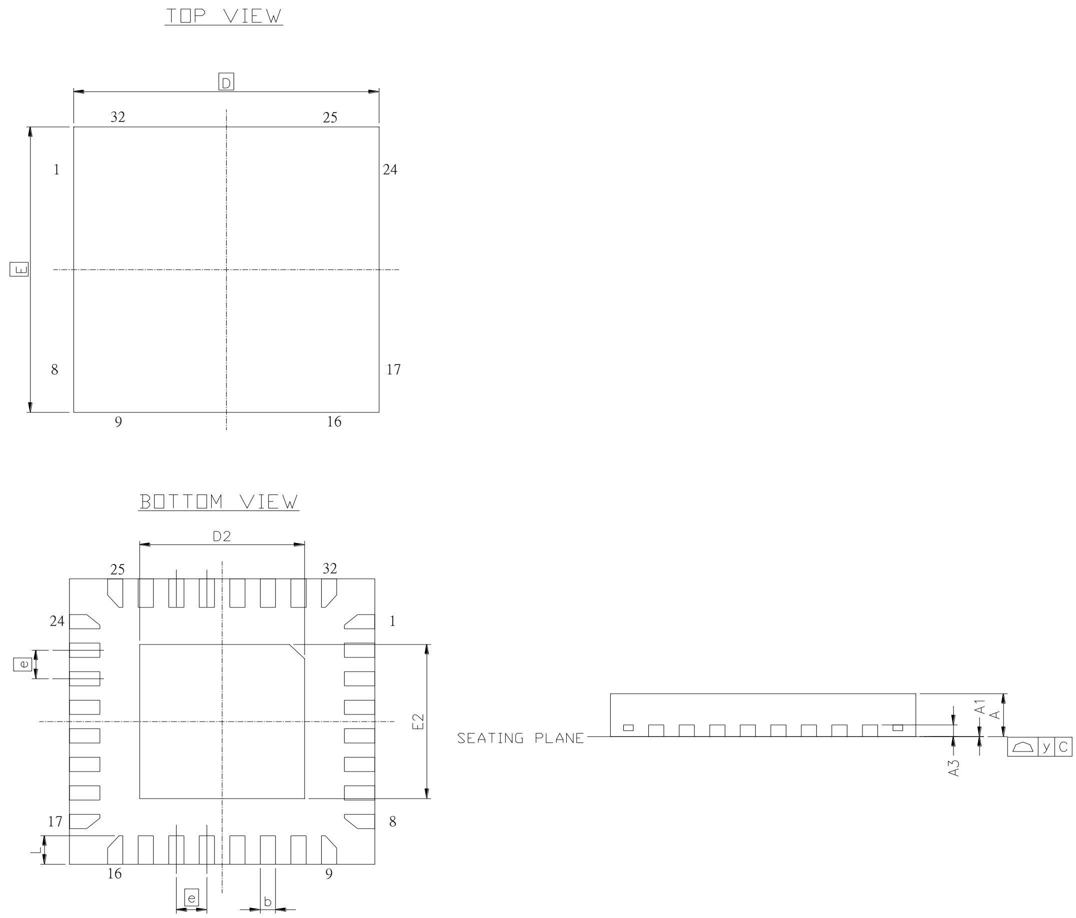
11. Typical Application Diagram



Note: * indicates optional components for improved noise reduction (refer to section 3.5)

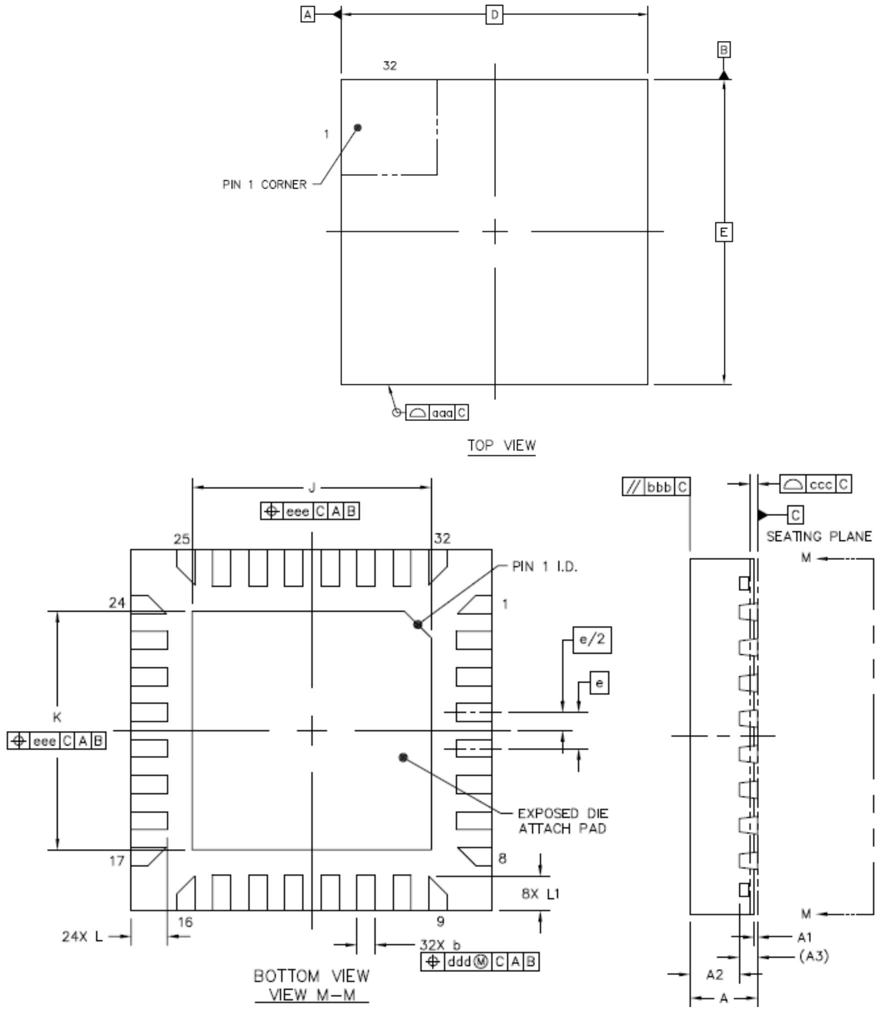
12. Package Information

32-lead plastic QFN 32L; 5X5mm2, 0.8mm thickness, 0.5mm lead pitch
(Saw Type) EP SIZE 3.5X3.5 mm



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
D2	2.60	2.70	2.80	0.1024	0.1063	0.1102
E	5.00 BSC			0.197 BSC		
E2	2.60	2.70	2.80	0.1024	0.1063	0.1102
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

32-lead plastic QFN 32L; 4X4mm2, 0.8mm(Max) thickness, 0.4mm lead pitch
(Saw Type) EP SIZE 3.5X3.5 mm



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.55	2.65	2.75
	Y	K	2.55	2.65	2.75
LEAD LENGTH		L	0.35	0.4	0.45
		L1	0.332	0.382	0.432
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

13. Ordering Information

Part Number	Dimension	Package	Package Material
NAU88L21YG	5x5 mm	QFN-32	Green
NAU88L21IG	4x4 mm	QFN-32	Green

NAU88L21 _ _

Package Material:

G = Pb-free Package

Package Type:

Y = 32-Pin QFN Package

I = 32-Pin QFN Package

Revision History

Version			DESCRIPTION
#	Date	Page(s)	
1.0	February 18, 2019	All	initial version
1.1	March 8, 2019	Front page	Add Cap-free and internal Resistor in MICBIAS
1.2	June, 12, 2019	64	Add Zebol Network in Application circuit.
1.3	September, 22, 2019	15	Added RC for MICDET – noise coupling.
1.4	October, 17, 2019	34	Modified Figure 34:2-Wire Read Sequence.
1.5	November, 8, 2019	66, 67	Add QFN4x4mm2 IC package
1.6	January 17, 2020	30,31	Enhance FLL application note
1.7	Febuary 24, 2020	2,5,6,7,9,62,64 7 27 42 56	Changed VDDC to VDDA Updated headphone performance MIPS400/500 informatin added Register 0x6[11:10] Device ID Reg0x58[5:2]=0x1823
1.8	April 5, 2020	6,7,8,27,49,56, 42-43	Pin 21 VDDA pin description change VDDA ISD change Headset standby mode current consumption changed HeadPHone offset voltage change ADC SNR Fs change Vih change for VDDA Register 0x58 changed Register setting for DAC OSR cases Register 0x2C DAC OSR description Enrich FLL register description, Figure 14
1.9	June 4, 2020	41-62	Whole register map updated

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.