Arm Cortex®-M0

32-bit Microcontroller

NuMicro® Family
NUC2201 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The NuMicro® NUC2201 series 32-bit microcontrollers are embedded with the Arm® Cortex®-M0 core with a cost equivalent to traditional 8-bit MCU for industrial control and applications requiring rich communication interfaces.

The NuMicro® NUC2201 USB Line with USB 2.0 full-speed functions is embedded with the Cortex®-M0 core running up to 72 MHz and features 128K bytes flash, 16K bytes embedded SRAM and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, Window Watchdog Timer, RTC, PDMA with CRC calculation unit, UART, SPI, I^2C, PWM Timer, GPIO, LIN, USB 2.0 FS Device, 12-bit ADC, Low Voltage Reset Controller and Brown-out Detector.

1.1 Key Features Support Table

Product Line	UART	SPI	I^2C	Timer	PWM	ADC	USB	Package
NUC2201L	2	1	2	4	4	10	1	LQFP48
NUC2201S	3	2	2	4	6	12	1	LQFP64

Table 1.1-1 NuMicro® NUC2201 Series Connectivity Support Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro® NUC2201 Features – USB Line

- Arm® Cortex®-M0 core
  - Runs up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 128K bytes Flash for program code
  - 8 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Configurable Data Flash address and size for 128 KB system
  - Supports 2-wired ICP update through SWD/ICE interface
- SRAM Memory
  - 16K bytes embedded SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ±3 % at -40 ℃ ~ +105 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 48 MHz internal high speed RC oscillator (HIRC) for USB device operation (Frequency variation < 2% at -40oC ~ +105oC)
    - Dynamically calibrating the HIRC OSC to 48 MHz ±0.25% from -40℃ to 105℃ by external 32.768K crystal oscillator (LXT) or internal USB synchronous mode
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL, up to 72 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function

- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Supports 4 selectable Watchdog Timer reset delay period(1026, 130, 18 or 3 WDT_CLK)
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports battery power pin (V_{BAT})
  - Supports wake-up function
- PWM/Capture
  - Up to three built-in 16-bit PWM generators providing six PWM outputs or three complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Supports One-shot or Auto-reload mode
  - Up to six 16-bit digital capture timers (shared with PWM timers) providing six rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to three UART controllers
  - UART ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports CTS wake-up function (UART0 and UART1 support)
  - Supports PDMA mode
- SPI
  - Up to two sets of SPI controllers
  - The maximum SPI clock rate of Master can up to 36 MHz (chip working at 5V)
  - The maximum SPI clock rate of Slave can up to 18 MHz (chip working at 5V)
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
  - Supports Byte Suspend mode in 32-bit transmission
  - Supports PDMA mode
  - Supports three wire, no slave select signal, bi-direction interface
- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)

  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12 Mbps
  - On-chip USB Transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 8 programmable endpoints
  - Includes 512 Bytes internal SRAM as USB buffer
  - Provides remote wake-up capability
  - Supports Crystal-less function
- ADC
  - 12-bit SAR ADC with 1 MSPS(chip working at 5V)
  - Up to 12-ch single-end input or 5-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion started by software programming, external input or PWM Center-aligned trigger
  - Supports PDMA mode
- EBI (External bus interface)
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8-/16-bit data width
  - Supports byte write in 16-bit data width mode
- 96-bit unique ID (UID)
- 128-bit unique customer ID(UCID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40℃ ~ 105℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin / 48-pin

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® NUC2201xxxAE Selection Guide

4.1.1 NuMicro® NUC2201 Naming Rule

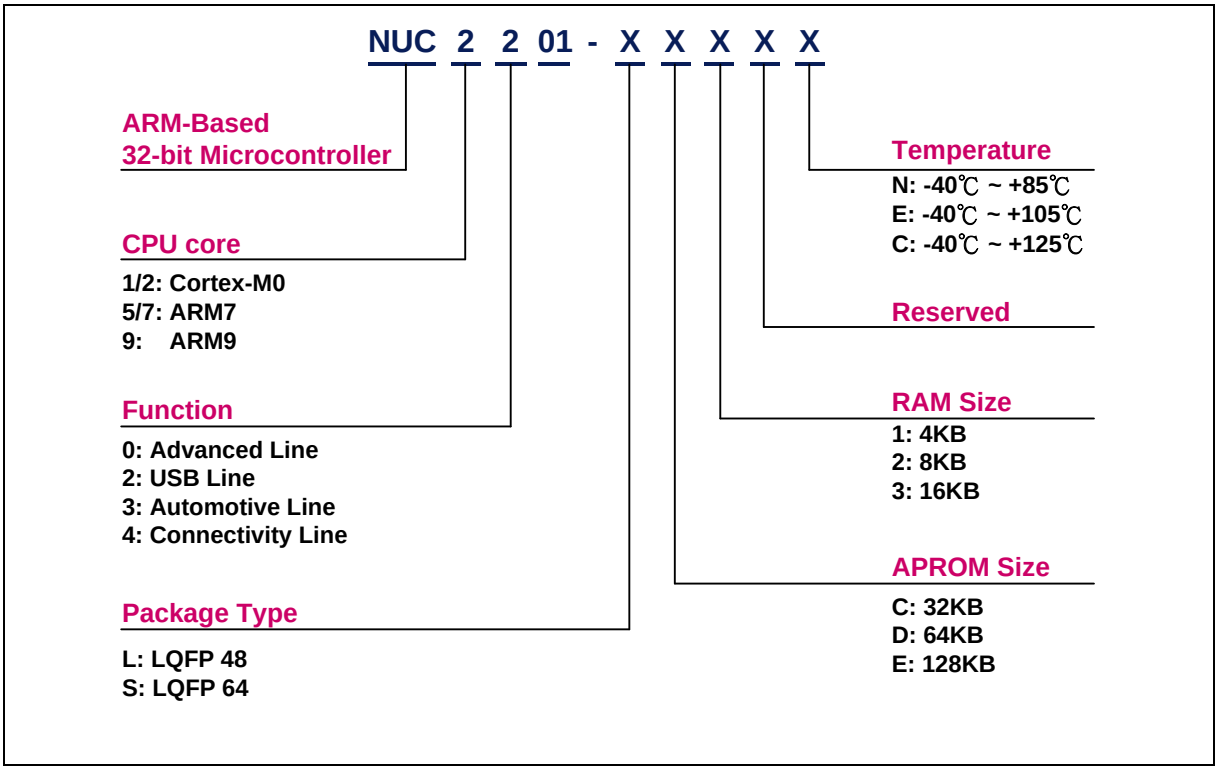


Figure 4-1 NuMicro® NUC2201 Series Selection Code

4.1.2 NuMicro® NUC2201 USB Line Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity						I²S	SC	Comp.	PWM	ADC (12-Bit)	RTC	EBI	ISP/ICP/IAP	Package
							UART	SPI	I²C	USB	LIN	CAN									
NUC2201LE3AE	128	16	Config.	8	31	4	2	1	2	1	2	-	-	-	-	6	10	v	-	v	LQFP48
NUC2201SE3AE	128	16	Config.	8	45	4	3	2	2	1	3	-	-	-	-	6	12	v	v	v	LQFP64

4.2 Pin Configuration

4.2.1 NuMicro® NUC2201 Pin Diagram

*4.2.1.1 NuMicro® NUC2201SxxAE LQFP 64 pin (7 mm * 7mm)*

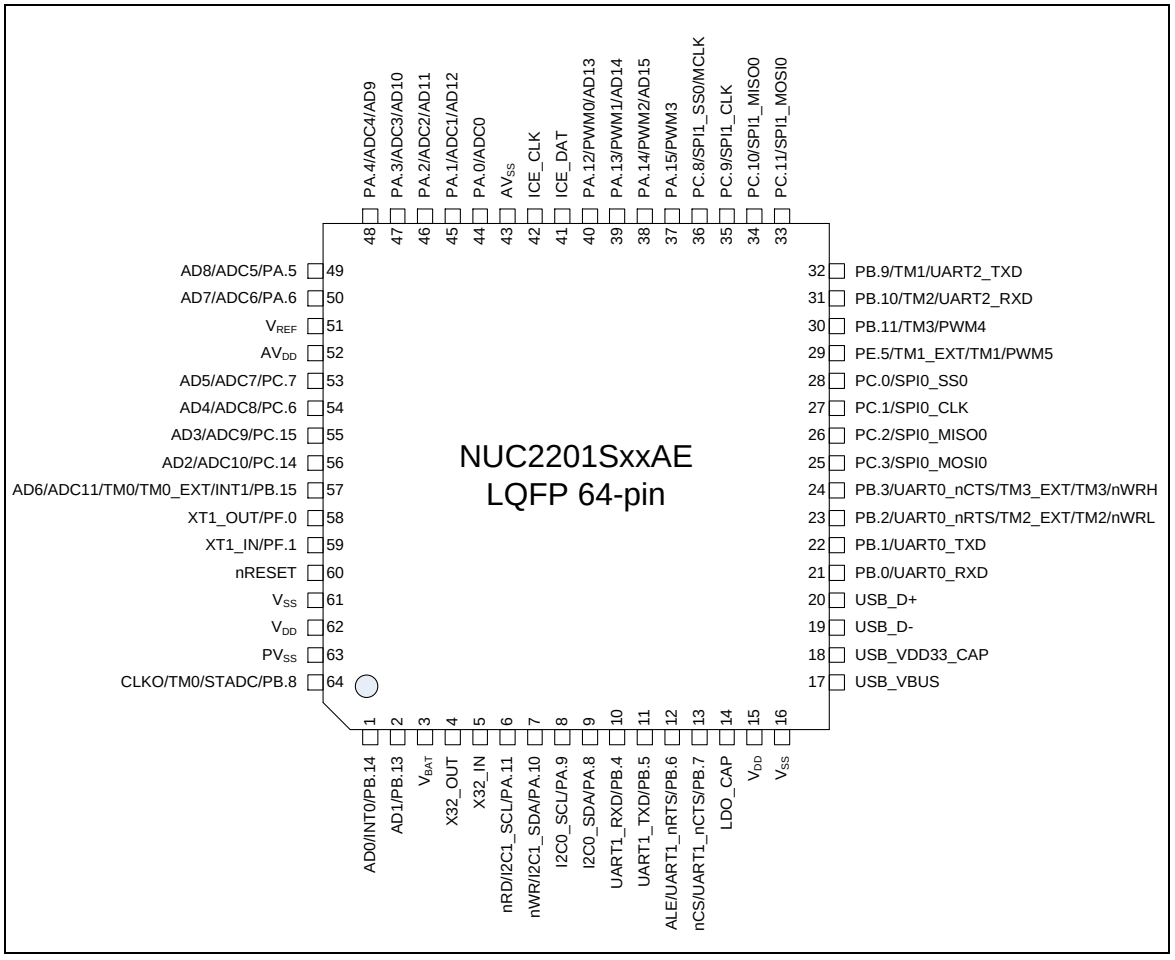


Figure 4-2 NuMicro® NUC2201SxxAE LQFP 64-pin Diagram

4.2.1.2 NuMicro® NUC2201LxxAE LQFP 48 pin (7 mm * 7mm)

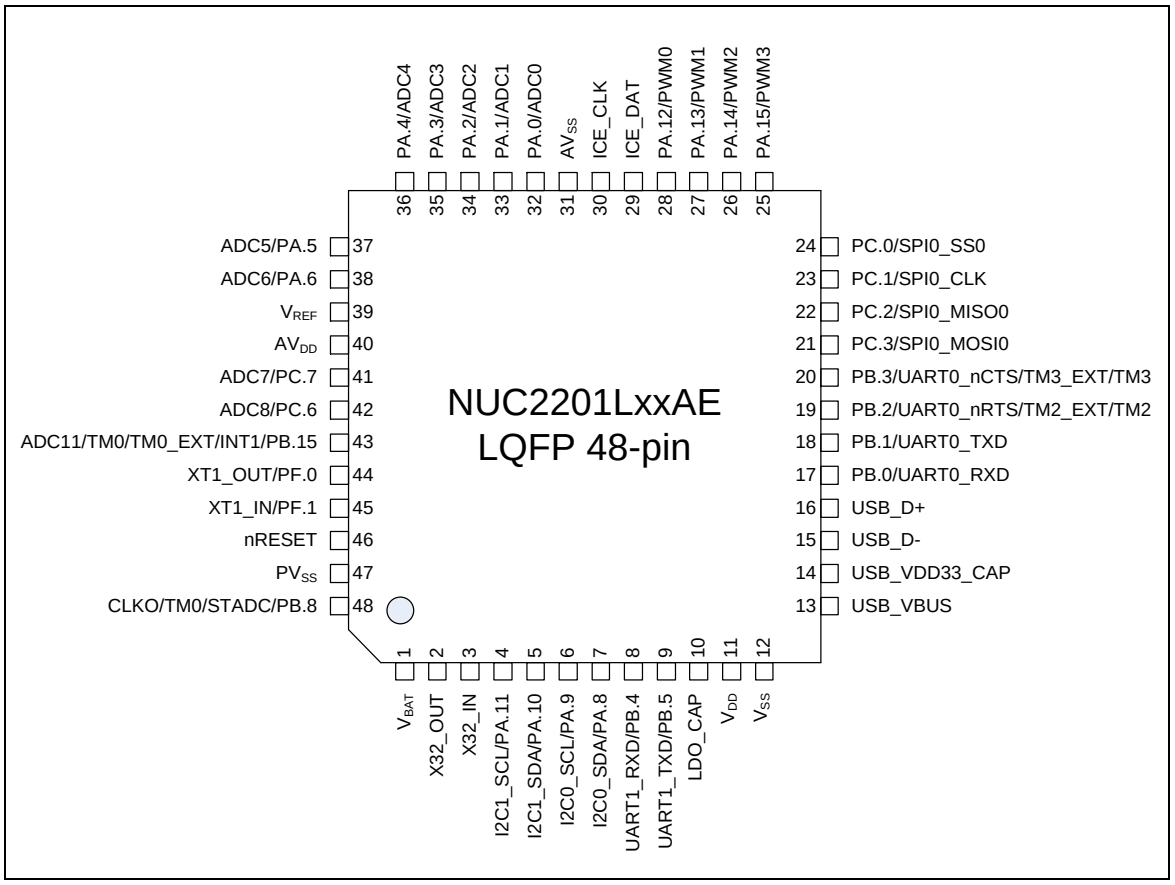


Figure 4-3 NuMicro® NUC2201LxxAE LQFP 48-pin Diagram

4.3 Pin Description

4.3.1 NuMicro® NUC2201 Pin Description

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
1		PB.14	I/O	General purpose digital I/O pin.
		INT0	I	External interrupt0 input pin.
		AD0	I/O	EBI Address/Data bus bit0
2		PB.13	I/O	General purpose digital I/O pin.
		AD1	I/O	EBI Address/Data bus bit1
3	1	V_{BAT}	P	Power supply by batteries for RTC.
4	2	X32_OUT	O	External 32.768 kHz (low speed) crystal output pin.
5	3	X32_IN	I	External 32.768 kHz (low speed) crystal input pin.
6	4	PA.11	I/O	General purpose digital I/O pin.
		I2C1_SCL	I/O	I^2C1 clock pin.
		nRD	O	EBI read enable output pin
7	5	PA.10	I/O	General purpose digital I/O pin.
		I2C1_SDA	I/O	I^2C1 data input/output pin.
		nWR	O	EBI write enable output pin
8	6	PA.9	I/O	General purpose digital I/O pin.
		I2C0_SCL	I/O	I^2C0 clock pin.
9	7	PA.8	I/O	General purpose digital I/O pin.
		I2C0_SDA	I/O	I^2C0 data input/output pin.
10	8	PB.4	I/O	General purpose digital I/O pin.
		UART1_RXD	I	Data receiver input pin for UART1.
11	9	PB.5	I/O	General purpose digital I/O pin.
		UART1_TXD	O	Data transmitter output pin for UART1.
12		PB.6	I/O	General purpose digital I/O pin.
		UART1_nRTS	O	Request to Send output pin for UART1.
		ALE	O	EBI address latch enable output pin
13		PB.7	I/O	General purpose digital I/O pin.
		UART1_nCTS	I	Clear to Send input pin for UART1.
		nCS	O	EBI chip select enable output pin
14	10	LDO_CAP	P	LDO output pin.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
15	11	V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
16	12	V_{SS}	**P**	Ground pin for digital circuit.
17	13	USB_VBUS	**USB**	Power supply from USB host or HUB.
18	14	USB_VDD33_CAP	**USB**	Internal power regulator output 3.3V decoupling pin.
19	15	USB_D-	**USB**	USB differential signal D-.
20	16	USB_D+	**USB**	USB differential signal D+.
21	17	PB.0	**I/O**	General purpose digital I/O pin.
		UART0_RXD	**I**	Data receiver input pin for UART0.
22	18	PB.1	**I/O**	General purpose digital I/O pin.
		UART0_TXD	**O**	Data transmitter output pin for UART0.
23	19	PB.2	**I/O**	General purpose digital I/O pin.
		UART0_nRTS	**O**	Request to Send output pin for UART0.
		TM2_EXT	**I**	Timer2 external capture input pin.
		TM2	**O**	Timer2 toggle output pin.
		nWRL	**O**	EBI low byte write enable output pin
24	20	PB.3	**I/O**	General purpose digital I/O pin.
		UART0_nCTS	**I**	Clear to Send input pin for UART0.
		TM3_EXT	**I**	Timer3 external capture input pin.
		TM3	**O**	Timer3 toggle output pin.
		nWRH	**O**	EBI high byte write enable output pin
25	21	PC.3	**I/O**	General purpose digital I/O pin.
		SPI0_MOSI0	**I/O**	1st SPI0 MOSI (Master Out, Slave In) pin.
26	22	PC.2	**I/O**	General purpose digital I/O pin.
		SPI0_MISO0	**I/O**	1st SPI0 MISO (Master In, Slave Out) pin.
27	23	PC.1	**I/O**	General purpose digital I/O pin.
		SPI0_CLK	**I/O**	SPI0 serial clock pin.
28	24	PC.0	**I/O**	General purpose digital I/O pin.
		SPI0_SS0	**I/O**	1st SPI0 slave select pin.
29		PE.5	**I/O**	General purpose digital I/O pin.
		PWM5	**I/O**	PWM5 output/Capture input.
		TM1_EXT	**I**	Timer1 external capture input pin.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		TM1	O	Timer1 toggle output pin.
30		PB.11	I/O	General purpose digital I/O pin.
		TM3	I/O	Timer3 event counter input / toggle output.
		PWM4	I/O	PWM4 output/Capture input.
31		PB.10	I/O	General purpose digital I/O pin.
		TM2	I/O	Timer2 event counter input / toggle output.
		UART2_RXD	I	Data receiver input pin for UART2.
32		PB.9	I/O	General purpose digital I/O pin.
		TM1	I/O	Timer1 event counter input / toggle output.
		UART2_TXD	O	Data transmitter output pin for UART2.
33		PC.11	I/O	General purpose digital I/O pin.
		SPI1_MOSI0	I/O	1st SPI1 MOSI (Master Out, Slave In) pin.
34		PC.10	I/O	General purpose digital I/O pin.
		SPI1_MISO0	I/O	1st SPI1 MISO (Master In, Slave Out) pin.
35		PC.9	I/O	General purpose digital I/O pin.
		SPI1_CLK	I/O	SPI1 serial clock pin.
36		PC.8	I/O	General purpose digital I/O pin.
		SPI1_SS0	I/O	1st SPI1 slave select pin.
		MCLK	O	EBI clock output
37	25	PA.15	I/O	General purpose digital I/O pin.
		PWM3	I/O	PWM3 output/Capture input.
38	26	PA.14	I/O	General purpose digital I/O pin.
		PWM2	I/O	PWM2 output/Capture input.
		AD15	I/O	EBI Address/Data bus bit15
39	27	PA.13	I/O	General purpose digital I/O pin.
		PWM1	I/O	PWM1 output/Capture input.
		AD14	I/O	EBI Address/Data bus bit14
40	28	PA.12	I/O	General purpose digital I/O pin.
		PWM0	I/O	PWM0 output/Capture input.
		AD13	I/O	EBI Address/Data bus bit13
41	29	ICE_DAT	I/O	Serial wire debugger data pin.
42	30	ICE_CLK	I	Serial wire debugger clock pin.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
43	31	AV_{SS}	**AP**	Ground pin for analog circuit.
44	32	PA.0	**I/O**	General purpose digital I/O pin.
		ADC0	**AI**	ADC0 analog input.
45	33	PA.1	**I/O**	General purpose digital I/O pin.
		ADC1	**AI**	ADC1 analog input.
		AD12	**I/O**	EBI Address/Data bus bit12
46	34	PA.2	**I/O**	General purpose digital I/O pin.
		ADC2	**AI**	ADC2 analog input.
		AD11	**I/O**	EBI Address/Data bus bit11
47	35	PA.3	**I/O**	General purpose digital I/O pin.
		ADC3	**AI**	ADC3 analog input.
		AD10	**I/O**	EBI Address/Data bus bit10
48	36	PA.4	**I/O**	General purpose digital I/O pin.
		ADC4	**AI**	ADC4 analog input.
		AD9	**I/O**	EBI Address/Data bus bit9
49	37	PA.5	**I/O**	General purpose digital I/O pin.
		ADC5	**AI**	ADC5 analog input.
		AD8	**I/O**	EBI Address/Data bus bit8
50	38	PA.6	**I/O**	General purpose digital I/O pin.
		ADC6	**AI**	ADC6 analog input.
		AD7	**I/O**	EBI Address/Data bus bit7
51	39	V_{REF}	**AP**	Voltage reference input for ADC.
52	40	AV_{DD}	**AP**	Power supply for internal analog circuit.
53	41	PC.7	**I/O**	General purpose digital I/O pin.
		ADC7	**AI**	ADC7 analog input.
		AD5	**I/O**	EBI Address/Data bus bit5
54	42	PC.6	**I/O**	General purpose digital I/O pin.
		ADC8	**AI**	ADC8 analog input.
		AD4	**I/O**	EBI Address/Data bus bit4
55		PC.15	**I/O**	General purpose digital I/O pin.
		ADC9	**AI**	ADC9 analog input.
		AD3	**I/O**	EBI Address/Data bus bit3

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
56		PC.14	I/O	General purpose digital I/O pin.
		ADC10	AI	ADC10 analog input.
		AD2	I/O	EBI Address/Data bus bit2
57	43	PB.15	I/O	General purpose digital I/O pin.
		INT1	I	External interrupt1 input pin.
		TM0_EXT	I	Timer 0 external capture input pin.
		TM0	I/O	Timer0 event counter input / toggle output.
		ADC11	AI	ADC11 analog input.
		AD6	I/O	EBI Address/Data bus bit6
58	44	PF.0	I/O	General purpose digital I/O pin.
		XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
59	45	PF.1	I/O	General purpose digital I/O pin.
		XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
60	46	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
61		V_{SS}	P	Ground pin for digital circuit.
62		V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
63	47	PV_{SS}	P	PLL ground.
64	48	PB.8	I/O	General purpose digital I/O pin.
		STADC	I	ADC external trigger input.
		TM0	I/O	Timer0 event counter input / toggle output.
		CLKO	O	Frequency divider clock output pin.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

5.1 NuMicro® NUC2201 Block Diagram

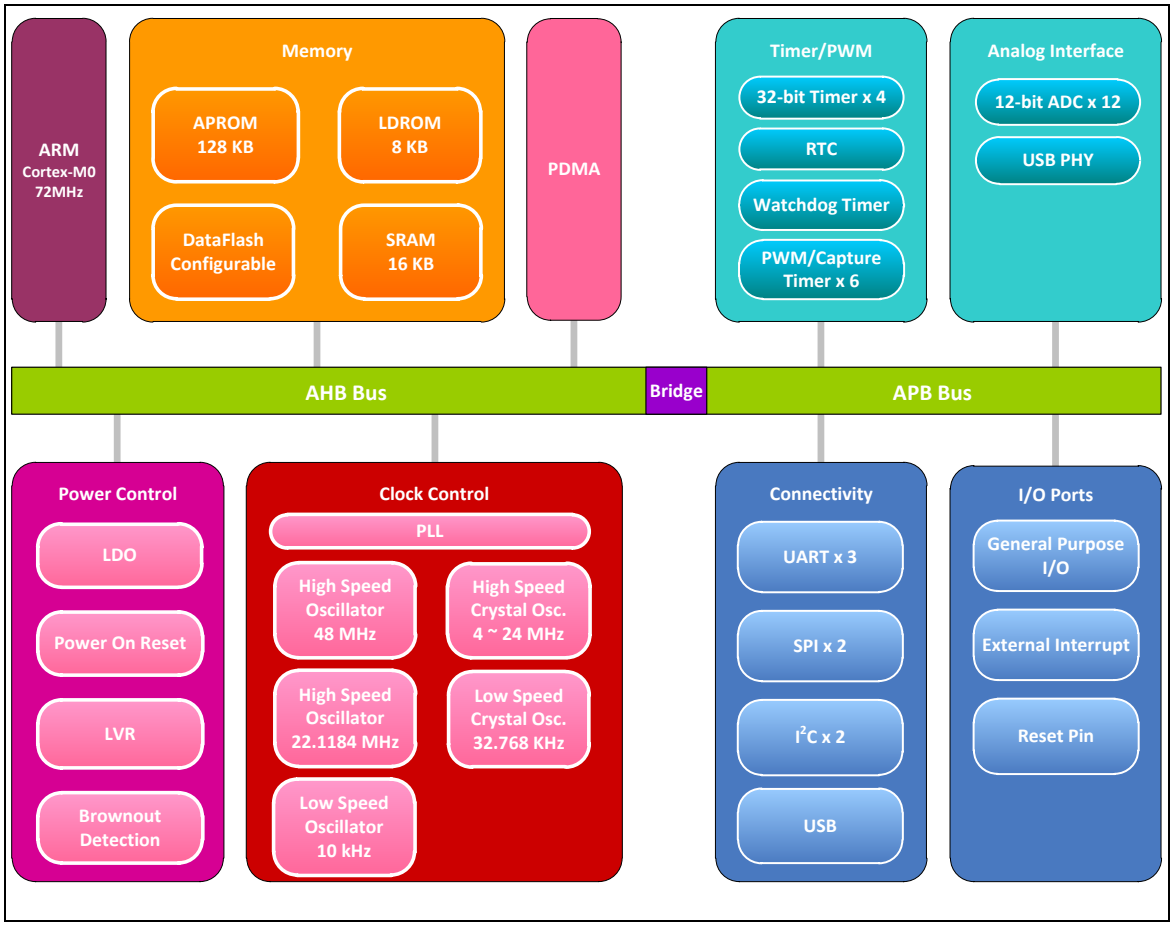


Figure 5-1 NuMicro® NUC2201 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6-1 shows the functional controller of processor.

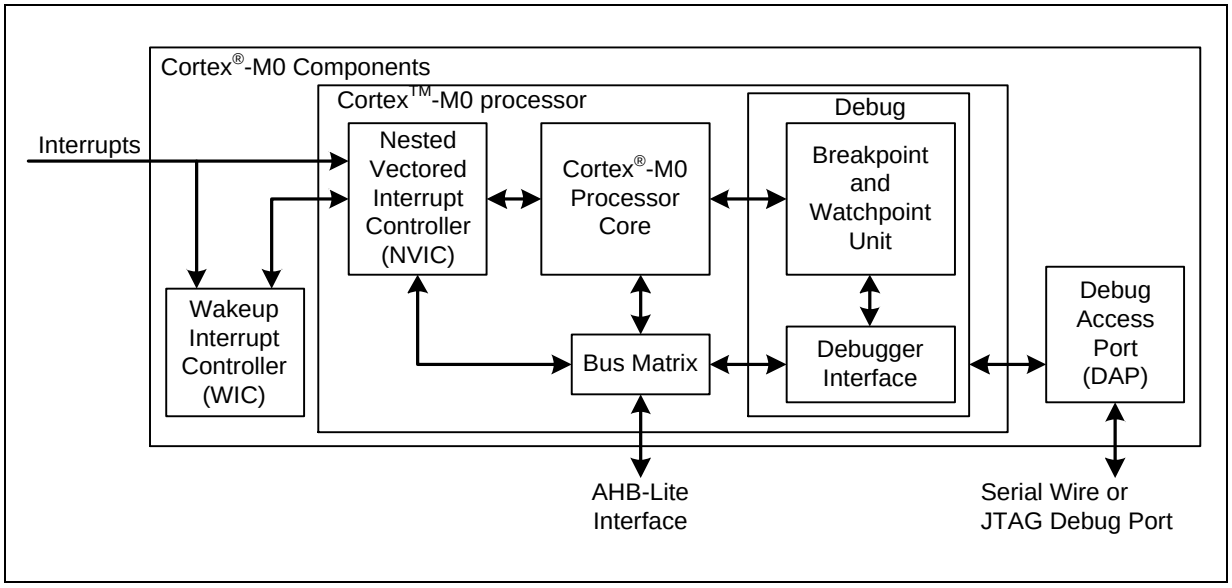


Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - Armv6-M Thumb® instruction set
  - Thumb-2 technology
  - Armv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the Armv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event

(WFE) instructions, or the return from interrupt sleep-on-exit feature

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Power-on Reset
- Low level on the nRESET pin
- Watchdog Time-out Reset
- Low Voltage Reset
- Brown-out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-on Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-on Reset is external crystal circuit and BS (ISPCON[1]) bit. System Reset does not reset external crystal circuit and BS (ISPCON[1]) bit, but Power-on Reset does.

6.2.3 System Power Distribution

In this chip, the power distribution is divided into four segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from V_{BUS} offers the power for operating the USB transceiver.
- Battery power from V_{BAT} supplies the RTC and external 32.768 kHz crystal.

The outputs of internal voltage regulators, LDO and V_{DD33}, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level with the digital power (V_{DD}). Figure 6-2 shows the NuMicro® NUC2201 power distribution.

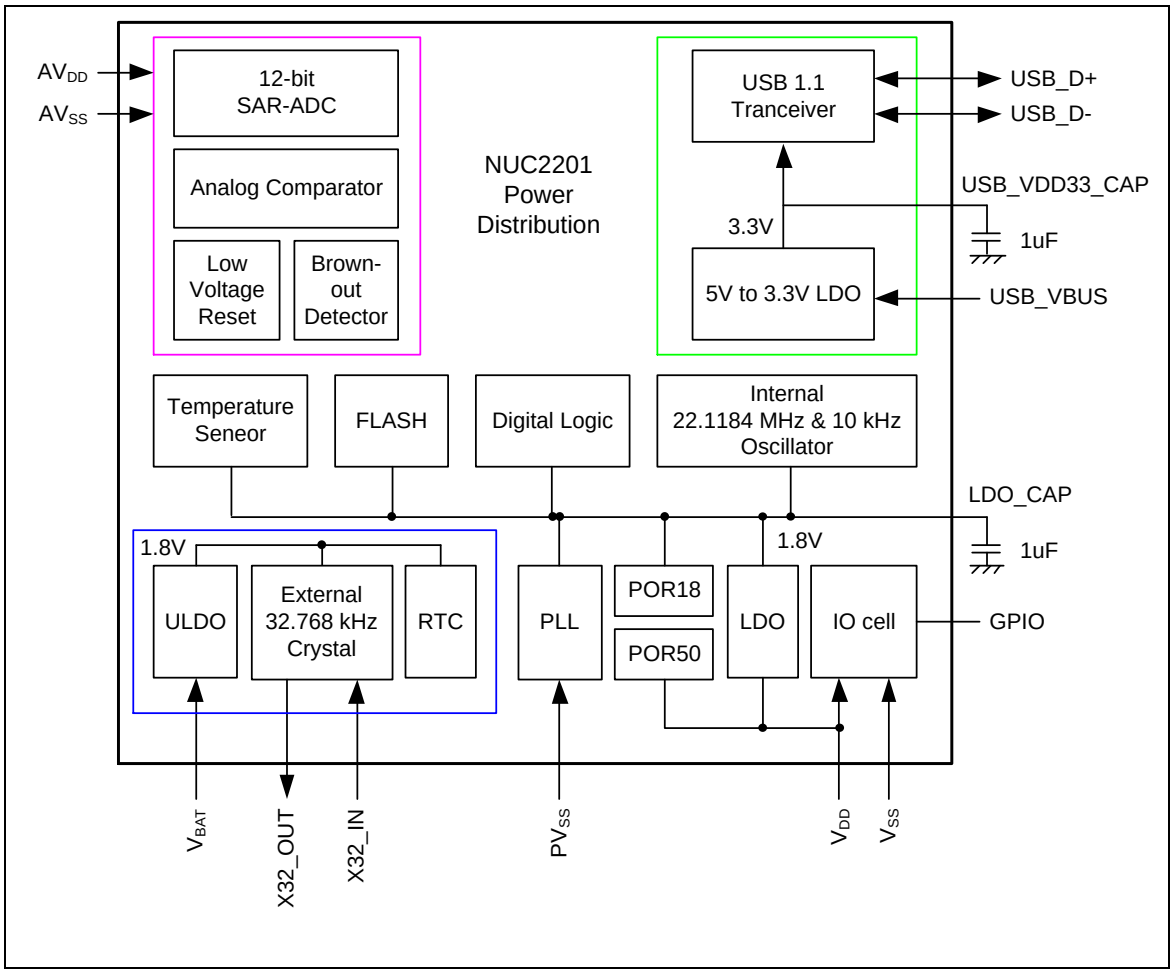


Figure 6-2 NuMicro® NUC2201 Power Distribution Diagram

6.2.4 System Memory Map

The NuMicro® NUC2201 provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripheral. The NuMicro® NUC2201 only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	External Bus Interface Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers

0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6-1 Address Space Assignments for On-Chip Controllers

6.2.5 Register Lock

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register REGWRPROT address at 0x5000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, user can check the protection disable bit at address 0x5000_0100 bit0, 1 is protection disable, and 0 is protection enable. Then user can update the target protected register value and then write any data to the address “0x5000_0100” to enable register protection.

The protected registers are listed as following table.

Register	Bit	Description
IPRSTC1	[3] EBI_RST	EBI Controller Reset (Write-protection Bit)
IPRSTC1	[2] PDMA_RST	PDMA Controller Reset (Write Protect)
IPRSTC1	[1] CPU_RST	CPU Kernel One-Shot Reset (Write Protect)
IPRSTC1	[0] CHIP_RST	CHIP One-Shot Reset (Write Protect)
BODCR	[7] LVR_EN	Low Voltage Reset Enable Bit (Write Protect)
BODCR	[5] BOD_LPM	Brown-Out Detector Low Power Mode (Write Protect)
BODCR	[3] BOD_RSTEN	Brown-Out Reset Enable Bit (Write Protect)
BODCR	[2:1] BOD_VL	Brown-Out Detector Threshold Voltage Selection (Write Protect)
BODCR	[0] BOD_EN	Brown-Out Detector Enable Bit (Write Protect)
PORCR	[15:0] POR_DIS_CODE	Power-On-Reset Enable Bit (Write Protect)
REGWRPROT	[7:0] REGWRPROT	Register Write-Protection Code (Write Only)
REGWRPROT	[0] REGPROTDIS	Register Write-Protection Disable Index (Read Only)
NMI_SEL	[8] NMI_EN	NMI Interrupt Enable Bit (Write Protect)
PWRCON	[8] PD_WAIT_CPU	Power-Down Entry Condition Control (Write Protect)
PWRCON	[7] PWR_DOWN_EN	System Power-Down Enable Bit (Write Protect)
PWRCON	[5] PD_WU_INT_EN	Power-Down Mode Wake-Up Interrupt Enable Bit (Write Protect)
PWRCON	[4] PD_WU_DLY	Wake-Up Delay Counter Enable Bit (Write Protect)
PWRCON	[3] OSC10K_EN	10 KHz Internal Low Speed RC Oscillator (LIRC) Enable Bit (Write Protect)
PWRCON	[2] OSC22M_EN	22.1184 MHz Internal High Speed RC Oscillator (HIRC) Enable Bit (Write Protect)
PWRCON	[1] XTL32K_EN	32.768 KHz External Low Speed Crystal Oscillator (LXT) Enable Bit

		(Write Protect)
PWRCON	[0] XTL12M_EN	4~24 MHz External High Speed Crystal Oscillator (HXT) Enable Bit (Write Protect)
APBCLK	[0] WDT_EN	Watchdog Timer Clock Enable Bit (Write Protect)
CLKSEL0	[5:3] STCLK_S	Cortex™-M0 SysTick Clock Source Select (Write Protect)
CLKSEL0	[2:0] HCLK_S	HCLK Clock Source Select (Write Protect)
CLKSEL1	[1:0] WDT_S	Watchdog Timer Clock Source Select (Write Protect)
ISPCON	[6] ISPFF	ISP Fail Flag (Write Protect)
ISPCON	[5] LDUEN	LDROM Update Enable Bit (Write Protect)
ISPCON	[4] CFGUEN	Enable Config Update By ISP (Write Protect)
ISPCON	[3] APUEN	APROM Update Enable Bit (Write Protect)
ISPCON	[1] BS	Boot Select (Write Protect)
ISPCON	[0] ISPEN	ISP Enable Bit (Write Protect)
ISPTRG	[0] ISPGO	ISP Start Trigger (Write-Protection Bit)
FATCON	[4] FOMSEL0	Chip Frequency Optimization Mode Select 0 (Write-Protection Bit)
ISPSTA	[6] ISPFF	ISP Fail Flag (Write-Protection Bit)
TCSR0	[31] DBGACK_TMR	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
TCSR1	[31] DBGACK_TMR	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
TCSR2	[31] DBGACK_TMR	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
TCSR3	[31] DBGACK_TMR	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
WTCR	[31] DBGACK_WDT	ICE Debug Mode Acknowledge Disable Bit (Write Protect)
WTCR	[10:8] WTIS	Watchdog Timer Time-Out Interval Selection (Write Protect)
WTCR	[7] WTE	Watchdog Timer Enable Bit (Write Protect)
WTCR	[6] WTIE	Watchdog Timer Time-Out Interrupt Enable Bit (Write Protect)
WTCR	[4] WTWKE	Watchdog Timer Time-Out Wake-Up Function Control (Write Protect)
WTCR	[1] WTRE	Watchdog Timer Reset Enable Bit (Write Protect)
WTCRALT	[1:0] WTRDSEL	Watchdog Timer Reset Delay Selection (Write Protect)

6.2.6 Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz and 22.1184 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 22.1184 MHz clock. In such case, if users do not want to use PLL as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQ_LOCK (SYS_IRCTSTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation. To get better results, it is recommended to set both TRIM_LOOP (SYS_IRCTCTL[5:4]) Trim Calculation Loop and

TRIM_RETRY_CNT (SYS_IRCTCTL[7:6] Trim Value Update Limitation Count) to “11”.

Another example is that the system needs an accurate 48 MHz clock for USB application. In such case, if neither using use PLL as the system clock source, user has to set FREQSEL (SYS_HIRCTCTL1[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Status bit FREQLOCK (SYS_HIRCTISTS[8] HIRC Frequency Lock Status) “1” indicates the HIRC48 output frequency is accurate within 0.25% deviation.

6.2.7 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “Arm® Cortex®-M0 Technical Reference Manual” and “Arm® v6-M Architecture Reference Manual”.

6.2.8 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “Arm® Cortex®-M0 Technical Reference Manual” and “Arm® v6-M Architecture Reference Manual”

6.2.8.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro® NUC2201. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6-2 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description
1 ~ 15	-	-	-	System exceptions
16	0	**BOD_INT**	Brown-out	Brown-out low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[6:0]/PA[15:8]/PB[11:0]/PB[15:13]
21	5	**GPCEF_INT**	GPIO	External interrupt from PC[3:0]/PC[11:6]/PC[15:14]/PE[5]/PF[1:0]
22	6	**PWMA_INT**	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	**PWMB_INT**	PWM4~7	PWM4 and PWM5 interrupt
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt
28	12	**UART02_INT**	UART0/2	UART0 and UART2 interrupt
29	13	**UART1_INT**	UART1	UART1 interrupt

30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**SPI1_INT**	SPI1	SPI1 interrupt
32	16	**-**	-	Reserved
33	17	**-**	-	Reserved
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**-**	-	Reserved
37	21	**-**	-	Reserved
38	22	**-**	-	Reserved
39	23	**USB_INT**	USBD	USB 2.0 FS Device interrupt
40	24	**-**	-	Reserved
41	25	**-**	-	Reserved
42	26	**PDMA_INT**	PDMA	PDMA interrupt
43	27	**-**	-	Reserved
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state
45	29	**ADC_INT**	ADC	ADC interrupt
46	30	**IRC_INT**	IRC	IRC TRIM interrupt
47	31	**RTC_INT**	RTC	Real Time Clock interrupt

Table 6-3 System Interrupt Map

6.2.8.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For Armv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-4 Vector Table Format

6.2.8.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

6.2.9 System Control

The Cortex®-M0 status and operating mode control are managed by System Control Registers. Including CPUID, Cortex™-M0 interrupt priority and Cortex®-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the "Arm® Cortex®-M0 Technical Reference Manual" and "Arm® v6-M Architecture Reference Manual".

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator and 22.1184/48 MHz internal high speed RC oscillator to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 6 clock sources as listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLL source can be selected from external 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC)) (PLL FOUT)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 48 MHz internal high speed RC oscillator (HIRC48)
- 10 kHz internal low speed RC oscillator (LIRC)

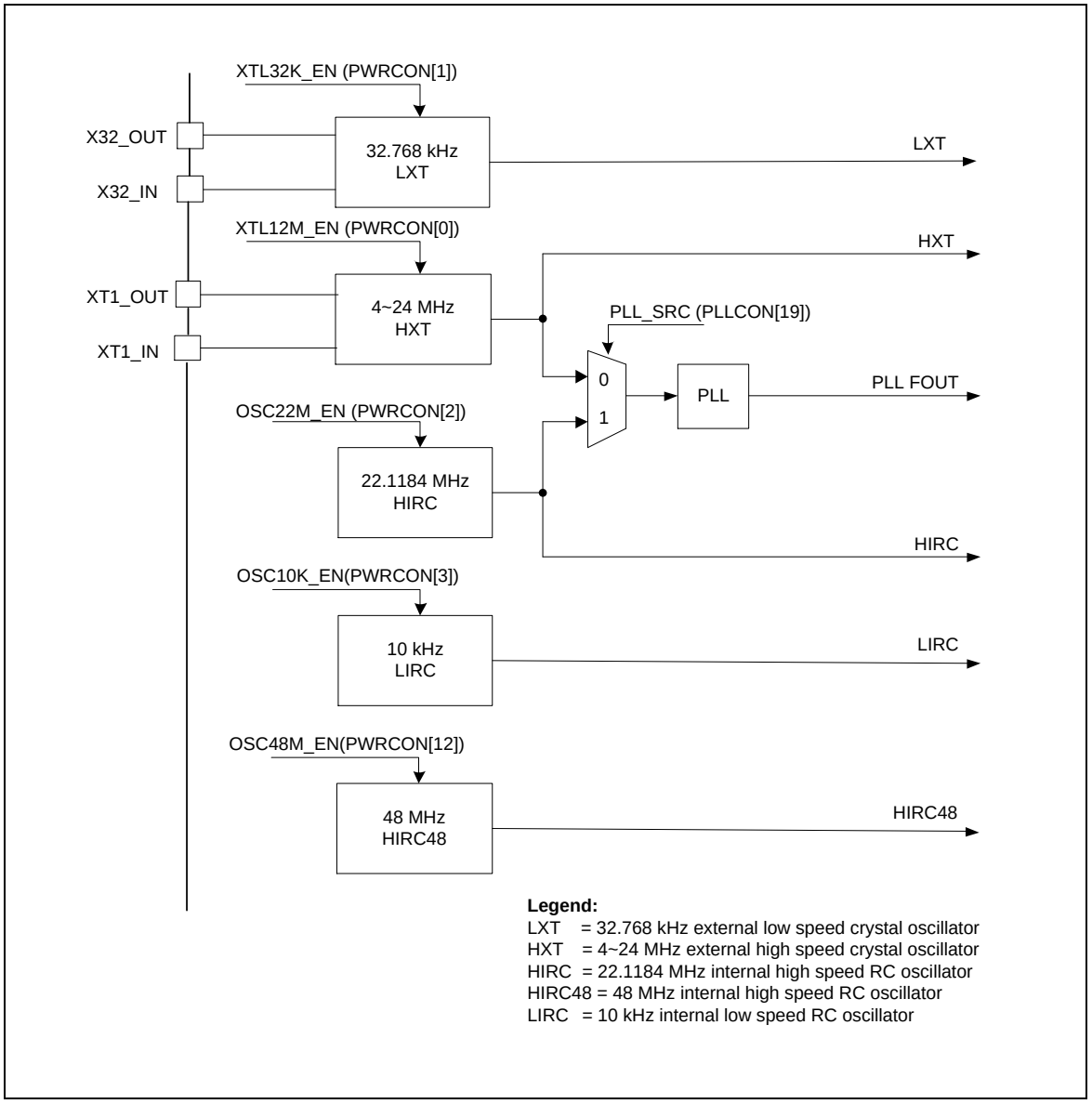


Figure 6-3 Clock Generator Block Diagram

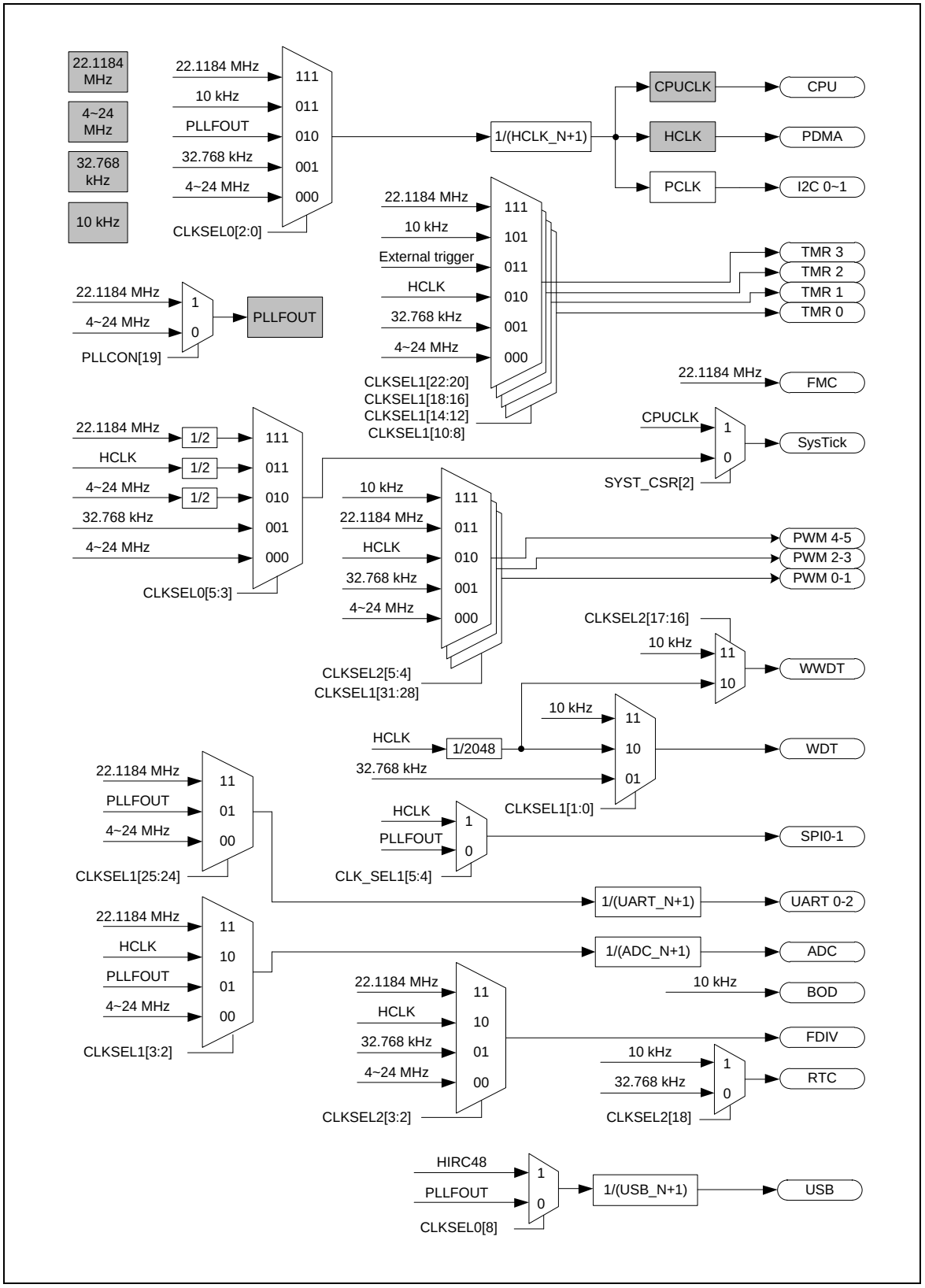
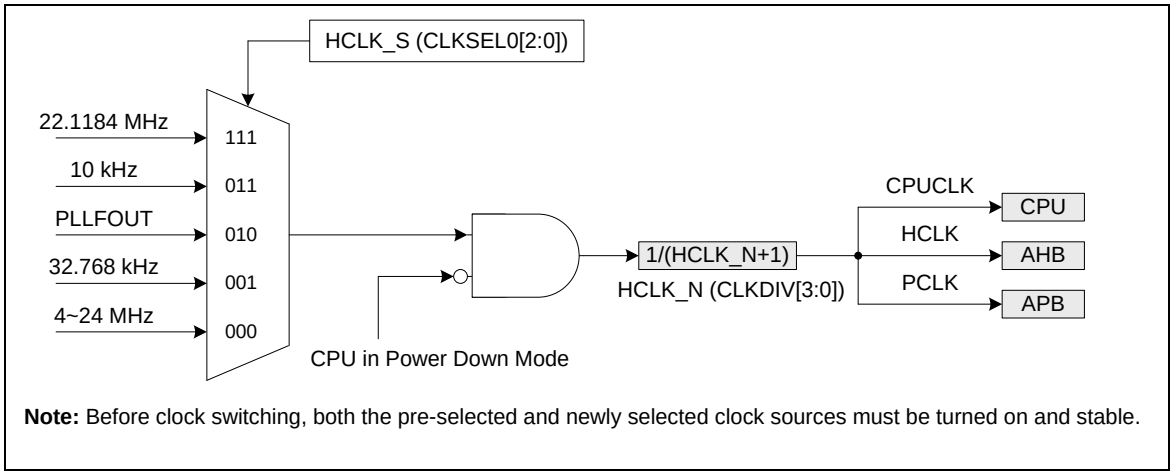


Figure 6-4 Clock Generator Global View Diagram

6.3.2 System Clock and SysTick Clock

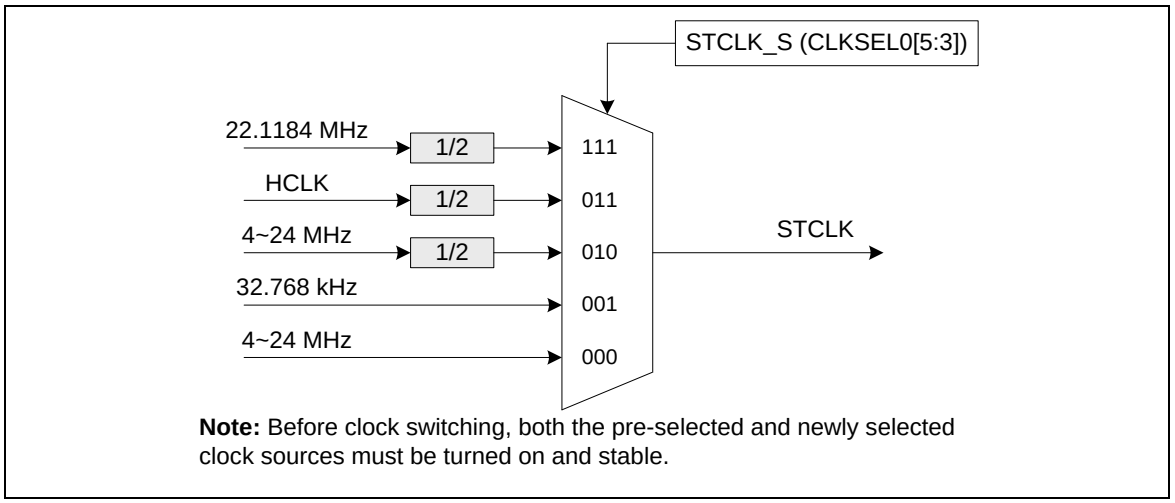
The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6-5.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-5 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6-6.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-6 SysTick Clock Control Block Diagram

6.3.3 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator clock
- RTC/WDT/Timer/PWM Peripherals Clock (when 32.768 kHz external low speed crystal oscillator or 10 kHz intertnal low speed RC oscillator is adopted as clock source)

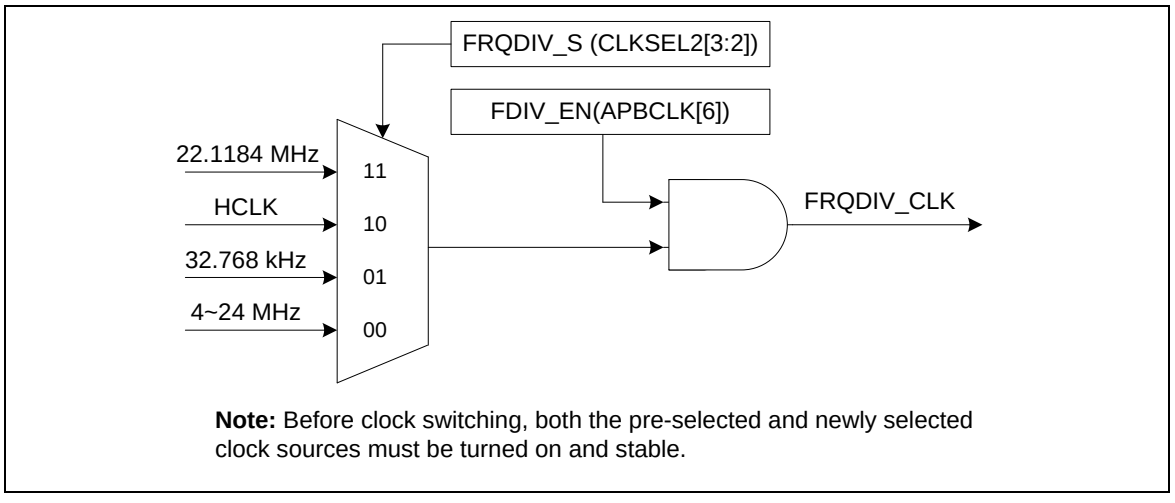
6.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-7 Clock Source of Frequency Divider

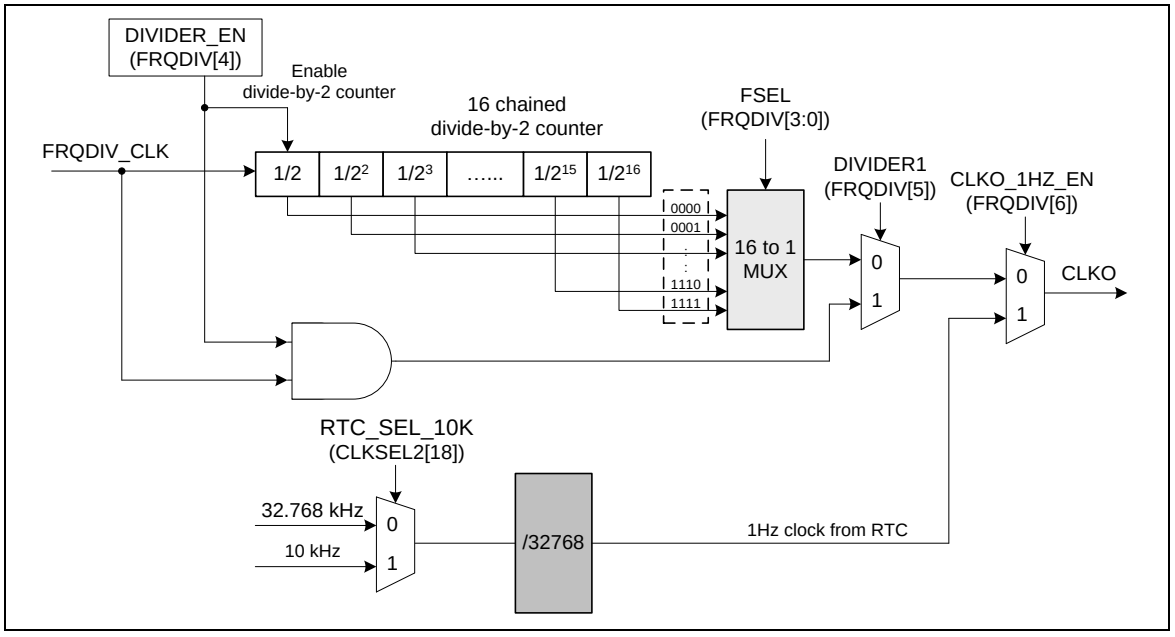


Figure 6-8 Frequency Divider Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro® NUC2201 has 128K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro® NUC2201 supports another flexible feature: configurable Data Flash size. The Data Flash size is decided by Data Flash enable (DFEN) in Config0 and Data Flash base address (DFBADR) in Config1. When DFEN is set to 1, the Data Flash size is zero and the APROM size is 128K bytes. When DFEN is set to 0, the APROM and Data Flash share 128K bytes continuous address and the start address of Data Flash is defined by (DFBADR) in Config1.

6.4.2 Features

- Runs up to 50 MHz with zero wait cycle for continuous address read access and runs up to 72 MHz with one wait cycle for continuous address read.
- All embedded flash memory supports 512 bytes page erase
- 128 KB application program memory (APROM)
- 8 KB In-System-Programming (ISP) loader program memory (LDROM)
- Configurable Data Flash size with 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

6.5 External Bus Interface (EBI)

6.5.1 Overview

The NuMicro® NUC2201 series LQFP-64 package equips an external bus interface (EBI) for access external device.

To save the connections between external device and this chip, EBI supports address bus and data bus multiplex mode. And, address latch enable (ALE) signal is used to differentiate the address and data cycle.

6.5.2 Features

External Bus Interface has the following functions:

- Supports external devices with max. 64 KB size (8-bit data width)/128 KB (16-bit data width)
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports 8-bit or 16-bit data width
- Supports variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD)
- Supports address bus and data bus multiplex mode to save the address pins
- Supports configurable idle cycle for different access condition: Write command finish (W2X), Read-to-Read (R2R)

6.6 General Purpose I/O (GPIO)

6.6.1 Overview

The NuMicro® NUC2201 series has up to 45 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 45 pins are arranged in 5 ports named as GPIOA, GPIOB, GPIOC, GPIOE and GPIOF. The GPIOA/B/C/E port has the maximum of 15 pins and GPIOF port has the maximum of 2 pins. Each of the 45 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} is from 5.0 V to 2.5 V.

6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function.

6.7 PDMA Controller (PDMA)

6.7.1 Overview

The NuMicro® NUC2201 series DMA contains nine-channel peripheral direct memory access (PDMA) controller and a cyclic redundancy check (CRC) generator.

The PDMA that transfers data to and from memory or transfer data to and from APB devices. For PDMA channel (PDMA CH0~CH8), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. Software can stop the PDMA operation by disable PDMA PDMACEN (PDMA_CSRx[0]). The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The PDMA controller can increase source or destination address or fixed them as well.

The DMA controller contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU PIO mode and DMA transfer mode.

6.7.2 Features

- Supports nine PDMA channels and one CRC channel. Each PDMA channel can support a unidirectional transfer
- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Hardware round robin priority scheme. DMA channel 0 has the highest priority and channel 8 has the lowest priority
- PDMA operation
  - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
  - Supports word/half-word/byte transfer data width from/to peripheral
  - Supports address direction: increment, fixed.
- Cyclic Redundancy Check (CRC)
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8: $X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$
    - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
  - Supports programmable CRC seed value.
  - Supports programmable order reverse setting for input data and CRC checksum.
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports CPU PIO mode or DMA transfer mode.
  - Supports the follows write data length in CPU PIO mode
    - 8-bit write mode (byte): 1-AHB clock cycle operation.
    - 16-bit write mode (half-word): 2-AHB clock cycle operation.

- 32-bit write mode (word): 4-AHB clock cycle operation.

- Supports byte alignment transfer data length and word alignment transfer source address in CRC DMA mode.

6.8 Timer Controller (TIMER)

6.8.1 Overview

The timer controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.8.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external counter pin (TM0~TM3)
- Supports external pin capture (TM0_EXT~TM3_EXT) for interval measurement
- Supports external pin capture (TM0_EXT~TM3_EXT) for reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.9 PWM Generator and Capture Timer (PWM)

6.9.1 Overview

The NuMicro® NUC2201 series has 2 sets of PWM group supporting a total of 3 sets of PWM generators that can be configured as 6 independent PWM outputs, PWM0~PWM5, or as 3 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5) with 3 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 3 sets of PWM generators provide eight independent PWM interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DZEN01 (PCR[4]) is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3) and (PWM4, PWM5) are controlled by PWM2 and PWM4 timers and Dead-zone generator 2 and 4, respectively. Refer from **錯誤! 找不到參照來源。** to **錯誤! 找不到參照來源。** for the architecture of PWM Timers.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0 (CCR0[1]) (Rising latch Interrupt enable) and CFL_IE0 (CCR0[2]) (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CRL_IE1 (CCR0[17]) and CFL_IE1 (CCR0[18]). And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will be 1/900ns ≈ 1000 kHz

6.9.2 Features

6.9.2.1 PWM Function:

- Up to 2 PWM groups (PWMA/PWMB) to support 6 PWM channels or 3 complementary PWM paired channels
- PWM group A has two PWM generators and PWM group B has one PWM generator with each PWM generator supporting one 8-bit prescaler, two clock dividers, two PWM-timers, one Dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode
- Edge-aligned type or Center-aligned type option
- PWM trigger ADC start-to-conversion

6.9.2.2 Capture Function:

- Timing control logic shared with PWM Generators
- Supports 6 Capture input channels shared with 6 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

6.10 Watchdog Timer (WDT)

6.10.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.10.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer reset delay period
  - Selectable it includes (1026、130、18 or 3) * WDT_CLK reset delay period.
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG0[31] Watchdog Enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

6.11 Window Watchdog Timer (WWDT)

6.11.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.11.2 Features

- 6-bit down counter value (WWDTVAL[5:0]) and 6-bit compare window value (WWDTCR[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value to programmable maximum 11-bit prescale counter period of WWDT counter

6.12 Real Time Clock (RTC)

6.12.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

The RTC controller also offers 80 bytes spare registers to store user's important information.

6.12.2 Features

- Supports real time counter in Time Loading Register (TLR) (hour, minute, second) and calendar counter in Calendar Loading Register (CLR) (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in Time Alarm Register (TAR) and Calendar Alarm Register (CAR) register
- Selectable 12-hour or 24-hour time scale in Time Scale Selection Register (TSSR) register
- Supports Leap Year indication in Leap Year Indicator Register (LIR) register
- Supports Day of the Week counter in Day of the Week Register (DWR) register
- Frequency of RTC clock source compensate by RTC Frequency Compensation Register (FCR) register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated
- Supports 80 bytes spare registers

6.13 UART Interface Controller (UART)

6.13.1 Overview

The NuMicro® NUC2201 series provides up to three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UART. Besides, only UART0 and UART1 support the flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave function and RS-485 function mode. Each UART Controller channel supports seven types of interrupts.

6.13.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 64/16/16 bytes (UART0/UART1/UART2) entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0 and UART1 support)
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0 and UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- UART0/UART1 can through DMA channels to receive/transmit data
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3-/16-bit duration for normal mode
- LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode.
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by RTS pin (UART0 and UART1 support)

6.14 I²C Serial Interface Controller (I²C)

6.14.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

6.14.2 Features

The I²C bus uses two wires (I2Cn_SDA and I2Cn_SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C serial interface controller
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in a 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function

6.15 Serial Peripheral Interface (SPI)

6.15.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro® NUC2201 series contains up to two sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a master or a slave device.

The SPI controller supports the variable bus clock function for special applications. This controller also supports the PDMA function to access the data buffer and also supports Dual I/O Transfer mode.

6.15.2 Features

- Up to two sets of SPI controllers
- Supports Master or Slave mode operation
- Supports Dual I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32 bits
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Two slave select lines in Master mode
- Supports the Byte Reorder function
- Supports Byte or Word Suspend mode
- Variable output bus clock frequency in Master mode
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface

6.16 USB Device Controller (USBD)

6.16.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/ isochronous transfer types, and use High Internal RC Oscillator (HIRC48M) obtain to crystal-less option.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through “buffer segmentation register (USB_BUFSEGx)”.

There are 8 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the wake-up function, device plug-in or plug-out event, USB events, and BUS events. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If DRVSE0 (USB_DRVSE0[0]) is set to 1, the USB controller will force the output of USB_D+ and USB_D- to level low. After DRVSE0 bit is cleared to 0, host will enumerate the USB device again.

Please refer to *Universal Serial Bus Specification Revision 1.1* for details.

6.16.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Provides 8 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provides remote wake-up capability
- Supports Crystal-less

6.17 Analog-to-Digital Converter (ADC)

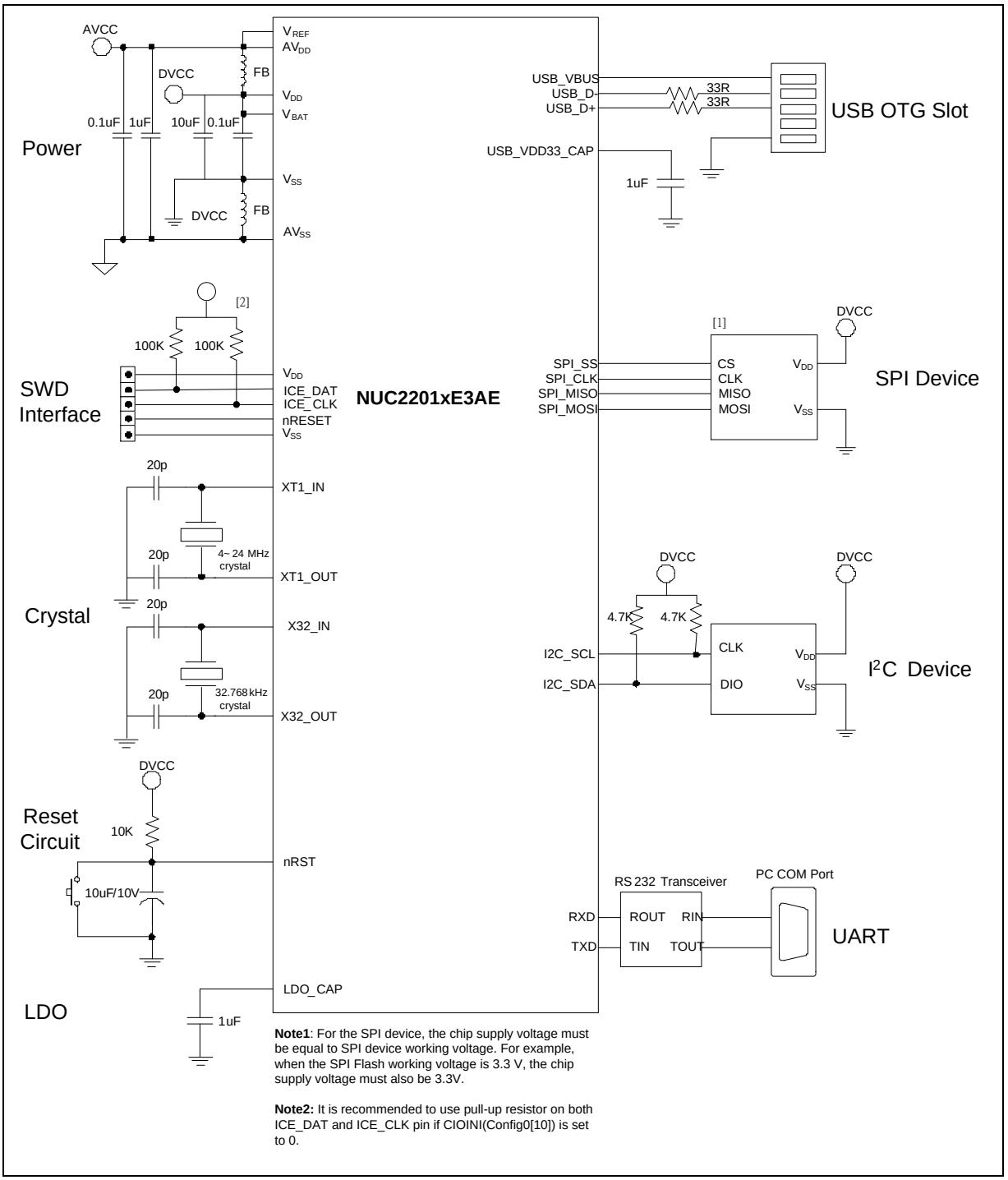
6.17.1 Overview

The NuMicro® NUC2201 series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 12 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converter can be started by software, PWM Center-aligned trigger and external STADC pin.

6.17.2 Features

- Analog input voltage range: 0~VREF
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 12 single-end analog input channels or 5 differential analog input channels
- Up to 1 MSPS conversion rate (chip working at 5V)
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by:
  - Writing 1 to ADST bit (ADCR[11])through software
  - PWM Center-aligned trigger
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Supports two set digital comparators. The conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 3 input sources: external analog voltage, internal Band-gap voltage, and internal temperature sensor output

7 APPLICATION CIRCUIT



Note1: For the SPI device, the chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the chip supply voltage must also be 3.3V.

Note2: It is recommended to use pull-up resistor on both ICE_DAT and ICE_CLK pin if CIOINI(Config0[10]) is set to 0.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Junction temperature	T_J	-40	+125	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

8.1.1 EMC characteristics

Symbol	Parameter	Conditions	Maximum value	Unit
V_{EFTB}	1. Fast transient voltage burst limits to be applied through 0.1 uF + 10 uF on VDD and VSS pins to induce a functional disturbance 2. to be applied through 1 uF on LDO_Pin and VSS pins	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 72 MHz	4.4	kV

Note: Guaranteed by characterization results, not tested in production.

Symbol	Ratings	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, excepte X32_IN pin	8	kV
		T_A = +25 °C	4	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, excepte X32_IN pin	1	
		T_A = +25 °C	0.5	

Note: Guaranteed by characterization results, not tested in production.

Symbol	Parameter	Conditions	Value	Unit
LU	Static latch-up class	T_A = +25 °C	300	mA

Note: Guaranteed by characterization results, not tested in production.

8.2 DC Electrical Characteristics

(V_{DD}-V_{SS} = 5.5 V, T_A = 25°C, F_{OSC} = 72 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation Voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5V ~ 5.5V up to 72 MHz				
RTC Operation voltage for PF.0~PF.2	V_{BAT}	2.5	-	5.5	V					
Power Ground	V_{SS} AV_{SS}	-0.3	0	0.3	V					
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} ≥ 2.5V				
Band-gap Voltage	V_{BG}	1.21	-	1.29	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = -40°C~105°C				
Allowed voltage difference for V_{DD} and AV_{DD}	V_{DD}-AV_{DD}	-0.3	-	0.3	V					
Operating Current Normal Run Mode at 72 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD1}		24		mA	V_{DD}	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{DD2}		16		mA	5.5V	12 MHz	X	V	X
	I_{DD3}		22.5		mA	3.3V	12 MHz	X	V	V
	I_{DD4}		14.5		mA	3.3V	12 MHz	X	V	X
Operating Current Normal Run Mode at 50 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD5}		18		mA	5.5V	12 MHz	X	V	V
	I_{DD6}		12.5		mA	5.5V	12 MHz	X	V	X
	I_{DD7}		16.5		mA	3.3V	12 MHz	X	V	V
	I_{DD8}		11		mA	3.3V	12 MHz	X	V	X
Operating Current Normal Run Mode at 22.1184 MHz while(1){} executed from flash VLDO =1.8 V	I_{DD9}	-	9	-	mA	5.5V	X	V	X	V
	I_{DD10}	-	4.5	-	mA	5.5V	X	V	X	X
	I_{DD11}	-	9	-	mA	3.3V	X	V	X	V
	I_{DD12}	-	4.5	-	mA	3.3V	X	V	X	X
Operating Current Normal Run Mode at 12 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD13}		5.5		mA	5.5V	12 MHz	X	X	V
	I_{DD14}		4.5		mA	5.5V	12 MHz	X	X	X
	I_{DD15}		4		mA	3.3V	12 MHz	X	X	V
	I_{DD16}		3		mA	3.3V	12 MHz	X	X	X
Operating Current	I_{DD17}		3		mA	5.5V	4 MHz	X	X	V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Normal Run Mode at 4 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD18}		2.5		mA	5.5V	4 MHz	X	X	X
	I_{DD19}		1.7		mA	3.3V	4 MHz	X	X	V
	I_{DD20}		1.3		mA	3.3V	4 MHz	X	X	X
Operating Current HCLK = 32.768 kHz while(1){} executed from flash	I_{DD21}		133		uA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital modules
						5.5V	32.768	X	X	V
	I_{DD22}		130		uA	5.5V	32.768	X	X	X
	I_{DD23}		119		uA	3.3V	32.768	X	X	V
	I_{DD24}		116		uA	3.3V	32.768	X	X	X
Operating Current Normal Run Mode at 10 kHz while(1){} executed from flash VLDO =1.8 V	I_{DD25}		127		µA	VDD	HXT/LXT	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{DD26}		126		µA	5.5V	X	10	X	X
	I_{DD27}		113		µA	3.3V	X	10	X	V
	I_{DD28}		112		µA	3.3V	X	10	X	X
Operating Current Idle Mode at 72 MHz VLDO =1.8 V	I_{IDLE1}		17		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{IDLE2}		9		mA	5.5V	12 MHz	X	V	X
	I_{IDLE3}		15.5		mA	3.3V	12 MHz	X	V	V
	I_{IDLE4}		7.5		mA	3.3V	12 MHz	X	V	X
Operating Current Idle Mode at 50 MHz VLDO =1.8 V	I_{IDLE5}		13		mA	5.5V	X	V	X	X
	I_{IDLE6}		7.5		mA	5.5V	X	V	X	X
	I_{IDLE7}		11.5		mA	3.3V	X	V	X	V
	I_{IDLE8}		6		mA	3.3V	X	V	X	X
Operating Current Idle Mode at 22.1184 MHz VLDO =1.8 V	I_{IDLE9}	-	6.5	-	mA	5.5V	X	V	X	X
	I_{IDLE10}	-	2	-	mA	5.5V	X	V	X	X
	I_{IDLE11}	-	6.5	-	mA	3.3V	X	V	X	V
	I_{IDLE12}	-	2	-	mA	3.3V	X	V	X	X
Operating Current Idle Mode at 12 MHz V_{LDO} =1.8 V	I_{IDLE13}		4.3		mA	5.5V	12 MHz	X	X	V
	I_{IDLE14}		3		mA	5.5V	12 MHz	X	X	X
	I_{IDLE15}		2.9		mA	3.3V	12 MHz	X	X	V
	I_{IDLE16}		1.6		mA	3.3V	12 MHz	X	X	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Idle Mode at 4 MHz V_{LDO} =1.8 V	I_{IDLE17}		2.6		mA	5.5V	4 MHz	X	X	V
	I_{IDLE18}		2.2		mA	5.5V	4 MHz	X	X	X
	I_{IDLE19}		1.4		mA	3.3V	4 MHz	X	X	V
	I_{IDLE20}		0.9		mA	3.3V	4 MHz	X	X	X
Operating Current Idle Mode at 32.768 kHz	I_{IDLE21}		130		µA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital modules
						5.5V	32.768	X	X	V
	I_{IDLE22}		126		µA	5.5V	32.768	X	X	X
	I_{IDLE23}		116		µA	3.3V	32.768	X	X	V
	I_{IDLE24}		113		µA	3.3V	32.768	X	X	X
Operating Current Idle Mode at 10 kHz	I_{IDLE25}		126		µA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{IDLE26}		125		µA	5.5V	X	10	X	X
	I_{IDLE27}		112		µA	3.3V	X	10	X	V
	I_{IDLE28}		111		µA	3.3V	X	10	X	X
Standby Current Power-down Mode (Deep Sleep Mode) V_{LDO} =1.6 V	I_{PWD1}		13		µA	V_{DD}	HXT/HIRC PLL	LXT (kHz)	RTC	RAM retension
						5.5V	X	X	X	V
	I_{PWD2}		15		µA	5.5V	X	32.768	V	V
	I_{PWD3}		11		µA	3.3V	X	X	X	V
	I_{PWD4}		13		µA	3.3V	X	32.768	V	V
RTC Operating Current	I_{VBAT}		2		µA	V_{BAT} = 5.0 V, 32.768 kHz external low speed crystal oscillator (LXT), RTC ON and V_{DD}/AV_{DD} power domain OFF.				
			2		µA	V_{BAT} = 3.0 V, 32.768 kHz external low speed crystal oscillator (LXT), RTC ON and V_{DD}/AV_{DD} power domain OFF.				
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}		-67	-75	µA	V_{DD} = V_{BAT} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}				
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-1	-	+1	µA	V_{DD} = V_{BAT} = 5.5V, 0<V_{IN}<V_{DD} Open-drain or input only mode.				

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]		-610	-650	µA	V_{DD} = 5.5V, V_{IN}=2.0V
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = V_{BAT} = 4.5 V
		-0.3	-	0.6		V_{DD} = V_{BAT} = 2.5 V
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = V_{BAT} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = V_{BAT} =3.0V
Input Low Voltage XT1_IN[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = V_{BAT} = 4.5V
		0	-	0.4		V_{DD} = V_{BAT} = 3.0V
Input High Voltage XT1_IN[*2]	V_{IH3}	3.5	-	V_{DD} +0.3	V	V_{DD} = V_{BAT} = 5.5V
		2.4	-	V_{DD} +0.3		V_{DD} = V_{BAT} = 3.0V
X32 Output Pin	V_{XOUT}	0.6		0.9	V	
Input Low Voltage X32I[*4]	V_{IL4}	0	-	V_{XOUT} - 0.3	V	
Input High Voltage X32I[*4]	V_{IH4}	V_{XOUT} +0.3		1.8	V	
Negative going threshold (Schmitt input), nRESET	V_{ILS}	-0.3	-	0.2V_{DD}	V	
Positive going threshold (Schmitt input), nRESET	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V	
Internal nRESET pin pull up resistor	R_{RST}	40		150	kΩ	
Negative going threshold (Schmitt input),	V_{ILS}	-0.3	-	0.3 VDD	V	
Positive going threshold (Schmitt input),	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-400		µA	V_{DD} = V_{BAT} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-80		µA	V_{DD} = V_{BAT} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-73		µA	V_{DD} = V_{BAT} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-30	-65		mA	V_{DD} = V_{BAT} = 4.5V, V_S = 2.4V
	I_{SR22}	-3	-5.2		mA	V_{DD} = V_{BAT} = 2.7V, V_S = 2.2V

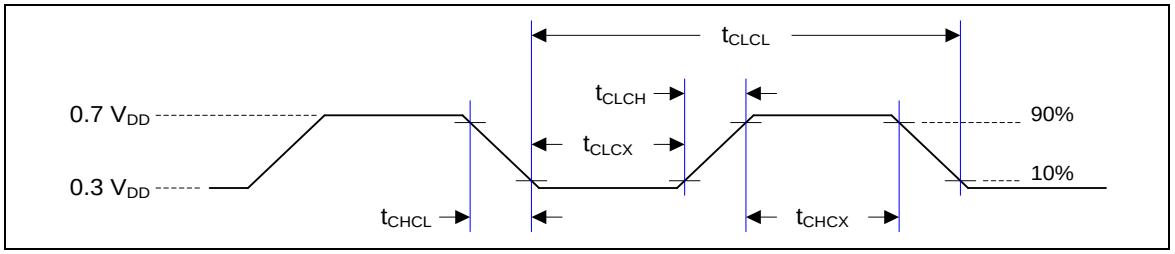
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{SR22}	-2.5	-5		mA	$V_{DD} = V_{BAT} = 2.5V$, $V_S = 2.0V$
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	9	13		mA	$V_{DD} = V_{BAT} = 4.5V$, $V_S = 0.45V$
	I_{SK1}	6	9		mA	$V_{DD} = V_{BAT} = 2.7V$, $V_S = 0.45V$
	I_{SK1}	4	8		mA	$V_{DD} = V_{BAT} = 2.5V$, $V_S = 0.45V$

Note:

1. nRESET pin is a Schmitt trigger input.
2. XT1_IN is a CMOS input.
3. Pins of PA, PB, PC, PD, PE and PF can source a transition current when they are being externally driven from 1 to 0. In the condition of $V_{DD} = 5.5$ V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.
4. If X32I is as external clock input, the input high voltage should be lower than 1.8V to avoid chip damage.

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

8.3.2 External 4~24 MHz High Speed Crystal

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2	-	mA	12 MHz, V_{DD} = 5.5V
		-	0.8	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

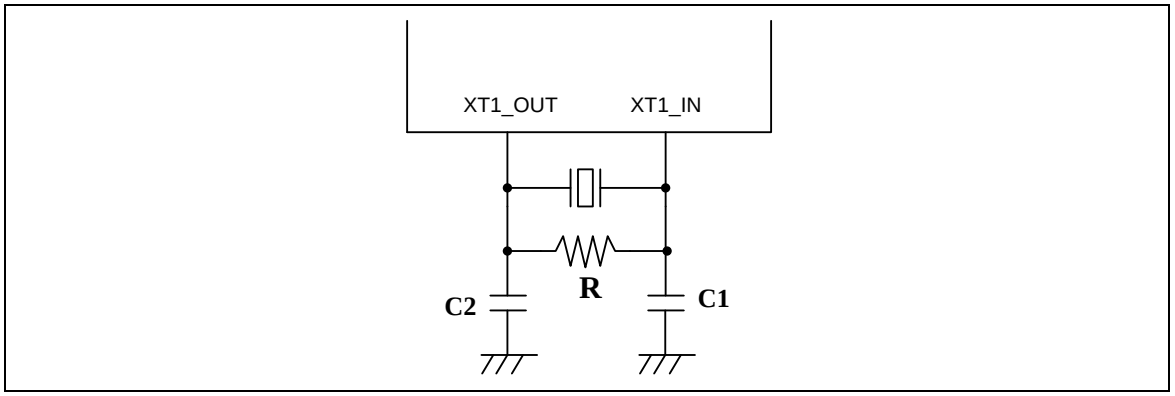
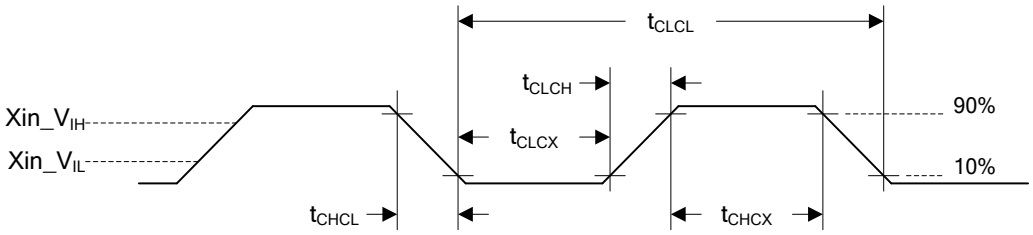


Figure 8-1 Typical Crystal Application Circuit

8.3.3 32.768 kHz External Low Speed Crystal Oscillator (LXT)



Note: *Duty cycle is 50%.*

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Operation Temperature	-	-40	-	105	℃
Operation Current	32.768KHz at V_{DD}=5V		1.6		μA
Clock Frequency	External crystal	-	32.768	-	kHz

8.3.3.1 Typical Crystal Application Circuits

CRYSTAL	C_1	C_2
32.768 kHz	10~20 pF	10~20 pF

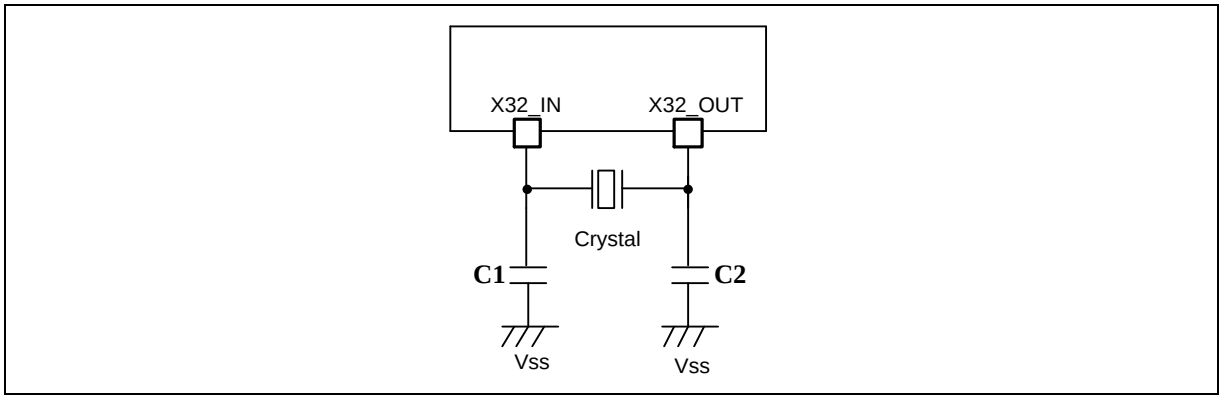


Figure 8.3-2 Typical Crystal Application Circuit

8.3.4 Internal 22.1184 MHz High Speed Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-3	-	+3	%	T_A = -40 ℃ ~ 105 ℃ V_{DD} = 2.5 V ~ 5 .5 V
I_{HRC}	Operating Current	-	1200	-	μA	T_A = 25 ℃,V_{DD} = 5 V

8.3.5 Internal 48 MHz High Speed Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	48		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-2	-	+2	%	T_A = -40 ℃ ~ 105 ℃ V_{DD} = 2.5 V ~ 5 .5 V
I_{HRC}	Operating Current	-	640	-	μA	T_A = 25 ℃,V_{DD} = 5 V

8.3.6 Internal 10 kHz Low Speed Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	2.5	-	5.5	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-10	-	+10	%	V_{DD} = 2.5 V ~ 5.5 V T_A = 25℃
		-50	-	+50	%	V_{DD} = 2.5 V ~ 5.5 V T_A = -40℃ ~ +105℃

8.3.7 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock		4		24	MHz
f_{PLL_OUT}	PLL multiplier output clock		50		500	MHz
T_S	PLL stable time[*1]		100		200	µs
Jitter	Cycle-to-cycle Jitter[*2]	Peak to peak @ 480M		200	350	ps

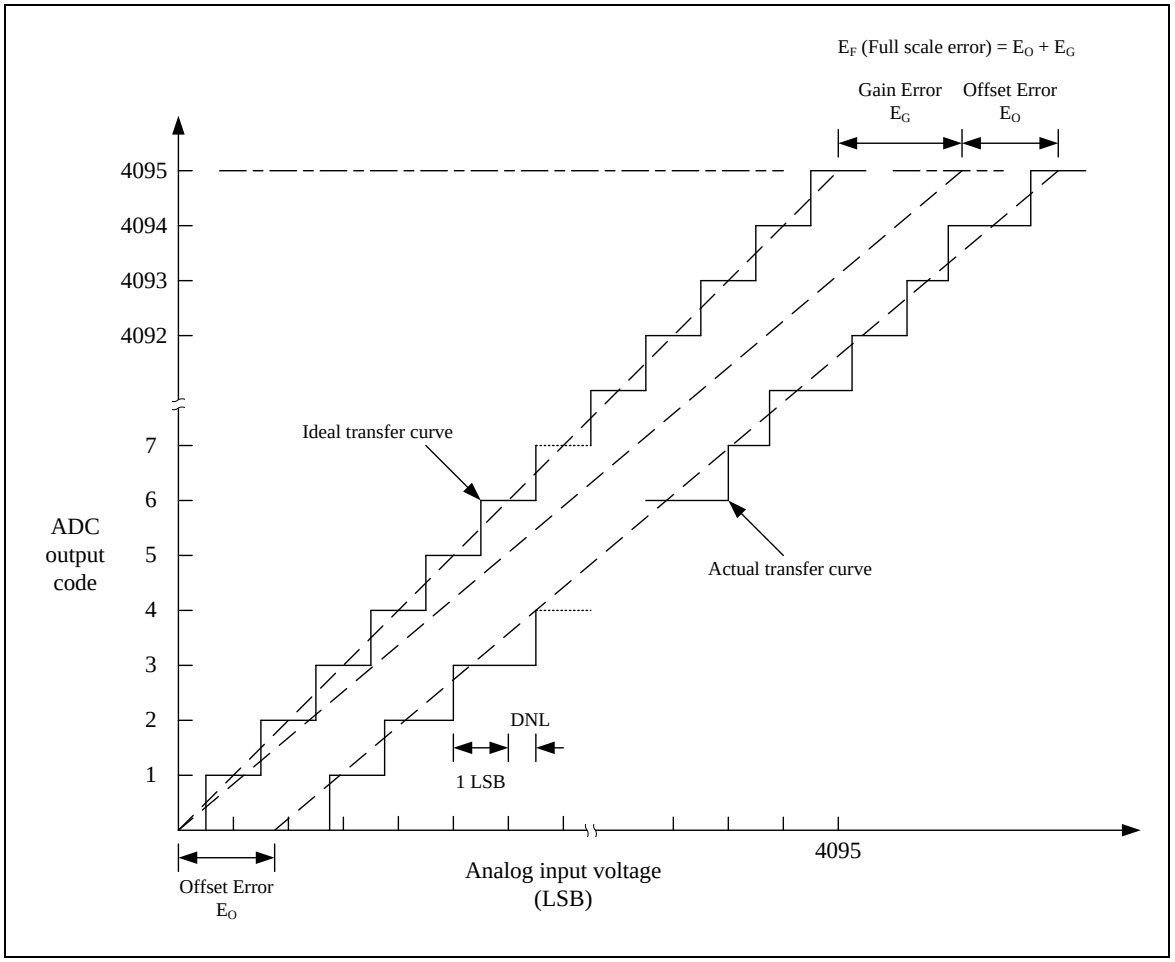
Note: Guaranteed by characterization and design results, not tested in production.

8.4 Analog Characteristics

8.4.1 12-bit SARADC Specification

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution		12		Bit	-
DNL	Differential Nonlinearity Error	-	-	±3	LSB	-
INL	Integral Nonlinearity Error	-	-	±4	LSB	-
E_O	Offset Error	-	3	-	LSB	-
E_G	Gain Error (Transfer Gain)	-	-2	-	LSB	-
E_A	Absolute Error	-	4	-	LSB	-
-	Monotonic		Guaranteed		-	-
F_{ADC}	ADC Clock Frequency	-	-	21	MHz	
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	1000	kSPS	
T_{ACQ}	Acquisition Time (Sample Stage)		2~9		$1/F_{ADC}$	-
T_{CONV}	Total Conversion Time		16~23		$1/F_{ADC}$	-
AV_{DD}	Supply Voltage	2.5	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	2.8	-	mA	AV_{DD} = 5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	6	-	pF	-
R_{IN}	Input Load	-	6.5	-	kΩ	-

Note: The condition is that the error in a conversion started after ADC enable is less than ±0.5 LSB. The reference and input signal are already settled.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.4.2 LDO and Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	105	℃	

Notes:

1. It is recommended that a 0.1 uF or higher capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

2. To ensure power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

8.4.3 Low Voltage Reset Specification

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Supply Voltage	0		5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{LVR}	Quiescent Current	-	1	5	μA	V_{DD} = 5.5 V
V_{LVR}	Threshold Voltage	1.90	2.00	2.10	V	TA = 25 ℃
		1.70	1.90	2.10	V	TA = -40 ℃
		2.00	2.20	2.45	V	TA = 105 ℃

8.4.4 Brown-out Detector Specification

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	-	140	μA	AV_{DD} = 5.5 V
V_{BOD}	Brown-out Voltage (Falling edge)	4.2	4.4	4.6	V	BOV_VL [1:0] = 11
		3.5	3.7	3.9	V	BOV_VL [1:0] = 10
		2.55	2.7	2.85	V	BOV_VL [1:0] = 01
		2.05	2.2	2.35	V	BOV_VL [1:0] = 00
V_{BOD}	Brown-out Voltage (Rising edge)	4.3	4.5	4.7	V	BOV_VL [1:0] = 11
		3.6	3.8	4.0	V	BOV_VL [1:0] = 10
		2.6	2.75	2.9	V	BOV_VL [1:0] = 01
		2.1	2.25	2.4	V	BOV_VL [1:0] = 00

8.4.5 Power-on Reset Specification

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Reset Voltage	1.6	2	2.4	V	-
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	100	mV	
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms	
t_{POR}	Minimum Time for V_{DD} Stays at VPOR to Ensure Power-on Reset	0.5	-	-	ms	

Note: Guaranteed by characterization results, not tested in production.

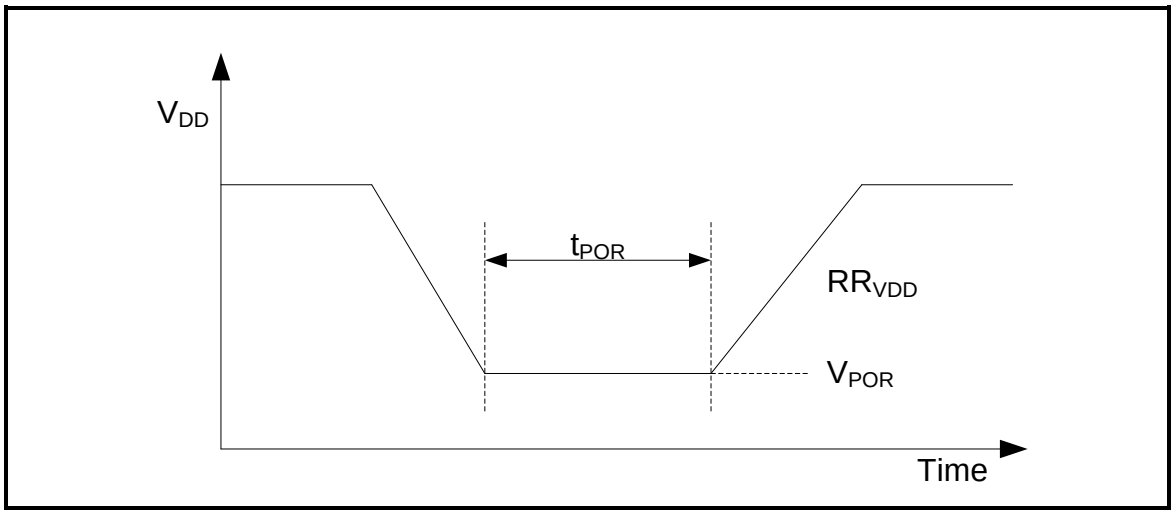


Figure 8-3 Power-up Ramp Condition

8.4.6 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	-	105	℃	
I_{TEMP}	Current Consumption	-	16	-	μA	
-	Gain	-1.55	-1.672	-1.75	mV/℃	
-	Offset	735	748	755	mV	T_A = 0 ℃

Note:

1. Guaranteed by design, not tested in production.
2. V_{TEMP} (mV) = T_c (mV/°C) x Temperature (°C) + V_{os} (mV)

8.4.7 USB PHY

8.4.7.1 Low-/full-Speed DC Electrical Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Input High (driven)	2.0	-		V	-
V_{IL}	Input Low	-	-	0.8	V	-
V_{DI}	Differential Input Sensitivity	0.2	-		V	|PADP-PADM|
V_{CM}	Differential Common-mode Range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended Receiver Threshold	0.8	-	2.0	V	-
	Receiver Hysteresis	-	200		mV	-
V_{OL}	Output Low (driven)	0	-	0.3	V	-
V_{OH}	Output High (driven)	2.8	-	3.6	V	-
V_{CRS}	Output Signal Cross Voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up Resistor	1.425	-	1.575	kΩ	-
Z_{DRV}	Driver Output Resistance	-	10	-	Ω	Steady state drive*
C_{IN}	Transceiver Capacitance	-	-	20	pF	Pin to GND

*Driver output resistance doesn't include series resistor resistance.

8.4.7.2 USB Full-Speed Driver Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
T_{FR}	Rise Time	4	-	20	ns	C_L=50p
T_{FF}	Fall Time	4	-	20	ns	C_L=50p
T_{FRFF}	Rise and Fall Time Matching	90	-	111.11	%	$T_{FRFF}=T_{FR}/T_{FF}$

8.4.7.3 USB LDO Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{BUS}	VBUS Pin Input Voltage	4.0	5.0	5.5	V	-
V_{DD33}	LDO Output Voltage	2.97	3.3	3.63	V	-
C_{bp}	External Bypass Capacitor	-	1.0	-	uF	-

8.5 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.62	1.8	1.98	V	-
N_{ENDUR}	Endurance	20,000	-		cycles[1]	-
T_{RET}	Data Retention	100	-	-	year	T_A = 25℃
		10			year	T_A = 85℃
T_{ERASE}	Page Erase Time	20		-	ms	-
T_{PROG}	Program Time	60		-	us	-
I_{DD1}	Read Current	-	9	-	mA	-
I_{DD2}	Program Current	-	8	-	mA	-
I_{DD3}	Erase Current	-	12	-	mA	-

Notes:

1. Number of program/erase cycles.
2. VFLA is source from chip LDO output voltage.

8.6 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

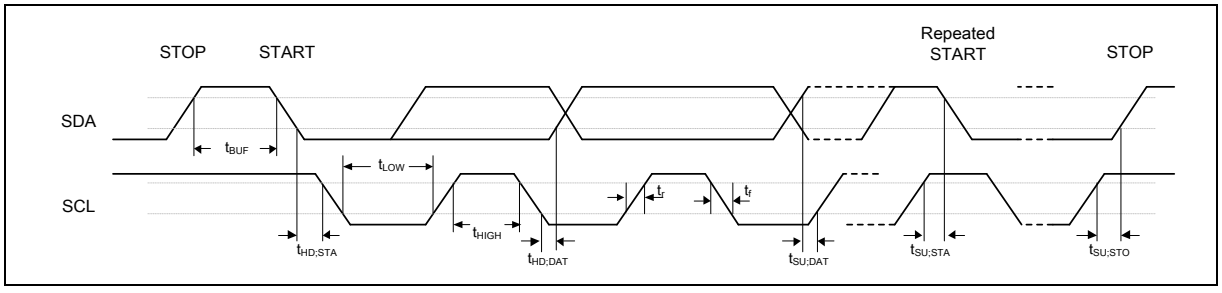


Figure 8-4 I²C Timing Diagram

8.7 SPI Dynamic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI Master Mode (VDD = 4.5 V ~ 5.5 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4	-	-	ns
t_V	Data output valid time	-	1	2	ns
SPI Master Mode (VDD = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4.5	-	-	ns
t_V	Data output valid time	-	2	4	ns
SPI Slave Mode (VDD = 4.5 V ~ 5.5 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	3.5	-	-	ns
t_V	Data output valid time	-	16	22	ns
SPI Slave Mode (VDD = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4.5	-	-	ns
t_V	Data output valid time	-	18	24	ns

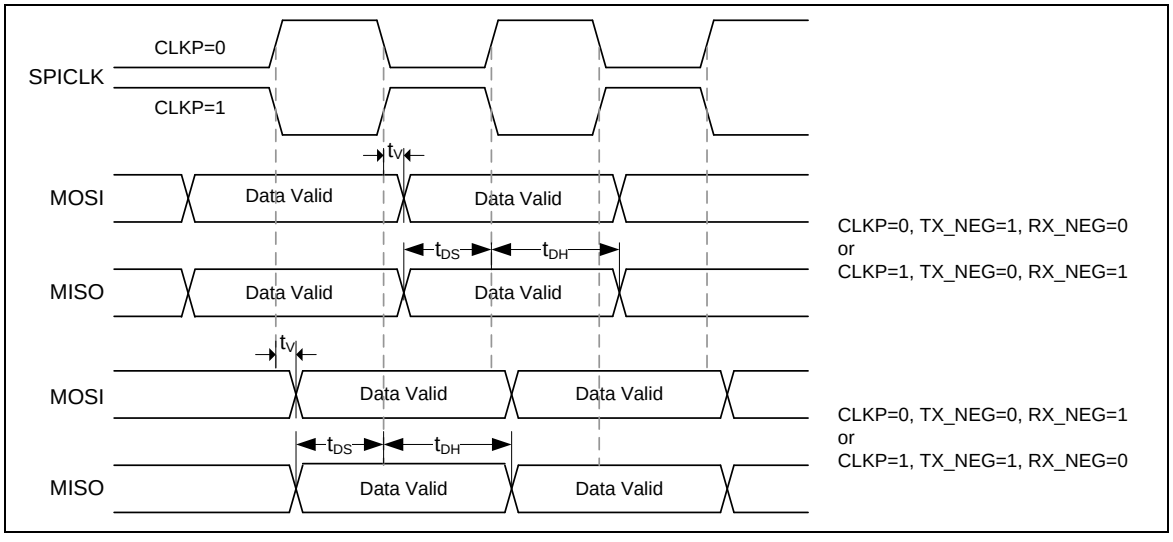


Figure 8-5 SPI Master Mode Timing Diagram

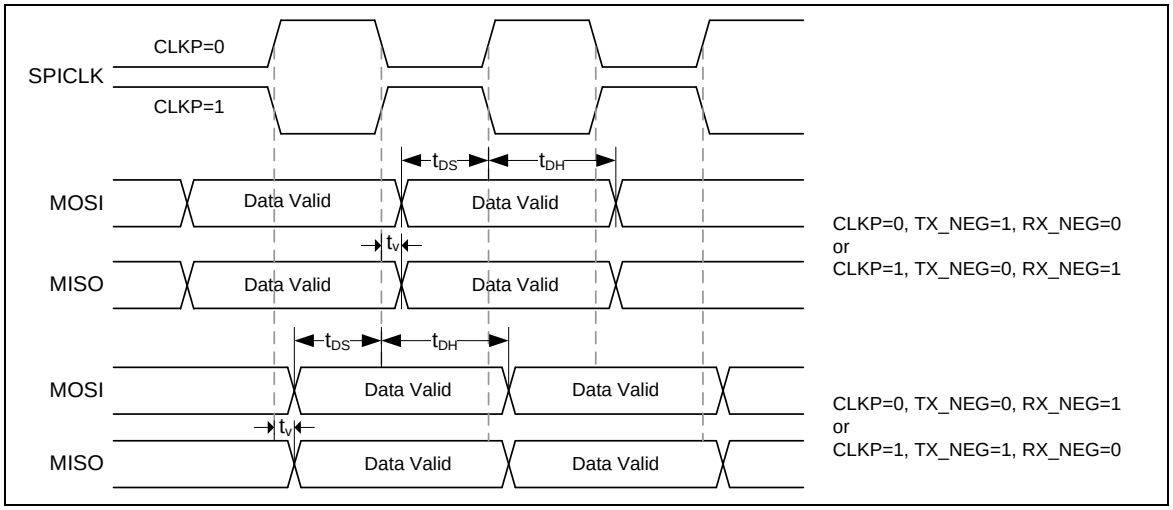
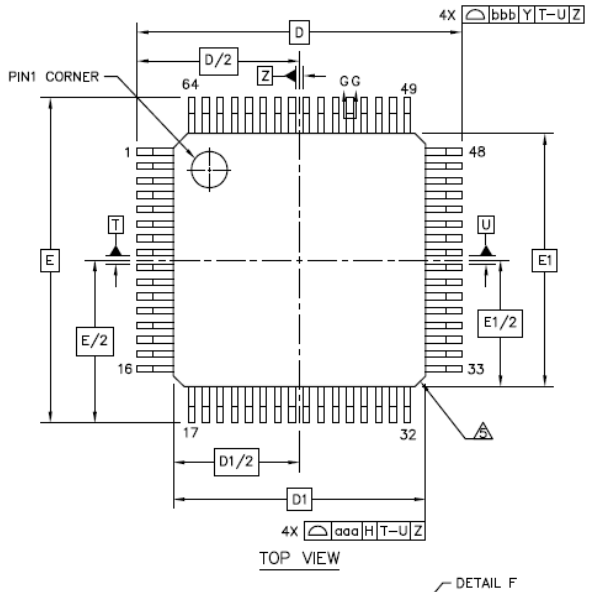


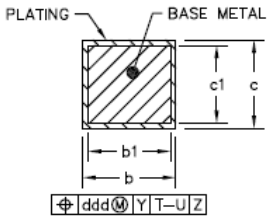
Figure 8-6 SPI Slave Mode Timing Diagram

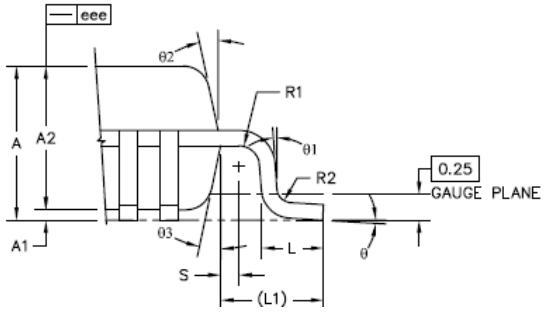
9 PACKAGE DIMENSIONS

9.1 64-pin LQFP (7x7x1.4 mm footprint 2.0 mm)

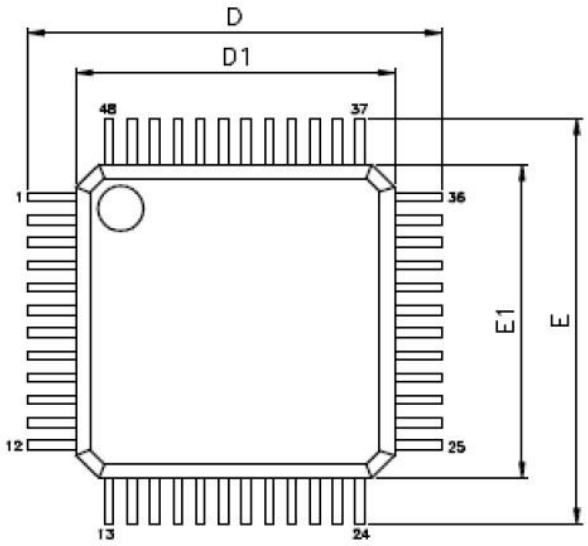


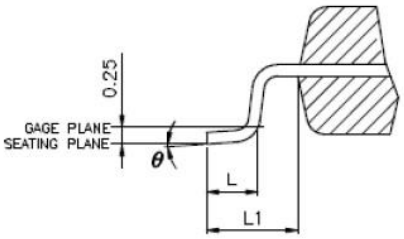
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

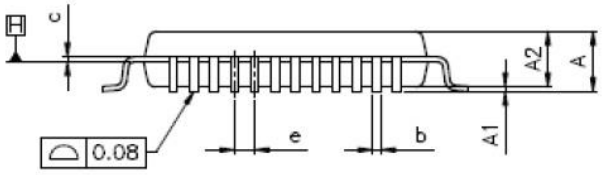




9.2 48-pin LQFP (7x7x1.4 mm footprint 2.0 mm)







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

10 REVISION HISTORY

Date	Revision	Description
2018.08.24	1.00	1. Initial version

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