W83793G / W83793AG
Nuvoton H/W Monitor

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1. GENERAL DESCRIPTION

The W83793G is an evolving version of the W83792D. Besides the conventional functions of the W83792D, the W83793G uniquely provides several innovative features. It is ASF 2.0 specification compliant, SMBus 2.0 ARP command compatible and has 8 sets of SMART FAN™. The W83793G can monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system, such as a server, or a workstation to work stably and efficiently.

A 10-bit analog-to-digital converter (ADC) is built inside the W83793G. The W83793G can simultaneously monitor 10 analog voltage inputs (including power 5VDD/5VSB/VBAT/Vtt monitoring), 12 fan tachometer inputs, 6 remote temperatures, 4 of which support Current Mode (dual current source) temperature measurement method, and the Watch Dog Timer function. The remote temperature can be sensed by thermistors, or directly from Intel® / AMD™ CPU with thermal diode output. The W83793G provides 8 PWM (pulse width modulation) / DC fan output modes for smart fan control – "Thermal Cruise™" mode and "SMART FAN™ II" mode. In "Thermal Cruise™" mode, temperatures of CPU and the system can be maintained within specific programmable ranges under the hardware control. The W83793G, as SMART FAN™ II, provides 8 temperature sets, each of which can control the fan's duty cycle. With this design, the fan can work at the lowest possible speed to avoid acoustic noise. As for the warning mechanism, the W83793G provides SMI#, OVT#, IRQ, and BEEP signals for system protection events. The W83793G also has 2 specific pins to provide selectable address settings for the applications of multiple devices (up to 4 devices) wired through the I^2C interface.

The W83793G can serve as an ASF sensor to respond to ASF master's request for the implementation of network management in OS-absent status. With the W83793G's compliance with ASF2.0 sensor specification, the network server is able to monitor the system status of each client in OS-absent state by PET (Platform Event Trap) frame values returned from the W83793G, such as temperatures, voltages, fan speed and case open. Moreover, the W83793G supports SMBus 2.0 ARP command to solve the address conflict problems by dynamically assigning a new address for ASF Function after UDID is sent.

Through the application software or BIOS, users can read all the monitored parameters of the system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper/preset range. The application software could be Nuvoton's Hardware Doctor™ or other management application software. Besides, users can set the bounds (alarm thresholds) of these monitored parameters and activate corresponding maskable interrupts.

There is a feature reduced version of the W83793G available, W83793AG, which supports almost the same functions as those of W83793G, but removes 3 sets of thermal diode inputs (TD2 ~ TD4, Pin 31 ~ Pin 36), VcoreB input, and VIDB. The package of the W83793AG is the same as that of W83793G, which is 56-pin SSOP.

2. FEATURES

2.1 Monitoring Items

VOLTAGE

Monitoring 10 voltages (4 power pins – 5VSB, 5VDD, VBAT, Vtt, and 6 external pins – VcoreA, VcoreB, VSEN1~4). (W83793AG does not support Vcore B.)

TEMPERATURE

4 thermal diode (D+, D-) inputs, supporting Current Mode (dual current source) temperature measurement method. (W83793AG supports 1 thermal diode input only; TD2 ~ TD4 are removed in the W83793AG.)

2 thermistor inputs

Support Intel® PECI

FAN

8 DC/PWM fan outputs for fan speed control

8 fan speed inputs for monitoring (up to 12 by register setups)

SMART FAN™ -- controls the most fitting speed automatically by temperature.

CASEOPEN

CASEOPEN# detection input.

2.2 Address Resolution Protocol and Alert Standard Format

Support System Management Bus (SMBus) version 2.0 specification

Comply with hardware sensor slave ARP (Address Resolution Protocol)

Response ASF 2.0 command --- GetEventData, GetEventStatus, DeviceTypePoll

Comply with ASF 2.0 sensors (Monitoring fan speed, voltage, temperature, thermal trip and case open event/status)

Support Remote Control subset: Remote Power on/ Power off/ Reset.

2.3 Actions Enabling

Issue SMI#, OVT# signals to activate system protection

Issue BEEP signal to activate system speaker or buzzer

2.4 General

I^2C serial bus interface

Watch Dog Timer function with pin WDTRST# and SYSRST_IN.

2 pins (A0, A1) to provide selectable address settings for the application of multiple devices (up to 4 devices) wired together through the I^2C interface

5V operation

2.5 Package

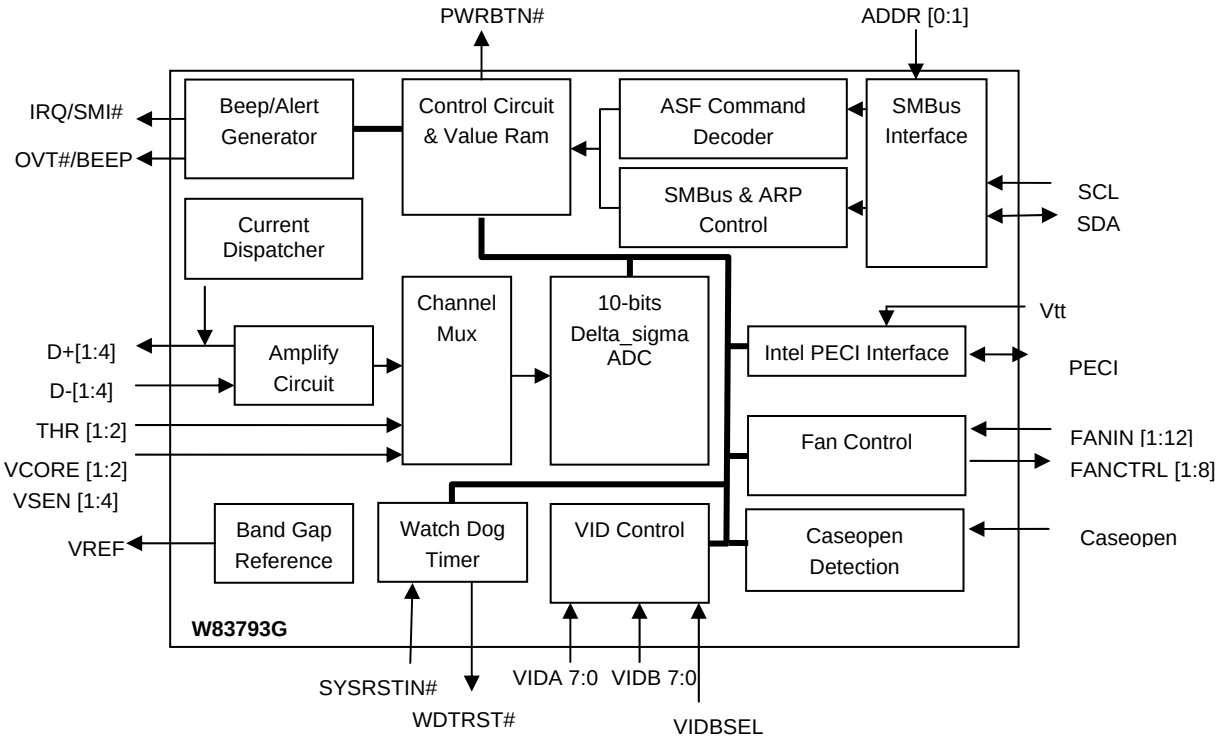
56 Pin SSOP 300mil. (For both W83793G and W83793AG)

3. KEY SPECIFICATIONS

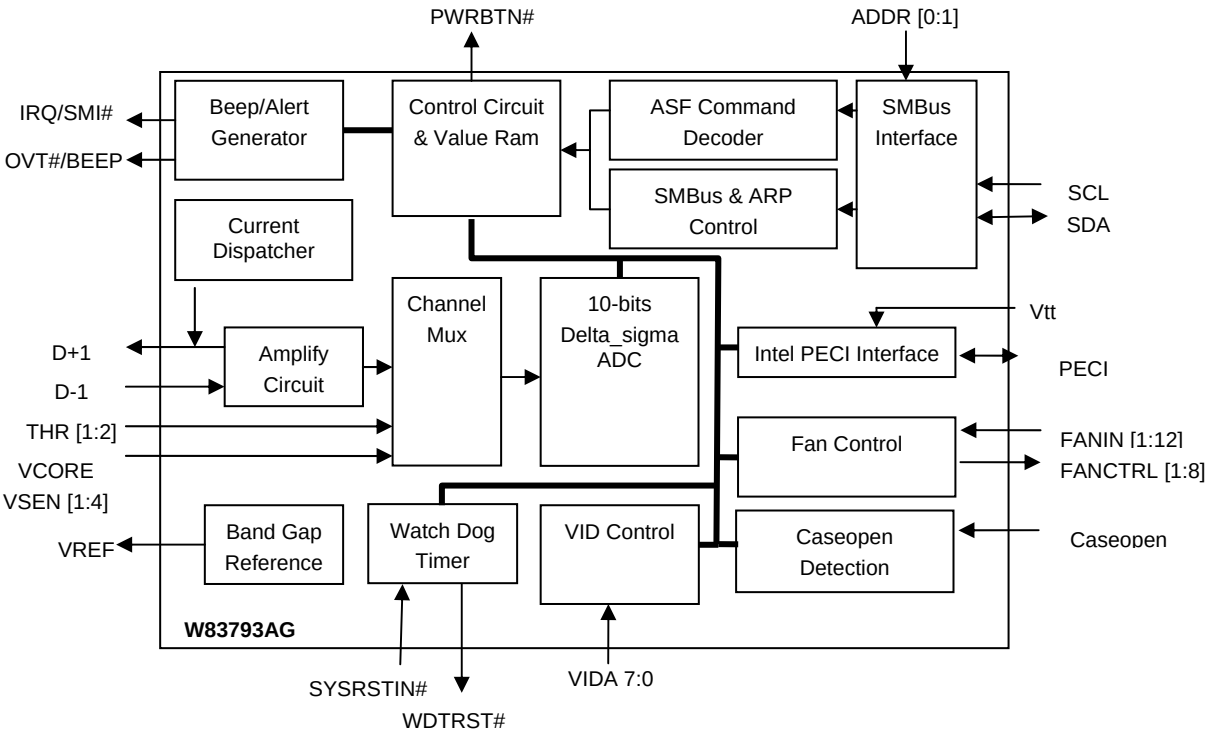
Voltage monitoring accuracy	±1%
● Temperature Sensor Accuracy	
Remote Diode Sensor Accuracy	± 1°C
Resolution	0.5 ℃
Supply Voltage (Pin 7, 5VSB)	5±0.25V
● Operating Supply Current	25 mA typ.
Current without 48MHz input at Pin 1	8 mA typ.
● ADC Resolution	10 Bits

4. BLOCK DIAGRAM

W83793G



W83793AG

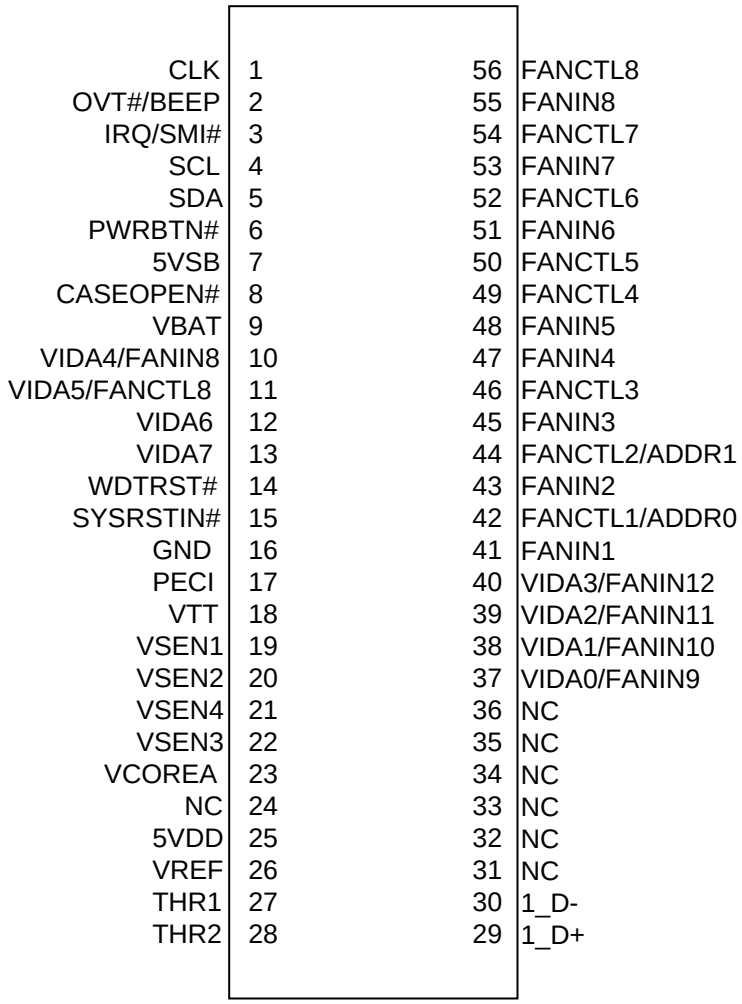

PWRBTN#
ADDR [0:1]
IRQ/SMI#
OVT#/BEEP
Beep/Alert Generator
Control Circuit & Value Ram
ASF Command Decoder
SMBus Interface
SMBus & ARP Control
SCL
SDA
Current Dispatcher
Channel Mux
10-bits Delta_sigma ADC
Vtt
D+1
D-1
Amplify Circuit
Intel PECI Interface
PECI
THR [1:2]
VCORE
VSEN [1:4]
Fan Control
FANIN [1:12]
FANCTRL [1:8]
VREF
Band Gap Reference
Watch Dog Timer
VID Control
Caseopen Detection
Caseopen
W83793AG
SYSRSTIN#
WDTRST#
VIDA 7:0

5. PIN CONFIGURATION

W83793G (56 SSOP)

CLK	1	56	VIDB7/FANCTL8
OVT#/BEEP	2	55	VIDB6/FANIN8
IRQ/SMI#	3	54	VIDB5/FANCTL7
SCL	4	53	VIDB4/FANIN7
SDA	5	52	VIDB3/FANCTL6
PWRBTN#	6	51	VIDB2/FANIN6
5VSB	7	50	VIDB1/FANCTL5
CASEOPEN#	8	49	VIDB0/FANCTL4
VBAT	9	48	FANIN5
VIDA4/FANIN8	10	47	FANIN4
VIDA5/FANCTL8	11	46	FANCTL3/VIDBSEL
VIDA6	12	45	FANIN3
VIDA7	13	44	FANCTL2/ADDR1
WDTRST#	14	43	FANIN2
SYSRSTIN#	15	42	FANCTL1/ADDR0
GND	16	41	FANIN1
PECI	17	40	VIDA3/FANIN12
VTT	18	39	VIDA2/FANIN11
VSEN1	19	38	VIDA1/FANIN10
VSEN2	20	37	VIDA0/FANIN9
VSEN4	21	36	4_D-
VSEN3	22	35	4_D+
VCOREA	23	34	3_D-
VCOREB	24	33	3_D+
5VDD	25	32	2_D-
VREF	26	31	2_D+
THR1	27	30	1_D-
THR2	28	29	1_D+

W83793AG (56 SSOP)



6. PIN DESCRIPTION

6.1 Pin Type Description

SYMBOL	DESCRIPTION
t	TTL level
v1	Vil/Vih=0.4/0.6 level
v2	Vil/Vih=0.8/1.4 level
v3	Vtt level
s	Schmitt trigger
12	12mA sink/source capability
OUT	Output pin
OD	Open-drain output pin
AOUT	Output pin (Analog)
IN	Input pin (digital)
AIN	Input pin(Analog)

6.2 Pin Description List

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
CLK	1	5VSB	IN_{ts}	48MHz System clock while 5VDD is powered up. PECI and the fan will use this clock to drive logics.
OVT#	2	5VSB	OD_{12}	Over temperature alert. Low active.
BEEP				BEEP output when any abnormal event occurs. If there is no abnormal event, this pin asserts low.
IRQ	3	5VSB	OUT_{12}	Interrupt request output when abnormal events occur.
SMI#			OD_{12}	System Management Interrupt (open drain).
SCL	4	5VSB	IN_{ts}	Serial Bus Clock.
SDA	5	5VSB	IN/OD_{12ts}	Serial Bus bi-directional data.

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
PWRBTN#	6	5VSB	OD_{12}	Power Button output signal to enable/ disable the power supply. This pin is related to ASF commands.
5VSB	7	-	POWER	This pin is the power source for the W83793G. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
CASEOPEN#	8	VBAT	IN_{ts}	CASE OPEN detection. An active low input from an external device when case is opened. This signal will be latched even when the case is closed.
VBAT	9		POWER	VBAT supplies power for CASEOPEN#. It is also a voltage monitor channel.
VIDA4	10	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 4 from CPU A. (Default)
FANIN8			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA5	11	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 5 from CPU A. (Default)
FANCTL8			OUT / OD_{12a}	FAN control output. The 8th fan control signal can be programmed to output through pin 56 or this pin. When this pin is programmed to be fan control signal, it only supports the PWM mode.
FANIN12			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA6	12	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 6 from CPU A.
VIDA7	13	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 7 from CPU A. (Default)
WDTRST#	14	5VSB	OD_{12}	Low active system reset. If triggered, this pin will send out 100ms low pulse for system reset.
SYSRSTIN#	15	5VSB	IN_{ts}	System reset input, used to control WDT.
GND	16		POWER	System Ground.
PECI	17	5VSB	IN/O_{V3}	Intel® CPU PECI interface
VTT	18		POWER	Intel® CPU Vtt power

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VSEN1	19		AIN	Voltage sensor input. The detection range is 0~4.096V
VSEN2	20		AIN	Voltage sensor input. The detection range is 0~4.096V
VSEN4	21	-	AIN	Voltage sensor input. The detection range is 0~2.048V.
VSEN3	22		AIN	Voltage sensor input. The detection range is 0~4.096V.
VCOREA	23		AIN	CPU A core voltage input. The detection range is 0~2.048V
VCOREB*	24		AIN	CPU B Core Voltage Input. The detection range is 0~2.048V.
5VDD	25	-	POWER	+5V VDD power. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
VREF	26		AOUT	Reference voltage output.
THR1	27		AIN	Thermistor 1 terminal input.
THR2	28		AIN	Thermistor 2 terminal input.
1_D+	29		AIN	Thermal diode 1 D+.
1_D-	30		AIN	Thermal diode 1 D-.
2_D+*	31		AIN	Thermal diode 2 D+.
2_D-*	32		AIN	Thermal diode 2 D-.
3_D+*	33		AIN	Thermal diode 3 D+.
3_D-*	34		AIN	Thermal diode 3 D-.
4_D+*	35		AIN	Thermal diode 4 D+.
4_D-*	36		AIN	Thermal diode 4 D-.
VIDA0	37	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 0 from CPU A. (Default)

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
FANIN9			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA1	38	5VSB	IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 1 from CPU A. (Default)
FANIN10			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA2	39	5VSB	IN_{v1s}	Voltage Supply readouts bit 2 from CPU A. (Default)
FANIN11			IN_{ts}	0V to +5V amplitude fan tachometer input
VIDA3	40	5VSB	IN_{v1s}	Voltage Supply readouts bit 3 from CPU A. (Default)
FANIN12			IN_{ts}	0V to +5V amplitude fan tachometer input
FANIN1	41	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANCTL1	42	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
ADDR0			IN_{ts}	I^2C device address bit 0 trapping during 5VSB power on.
FANIN2	43	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANCTL2	44	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
ADDR1			IN_{ts}	I^2C device address bit 1 trapping during 5VSB power on.
FANIN3	45	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANCTL3	46	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VIDBSEL**			IN_{ts}	The pin straps the fan mode and VID mode during 5VSB power on. When strapped to high, it will select VID mode. When strapped to low, it will select Fan mode for pin49~56.
FANIN4	47	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANIN5	48	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
FANCTL4	49	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
VIDB0*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 0 from CPU B.
FANCTL5	50	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
VIDB1*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 1 from CPU B.
FANIN9			INts	0V to +5V amplitude fan tachometer input
FANIN6	51	5VSB	INts	0V to +5V amplitude fan tachometer input
VIDB2*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 2 from CPU B.
FANCTL6	52	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
FANIN10			INts	0V to +5V amplitude fan tachometer input
VIDB3*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 3 from CPU B.
FANIN7	53	5VSB	INts	0V to +5V amplitude fan tachometer input

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VIDB4*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 4 from CPU B.
FANCTL7	54	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
FANIN11			INts	0V to +5V amplitude fan tachometer input
VIDB5*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 5 from CPU B.
FANIN8	55	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
VIDB6*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 6 from CPU B.
FANCTL8	56	5VSB	OUT / OD_{12} / AOUT	Fan speed control PWM/DC output. The 8^{th} fan control signal can be programmed to output through pin 11 or this pin. When the power of 5VDD is 0V, this pin will drive logic 0. The power of this pin is supplied by 5VSB. As DC output, 64 steps output voltage scaled from 0 to 5VSB.
VIDB7*			IN_{v1s} or IN_{v2s}	Voltage Supply readouts bit 7 from CPU B.

Pins with * are for the W83793G only, not for the W83793AG.

Pins with ** are for the W83793G only. Please always strap low to select FANIN or FANCTL for the W83793AG.

7. FUNCTIONAL DESCRIPTION

This section is blank now. Refer to Chap 8 for function description.

8. CONFIGURATION REGISTERS

8.1 ID, Bank Select Registers

Inside the W83793G resides three banks of registers. Customers must set the banks correctly to access correct registers. All the registers described here can be accessed in all banks.

8.1.1 ID, Bank Select Registers Map

Address 00_{HEX}, $0D_{HEX}$, $0E_{HEX}$, $0F_{HEX}$ in all three register banks are reserved as ID and Bank Select registers.

Mnemonic	Register Name	Type
BankSel.	Bank Select	RW
VendorID.	Nuvoton Vendor ID	RO
ChipID.	Nuvoton Chip ID	RO
DeviceID.	Nuvoton Device Version ID	RO

8.1.2 ID, Bank Select Register Details

8.1.2.1. Bank Select Register (Bank Select)

Three banks of registers are inside the W83793G. The register bank could be selected by programming the Bank Select register. All 00_{HEX} Addresses in these three banks are defined as Bank Select register.

Location: Bank 0, 1, 2 Address 00_{HEX}
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

BANKSELECT

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	Reserve				BANK Select		
RESET	1	0_{HEX}				0_{HEX}		

BIT	DESCRIPTION
7	**HBACS** (High Byte Access) 0: Return the low byte while reading Nuvoton Vendor ID. 1: Return the high byte while reading Nuvoton Vendor ID.
6-3	Reserved.
2-0	BANK Select. 000_{BIN}: Bank 0 is selected. 001_{BIN}: Bank 1 is selected. 010_{BIN}: Bank 2 is selected.

8.1.2.2. Nuvoton Vendor ID Register (Vender ID)

The Nuvoton Vendor ID contains two-byte data. By programming register **HBACS**, the customer can choose to access either the high or the low byte of Nuvoton Vendor ID.

Location: Bank 0, 1, 2 Address $0D_{HEX}$
Type: Read Only
Reset: No Reset

VENDORID (NUVOTON VENDOR ID)

BIT	7	6	5	4	3	2	1	0
NAME	VendorID							

FIXED	$5C_{HEX}$ / $A3_{HEX}$

BIT	DESCRIPTION
7-0	VendorID. Return $5C_{HEX}$ if **HBACS** = 1; return $A3_{HEX}$ if **HBACS** = 0.

8.1.2.3. Nuvoton Chip ID Register (ChipID)

Location: Bank 0, 1, 2 Address $0E_{HEX}$
Type: Read Only
Reset: No Reset

CHIPID (NUVOTON CHIP ID)

BIT	7	6	5	4	3	2	1	0
NAME	**ChipID**							
RESET	$7B_{HEX}$							

BIT	DESCRIPTION
7-0	ChipID. Chip ID of W83793G is $7B_{HEX}$

8.1.2.4. Nuvoton Version ID Register (Device ID)

Location: Bank 0, 1, 2 Address $0F_{HEX}$
Type: Read Only
Reset: No Reset

VERSION ID

BIT	7	6	5	4	3	2	1	0
NAME	DeviceID							
FIXED	11_{HEX} /12_{HEX}							

BIT	DESCRIPTION
7-0	Version ID. Device ID of the W83793G. 11_{HEX} for B Version, and 12_{HEX} for C Version.

8.2 Watch Dog Timer Registers

The W83793G is integrated with a Watch Dog Timer, which enables users to reset the system by Pin 14 while the system is in an abnormal state. Once Watch Dog Timer is enabled, the W83793G starts to count down, and the host should set the timer for further count down or clear/disable the timer to prevent the W83793G from issuing reset signals.

8.2.1 Watch Dog Timer Registers Map

Watch Dog Timer consists of four registers. WDTLock and ENABLE_WDT are used to activate Soft-WDT and Hard-WDT, respectively. WDT_STS and DownCounter can inform the host whether the system time is up or not.

Mnemonic	Register Name	Type
WDTLock.	Lock Watch Dog	WO
EnableWDT.	Watch Dog Enable	RO
WDT_STS.	Watch Dog Status	R/W
DownCounter.	Watch Dog Timer	R/W

Two kinds of watchdog timer functions are supported by the W83793G. One is so-called Soft Watch Dog Timer, and the other is Hard Watch Dog Timer.

Hard Watch Dog timer, if enabled, will start a 4-minute WDT after the system reset is completed. (A low-to-high transition on SYSRSTIN# pin). BIOS needs to write a 00_{HEX} into Watch Dog Timer Register (04_{HEX}) to disable the timer within 4 minutes. Otherwise, Pin 14 WDTRST# will assert to reset the system.

Soft Watch Dog Timer will start counting down whenever Timeout Time is set and Soft Watch Dog Timer is enabled. WDTRST# will be issued when the time runs out.

Soft Watch Dog Timer will be disabled automatically after receiving a SYSRSTIN_N low signal.

Bank0, CR40 [2]/**ENWDT** must be set to 1 if wish to program the four Watch Dog Timer Registers.

8.2.2 Watch Dog Timer Register Details

8.2.2.1. Lock Watch Dog Register (WDT Lock)

Writing this register enables the Soft or Hard Watch Dog Timer. This register type is write only and ENABLE_WDT confirms whether the write is successful.

Location: Bank 0 Address 01_{HEX}
Type: Write Only
Reset: VSB5V (Pin 7) Rising,
SYSRSTIN_N (Pin 15) Falling in Soft WDT mode.

WDTLOCK (WATCH DOG TIMER LOCK)

Bit	7	6	5	4	3	2	1	0
Name	**UNLOCK CODE**							

Bit	Description
7-0	Unlock Code. Write 55_{HEX}, Enables Soft Watch Dog Timer. Write AA_{HEX}, Disables Soft Watch Dog Timer. Write 33_{HEX}, Enables Hard Watch Dog Timer. Write CC_{HEX}, Disables Hard Watch Dog Timer.

8.2.2.2. Watch Dog Enable Register (Enable WDT)

Location: Bank 0 Address 02_{HEX}
Type: Read Only
Reset: VSB5V (Pin 7) Rising.

ENABLE WDT (WATCH DOG TIMER ENABLE STATUS)

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**						**HARD**	**SOFT**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-2	Reserved
1	HARD. 1: Hard Watch Dog is enabled. 0: Hard Watch Dog is disabled.
0	SOFT. 1: Soft Watch Dog is enabled. 0: Soft Watch Dog is disabled.

8.2.2.3. Watch Dog Status Register

Location: Bank 0 Address 03_{HEX}
Type: Read / Write
Reset: VSB5V (Pin 7) Rising.

WDT_STS (WATCH DOG STATUS)

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**				**WDT STAGE**		**HARD_TO**	**SOFT_TO**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	Reserved
3-2	WDT Stage. These 2 bits record last WDT stage for BIOS readout. The information is used to help BIOS to identify WDT timeout issuance.
1	HARD_TO. 1: A hard timeout occurs. This bit will be cleared after reading.
0	SOFT_TO. 1: A soft timeout occurs. This bit will be cleared after reading.

8.2.2.4. Watch Dog Timer Register (Down Counter)

Location: Bank 0 Address 04_{HEX}
Type: Read / Write
Reset: VSB5V (Pin 7) Rising.

DOWN COUNTER (WATCH DOG TIMER)

Bit	7	6	5	4	3	2	1	0
Name	**Timeout Time**							
Reset	00_{HEX}							

Bit	Description
7-0	Timeout Time. To write 00_{HEX} can disable the timer while in Hard Watch Dog Timer mode. To set Timeout Time for SOFT Watch Dog Timer, the unit is minute.

Timeout Time is unit in minutes. 0 represents time is up or the timer is cleared. 1 represents there is still 1 second to 1 minute time for this timer. Similarly, 2 means there is still 1 minute 1 second to 2 minutes left.

8.3 Configuration and Address Select Registers

8.3.1 Register Maps

Mnemonic	Register Name	Type
I2CADDR	I²C Address	R/W
TEMPD1/2ADDR	LM75 Temperature Sensor I²C Address	R/W

8.3.1.1. I²C Address Registers Map

There are four Addresses (58_{HEX}, $5A_{HEX}$, $5C_{HEX}$, $5E_{HEX}$) that can be assigned for the I²C interface. Four I²C Addresses for each LM75-like Temperature Sensor (90_{HEX}, 92_{HEX}, 94_{HEX}, 96_{HEX} for TD1 and 98_{HEX}, $9A_{HEX}$, $9C_{HEX}$, $9E_{HEX}$ for TD2) are also provided. These four addresses can be set by strapping pin 42 & 44 input value at 100ms after power ready.

The registers for Temperature sensor D1 & D2 can also be accessed by respective addresses that are set as I²C address of the W83793G. The default of this LM75-like function is enabled and can be disabled by setting bit 3 and bit 7 of TEMPD1/2ADDR to 1.

8.3.1.2. Configuration Register Maps

Mnemonic	Register Name	Type
CONFIG	Configuration Register	R/W

Configuration Register controls the system reset source, stop, power down and warning output mode.

8.3.2 Register Details

8.3.2.1. I^2C Address Register (I2CADDR)

Location: Bank 0 Address $0B_{HEX}$
Type: Read Only
Reset: 100ms after VSB5V (Pin 7) Rising.

I2CADDR

Bit	7	6	5	4	3	2	1	0
Name	**SMBUSADDR**							

Bit	Description
7-0	SMBUSADDR. The value of **SMBUSADDR** is the strapping pin voltage on PADDR0 (pin42) and PADDR1 (pin44) at 100ms after VSB power ready.

ADDR1	ADDR0	I^2C Address
0	0	58_{HEX}
0	1	$5A_{HEX}$
1	0	$5C_{HEX}$
1	1	$5E_{HEX}$

8.3.2.2. LM75-like Temperature Sensor I^2C Address Register

Location: Bank 0 Address $0C_{HEX}$
Type: Read / Write
Reset: 100ms after VSB5V (Pin 7) Rising.

TEMPD1/2ADDR

Bit	7	6	5	4	3	2	1	0
Name	**DIS_TD2**	**I2CADDR75B**			**DIS_TD1**	**I2CADDR75A**		
Reset	0	Trapped Value			0	Trapped Value		

Bit	Description
7	DIS_TD2. If set to 1, temperature sensor 2 cannot be accessed by temperature sensor 2 I2C address.
6-4	I2CADDR75B. The value of I2CADDR75B is obtained by strapping PADDR0 (pin42) and PADDR1 (pin44) at 100ms after valid VSB power is issued.

Bit	Description
	<table><tr><th>ADDR1</th><th>ADDR0</th><th>I2CADDR75B</th><th>Temperature sensor 2 I2C Address</th></tr><tr><td>0</td><td>0</td><td>100</td><td>98_{HEX}</td></tr><tr><td>0</td><td>1</td><td>101</td><td>$9A_{HEX}$</td></tr><tr><td>1</td><td>0</td><td>110</td><td>$9C_{HEX}$</td></tr><tr><td>1</td><td>1</td><td>111</td><td>$9E_{HEX}$</td></tr></table>
3	DIS_TD1. If set to 1, it cannot access the registers for temperature sensor 1 by temperature sensor 1 I2C address.
2-0	I2CADDR75A. The value of I2CADDR75B is obtained by strapping PADDR0 (pin42) and PADDR1 (pin44) at 100ms after valid VSB power is issued. <table><tr><th>ADDR1</th><th>ADDR0</th><th>I2CADDR75A</th><th>Temperature sensor 1 I2C Address</th></tr><tr><td>0</td><td>0</td><td>000</td><td>90_{HEX}</td></tr><tr><td>0</td><td>1</td><td>001</td><td>92_{HEX}</td></tr><tr><td>1</td><td>0</td><td>010</td><td>94_{HEX}</td></tr><tr><td>1</td><td>1</td><td>011</td><td>96_{HEX}</td></tr></table>

8.3.2.3. Configuration Register

Location: Bank 0 Address 40_{HEX}
Type: Read / Write
Reset: bit 0~3 & 7:
VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.
Bit 4 & 5:
VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set.

CONFIG

Bit	7	6	5	4	3	2	1	0
Name	**INIT**	**Reserve**	**SYSRST_MD**	**RST_VDD_MD**	**EN_BAT_MNT**	**EN_WDT**	**INT_Clear**	**START**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	INIT. Setting to one restores power-on default values to all registers, except the Serial Bus Address register. This bit clears itself since the power-on default is zero.
6	Reserved

Bit	Description
5	SYSRST_MD. Write 1, the whole chip will be reset when the SYSRSTIN# input signal is issued. Write 0, no operation when the SYSRSTIN# input signal is issued.
4	RST_VDD_MD. Write 1, the whole chip will be reset when 5VDD is up. Write 0, no operation when 5VDD is up.
3	EN_BAT_MNT. Write 1; battery voltage monitor is enabled. Write 0; battery voltage monitor is disabled. If enable this bit, the monitor value is valid after one monitor cycle.
2	EN_WDT. Setting this bit to 1 will enable the Watch Dog Timer function, which resets the system (pin 47) while the time is out.
1	INT_Clear. A one disables the SMI# and IRQ# outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring at last channel. It will resume upon clearing of this bit.
0	START. 1: Enables startup of monitoring operations; 0: Puts the analog part in the Power-down mode.

8.4 VID Control/Status Registers

The W83793G provides dual Vcore monitoring channels. Vcore Channels are automatically monitored once 5VSB is applied onto the W83793G, but the W83793G will issue alert information only when the corresponding high/low limits of Vcore channels are being violated. ASF is also based on these limit registers to judge the current channel status and report to the host.

Two methods are used to assign the Vcore Limits, manually or automatically by VID inputs. The following register sets allow users to choose their preferred method.

Please be noted that VIDB are for the W83793G only; the W83793AG does not support VIDB.

8.4.1 VID Control/Status Registers Map

Mnemonic	Register Name	Type
VIDIN_A	VIDA Input Value	RO
VIDIN_B	VIDB Input Value	RO
VIDA_Latch	VIDA Latch Value	RO
VIDB_Latch	VIDB Latch Value	RO
VID_Control	VID Control	R/W
VCORE_LIMHI	Vcore High Tolerance	R/W
VCORE_LIMLO	Vcore Low Tolerance	R/W

The W83793G supplies two sets of VID input pins for VOCREA and VCOREB channels. If dynamic VID function is enabled, the high/low limit of VCOREA and VCOREB channel will auto-update when the VID input value changes.

Some VIDA and all VIDB input pins are multi-function pin. Programming Multi-function Pin Control Registers at Bank0, CR58h properly is required to make these pins function.

8.4.2 VID Register Details

8.4.2.1. VIDA Input Value Register (VIDIN_A)

Location: Bank 0 Address 05_{HEX}
Type: Read Only

VIDIN_A

Bit	7	6	5	4	3	2	1	0
Name	**VIDAIN7**	**VIDAIN6**	**VIDAIN5**	**VIDAIN4**	**VIDAIN3**	**VIDAIN2**	**VIDAIN1**	**VIDAIN0**

Bit	Description
7	VIDAIN7. Real time pin 13 input value. This is available for VRM11 only.
6	VIDAIN6. Real time pin 12 input value. This is available for VRM10 and VRM11 only.
5	VIDAIN5. Real time pin 11 input value. This is available for VRM10, VRM11 and AMD Opteron™ 6-bit VID only.
4	VIDAIN4. Real time pin 10 input value.
3	VIDAIN3. Real time pin 40 input value.
2	VIDAIN2. Real time pin 39 input value.
1	VIDAIN1. Real time pin 38 input value.
0	VIDAIN0. Real time pin 37 input value.

8.4.2.2. VIDB Input Value Register (VIDIN_B)

Location: Bank 0 Address 06_{HEX}
Type: Read Only

VIDIN_B

Bit	7	6	5	4	3	2	1	0
Name	**VIDBIN7**	**VIDBIN6**	**VIDBIN5**	**VIDBIN4**	**VIDBIN3**	**VIDBIN2**	**VIDBIN1**	**VIDBIN0**

Bit	Description

Bit	Description
7	VIDBIN7. Real time pin 56 input value. This is available for VRM11 only.
6	VIDBIN6. Real time pin 55 input value. This is available for VRM10 and VRM11 only.
5	VIDBIN5. Real time pin 54 input value. This is available for VRM10, VRM11 and AMD Opteron™ 6-bit VID only.
4	VIDBIN4. Real time pin 53 input value.
3	VIDBIN3. Real time pin 52 input value.
2	VIDBIN2. Real time pin 51 input value.
1	VIDBIN1. Real time pin 50 input value.
0	VIDBIN0. Real time pin 49 input value.

8.4.2.3. VIDA Latch Value Register (VIDA_Latch)

Previous **VIDIN_A** and **VIDIN_B** allow users to read the current value on VID pins, but VIDA_Latch and VIDB_Latch allow users to keep the VID value at any time by assigning the **Latch_VIDA/Latch_VIDB** bits to 1.

Location: Bank 0 Address 07_{HEX}
Type: Read Only

VIDA_LATCH

Bit	7	6	5	4	3	2	1	0
Name	**VIDA7**	**VIDA6**	**VIDA5**	**VIDA4**	**VIDA3**	**VIDA2**	**VIDA1**	**VIDA0**

Bit	Description
7	VIDA7. Reading this bit returns VIDA7 register value if Latch_VIDA is set to 1. Otherwise, the pin value of VIDAIN7 is returned.
6	VIDA6. Reading this bit returns VIDA6 register value if Latch_VIDA is set to 1. Otherwise, the pin value of VIDAIN6 is returned.
5	VIDA5. Reading this bit returns VIDA5 register value if Latch_VIDA is set to 1. Otherwise, the pin value of VIDAIN5 is returned.
4	VIDA4.

Bit	Description
	Reading this bit eturns VIDA4 register value if Latch_VIDA is set to 1. Otherwise, the pin value of VIDAIN4 is returned.
3	VIDA3. Reading this bit returns VIDA3 register value if Latch_VIDA is set to 1. Otherwise, the pin value of VIDAIN3 is returned.
2	VIDA2. Reading this bit returns VIDA2 register value if Latch_VIDA is set to 1. Otherwise, the pin value of VIDAIN2 is returned.
1	VIDA1. Reading this bit returns VIDA1 register value if Latch_VIDA is set to 1. Otherwise, the pin value of VIDAIN1 is returned.
0	VIDA0. Reading this bit returns VIDA0 register value if Latch_VIDA is set to 1. Otherwise, the pin value of VIDAIN0 is returned.

8.4.2.4. VIDB Latch Value Register (VIDB_Latch)

Location: Bank 0 Address 08_{HEX}
Type: Read Only

VIDB_LATCH

Bit	7	6	5	4	3	2	1	0
Name	**VIDB7**	**VIDB6**	**VIDB5**	**VIDB4**	**VIDB3**	**VIDB2**	**VIDB1**	**VIDB0**

Bit	Description
7	VIDB7. Reading this bit returns VIDB7 register value if Latch_VIDB is set to 1. Otherwise, the pin value of VIDBIN7 is returned.
6	VIDB6. Reading this bit returns VIDB6 register value if Latch_VIDB is set to 1. Otherwise, the pin value of VIDBIN6 is returned.
5	VIDB5. Reading this bit returns VIDB5 register value if Latch_VIDB is set to 1. Otherwise, the pin value of VIDBIN5 is returned.
4	VIDB4. Reading this bit returns VIDB4 register value if Latch_VIDB is set to 1. Otherwise, the pin value of VIDBIN4 is returned.
3	VIDB3. Reading this bit returns VIDB3 register value if Latch_VIDB is set to 1. Otherwise, the pin value of VIDBIN3 is returned.
2	VIDB2. Reading this bit returns VIDB2 register value if Latch_VIDB is set to 1. Otherwise,

Bit	Description
	the pin value of VIDBIN2 is returned.
1	VIDB1. Reading this bit returns VIDB1 register value if Latch_VIDB is set to 1. Otherwise, the pin value of VIDBIN1 is returned.
0	VIDB0. Reading this bit returns VIDB0 register value if Latch_VIDB is set to 1. Otherwise, the pin value of VIDBIN0 is returned.

8.4.2.5. VID Control Register (VID_Control)

Location: Bank 0 Address 59_{HEX}
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

VID_CONTROL

Bit	7	6	5	4	3	2	1	0
Name	**Level_Select**		**EN_DVID**	**Latch_VIDB**	**Latch_VIDA**	**VID_SEL**		
Reset	00_{BIN}		0	0	0	001_{BIN}		

Bit	Description
7-6	Level_Select. Set VID input pin V_{IH}/V_{IL} level 00_{BIN} : 0.6V/0.4 for VRM10, 11 01_{BIN} : 1.6V/0.8V for AMD VID 10_{BIN} : 2.0V/0.8V 11_{BIN} :.Reserved.
5	EN_DVID. Writing 1 enables the dynamic VID function. If VID is changed, the high/low limit of corresponding Vcore sensing voltage will be auto-updated. If manually programming High/Low limit of Vcore sensing voltage is required, this bit has to be cleared as 0.
4	Latch_VIDB. If write 1, CR08 latches the current pin value of VIDB.
3	Latch_VIDA. If write 1, CR07 latches the current pin value of VIDA.
2-0	VID_SEL. Selectable VID tables: 000_{BIN} : Reserved

Bit	Description
	001_{BIN} : VRM10 (default) 010_{BIN} : VRM11 011_{BIN} : AMD Opteron™ 5 bit VID Codes 100_{BIN} : AMD Opteron™ 6 bit VID Codes

8.4.2.6. Vcore High Tolerance Register (VCORE_LIMHI)

Location: Bank 0 Address 09_{HEX}
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

VCORE_LIMHI

Bit	7	6	5	4	3	2	1	0
Name	**Vcore High Tolerance**							
Reset	64_{HEX}							

Bit	Description
7-0	Vcore High Tolerance. If the dynamic VID function (set Bank0 CR59 bit5 to 1) is enabled, writing Tolerance register will force VCORE Limit to update with new voltage limits for VCORE. The unit is 2mV

8.4.2.7. Vcore Low Tolerance Register (VCORE_LIMLO)

Location: Bank 0 Address $0A_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

VCORE_LIMLO

Bit	7	6	5	4	3	2	1	0
Name	**Vcore Low Tolerance**							
Reset	64_{HEX}							

Bit	Description
7-0	Vcore Low Tolerance. If the dynamic VID function (set Bank0 CR59 bit5 to 1) is enabled, writing Tolerance register will force VCORE Limit Generator to generate new voltage limits for VCORE. The unit is 2mV

8.5 INT/SMI# Control/Status Registers

Several mechanisms are provided to alarm the system when monitored channels are abnormal. In this paragraph, three kinds of control/status registers are introduced. “Real time status” shows the current status of each channel; “Channel Mask” defines which channel needs to issue warning when abnormal operation occurs, and when the warning should be ignored due to floating or in other circumstances. The final one is “Interrupt Status,” which gives the host information of which channel is issuing alert, and the host can base on this channel and do proper process to ensure a reliable system.

8.5.1 INT/SMI Control/Status Register Map

Mnemonic	Register Name	Type
INT_STS1 INT_STS5	Interrupt Status 1 Interrupt Status 5	RO
MASK1 MASK5	SMI/IRQ Mask 1 SMI/IRQ Mask 5	R/W
REAL_STS1 REAL_STS5	Real Time status 1 Real Time status 5	RO
SMIINT_Ctrl	SMI/IRQ Control	R/W

Pin 3 of the W83793G is a multi-function pin. It can be the IRQ output or the SMI# output signal. The function is selected by programming Bank0 CR50 SMI/IRQ Control register.

The interrupt mode for voltage and FANIN is only two-time interrupt mode.

For temperature, there are three modes to serve: <1> Comparator mode, <2>One-Time Interrupt mode, and <3> Two-Time Interrupt mode.

8.5.2 INT/SMI Control/Status Register Details

8.5.2.1. Interrupt Status Register (INT_STS)

A one represents corresponding channel have been exceed its limit. Read Interrupt Status will clear the interrupt flag.

VIDCHG will assert if VID has a change during last 1ms.

TART will assert while target temperature cannot be achieved after 3 minutes full speed of corresponding FAN.

Location:

INT_STS1 - Bank 0 Address 41_{HEX}
INT_STS2 - Bank 0 Address 42_{HEX}
INT_STS3 - Bank 0 Address 43_{HEX}
INT_STS4 - Bank 0 Address 44_{HEX}
INT_STS5 - Bank 0 Address 45_{HEX}

Type: Read Only
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

INT_STS1

Bit	7	6	5	4	3	2	1	0
Name	**VSEN4**	**VSEN3**	**VSEN2**	**VSEN1**	**Reserve**	**VTT**	**VCOREB**	**VCOREA**
Reset	0	0	0	0	0	0	0	0

INT_STS2

Bit	7	6	5	4	3	2	1	0
Name	**TD4**	**TD3**	**TD2**	**TD1**	**VIDCHG**	**VBAT**	**5VSB**	**5VDD**
Reset	0	0	0	0	0	0	0	0

INT_STS3

Bit	7	6	5	4	3	2	1	0
Name	**FANIN6**	**FANIN5**	**FANIN4**	**FANIN3**	**FANIN2**	**FANIN1**	**TR2**	**TR1**
Reset	0	0	0	0	0	0	0	0

INT_STS4

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**	**Chassis**	**FANIN12**	**FANIN11**	**FANIN10**	**FANIN9**	**FANIN8**	**FANIN7**
Reset	0	0	0	0	0	0	0	0

INT_STS5

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**TART6**	**TART5**	**TART4**	**TART3**	**TART2**	**TART1**
Reset	0	0	0	0	0	0	0	0

8.5.2.2. SMI/IRM Mask Register (MASK)

Setting to one will disable the corresponding interrupt sources. Clearing to 0 will enable that interrupt source.

SMI Mask4 bit 7 is CLR_CHS (Clear Chassis), writing this bit to one will clear the internal caseopen latch. After the latch is cleared, CLR_CHS will self-reset to 0.

Location:

MASK1 - Bank 0 Address 46_{HEX}
MASK2 - Bank 0 Address 47_{HEX}
MASK3 - Bank 0 Address 48_{HEX}
MASK4 - Bank 0 Address 49_{HEX}
MASK5 - Bank 0 Address $4A_{HEX}$

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

MASK1

Bit	7	6	5	4	3	2	1	0
Name	**VSEN4**	**VSEN3**	**VSEN2**	**VSEN1**	**Reserve**	**VTT**	**VCOREB**	**VCOREA**
Reset	0	0	0	0	0	0	0	0

MASK2

Bit	7	6	5	4	3	2	1	0
Name	**TD4**	**TD3**	**TD2**	**TD1**	**VIDCHG**	**VBAT**	**5VSB**	**5VDD**
Reset	0	0	0	0	0	0	0	0

MASK3

Bit	7	6	5	4	3	2	1	0
Name	**FANIN6**	**FANIN5**	**FANIN4**	**FANIN3**	**FANIN2**	**FANIN1**	**TR2**	**TR1**
Reset	0	0	0	0	0	0	0	0

MASK4

Bit	7	6	5	4	3	2	1	0
Name	**CLR_CHS**	**Chassis**	**FANIN12**	**FANIN11**	**FANIN10**	**FANIN9**	**FANIN8**	**FANIN7**
Reset	0	0	0	0	0	0	0	0

MASK5

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**TART6**	**TART5**	**TART4**	**TART3**	**TART2**	**TART1**
Reset	0	0	0	0	0	0	0	0

8.5.2.3. Real Time status Register (REAL_STS)

Real-time status registers show whether the values of related channels exceed the limit or not at the polling moment. The returning of 1 indicates the limit of related channel defined in limit registers has been exceeded.

Location:

REAL_STS1 - Bank 0 Address $4B_{HEX}$
REAL_STS2 - Bank 0 Address $4C_{HEX}$
REAL_STS3 - Bank 0 Address $4D_{HEX}$
REAL_STS4 - Bank 0 Address $4E_{HEX}$
REAL_STS5 - Bank 0 Address $4F_{HEX}$

Type: Read Only

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

REAL_STS1

Bit	7	6	5	4	3	2	1	0
Name	**VSEN4**	**VSEN3**	**VSEN2**	**VSEN1**	**Reserve**	**VTT**	**VCOREB**	**VCOREA**
Reset	0	0	0	0	0	0	0	0

REAL_STS2

Bit	7	6	5	4	3	2	1	0
Name	**TD4**	**TD3**	**TD2**	**TD1**	**VIDCHG**	**VBAT**	**5VSB**	**5VDD**
Reset	0	0	0	0	0	0	0	0

REAL_STS3

Bit	7	6	5	4	3	2	1	0
Name	**FANIN6**	**FANIN5**	**FANIN4**	**FANIN3**	**FANIN2**	**FANIN1**	**TR2**	**TR1**
Reset	0	0	0	0	0	0	0	0

REAL_STS4

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**	**Chassis**	**FANIN12**	**FANIN11**	**FANIN10**	**FANIN9**	**FANIN8**	**FANIN7**
Reset	0	0	0	0	0	0	0	0

REAL_STS5

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**TART6**	**TART5**	**TART4**	**TART3**	**TART2**	**TART1**
Reset	0	0	0	0	0	0	0	0

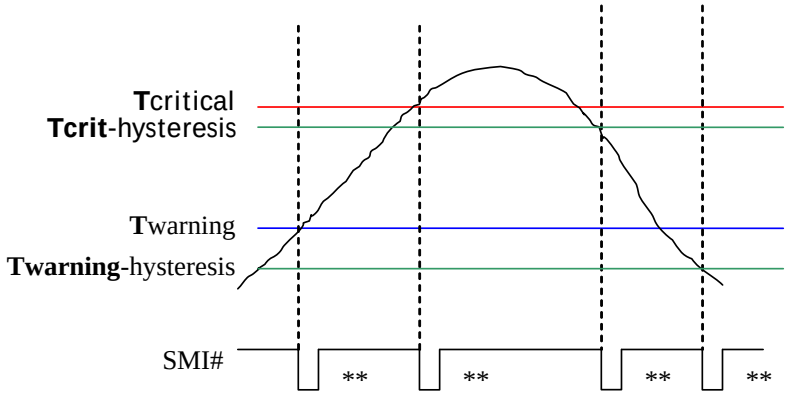
8.5.2.4. SMI/IRQ Control Register (SMIINT_Ctrl)

Location: Bank 0 Address 50_{HEX}
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

SMIINT_CTRL

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**IRQ_MD**	**IRQSEL**	**TEMP_SMI_MD**		**EN_IRQSMI**	**POL**
Reset	0	0	0	1	0	0	0	0

Bit	Description
7-6	Reserved.
5	IRQ_MD. If set to 0, the bit outputs IRQ output level signal. If set to 1, the bit outputs 200 us pulse signal. The default value is 0.
4	IRQ_SEL. Set Pin 3 to the IRQ mode. While this bit is set to 1 and EN_IRQSMI is set to 1, Pin 3 is enabled with IRQ interrupt output.
3-2	TEMP_SMI_MD. Temperature SMI# Mode Select. 00_{BIN} : Comparator Interrupt Mode:(Default) Temperature TD1/TD2/TD3/TD4/TR1/TR2 exceeding T_O (Critical temperature) limit causes an interrupt and this interrupt will be cleared by reading all the Interrupt Status. 01_{BIN} : Two Time Interrupt Mode:

Bit	Description
	Temperature sensors TD1/TD2/TD3/TD4/TR1/TR2 are used in the interrupt mode with hysteresis. Temperature exceeding T_O (Critical Temperature) causes an interrupt. Temperatures that fall below T_{HYST} (Critical Temperature Hysteresis) will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once the temperature exceeds T_O (Critical Temperature), an interrupt will be issued and the bit will be reset before the temperature falls to T_{HYST} (Critical Temperature Hysteresis). 10_{BIN} : One Time Interrupt Mode: Temperature sensors TD1/TD2/TD3/TD4/TR1/TR2 are used in the interrupt mode with hysteresis. Temperature exceeding T_O (Critical Temperature) causes an interrupt and then temperature going below T_{HYST} (Critical Temperature Hysteresis) will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O (Critical Temperature), then going below T_{HYST} (Critical Temperature Hysteresis), and interrupt will not occur again until the temperature exceeding T_O (Critical Temperature). 11_{BIN} : Two Time Non-related Interrupt Mode: Temperature sensors TD1/TD2/TD3/TD4/TR1/TR2 are used in the interrupt mode with hysteresis. Temperature exceeding T_O, causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}. If this mode is selected, for all monitor channels (it is not necessary to read the status for generating the next IRQ/SMI# pulse.  Two-Time Intrrupt Mode ** : Interrupt Status is read Note: It can be programmed to be as not necessary to read the status for generating the next SMI# pulse by setting TEMP_SMI_MD = 2'b11.
1	EN_IRQSMI. A one enables the IRQ/SMI# Interrupt output.
0	**POL**. (polarity) When set to 1, IRQ/SMI# active high. Set to 0, IRQ/SMI# active low.

8.6 OVT/BEEP Control Register

Another solution to deal with abnormal situation is through OVT (Over Temperature) or Beep.

OVT, as the name suggests, represents abnormal temperatures. In some applications, it can work with Fan control to throttle the Fan Speed.

Beep can directly use sound of two tones to inform the user of abnormal system operation. Unlike OVT, Beep can be issued due to abnormal operations of any channel.

8.6.1 OVT/BEEP Control Registers Map

Mnemonic	Register Name	Type
OVT_Ctrl	OVT Control	R/W
OVT_BeepEn	OVT/Beep Global Enable	R/W
BEEP_Ctrl1 BEEP_Ctrl5	BEEP Control 1 BEEP Control 5	R/W

Pin 2 of the W83793G is also a multi-function pin. It can be OVT# output signal or BEEP output signal and be selected by programming Bank0 CR52 OVT/BEEP Control register.

8.6.2 OVT/BEEP Control Registers Details

8.6.2.1. OVT Control Register (OVT_Ctrl)

Location: Bank 0 Address 51_{HEX}
Type: Read / Write
Reset: VSB5V (Pin 7) Rising.

OVT_CTRL

Bit	7	6	5	4	3	2	1	0
Name	**OVT_MD**	**EN_OVTR2**	**EN_OVTR1**	**EN_OVTD4**	**EN_OVTD3**	**EN_OVTD2**	**EN_OVTD1**	**OVTPOL**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	OVT_MD. There are two OVT# signal output types. 0_{BIN} : Comparator Mode: (Default) Temperature exceeding Tcritical (Critical Temperature) activates the OVT# output until the temperature is lower than T_{HYST} (Critical Temperature Hysteresis). 1_{BIN} : Interrupt Mode: Temperatures exceeding Tcritical (Critical Temperature) will activate the OVT# output until temperature sensor TD1/TD2/TD3/TD4/TR1/TR2 registers are read. If the current temperature rises from T_{HYST} (Critical Temperature Hysteresis) and exceeds Tcritical (Critical Temperature), the OVT# pin will be de-asserted. If the temperature falls below T_{HYST}, the OVT# pin will also generates an interrupt until it is reset by reading temperature sensor TD1/TD2/TD3/TD4/TR1/TR2 (interrupt status). Once the interrupt is generated, the OVT# pin does not issue additional interrupts even it the temperature remains above Tcritical.
6	EN_OVTR2. Enable the over-temperature (OVT) of temperature sensor TR2 if set to 1. The default value is 0; the OVTR2 output is disabled through pin OVT#. Pin OVT# is wire OR with OVTD1, OVTD2, OVTD3, OVTD4 and OVTR1.
5	EN_OVTR1. Enable temperature sensor TR1 over-temperature (OVT) output if set to 1. The default value is 0; the OVTR1 output is disabled through pin OVT#. Pin OVT# is wire OR with OVTD1, OVTD2, OVTD3, OVTD4 and OVTR2.
4	EN_OVTD4. Enable temperature sensor TD4 over-temperature (OVT) output if set to 1. The default value is 0; the OVTD4 output is disabled through pin OVT#. Pin OVT# is wire OR with OVTD1, OVTD2, OVTD3, OVTR1 and OVTR2
3	EN_OVTD3. Enable temperature sensor TD3 over-temperature (OVT) output if set to 1. The default value is 0; the OVTD3 output is disabled through pin OVT#. Pin OVT# is wire

Bit	Description
	OR with OVTD1, OVTD2, OVTD4, OVTR1 and OVTR2
2	EN_OVTD2. Enable temperature sensor TD2 over-temperature (OVT) output if set to 1. The default value is 0; the OVTD2 output is disabled through pin OVT#. Pin OVT# is wire OR with OVTD1, OVTD3, OVTD4, OVTR1 and OVTR2
1	EN_OVTD1. Enable temperature sensor TD1 over-temperature (OVT) output if set to 1. The default value is 0; the OVTD1 output is disabled through pin OVT#. Pin OVT# is wire OR with OVTD2, OVTD3, OVTD4, OVTR1 and OVTR2
0	OVTPOL. Write 1, pin OVT# is active high. Write 0, pin OVT# is active low.

8.6.2.2. OVT/Beep Global Enable Register (OVT_BeepEn)

Location: Bank 0 Address 52_{HEX}
Type: Read / Write
Reset: VSB5V(Pin 7) Rising.

OVT_BEEPEN

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**BEEPSEL**	**EN_BEEP**	**EN_OVT**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	Reserved.
2	BEEPSEL. 1: Direct Beep signal to Pin 2. 0: Direct OVT signal to Pin 2.
1	EN_BEEP. (Beep Output Global Enable) 1: Beep is enabled. Users can select event trigger source from BEEP_Ctrl. 0: Beep is disabled.
0	ENOVT. (OVT Output Global Enable) 1: OVT is enabled. Users can select OVT trigger source from OVT_Ctrl. 0: OVT is disabled.

8.6.2.3. BEEP Control Register (BEEP_Ctrl)

Setting to one will enable the corresponding BEEP output. Clearing to 0 will disable that BEEP output.

Location:

BEEP_Ctrl1 - Bank 0 Address 53_{HEX}
BEEP_Ctrl2 - Bank 0 Address 54_{HEX}
BEEP_Ctrl3 - Bank 0 Address 55_{HEX}
BEEP_Ctrl4 - Bank 0 Address 56_{HEX}
BEEP_Ctrl5 - Bank 0 Address 57_{HEX}

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

BEEP_CTRL1

Bit	7	6	5	4	3	2	1	0
Name	**VSEN4**	**VSEN3**	**VSEN2**	**VSEN1**	**Reserve**	**VTT**	**VCOREB**	**VCOREA**
Reset	0	0	0	0	0	0	0	0

BEEP_CTRL2

Bit	7	6	5	4	3	2	1	0
Name	**TD4**	**TD3**	**TD2**	**TD1**	**RESERVE**	**VBAT**	**5VSB**	**5VDD**
Reset	0	0	0	0	0	0	0	0

BEEP_CTRL3

Bit	7	6	5	4	3	2	1	0
Name	**FANIN6**	**FANIN5**	**FANIN4**	**FANIN3**	**FANIN2**	**FANIN1**	**TR2**	**TR1**
Reset	0	0	0	0	0	0	0	0

BEEP_CTRL4

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**	**Chassis**	**FANIN12**	**FANIN11**	**FANIN10**	**FANIN9**	**FANIN8**	**FANIN7**
Reset	0	0	0	0	0	0	0	0

BEEP_CTRL5

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**TART6**	**TART5**	**TART4**	**TART3**	**TART2**	**TART1**

Reset	0	0	0	0	0	0	0	0

8.7 Multi-Function Pin Control Register

Many functions exhibited in the W83793G are not default functions, and might share pin out with other functions. Here lists three registers that define the function enable registers.

8.7.1 Multi-Function Pin Control Register Map

Mnemonic	Register Name	Type
MFC	Multi-Function Pin Control	R/W
FANIN_Ctrl	FANIN Control	R/W
FAN_SEL	FANIN Input Pin Redirection	R/W

In the W83793G, Pin 10~13, Pin 37~40, and Pin 49~56 are multi-function pins. All non-default functions are enabled by setting Bank0 CR58, CR5C and CR5D.

8.7.2 Multi-Function Pin Control Register Details

8.7.2.1. Multi-Function Pin Control Register (MFC)

Location: Bank 0 Address 58_{HEX}
Type: Read / Write
Reset: bit 0~6:
VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.
Bit7: Trapping at 100ms after VSB5V (Pin 7) Rising.

MFC

Bit	7	6	5	4	3	2	1	0
Name	**VIDBSEL**	**SIB_SEL**	**SID_SEL**		**SIC_SEL**		**SIA_SEL**	**FAN8SEL**
Reset	Trap	0	0	0	0	0	0	0

Bit	Description
7	VIDBSEL. Pin 49~56 function select. Power-on Strapping input value of Pin 46. 1_{BIN}: Pin 49~56 are VIDB. 0_{BIN}: Pin 49~54 are fan speed control output or fan tachometer input; the functions of Pin 55~56 are controlled by bit SIB_SEL.
6	SIB_SEL. While VIDBSEL is 0, SIB_SEL sets the functions of Pin 55~56: $0_{BIN:}$ Pin 55~56 are FANIN8/FANCTRL8. 1_{BIN}: **Reserved.** This bit must be set to 0.
5-4	SID_SEL. Set the functions of Pin39~40: $0X_{BIN}$: Pin 39~40 are VIDA2/VIDA3. 10_{BIN}: Pin 39~40 are FANIN1/FANIN12. 11_{BIN}: Reserved. These two bits should not be set to 11_{BIN}.
3-2	SIC_SEL. Set the functions of Pin37~38: $0x_{BIN}$: Pin 37~38 are VIDA0/VIDA1. 10_{BIN}: Pin 37~38 are FAIN9/FANI10. 11_{BIN}: Reserved. These two bits should not be set to 11_{BIN}.

Bit	Description
1	SIA_SEL. Set the functions of Pin12~13: 0_{BIN}: Pin 12~13 are VIDA6/VIDA7. 1_{BIN}: Reserved. This bit must be set to 0.
0	FAN8SEL. Set the functions of Pin10~11: 0_{BIN}: Pin 10~11 are VIDA4/VIDA5. 1_{BIN}: Pin 12~13 are FANIN8/FANCTRL8.

8.7.2.2. FANIN Control Register (FANIN_Ctrl)

The register enables the setup of the multi-function fan inputs. With any reset, the register is cleared. (00_{HEX})

Location: Bank 0 Address $5C_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

FANIN_CTRL

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**	**EN_FANIN12**	**EN_FANIN11**	**EN_FANIN10**	**EN_FANIN9**	**EN_FANIN8**	**EN_FANIN7**	**EN_FANIN6**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	Reserved.
6	**EN_FANIN12**.(Fan In 12 Enable Bit) 1: If SID_SEL = 10_{BIN}, enable FANIN12 monitor. 0: Disable. The default is VID function.
5	**EN_FANIN11**.(Fan In 11 Enable Bit) If SID_SEL = 10, setting to 1 will enable FANIN11 monitor. If cleared, Pin39 can be selected as Processor A VID Bit 2(EN_D-VID).
4	**EN_FANIN10**.(Fan In 10 Enable Bit) If SIC_SEL = 10, setting to 1 will enable FANIN10 monitor. If cleared, Pin 38 can be selected as Processor A VID Bit 1.
3	**EN_FANIN9**.(Fan In 9 Enable Bit)

Bit	Description
	If SIC_SEL = 10, setting to 1 will enable FANIN9 monitor. If cleared, Pin 37 can be selected as Processor A VID Bit 0(EN_D-VID).
2	**EN_FANIN8**.(Fan In 8 Enable Bit) Setting to 1 enables FANIN8 monitor. If wish to connect FANIN8 to Pin55 is desired, VIDBSEL, SIDB_SEL and FAN8SEL must be set to 0. If wish to connect FANIN8 to Pin 10, setting FAN8SEL = 1 is a must. Setting to 0 enables Pin 10 with Processor A VID Bit 4(EN_D-VID)
1	**EN_FANIN7**.(Fan In 7 Enable Bit) If VIDBSEL = 0, setting to 1 will enable FANIN7 monitor. Setting to 0 enables Pin 53 with Processor B VID Bit 4(VIDBSEL = 1)
0	**EN_FANIN6**.(Fan In 6 Enable Bit) If VIDBSEL = 0, setting to 1 will enable FANIN6 monitor. Setting to 0 enables Pin 51 with Processor B VID Bit2(VIDBSEL = 1)

8.7.2.3. FANIN Input Pin Redirection Register (FANIN_Sel)

Location: Bank 0 Address $5D_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

FANIN_SEL

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**FANIN12Sel**	**FANIN11Sel**	**FANIN10Sel**	**FANIN9Sel**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	Reserve.
3	FANIN12Sel. If **FANIN12Sel** is set to 0, connect FANIIN12 to Pin 40; otherwise, connect FANIN12 to Pin 11. When FANIIN12 is connected to Pin 11, Bank0 CR58 bit0 FAN8SEL must be set to 1.
2	FANIN11Sel. If **FANIN11Sel** is set to 0, connect FANIIN11 to Pin 39; otherwise, connect FANIN11 to Pin 54.

Bit	Description
	When FANIIN11 is connected to Pin 54, Bank0 CR58 bit7 VIDBSEL must be set to 0.
1	FANIN10Sel. If **FANIN10Sel** is set to 0, connect FANIIN10 to Pin 38; otherwise, connect FANIN10 to Pin 52. When FANIIN10 is connected to Pin 52, VIDBSEL must set be to 0.
0	FANIN9Sel. If **FANIN9Sel** is set to 0, connect FANIIN9 to Pin 37; otherwise, connect FANIN9 to Pin 50. When FANIIN9 is connected to Pin 50, VIDBSEL must be set to 0.

8.8 Temperature Sensors Control Register

The W83793G provides two sets of LM75-like sensors, which function as two independent sensors through different I^2C address accesses (90_{HEX} ~ $9E_{HEX}$). These two sensors can also be accessed and controlled from the W83793G addresses (58_{HEX} ~ $5E_{HEX}$). Here lists the control registers for the LM75-like sensors.

8.8.1 Temperature Sensors Control Register Map

Mnemonic	Register Name	Type
TD1_Config.	Temperature Sensor TD1 Configuration (LM75A)	R/W
TD2_Config.	Temperature Sensor TD2 Configuration (LM75B)	R/W
TD_MD	Temperature Sensor mode Select 1	R/W
TR_MD	Temperature Sensor mode Select 2	R/W
TempOffset	Temperature Channel Offset	R/W

Please be noted that the W83793G supports 4 thermal diode inputs and 2 thermistor inputs, while the W83793AG supports only 1 thermal diode input and 2 thermistor inputs.

8.8.2 Temperature Sensors Control Register Details

8.8.2.1. TD1 Configuration (LM75A) Register (TD1_Config)

Location: Bank 0 Address $5A_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

TD1_CONFIG

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**FaultQ1**		**Reserve**			**STOP1**
Reset	0	0	00		0	0	0	0

Bit	Description
7-6	Reserved.
5-4	FaultQ1. Number of faults to detect before setting OVT# output to avoid false strapping due to noise.
3-1	Reserved.
0	STOP1. If temperature sensor TD1 is set as an internal temperature sensor (CR5D), setting to 1 will stop the temperature sensor.

8.8.2.2. TD2 Configuration (LM75B) Register (TD2_Config)

Location: Bank 0 Address $5B_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

TD2_CONFIG

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**FaultQ2**		**Reserve**			**STOP2**
Reset	0	0	00		0	0	0	0

Bit	Description
7-6	Reserved.
5-4	FaultQ2. Number of faults to detect before setting OVT# output to avoid false strapping due to noise.
3-1	Reserved.
0	STOP2. If temperature sensor TD2 is set as internal temperature sensor (CR5D), setting to 1 will stop the temperature sensor monitoring.

8.8.2.3. TD Mode Select Register (TD_MD)

Before enabling monitoring, it needs to set correct values to the pins (Bank0.CR58) and sensor select registers (Bank0.CR5E).

Location: **TD_MD** - Bank 0 Address $5E_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

TD_MD

Bit	7	6	5	4	3	2	1	0
Name	**TD4_MD**		**TD3_MD**		**TD2_MD**		**TD1_MD**	
Reset	01		01		01		01	

Bit	Description
7-6	TD4_MD. Temperature D4 mode 00_{BIN}: Temperature D4 stops monitoring. 01_{BIN}: Temperature D4 starts monitoring using the internal temperature sensor (default). 10_{BIN}: Reserved. 11_{BIN}: Temperature D4 starts monitoring using the temperature sensor in Intel CPU and obtains the results by PECI.
5-4	TD3_MD. Temperature D3 mode 00_{BIN}: Temperature D3 stops monitoring. 01_{BIN}: Temperature D3 starts monitoring using the internal temperature sensor (default).

Bit	Description
	10_{BIN}: Reserved. 11_{BIN}: Temperature D3 starts monitoring using the temperature sensor in Intel CPU and obtains the results by PECI.
3-2	TD2_MD. Temperature D2 mode 00_{BIN}: Temperature D2 stops monitor 01_{BIN}: Temperature D2 starts monitoring using the internal temperature sensor (default). 10_{BIN}: Reserved. 11_{BIN}: Temperature D2 starts monitoring using the temperature sensor in Intel CPU and obtains the results by PECI.
1-0	TD1_MD. Temperature D1 mode 00_{BIN}: Temperature D1 stops monitoring. 01_{BIN}: Temperature D1 starts monitoring using the internal temperature sensor (default). 10_{BIN}: Reserved. 11_{BIN}: Temperature D1 starts monitoring using the temperature sensor in Intel CPU and obtains the results by PECI.

8.8.2.4. TR Mode Select Register (TR_MD)

Location: **TR_MD** - Bank 0 Address $5F_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

TR_MD

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**						**TR2_MD**	**TR1_MD**
Reset	0	0	0	0	0	0	1	1

Bit	Description
7-2	Reserve.
1	TR2_MD. Setting to 1 will enable Temperature sensor TR2 monitor.
0	TR1_MD. Setting to 1 will enable Temperature sensor TR1 monitor.

8.8.2.5. Temperature Channel Offset Register (TempOffset)

Each temperature channel has a corresponding offset register. In some situations, the customer may want to shift the offset. The default is 00_{HEX}.

Location:

TD1Offset - Bank 0 Address $A8_{HEX}$
TD2Offset - Bank 0 Address $A9_{HEX}$
TD3Offset - Bank 0 Address AA_{HEX}
TD4Offset - Bank 0 Address AB_{HEX}
TR1Offset - Bank 0 Address AC_{HEX}
TR2Offset - Bank 0 Address AD_{HEX}

Type: Read / Write
Reset: VSB5V (Pin 7) Rising.

TD/TROFFSET

Bit	7	6	5	4	3	2	1	0
Name	**Sign**	**Offset value**						
Reset	0	0	0	0	0	0	1	1

Bit	Description
7-0	TD1~TR2 Offset Value.

8.9 Voltage Channel Registers

The monitored values and their corresponding limitation settings are listed. The W83793G provides more detailed resolution for VCoreA, VCoreB, and Vtt channels. Besides the 8-bit readout, there are still lower bits to be read.

Please be noted that VCOREB is for the W83793G only; the W83793AG does not support VCOREB.

8.9.1 Voltage Channel Registers Map

8.9.1.1. Voltage Channel Monitor Value Register Map

Mnemonic	Register Name	Type
VcoreA.	VCOREA Readout	RO
VcoreB.	VCOREB Readout	RO
Vtt.	Vtt Readout	RO
VINLowB.	VIN Low bit Readout	RO
VSEN1.	VSEN1 Readout	RO
VSEN2.	VSEN2 Readout	RO
VSEN3.	VSEN3 Readout	RO
VSEN4.	VSEN4 Readout	RO
5VDD.	5VDD Readout	RO
5VSB.	5VSB Readout	RO
VBAT.	VBAT Readout	RO

8.9.1.2. Voltage Channel Limit Value Registers Map

Mnemonic	Register Name	Type
VcoreA HL/LL.	VCOREA High/Low Limit	R/W

VcoreB HL/LL.	VCOREB High/Low Limit	R/W
Vtt HL/LL.	Vtt High/Low Limit	R/W
VINHLLowB.	VIN High Limit Low bit	R/W
VINLLLowB.	VIN Low Limit Low bit	R/W
VSEN1 HL/LL.	VSEN1 High/Low Limit	R/W
VSEN2 HL/LL.	VSEN2 High/Low Limit	R/W
VSEN3 HL/LL.	VSEN3 High/Low Limit	R/W
VSEN4 HL/LL.	VSEN4 High/Low Limit	R/W
5VDD HL/LL.	5VDD High/Low Limit	R/W
5VSB HL/LL.	5VSB High/Low Limit	R/W
VBAT HL/LL.	VBAT High/Low Limit	R/W

8.9.2 Voltage Channel Register Details

8.9.2.1. Voltage Channel Monitored Value

Location:

VCOREA Readout - Bank 0 Address 10_{HEX}
VCOREB Readout - Bank 0 Address 11_{HEX}
Vtt Readout - Bank 0 Address 12_{HEX}
VIN Low bit - Bank 0 Address $1B_{Hex}$
VSEN1 Readout - Bank 0 Address 14_{HEX}
VSEN2 Readout - Bank 0 Address 15_{HEX}
VSEN3 Readout - Bank 0 Address 16_{HEX}
VSEN4 Readout - Bank 0 Address 17_{HEX}
5VDD Readout - Bank 0 Address 18_{HEX}
5VSB Readout - Bank 0 Address 19_{HEX}
VBAT Readout - Bank 0 Address $1A_{HEX}$

Type: Read Only
Reset: No Reset

VOLTAGE READOUT

Bit	7	6	5	4	3	2	1	0
Name	**Voltage Voltage**							

VIN LOW BIT READOUT

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**VttL**		**VCOREBL**		**VcoreAL**	

Channel VcoreA/B, and Vtt combines the 8-bit readout and the low nibble to express each channel's monitored results; therefore, it is 10-bit format data. For example, the monitored value of VCOREA can be obtained from the combination of VCOREA Readout and bit 1~0 of VIN Low bit Readout. In order to read the correct result, it needs to read the high byte first and then to read its corresponding low byte. The real voltage calculation of these three channels should follow the formula

Vcore A Voltage = (CR [10]*4 + CR [1B] &0x03) * 0.002;
Vcore B Voltage = (CR [11]*4 + (CR [1B] &0x0C)/4) * 0.002;
Vtt Voltage = (CR [12]*4 + (CR [1B] &0x30)/16) * 0.002;

The rest voltage channels only support 8-bit output format. The real voltage calculation of these three channels should follow the formula

VSEN1 Voltage = CR [14] * (2 * 0.008);
VSEN2 Voltage = CR [15] * (2 * 0.008);
VSEN3 Voltage = CR [16] * (2 * 0.008);
VSEN4 Voltage = CR [17] * 0.008;
5VDD Voltage = CR [18] * (2 * 1.5 * 0.008)+0.15;
5VSB Voltage = CR [19] * (2 * 1.5 * 0.008)+0.15;
VBAT Voltage = CR [1A] * (2 * 0.008);

8.9.2.2. Voltage Channel Limitation Registers

Location:

VCOREA High Limit Bank 0 Address 60_{HEX}
VCOREA Low Limit Bank 0 Address 61_{HEX}
VCOREB High Limit Bank 0 Address 62_{HEX}
VCOREB Low Limit Bank 0 Address 63_{HEX}
Vtt High Limit Bank 0 Address 64_{HEX}
Vtt Low Limit Bank 0 Address 65_{HEX}
High Limit Low bit Bank 0 Address 68_{HEX}
Low Limit Low bit Bank 0 Address 69_{HEX}
VSEN1 High Limit Bank 0 Address $6A_{HEX}$
VSEN1 Low Limit Bank 0 Address $6B_{HEX}$
VSEN2 High Limit Bank 0 Address $6C_{HEX}$
VSEN2 Low Limi Bank 0 Address $6D_{HEX}$
VSEN3 High Limit Bank 0 Address $6E_{HEX}$
VSEN3 Low Limit Bank 0 Address $6F_{HEX}$
VSEN4 High Limit Bank 0 Address 70_{HEX}
VSEN4 Low Limit Bank 0 Address 71_{HEX}
5VDD High Limit Bank 0 Address 72_{HEX}
5VDD Low Limit Bank 0 Address 73_{HEX}
5VSB High Limit Bank 0 Address 74_{HEX}
5VSB Low Limit Bank 0 Address 75_{HEX}
VBAT High Limit Bank 0 Address 76_{HEX}
VBAT Low Limit Bank 0 Address 77_{HEX}

Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set.

VOLTAGE HIGH LIMIT

Bit	7	6	5	4	3	2	1	0
Name	**Voltage High Limit**							
Reset	FF_{HEX}							

VOLTAGE LOW LIMIT

Bit	7	6	5	4	3	2	1	0
Name	**Voltage Low Limit**							
Reset	00_{HEX}							

VIN HIGH LIMIT LOW BIT

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**VTTHLL**		**VCOREBHLL**		**VcoreAHLL**	
Reset	00		11		11		11	

VIN LOW LIMIT LOW BIT

Bit	7	6	5	4	3	2	1	0
Name	**Reserve**		**VTTLLL**		**VCOREBLLL**		**VcoreALLL**	
Reset	00		00		00		00	

The code calculation of high/low limit should follow the formula

VCoreA, VCoreB, Vtt Limit Setup
CR60~66 = [Desired Voltage]/0.008;
CR68/69 = ([Desired Voltage]/0.002) – CR60~67 * 4;

VSEN1, VSEN2, VSEN3 Limit Setup
CR6A~6F = [Desired Voltage] / 0.016;

VSEN4 Limit Setup
CR70~71 = [Desired Voltage] / 0.08;

5VDD, 5VSB Limit Setup
CR72~75 = [Desired Voltage] - 0.15 / 0.024;

VBAT Limit Setup
CR76~77 = [Desired Voltage] / 0.016;

8.10 Temperature Channel Registers

8.10.1 Temperature Channel Register Map

8.10.1.1. Temperature Channel Monitored Value Register Map

Mnemonic	Register Name	Type
TD1.	Temperature Sensor TD1 Readout	RO
TD2.	Temperature Sensor TD2 Readout	RO
TD3.	Temperature Sensor TD3 Readout	RO
TD4.	Temperature Sensor TD4 Readout	RO
TDLowB.	Temperature Sensor TD Low Bit Readout	RO
TR1.	Temperature Sensor TR1 Readout	RO
TR2.	Temperature Sensor TR2 Readout	RO

8.10.1.2. Temperature Channel Limitation Value Register Map

Mnemonic	Register Name	Type
TD1 CT/CTH.	TD1 Critical Temperature / Critical Temperature Hysteresis	R/W
TD1 WT/WTH.	TD1 Warning Temperature / Warning Temperature Hysteresis	R/W
TD2 CT/CTH.	TD2 Critical Temperature / Critical Temperature Hysteresis	R/W
TD2 WT/WTH.	TD2 Warning Temperature / Warning Temperature Hysteresis	R/W
TD3 CT/CTH.	TD3 Critical Temperature / Critical Temperature Hysteresis	R/W

Mnemonic	Register Name	Type
TD3 WT/WTH.	TD3 Warning Temperature / Warning Temperature Hysteresis	R/W
TD4 CT/CTH.	TD4 Critical Temperature / Critical Temperature Hysteresis	R/W
TD4 WT/WTH.	TD4 Warning Temperature / Warning Temperature Hysteresis	R/W
TR1 CT/CTH.	TR1 Critical Temperature / Critical Temperature Hysteresis	R/W
TR1 WT/WTH.	TR1 Warning Temperature / Warning Temperature Hysteresis	R/W
TR2 CT/CTH.	TR2 Critical Temperature / Critical Temperature Hysteresis	R/W
TR2 WT/WTH.	TR2 Warning Temperature / Warning Temperature Hysteresis	R/W

8.10.2 Temperature Channel Register Details

8.10.2.1. Temperature Channel Monitored Registers

Location:

TD1 Readout - Bank 0 Address $1C_{HEX}$
TD2 Readout - Bank 0 Address $1D_{HEX}$
TD3 Readout - Bank 0 Address $1E_{HEX}$
TD4 Readout - Bank 0 Address $1F_{HEX}$
Low bit Readout - Bank 0 Address 22_{HEX}
Type: Read Only

TR1 Readout - Bank 0 Address 20_{HEX}
TR2 Readout - Bank 0 Address 21_{HEX}

TEMP READOUT

Bit	7	6	5	4	3	2	1	0
Name	**Temperature**							

TD LOW BIT READOUT

Bit	7	6	5	4	3	2	1	0
Name	**TD4L**		**TD3L**		**TD2L**		**TD1L**	

The format of Temperature channel readout is 2'complement. TD channel expresses the temperature using 10-bit data, including 1-bit sign bit, 7-bit integer, and 2 bits decimal. TR channel expresses the temperature using 8-bit data, including 1-bit sign bit, and 7-bit integer.

For TD channel temperature = TDx + TDxL* 0.25

TR channel temperature = TRx

8.10.2.2. Temperature Channel Limitation Registers

Location:

TD1 Critical - Bank 0 Address 78_{HEX}
TD1 Critical Hystersis - Bank 0 Address 79_{HEX}
TD1 Warning - Bank 0 Address $7A_{HEX}$
TD1 Warning Hystersis - Bank 0 Address $7B_{HEX}$
TD2 Critical - Bank 0 Address $7C_{HEX}$
TD2 Critical Hystersis - Bank 0 Address $7D_{HEX}$
TD2 Warning - Bank 0 Address $7E_{HEX}$
TD2 Warning Hystersis - Bank 0 Address $7F_{HEX}$
TD3 Critical - Bank 0 Address 80_{HEX}
TD3 Critical Hystersis - Bank 0 Address 81_{HEX}
TD3 Warning - Bank 0 Address 82_{HEX}
TD3 Warning Hystersis - Bank 0 Address 83_{HEX}

TD4 Critical - Bank 0 Address 84_{HEX}
TD4 Critical Hystersis - Bank 0 Address 85_{HEX}
TD4 Warning - Bank 0 Address 86_{HEX}
TD4 Warning Hystersis - Bank 0 Address 87_{HEX}
TR1 Critical - Bank 0 Address 88_{HEX}
TR1 Critical Hystersis - Bank 0 Address 89_{HEX}
TR1 Warning - Bank 0 Address $8A_{HEX}$
TR1 Warning Hystersis-Bank 0 Address $8B_{HEX}$
TR2 Critical - Bank 0 Address $8C_{HEX}$

TR2 Critical Hystersis - Bank 0 Address $8D_{HEX}$ **TR2 Warning Hystersis**- Bank 0 Address $8F_{HEX}$
TR2 Warning - Bank 0 Address $8E_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising.

SENSOR CRITICAL TEMPERATURE

Bit	7	6	5	4	3	2	1	0
Name	**Temp Critical Temperature**							
Reset	64_{HEX} (100 C)							

SENSOR CRITICAL TEMPERATURE HYSTERSIS

Bit	7	6	5	4	3	2	1	0
Name	**Sensor Critical Temperature Hysteresis**							
Reset	$5F_{HEX}$ (95 C)							

SENSOR CRITICAL TEMPERATURE

Bit	7	6	5	4	3	2	1	0
Name	**Sensor Warning Temperature**							
Reset	55_{HEX} (85 C)							

SENSOR WARNING TEMPERATURE HYSTERSIS

Bit	7	6	5	4	3	2	1	0
Name	**Sensor Warning Temperature Hysteresis**							
Reset	50_{HEX} (80 C)							

The format of Temperature channel limit is 2'complement; bit 7 is sign bit, and the range is –128~127.

8.11 Fan Control Registers

All Fan Control/Status registers are located in Bank 0 and Bank 2. Bank 0 resides common-used control/status registers, and in Bank 2 are the Smart Fan Control setups.

8.11.1 Fan Register Map

8.11.1.1. Common Register Control/Status registers Block

All common Fan Control/Status registers are located in Bank 0.

Mnemonic	Register Name	Type
Fan1CountH/L. | Fan12CountH/L.	Fan tachometer readout high/low Byte	RO
Fan1LimitH/L. | Fan12LimitH/L.	Fan Count Limit high/low Byte	RW
FanCtrl1. FanCtrl2.	Fan Output style Control	RW
DefaultSpeed.	Default Fan Speed at power-on	RW
Fan1Duty. | Fan8Duty.	Current Fan output Duty Cycle	RW
PWM1Prescalar. | PWM8Prescalar.	Fan PWM output frequency pre-scalar	RW

Here listed registers which can read the tachometer values, and their limit registers. All of these registers are separated into 2 bytes. Reading tachometer count high byte will lock the corresponding low byte to ensure data consistency in next reading on the low byte.

Because FANIN 6~12 (Pins 37, 38, 39, 40, 51, 53, and 55) are multifunction pins, **FanInControl** provides the selection between FanIn functions and other functions.

Fan Output style (DC/PWM), Duty cycle, and frequency controls are also provided.

8.11.1.2. Smart Fan Setup/Status registers

Registers of SmartFan setup resides in Bank 0 and Bank 2. Most used step timing control and critical temperature setup are located in Bank 0. All the others are located in Bank 2.

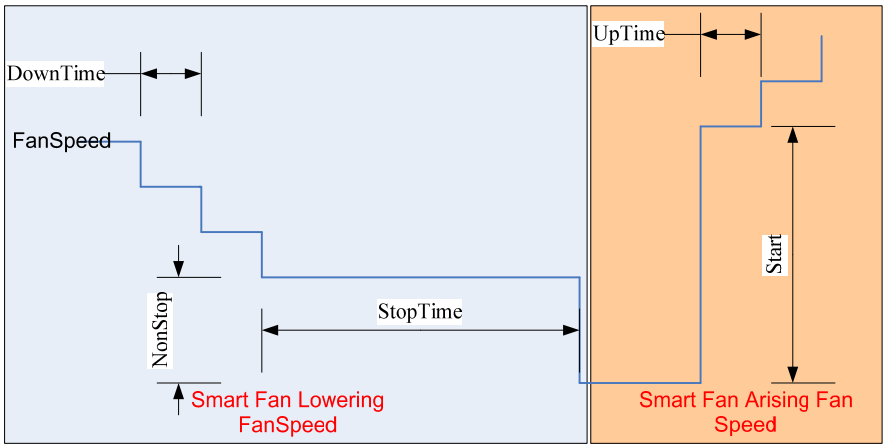
Mnemonic	Register Name	Type
UpTime.	SmartFan Fan Step Up Time	RW
DownTime.	SmartFan Fan Step Down Time	RW

Mnemonic	Register Name	Type
CriticalTemp.	All Fan full speed temperature	RW
TD1FanSelect. TR2FanSelect.	Temperature to Fan mapping relationships in SmartFan mode	RW
FanCtrlMode.	SmartFan Control Mode Select	RW
TolTD12. TolTR12.	Hysteresis tolerance of each temperature source	RW
Fan1Nonstop. Fan8Nonstop.	Fan Output Nonstop Duty cycle	RW
Fan1Start. Fan8Start.	Fan Output Start Duty Cycle	RW
Fan1StopTime. Fan8StopTime.	Fan Stop Time from nonstop level to turn off.	RW

Smart Fan Mode is activated on the corresponding fans once users define the relationship between the fan and the temperature input in TempFanSelect. Under SmartFan Mode, user can select Thermal Cruise mode or SMART FAN™ II mode by assigning FanCtrlMode.

TempFanSelect enables users to arbitrarily define the Temperature-to-Fan relationship. For example, one can define Thermistor input 1 as chassis temperature sensor, and Temperature 1(Diode Input 1) as CPU sensor. Users can manipulate Fan1 (CPU Fan) and Fan2 (System Fan) as the following. Assigning TD1FanSelect 03_{HEX} and TR1FanSelect 02_{HEX}, the W83793G will connect the system fan with the CPU sensor and the Chassis sensor, but the CPU fan will only be affected by the CPU sensor. More descriptions can be found at the register definition section for this issue.

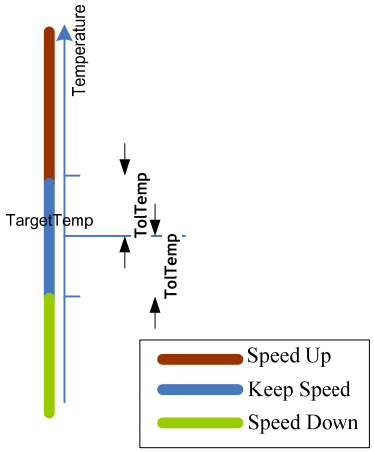
In SmartFan Mode, a specific temperature will be defined in **CriticalTemp**. If any temperature input detected is higher than this, all fans will operate at full speed simultaneously. The definitions of the control parameters in normal use are shown in the following graph.



8.11.1.3. Thermal Cruise Mode Registers (Bank 2)

Mnemonic	Register Name	Type
TD1Target. TR2Target.	Target Temperature of Temperature inputs	RW

Thermal Cruise mode is an algorithm to control the fan speed to keep the temperature source around the target temperature. If the temperature source detects temperatures higher or lower than the target temperatures with **TolTemp** tolerance, Smart Fan Control will take actions to speed up or slow down the fan to keep the temperature within the tolerance range.



The concept is quite simple. When the temperature is higher than **TargetTemp**+**TolTemp**, the fan will be speeded up. When the temperature is lower than **TargetTemp**-**TolTemp**, the fan will be slowed down. Otherwise, the fan keeps its current speed.

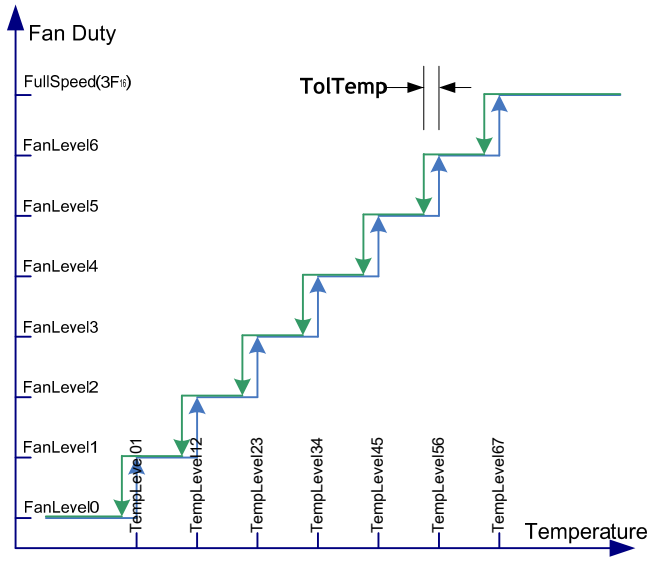
8.11.1.4. Smart Fan II Control registers (Bank 2)

Mnemonic	Register Name	Type

Mnemonic	Register Name	Type
TD1Level01. TR2Level67.	Smart Fan II Fan Transition temperature levels	RW
TD1FanLevel0. TR2FanLevel6.	Smart Fan II Fan Output Levels	RW

SMART FAN^{TM}II algorithm provides users a mechanism to set up the fan speed via Temperature level relationship. Each temperature source has a corresponding table, and totally six tables are used to control Temperature 1(D1) to Temperature 6 (R2).

A table consists of 7 temperature levels and 7 fan levels as the following.



When the fan speed jumps from one level to another, there is a hysterisis mechanism to prevent the fan from throttling. When the temperature rises from one level to another, the fan speed rises to a higher level. However, the temperature has to be lower than the specified temperature minus the tolerance to make the fan speed drop to the lower level.

8.11.2 Fan Register Details

8.11.2.1. Fan Tachometer Readout high/low Byte Register (FanCountH/L)

The FanCountH/L maintains current count value of corresponding fan inputs. When 5VSB is on, it is cleared (00_{HEX}). The effective width of FanCountH/L is 12-bit. The FanCountH high nibble is not used.

Location:

Fan1CountH - Bank 0 Address 23_{HEX}
Fan1CountL – Bank 0 Address 24_{HEX}
Fan2CountH – Bank 0 Address 25_{HEX}
Fan2CountL – Bank 0 Address 26_{HEX}
Fan3CountH – Bank 0 Address 27_{HEX}
Fan3CountL – Bank 0 Address 28_{HEX}
Fan4CountH – Bank 0 Address 29_{HEX}
Fan4CountL – Bank 0 Address $2A_{HEX}$
Fan5CountH – Bank 0 Address $2B_{HEX}$
Fan5CountL – Bank 0 Address $2C_{HEX}$
Fan6CountH – Bank 0 Address $2D_{HEX}$
Fan6CountL – Bank 0 Address $2E_{HEX}$
Fan7CountH – Bank 0 Address $2F_{HEX}$
Fan7CountL – Bank 0 Address 30_{HEX}
Fan8CountH – Bank 0 Address 31_{HEX}
Fan8CountL – Bank 0 Address 32_{HEX}
Fan9CountH – Bank 0 Address 33_{HEX}
Fan9CountL – Bank 0 Address 34_{HEX}
Fan10CountH – Bank 0 Address 35_{HEX}
Fan10CountL – Bank 0 Address 36_{HEX}
Fan11CountH – Bank 0 Address 37_{HEX}
Fan11CountL – Bank 0 Address 38_{HEX}
Fan12CountH – Bank 0 Address 39_{HEX}
Fan12CountL – Bank 0 Address $3A_{HEX}$

Type: Read Only
Reset: VSB5V (Pin 7) Rising

FAN1COUNTH~FAN12COUNTH

Bit	7	6	5	4	3	2	1	0
Name	**FanCountH**							
Reset	00_{HEX}							

Bit	Description
7-0	**FanCountH** (Fan tachometer readout high byte). The count value high byte of FanIn signal period with 45KHz clock.

FAN1COUNTL~FAN12COUNTL

Bit	7	6	5	4	3	2	1	0
Name	**FanCountL**							
Reset	00_{HEX}							

Bit	Description
7-0	**FanCountL**(Fan tachometer readout low byte). The count value low byte of FanIn signal period with 45KHz clock.

FAN COUNT CALCULATION

Fan1CountL together with Fan1CountH form the 12-bit count value. If Fan1CountH and Fan1CountL are read successively, the W83793G will make these two count values consistent (i.e. the same counting). If the user reads them in reverse order or there is other read/write in between, it is possible that the high/low byte may come from different counting and lead to abnormal reading. Same rules can be applied to other FanCounts.

Real RPM (Rotate per Minute) calculations should follow the formula

$$FanSpeed(RPM) = \frac{1.35 \times 10^6}{(12 - bitCountValue) \times (FanPoles/4)}$$

In this formula, *12-bitCountValue* represents the values stored in FanCountH/L, and *FanPoles* stands for the number of NS pole pairs inside the fan. Normally an N-S-N-S Fan (*FanPoles* = 4) generates 2 pulses after completing one rotation.

The frequency range for the fan tachometer is below 4.5 KHz (if FanPoles=4, it means 135KRPM). It is almost impossible, but a fan working faster than this will cause the malfunction of the W83793G.

8.11.2.2. Fan Count Limit High/Low Byte (FanLimitH/L)

The **FanLimitH/L** sets up the limit range for the fan in count values. If the counter counts value larger than what the registers indicate, the W83793G will show alert in the real-time status and may take further actions based on user setups. While reset it is set (FF_{HEX}).

Location:

Fan1LimitH - Bank 0 Address 90_{HEX}
Fan1LimitL – Bank 0 Address 91_{HEX}
Fan2LimitH – Bank 0 Address 92_{HEX}
Fan2LimitL – Bank 0 Address 93_{HEX}
Fan3LimitH – Bank 0 Address 94_{HEX}
Fan3LimitL – Bank 0 Address 95_{HEX}
Fan4LimitH – Bank 0 Address 96_{HEX}
Fan4LimitL – Bank 0 Address 97_{HEX}
Fan5LimitH – Bank 0 Address 98_{HEX}
Fan5LimitL – Bank 0 Address 99_{HEX}
Fan6LimitH – Bank 0 Address $9A_{HEX}$
Fan6LimitL – Bank 0 Address $9B_{HEX}$
Fan7LimitH – Bank 0 Address $9C_{HEX}$
Fan7LimitL – Bank 0 Address $9D_{HEX}$
Fan8LimitH – Bank 0 Address $9E_{HEX}$
Fan8LimitL – Bank 0 Address $9F_{HEX}$
Fan9LimitH – Bank 0 Address $A0_{HEX}$
Fan9LimitL – Bank 0 Address $A1_{HEX}$
Fan10LimitH – Bank 0 Address $A2_{HEX}$
Fan10LimitL – Bank 0 Address $A3_{HEX}$
Fan11LimitH – Bank 0 Address $A4_{HEX}$
Fan11LimitL – Bank 0 Address $A5_{HEX}$
Fan12LimitH – Bank 0 Address $A6_{HEX}$
Fan12LimitL – Bank 0 Address $A7_{HEX}$

Type: Read / Write

Reset: VSB5V (Pin 7) Rising.

FAN1LIMITH ~ FAN12LIMITH

Bit	7	6	5	4	3	2	1	0
Name	**FanLimitH**							
Reset	FF_{HEX}							

Bit	Description
7-0	**FanLimitH** (Fan tachometer limit high byte). The limitation of the count value high byte of FanIn.

FAN1LIMITL~FAN12LIMITL

Bit	7	6	5	4	3	2	1	0
Name	**FanLimitL**							
Reset	FF_{HEX}							

Bit	Description
7-0	**FanLimitL** (Fan tachometer readout limit low byte). The limitation of the count value low byte of FanIn.

8.11.2.3. Fan Output Style Control (FanCtrl)

FanCtrl1/2 decide the fan output style. Several output styles are available in the W83793G, including the OD mode (Open-Drain), the OB mode (Output-Buffer), and the DC mode (DAC output). The OD mode is the default of all fan outputs.

Location:

FanCtrl1 - Bank 0 Address $B0_{HEX}$

FanCtrl2 – Bank 0 Address $B1_{HEX}$

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

FANCTRL1

Bit	7	6	5	4	3	2	1	0
Name	**F8OB**	**F7OB**	**F6OB**	**F5OB**	**F4OB**	**F3OB**	**F2OB**	**F1OB**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**F8OB** (Fan output 8 Output Buffer Mode Control). 0: Depends on **F8DC** (CRB1.Bit7). If F8DC=1, Pin 11 outputs with the DC mode. Otherwise, the output is configured to the OD mode. 1: Depends on **F8DC** (CRB1.Bit7). If F8DC=1, Pin 11 outputs with the DC mode. Otherwise, the output is configured to the OB mode
6	**F7OB** (Fan output 7 Output Buffer Mode Control). 0: Depends on **F7DC** (CRB1.Bit6). If F7DC=1, Pin 54 outputs with the DC mode.

Bit	Description
	Otherwise, the output is configured to the OD mode. 1: Depends on **F7DC** (CRB1.Bit6). If F7DC=1, Pin 54 outputs with the DC mode. Otherwise, the output is configured to the OB mode
5	**F6OB** (Fan output 6 Output Buffer Mode Control). 0: Depends on **F6DC** (CRB1.Bit5). If F6DC=1, Pin 52 outputs with the DC mode. Otherwise, the output is configured to the OD mode. 1: Depends on **F6DC** (CRB1.Bit5). If F6DC=1, Pin 52 outputs with the DC mode. Otherwise, the output is configured to the OB mode
4	**F5OB** (Fan output 5 Output Buffer Mode Control). 0: Depends on **F5DC** (CRB1.Bit4).If F5DC=1, Pin 50 outputs with the DC mode. Otherwise, the output is configured to the OD mode. 1: Depends on **F5DC** (CRB1.Bit4). If F5DC=1, Pin 50 outputs with the DC mode. Otherwise, the output is configured to the OB mode
3	**F4OB** (Fan output 4 Output Buffer Mode Control). 0: Depends on **F4DC** (CRB1.Bit3). If F4DC=1, Pin 49 outputs with the DC mode. Otherwise, the output is configured to the OD mode. 1: Depends on **F4DC** (CRB1.Bit3). If F4DC=1, Pin 49 outputs with the DC mode. Otherwise, the output is configured to the OB mode
2	**F3OB** (Fan output 3 Output Buffer Mode Control). 0: Depends on **F3DC** (CRB1.Bit2). If F3DC=1, Pin 46 outputs with the DC mode. Otherwise, the output is configured to the OD mode. 1: Depends on **F3DC** (CRB1.Bit2). If F3DC=1, Pin 46 outputs with the DC mode. Otherwise, the output is configured to the OB mode
1	**F2OB** (Fan output 2 Output Buffer Mode Control). 0: Depends on **F2DC** (CRB1.Bit1). If F2DC=1, Pin 44 outputs with the DC mode. Otherwise, the output is configured to the OD mode. 1: Depends on **F2DC** (CRB1.Bit1). If F2DC=1, Pin 44 outputs with the DC mode. Otherwise, the output is configured to the OB mode
0	**F1OB** (Fan output 1 Output Buffer Mode Control). 0: Depends on **F1DC** (CRB1.Bit0). If F1DC=1, Pin 42 outputs with the DC mode. Otherwise, the output is configured to the OD mode. 1: Depends on **F1DC** (CRB1.Bit0). If F1DC=1, Pin 42 outputs with the DC mode. Otherwise, the output is configured to the OB mode

FANCTRL2

Bit	7	6	5	4	3	2	1	0
Name	**F8DC**	**F7DC**	**F6DC**	**F5DC**	**F4DC**	**F3DC**	**F2DC**	**F1DC**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**F8DC** (Fan output 8 Direct Current Mode Control).

Bit	Description
	0: OD or OB mode on Pin 11. Depend on **F8OB** (CRB0.Bit7) 1: Pin 11 is set to the DC mode.
6	**F7DC** (Fan output 7 Direct Current Mode Control). 0: OD or OB mode on Pin 54. Depend on **F7OB** (CRB0.Bit6) 1: Pin 54 is set to the DC mode.
5	**F6DC** (Fan output 6 Direct Current Mode Control). 0: OD or OB mode on Pin 52. Depend on **F6OB** (CRB0.Bit5) 1: Pin 52 is set to the DC mode.
4	**F5DC** (Fan output 5 Direct Current Mode Control). 0: OD or OB mode on Pin 50. Depend on **F5OB** (CRB0.Bit4) 1: Pin 50 is set to the DC mode.
3	**F4DC** (Fan output 4 Direct Current Mode Control). 0: OD or OB mode on Pin 49. Depend on **F4OB** (CRB0.Bit3) 1: Pin 49 is set to the DC mode.
2	**F3DC** (Fan output 3 Direct Current Mode Control). 0: OD or OB mode on Pin 46. Depend on **F3OB** (CRB0.Bit2) 1: Pin 46 is set to the DC mode.
1	**F2DC** (Fan output 2 Direct Current Mode Control). 0: OD or OB mode on Pin 44. Depend on **F2OB** (CRB0.Bit1) 1: Pin 44 is set to the DC mode.
0	**F1DC** (Fan output 1 Direct Current Mode Control). 0: OD or OB mode on Pin 42. Depend on **F1OB** (CRB0.Bit0) 1: Pin 42 is set to the DC mode.

8.11.2.4. Default Fan Speed at Power-on (DefaultSpeed)

DefaultSpeed sets the initial speed of every fan. When the system is turned on, a default will be given to all fan outputs according to the register content. This register is specially designed to be reset by VSB only, so at the second system power on, the system will use the last setup speed to turn on all of the fans.

Location: **DefaultSpeed** - Bank 0 Address $B2_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising.

DefaultSpeed

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**DefaultSpeed**					
Reset	0	0	30_{HEX}					

Bit	Description

Bit	Description
7-6	Reserved.
5-0	**DefaultSpeed** (Default Fan Speed at Power-on). Specifies the fan duty at next power on.

8.11.2.5. Current Fan Output Duty Cycle (FanDuty)

FanDuty reflects the current output duty cycle. In the manual mode, the user can set preferred duty cycles. However, in the Smart Fan mode, it is read-only.

Location:

Fan1Duty - Bank 0 Address $B3_{HEX}$
Fan2Duty - Bank 0 Address $B4_{HEX}$
Fan3Duty - Bank 0 Address $B5_{HEX}$
Fan4Duty - Bank 0 Address $B6_{HEX}$
Fan5Duty - Bank 0 Address $B7_{HEX}$
Fan6Duty - Bank 0 Address $B8_{HEX}$
Fan7Duty - Bank 0 Address $B9_{HEX}$
Fan8Duty - Bank 0 Address BA_{HEX}

Type: Read / Write (Only in Manual Mode, make sure 5VDD and Pin 1 CLK are ready)
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

FAN1DUTY ~ FAN8DUTY

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**FanDuty**					
Reset	0	0	Depend on DefaultSpeed.					

Bit	Description
7-6	Reserved.
5-0	**FanDuty**(Current Fan output Duty Cycle). Specifies the current duty cycle of the fan. If 5VDD is low, this register is set to zero by the hardware.

FanDuty also has a special characteristic- sequential power-on. This function is used to avoid over loads of the system current when the system is powered-on and all fans start to spin. The W83793G takes 0.1 second (12.5ms intervals for 8 fans) to turn on all of the fans one by one.

8.11.2.6. Fan PWM Output Frequency Prescalar (PWMPrescalar)

PWMPrescalar controls the output frequency in the PWM mode. A wide range of clocks can be selected to satisfy customer needs. The default output frequency is 25 KHz.

Location:

PWM1Prescalar - Bank 0 Address BB_{HEX}
PWM2Prescalar - Bank 0 Address BC_{HEX}
PWM3Prescalar - Bank 0 Address BD_{HEX}
PWM4Prescalar - Bank 0 Address BE_{HEX}
PWM5Prescalar - Bank 0 Address BF_{HEX}
PWM6Prescalar - Bank 0 Address $C0_{HEX}$

PWM7Prescalar - Bank 0 Address $C1_{HEX}$ **PWM8Prescalar** - Bank 0 Address $C2_{HEX}$

Type: Read / Write (Only in Manual Mode)

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

PWM1PRESCALAR ~ PWM8PRESCALAR

Bit	7	6	5	4	3	2	1	0
Name	**CKSEL**	**Divisor**						
Reset	1	09_{HEX}						

Bit	Description
7	**CKSEL** (clock source select). 0: 512Hz. 1: 250KHz.
6-0	**Divisor** (Clock Divisor). Clock frequency Divisor.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency. There are 2 divisors depending on CKSEL.

If CKSEL equals 1, then the output clock is simply equal to 250/ (Divisor+1) KHz.

If CKSEL equals 0, the output clock is 512Hz/MappedDivisor. MappedDivisor depends on Divisor[3:0] and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	512Hz	1000	12	43Hz
0001	2	256Hz	1001	16	32Hz
0010	3	171Hz	1010	32	16Hz
0011	4	128Hz	1011	64	8Hz
0100	5	102Hz	1100	128	4Hz
0101	6	85Hz	1101	256	2Hz
0110	7	73Hz	1110	512	1Hz
0111	8	64Hz	1111	1024	0.5Hz

8.11.2.7. SmartFan Output Step Up Time (UpTime)

UpTime adjusts the time interval of the fan speed up by a unit. The default setting is 0.6sec.

Location: **UpTime** - Bank 0 Address $C3_{HEX}$

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,

Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

UPTIME

Bit	7	6	5	4	3	2	1	0
Name	**UpTime**							
Reset	06_{HEX}							

Bit	Description
7-0	**UpTime**(SmartFan Step Up Time). Unit in 0.1sec. Programmed as the interval of continuous Fan ramping up.

SmartFan is designed for the smooth operation of the fan. The fan duty is seldom suddenly increased or decreased. Instead, most often the duty is increased or decreased by 1 LSB. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed. On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat. This register should never be set to 0. Otherwise, the fan duty will be abnormal.

Only in the following cases will the fan duty soar or plummet.

→VDD Power – on/off

→Critical Temperature reached

→Fan Turn off state to Start

→Fan at NonStop Level to turn off state

8.11.2.8. SmartFan Output Step Down Time (DownTime)

Down Time reduces the time interval of the fastest fan speed by a unit. The default setting is 0.6sec.

Location: **DownTime** - Bank 0 Address $C4_{HE}X$

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

DOWNTIME

Bit	7	6	5	4	3	2	1	0
Name	**DownTime**							
Reset	06_{HEX}							

Bit	Description

7-0	**DownTime** (SmartFan Step Down Time). Unit in 0.1sec. Programmed as the interval of continuous Fan ramping Down.

This register should never be set to 0. Otherwise, the fan duty will be abnormal.

8.11.2.9. All Fan Full Speed Temperature (CriticalTemp)

CriticalTemp defines a system critical temperature. Temperatures exceeding this threshold may lead to system damage or crash. When the W83793G detects any temperature input exceeding **CriticalTemp**, it will speed up all of the fans to lower the temperature.

Location:

CritcalTemp - Bank 0 Address $C5_{HEX}$

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

UPTIME

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**CriticalTemp**						
Reset	0	50_{HEX}						

Bit	Description
7	Reserved.
6-0	**CriticalTemp**(All Fan Full Speed Temperature).

8.11.2.10. Temperature to Fan mapping relationships Register (TempFanSelect)

TempFanSelect deals with the relationship between the fan and the temperature source. While reset it is cleared (00_{HEX}).

Location:

TD1FanSelect - Bank 2 Address 01_{HEX}
TD2FanSelect - Bank 2 Address 02_{HEX}
TD3FanSelect - Bank 2 Address 03_{HEX}
TD4FanSelect - Bank 2 Address 04_{HEX}
TR1FanSelect - Bank 2 Address 05_{HEX}
TR2FanSelect - Bank 2 Address 06_{HEX}

Type: Read / Write

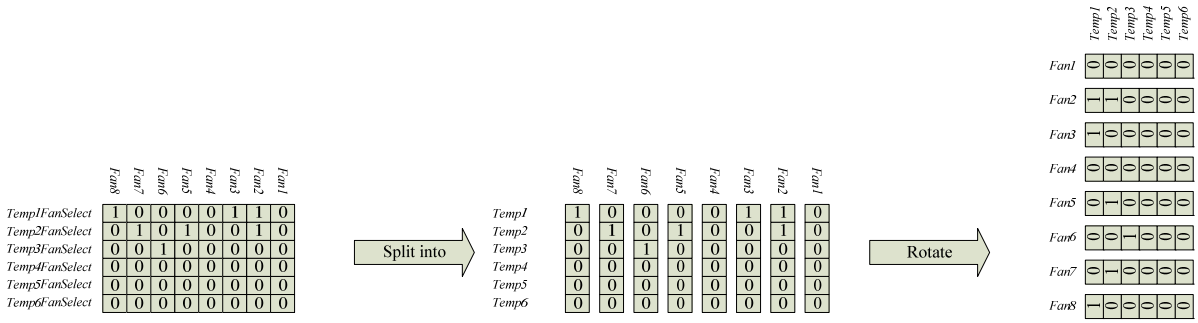
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

TD1FANSELECT ~ TR2FANSELECT

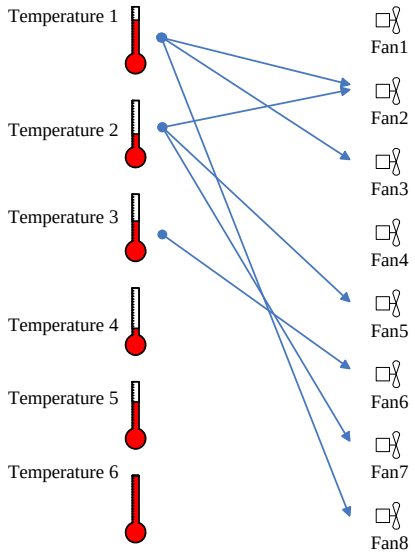
Bit	7	6	5	4	3	2	1	0
Name	**Fan8**	**Fan7**	**Fan6**	**Fan5**	**Fan4**	**Fan3**	**Fan2**	**Fan1**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Fan8** (Enable Fan8 Smart Fan). 0: Fan8 has no relation with this temperature source. 1: Applies SmartFan control on Fan8 and this temperature.
6	**Fan7** (Enable Fan7 Smart Fan). 0: Fan7 has no relation with this temperature source. 1: Applies SmartFan control on Fan7 and this temperature.
5	**Fan6** (Enable Fan6 Smart Fan). 0: Fan6 has no relation with this temperature source. 1: Applies SmartFan control on Fan6 and this temperature.
4	**Fan5** (Enable Fan5 Smart Fan). 0: Fan5 has no relation with this temperature source. 1: Applies SmartFan control on Fan5 and this temperature.
3	**Fan4** (Enable Fan4 Smart Fan). 0: Fan4 has no relation with this temperature source. 1: Applies SmartFan control on Fan4 and this temperature.
2	**Fan3** (Enable Fan3 Smart Fan). 0: Fan3 has no relation with this temperature source. 1: Applies SmartFan control on Fan3 and this temperature.
1	**Fan2** (Enable Fan2 Smart Fan). 0: Fan2 has no relation with this temperature source. 1: Applies SmartFan control on Fan2 and this temperature.
0	**Fan1** (Enable Fan1 Smart Fan). 0: Fan1 has no relation with this temperature source. 1: Applies SmartFan control on Fan1 and this temperature.

The following example explains the concept of **TempFanSelect** Mapping. In this case, **TD1FanSelect** is set to 86_{HEX}; **TD2FanSelect** is set to 52_{HEX}; **TD3FanSelect** is set 20_{HEX}, and the other 3 are left unset.



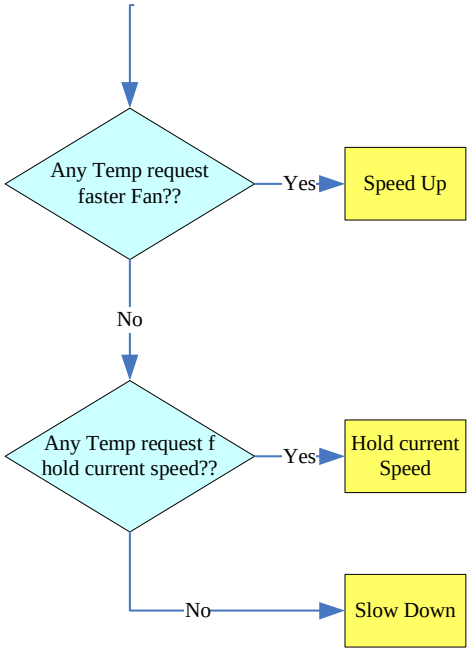
Splitting and rotating the six registers bit by bit as the figure above helps to understand the relationship better. For the rows of Fan1 and Fan4, all of the temperatures are de-asserted, which means Fan1/Fan4 and the temperature are irrelevant. Thus they are in the manual mode under this setting. For Fan2, it is clear that it is relative to temperature 1 and 2, so it will activate SmartFan control with temperature 1/2 as its input.



The right graph gives a picture of how the mapping relationship is made by this setting.

In this example, Fan2 retrieves information from Temperature 1 and Temperature 2, and decides the next duty cycle applied to Fan2. To speed up or to slow down the fan is based on the analysis of the W83793G. Basically, the W83793G sorts and analyzes the information from each temperature sensor and SmartFan Controls. The analysis may be like, “TD1 needs to speed up the fan”; “TD2 does not need so fast fan speed”; “TD1 does not need fast fans any more”, and “TD2 hopes to keep the current fan speed”. Then, the algorithm will make a decision to control the fan by the following simple rule.

If TD1 says, “I need a faster fan”, and TD2 says, “No fast fan needed”. The W83793G will take request of TD1 short, the W83793G request and applies and start to speed up the fan. In always takes the most critical it to the related fan.



8.11.2.11. SmartFan Control Mode Select Register (FanCtrlMode)

Once the SmartFan function is enabled, the W83793G supports two SmartFan modes, Thermal Cruise mode and SMART FAN™II mode (Please refer to **TempFanSelect** to enable SmartFan Function). While reset it is cleared (00_{HEX}), and is in the SMART FAN™II mode.

Location: **FanCtrlMode** - Bank 2 Address 07_{HEX}

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,

SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

FANCTRLMODE

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**TR2_MD**	**TR1_MD**	**TD4_MD**	**TD3_MD**	**TD2_MD**	**TD1_MD**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	Reserved.
5	**TR2_MD** (Thermistor 2 SmartFan Control Mode) 0: SMART FAN^{TM}II Mode. 1: Thermal Cruise Mode.
4	**TR1_MD** (Thermistor 1 SmartFan Control Mode) 0: SMART FAN^{TM}II Mode. 1: Thermal Cruise Mode.
3	**TD4_MD** (Thermal Diode 4 SmartFan Control Mode) 0: SMART FAN^{TM}II Mode. 1: Thermal Cruise Mode.
2	**TD3_MD** (Thermal Diode 3 SmartFan Control Mode) 0: SMART FAN^{TM}II Mode. 1: Thermal Cruise Mode.
1	**TD2_MD** (Thermal Diode 2 SmartFan Control Mode) 0: SMART FAN^{TM}II Mode. 1: Thermal Cruise Mode.
0	**TD1_MD** (Thermal Diode 1 SmartFan Control Mode) 0: SMART FAN^{TM}II Mode. 1: Thermal Cruise Mode.

8.11.2.12. Hysteresis Tolerance of Temperature Register (TolTemp)

In SMART FAN^{TM} mode, to prevent unstable temperatures from throttling the fan speed, the W83793G employs a hysteresis temperature to separate the speed-up/slow-down temperature points. While reset it is set to 2℃ (22_{HEX}).

Location:

TolTD12 - Bank 2 Address 08_{HEX}
TolTD34 - Bank 2 Address 09_{HEX}
TolTR12 - Bank 2 Address $0A_{HEX}$

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

TOLTD12

Bit	7	6	5	4	3	2	1	0
Name	**TolTD2**				**TolTD1**			
Reset	2_{HEX}				2_{HEX}			

Bit	Description
7-4	**TolTD2** (TD 2 Tolerance Range). Unit in ℃.
3-0	**TolTD1** (TD 1 Tolerance Range). Unit in ℃.

TOLTD34

Bit	7	6	5	4	3	2	1	0
Name	**TolTD4**				**TolTD3**			
Reset	2_{HEX}				2_{HEX}			

Bit	Description
7-4	**TolTD4** (TD 4 Tolerance Range). Unit in ℃.
3-0	**TolTD3** (TD 3 Tolerance Range). Unit in ℃.

TOLTR12

Bit	7	6	5	4	3	2	1	0
Name	**TolTR2**				**TolTR1**			
Reset	2_{HEX}				2_{HEX}			

Bit	Description
7-4	**TolTR2** (TR2 Tolerance Range). Unit in ℃.
3-0	**TolTR1** (TR1 Tolerance Range). Unit in ℃.

8.11.2.13. Fan Output Nonstop Duty Cycle Register (FanNonStop)

It takes some time to bring a fan from still to working state. Therefore, FanNonStop is designed with a minimum duty cycle to keep the fan working when the system does not require the fan to help reduce heat but still want to keep the fast response time to speed up the fan. (Please refer to Graph)

Location:

Fan1NonStop - Bank 2 Address 18_{HEX}

Fan2NonStop - Bank 2 Address 19_{HEX}

Fan3NonStop - Bank 2 Address $1A_{HEX}$

Fan4NonStop - Bank 2 Address $1B_{HEX}$

Fan5NonStop - Bank 2 Address $1C_{HEX}$
Fan6NonStop - Bank 2 Address $1D_{HEX}$
Fan7NonStop - Bank 2 Address $1E_{HEX}$
Fan8NonStop - Bank 2 Address $1F_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

FANNONSTOP

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**FanNonStop**					
Reset	0		4_{HEX}					

Bit	Description
7-6	Reserved.
5-0	**FanNonStop**(Fan Output NonStop Duty Cycle).

8.11.2.14. Fan Output Start Duty Cycle Register (FanStart)

From still to rotate, the fan usually needs a higher duty cycle to generate enough torque to conquer the restriction force. Thus the W83793G includes a FanStart to turn on the fan with the specified duty. (Please refer to Graph)

Location:
Fan1Start - Bank 2 Address 20_{HEX}
Fan2Start - Bank 2 Address 21_{HEX}
Fan3Start - Bank 2 Address 22_{HEX}
Fan4Start - Bank 2 Address 23_{HEX}
Fan5Start - Bank 2 Address 24_{HEX}
Fan6Start - Bank 2 Address 25_{HEX}
Fan7Start - Bank 2 Address 26_{HEX}
Fan8Start - Bank 2 Address 27_{HEX}
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

FANSTART

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**FanStart**					
Reset	0		8_{HEX}					

Bit	Description

Bit	Description
7-6	Reserved.
5-0	**FanStart**(Fan Output Start Duty Cycle).

8.11.2.15. Fan Output Stop Time Register (FanStopTime)

A time interval is specified to tell the W83793G when to turn off the fan if SmartFan continuously requests to slow down the fan which has already reached the **NonStop** Level. The default is 10 sec. (Please refer to Graph)

Location:

Fan1StopTime - Bank 2 Address 28_{HEX}
Fan2StopTime - Bank 2 Address 29_{HEX}
Fan3StopTime - Bank 2 Address $2A_{HEX}$
Fan4StopTime - Bank 2 Address $2B_{HEX}$
Fan5StopTime - Bank 2 Address $2C_{HEX}$
Fan6StopTime - Bank 2 Address $2D_{HEX}$
Fan7StopTime - Bank 2 Address $2E_{HEX}$
Fan8StopTime - Bank 2 Address $2F_{HEX}$

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

FANSTOPTIME

Bit	7	6	5	4	3	2	1	0
Name	**FanStopTime**							
Reset	64_{HEX}							

Bit	Description
7-0	**FanStopTime** (Fan Stop time from Nonstop level to the off state). Unit in 0.1sec. Ranges from 0.1sec to 25.5sec. If set to 0, the fan will never stop.

8.11.2.16. Target Temperature of Temperature Inputs Register (TempTarget)

In Thermal Cruise mode, each temperature source has to have a target temperature. The W83793G will try to tune the fan speed to keep the temperature of the target device around the target temperature. The default target temperature for diode sensors is 40℃, and 32℃ for thermistor sensors.

Location:

TD1Target - Bank 2 Address 10_{HEX}
TD2Target - Bank 2 Address 11_{HEX}
TD3Target - Bank 2 Address 12_{HEX}
TD4Target - Bank 2 Address 13_{HEX}
TR1Target - Bank 2 Address 14_{HEX}
TR2Target - Bank 2 Address 15_{HEX}

Type: Read / Write

Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

TD1TARGET ~ TD4TARGET

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TempTarget**						
Reset	0	28_{HEX}						

Bit	Description
7	Reserved.
6-0	**TempTarget**. (the target temperature of the Diode Temperature sensor). Unit in ℃

TR1TARGET ~ TR2TARGET

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TempTarget**						
Reset	0	20_{HEX}						

Bit	Description
7	Reserved.
6-0	**TempTarget**. (the target temperature of the Thermistor Temperature sensor). Unit in ℃

See also: TolTemp, FanCtrlMode, Thermal Cruise mode.

8.11.2.17. SMART FAN™II Fan Transition Temperature Level Registers (TempLevel)

SMART FAN™II is an algorithm providing a table mapping mechanism to translate the temperature information into output fan duties. The mapping table requires 2 domains for the translation. In the table, a certain temperature corresponds to a certain duty. **TempLevel** (Temperature) and **TempFanLevel** (Duty Cycle) are used to define the table. There are totally six tables reside in the W83793G, one table per temperature channel and 7 entries per table. Therefore, **TempLevel** will have 42 registers, and another 42 registers for **TempFanLevel** in this and next section.

Location:

TD1Level01 - Bank 2 Address 30_{HEX}
TD1Level12 - Bank 2 Address 31_{HEX}
TD1Level23 - Bank 2 Address 32_{HEX}
TD1Level34 - Bank 2 Address 33_{HEX}
TD1Level45 - Bank 2 Address 34_{HEX}
TD1Level56 - Bank 2 Address 35_{HEX}
TD1Level67 - Bank 2 Address 36_{HEX}

TD2Level01 - Bank 2 Address 40_{HEX}
TD2Level12 - Bank 2 Address 41_{HEX}
TD2Level23 - Bank 2 Address 42_{HEX}
TD2Level34 - Bank 2 Address 43_{HEX}
TD2Level45 - Bank 2 Address 44_{HEX}
TD2Level56 - Bank 2 Address 45_{HEX}
TD2Level67 - Bank 2 Address 46_{HEX}

TD3Level01 - Bank 2 Address 50_{HEX}
TD3Level12 - Bank 2 Address 51_{HEX}
TD3Level23 - Bank 2 Address 52_{HEX}
TD3Level34 - Bank 2 Address 53_{HEX}
TD3Level45 - Bank 2 Address 54_{HEX}
TD3Level56 - Bank 2 Address 55_{HEX}
TD3Level67 - Bank 2 Address 56_{HEX}

TD4Level01 - Bank 2 Address 60_{HEX}
TD4Level12 - Bank 2 Address 61_{HEX}
TD4Level23 - Bank 2 Address 62_{HEX}
TD4Level34 - Bank 2 Address 63_{HEX}
TD4Level45 - Bank 2 Address 64_{HEX}
TD4Level56 - Bank 2 Address 65_{HEX}
TD4Level67 - Bank 2 Address 66_{HEX}

TR1Level01 - Bank 2 Address 70_{HEX}
TR1Level12 - Bank 2 Address 71_{HEX}
TR1Level23 - Bank 2 Address 72_{HEX}
TR1Level34 - Bank 2 Address 73_{HEX}
TR1Level45 - Bank 2 Address 74_{HEX}
TR1Level56 - Bank 2 Address 75_{HEX}
TR1Level67 - Bank 2 Address 76_{HEX}

TR2Level01 - Bank 2 Address 80_{HEX}
TR2Level12 - Bank 2 Address 81_{HEX}
TR2Level23 - Bank 2 Address 82_{HEX}
TR2Level34 - Bank 2 Address 83_{HEX}
TR2Level45 - Bank 2 Address 84_{HEX}
TR2Level56 - Bank 2 Address 85_{HEX}
TR2Level67 - Bank 2 Address 86_{HEX}

Type: Read / Write

Reset:

VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

TD1LEVEL01 ~ TR2LEVEL01

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TempLevel01**						
Reset	0	$1E_{HEX}$						

Bit	Description
7	Reserved.
6-0	**TempLevel01**. (Temperature Level between TempFanLevel0 and TempFanLevel1). Unit in ℃

TD1LEVEL12 ~ TR2LEVEL12

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TempLevel12**						
Reset	0	23_{HEX}						

Bit	Description
7	Reserved.
6-0	**TempLevel12**. (Temperature Level between TempFanLevel1 and TempFanLevel2). Unit in ℃

TD1LEVEL23 ~ TR2LEVEL23

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TempLevel23**						
Reset	0	28_{HEX}						

Bit	Description
7	Reserved.
6-0	**TempLevel23**. (Temperature Level between TempFanLevel2 and TempFanLevel3). Unit in ℃

TD1LEVEL34 ~ TR2LEVEL34

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TempLevel34**						
Reset	0	$2D_{HEX}$						

Bit	Description

Bit	Description
7	Reserved.
6-0	**TempLevel34**. (Temperature Level between TempFanLevel3 and TempFanLevel4). Unit in ℃

TD1LEVEL45 ~ TR2LEVEL45

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TempLevel45**						
Reset	0	32_{HEX}						

Bit	Description
7	Reserved.
6-0	**TempLevel45**. (Temperature Level between TempFanLevel4 and TempFanLevel5). Unit in ℃

TD1LEVEL56 ~ TR2LEVEL56

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TempLevel56**						
Reset	0	37_{HEX}						

Bit	Description
7	Reserved.
6-0	**TempLevel56**. (Temperature Level between TempFanLevel5 and TempFanLevel6). Unit in ℃

TD1LEVEL67 ~ TR2LEVEL67

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TempLevel67**						
Reset	0	$3C_{HEX}$						

Bit	Description

Bit	Description
7	Reserved.
6-0	**TempLevel67**. (Temperature Level between TempFanLevel6 and TempFanLevel7). Unit in ℃

See also: TolTemp, FanCtrlMode, Smart Fan II mode.

8.11.2.18. Smart Fan II Fan Output Levels Registers (TempFanLevel)

The previous section describes one temperature axis of SMART FAN™II Table. Here introduced Fan Duty axis for the table, **TempFanLevel** registers.

Location:

TD1FanLevel0 - Bank 2 Address 38_{HEX}
TD1FanLevel1 - Bank 2 Address 39_{HEX}
TD1FanLevel2 - Bank 2 Address $3A_{HEX}$
TD1FanLevel3 - Bank 2 Address $3B_{HEX}$
TD1FanLevel4 - Bank 2 Address $3C_{HEX}$
TD1FanLevel5 - Bank 2 Address $3D_{HEX}$
TD1FanLevel6 - Bank 2 Address $3E_{HEX}$

TD2FanLevel0 - Bank 2 Address 48_{HEX}
TD2FanLevel1 - Bank 2 Address 49_{HEX}
TD2FanLevel2 - Bank 2 Address $4A_{HEX}$
TD2FanLevel3 - Bank 2 Address $4B_{HEX}$
TD2FanLevel4 - Bank 2 Address $4C_{HEX}$
TD2FanLevel5 - Bank 2 Address $4D_{HEX}$
TD2FanLevel6 - Bank 2 Address $4E_{HEX}$

TD3FanLevel0 - Bank 2 Address 58_{HEX}
TD3FanLevel1 - Bank 2 Address 59_{HEX}
TD3FanLevel2 - Bank 2 Address $5A_{HEX}$
TD3FanLevel3 - Bank 2 Address $5B_{HEX}$
TD3FanLevel4 - Bank 2 Address $5C_{HEX}$
TD3FanLevel5 - Bank 2 Address $5D_{HEX}$
TD3FanLevel6 - Bank 2 Address $5E_{HEX}$

TD4FanLevel0 - Bank 2 Address 68_{HEX}
TD4FanLevel1 - Bank 2 Address 69_{HEX}
TD4FanLevel2 - Bank 2 Address $6A_{HEX}$
TD4FanLevel3 - Bank 2 Address $6B_{HEX}$
TD4FanLevel4 - Bank 2 Address $6C_{HEX}$
TD4FanLevel5 - Bank 2 Address $6D_{HEX}$
TD4FanLevel6 - Bank 2 Address $6E_{HEX}$

TR1FanLevel0 - Bank 2 Address 78_{HEX}
TR1FanLevel1 - Bank 2 Address 79_{HEX}
TR1FanLevel2 - Bank 2 Address $7A_{HEX}$
TR1FanLevel3 - Bank 2 Address $7B_{HEX}$
TR1FanLevel4 - Bank 2 Address $7C_{HEX}$
TR1FanLevel5 - Bank 2 Address $7D_{HEX}$
TR1FanLevel6 - Bank 2 Address $7E_{HEX}$

TR2FanLevel0 - Bank 2 Address 88_{HEX}
TR2FanLevel1 - Bank 2 Address 89_{HEX}
TR2FanLevel2 - Bank 2 Address $8A_{HEX}$
TR2FanLevel3 - Bank 2 Address $8B_{HEX}$
TR2FanLevel4 - Bank 2 Address $8C_{HEX}$
TR2FanLevel5 - Bank 2 Address $8D_{HEX}$
TR2FanLevel6 - Bank 2 Address $8E_{HEX}$

Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set,
SYSRSTIN_N (Pin 15) Falling @ SYSRST_MD (CR40.Bit5) set.

TD1FANLEVEL0 ~ TR2FANLEVEL0

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**TempFanLevel0**					
Reset	0		08_{HEX}					

Bit	Description
7-6	Reserved.
5-0	**TempFanLevel0**. (Fan Output Level 0).

TD1FANLEVEL1 ~ TR2FANLEVEL1

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**TempFanLevel1**					
Reset	0		$0C_{HEX}$					

Bit	Description
7-6	Reserved.
5-0	**TempFanLevel1**. (Fan Output Level 1).

TD1FANLEVEL2 ~ TR2FANLEVEL2

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**TempFanLevel2**					
Reset	0		10_{HEX}					

Bit	Description
7-6	Reserved.
5-0	**TempFanLevel2**. (Fan Output Level 2).

TD1FANLEVEL3 ~ TR2FANLEVEL3

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**TempFanLevel3**					
Reset	0		18_{HEX}					

Bit	Description
7-6	Reserved.
5-0	**TempFanLevel3**. (Fan Output Level 3).

TD1FANLEVEL4 ~ TR2FANLEVEL4

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**TempFanLevel4**					
Reset	0		20_{HEX}					

Bit	Description
7-6	Reserved.
5-0	**TempFanLevel4**. (Fan Output Level 4).

TD1FANLEVEL5 ~ TR2FANLEVEL5

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**TempFanLevel5**					
Reset	0		30_{HEX}					

Bit	Description
7-6	Reserved.
5-0	**TempFanLevel5**. (Fan Output Level 5).

TD1FANLEVEL6 ~ TR2FANLEVEL6

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**TempFanLevel6**					
Reset	0		38_{HEX}					

Bit	Description
7-6	Reserved.
5-0	**TempFanLevel6**. (Fan Output Level 6).

See also: TolTemp, FanCtrlMode, Smart Fan II mode.

8.12 PECI Control Registers

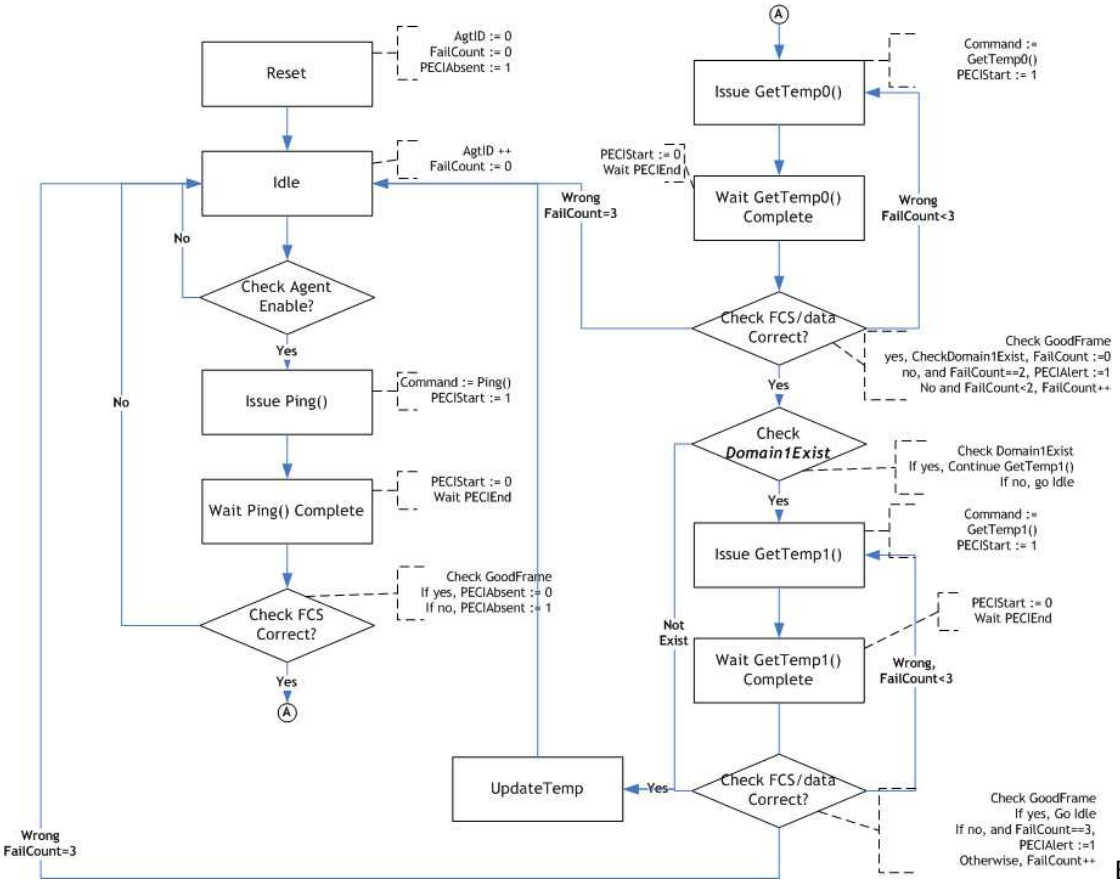
Intel® new generation CPUs such as Presler begin to support new single wire digital temperature monitoring interface which is called Platform Environment Control Interface or PECI. The W83793G supports the PECI* version 1.0 for these new generation CPUs. All PECI control registers are located in Bank 0. Pin 1, PCLK, is the timing base of PECI control circuit. If PECI function is needed, Pin 1 is required to feed a 48MHz clock.

The W83793G PECI configuration, including the PECI address and number of domains, must match the CPU type. BIOS have to detect which kind of CPU it is and program the correct configuration in the W83793G.

8.12.1 PECI Register Map

Mnemonic	Register Name	Type
AgtConfig	Agent Configuration Register	RW
Agt1Tcase | **Agt4Tcase**	Tcase Register	RW
ReportStyle	PECI Report Temperature Style Register	RW
PECIWarning	PECI Warning Flag Register	RO
Agt1RelTempH/L | **Agt4RelTempH/L**	Agent Relative Temperature Registers	RO

Three control registers and 2 status registers are listed here. The detailed operation of the PECI host is shown in the figure below.



Every time the W83793G PECI host detects that the user enables an agent by setting **AgtEn**, it start to Ping. If the client exists, it continues to issue GetTemp0 or GetTemp1 (when **DM1Exist** is asserted). If there is no client, it sets a **PECIAbsent** flag to inform the host. A fault queue is made to ensure that the host can obtain correct temperatures. However, consecutive 3 FCS errors indicate that the data is invalid. The PECI warning flag will be set.

8.12.2 PECI Register Details

8.12.2.1. Agent Configuration Register (AgtConfig)

This register commands the PECI host to process related agents and domains. Only the agent or domain specified in this register will process PECI transactions. It is reset to 00_{HEX}.

Location: **AgtConfig** - Bank 0 Address $D0_{HEX}$
Type: Read Write
Reset: VSB5V (Pin 7) Rising,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set.

AGTCONFIG

Bit	7	6	5	4	3	2	1	0
Name	**Agt4EN**	**Agt3EN**	**Agt2EN**	**Agt1EN**	**Agt4D1**	**Agt3D1**	**Agt2D1**	**Agt1D1**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Agt4EN** (Agent 4 Enable Bit). 0_{BIN}: Agent 4 is disabled. 1_{BIN}: Agent 4 is enabled.
6	**Agt3EN** (Agent 3 Enable Bit). 0_{BIN}: Agent 3 is disabled. 1_{BIN}: Agent 3 is enabled.
5	**Agt2EN** (Agent 2 Enable Bit). 0_{BIN}: Agent 2 is disabled. 1_{BIN}: Agent 2 is enabled.
4	**Agt1EN** (Agent 1 Enable Bit). 0_{BIN}: Agent 1 is disabled. 1_{BIN}: Agent 1 is enabled.
3	**Agt4D1** (Agent 4 Domain 1 Enable Bit). 0_{BIN}: Agent 4 does not have domain 1. 1_{BIN}: Agent 4 has domain 1.
2	**Agt3D1** (Agent 3 Domain 1 Enable Bit). 0_{BIN}: Agent 3 does not have domain 1. 1_{BIN}: Agent 3 has domain 1.
1	**Agt2D1** (Agent 2 Domain 1 Enable Bit). 0_{BIN}: Agent 2 does not have domain 1. 1_{BIN}: Agent 2 has domain 1.
0	**Agt1D1** (Agent 1 Domain 1 Enable Bit). 0_{BIN}: Agent 1 does not have domain 1. 1_{BIN}: Agent 1 has domain 1.

8.12.2.2. Agent TCase Register (AgtTcase)

Intel® CPU introduces a Tcase concept on the temperature management. In Presler generation CPUs, Tcase can be read from the CPU register by BIOS and refills the value to the W83793G registers. The default setting is 70℃, which is 10℃ higher than TempLevel67. In later generation CPUs, the CPU might only respond with the Tcase value as an offset temperature to PROCHOT# assertion. It is reset to 46_{HEX}.

Location:
Agt1TCase - Bank 0 Address $D1_{HEX}$ **Agt3TCase** - Bank 0 Address $D3_{HEX}$
Agt2TCase - Bank 0 Address $D2_{HEX}$ **Agt4TCase** - Bank 0 Address $D4_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set.

AGT1TCASE~AGT4TCASE

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TCase Temperature**						
Reset	0	1	0	0	0	1	1	0

Bit	Description
7	Reserved.
6-0	**TCase**(TCase Temperature Setting). TCase must always be a positive value; a negative value will introduce abnormal temperature response.

8.12.2.3. PECI Report Temperature Style Register (ReportStyle)

ReportStyle controls which value to be loaded into Absolute Temp or Relative Temp.

If RtHigh = 1, the PECI host will automatically compare the highest temperature domain and load it into Abs/Rel-Temp. If **RtHigh** = 0, **RtDm** will return Domain 0 temperature to the W83793G if the register is set to 0, and return Domain 1 temperature to the W83793G if the register is set to 1. It is reset to 00_{HEX}.

Location: **ReportStyle** - Bank 0 Address $D5_{HEX}$
Type: Read / Write
Reset: VSB5V (Pin 7) Rising,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set.

REPORTSTYLE

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**RtHigh**	**RTD4**	**RTD3**	**RTD2**	**RTD1**

Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	Reserved.
4	**RtHigh** (Return High Temperature). 0_{BIN}: Return the domain temperature by RTD selection (RTD1~RTD4). 1_{BIN}: Return the highest temperature in the same agent.
3	**RtD4** (Agent 4 Return Domain 1 Enable Bit). Only takes effect when RtHigh deasserts. 0_{BIN}: Agent 4 always returns the temperature from domain 0. 1_{BIN}: Agent 4 always returns the temperature from domain 1.
2	**RtD3** (Agent 3 Return Domain 1 Enable Bit). Only takes effect when RtHigh deasserts. 0_{BIN}: Agent 3 always returns the temperature from domain 0. 1_{BIN}: Agent 3 always returns the temperature from domain 1.
1	**RtD2** (Agent 2 Return Domain 1 Enable Bit). Only takes effect when RtHigh deasserts. 0_{BIN}: Agent 2 always returns the temperature from domain 0. 1_{BIN}: Agent 2 always returns the temperature from domain 1.
0	**RtD1** (Agent 1 Return Domain 1 Enable Bit). Only takes effect when RtHigh deasserts. 0_{BIN}: Agent 1 always returns the temperature from domain 0. 1_{BIN}: Agent 1 always returns the temperature from domain 1.

8.12.2.4. PECI Warning Flag Register (PECIWarning)

Few warnings may be generated when the PECI protocol is applied. First, the PECI host may not be able to detect a PECI Client (or the client does not respond to the host Ping() command). In this case, PECI issues a flag called “Absent” to inform users that it cannot detect the client. Another case is that the PECI Client returns invalid FCS in successive 3 time polling; the host will issue an Alert flag. It is reset to 00_{HEX}.

Location: **PECIWarning** - Bank 0 Address $D6_{HEX}$
Type: Read Only
Reset: VSB5V (Pin 7) Rising,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set.

PECIWARNING

Bit	7	6	5	4	3	2	1	0
Name	**Absent4**	**Absent3**	**Absent2**	**Absent1**	**Alert4**	**Alert3**	**Alert2**	**Alert1**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Absent4** (PECI Agent 4 Absent Bit). 0_{BIN}: Agent 4 is detected.

Bit	Description
	1_{BIN}: Agent 4 cannot be detected.
6	**Absent3** (PECI Agent 3 Absent Bit). 0_{BIN}: Agent 3 is detected. 1_{BIN}: Agent 3 cannot be detected.
5	**Absent2** (PECI Agent 2 Absent Bit). 0_{BIN}: Agent 2 is detected. 1_{BIN}: Agent 2 cannot be detected.
4	**Absent1** (PECI Agent 1 Absent Bit). 0_{BIN}: Agent 1 is detected. 1_{BIN}: Agent 1 cannot be detected.
3	**Alert4** (PECI Agent 4 Alert Bit). 0_{BIN}: Agent 4 has good FCS. 1_{BIN}: Agent 4 has bad FCS in last 3 transactions.
2	**Alert3** (PECI Agent 3 Alert Bit). 0_{BIN}: Agent 3 has good FCS. 1_{BIN}: Agent 3 has bad FCS in last 3 transactions.
1	**Alert2** (PECI Agent 2 Alert Bit). 0_{BIN}: Agent 2 has good FCS. 1_{BIN}: Agent 2 has bad FCS in last 3 transactions.
0	**Alert1** (PECI Agent 1 Alert Bit). 0_{BIN}: Agent 1 has good FCS. 1_{BIN}: Agent 1 has bad FCS in last 3 transactions.

While PECI is activated, Alert flag will be asserted when the corresponding agent returns invalid FCS for successive 3 times. In this case, the W83793G will think this agent has problems in the interface, and for safety reason the W83793G will turn on the related fan to full speed in SmartFan mode. The fan and PECI agent relationship is defined in **TempFanSelect** registers.

8.12.2.5. Agent Relative Temperature Register (AgtRelTemp)

These registers return the raw data retrieved from PECI. The data may be the error code (range: 8000H~81FFH) or relative temperatures to process the defined **Tcase**. The error code will only be update in **AgtRelTemp**, Absolute Temperature will not be updated when the error code is received. If the **ReturnHigh** mechanism is activated, the normal temperature will always be returned first. In case both 2 domains return errors, the return priority will be Overflow Error > Underflow Error > Missing Diode > General Error. The reset value is $8001_{HEX,}$ in that PECI is defaulted to be off. In PECI, 8001_{HEX} means the diode is missing.

Location:

Agt1RelTempH - Bank 0 Address $D8_{HEX}$
Agt1RelTempL - Bank 0 Address $D9_{HEX}$
Agt2RelTempH - Bank 0 Address DA_{HEX}
Agt2RelTempL - Bank 0 Address DB_{HEX}
Agt3RelTempH - Bank 0 Address DC_{HEX}
Agt3RelTempL - Bank 0 Address DD_{HEX}
Agt4RelTempH - Bank 0 Address DE_{HEX}
Agt4RelTempL - Bank 0 Address DF_{HEX}

Type: Read Only

Reset: VSB5V (Pin 7) Rising,
VDD5V (Pin 25) Rising @ RST_VDD_MD (CR40.Bit4) set.

AGT1RELTEMPH/L~AGT4RELTEMPH/L

Bit	7	6	5	4	3	2	1	0
Name	**Sign**	**Temperature[8:2]**						
Reset	1	0	0	0	0	0	0	0
Name	**Temperature[1:0]**		**TEMP_2**	**TEMP_4**	**TEMP_8**	**TEMP_16**	**TEMP_32**	**TEMP_64**
Reset	0	0	0	0	0	0	0	1

Bit	Description
15	**Sign Bit**. In PECI Protocol, this bit should always be 1 to represent a negative temperature.
14-6	Temperature The integer part of the relative temperature.
5	**TEMP_2**. 0.5℃ unit.
4	**TEMP_4**. 0.25℃ unit.
3	**TEMP_8**. 0.125℃ unit.
2	**TEMP_16**. 0.0625℃ unit.
1	**TEMP_32**. 0.03125℃ unit.
0	**TEMP_64**. 0.015625℃ unit.

On some occasions, PECI will return the abnormal states of the PECI bus in addition to the temperature. All the information will be recorded in AgtRelTemp. In some cases, the W83793G will also do further processing for the alert mechanism. The following describes these codes and their effects to the W83793G.

Error Code	Description	W83793G host operation
8000_{HEX}	General Sensor Error	No further processing.
8001_{HEX}	Sensing Device Missing	
8002_{HEX}	Operational, but the temperature is lower than the sensor operation range.	Compulsorily write 0℃ back to the temperature readouts.(Bank 0 Index $1C_{HEX}$ ~ $1F_{HEX}$)
8003_{HEX}	Operational, but the temperature is higher than the sensor operation range.	compulsorily write 127℃ back to the temperature readouts.(Bank 0 Index $1C_{HEX}$ ~ $1F_{HEX}$)
8004_{HEX} $81FF_{HEX}$	Reserved.	No further operation.

Besides error conditions or invalid FCS, the normal temperature will be written back to Temperature Readouts with the sum of AgtRelTemp value and Tcase value.

8.13 ASF Control Registers

ASF or Alert Standard Format provides remote system abilities to monitor, discover and manage the local platform. All ASF control registers are located in Bank 1*.

*About the Bank Selection, please refer to the Bank Select register located at address $00_{Hex.}$

8.13.1 ASF Register Map

8.13.1.1. SMBus ARP UDID Control Registers

Mnemonic	Register Name	Type
UDIDDevCap.	UDID Device Capability Register	RO
UDIDVersion.	UDID Version Number Register	RO
UDIDVendorH. UDIDVendorL.	UDID Vendor ID High/Low Byte Register	RO
UDIDDevH. UDIDDevL.	UDID Device ID High/Low Byte Register	RW
UDIDIFH. UDIDIFL.	UDID Interface High/Low Byte Register	RW
UDIDSubVenH. UDIDSubVenL.	UDID Subsystem Vendor ID High/Low Byte Registers	RW
UDIDSubDevH. UDIDSubDevL.	UDID Subsystem Device ID High/Low Byte Registers	RW
UDIDSpeID1. UDIDSpeID4.	UDID Vendor Specific ID Byte 1~4	RW
RNG1. RNG4.	Random Number Generator Byte 1~4	RO
ASFAddr.	ASF Assigned Address Register	RO

Before activating ASF, the user must go through the ARP (Address Resolution Protocol) to dynamically obtain a valid address to manipulate ASF commands. In ARP, it is very important that UDID (Unique Device Identifier) is defined to distinguish different devices. Registers in this section are used to set up UDID.

For detailed operation of ARP and UDID, please refer to SMBus Specification version 2.0 (http://www.smbus.org/specs/smbus20.pdf) section 5.6 in page 34.

8.13.1.2. ASF Sensor Entity Definition Registers

In ASF Sensor, each sensor channel has 2 parameters, entity Instance and entity ID, to tell the ASF host its related location information on the platform. If the user uses the temperature sensor in locations different from the default, the W83793G provides all channel parameters that can be programmed to fit customers' application.

Mnemonic	Register Name	Type
VCA_ENTY.	VCoreA Entity ID Register	RW

VCB_ENTY.	VCoreB Entity ID Register	RW
Vtt_ENTY.	Vtt Entity ID Register	RW
VDD_ENTY.	VDD Entity ID Register	RW
VSB_ENTY.	VSB Entity ID Register	RW
VBAT_ENTY.	VBAT Entity ID Register	RW
VSEN1_ENTY. VSEN4_ENTY.	VSEN1~VSEN4 Entity ID Register	RW
FAN1_ENTY. FAN12_ENTY.	FAN1~FAN12 Entity ID Register	RW
TD1_ENTY. TR2_ENTY.	TD1~TR2 Entity ID Register	RW
CHS_ENTY.	Chassis Entity Register	RW

For details of entity ID, please refer to Platform Event Trap Format Specification Version 1.0 Table 6 in page 13.

Mnemonic	Register Name	Type
ENTINS1.	VCoreA/VCoreB Entity Instance Register	RW
ENTINS2.	VDD/Vtt Entity Instance Register	RW
ENTINS3.	VBAT/VSB Entity Instance Register	RW
ENTINS4.	VIN1/VIN2 Entity Instance Register	RW
ENTINS5.	VIN3/VIN4 Entity Instance Register	RW
ENTINS6.	FAN1/FAN2 Entity Instance Register	RW
ENTINS7.	FAN3/FAN4 Entity Instance Register	RW

ENTINS8.	FAN5/FAN6 Entity Instance Register	RW
ENTINS9.	FAN7/FAN8 Entity Instance Register	RW
ENTINS10.	FAN9/FAN10 Entity Instance Register	RW
ENTINS11.	FAN11/FAN12 Entity Instance Register	RW
ENTINS12.	TD1/TD2 Entity Instance Register	RW
ENTINS13.	TD3/TD4 Entity Instance Register	RW
ENTINS14.	TR1/TR2 Entity Instance Register	RW
ENTINS15.	Chassis Entity Instance Register	RW

Entity Instance is a sequential number which helps identify the sensor's location. The customer can set preferable sequence orders.

The summary of Entity and Entity Instance is in the following table.

Sensor in W83793G	Event Status Index	Event Sensor Type	Event Number	Entity ID (Programmable)	Entity Instance (Programmable)
VCOREA	00h	02h	01h	03h (Processor)	01h
VCOREB	01h	02h	02h		02h
Vtt	02h	02h	03h		03h
TD1	03h	01h (Temperature)	04h	07h (System Board)	01h
TD2	04h	01h	05h		02h
TD3	05h	01h	06h		03h
TD4	06h	01h	07h		04h
TR1	07h	01h	08h		05h
TR2	08h	01h	09h		06h
5VDD	09h	02h	0Ah		01h
VSB	0Ah	02h	0Bh		02h
VBAT	0Bh	02h	0Ch		03h
VSEN1	0Ch	02h (Voltage)	0Dh		04h

Sensor in W83793G	Event Status Index	Event Sensor Type	Event Number	Entity ID (Programmable)	Entity Instance (Programmable)
VSEN2	0Dh	02h	0Eh		05h
VSEN3	0Eh	02h	0Fh		06h
VSEN4	0Fh	02h	10h		07h
FAN1	10h	04h (Fan)	11h		01h
FAN2	11h	04h	12h		02h
FAN3	12h	04h	13h		03h
FAN4	13h	04h	14h		04h
FAN5	14h	04h	15h		05h
FAN6	15h	04h	16h		06h
FAN7	16h	04h	17h		07h
FAN8	17h	04h	18h		08h
FAN9	18h	04h	19h		09h
FAN10	19h	04h	1Ah		0Ah
FAN11	1Ah	04h	1Bh		0Bh
FAN12	1Bh	04h	1Ch		0Ch
Case OPEN / Intrusion	1Ch	05h (Physical Security)	1Dh	23h (System Chassis)	01h

The channels in light-green can be disabled by multi-function pin selection or control registers.
The channels are described in the following terms according to the status of each channel.

Description	Status	Event Sensor Type	Event Type	Event Offset	Event Severity
TEMPERATURE SENSORS					
Upper-Critical Going High	3h Assert	01h Temperature	01h Threshold-Based	09h	10h Critical
Upper-Critical Going Low				08h	
Upper-Non-critical Going High				07h	08h Non-critical
Upper-Non-critical Going Low				06h	
Lower-Non-critical Going High	2h Deassert			01h	01h Monitor
Lower-Non-critical Going Low				00h	
VOLTAGE SENSORS					
Generic Over Voltage	3h	02h	07h	02h	10h

Description	Status	Event Sensor Type	Event Type	Event Offset	Event Severity
Problem		Voltage	Generic-Severity		
Normal Voltage	2h			07h	01h
Generic Under Voltage Problem	3h			02h	10h
FAN SENSORS					
Normal FAN Speed	2h	04h Fan	07h	07h	01h
Generic FAN Failure	3h			02h	10h
CASEOPEN/ CASE INTRUSION					
Case Intruded	3h	05h Physical Security	6Fh Sensor Specific	00h	10h
Case Normal	2h			80h	01h

8.13.1.3. ASF Remote Control Definition Registers

ASF function in the W83793G also supports Remote Control. This function enables Management Information System (MIS) to remotely power on, power down, or reset the client's computer when there is abnormal operation.

Mnemonic	Register Name	Type
PwrOnOption.	Power On Control Option Register	RW
PwrOnCmd.	Remote Control Power On Command Register	RW
PwrOffCmd.	Remote Control Power Down Command Register	RW
RstCmd.	Remote Control Reset Command Register	RW

The Remote Control function in the W83793G enables MIS to use side-band of Network Interface Controller to send ASF commands with SMBus. The format looks like

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command	A	Write Data	A	PEC	A	P
	Control Device Address	0	0	Control Command	0	Control Data Value	0	CRC Checksum	0	

"S" represents "Start" Cycle of SMBus transaction; "Wr" means "Write" Flag; "A" means "Acknowledge" from the W83793G, and "P" indicates a "Stop" Cycle. Letters in shadow mean responses from the W83793G. Otherwise, it is a host transmitted signal.

The last row above shows the meaning of each data. Control Device Address is the address assigned in the ARP process; Control Command is specified in the above registers. Control Data option is not supported in the W83793G. Thus with any value in this field, the W83793G will perform the same action.

Please refer to Section 5.4 in page 76 and Section 3.2.4.1 in page 33 in Alert Standard Format Specification v2.0 for more details.

8.13.2 ASF Register Details

8.13.2.1. UDID Device Capability Register (UDIDDevCap)

SMBus Specification Working Group intends to use device capability to distinguish the arbitration priority of GeneralGetUDID() first. Thus the very first byte of the UDID is device capability, because SMBus is a MSB first serial protocol and if the client was pulled low, it wins the arbitration. It is set as $C1_{HEX}$.

Location: **UDIDVersion** - Bank 1 Address 20_{HEX}
Type: Read Only
Reset: No Reset.

UDIDDEVCAP

Bit	7	6	5	4	3	2	1	0
Name	**Address Type**		**Reserved**					**PEC**
Reset	1	1	0	0	0	0	0	1

Bit	Description
7-6	Address Type. 00_{BIN}: Fixed address device. It's the highest priority device. 01_{BIN}: Dynamic and persistent address device. 10_{BIN}: Dynamic and volatile address device. If powered-down, the address needs to be reassigned at next power on. The W83793G ASF address will be lost if 5VSB does not exist. 11_{BIN}: Random number device.
5-1	Reserved.
0	PEC Support. 0: PEC (Packet Error Code) is not supported on this device. 1: PEC is supported on this device.

8.13.2.2. UDID Version Number Register (UDIDVersion)

This field defines the version of UDID and Silicon for the W83793G. It is 08_{HEX}.

Location: **UDIDVersion** - Bank 1 Address 21_{HEX}
Type: Read Only
Reset: No Reset

UDIDVERSION

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**UDID Version**			**Silicon Version**		

Fixed	0	0	0	0	1	0	0	0

Bit	Description
7-6	Reserved.
5-3	UDID Version. 000_{BIN}: Reserved. 001_{BIN}: UDID version 1. 010_{BIN}-111_{BIN}: Reserved for future use.
2-0	Silicon Version. For the identification of the W83793G silicon version. 000_{BIN} stands for Version A/B.

8.13.2.3. UDID Vendor ID High/Low Byte Register (UDIDVendorH/L)

This field defines Nuvoton vendor ID. The default is $1050_{HEX.}$

Location: **UDIDVendorH** - Bank 1 Address 22_{HEX}
UDIDVendorL - Bank 1 Address 23_{HEX}

Type: Read Only

Reset: No Reset

UDIDVENDORH

Bit	7	6	5	4	3	2	1	0
Name	**Vendor ID High Byte**							
Fixed	0	0	0	1	0	0	0	0

UDIDVENDORL

Bit	7	6	5	4	3	2	1	0
Name	**Vendor ID Low Byte**							
Fixed	0	1	0	1	0	0	0	0

Bit	Description
15-0	**Nuvoton Vendor ID.**

8.13.2.4. UDID Device ID High/Low Byte Register (UDIDDevH/L)

This field defines Nuvoton device ID. The default is $0100_{HEX.}$

Location:

UDIDDevH - Bank 1 Address 24_{HEX}
UDIDDevL - Bank 1 Address 25_{HEX}
Type: Read Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set.

UDIDDEVH

Bit	7	6	5	4	3	2	1	0
Name	**Device ID High Byte**							
Reset	0	0	0	0	0	0	0	1

UDIDDEVL

Bit	7	6	5	4	3	2	1	0
Name	**Device ID Low Byte**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
15-0	**Nuvoton Device ID.**

8.13.2.5. UDID Interface High/Low Byte Register (UDIDIFH/L)

This field defines SMBus version and the supported protocol. It is reset to $0024_{HEX.}$
Location:
UDIDIFH - Bank 1 Address 26_{HEX}
UDIDIFL - Bank 1 Address 27_{HEX}
Type: Read Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set.

UDIDIFH

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							
Reset	0	0	0	0	0	0	0	0

UDIDIFL

Bit	7	6	5	4	3	2	1	0

Name	Reserved	IPMI	ASF	OEM	SMBus Version			
Reset	0	0	1	0	0	1	0	0

Bit	Description
15-7	Reserved.
6	**IPMI**. This device supports additional interface access capability per IPMI specification. 0: Not supported. 1: Supported.
5	**ASF**. This device supports additional interface access capability per ASF specification. 0: Not supported. 1: Supported.
4	**OEM**. Device supports vendor specific access capability per Subsystem Vendor ID and Subsystem Device ID. 0: Not supported. 1: Supported.
3-0	SMBus Version 0_{HEX}: SMBus 1.0, not ARPable. 1_{HEX}: SMBus 1.1, not ARPable. 4_{HEX}: SMBus 2.0.

8.13.2.6. UDID Subsystem Vendor ID High/Low Byte Register (UDIDSubVenH/L)

This field defines UDID support for Subsystems. If no subsystem is supported, it must be written with 0000_{HEX}. It is reset to $0000_{HEX.}$

Location: **UDIDSubVenH** - Bank 1 Address 28_{HEX}
UDIDSubVenL - Bank 1 Address 29_{HEX}
Type: Read Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set.

UDIDSUBVENH

Bit	7	6	5	4	3	2	1	0
Name	**UDID Subsystem Vendor ID High Byte**							
Reset	0	0	0	0	0	0	0	0

UDIDSUBVENL

Bit	7	6	5	4	3	2	1	0
Name	**UDID Subsystem Vendor ID Low Byte**							

Reset	0	0	0	0	0	0	0	0

Bit	Description
15-0	**UDID subsystem Vendor.**

8.13.2.7. UDID Subsystem Device ID High/Low Byte Register (UDIDSubDevH/L)

This field defines UDID support for Subsystems. If no subsystem is supported, it must be written with 0000_{HEX}. It is reset to $0000_{HEX.}$

Location: **UDIDSubDevH** - Bank 1 Address $2A_{HEX}$
UDIDSubDevL - Bank 1 Address $2B_{HEX}$
Type: Read Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set.

UDIDSUBVENH

Bit	7	6	5	4	3	2	1	0
Name	**UDID Subsystem Device ID High Byte**							
Reset	0	0	0	0	0	0	0	0

UDIDSUBVENL

Bit	7	6	5	4	3	2	1	0
Name	**UDID Subsystem Device ID Low Byte**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
15-0	**UDID subsystem Device ID.**

8.13.2.8. UDID Vendor-Specific ID Register (UDIDSpecID1/2/3/4)

This field defines unique Vendor-Specific ID for different versions of the W83793G. With this field, different W83793G will be identified on the same SMBus interface. This register will be loaded with a random number when receiving the reset signal.

Location:
UDIDSpecID1 - Bank 1 Address $2C_{HEX}$
UDIDSpecID2 - Bank 1 Address $2D_{HEX}$
UDIDSpecID3 - Bank 1 Address $2E_{HEX}$
UDIDSpecID4 - Bank 1 Address $2F_{HEX}$

Type: Read Write
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,
ARP ResetDevice Command.

UDIDSPECID1~UDIDSPECID4

Bit	7	6	5	4	3	2	1	0
Name	**UDID Specific Vendor ID**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
31-0	UDID Vendor-Specific ID.

8.13.2.9. Random Number Generator Register (RNG1/2/3/4)

The W83793G internally generates pseudo random numbers by using CRC generator and internal clock. Due to the deviations of the internal clock, different IC and different power-on time will affect the results of the random numbers. It is reset to $FFFF_{HEX.}$

Location:
RNG4 - Bank 1 Address 30_{HEX}
RNG3 - Bank 1 Address 31_{HEX}
RNG2 - Bank 1 Address 32_{HEX}
RNG1 - Bank 1 Address 33_{HEX}

Type: Read Only
Reset: None.

RNG1~RNG4

Bit	7	6	5	4	3	2	1	0
Name	**Random Number Code**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
31-0	Random Number Code.

8.13.2.10. ASF Assigned Address Register (ASFAddr)

After the ARP host obtains related device UDID, it will start to assign each device for later use. The W83793G will record this assigned address and set it as the default address for ASF transactions. It is reset to $00_{HEX.}$

Location: **ASFAddr** - Bank 1 Address $4F_{HEX}$

Type: Read Only
Reset: VSB5V (Pin 7) Rising,
Init Reset (CR40.Bit7) is set,

ASFADDR

Bit	7	6	5	4	3	2	1	0
Name	**ASF Address**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
31-0	**ASF Address**. This register will be assigned while ARP AssignAddress command issued.

8.13.2.11. ASF Entity/Instance Registers (ENITIY/ENTINS)

The W83793G supports various channels which can be reported to the host through ASF protocol. Each sensor channel is associated with an entity (or location on the motherboard) and entity instance. The Table provides an overall look for these registers.

Location:

VCA_ENTY - Bank 1 Address 50_{HEX}
VCB_ENTY - Bank 1 Address 51_{HEX}
Vtt_ENTY - Bank 1 Address 52_{HEX}
VDD_ENTY - Bank 1 Address 53_{HEX}
VSB_ENTY - Bank 1 Address 54_{HEX}
VBAT_ENTY - Bank 1 Address 55_{HEX}
VSEN1_ENTY - Bank 1 Address 56_{HEX}
VSEN2_ENTY - Bank 1 Address 57_{HEX}
VSEN3_ENTY - Bank 1 Address 58_{HEX}
VSEN4_ENTY- Bank 1 Address 59_{HEX}
FAN1_ENTY - Bank 1 Address $5A_{HEX}$
FAN2_ENTY - Bank 1 Address $5B_{HEX}$
FAN3_ENTY - Bank 1 Address $5C_{HEX}$
FAN4_ENTY - Bank 1 Address $5D_{HEX}$
FAN5_ENTY - Bank 1 Address $5E_{HEX}$
FAN6_ENTY - Bank 1 Address $5F_{HEX}$
FAN7_ENTY - Bank 1 Address 60_{HEX}
FAN8_ENTY - Bank 1 Address 61_{HEX}
FAN9_ENTY - Bank 1 Address 62_{HEX}
FAN10_ENTY - Bank 1 Address 63_{HEX}
FAN11_ENTY - Bank 1 Address 64_{HEX}
FAN12_ENTY - Bank 1 Address 65_{HEX}
TD1_ENTY - Bank 1 Address 66_{HEX}
TD2_ENTY - Bank 1 Address 67_{HEX}
TD3_ENTY - Bank 1 Address 68_{HEX}
TD4_ENTY - Bank 1 Address 69_{HEX}
TR1_ENTY - Bank 1 Address $6A_{HEX}$
TR2_ENTY - Bank 1 Address $6B_{HEX}$
CHS_ENTY - Bank 1 Address $6C_{HEX}$

ENTINS1 - Bank 1 Address 70_{HEX}
ENTINS2 - Bank 1 Address 71_{HEX}
ENTINS3 - Bank 1 Address 72_{HEX}
ENTINS4 - Bank 1 Address 73_{HEX}
ENTINS5 - Bank 1 Address 74_{HEX}
ENTINS6 - Bank 1 Address 75_{HEX}
ENTINS7 - Bank 1 Address 76_{HEX}
ENTINS8 - Bank 1 Address 77_{HEX}
ENTINS9 - Bank 1 Address 78_{HEX}
ENTINS10 - Bank 1 Address 79_{HEX}
ENTINS11 - Bank 1 Address $7A_{HEX}$
ENTINS12 - Bank 1 Address $7B_{HEX}$
ENTINS13 - Bank 1 Address $7C_{HEX}$
ENTINS14 - Bank 1 Address $7D_{HEX}$

ENTINS15 - Bank 1 Address $7E_{HEX}$

Type: Read / Write
Reset: 5VSB (Pin 7) Rising.

VCA_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**VCore A Entity ID.**							
Reset	03_{HEX}							

VCB_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**VCore B Entity ID.**							
Reset	03_{HEX}							

VTT_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**Vtt Entity ID.**							
Reset	03_{HEX}							

VDD_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**VDD Entity ID.**							
Reset	07_{HEX}							

VSB_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**VSB Entity ID.**							
Reset	07_{HEX}							

VBAT_ENTITY

Bit	7	6	5	4	3	2	1	0

Name	VBAT Entity ID.
Reset	07_{HEX}

VSEN1_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	VSEN1 Entity ID.							
Reset	07_{HEX}							

VSEN2_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	VSEN2 Entity ID.							
Reset	07_{HEX}							

VSEN3_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	VSEN3 Entity ID.							
Reset	07_{HEX}							

VSEN4_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	VSEN4 Entity ID.							
Reset	07_{HEX}							

FAN1_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	FAN1 Entity ID.							
Reset	07_{HEX}							

FAN2_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	FAN2 Entity ID.							
Reset	07_{HEX}							

FAN3_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN3 Entity ID.**							
Reset	07_{HEX}							

FAN4_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN4 Entity ID.**							
Reset	07_{HEX}							

FAN5_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN5 Entity ID.**							
Reset	07_{HEX}							

FAN6_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN6 Entity ID.**							
Reset	07_{HEX}							

FAN7_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN7 Entity ID.**							
Reset	07_{HEX}							

FAN8_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN8 Entity ID.**							
Reset	07_{HEX}							

FAN9_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN9 Entity ID.**							
Reset	07_{HEX}							

FAN10_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN10 Entity ID.**							
Reset	07_{HEX}							

FAN11_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN11 Entity ID.**							
Reset	07_{HEX}							

FAN12_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**FAN12 Entity ID.**							
Reset	07_{HEX}							

TD1_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**TD1 Entity ID.**							
Reset	07_{HEX}							

TD2_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**TD2 Entity ID.**							
Reset	07_{HEX}							

TD3_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**TD3 Entity ID.**							

Reset	07_{HEX}

TD4_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**TD4 Entity ID.**							
Reset	07_{HEX}							

TR1_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**TR1 Entity ID.**							
Reset	07_{HEX}							

TR2_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**TR2 Entity ID.**							
Reset	07_{HEX}							

CHS_ENTITY

Bit	7	6	5	4	3	2	1	0
Name	**Chassis Entity ID.**							
Reset	23_{HEX}							

ENTINS1

Bit	7	6	5	4	3	2	1	0
Name	**VCoreB Entity Instance**				**VCoreA Entity Instance**			
Reset	02_{HEX}				01_{HEX}			

ENTINS2

Bit	7	6	5	4	3	2	1	0
Name	**VDD Entity Instance**				**Vtt Entity Instance**			
Reset	01_{HEX}				03_{HEX}			

ENTINS3

Bit	7	6	5	4	3	2	1	0
Name	**VBAT Entity Instance**				**VSB Entity Instance**			
Reset	03_{HEX}				02_{HEX}			

ENTINS4

Bit	7	6	5	4	3	2	1	0
Name	**VSEN2 Entity Instance**				**VSEN1 Entity Instance**			
Reset	05_{HEX}				04_{HEX}			

ENTINS5

Bit	7	6	5	4	3	2	1	0
Name	**VSEN4 Entity Instance**				**VSEN3 Entity Instance**			
Reset	07_{HEX}				06_{HEX}			

ENTINS6

Bit	7	6	5	4	3	2	1	0
Name	**FAN2 Entity Instance**				**FAN1 Entity Instance**			
Reset	02_{HEX}				01_{HEX}			

ENTINS7

Bit	7	6	5	4	3	2	1	0
Name	**FAN4 Entity Instance**				**FAN3 Entity Instance**			
Reset	04_{HEX}				03_{HEX}			

ENTINS8

Bit	7	6	5	4	3	2	1	0
Name	**FAN6 Entity Instance**				**FAN5 Entity Instance**			
Reset	06_{HEX}				05_{HEX}			

ENTINS9

Bit	7	6	5	4	3	2	1	0
Name	**FAN8 Entity Instance**				**FAN7 Entity Instance**			

Reset	08_{HEX}	07_{HEX}

ENTINS10

Bit	7	6	5	4	3	2	1	0
Name	**FAN10 Entity Instance**				**FAN9 Entity Instance**			
Reset	$0A_{HEX}$				09_{HEX}			

ENTINS11

Bit	7	6	5	4	3	2	1	0
Name	**FAN12 Entity Instance**				**FAN11 Entity Instance**			
Reset	$0C_{HEX}$				$0B_{HEX}$			

ENTINS12

Bit	7	6	5	4	3	2	1	0
Name	**TD2 Entity Instance**				**TD1 Entity Instance**			
Reset	02_{HEX}				01_{HEX}			

ENTINS13

Bit	7	6	5	4	3	2	1	0
Name	**TD4 Entity Instance**				**TD3 Entity Instance**			
Reset	04_{HEX}				03_{HEX}			

ENTINS14

Bit	7	6	5	4	3	2	1	0
Name	**TR2 Entity Instance**				**TR1 Entity Instance**			
Reset	06_{HEX}				05_{HEX}			

ENTINS15

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Chassis Entity Instance**			
Reset	00_{HEX}				01_{HEX}			

Bit	Description
7-0	**ENTITY**. Entity of each sensor channel. 03_{HEX}: Processor 07_{HEX}: System Board. 23_{HEX}: Chassis Back Panel Board. For other entity types, please refer to PET Spec. page 13.

8.13.2.12. Power on Control Option Register (PwrOnOption)

The W83793G supports 2 ways to power the system. One is to power the system only one time, no matter 5VDD rises or not. The other is the W83793G continues to issues power-on cycles until it detects VDD is already powered on.

Location: **PwrOnOption** - Bank 1 Address $7F_{HEX}$

Type: Read Write

Reset: VSB5V (Pin 7) Rising.

PWRONOPTION

Bit	7	6	5	4	3	2	1	0
Name	**Nuvoton Test Modes**							**PWR1T**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-1	**Nuvoton Test Mode**. Test modes for production. Nuvoton strongly suggests the customer not use these registers to avoid system malfunction.
0	**PWR1T** (Power on One Time). 0: Continues to issue power-on cycles (PWRBTN_N assert 0.1sec every 1sec) until VDD is powered-on. 1: Issues power-on cycle for only once.

8.13.2.13. Power on Command Register (PwrOnCmd)

ASF Remote Control Command supports Remote Power on features. Here defines the Power on commands supported by the W83793G.

Location: **PwrOnCmd** - Bank 1 Address 80_{HEX}

Type: Read Write

Reset: VSB5V (Pin 7) Rising.

PWRONCMD

Bit	7	6	5	4	3	2	1	0
Name	**Remote Power On Command**							

Reset	11_{HEX}

Bit	Description
7-0	Remote Power On Command.

8.13.2.14. Power down Command Register (PwrOffCmd)

ASF Remote Control Command supports Remote Power Down features. Here defines the Power off commands supported by the W83793G.

Location: **PwrOffCmd** - Bank 1 Address 81_{HEX}

Type: Read Write

Reset: VSB5V (Pin 7) Rising.

PWROFFCMD

Bit	7	6	5	4	3	2	1	0
Name	**Remote Power Off Command**							
Reset	12_{HEX}							

Bit	Description
7-0	Remote Power Off Command.

8.13.2.15. Reset Command Register (Rst Cmd)

ASF Remote Control Command supports Remote Reset features. Here defines the Reset commands supported by the W83793G.

Location: **RstCmd** - Bank 1 Address 82_{HEX}

Type: Read Write

Reset: VSB5V (Pin 7) Rising.

RSTCMD

Bit	7	6	5	4	3	2	1	0
Name	**Remote Reset Command**							
Reset	10_{HEX}							

Bit	Description
7-0	Remote Reset Command.

9. SPECIFICATIONS

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

9.2 DC Characteristics

(Ta = 0° C to 70° C, 5VDD = 5V ± 10%, 5VSB =5V ± 5%, V_{SS} = 0V)

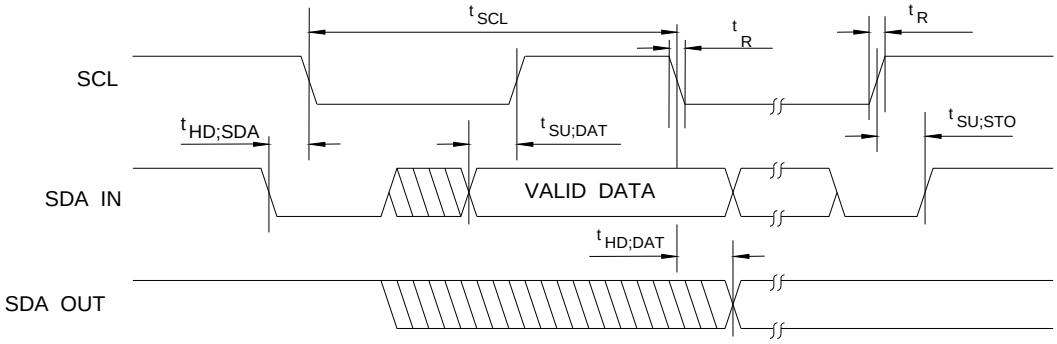
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT/OD_{12} – Output buffer or Open-drain output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA, OB mode
IN/ODB_{12v1sB} - bi-directional pin with sink capability of 12 mA and schmitt-trigger level input						
Input Low Voltage	V_{IL}			0.4	V	5VDD = 5 V
Input High Voltage	V_{IH}	0.6			V	5VDD = 5 V
Hysteresis	V_{TH}	0.2			V	5VDD = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = VDD
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
IN/ODB_{12tsB} - TTL level bi-directional pin with sink capability of 12 mA and schmitt-trigger level input						
Input Low Voltage	V_{IL}			0.8	V	5VDD = 5 V
Input High Voltage	V_{IH}	2.0			V	5VDD = 5 V
Hysteresis	V_{TH}	1.2			V	5VDD = 5 V

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = VDD
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
$OUTB_{12B}$ - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
ODB_{12B} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
AOUT – Analog output						
		N.A.				
INB_{V1SB} - VID input pin						
for INTEL™ VRM10.0, and VRM11 design						
Input Low Voltage	V_{IL}			0.4	V	
Input High Voltage	V_{IH}	0.6			V	
IN_{tV2SB} - VID input pin						
for AMD™ VRM design						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	1.4			V	
IN/OB_{V3B} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA						
for INTEL™ PECI						
Input Low Voltage	V_{IL}	$0.275V_{tt}$		$0.5V_{tt}$	V	
Input High Voltage	V_{IH}	$0.55V_{tt}$		$0.725V_{tt}$	V	
Output Low Voltage	V_{OL}			$0.25V_{tt}$	V	
Output High Voltage	V_{OH}	$0.75V_{tt}$			V	
Hysterisis	V_{Hys}	$0.1V_{tt}$			V	
INB_{tsB} - TTL level Schmitt-triggered input pin						

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	5VDD = 5 V
Input High Voltage	V_{IH}	2.0			V	5VDD = 5 V
Hysteresis	V_{TH}	1.2			V	5VDD = 5 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = VDD
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

9.3 AC Characteristics

9.3.1 Access Interface

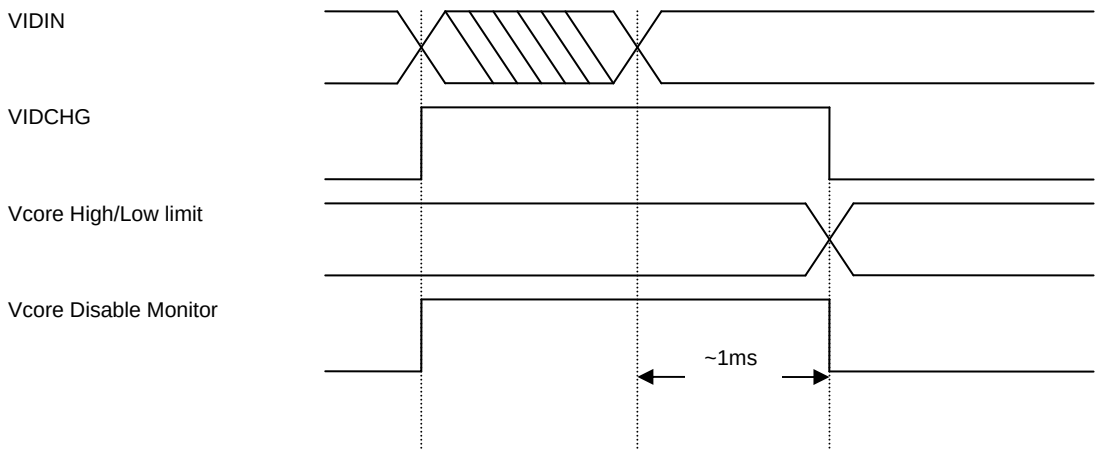


Serial Bus Timing Diagram

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	150		nS
DATA to SCL hold time	$t_{HD;DAT}$	270		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

9.3.2 Dynamic Vcore Limit Setting

If the dynamic VID function is enabled, the Vcore channel high/low limit will change in accordance with the VID table. When the VIDIN value changes, the internal VIDCHG signal will be set, until the VIDIN value is stable for more than 1ms. New Vcore high/low limit will be set at the falling edge of VIDCHG and the Vcore channel will enable the monitoring at the same time.



9.3.3 Power on Reset

The power-on reset threshold is 4.3V (typical). When VCC exceeds this threshold, the internal reset signal will be asserted for 3uS. During this time period, the W83793G is in the reset state. When the internal reset signal is de-asserted, the W83793G is in the operating state.

In the operating state, if VCC drops below 4.0V and then rises above 4.3V, the internal reset signal will be asserted immediately. Fig 1 illustrates the reset mechanism.

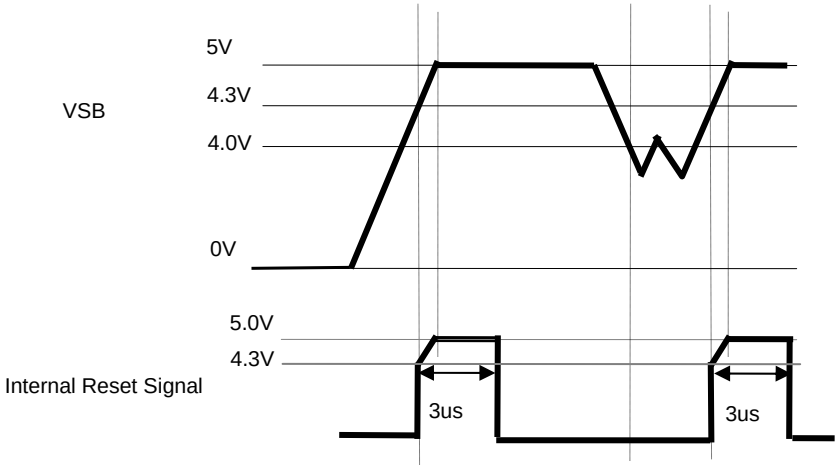
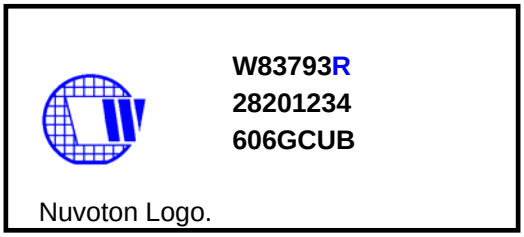


Figure 1.

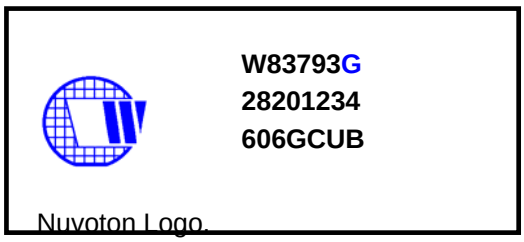
10. ORDERING INFORMATION

PART NO.	PACKAGE	REMARKS
W83793G	SSOP56	Pb-free Package

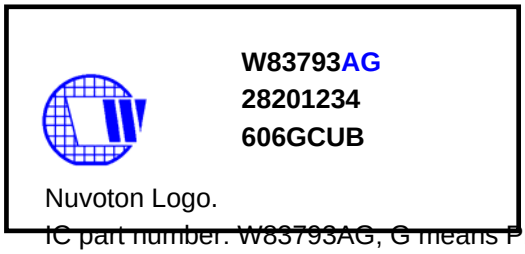
11. TOP MARKING SPECIFICATION



Left	Nuvoton Logo.
First Line	IC part number: W83793R; R means SSOP, leaded package.
Second Line	Serial number
Third Line	Tracking Code: 6 06 G C UB for Package information
	6 Package is made in 2006
	06 Week: 06
	G Assembly house ID; G means Greatek; A means ASE; O means OSE
	C IC version
	UB Mask version



Left	Nuvoton Logo.
First Line	IC part number: W83793G; G means Pb-free package.
Second Line	Serial number
Third Line	Tracking Code: 6 06 G C UB for Package information
	6 Package is made in 2006
	06 Week: 06
	G Assembly house ID; G means Greatek; A means ASE; O means OSE
	C IC version
	UB Mask version

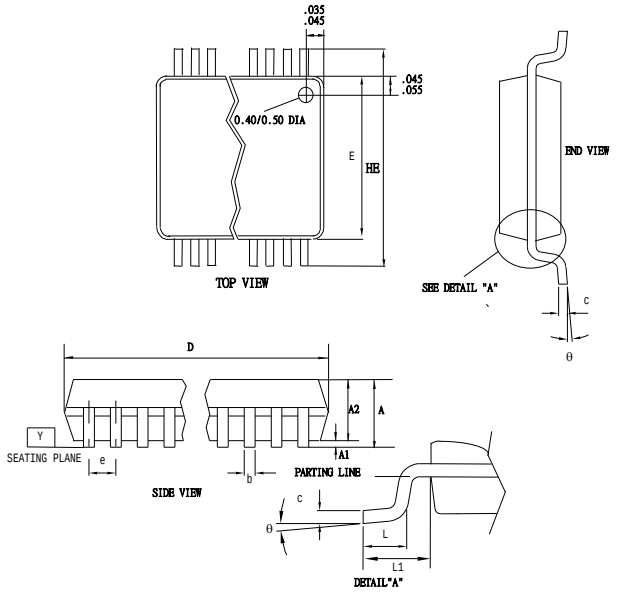


Left	Nuvoton Logo.
First Line	IC part number: W83793AG; G means Pb-free package.
Second Line	Serial number
Third Line	Tracking Code: 6 06 G C UB for Package information

6	Package is made in 2006
06	Week: 06
G	Assembly house ID; G means Greatek; A means ASE; O means OSE
C	IC version
UB	Mask version

12. PACKAGE DRAWING AND DIMENSIONS

(56-pin SSOP 300mil)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.41	2.57	2.79	0.095	0.101	0.110
A1	0.20	0.30	0.41	0.008	0.012	0.016
A2	2.24	2.29	2.34	0.088	0.090	0.092
b	0.20	0.25	0.34	0.008	0.010	0.0135
c	0.13	—	0.25	0.005	—	0.010
D	18.2	18.42	18.54	0.720	0.725	0.730
H_E	10.16	10.31	10.41	0.400	0.406	0.410
E	7.42	7.52	7.59	0.292	0.296	0.299
e	0.51	0.64	0.76	0.020	0.025	0.030
L	0.61	0.81	1.02	0.024	0.032	0.040
L1	—	1.40	—	—	0.055	—
Y	—	—	0.08	—	—	0.003
θ	0	—	8	0	—	8

13. APPENDIX

13.1 Register Summary

BANK 0

Index	Register Name	Index	Register Name
BANK 0 ADDRESS 00-1F			
00_{HEX}	Bank Selection	10_{HEX}	VCore A Readout
01_{HEX}	Watch Dog Lock	11_{HEX}	VCore B Readout
02_{HEX}	Watch Dog Enable	12_{HEX}	Vtt Readout
03_{HEX}	Watch Dog Status	13_{HEX}	
04_{HEX}	Watch Dog Timer	14_{HEX}	VSEN1 Readout
05_{HEX}	VIDA Input Value	15_{HEX}	VSEN2 Readout
06_{HEX}	VIDB Input Value	16_{HEX}	VSEN3 Readout
07_{HEX}	VIDA Latch	17_{HEX}	VSEN4 Readout
08_{HEX}	VIDB Latch	18_{HEX}	5VDD Readout
09_{HEX}	VCore High Tolerance	19_{HEX}	5VSB Readout
$0A_{HEX}$	VCore Low Tolerance	$1A_{HEX}$	VBAT Readout
$0B_{HEX}$	I^2C Address	$1B_{HEX}$	VIN Low Bit
$0C_{HEX}$	Sensor 1/2 Address	$1C_{HEX}$	TD1 Readout
$0D_{HEX}$	Nuvoton Vendor ID	$1D_{HE}X$	TD2 Readout
$0E_{HEX}$	Nuvoton Chip ID	$1E_{HEX}$	TD3 Readout
$0F_{HEX}$	Nuvoton Device ID	$1F_{HEX}$	TD4 Readout
BANK 0 ADDRESS 20-3F			
20_{HEX}	TR1 Readout	30_{HEX}	Fan7 Count Low Byte
21_{HEX}	TR2 Readout	31_{HEX}	Fan8 Count High Byte
22_{HEX}	Temp Low Bit Readout	32_{HEX}	Fan8 Count Low Byte

Index	Register Name	Index	Register Name
23_{HEX}	Fan1 Count High Byte	33_{HEX}	Fan9 Count High Byte
24_{HEX}	Fan1 Count Low Byte	34_{HEX}	Fan9 Count Low Byte
25_{HEX}	Fan2 Count High Byte	35_{HEX}	Fan10 Count High Byte
26_{HEX}	Fan2 Count Low Byte	36_{HEX}	Fan10 Count Low Byte
27_{HEX}	Fan3 Count High Byte	37_{HEX}	Fan11 Count High Byte
28_{HEX}	Fan3 Count Low Byte	38_{HEX}	Fan11 Count Low Byte
29_{HEX}	Fan4 Count High Byte	39_{HEX}	Fan12 Count High Byte
$2A_{HEX}$	Fan4 Count Low Byte	$3A_{HEX}$	Fan12 Count Low Byte
$2B_{HEX}$	Fan5 Count High Byte	$3B_{HEX}$	
$2C_{HEX}$	Fan5 Count Low Byte	$3C_{HEX}$	
$2D_{HEX}$	Fan6 Count High Byte	$3D_{HEX}$	
$2E_{HEX}$	Fan6 Count Low Byte	$3E_{HEX}$	
$2F_{HEX}$	Fan7 Count High Byte	$3F_{HEX}$	
BANK 0 ADDRESS 40-5F			
40_{HEX}	Configuration	50_{HEX}	SMI/IRQ Control
41_{HEX}	Interrupt Status 1	51_{HEX}	OVT Control
42_{HEX}	Interrupt Status 2	52_{HEX}	OVT/Beep Global Enable
43_{HEX}	Interrupt Status 3	53_{HEX}	Beep Control 1
44_{HEX}	Interrupt Status 4	54_{HEX}	Beep Control 2
45_{HEX}	Interrupt Status 5	55_{HEX}	Beep Control 3
46_{HEX}	Interrupt Mask 1	56_{HEX}	Beep Control 4
47_{HEX}	Interrupt Mask 2	57_{HEX}	Beep Control 5
48_{HEX}	Interrupt Mask 3	58_{HEX}	Multi-Function Pin Control
49_{HEX}	Interrupt Mask 4	59_{HEX}	VID Control
$4A_{HEX}$	Interrupt Mask 5	$5A_{HEX}$	TD1 Configuration

Index	Register Name	Index	Register Name
$4B_{HEX}$	Real Time Status 1	$5B_{HEX}$	TD2 Configuration
$4C_{HEX}$	Real Time Status 2	$5C_{HEX}$	FanIn Control
$4D_{HEX}$	Real Time Status 3	$5D_{HEX}$	FanIn Redirection
$4E_{HEX}$	Real Time Status 4	$5E_{HEX}$	TD Mode Select
$4F_{HEX}$	Real Time Status 5	$5F_{HEX}$	TR Mode Select
BANK 0 ADDRESS 60-7F			
60_{HEX}	VCoreA High Limit	70_{HEX}	VSEN4 High Limit
61_{HEX}	VCoreA Low Limit	71_{HEX}	VSEN4 Low Limit
62_{HEX}	VCoreB High Limit	72_{HEX}	5VDD High Limit
63_{HEX}	VCoreB Low Limit	73_{HEX}	5VDD Low Limit
64_{HEX}	Vtt High Limit	74_{HEX}	5VSB High Limit
65_{HEX}	Vtt Low Limit	75_{HEX}	5VSB Low Limit
66_{HEX}		76_{HEX}	VBAT High Limit
67_{HEX}		77_{HEX}	VBAT Low Limit
68_{HEX}	High Limit Low Bit	78_{HEX}	TD1 Critical
69_{HEX}	Low Limit Low Bit	79_{HEX}	TD1 Critical Hysterisis
$6A_{HEX}$	VSEN1 High Limit	$7A_{HEX}$	TD1 Warning
$6B_{HEX}$	VSEN1 Low Limit	$7B_{HEX}$	TD1 Warning Hysterisis
$6C_{HEX}$	VSEN2 High Limit	$7C_{HEX}$	TD2 Critical
$6D_{HEX}$	VSEN2 Low Limit	$7D_{HEX}$	TD2 Critical Hysterisis
$6E_{HEX}$	VSEN3 High Limit	$7E_{HEX}$	TD2 Warning
$6F_{HEX}$	VSEN3 Low Limit	$7F_{HEX}$	TD2 Warning Hysterisis
BANK 0 ADDRESS 80-9F			
80_{HEX}	TD3 Critical	90_{HEX}	Fan1 Limit High Byte
81_{HEX}	TD3 Critical Hysterisis	91_{HEX}	Fan1 Limit Low Byte

Index	Register Name	Index	Register Name
82_{HEX}	TD3 Warning	92_{HEX}	Fan2 Limit High Byte
83_{HEX}	TD3 Warning Hysterisis	93_{HEX}	Fan2 Limit Low Byte
84_{HEX}	TD4 Critical	94_{HEX}	Fan3 Limit High Byte
85_{HEX}	TD4 Critical Hysterisis	95_{HEX}	Fan3 Limit Low Byte
86_{HEX}	TD4 Warning	96_{HEX}	Fan4 Limit High Byte
87_{HEX}	TD4 Warning Hysterisis	97_{HEX}	Fan4 Limit Low Byte
88_{HEX}	TR1 Critical	$98_{HE}X$	Fan5 Limit High Byte
89_{HEX}	TR1 Critical Hysterisis	99_{HEX}	Fan5 Limit Low Byte
$8A_{HEX}$	TR1 Warning	$9A_{HEX}$	Fan6 Limit High Byte
$8B_{HEX}$	TR1 Warning Hysterisis	$9B_{HEX}$	Fan6 Limit Low Byte
$8C_{HEX}$	TR2 Critical	$9C_{HEX}$	Fan7 Limit High Byte
$8D_{HEX}$	TR2 Critical Hysterisis	$9D_{HEX}$	Fan7 Limit Low Byte
$8E_{HEX}$	TR2 Warning	$9E_{HEX}$	Fan8 Limit High Byte
$8F_{HEX}$	TR2 Warning Hysterisis	$9F_{HEX}$	Fan8 Limit Low Byte
BANK 0 ADDRESS A0-BF			
$A0_{HEX}$	Fan9 Limit High Byte	$B0_{HEX}$	Fan Output Style 1
$A1_{HEX}$	Fan9 Limit Low Byte	$B1_{HEX}$	Fan Output Style 2
$A2_{HEX}$	Fan10 Limit High Byte	$B2_{HEX}$	Fan Default Speed
$A3_{HEX}$	Fan10 Limit Low Byte	$B3_{HEX}$	Fan1 Duty
$A4_{HEX}$	Fan11 Limit High Byte	$B4_{HEX}$	Fan2 Duty
$A5_{HEX}$	Fan11 Limit Low Byte	$B5_{HEX}$	Fan3 Duty
$A6_{HEX}$	Fan12 Limit High Byte	$B6_{HEX}$	Fan4 Duty
$A7_{HEX}$	Fan12 Limit Low Byte	$B7_{HEX}$	Fan5 Duty
$A8_{HEX}$	TD1 Temperature Offset	$B8_{HEX}$	Fan6 Duty
$A9_{HEX}$	TD2 Temperature Offset	$B9_{HEX}$	Fan7 Duty

Index	Register Name	Index	Register Name
AA_{HEX}	TD3 Temperature Offset	BA_{HEX}	Fan8 Duty
AB_{HEX}	TD4 Temperature Offset	BB_{HEX}	Fan1 Output Prescalar
AC_{HEX}	TR1 Temperature Offset	BC_{HEX}	Fan2 Output Prescalar
AD_{HEX}	TR2 Temperature Offset	BD_{HEX}	Fan3 Output Prescalar
AE_{HEX}		BE_{HEX}	Fan4 Output Prescalar
AF_{HEX}		BF_{HEX}	Fan5 Output Prescalar
BANK 0 ADDRESS C0-DF			
$C0_{HEX}$	Fan6 Output Prescalar	$D5_{HEX}$	PECI Return Domain
$C1_{HEX}$	Fan7 Output Prescalar	$D6_{HEX}$	PECI Warning Flags
$C2_{HEX}$	Fan8 Output Prescalar	$D7_{HEX}$	
$C3_{HEX}$	Step Up Time	$D8_{HEX}$	PECI Agent1 RelTempH
$C4_{HEX}$	Step Down Time	$D9_{HEX}$	PECI Agent1 RelTempL
$C5_{HEX}$	Critical Temperature	DA_{HEX}	PECI Agent2 RelTempH
$D0_{HEX}$	PECI Agent Configure	DB_{HEX}	PECI Agent2 RelTempL
$D1_{HEX}$	PECI Agent1 Tcase	DC_{HEX}	PECI Agent3 RelTempH
$D2_{HEX}$	PECI Agent2 Tcase	DD_{HEX}	PECI Agent3 RelTempL
$D3_{HEX}$	PECI Agent3 Tcase	DE_{HEX}	PECI Agent4 RelTempH
$D4_{HEX}$	PECI Agent4 Tcase	DF_{HEX}	PECI Agent4 RelTempL

BANK 1

Index	Register Name	Index	Register Name
BANK 1 ADDRESS 00-1F			
00_{HEX}	Bank Select	$0E_{HEX}$	Nuvoton Chip ID
$0D_{HEX}$	Nuvoton Vendor ID	$0F_{HEX}$	Nuvoton Device ID
BANK 1 ADDRESS 20-33			
20_{HEX}	UDID Device Capability	$2A_{HEX}$	UDID SubDevice ID High

Index	Register Name	Index	Register Name
21_{HEX}	UDID Version Number	$2B_{HEX}$	UDID SubDevice ID Low
22_{HEX}	UDID Vendor ID High	$2C_{HEX}$	UDID Specific Vendor ID1
23_{HEX}	UDID Vendor ID Low	$2D_{HEX}$	UDID Specific Vendor ID2
24_{HEX}	UDID Device ID High	$2E_{HEX}$	UDID Specific Vendor ID3
25_{HEX}	UDID Device ID Low	$2F_{HEX}$	UDID Specific Vendor ID4
26_{HEX}	UDID Interface High Byte	30_{HEX}	Random Number 1
27_{HEX}	UDID Interface Low Byte	31_{HEX}	Random Number 2
28_{HEX}	UDID SubVendor ID High	32_{HEX}	Random Number 3
29_{HEX}	UDID SubVendor ID Low	33_{HEX}	Random Number 4
BANK 1 ADDRESS 40			
40_{HEX}	ARP Assigned Address		
BANK 1 ADDRESS 50-6F			
50_{HEX}	VCoreA Entity ID	60_{HEX}	Fan7 Entity ID
51_{HEX}	VCoreB Entity ID	61_{HEX}	Fan8 Entity ID
52_{HEX}	Vtt Entity ID	62_{HEX}	Fan9 Entity ID
53_{HEX}	VDD Entity ID	63_{HEX}	Fan10 Entity ID
54_{HEX}	VSB5V Entity ID	64_{HEX}	Fan11 Entity ID
55_{HEX}	VBAT Entity ID	65_{HEX}	Fan12 Entity ID
56_{HEX}	VSEN1 Entity ID	66_{HEX}	TD1 Entity ID
57_{HEX}	VSEN2 Entity ID	67_{HEX}	TD2 Entity ID
58_{HEX}	VSEN3 Entity ID	68_{HEX}	TD3 Entity ID
59_{HEX}	VSEN4 Entity ID	69_{HEX}	TD4 Entity ID
$5A_{HEX}$	Fan1 Entity ID	$6A_{HEX}$	TR1 Entity ID
$5B_{HEX}$	Fan2 Entity ID	$6B_{HEX}$	TR2 Entity ID
$5C_{HE}X$	Fan3 Entity ID	$6C_{HEX}$	Chassis Entity ID

Index	Register Name	Index	Register Name
$5D_{HEX}$	Fan4 Entity ID	$6D_{HEX}$	
$5E_{HEX}$	Fan5 Entity ID	$6E_{HEX}$	
$5F_{HEX}$	Fan6 Entity ID	$6F_{HEX}$	
BANK 1 ADDRESS 70-8F			
70_{HEX}	VCoreA/VCoreB EntityID	80_{HEX}	Remote PowerOn Command
71_{HEX}	VDD/Vtt EntityID	81_{HEX}	Remote Power Off Command
72_{HEX}	VBAT/VSB EntityID	82_{HEX}	Remote Reset Command
73_{HEX}	VCoreA/VCoreB EntityID	83_{HEX}	
74_{HEX}	VSEN1/VSEN2 EntityID	84_{HEX}	
75_{HEX}	VSEN4/VSEN3 EntityID	85_{HEX}	
76_{HEX}	Fan1/2 EntityID	86_{HEX}	
77_{HEX}	Fan3/4 EntityID	87_{HEX}	
78_{HEX}	Fan5/6 EntityID	88_{HEX}	
79_{HEX}	Fan7/8 EntityID	89_{HEX}	
$7A_{HEX}$	Fan9/10 EntityID	$8A_{HEX}$	
$7B_{HEX}$	Fan11/12 EntityID	$8B_{HEX}$	
$7C_{HEX}$	TD1/2 EntityID	$8C_{HEX}$	
$7D_{HEX}$	TD3/4 EntityID	$8D_{HEX}$	
$7E_{HEX}$	Chassis EntityID	$8E_{HEX}$	
$7F_{HEX}$	Power On Option	$8F_{HEX}$	

BANK 2

Index	Register Name	Index	Register Name
BANK 2 ADDRESS 00-1F			
00_{HEX}	Bank Select	10_{HEX}	TD1 Target Temperature
01_{HEX}	TD1 Fan Mapping Select	11_{HEX}	TD2 Target Temperature

02_{HEX}	TD2 Fan Mapping Select	12_{HEX}	TD3 Target Temperature
03_{HEX}	TD3 Fan Mapping Select	13_{HEX}	TD4 Target Temperature
04_{HEX}	TD4 Fan Mapping Select	14_{HEX}	TR1 Target Temperature
05_{HEX}	TR1 Fan Mapping Select	15_{HEX}	TR2 Target Temperature
06_{HEX}	TR2 Fan Mapping Select	16_{HEX}	
07_{HEX}	Fan Control Mode Select	17_{HEX}	
08_{HEX}	TD1/2 Temp Tolerance	18_{HEX}	Fan1 Nonstop Duty Cycle
09_{HEX}	TD3/4 Temp Tolerance	19_{HEX}	Fan2 Nonstop Duty Cycle
$0A_{HEX}$	TR1/2 Temp Tolerance	$1A_{HEX}$	Fan3 Nonstop Duty Cycle
$0B_{HEX}$		$1B_{HEX}$	Fan4 Nonstop Duty Cycle
$0C_{HEX}$		$1C_{HEX}$	Fan5 Nonstop Duty Cycle
$0D_{HEX}$	Nuvoton Vendor ID	$1D_{HEX}$	Fan6 Nonstop Duty Cycle
$0E_{HEX}$	Nuvoton Chip ID	$1E_{HEX}$	Fan7 Nonstop Duty Cycle
$0F_{HEX}$	Nuvoton Device ID	$1F_{HEX}$	Fan8 Nonstop Duty Cycle
BANK 2 ADDRESS 20-3F			
20_{HEX}	Fan1 Start Duty Cycle	30_{HEX}	TD1 Temp Level01
21_{HEX}	Fan2 Start Duty Cycle	31_{HEX}	TD1 Temp Level12
22_{HEX}	Fan3 Start Duty Cycle	32_{HEX}	TD1 Temp Level23
23_{HEX}	Fan4 Start Duty Cycle	33_{HEX}	TD1 Temp Level34
24_{HEX}	Fan5 Start Duty Cycle	34_{HEX}	TD1 Temp Level45
25_{HEX}	Fan6 Start Duty Cycle	35_{HEX}	TD1 Temp Level56
26_{HEX}	Fan7 Start Duty Cycle	36_{HEX}	TD1 Temp Level67
27_{HEX}	Fan8 Start Duty Cycle	37_{HEX}	
28_{HEX}	Fan1 Stop Time	38_{HEX}	TD1 Fan Level0
29_{HEX}	Fan2 Stop Time	39_{HEX}	TD1 Fan Level1
$2A_{HEX}$	Fan3 Stop Time	$3A_{HEX}$	TD1 Fan Level2

$2B_{HEX}$	Fan4 Stop Time	$3B_{HEX}$	TD1 Fan Level3
$2C_{HEX}$	Fan5 Stop Time	$3C_{HEX}$	TD1 Fan Level4
$2D_{HEX}$	Fan6 Stop Time	$3D_{HEX}$	TD1 Fan Level5
$2E_{HEX}$	Fan7 Stop Time	$3E_{HEX}$	TD1 Fan Level6
$2F_{HEX}$	Fan8 Stop Time	$3F_{HEX}$	
BANK 2 ADDRESS 40-5F			
40_{HEX}	TD2 Temp Level01	50_{HEX}	TD3 Temp Level01
41_{HEX}	TD2 Temp Level12	51_{HEX}	TD3 Temp Level12
42_{HEX}	TD2 Temp Level23	52_{HEX}	TD3 Temp Level23
43_{HEX}	TD2 Temp Level34	53_{HEX}	TD3 Temp Level34
44_{HEX}	TD2 Temp Level45	54_{HEX}	TD3 Temp Level45
45_{HEX}	TD2 Temp Level56	55_{HEX}	TD3 Temp Level56
46_{HEX}	TD2 Temp Level67	56_{HEX}	TD3 Temp Level67
47_{HEX}		57_{HEX}	
48_{HEX}	TD2 Fan Level0	58_{HEX}	TD3 Fan Level0
49_{HEX}	TD2 Fan Level1	59_{HEX}	TD3 Fan Level1
$4A_{HEX}$	TD2 Fan Level2	$5A_{HEX}$	TD3 Fan Level2
$4B_{HEX}$	TD2 Fan Level3	$5B_{HEX}$	TD3 Fan Level3
$4C_{HEX}$	TD2 Fan Level4	$5C_{HEX}$	TD3 Fan Level4
$4D_{HEX}$	TD2 Fan Level5	$5D_{HEX}$	TD3 Fan Level5
$4E_{HEX}$	TD2 Fan Level6	$5E_{HEX}$	TD3 Fan Level6
$4F_{HEX}$		$5F_{HEX}$	
BANK 2 ADDRESS 60-7F			
60_{HEX}	TD4 Temp Level01	70_{HEX}	TR1 Temp Level01
61_{HEX}	TD4 Temp Level12	71_{HEX}	TR1 Temp Level12
62_{HEX}	TD4 Temp Level23	72_{HEX}	TR1 Temp Level23

63_{HEX}	TD4 Temp Level34	73_{HEX}	TR1 Temp Level34
64_{HEX}	TD4 Temp Level45	74_{HEX}	TR1 Temp Level45
65_{HEX}	TD4 Temp Level56	75_{HEX}	TR1 Temp Level56
66_{HEX}	TD4 Temp Level67	76_{HEX}	TR1 Temp Level67
67_{HEX}		77_{HEX}	
68_{HEX}	TD4 Fan Level0	78_{HEX}	TR1 Fan Level0
69_{HEX}	TD4 Fan Level1	79_{HEX}	TR1 Fan Level1
$6A_{HEX}$	TD4 Fan Level2	$7A_{HEX}$	TR1 Fan Level2
$6B_{HEX}$	TD4 Fan Level3	$7B_{HEX}$	TR1 Fan Level3
$6C_{HEX}$	TD4 Fan Level4	$7C_{HEX}$	TR1 Fan Level4
$6D_{HEX}$	TD4 Fan Level5	$7D_{HEX}$	TR1 Fan Level5
$6E_{HEX}$	TD4 Fan Level6	$7E_{HEX}$	TR1 Fan Level6
$6F_{HEX}$		$7F_{HEX}$	
BANK 2 ADDRESS 80-8F			
80_{HEX}	TR2 Temp Level01	88_{HEX}	TR2 Fan Level0
81_{HEX}	TR2 Temp Level12	89_{HEX}	TR2 Fan Level1
82_{HEX}	TR2 Temp Level23	$8A_{HEX}$	TR2 Fan Level2
83_{HEX}	TR2 Temp Level34	$8B_{HEX}$	TR2 Fan Level3
84_{HEX}	TR2 Temp Level45	$8C_{HEX}$	TR2 Fan Level4
85_{HEX}	TR2 Temp Level56	$8D_{HEX}$	TR2 Fan Level5
86_{HEX}	TR2 Temp Level67	$8E_{HEX}$	TR2 Fan Level6
87_{HEX}		$8F_{HEX}$	

14. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1		N.A.	Preliminary
0.2	06/06/05	N.A.	Modify the pin types for VID pins in section 4.1 and 5.2.
0.3	08/01/05	N.A.	Add Vtt and PECI pin.
0.32		N.A.	1. Modify Chapter 4 Block Diagram) and Chapter 5 Pin Configuration.
0.33	01/20/06	N.A.	Modify Registers for B version.
0.34	01/06/06	N.A.	1. Modify the formula to calculate the RPM. 2. Add information of “The Top Marking”. 3. Change the part name to W83793G
0.35	02/27/06	9, 13, 14	Add the descriptions of FANIN9~FANIN12.
1.0	07/21/06	N.A.	1. Modify 8.8.2.3 register descriptions. 2. Update 8.9.2.1 voltage reading formula. 3. Remove the AMD SI descriptions. 4. Update 8.3.2.2 Index 0Ch I2CADDR75B registers. Update AC Characteristic in Chap 9.3.
1.1	12/03/06	N.A.	Add W83793AG
1.2	05/21/07	N.A.	1. Correct grammar mistakes. 2. Update 3VSEN and 12VSEN to VSEN3 and VSEN4. 3. Update “Tcontrol” to “Tcase”. 4. Update the descriptions of Chapter 1, Chapter 2 and Chapter 4. Update the information of the W83793AG.
1.3	05/08/08	8,9,12.	1. Update VSEN3 and VSEN4 2. Move the revision history to the last chapter.
1.4	12/12/08	NA	Change Nuvoton logo to Nuvoton

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