DATA SHEET

74ABT245

Octal transceiver with direction pin (3-State)

Product data
Supersedes data of 1998 Jan 16

2003 Feb 06

Philips
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Octal transceiver with direction pin (3-State) 74ABT245

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64 mA/–32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 833 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted
- Inputs are disabled during 3-State mode

DESCRIPTION

The 74ABT245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT245 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

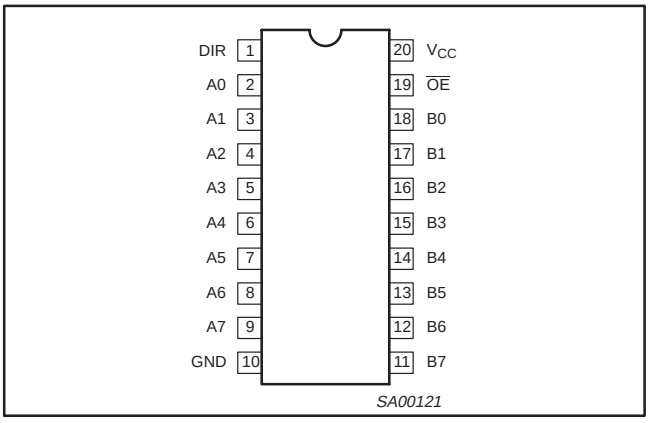
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 5 V	2.2 2.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0 V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; V_O = 0 V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5 V	50	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
20-Pin plastic SO	–40 °C to +85 °C	74ABT245D	SOT163-1
20-Pin Plastic SSOP Type II	–40 °C to +85 °C	74ABT245DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40 °C to +85 °C	74ABT245PW	SOT360-1

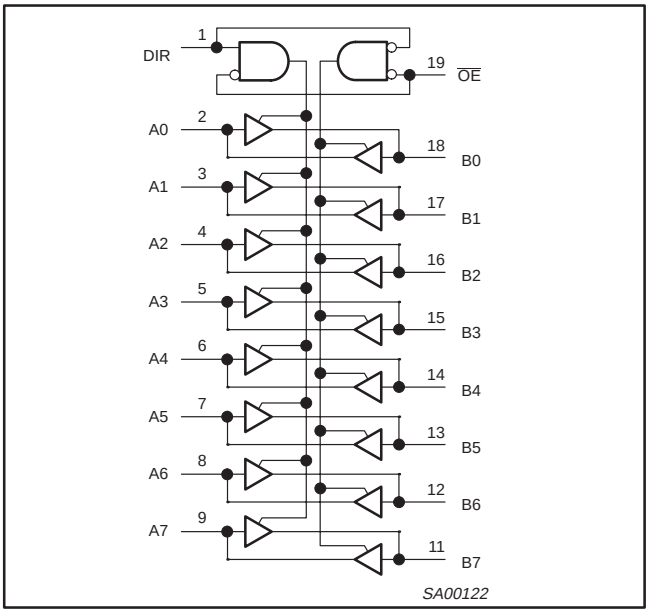
PIN CONFIGURATION



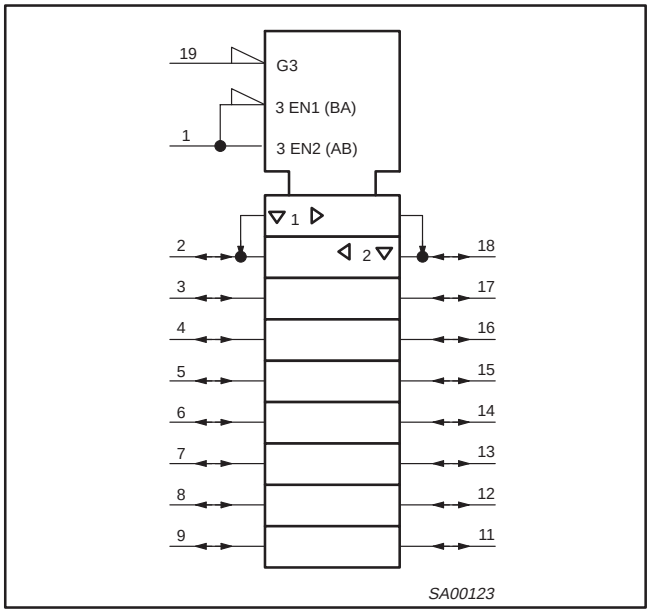
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OE}$	Output enable input (active-LOW)
10	GND	Ground (0 V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	An = Bn	Inputs
L	H	Inputs	Bn = An
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0		V
V_{IL}	LOW-level Input voltage		0.8	V
I_{OH}	HIGH-level output current		–32	mA
I_{OL}	LOW-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V; I_{IK} = –18 mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
			V_{CC} = 5.0 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
			V_{CC} = 4.5 V; I_{OH} = –32 mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5 V; V_I = GND or 5.5 V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5 V; V_I = GND or 5.5 V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} = 0.0 V; V_I or $V_O \leq$ 4.5 V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]		V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OE} = Don't care		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5 V; V_O = 2.7 V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output high leakage current		V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5 V; V_O = 2.5 V	–40	–100	–180	–40	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5 V; Outputs HIGH; V_I = GND or V_{CC}		50	250		250	µA
I_{CCL}			V_{CC} = 5.5 V; Outputs LOW; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}			V_{CC} = 5.5 V; Outputs 3-State; V_I = GND or V_{CC}		50	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one input at 3.4 V, other inputs at V_{CC} or GND; V_{CC} = 5.5 V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4 V, other inputs at V_{CC} or GND; V_{CC} = 5.5 V		50	250		250	µA
			Outputs 3-State, one enable input at 3.4 V, other inputs at V_{CC} or GND; V_{CC} = 5.5 V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec. For V_{CC} = 2.1 V to V_{CC} = 5 V ± 10%, a transition time of up to 100 µsec is permitted.

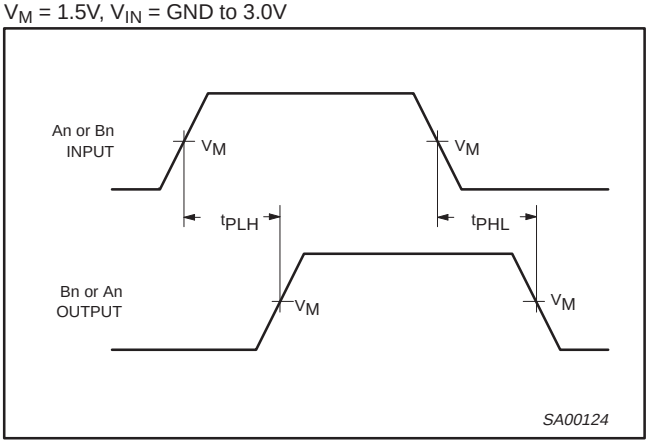
AC CHARACTERISTICS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF, R_L = 500 Ω

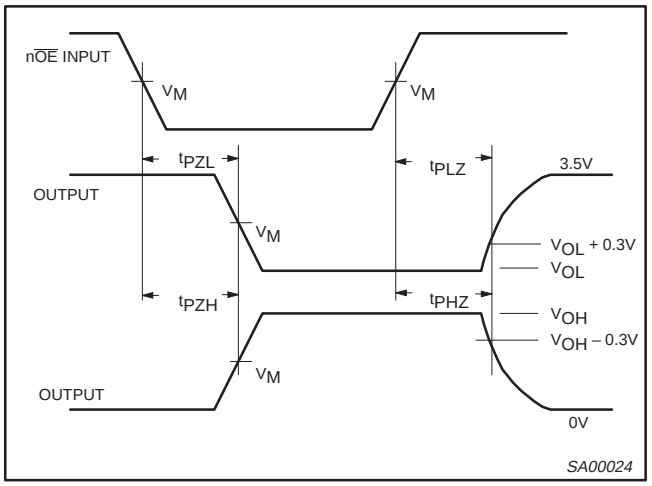
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C, V_{CC} = +5.0 V			T_{amb} = –40 °C to +85 °C, V_{CC} = +5.0 V ±0.5 V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	2.2 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	2	1.3 2.3	3.0 4.0	4.8 5.8	1.3 2.3	5.3 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW Level	2	1.0 1.0	4.7 4.1	6.2 5.8	1.0 1.0	7.2 6.3	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V

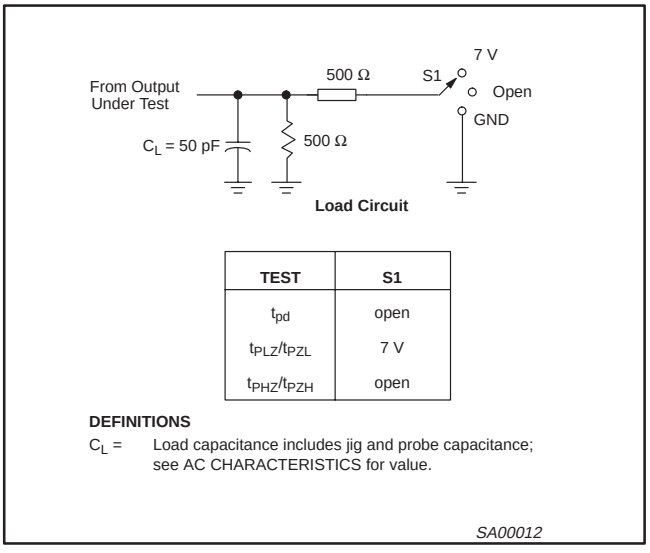


Waveform 1. Waveforms showing the input to output propagation delays

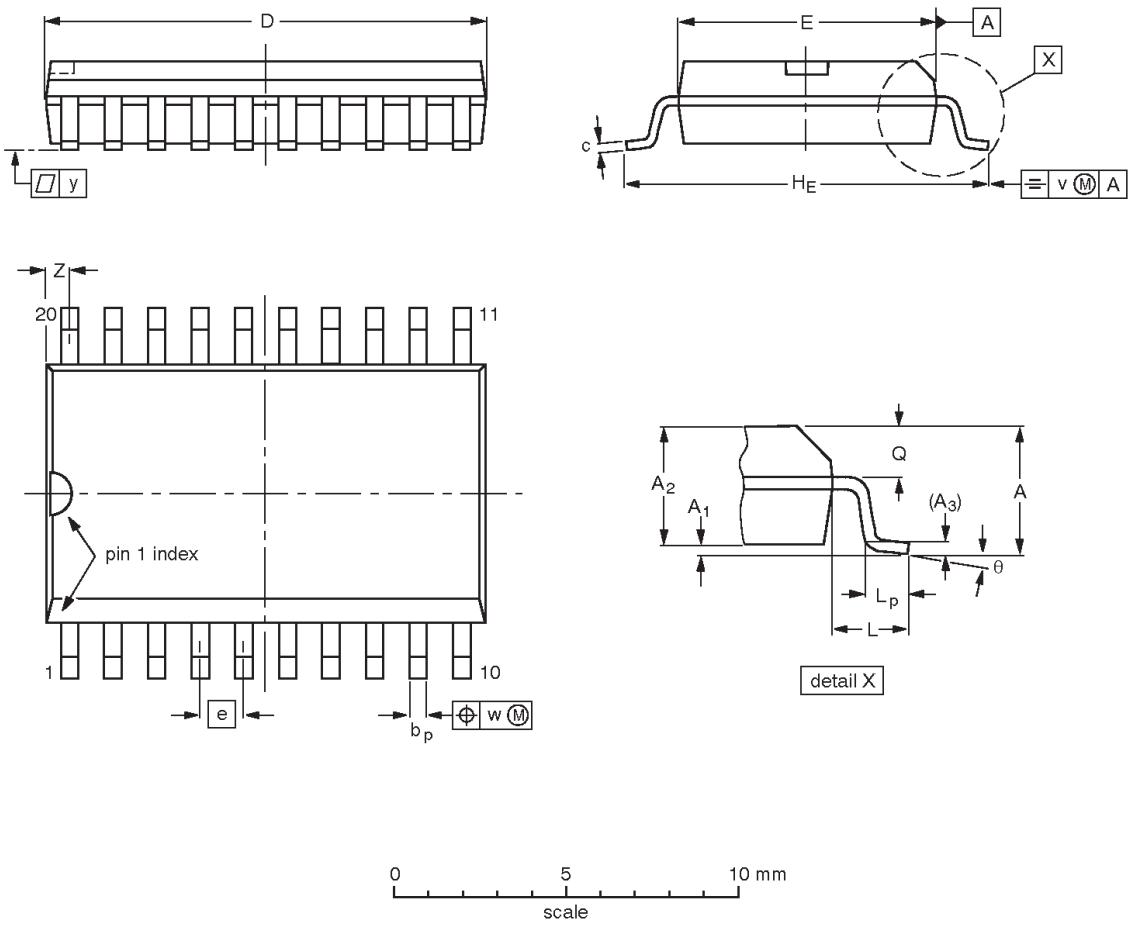


Waveform 2. Waveforms showing the 3-State Output Enable and Disable times

TEST CIRCUIT AND WAVEFORMS



SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

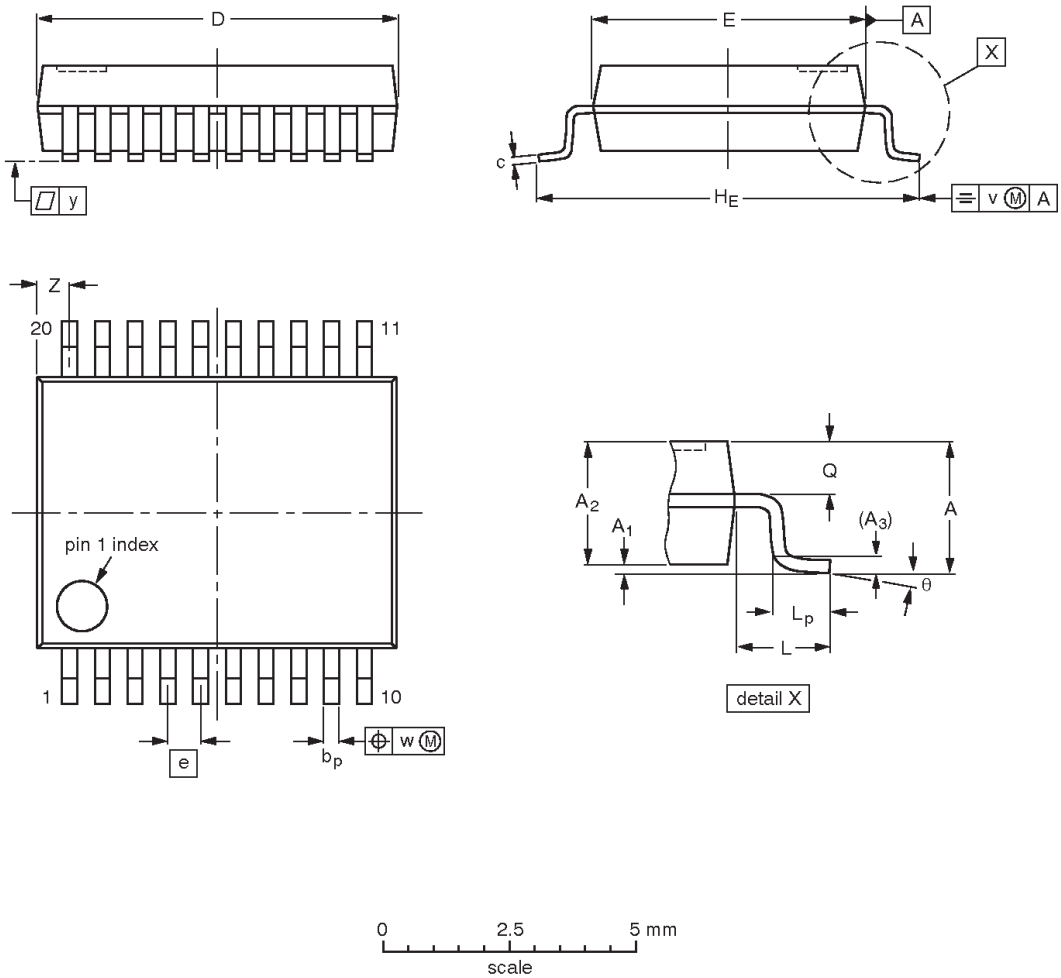
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

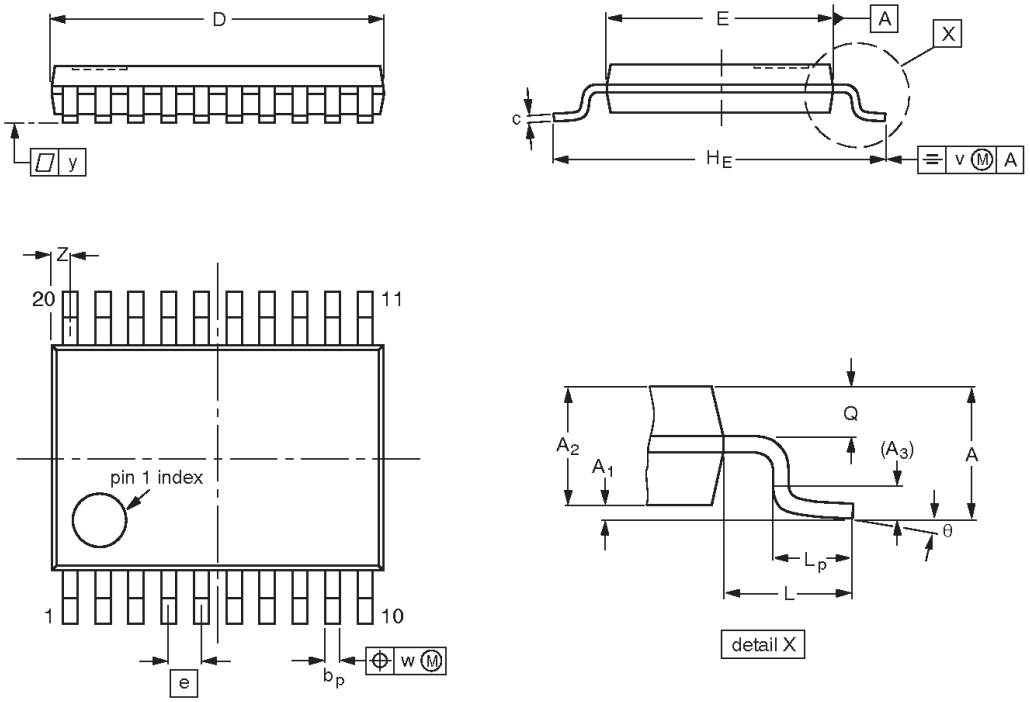
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

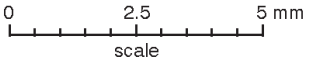
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_3	20030206	**Product data (9397 750 11087); ECN 853-1447 29305 of 17 December 2002; Supersedes Product specfication (9397 750 03467) of 1998 Jan 16.** Modifications: • Delete all references to N package. DIP20 package option discontinued.
_2	19980116	**Product specification (9397 750 03467) 1998 Jan 16; ECN 853-1447 18867 of 16 January 1998. Supersedes data of 1996 Sep 10.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 01-03

Document order number: 9397 750 11087

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