

74AHC164; 74AHCT164

8-bit serial-in/parallel-out shift register

Rev. 4 — 11 June 2020

Product data sheet

1. General description

The 74AHC164; 74AHCT164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel data outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input (\overline{MR}) clears the register and forces all outputs LOW, independently of other inputs. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features

- Wide supply voltage range from 2.0 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Input levels:
 - For 74AHC164: CMOS level
 - For 74AHCT164: TTL level
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74AHC164D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74AHCT164D | | | | |
| 74AHC164PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74AHCT164PW | | | | |
| 74AHC164BQ | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |
| 74AHCT164BQ | | | | |

4. Functional diagram

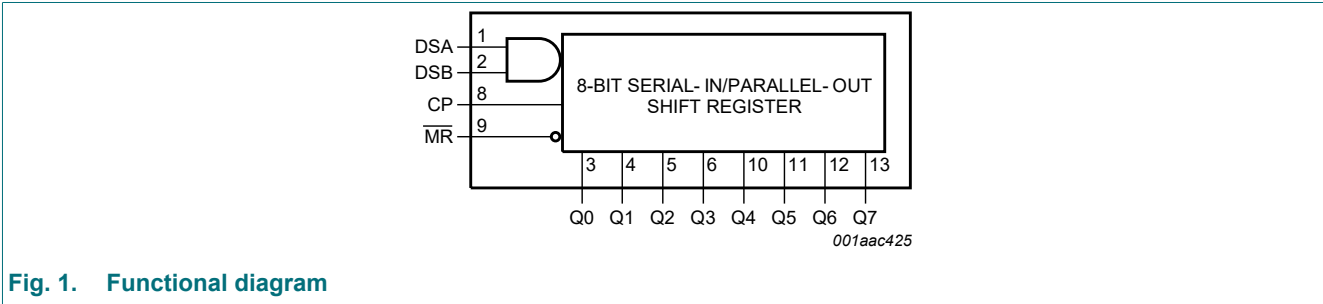


Fig. 1. Functional diagram

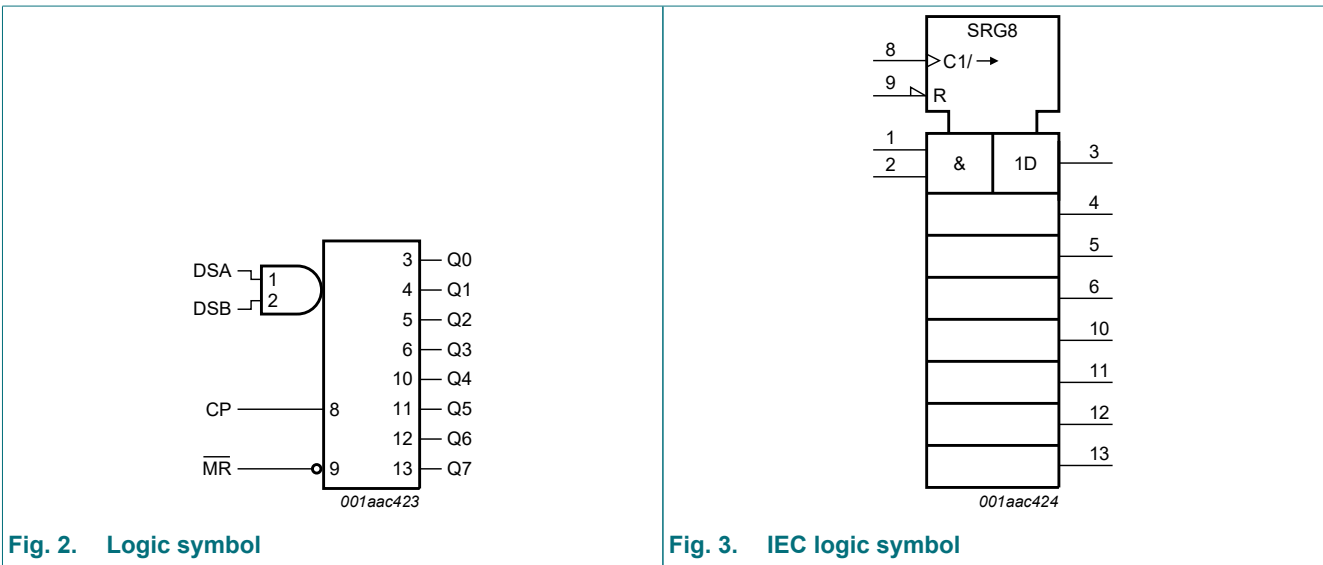


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

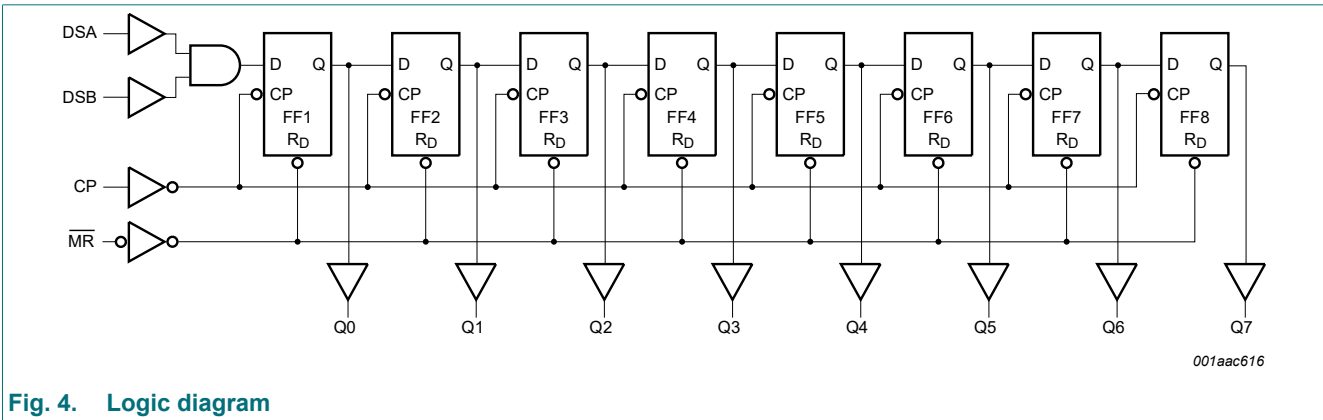
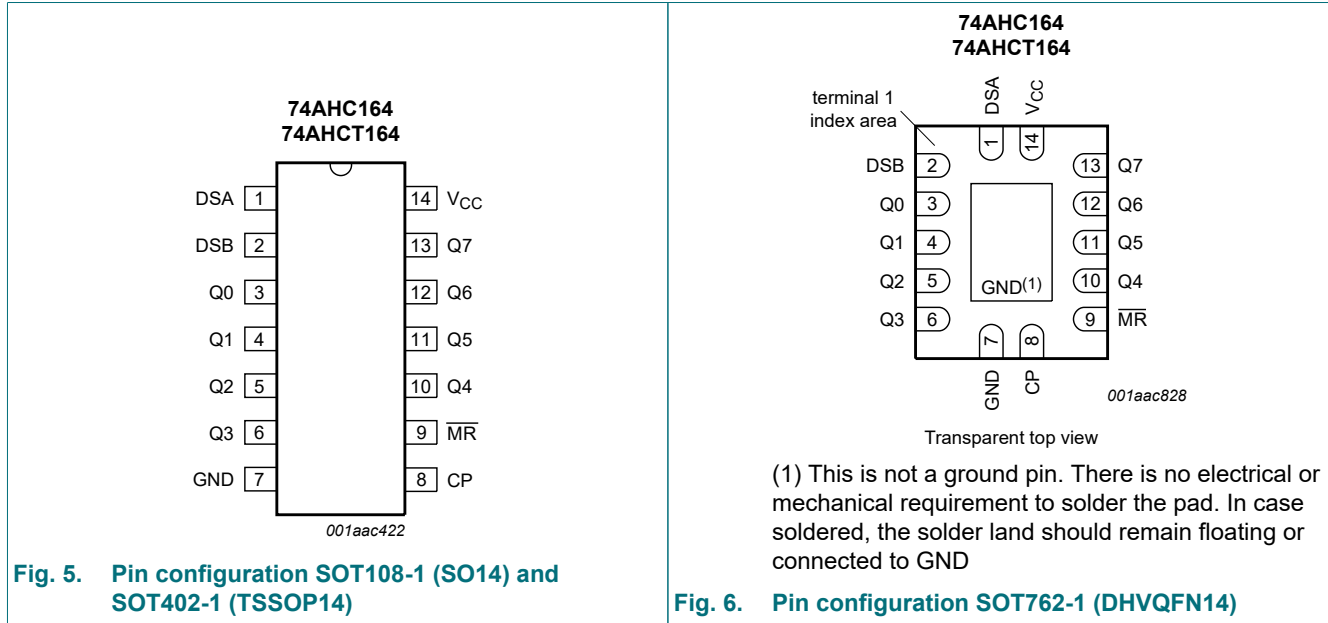


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|-----|--|
| DSA | 1 | serial data input A |
| DSB | 2 | serial data input B |
| Q0 | 3 | output 0 |
| Q1 | 4 | output 1 |
| Q2 | 5 | output 2 |
| Q3 | 6 | output 3 |
| GND | 7 | ground (0 V) |
| CP | 8 | clock input (LOW-to-HIGH edge-triggered) |
| MR | 9 | master reset input (active LOW) |
| Q4 | 10 | output 4 |
| Q5 | 11 | output 5 |
| Q6 | 12 | output 6 |
| Q7 | 13 | output 7 |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH transition;

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

q = lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

| Operating mode | Control | | Input | | Output | |
|----------------|---------|----|-------|-----|--------|----------|
| | MR | CP | DSA | DSB | Q0 | Q1 to Q7 |
| Reset (clear) | L | X | X | X | L | L to L |
| Shift | H | ↑ | l | l | L | q0 to q6 |
| | | | l | h | L | q0 to q6 |
| | | | h | l | L | q0 to q6 |
| | | | h | h | H | q0 to q6 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V [1] | -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1] | -20 | +20 | mA |
| I_O | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5)$ V | -25 | +25 | mA |
| I_{CC} | supply current | | - | +75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 74AHC164 | | | 74AHCT164 | | | Unit |
|---------------------|-------------------------------------|------------------------------|----------|-----|----------|-----------|-----|----------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 3.3$ V \pm 0.3 V | - | - | 100 | - | - | - | ns/V |
| | | $V_{CC} = 5.0$ V \pm 0.5 V | - | - | 20 | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---------------------------|---|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74AHC164 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | V _{CC} = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | V _{CC} = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| I _O = -8.0 mA; V _{CC} = 4.5 V | 3.94 | - | - | 3.80 | - | 3.70 | - | V | | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _O = 8.0 mA; V _{CC} = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V | | |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | μA |
| C _I | input capacitance | | - | 3 | 10 | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------|-----|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74AHCT164 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -50 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -8.0 mA | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 50 µA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other pins at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C _I | input capacitance | | - | 3 | 10 | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------------|-------------------|----------------------------------|-------|--------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| 74AHC164 | | | | | | | | | | |
| t _{pd} | propagation delay | CP to Qn; see Fig. 7 [2] | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | | | | | | | | |
| | | C _L = 15 pF | - | 6.5 | 12.8 | 1.0 | 15.0 | 1.0 | 16.0 | ns |
| | | C _L = 50 pF | - | 9.3 | 16.3 | 1.0 | 18.5 | 1.0 | 20.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 4.5 | 9.0 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| | | C _L = 50 pF | - | 6.4 | 11.0 | 1.0 | 12.5 | 1.0 | 14.0 | ns |
| | | MR to Qn; see Fig. 8 [3] | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | | | | | | | | |
| | | C _L = 15 pF | - | 5.3 | 12.8 | 1.0 | 15.0 | 1.0 | 16.0 | ns |
| | | C _L = 50 pF | - | 7.6 | 16.3 | 1.0 | 18.5 | 1.0 | 20.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| C _L = 15 pF | - | 4.0 | 8.6 | 1.0 | 10.0 | 1.0 | 11.0 | ns | | |
| C _L = 50 pF | - | 5.8 | 10.6 | 1.0 | 12.0 | 1.0 | 13.5 | ns | | |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|-------|--------|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| f _{max} | maximum frequency | see Fig. 7 | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | | | | | | | | |
| | | C _L = 15 pF | 80 | 125 | - | 65 | - | 50 | - | MHz |
| | | C _L = 50 pF | 50 | 75 | - | 45 | - | 35 | - | MHz |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | 125 | 175 | - | 105 | - | 85 | - | MHz |
| | | C _L = 50 pF | 85 | 115 | - | 75 | - | 65 | - | MHz |
| t _w | pulse width | CP HIGH or LOW; see Fig. 7 | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t _{WL} | pulse width LOW | MR; see Fig. 8 | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t _{su} | set-up time | DSA, DSB to CP; see Fig. 9 | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 5.0 | - | - | 6.0 | - | 6.0 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 4.5 | - | - | 4.5 | - | 4.5 | - | ns |
| t _h | hold time | DSA, DSB to CP; see Fig. 9 | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | - | - | 1.5 | - | 1.5 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | ns |
| t _{rec} | recovery time | MR to CP; see Fig. 8 | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 2.5 | - | - | 2.5 | - | 2.5 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 2.5 | - | - | 2.5 | - | 2.5 | - | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} [4] | - | 48 | - | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|-------------------------------|---|-------|--------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| 74AHCT164; V_{CC} = 4.5 V to 5.5 V | | | | | | | | | | |
| t _{pd} | propagation delay | CP to Qn; see Fig. 7 [2] | | | | | | | | |
| | | C _L = 15 pF | - | 3.4 | 9.0 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| | | C _L = 50 pF | - | 4.9 | 11.0 | 1.0 | 12.5 | 1.0 | 14.0 | ns |
| | | MR to Qn; see Fig. 8 [3] | | | | | | | | |
| | | C _L = 15 pF | - | 3.5 | 8.6 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| | | C _L = 50 pF | - | 5.0 | 10.6 | 1.0 | 12.0 | 1.0 | 13.5 | ns |
| f _{max} | maximum frequency | see Fig. 7 | | | | | | | | |
| | | C _L = 15 pF | 125 | 175 | - | 105 | - | 85 | - | MHz |
| | | C _L = 50 pF | 85 | 115 | - | 75 | - | 65 | - | MHz |
| t _w | pulse width | CP HIGH or LOW; see Fig. 7 | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t _{WL} | pulse width LOW | MR; see Fig. 8 | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t _{su} | set-up time | DSA, DSB to CP; see Fig. 9 | 4.5 | - | - | 4.5 | - | 4.5 | - | ns |
| t _h | hold time | DSA, DSB to CP; see Fig. 9 | 2.0 | - | - | 2.0 | - | 2.0 | - | ns |
| t _{rec} | recovery time | MR to CP; see Fig. 8 | 2.5 | - | - | 2.5 | - | 2.5 | - | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} [4] | - | 51 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{pd} is the same as t_{PHL} only.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

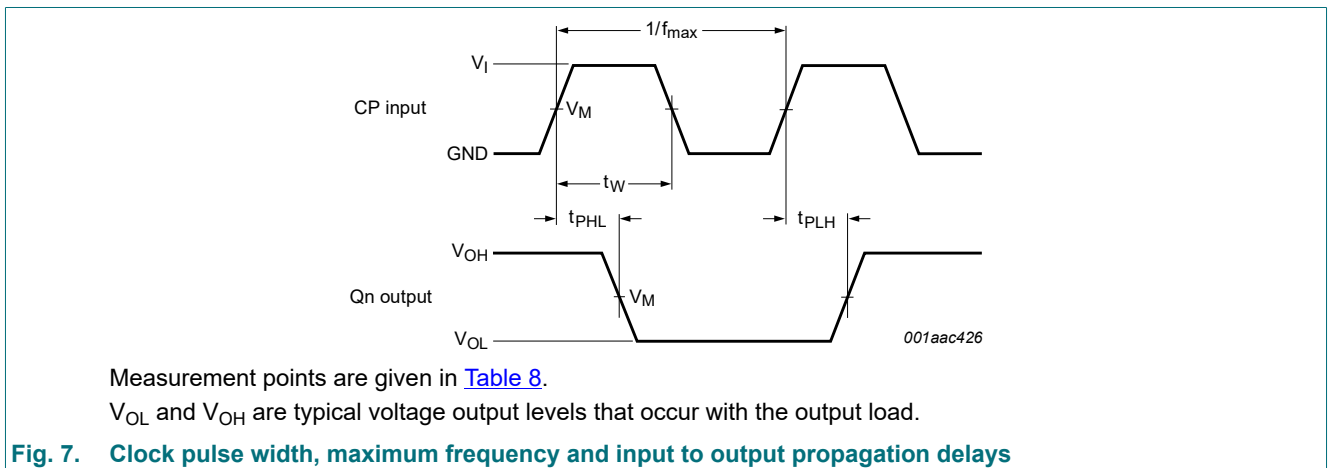
C_L = output load capacitance in pF;

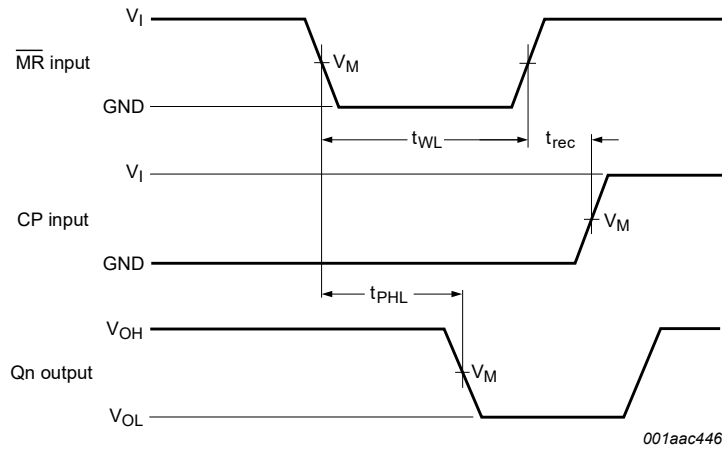
V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

10.1. Waveforms and test circuit

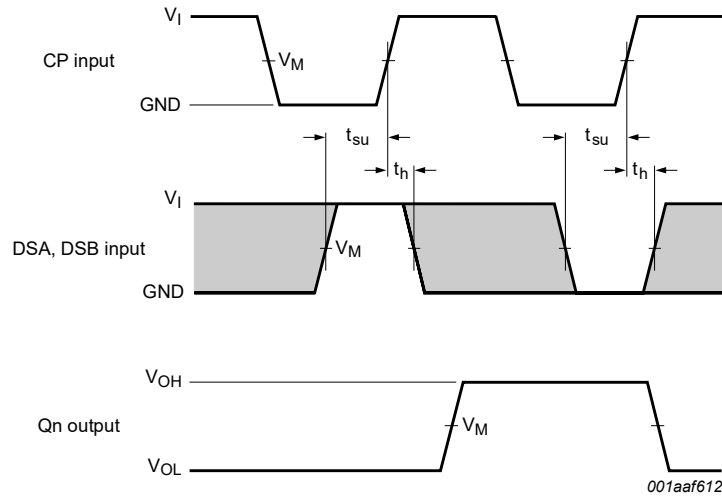




Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Master reset pulse width, recovery time and propagation delays



Measurement points are given in [Table 8](#).

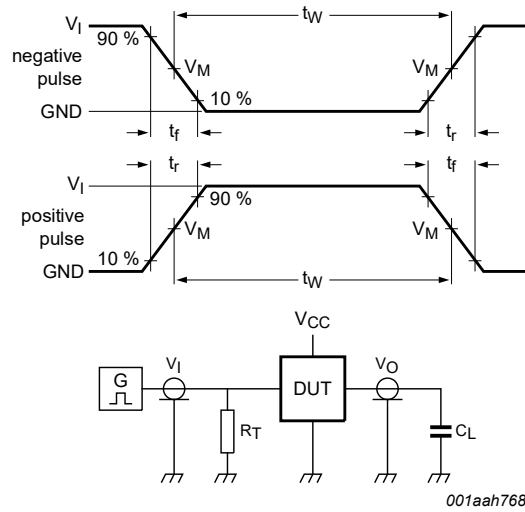
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 9. Data set-up and hold times

Table 8. Measurement points

| Type | Input | Output |
|-----------|---------------------|---------------------|
| | V_M | V_M |
| 74AHC164 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 74AHCT164 | 1.5 V | $0.5 \times V_{CC}$ |



001aah768

Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

Fig. 10. Test circuit for measuring switching times

Table 9. Test data

| Type | Input | | Load | Test |
|-----------|----------|---------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | |
| 74AHC164 | V_{CC} | ≤ 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |
| 74AHCT164 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

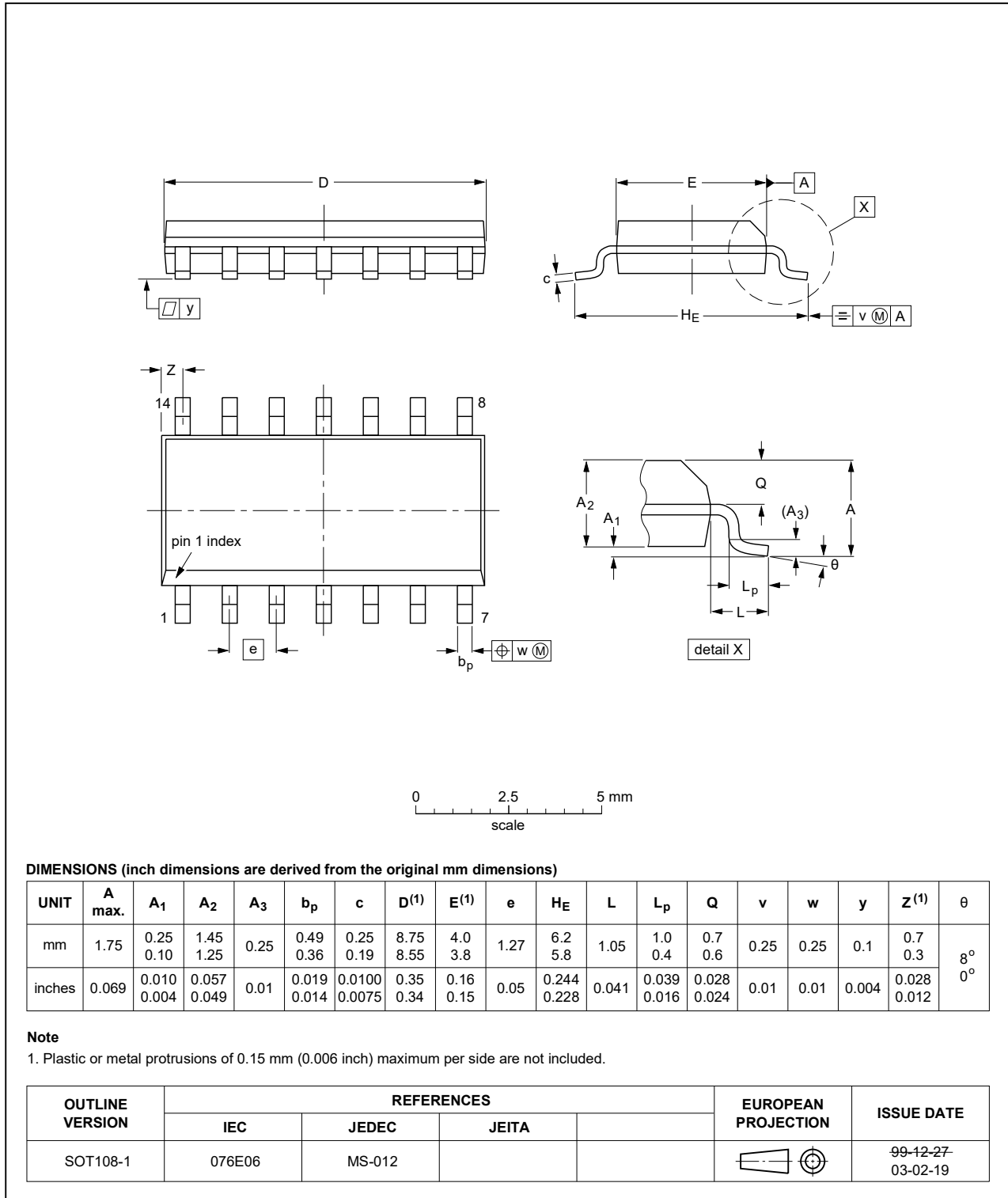


Fig. 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

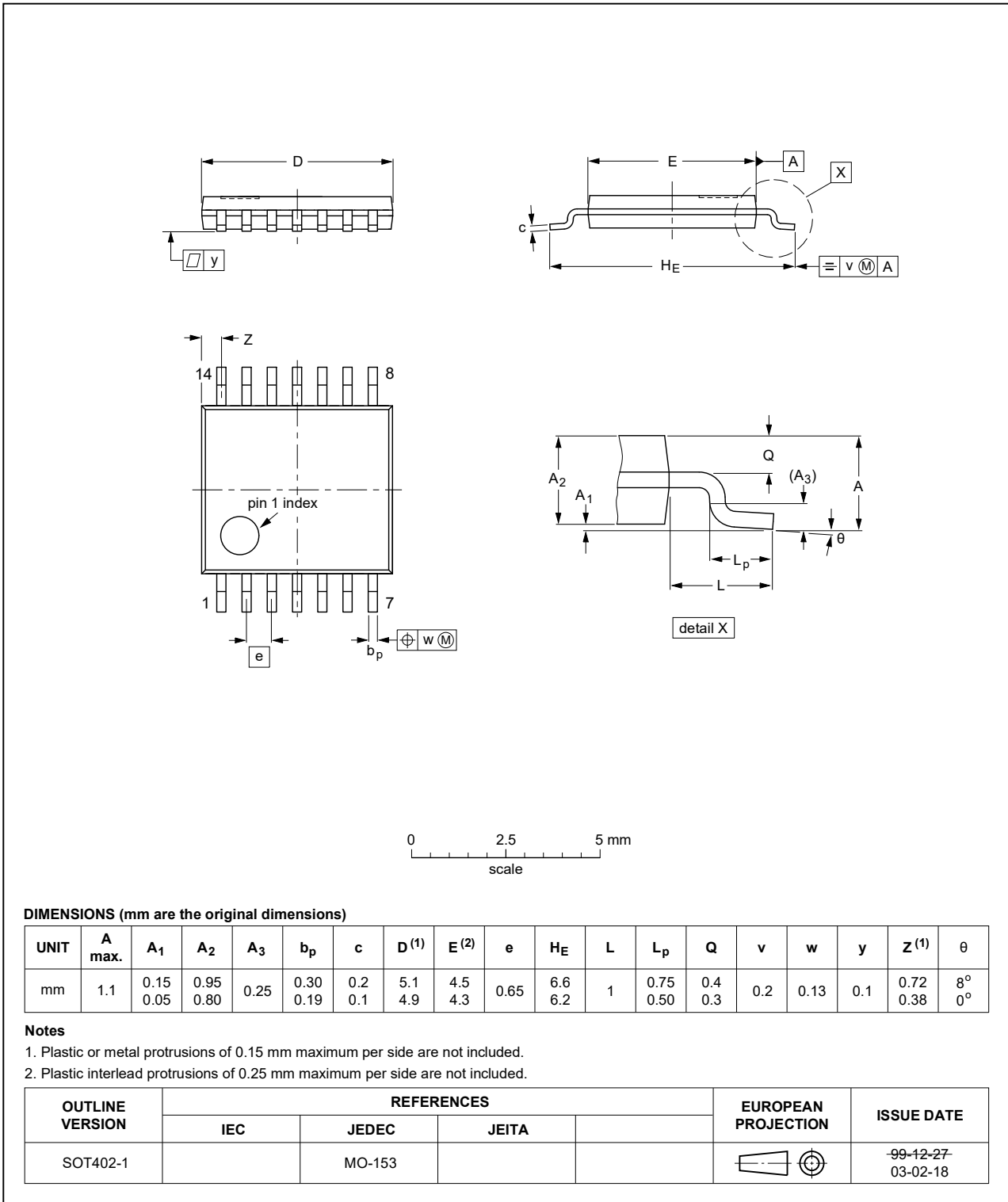


Fig. 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

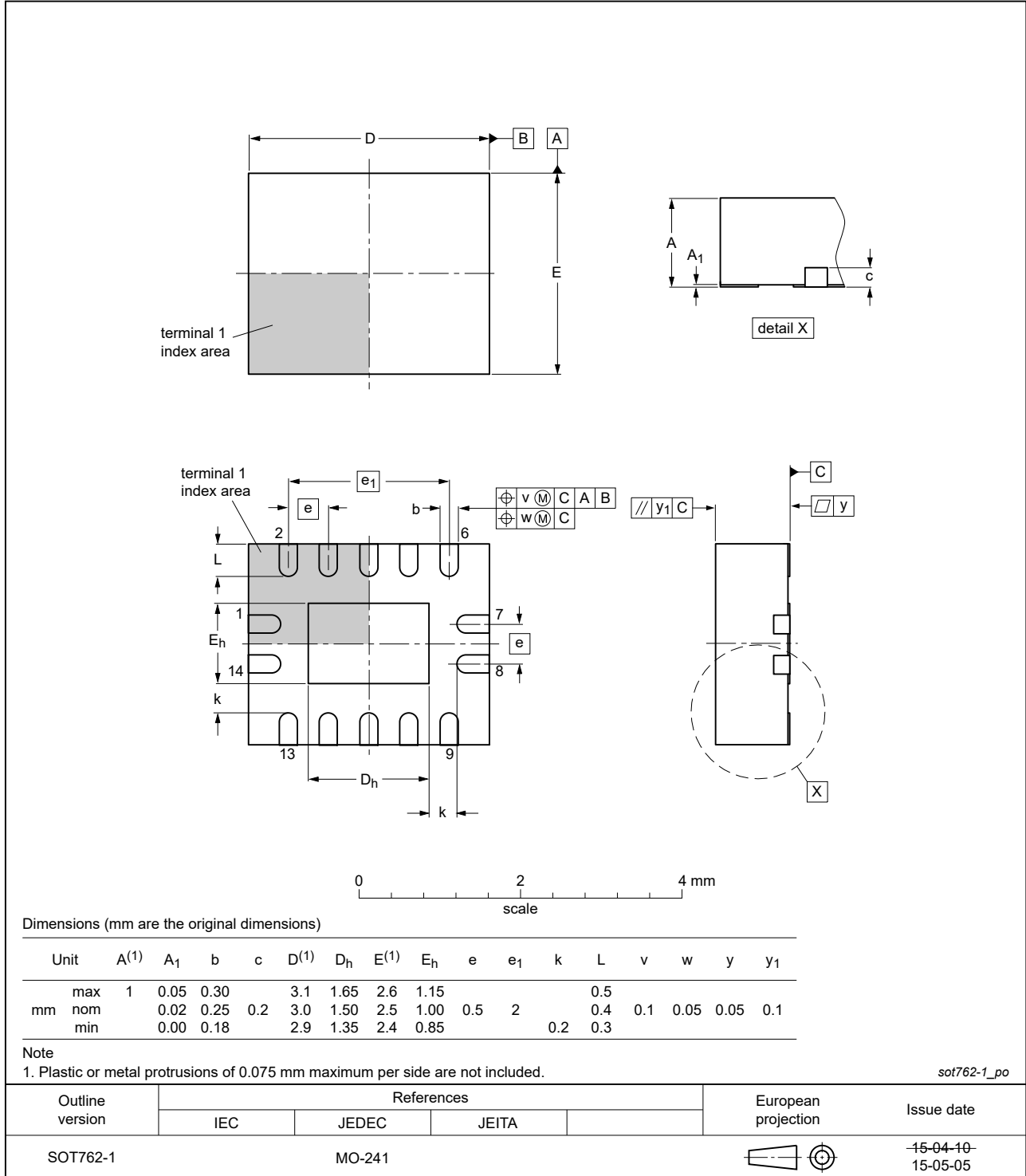


Fig. 13. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|---|-----------------------|---------------|-------------------|
| 74AHC_AHCT164 v.4 | 20200611 | Product data sheet | - | 74AHC_AHCT164 v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation have been updated. Package outline drawing of SOT762-1 (Fig. 13) updated. | | | |
| 74AHC_AHCT164 v.3 | 20080424 | Product data sheet | - | 74AHC_AHCT164 v.2 |
| Modifications: | <ul style="list-style-type: none"> Table 6: the conditions for input leakage current have been changed. | | | |
| 74AHC_AHCT164 v.2 | 20061129 | Product data sheet | - | 74AHC_AHCT164 v.1 |
| 74AHC_AHCT164 v.1 | 20000815 | Product specification | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
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