

# DATA SHEET

## **74ALVC244**

### **Octal buffer/line driver; 3-state**

Product specification  
Supersedes data of 2003 Aug 11

2003 Sep 08

## Octal buffer/line driver; 3-state

## 74ALVC244

## FEATURES

- Wide supply voltage range from 1.65 to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:  
JESD8-7 (1.65 to 1.95 V)  
JESD8-5 (2.3 to 2.7 V)  
JESD8B/JESD36 (2.7 to 3.6 V)
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

## DESCRIPTION

The 74ALVC244 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74ALVC244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $1\overline{OE}$  and  $2\overline{OE}$ . A HIGH on  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nAn to nYn	$V_{CC} = 1.8\text{ V}; C_L = 30\text{ pF}; R_L = 1\text{ k}\Omega$	2.7	ns
		$V_{CC} = 2.5\text{ V}; C_L = 30\text{ pF}; R_L = 500\ \Omega$	2.0	ns
		$V_{CC} = 2.7\text{ V}; C_L = 50\text{ pF}; R_L = 500\ \Omega$	2.3	ns
		$V_{CC} = 3.3\text{ V}; C_L = 50\text{ pF}; R_L = 500\ \Omega$	2.2	ns
$C_I$	input capacitance		3.5	pF
$C_{PD}$	power dissipation capacitance per buffer	$V_{CC} = 3.3\text{ V}$ ; notes 1 and 2	20	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

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## FUNCTION TABLE

See note 1.

INPUT		OUTPUT
$\overline{\text{nOE}}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

## Note

1. H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
Z = high-impedance OFF-state.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74ALVC244D	-40 to +85 °C	20	SO20	plastic	SOT163-1
74ALVC244PW	-40 to +85 °C	20	TSSOP20	plastic	SOT360-1
74ALVC244BQ	-40 to +85 °C	20	DHVQFN20	plastic	SOT764-1

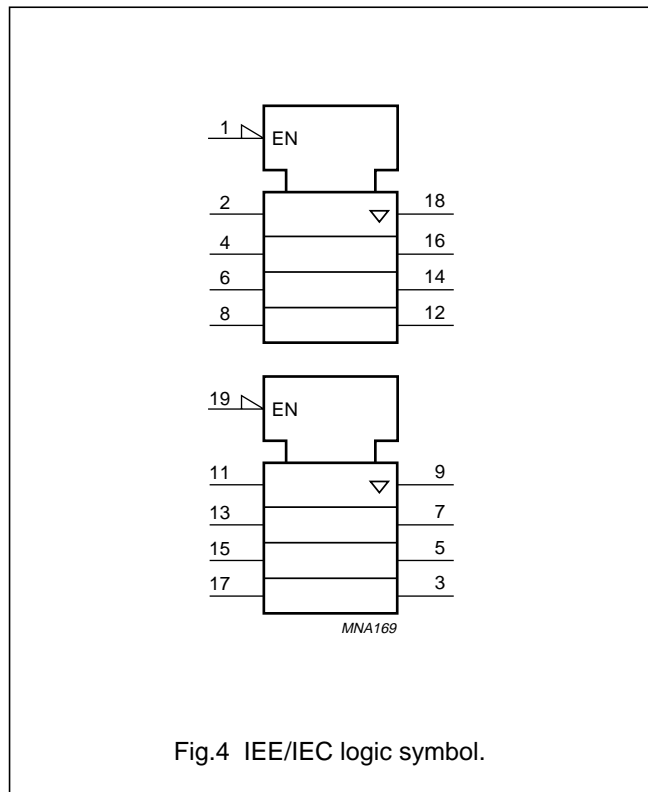
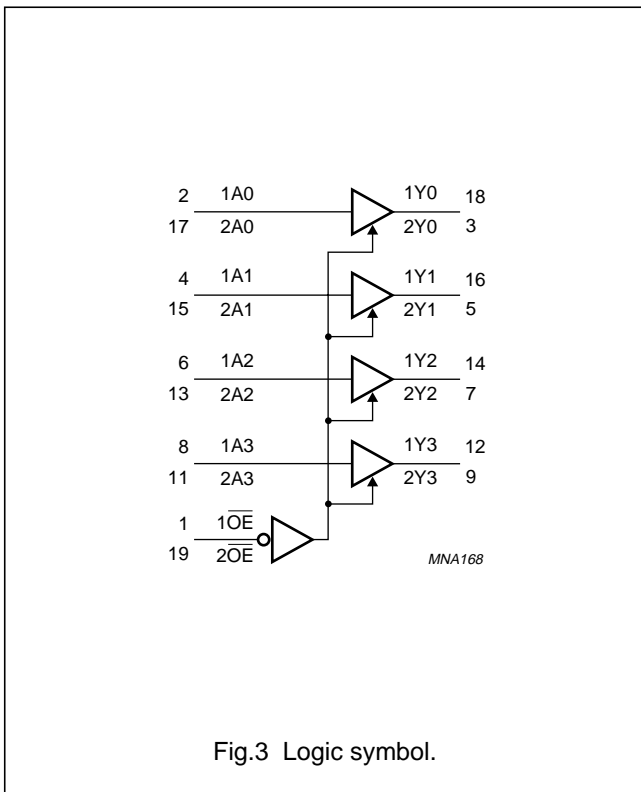
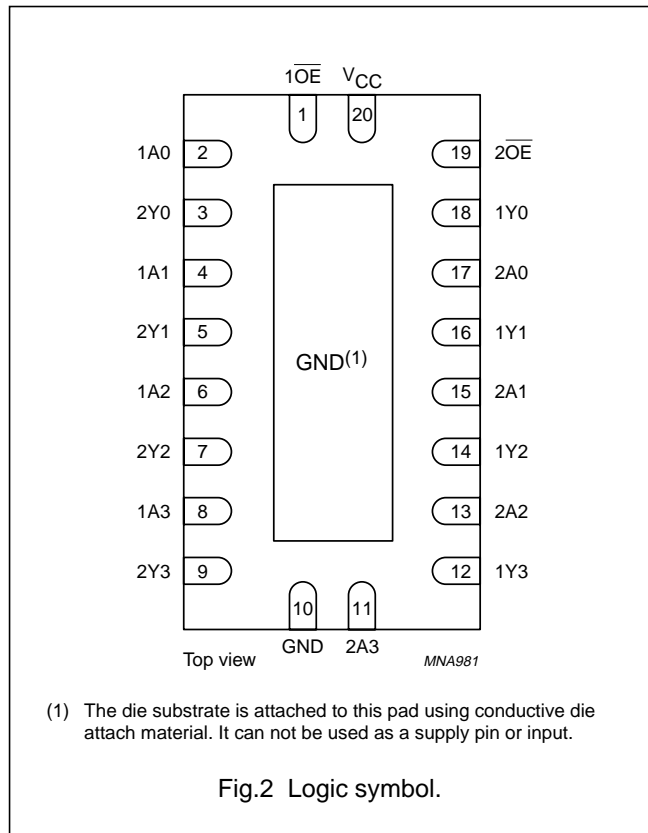
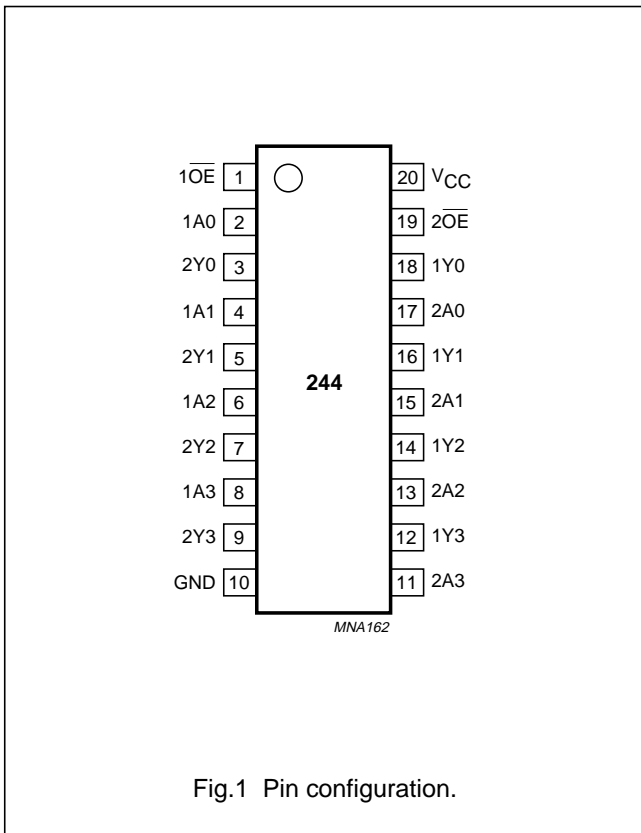
## PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{1OE}$	output enable input (active LOW)
2	1A0	data input
3	2Y0	bus output
4	1A1	data input
5	2Y1	bus output
6	1A2	data input
7	2Y2	bus output
8	1A3	data input
9	2Y3	bus output
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	2A3	data input
12	1Y3	bus output
13	2A2	data input
14	1Y2	bus output
15	2A1	data input
16	1Y1	bus output
17	2A0	data input
18	1Y0	bus output
19	$\overline{2OE}$	output enable input (active LOW)
20	V <sub>CC</sub>	supply voltage

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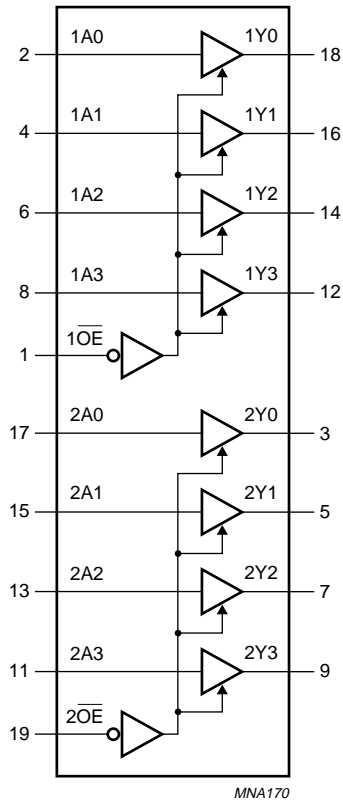


Fig.5 Logic diagram.

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		1.65	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	$V_{CC} = 1.65$ to $3.6$ V; enable mode	0	$V_{CC}$	V
		$V_{CC} = 1.65$ to $3.6$ V; disable mode	0	3.6	V
		$V_{CC} = 0$ V; Power-down mode	0	3.6	V
$T_{amb}$	operating ambient temperature		-40	+85	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.65$ to $2.7$ V	0	20	ns/V
		$V_{CC} = 2.7$ to $3.6$ V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input diode current	$V_I < 0$	-	-50	mA
$V_I$	input voltage		-0.5	+4.6	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
$V_O$	output voltage	enable mode; notes 1 and 2	-0.5	$V_{CC} + 0.5$	V
		disable mode	-0.5	+4.6	V
		Power-down mode; note 2	-0.5	+4.6	V
$I_O$	output source or sink current	$V_O = 0$ to $V_{CC}$	-	±50	mA
$I_{GND}, I_{CC}$	$V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ to $+85$ °C; note 3	-	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- When  $V_{CC} = 0$  V (Power-down mode), the output voltage can be 3.6 V in normal operation.
- For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
For TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V <sub>CC</sub>	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.65 to 3.6	–	–	0.2	V
		I <sub>O</sub> = 100 μA	1.65	–	–	0.3	V
		I <sub>O</sub> = 6 mA	2.3	–	–	0.4	V
		I <sub>O</sub> = 12 mA	2.3	–	–	0.6	V
		I <sub>O</sub> = 18 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 12 mA	3.0	–	–	0.4	V
		I <sub>O</sub> = 18 mA	3.0	–	–	0.55	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.65 to 3.6	V <sub>CC</sub> – 0.2	–	–	V
		I <sub>O</sub> = -100 μA	1.65	1.25	–	–	V
		I <sub>O</sub> = -6 mA	2.3	1.8	–	–	V
		I <sub>O</sub> = -12 mA	2.3	1.7	–	–	V
		I <sub>O</sub> = -18 mA	2.7	2.2	–	–	V
		I <sub>O</sub> = -12 mA	3.0	2.4	–	–	V
		I <sub>O</sub> = -18 mA	3.0	2.2	–	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 3.6 V or GND	3.6	–	±0.1	±5	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 3.6 V or GND; note 2	3.6	–	0.1	±10	μA
I <sub>off</sub>	power OFF leakage current	V <sub>I</sub> or V <sub>O</sub> = 3.6 V	0.0	–	±0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	0.2	20	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0	3.0 to 3.6	–	5	750	μA

## Notes

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. For transceivers, the parameters I<sub>OZ</sub> includes the input leakage current.

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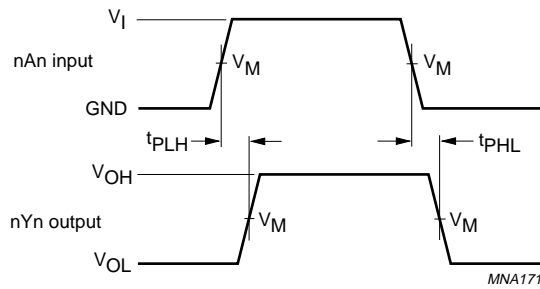
AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nAn to nYn	see Figs 6 and 8	1.65 to 1.95	1.0	2.7	4.4	ns
			2.3 to 2.7	1.0	2.0	3.1	ns
			2.7	1.0	2.3	3.1	ns
			3.0 to 3.6	1.0	2.2	2.8	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time n $\overline{OE}$ to nYn	see Figs 7 and 8	1.65 to 1.95	1.0	3.4	6.9	ns
			2.3 to 2.7	1.0	2.6	5.4	ns
			2.7	1.0	3.2	5.3	ns
			3.0 to 3.6	1.0	2.5	4.5	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time n $\overline{OE}$ to nYn	see Figs 7 and 8	1.65 to 1.95	1.0	3.8	5.9	ns
			2.3 to 2.7	1.0	2.2	4.1	ns
			2.7	1.0	3.0	4.4	ns
			3.0 to 3.6	1.0	2.9	4.2	ns

Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

AC WAVEFORMS



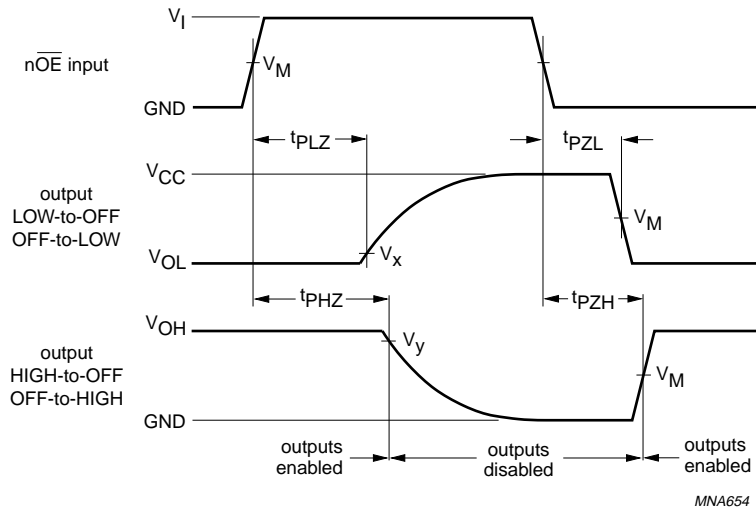
V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.65 to 1.95 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

Fig.6 Input nAn to output nYn propagation delay times.



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MNA654

V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.65 to 1.95 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

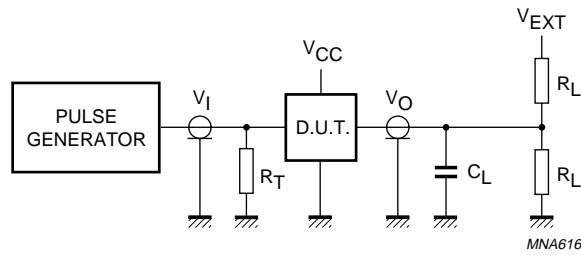
V<sub>x</sub> = V<sub>OL</sub> + 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>x</sub> = V<sub>OL</sub> + 0.15 V at V<sub>CC</sub> < 2.7 V;  
 V<sub>y</sub> = V<sub>OH</sub> - 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>y</sub> = V<sub>OH</sub> - 0.15 V at V<sub>CC</sub> < 2.7 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.

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V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.65 to 1.95 V	V <sub>CC</sub>	30 pF	1 kΩ	open	GND	2 × V <sub>CC</sub>
2.3 to 2.7 V	V <sub>CC</sub>	30 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V

Definitions for test circuit:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.8 Load circuitry for switching times.

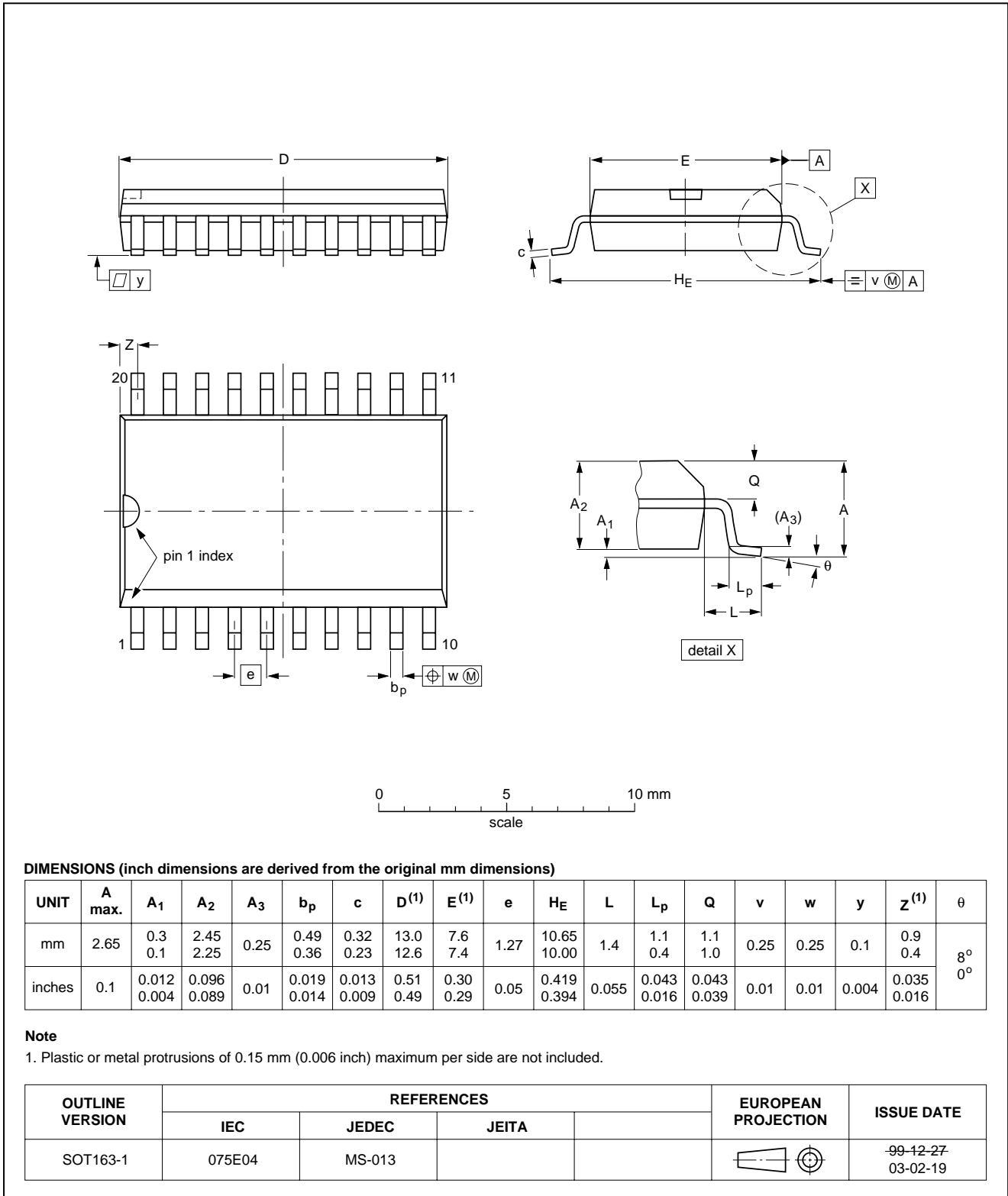
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PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

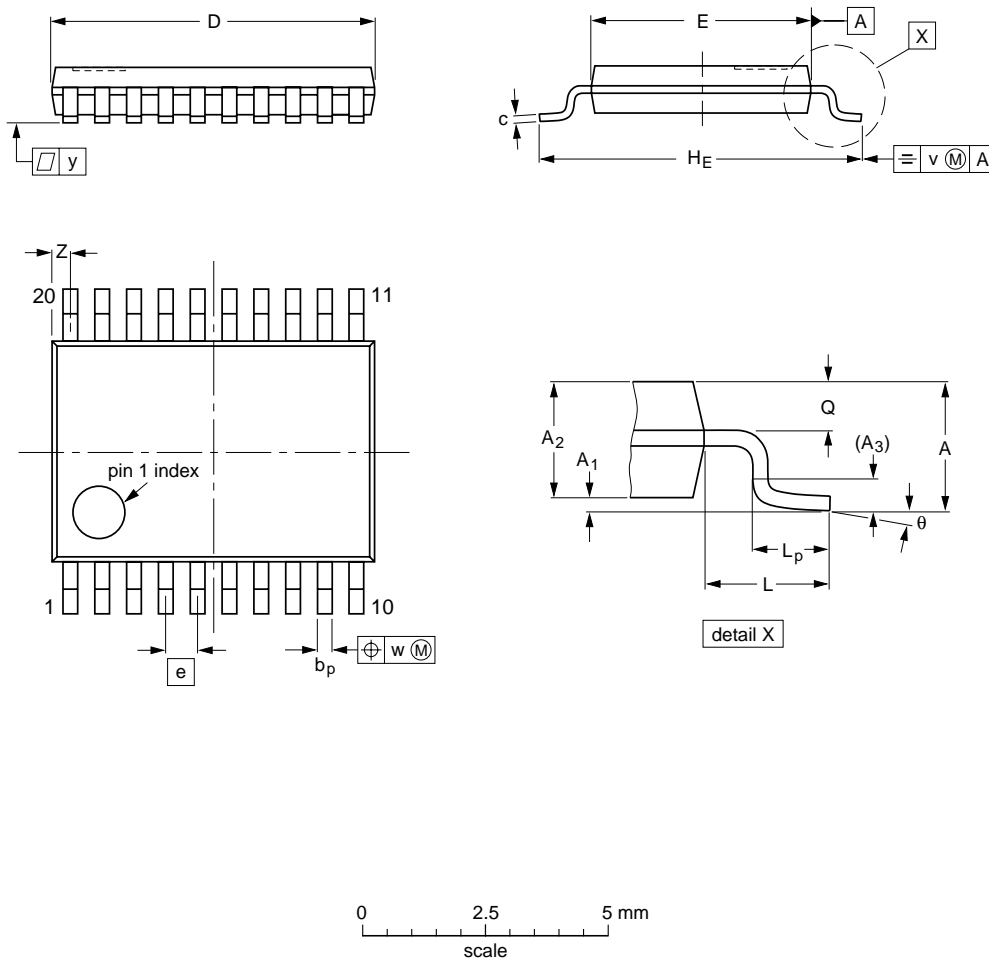


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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	$\theta$
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

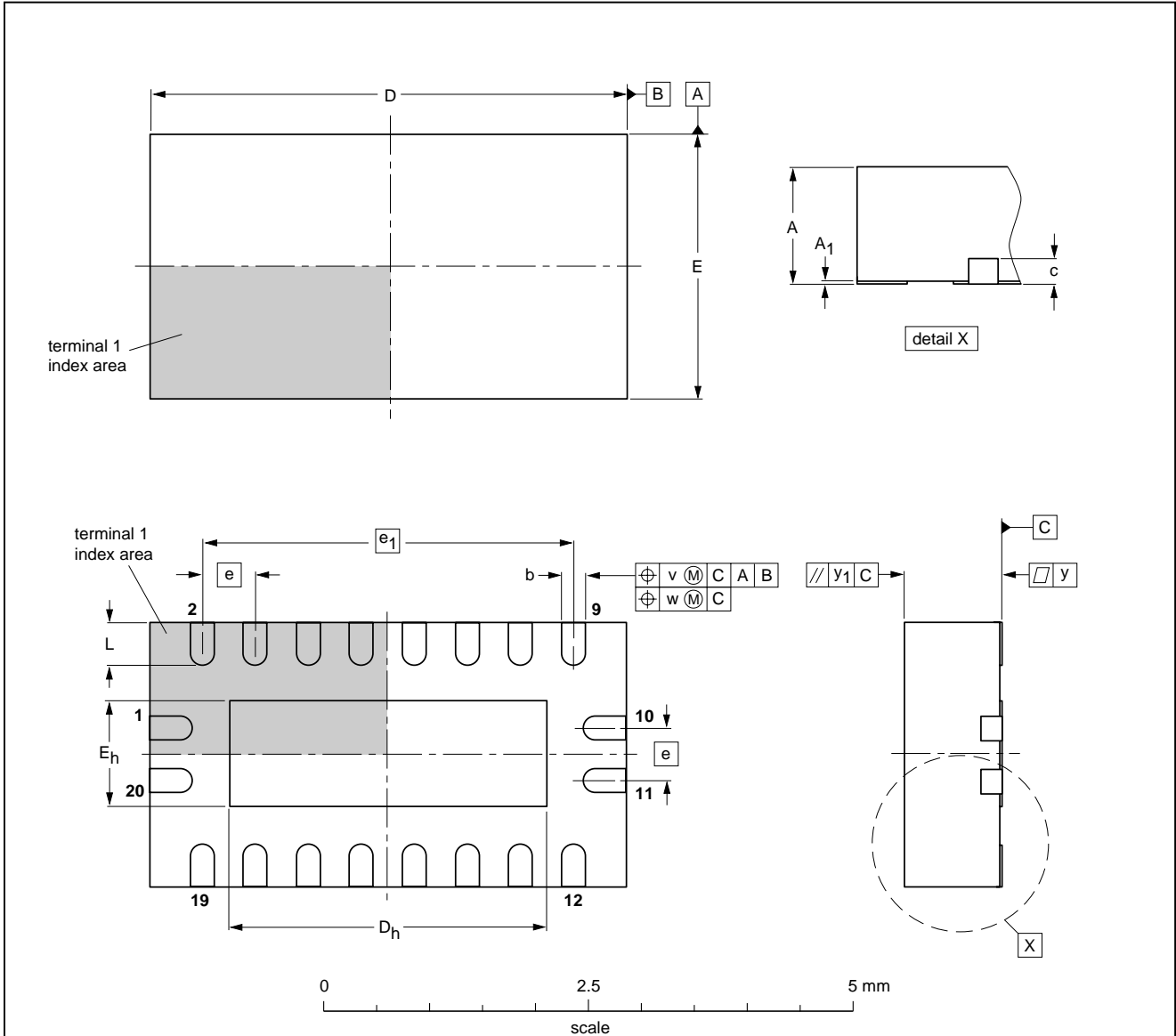
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				99-12-27 03-02-19

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DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT764-1	---	MO-241	---			02-10-17 03-01-27

## Octal buffer/line driver; 3-state

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
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[MCIMX6SX-SDB](#) [74ALVC125BQ,115](#) [74HC4050N](#) [74HC4514N](#) [MK21FN1M0AVLQ12](#) [MKV30F128VFM10](#) [FRDM-K66F](#) [FRDM-](#)  
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[MPC565MVR56](#) [MPC574XG-176DS](#) [MPC860PCVR66D4](#) [BT137-600E](#) [BT139X-600.127](#) [BUK7628-100A118](#) [BUK765R0-100E.118](#)  
[BZT52H-B9V1.115](#) [BZV85-C3V9.113](#) [BZX79-C47.113](#) [P5020NSE7VNB](#) [S12ZVML12EVBLIN](#) [SCC2692AC1N40](#) [LPC1785FBD208K](#)  
[LPC2124FBD64/01](#) [LS1020ASN7KQB](#) [LS1020AXN7HNB](#) [LS1020AXN7KQB](#) [LS1043ASE7PQA](#) [T1023RDB-PC](#) [FRDM-KW24D512](#)