DATA SHEET

74ALVC74
Dual D-type flip-flop with set and reset; positive-edge trigger

Product specification
Supersedes data of 2003 Jan 24

2003 May 26

Philips
Semiconductors

PHILIPS

Dual D-type flip-flop with set and reset; positive-edge trigger

74ALVC74

FEATURES

- Wide supply voltage range from 1.65 to 3.6 V
- Complies with JEDEC standard:
  JESD8-7 (1.65 to 1.95 V)
  JESD8-5 (2.3 to 2.7 V)
  JESD8B/JESD36 (2.7 to 3.6 V).
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.

DESCRIPTION

The 74ALVC74 is a dual positive-edge triggered, D-type flip-flop with individual data (D), clock (CP), set ($\overline{SD}$) and reset ($\overline{RD}$) inputs and complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	3.7	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	2.6	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	2.8	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	2.7	ns
t_{PHL}/t_{PLH}	propagation delay n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	3.5	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	2.5	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	3.1	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	2.3	ns
f_{max}	maximum clock frequency		425	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V; notes 1 and 2	35	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74ALVC74D	–40 to +85 °C	14	SO14	plastic	SOT108-1
74ALVC74PW	–40 to +85 °C	14	TSSOP14	plastic	SOT402-1
74ALVC74BQ	–40 to +85 °C	14	DHVQFN14	plastic	SOT762-1

FUNCTION TABLES

Table 1 See note 1

INPUT				OUTPUT	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Table 2 See note 1

INPUT				OUTPUT	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ_{n+1}	$n\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   ↑ = LOW-to-HIGH CP transition;
   Q_{n+1} = state after the next LOW-to-HIGH transition of CP.

Dual D-type flip-flop with set and reset; positive-edge trigger

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PINNING

PIN	SYMBOL	DESCRIPTION
1	$1\overline{R}D$	asynchronous reset-direct input (active LOW)
2	1D	data input
3	1CP	clock input (LOW-to-HIGH, edge-triggered)
4	$1\overline{S}D$	asynchronous set-direct input (active LOW)
5	1Q	true flip-flop output
6	$1\overline{Q}$	complement flip-flop output
7	GND	ground (0 V)
8	$2\overline{Q}$	complement flip-flop output
9	2Q	true flip-flop output
10	$2\overline{S}D$	asynchronous set-direct input (active LOW)
11	2CP	clock input (LOW-to-HIGH, edge-triggered)
12	2D	data input
13	$2\overline{R}D$	asynchronous reset-direct input (active LOW)
14	V_{CC}	supply voltage

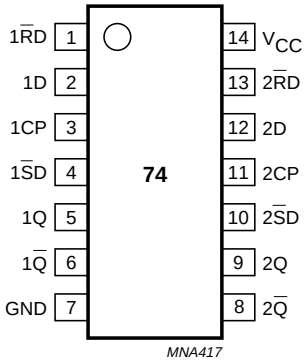
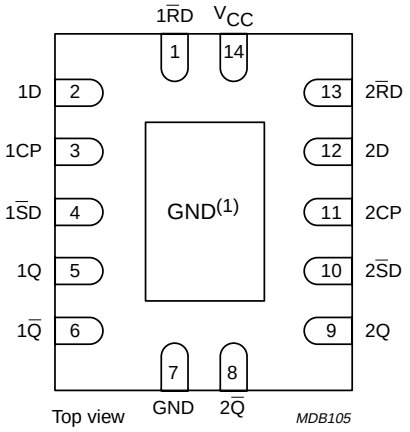


Fig.1 Pin configuration SO14 and TSSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

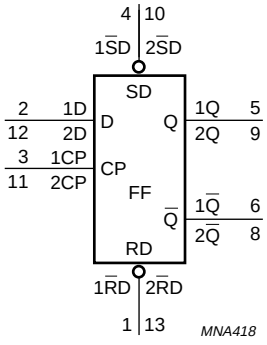


Fig.3 Logic symbol.

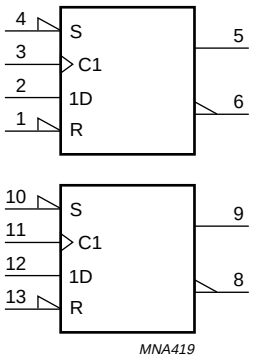


Fig.4 IEC logic symbol.

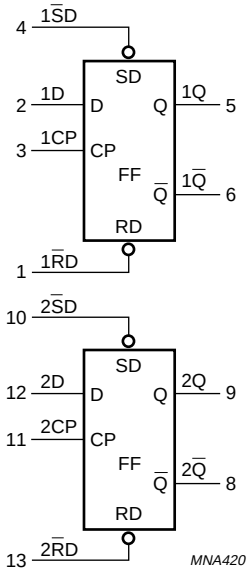


Fig.5 Functional diagram.

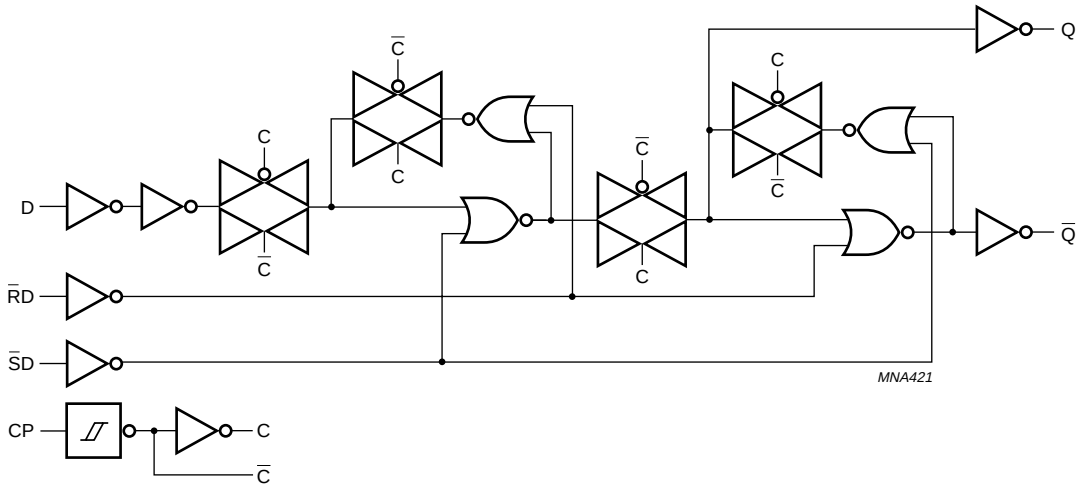


Fig.6 Logic diagram (one flip-flop).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	V_{CC} = 1.65 to 3.6 V	0	V_{CC}	V
		V_{CC} = 0 V; Power-down mode	0	3.6	V
T_{amb}	operating ambient temperature		–40	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+4.6	V
I_{IK}	input diode current	V_I < 0	–	–50	mA
V_I	input voltage		–0.5	+4.6	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0	–	±50	mA
V_O	output voltage	note 1	–0.5	V_{CC} + 0.5	V
		Power-down mode; note 2	–0.5	+4.6	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +85 °C; note 3	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 3.6 V in normal operation.
3. For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
   For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
   For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	1.65 to 3.6	–	–	0.2	V
		I_O = 6 mA	1.65	–	0.11	0.3	V
		I_O = 12 mA	2.3	–	0.17	0.4	V
		I_O = 18 mA	2.3	–	0.25	0.6	V
		I_O = 12 mA	2.7	–	0.16	0.4	V
		I_O = 18 mA	3.0	–	0.23	0.4	V
		I_O = 24 mA	3.0	–	0.30	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −100 μA	1.65 to 3.6	V_{CC} − 0.2	–	–	V
		I_O = −6 mA	1.65	1.25	1.51	–	V
		I_O = −12 mA	2.3	1.8	2.10	–	V
		I_O = −18 mA	2.3	1.7	2.01	–	V
		I_O = −12 mA	2.7	2.2	2.53	–	V
		I_O = −18 mA	3.0	2.4	2.76	–	V
		I_O = −24 mA	3.0	2.2	2.68	–	V
I_{LI}	input leakage current	V_I = 3.6 V or GND	3.6	–	±0.1	±5	μA
I_{off}	power OFF leakage current	V_I or V_O = 3.6 V	0.0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	3.6	–	0.2	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ − 0.6 V; I_O = 0	3.0 to 3.6	–	5	750	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

AC CHARACTERISTICS

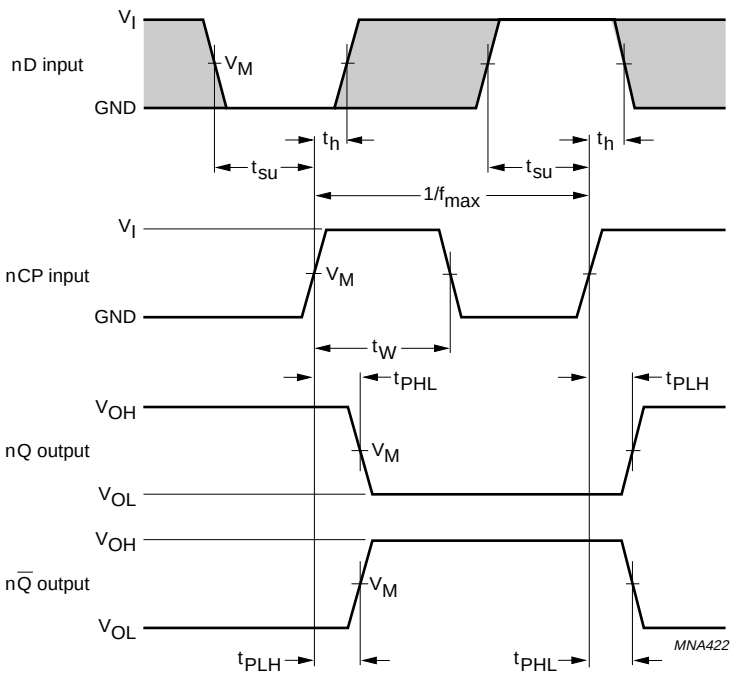
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$	see Figs 6 and 8	1.65 to 1.95	1.0	3.7	6.2	ns
			2.3 to 2.7	1.0	2.6	4.2	ns
			2.7	1.0	2.8	4.2	ns
			3.0 to 3.6	1.0	2.7	3.8	ns
t_{PHL}/t_{PLH}	propagation delay n$\overline{S}$D to nQ, n$\overline{Q}$	see Figs 7 and 8	1.65 to 1.95	1.0	3.4	5.4	ns
			2.3 to 2.7	1.0	2.4	3.8	ns
			2.7	1.0	3.2	4.2	ns
			3.0 to 3.6	1.0	2.3	3.5	ns
t_{PHL}/t_{PLH}	propagation delay n$\overline{R}$D to nQ, n$\overline{Q}$	see Figs 7 and 8	1.65 to 1.95	1.0	3.5	5.4	ns
			2.3 to 2.7	1.0	2.5	3.8	ns
			2.7	1.0	3.1	4.3	ns
			3.0 to 3.6	1.0	2.3	3.5	ns
t_W	clock pulse width HIGH or LOW	see Figs 6 and 8	1.65 to 1.95	2.5	0.9	–	ns
			2.3 to 2.7	2.5	0.6	–	ns
			2.7	2.5	1.3	–	ns
			3.0 to 3.6	2.5	1.3	–	ns
t_W	set or reset pulse width LOW	see Figs 7 and 8	1.65 to 1.95	2.5	0.9	–	ns
			2.3 to 2.7	2.5	0.9	–	ns
			2.7	2.5	1.0	–	ns
			3.0 to 3.6	2.5	0.7	–	ns
t_{rem}	removal time set or reset	see Figs 7 and 8	1.65 to 1.95	0.7	–0.2	–	ns
			2.3 to 2.7	0.7	–0.1	–	ns
			2.7	0.7	–0.1	–	ns
			3.0 to 3.6	0.7	–0.1	–	ns
t_{su}	set-up time nD to nCP	see Figs 6 and 8	1.65 to 1.95	1.2	0.6	–	ns
			2.3 to 2.7	1.2	0.8	–	ns
			2.7	0.9	0.5	–	ns
			3.0 to 3.6	0.8	0.4	–	ns
t_h	hold time nD to nCP	see Figs 6 and 8	1.65 to 1.95	0.6	–0.4	–	ns
			2.3 to 2.7	0.6	–0.3	–	ns
			2.7	0.7	–0.4	–	ns
			3.0 to 3.6	0.8	–0.1	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
f_{max}	maximum clock pulse frequency	see Figs 6 and 8	1.65 to 1.95	150	275	–	MHz
			2.3 to 2.7	200	325	–	MHz
			2.7	250	375	–	MHz
			3.0 to 3.6	300	425	–	MHz

Note

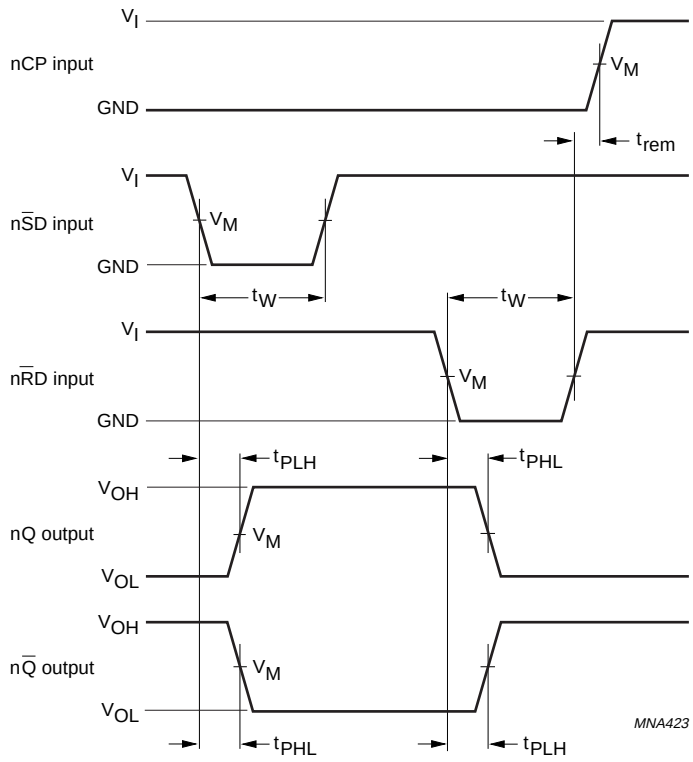
1. All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS



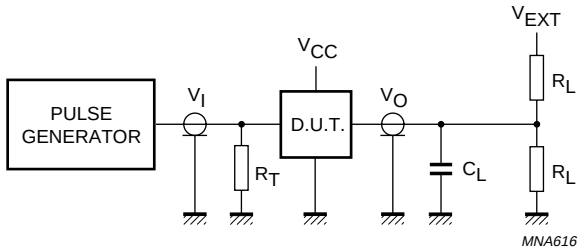
V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

Fig.6 The clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

Fig.7 The set ($n\overline{S}D$) and reset ($n\overline{R}D$) input to output (nQ, $n\overline{Q}$) propagation delays, the set and reset pulse widths and the $n\overline{R}D$ to nCP removal time.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.65 to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V

Definitions for test circuits:

R_L = Load resistor.

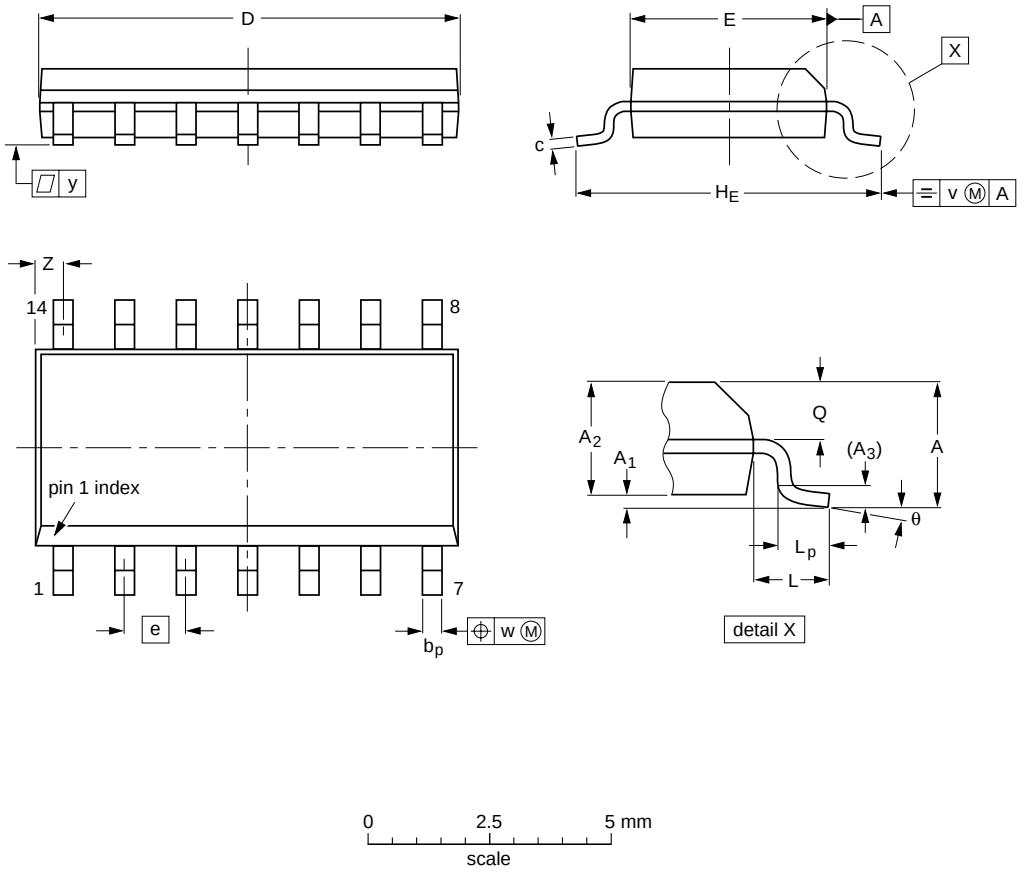
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

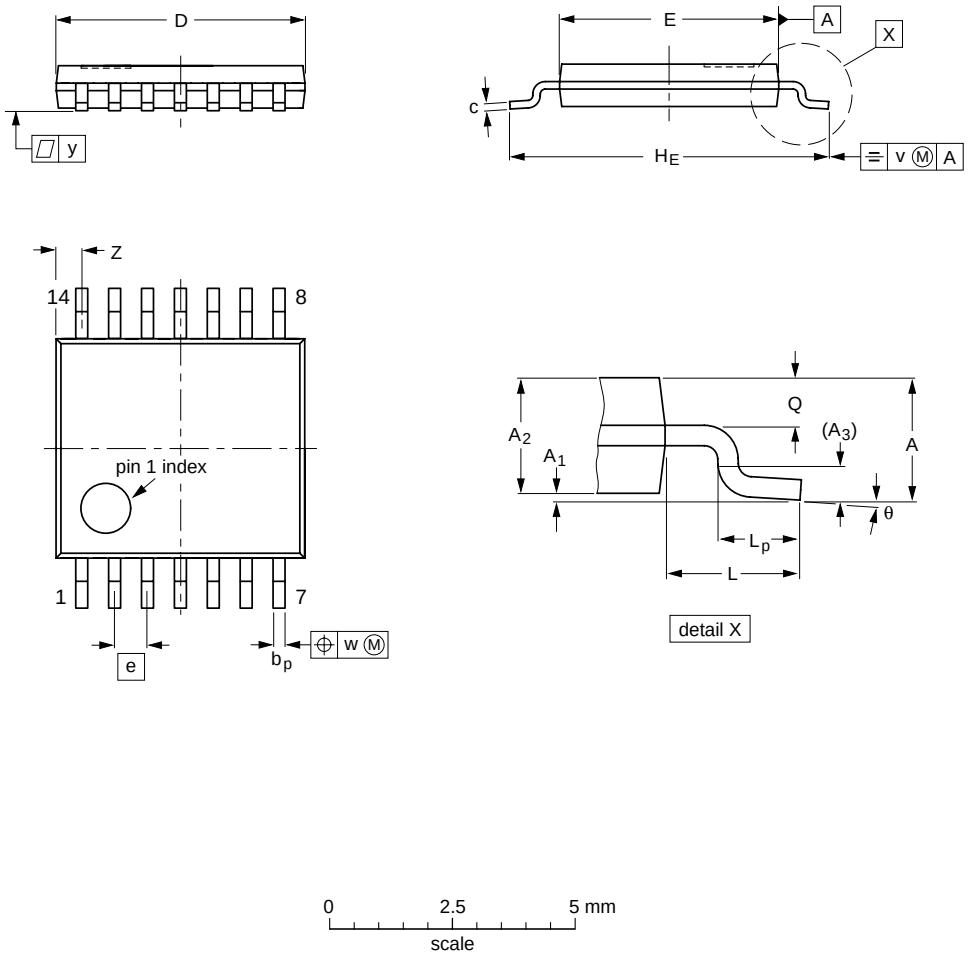
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

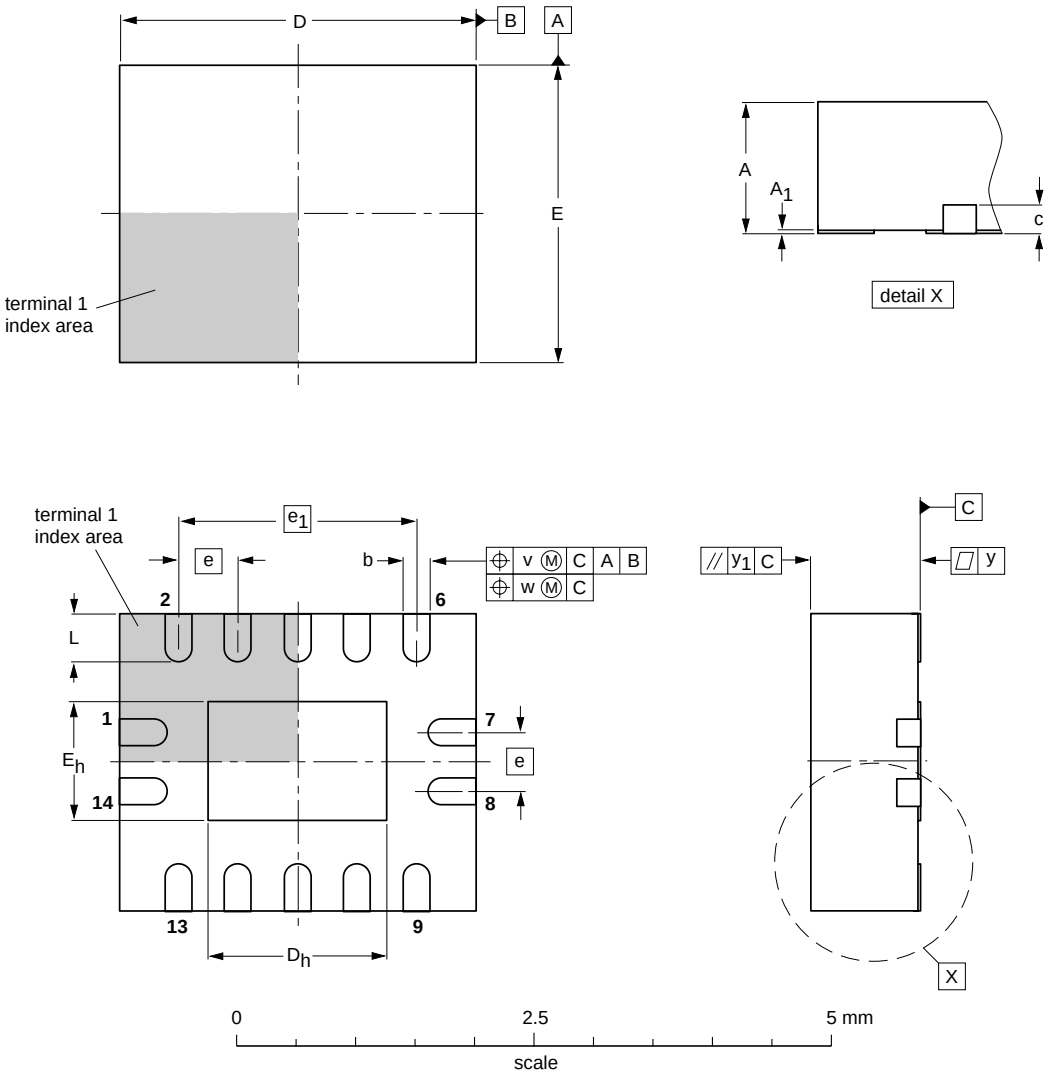
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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