74ALVT16244

16-bit buffer/line driver; 3-state

Rev. 5 — 2 February 2018 Product data sheet

1 General description

The 74ALVT16244 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-state bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

2 Features and benefits

- 16-bit bus interface
- 3-State buffers
- 5V I/O compatible
- Output capability: +64 mA/–32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - JESD17: exceeds 500 mA
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - MM exceeds 200 V

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVT16244DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4 Functional diagram

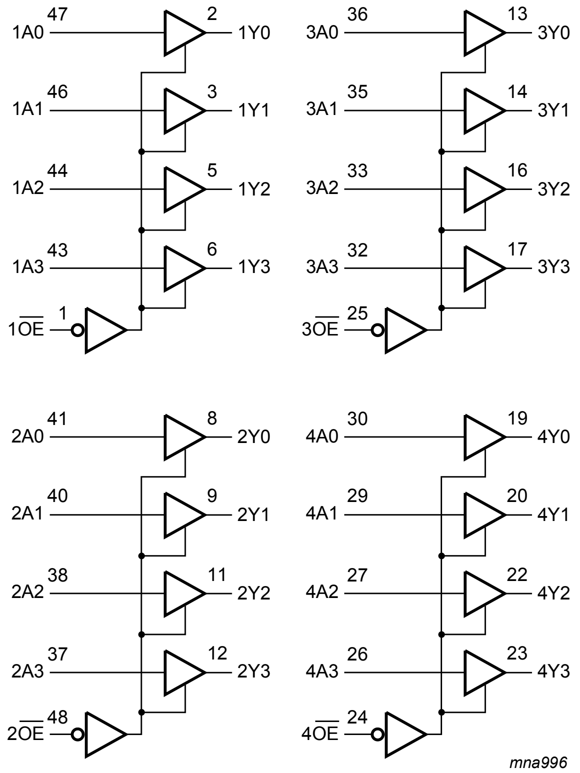

Figure 1. Logic symbol

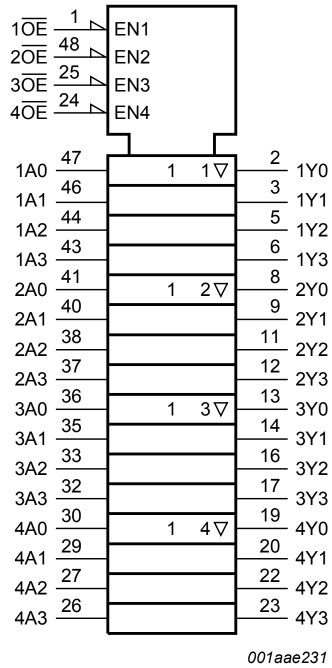

Figure 2. IEC logic symbol

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5 Pinning information

5.1 Pinning

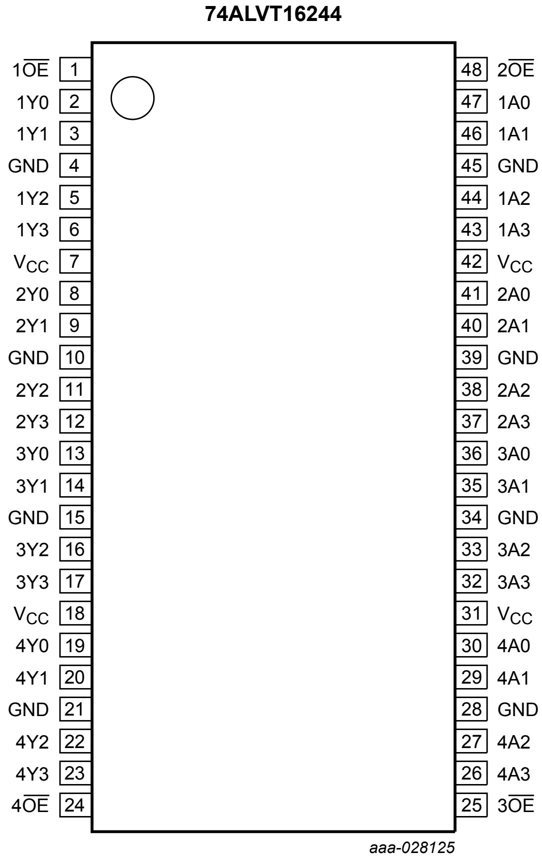

Figure 3. Pin configuration SOT362-1 (TSSOP48)

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$	1, 48, 25, 24	output enable inputs (active LOW)
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data inputs
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data inputs
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data inputs
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data inputs
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data outputs
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data outputs
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data outputs
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage

6 Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
n$\overline{OE}$	**nAn**	**nYn**
L	L	L
L	H	H
H	X	Z

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7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	V_I < 0 V	-50	-	mA
I_{OK}	output clamping current	V_O < 0 V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[2]	-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		Unit
			Min	Max	Min	Max	
V_{CC}	supply voltage		2.3	2.7	3.0	3.6	V
V_I	input voltage		0	5.5	0	5.5	V
I_{OH}	HIGH-level output current		-	−8	-	−32	mA
I_{OL}	LOW-level output current	none	-	8	-	32	mA
		current duty cycle ≤ 50 %; f_i ≥ 1 kHz	-	24	-	64	mA
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	10	-	10	ns/V
T_{amb}	ambient temperature	free-air	−40	+85	−40	+85	°C

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; T_{amb} = -40 °C to +85 °C ; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{CC} = 2.5 V ± 0.2 V						
V_{IK}	input clamping voltage	V_{CC} = 2.3 V; I_{IK} = -18 mA	-	-0.85	-1.2	V
V_{IH}	HIGH-level input voltage	V_{CC} = 2.5 V ± 0.2 V	1.7	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.5 V ± 0.2 V	-	-	0.7	V

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Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	V_{CC} = 2.5 V ± 0.2 V; I_O = -100 µA		V_{CC} − 0.2	V_{CC}	-	V
		V_{CC} = 2.3 V; I_O = -8 mA		1.8	2.5	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.3 V; I_O = 100 µA		-	0.07	0.2	V
		V_{CC} = 2.3 V; I_O = 24 mA		-	0.3	0.5	V
I_I	input leakage current	all input pins	[2]				
		V_{CC} = 0 V or 2.7 V; V_I = 5.5 V		-	0.1	10	µA
		control pins					
		V_{CC} = 2.7 V; V_I = V_{CC} or GND		-	0.1	±1	µA
		data pins;	[2]				
		V_{CC} = 2.7 V; V_I = V_{CC}		-	0.1	1	µA
		V_{CC} = 2.7 V; V_I = 0 V		-	0.1	-5	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		-	0.1	±100	µA
I_{BHL}	bus hold LOW current	data inputs; V_{CC} = 2.3 V; V_I = 0.7 V	[3]	-	115	-	µA
I_{BHH}	bus hold HIGH current	data inputs; V_{CC} = 2.3 V; V_I = 1.7 V	[3]	-	-10	-	µA
I_{EX}	external current	output in HIGH-state when V_O > V_{CC}; V_O = 5.5 V; V_{CC} = 2.3 V		-	10	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care	[4]	-	1	±100	µA
I_{OZ}	OFF-state output current	V_{CC} = 2.7 V; V_I = V_{IL} or V_{IH}					
		output HIGH: V_O = 2.3V		-	0.5	5	µA
		output LOW: V_O = 0.5 V		-	0.5	-5	µA
I_{CC}	supply current	V_{CC} = 2.7 V; V_I = GND or V_{CC}; I_O = 0 A					
		outputs HIGH		-	0.04	0.1	mA
		outputs LOW		-	2.5	4.5	mA
		outputs disabled	[5]	-	0.04	0.1	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.3 V to 2.7 V; one input at V_{CC} - 0.6 V; other inputs at V_{CC} or GND	[6]	-	0.04	0.4	mA
C_I	input capacitance	$n\overline{OE}$; V_I = 0 V or V_{CC}		-	3	-	pF
C_O	output capacitance	V_O = 0 V or V_{CC}		-	9	-	pF
V_{CC} = 3.3 V ± 0.3 V							
V_{IK}	input clamping voltage	V_{CC} = 3.0 V; I_{IK} = -18 mA		-	-0.85	-1.2	V
V_{IH}	HIGH-level input voltage	V_{CC} = 3.3 V ± 0.3 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 3.3 V ± 0.3 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC} = 3.3 V ± 0.3 V; I_O = -100 µA		V_{CC} − 0.2	V_{CC}	-	V
		V_{CC} = 3.0 V; I_O = -32 mA		2.0	2.3	-	V

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Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{OL}	LOW-level output voltage	V_{CC} = 3.0 V; I_O = 100 μA	-	0.07	0.2	V
		V_{CC} = 3.0 V; I_O = 16 mA	-	0.25	0.4	V
		V_{CC} = 3.0 V; I_O = 32 mA	-	0.3	0.5	V
		V_{CC} = 3.0 V; I_O = 64 mA	-	0.4	0.55	V
I_I	input leakage current	all input pins [2]				
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	0.1	10	μA
		control pins				
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	0.1	±1	μA
		data pins [2]				
		V_{CC} = 3.6 V; V_I = V_{CC}	-	0.5	1	μA
		V_{CC} = 3.6 V; V_I = 0 V	-	0.1	-5	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	0.1	±100	μA
I_{BHL}	bus hold LOW current	data inputs; V_{CC} = 3 V; V_I = 0.8 V	75	130	-	μA
I_{BHH}	bus hold HIGH current	data inputs; V_{CC} = 3 V; V_I = 2.0 V	-75	-140	-	μA
I_{BHLO}	bus hold LOW overdrive current	data inputs; V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [7]	500	-	-	μA
I_{BHHO}	bus hold HIGH overdrive current	data inputs; V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [7]	-500	-	-	μA
I_{EX}	external current	output in HIGH-state when V_O > V_{CC}; V_O = 5.5 V; V_{CC} = 3.0 V	-	10	125	μA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care [8]	-	1	±100	μA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IL} or V_{IH}				
		output HIGH: V_O = 3.0V	-	0.5	5	μA
		output LOW: V_O = 0.5 V	-	0.5	-5	μA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A				
		outputs HIGH	-	0.05	0.1	mA
		outputs LOW	-	3.6	5	mA
		outputs disabled [5]	-	0.06	0.1	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3 V to 3.6 V; one input at V_{CC} - 0.6 V; other inputs at V_{CC} or GND [6]	-	0.04	0.4	mA
C_I	input capacitance	$n\overline{OE}$; V_I = 0 V or V_{CC}	-	3	-	pF
C_O	output capacitance	V_O = 0 V or V_{CC}	-	9	-	pF

[1] Typical values for V_{CC} = 2.5 V ± 0.2 V are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
Typical values for V_{CC} = 3.3 V ± 0.3 V are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
[2] Unused pins at V_{CC} or GND.
[3] Not guaranteed.
[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
From V_{CC} = 1.2 V to V_{CC} = 2.5 V ± 0.2 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.
[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.
[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
[7] This is the bus hold overdrive current required to force the input to the opposite logic state.
[8] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.

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10 Dynamic characteristics

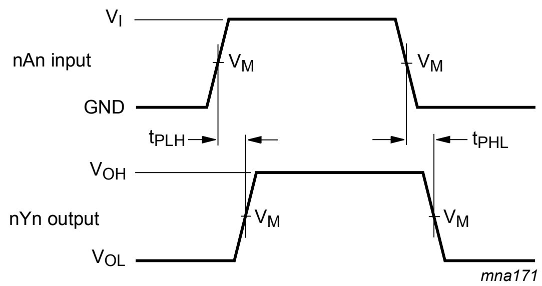
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +85 °C; for test circuit see Figure 6.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{CC} = 2.5 V ± 0.2 V						
t_{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Figure 4	1.0	1.8	3.0	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Figure 4	1.0	1.9	3.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nYn; see Figure 5	2.0	3.1	5.9	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nYn; see Figure 5	1.5	2.5	4.7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nYn; see Figure 5	1.5	2.7	4.4	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nYn; see Figure 5	1.0	2.0	3.4	ns
V_{CC} = 3.3 V ± 0.3 V						
t_{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Figure 4	0.8	1.5	2.4	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Figure 4	0.8	1.5	2.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nYn; see Figure 5	1.0	2.3	3.8	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nYn; see Figure 5	0.5	1.8	2.9	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nYn; see Figure 5	1.5	2.7	4.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nYn; see Figure 5	1.5	2.3	3.6	ns

[1] Typical values for V_{CC} = 2.5 V ± 0.2 V are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
Typical values for V_{CC} = 3.3 V ± 0.3 V are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

10.1 Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 4. Inputs nAn to output nYn propagation delays

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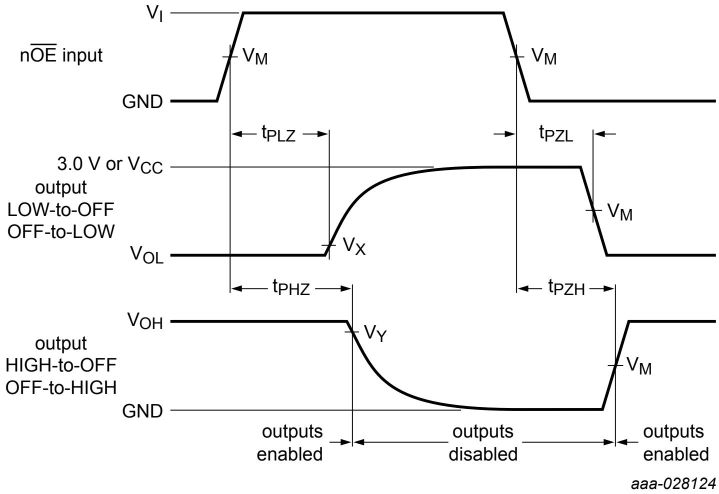

Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. OFF-state to HIGH or LOW and HIGH or LOW to OFF-state propagation delays

Table 8. Measurement points

V_{CC}	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
$V_{CC} \leq 2.7$ V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
$V_{CC} \geq 3.0$ V	3.0 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V

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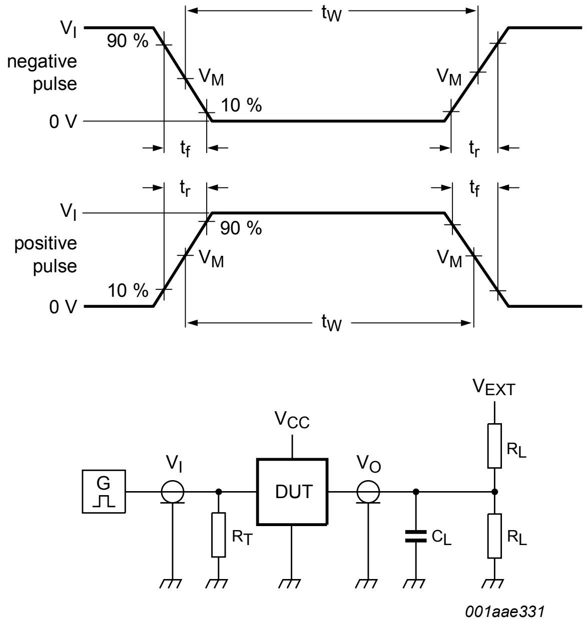

Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Figure 6. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V or V_{CC} whichever is less	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V or V_{CC} x 2	open

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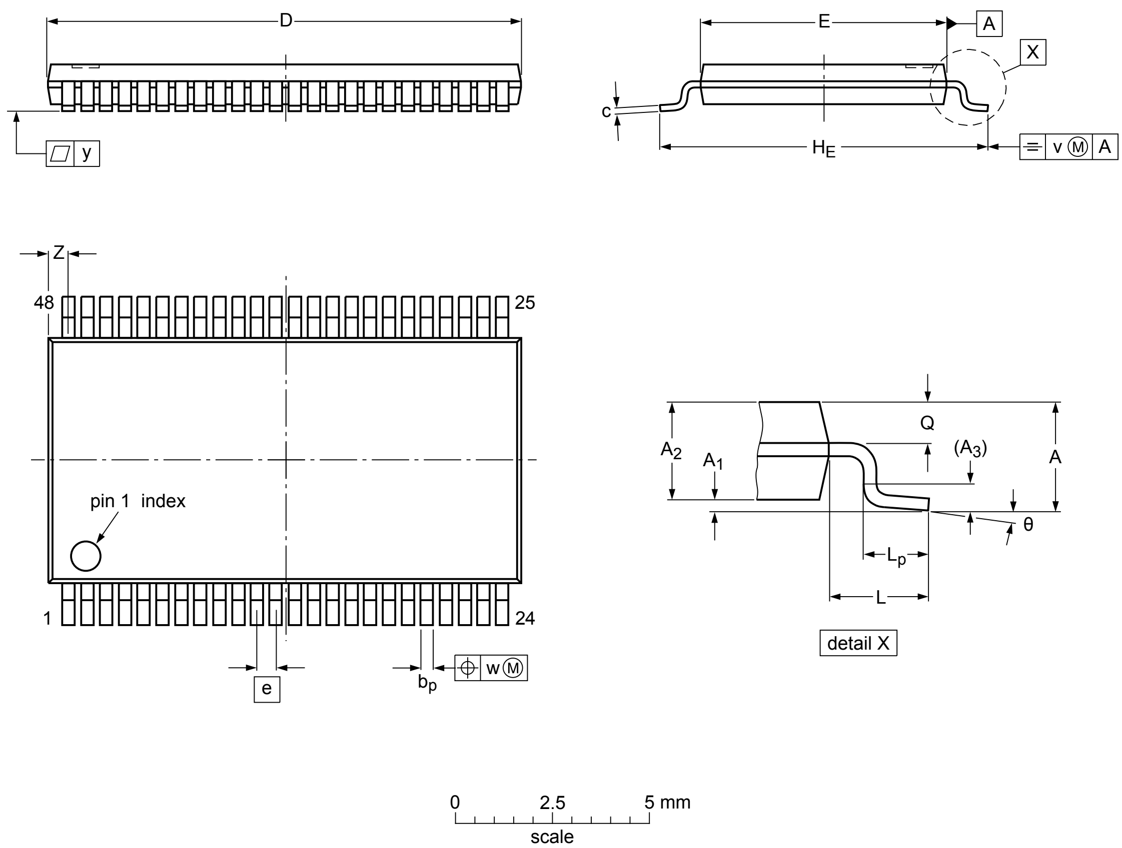
11 Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom	1.2			0.25					0.5		1			0.25	0.08	0.1		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~03-02-19~~ 13-08-05

Figure 7. Package outline SOT362-1 (TSSOP48)

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12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVT16244 v.5	20180202	Product data sheet	-	74ALVT16244 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74ALVT16244DL (SOT370-1 / SSOP48) removed.			
74ALVT16244 v.4	19981007	Product specification	-	74ALVT16244 v.3
74ALVT16244 v.3	19980213	Product specification	-	74ALVT16244 v.2
74ALVT16244 v.2	19980213	Product specification	-	74ALVT16244 v.1
74ALVT16244 v.1	19960529	Product specification	-	-

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14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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Date of release: 2 February 2018
Document identifier: 74ALVT16244

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