# Low-power 2-input EXCLUSIVE-OR gate Rev. 5 — 28 June 2012

**Product data sheet** 

#### **General description** 1.

The 74AUP1G86 provides the single 2-input EXCLUSIVE-OR function.

Schmitt-trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V<sub>CC</sub> range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V<sub>CC</sub> range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I<sub>OFF</sub>.

The I<sub>OFF</sub> circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

#### 2. **Features and benefits**

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - ◆ JESD8-12 (0.8 V to 1.3 V)
  - ◆ JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 5000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; I<sub>CC</sub> = 0.9 μA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V<sub>CC</sub>
- I<sub>OFF</sub> circuitry provides partial power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



# 3. Ordering information

Table 1. Ordering information

Type number	Package							
	Temperature range Name		Description	Version				
74AUP1G86GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1				
74AUP1G86GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 $\times$ 1.45 $\times$ 0.5 mm	SOT886				
74AUP1G86GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 $\times$ 1 $\times$ 0.5 mm	SOT891				
74AUP1G86GN	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115				
74AUP1G86GS	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 $\times$ 1.0 $\times$ 0.35 mm	SOT1202				
74AUP1G86GX	–40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body $0.8 \times 0.8 \times 0.35$ mm	SOT1226				

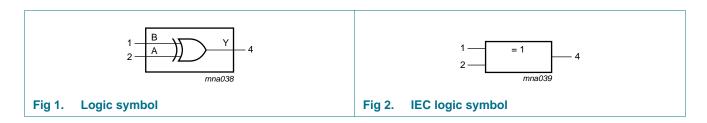
# 4. Marking

Table 2. Marking

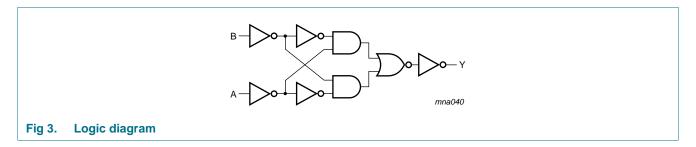
Type number	Marking code <sup>[1]</sup>
74AUP1G86GW	рН
74AUP1G86GM	рН
74AUP1G86GF	рН
74AUP1G86GN	рН
74AUP1G86GS	рН
74AUP1G86GX	рН

<sup>[1]</sup> The pin 1 indicator is located on the lower left corner of the device, below the marking code.

# 5. Functional diagram



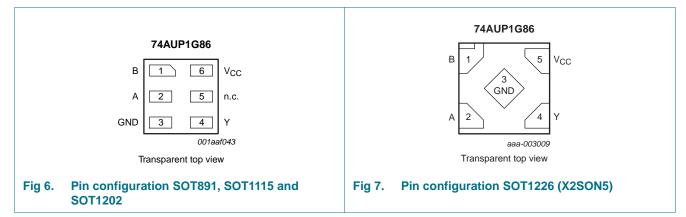
#### Low-power 2-input EXCLUSIVE-OR gate



# 6. Pinning information

### 6.1 Pinning





Low-power 2-input EXCLUSIVE-OR gate

### 6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5 and X2SON5	XSON6	
В	1	1	data input
Α	2	2	data input
GND	3	3	ground (0 V)
Υ	4	4	data output
n.c.	-	5	not connected
V <sub>CC</sub>	5	6	supply voltage

# 7. Functional description

Table 4. Function table[1]

Input		Output
Α	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level.

# 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
$V_{I}$	input voltage		<u>[1]</u> –0.5	+4.6	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
V <sub>O</sub>	output voltage	Active mode and Power-down mode	<u>[1]</u> –0.5	+4.6	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±20	mA
I <sub>CC</sub>	supply current		-	+50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb}$ = -40 °C to +125 °C	[2] -	250	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>[2]</sup> For TSSOP5 packages: above 87.5  $^{\circ}$ C the value of P<sub>tot</sub> derates linearly with 4.0 mW/K. For XSON6 and X2SON5 packages: above 118  $^{\circ}$ C the value of P<sub>tot</sub> derates linearly with 7.8 mW/K.

Low-power 2-input EXCLUSIVE-OR gate

# 9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		0.8	3.6	V
$V_{I}$	input voltage		0	3.6	V
V <sub>O</sub>	output voltage	Active mode	0	$V_{CC}$	V
		Power-down mode; V <sub>CC</sub> = 0 V	0	3.6	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	0	200	ns/V

# 10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T <sub>amb</sub> = 2	5 °C					
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20 \mu A$ ; $V_{CC} = 0.8 \text{ V}$ to 3.6 V	V <sub>CC</sub> - 0.1	-	-	V
		$I_{O} = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.75 \times V_{CC}$	-	-	V
		$I_{O} = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	1.11	-	-	V
		$I_{O} = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.32	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	2.05	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.72	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.6	-	-	V
$V_{OL}$	LOW-level output voltage	$V_{I} = V_{IH}$ or $V_{IL}$				
		$I_O$ = 20 $\mu$ A; $V_{CC}$ = 0.8 $V$ to 3.6 $V$	-	-	0.1	V
		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	$0.3 \times V_{CC}$	V
		$I_{O} = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.31	V
		$I_{O} = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.31	V
		$I_{O} = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.31	V
		$I_{O} = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.44	V
		$I_{O} = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.31	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.44	V
74AUP1G86		All information provided in this document is subject to legal disclaimers	i		© NXP B.V. 2012. All righ	nts reserve

# Low-power 2-input EXCLUSIVE-OR gate

**Table 7. Static characteristics** ...continued
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
l <sub>l</sub>	input leakage current	$V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V	-	-	±0.1	μΑ
OFF	power-off leakage current	$V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V	-	-	±0.2	μΑ
$\Delta I_{OFF}$	additional power-off leakage current	$V_1$ or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.2	μΑ
CC	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.5	μΑ
Δl <sub>CC</sub>	additional supply current	$V_1 = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}$	[1] -	-	40	μΑ
Cı	input capacitance	$V_{CC}$ = 0 V to 3.6 V; $V_I$ = GND or $V_{CC}$	-	0.8	-	рF
Co	output capacitance	$V_O = GND; V_{CC} = 0 V$	-	1.7	-	рF
T <sub>amb</sub> = -	40 °C to +85 °C					
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_{O} = -20 \mu A$ ; $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> - 0.1	-	-	V
		$I_{O} = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.7 \times V_{CC}$	-	-	٧
		$I_{O} = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	1.03	-	-	٧
		$I_{O} = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.30	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.97	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.85	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.67	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.55	-	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20 \mu A$ ; $V_{CC} = 0.8 \text{ V}$ to 3.6 V	-	-	0.1	V
		$I_O = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.37	V
		$I_O = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.35	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.33	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.33	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.45	V
   <sub> </sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.5	μΑ
l <sub>OFF</sub>	power-off leakage current	$V_1$ or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.5	μΑ
$\Delta l_{OFF}$	additional power-off	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.6	μΑ

### Low-power 2-input EXCLUSIVE-OR gate

**Table 7. Static characteristics** ...continued
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Uni
CC	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.9	μΑ
7I <sup>CC</sup>	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}$	<u>[1]</u> -	-	50	μΑ
Γ <sub>amb</sub> = -	40 °C to +125 °C					
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	$0.75 \times V_{CC}$	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	-	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
/ <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	$0.25 \times V_{CC}$	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20 \mu A$ ; $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> - 0.11	-	-	V
		$I_O = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.6 \times V_{CC}$	-	-	V
		$I_O = -1.7 \text{ mA}$ ; $V_{CC} = 1.4 \text{ V}$	0.93	-	-	V
		$I_O = -1.9 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	1.17	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.77	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.67	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.40	-	-	V
		$I_O = -4.0 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	2.30	-	-	V
/ <sub>OL</sub>	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20 \mu A$ ; $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.11	V
		$I_O = 1.1 \text{ mA}$ ; $V_{CC} = 1.1 \text{ V}$	-	-	$0.33 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}$ ; $V_{CC} = 1.4 \text{ V}$	-	-	0.41	V
		$I_O = 1.9 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	-	-	0.39	V
		$I_O = 2.3 \text{ mA}$ ; $V_{CC} = 2.3 \text{ V}$	-	-	0.36	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.50	V
		$I_O = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.50	V
l	input leakage current	$V_{I} = GND \text{ to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.75	μΑ
OFF	power-off leakage current	$V_{I}$ or $V_{O} = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	±0.75	μΑ
VI <sub>OFF</sub>	additional power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V to 0.2 V	-	-	±0.75	μΑ
СС	supply current	V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	1.4	μΑ
VI <sub>CC</sub>	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}$	[1] -	-	75	μΑ

<sup>[1]</sup> One input at  $V_{CC}$  – 0.6 V, other input at  $V_{CC}$  or GND.

# Low-power 2-input EXCLUSIVE-OR gate

# 11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T <sub>amb</sub> = 25	°C; C <sub>L</sub> = 5 pF						
t <sub>pd</sub>	propagation delay	A or B to Y; see Figure 8	[2]				
		V <sub>CC</sub> = 0.8 V		-	21.2	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		2.3	5.9	13.1	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		1.8	4.1	7.7	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.5	3.3	5.9	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.2	2.6	4.4	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.0	2.3	4.0	ns
T <sub>amb</sub> = 25	°C; C <sub>L</sub> = 10 pF						
t <sub>pd</sub>	propagation delay	A or B to Y; see Figure 8	[2]				
		V <sub>CC</sub> = 0.8 V		-	24.7	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V		2.6	6.8	14.8	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		2.2	4.8	8.7	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.8	3.9	6.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.5	3.1	5.2	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.3	2.9	4.8	ns
T <sub>amb</sub> = 25	°C; C <sub>L</sub> = 15 pF						
t <sub>pd</sub>	propagation delay	A or B to Y; see Figure 8	[2]				
		V <sub>CC</sub> = 0.8 V		-	28.2	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		3.0	7.6	16.5	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		2.4	5.3	9.6	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		2.1	4.4	7.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.8	3.6	5.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.6	3.3	5.4	ns
T <sub>amb</sub> = 25	°C; C <sub>L</sub> = 30 pF						
t <sub>pd</sub>	propagation delay	A or B to Y; see Figure 8	[2]				
		V <sub>CC</sub> = 0.8 V		-	38.5	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		3.9	9.9	21.5	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		3.2	6.9	12.5	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		2.8	5.7	9.8	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2.4	4.7	7.6	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		2.2	4.4	7.1	ns

### Low-power 2-input EXCLUSIVE-OR gate

 Table 8.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9

Symbol	Parameter	Conditions	N	Min	Typ[1]	Max	Unit
<b>T</b> <sub>amb</sub> = 25	°C						
$C_{PD}$	power dissipation capacitance	$f = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}$	[3]				
		$V_{CC} = 0.8 \text{ V}$		-	2.7	-	pF
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		-	2.9	-	pF
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		-	3.0	-	pF
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		-	3.1	-	pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-	3.6	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		-	4.2	-	pF

<sup>[1]</sup> All typical values are measured at nominal  $V_{CC}$ .

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}{}^2 \times f_o) \text{ where:}$ 

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9

Symbol	Parameter	Conditions		–40 °C t	o +85 °C	-40 °C to	+125 °C	Unit
				Min	Max	Min	Max	
$C_L = 5 pF$								
t <sub>pd</sub>	propagation delay	A or B to Y; see Figure 8	<u>[1]</u>					
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		2.1	14.3	2.1	15.8	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		1.6	8.8	1.6	9.7	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.4	6.9	1.4	7.6	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.1	5.3	1.1	5.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		0.9	4.7	0.9	5.2	ns
C <sub>L</sub> = 10 pF								
t <sub>pd</sub>	propagation delay	A or B to Y; see Figure 8	<u>[1]</u>					
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		2.4	16.2	2.4	17.9	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		1.9	10.0	1.9	11.0	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.7	8.0	1.7	8.8	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.4	6.2	1.4	6.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.3	5.6	1.3	6.2	ns

<sup>[2]</sup>  $t_{pd}$  is the same as  $t_{PZL}$  and  $t_{PLZ}$ .

<sup>[3]</sup>  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

### Low-power 2-input EXCLUSIVE-OR gate

 Table 9.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9

Symbol	Parameter	Conditions		–40 °C t	o +85 °C	–40 °C to	+125 °C	Unit
				Min	Max	Min	Max	
$C_L = 15 pF$	:				'		•	
t <sub>pd</sub>	propagation delay	A or B to Y; see Figure 8	<u>[1]</u>					
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		2.7	18.1	2.7	20.0	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		2.2	11.3	2.2	12.5	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.9	9.0	1.9	9.9	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.6	7.0	1.6	7.7	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.5	6.4	1.5	7.1	ns
$C_L = 30 pF$								
t <sub>pd</sub>	propagation delay	A or B to Y; see Figure 8	<u>[1]</u>					
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		3.5	24.1	3.5	26.6	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		2.8	14.8	2.8	16.3	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		2.5	11.7	2.5	12.9	ns ns ns ns ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2.2	9.1	2.2	10.1	
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		2.1	8.3	2.1	9.2	ns

<sup>[1]</sup>  $t_{pd}$  is the same as  $t_{PZL}$  and  $t_{PLZ}$ .

### 12. Waveforms

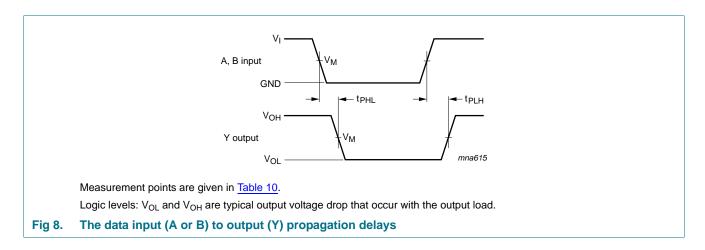
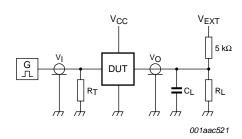


Table 10. Measurement points

Supply voltage	Output	Input		
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>I</sub>	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>CC</sub>	≤ 3.0 ns

### Low-power 2-input EXCLUSIVE-OR gate



Test data is given in Table 11.

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

 $V_{\text{EXT}}$  = External voltage for measuring switching times.

Fig 9. Test circuit for measuring switching times

#### Table 11. Test data

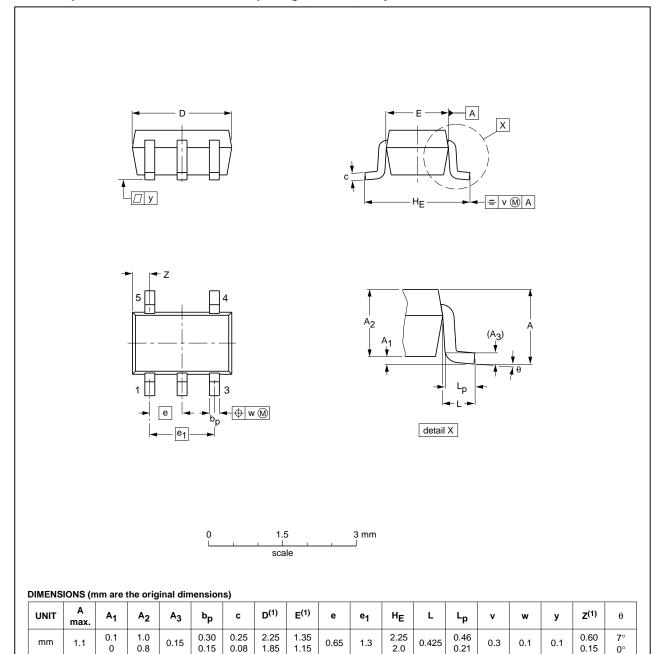
Supply voltage	Load		V <sub>EXT</sub>		
V <sub>CC</sub>	C <sub>L</sub>	R <sub>L</sub> [1]	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k $\Omega$ or 1 M $\Omega$	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times  $R_L$  = 5  $k\Omega$ , for measuring propagation delays, setup and hold times and pulse width  $R_L$  = 1  $M\Omega$ .

# 13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



#### . . .

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT353-1		MO-203	SC-88A			<del>-00-09-01</del> 03-02-19

Fig 10. Package outline SOT353-1 (TSSOP5)

74AUP1G86 All information provided in this document is subject to legal disclaimers.

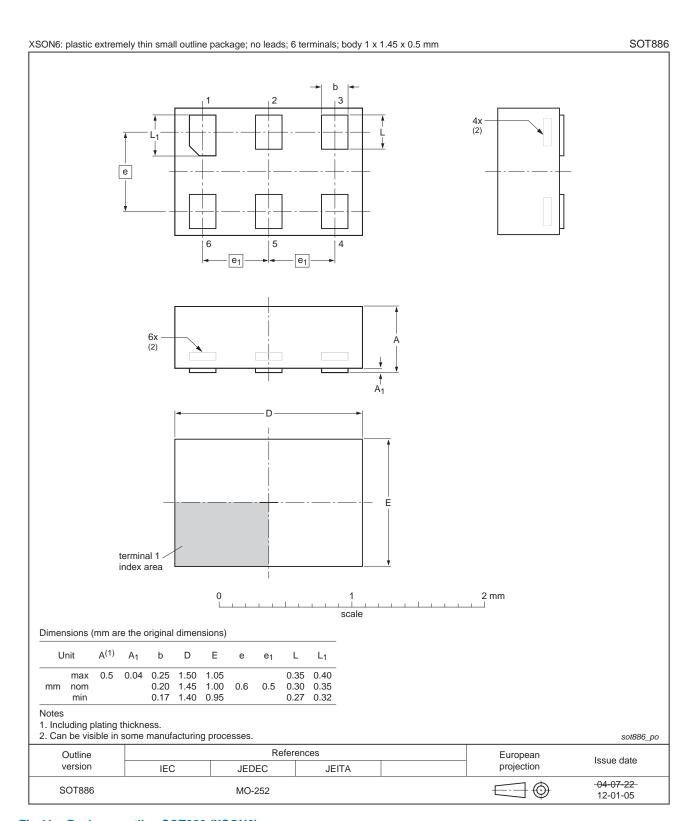


Fig 11. Package outline SOT886 (XSON6)

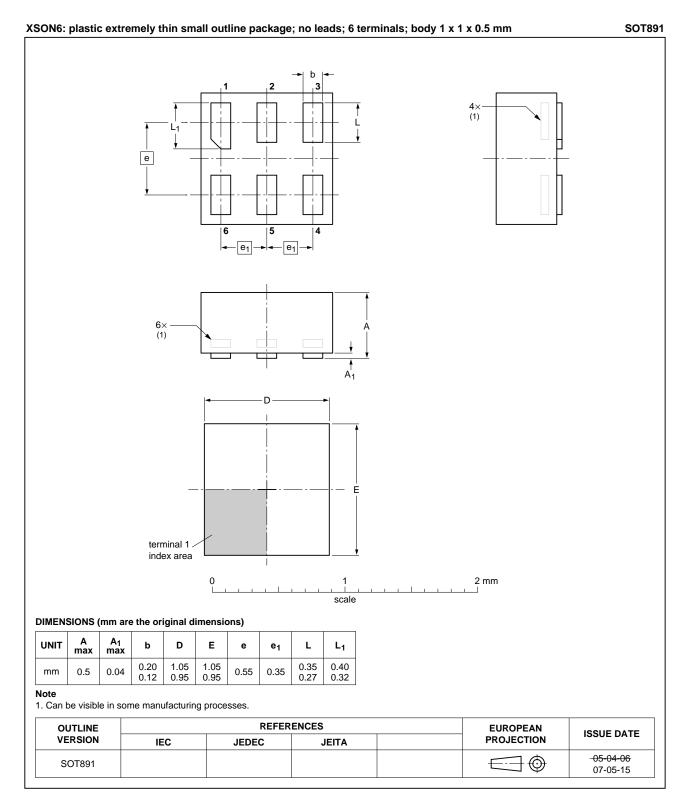


Fig 12. Package outline SOT891 (XSON6)

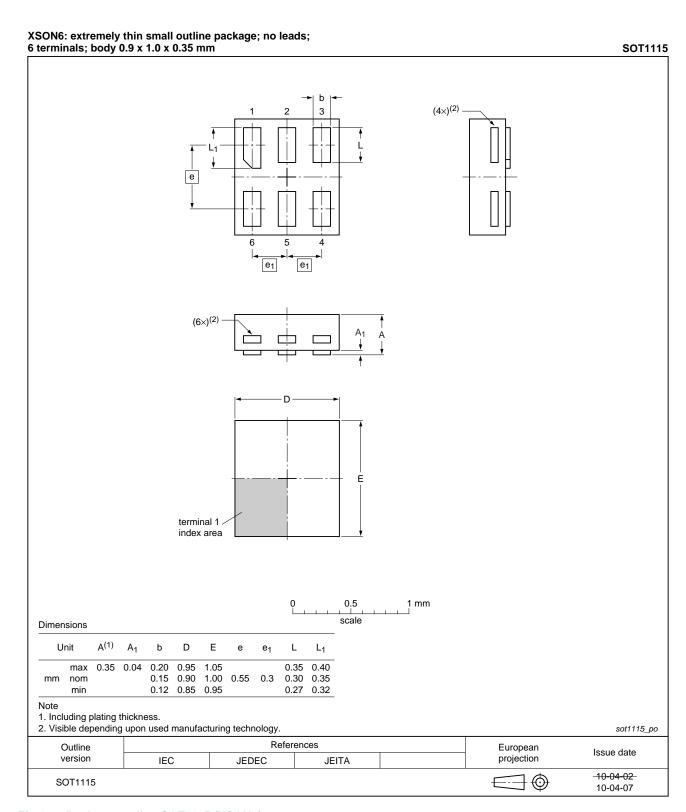


Fig 13. Package outline SOT1115 (XSON6)

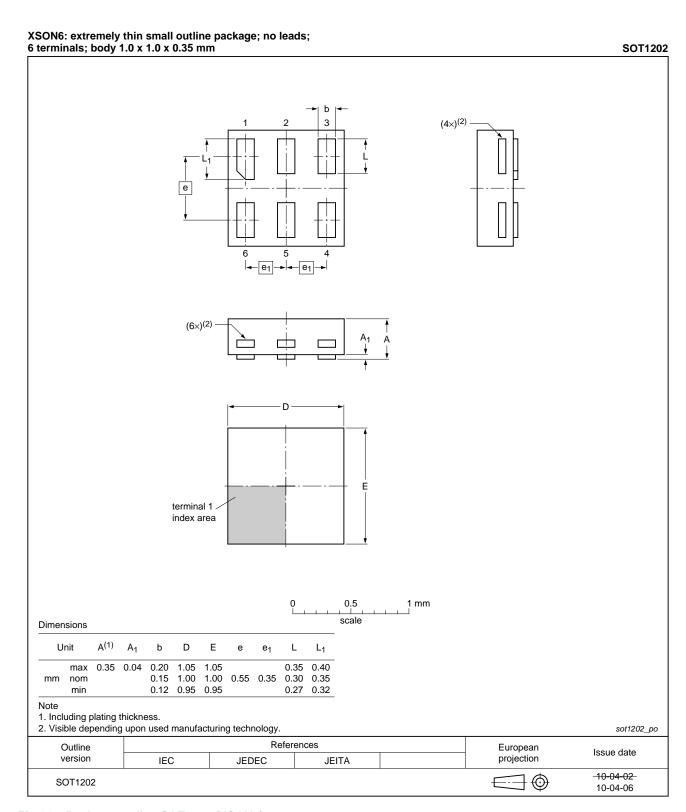


Fig 14. Package outline SOT1202 (XSON6)

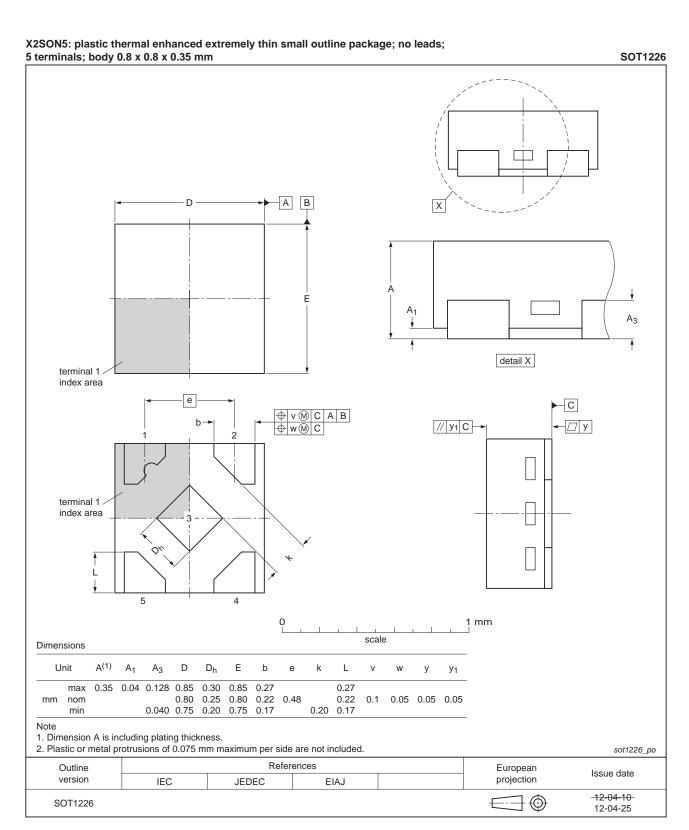


Fig 15. Package outline SOT1226 (X2SON5)

Rev. 5 — 28 June 2012

# Low-power 2-input EXCLUSIVE-OR gate

# 14. Abbreviations

#### Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

# 15. Revision history

### Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G86 v.5	20120628	Product data sheet	-	74AUP1G86 v.4
Modifications:	Added type	number 74AUP1G86GX (SO	Γ1226)	
	<ul> <li>Package out</li> </ul>	line drawing of SOT886 (Figu	<u>ire 11</u> ) modified.	
74AUP1G86 v.4	20111129	Product data sheet	-	74AUP1G86 v.3
Modifications:	<ul> <li>Legal pages</li> </ul>	updated.		
74AUP1G86 v.3	20101005	Product data sheet	-	74AUP1G86 v.2
74AUP1G86 v.2	20060628	Product data sheet	-	74AUP1G86 v.1
74AUP1G86 v.1	20050805	Product data sheet	-	-

#### Low-power 2-input EXCLUSIVE-OR gate

### 16. Legal information

#### 16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

#### 16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

#### 16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <a href="http://www.nxp.com/profile/terms">http://www.nxp.com/profile/terms</a>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

74AUP1G86

All information provided in this document is subject to legal disclaimers.

### Low-power 2-input EXCLUSIVE-OR gate

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

#### 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

### 17. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

### Low-power 2-input EXCLUSIVE-OR gate

### 18. Contents

1	General description
2	Features and benefits
3	Ordering information 2
4	Marking 2
5	Functional diagram 2
6	Pinning information 3
6.1	Pinning
6.2	Pin description 4
7	Functional description 4
8	Limiting values 4
9	Recommended operating conditions 5
10	Static characteristics 5
11	Dynamic characteristics 8
12	Waveforms
13	Package outline
14	Abbreviations
15	Revision history 18
16	Legal information
16.1	Data sheet status
16.2	Definitions
16.3	Disclaimers
16.4	Trademarks20
17	Contact information 20
18	Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

# **X-ON Electronics**

Largest Supplier of Electrical and Electronic Components

Click to view similar products for nxp manufacturer:

Other Similar products are found below:

MC13211R2 PCA9518PW,112 LFSTBEB865X MC33399PEFR2 PCA9551PW,112 MC34825EPR2 CBTW28DD14AETJ PCF8583P MC68340AB16E MC8640DTVJ1250HE EVBCRTOUCH MC9S08PT16AVLC MC9S08PT8AVTG MC9S08SH32CTL MCF54415CMJ250 MCIMX6Q-SDB MCIMX6SX-SDB 74ALVC125BQ,115 74HC4050N 74HC4514N MK21FN1M0AVLQ12 MKV30F128VFM10 FRDM-K66F FRDM-KW40Z FRDM-MC-LVBLDC PESD18VF1BSFYL PMF63UNEX PSMN4R0-60YS,115 HEF4028BPN RAPPID-567XFSW MPC565MVR56 MPC574XG-176DS MPC8548VJAUJD MPC860PCVR66D4 BT137-600E BT137S-600D.115 BT138-600E.127 BT139X-600.127 BT258-600R.127 BUK7628-100A118 BUK765R0-100E.118 P5020NSE7VNB S12ZVML12EVBLIN SCC2692AC1N40 LPC1785FBD208K LPC2124FBD64/01 LS1020ASN7KQB LS1020AXN7HNB LS1020AXN7KQB LS1043ASE7PQA