74HC05

Hex inverter with open-drain outputs

Rev. 3 — 8 July 2020

Product data sheet

1. General description

The 74HC05 contains six inverters. The outputs of the 74HC05 are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. The open-drain outputs require pull-up resistors to perform correctly.

2. Features and benefits

- Wide operating voltage 2.0 V to 6.0 V
- CMOS input levels
- · Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- · Complies with JEDEC standard no. 7A
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

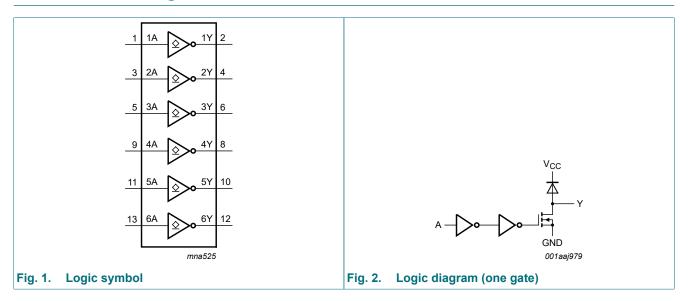
Table 1. Ordering information

Type number	Package									
	Temperature range	Name	Description	Version						
74HC05D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1						
74HC05PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1						
74HC05BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1						



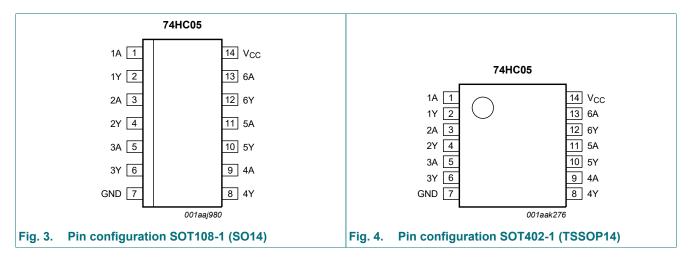
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4. Functional diagram

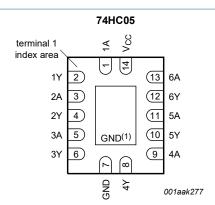


5. Pinning information

5.1. Pinning



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Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	data input
1Y to 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Output
nA	nY
L	Z
Н	L

Product data sheet

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Vo	output voltage	[1]	-0.5	V _{CC} + 0.5 V	V
Io	output current	V _O < V _{CC} + 0.5 V	-	25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	ns/V
		V _{CC} = 4.5 V	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	ns/V

^[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C. For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IL}$; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.5	-	±5.0	-	±10	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μA
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit see Fig. 7.

Symbol	Parameter	Conditions		25 °C		-40 °C to	Unit	
			Min	Тур	Max	Max (85 °C)	Max (125 °C)	
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 6						
		V _{CC} = 2.0 V	-	20	90	115	135	ns
		V _{CC} = 4.5 V	-	11	18	23	27	ns
		V _{CC} = 6.0 V	-	10	15	20	23	ns
t _{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 6						
		V _{CC} = 2.0 V	-	22	90	115	135	ns
		V _{CC} = 4.5 V	-	9	18	23	27	ns
		V _{CC} = 6.0 V	-	8	15	20	23	ns
t _{THL}	HIGH to LOW	see Fig. 6						
	output transition time	V _{CC} = 2.0 V	-	18	75	95	110	ns
	ume	V _{CC} = 4.5 V	-	6	15	19	22	ns
		V _{CC} = 6.0 V	-	5	13	16	19	ns
C _{PD}	power dissipation capacitance	per inverter; V_I = GND to V_{CC} ; [1] V_{CC} = 5.0 V	-	4	-	-	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (0.5 \times C_L \times V_O^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

V_O = output voltage in V (output HIGH);

V_{CC} = supply voltage in V;

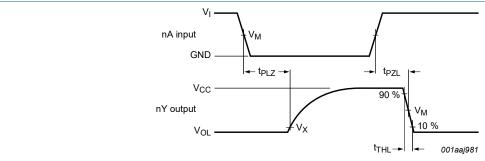
N = number of inputs switching;

 R_L = load resistance in $M\Omega$;

C_L = load capacitance in pF;

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10.1. Waveforms and test circuit



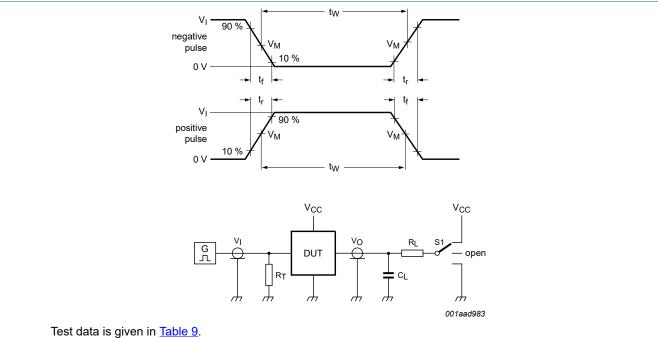
Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. The input nA to output nY propagation delays and output transition times

Table 8. Measurement points

Input	Output					
V_{M}	V _M	V _X				
0.5V _{CC}	0.5V _{CC}	0.1V _{CC}				



Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

R_L = Load resistance.

Test circuit for measuring switching times Fig. 7.

Table 9. Test data

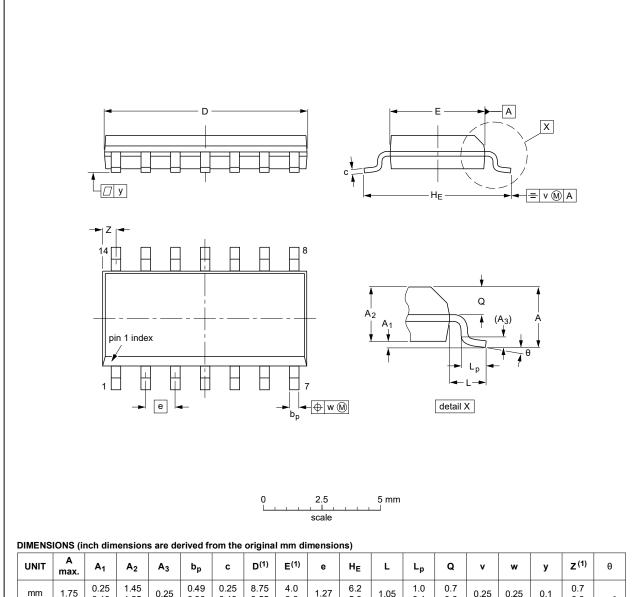
Input		Load	S1 position	
V_{l} t_{r}, t_{f}		CL	R _L	t _{PZL} , t _{PLZ}
V _{CC}	6 ns	50 pF	1 kΩ	V _{CC}

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11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

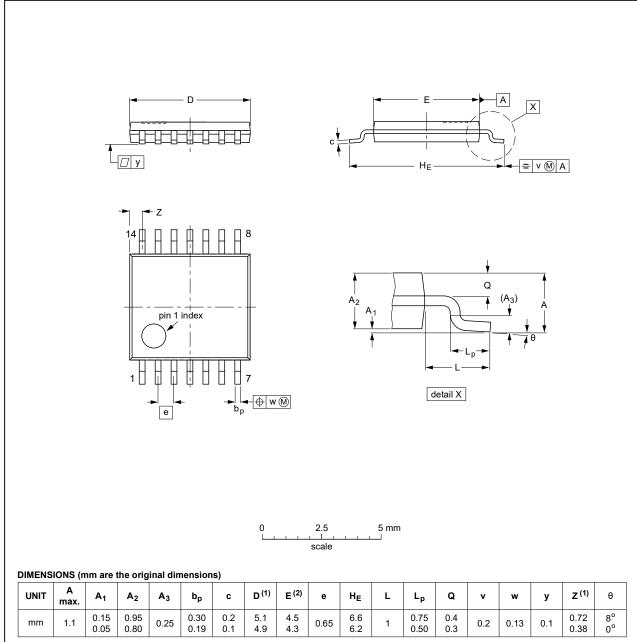
OUTLINE VERSION	OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
	IEC	JEDEC	JEITA		PROJECTION		
	SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig. 8. Package outline SOT108-1 (SO14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				99-12-27 03-02-18

Fig. 9. Package outline SOT402-1 (TSSOP14)

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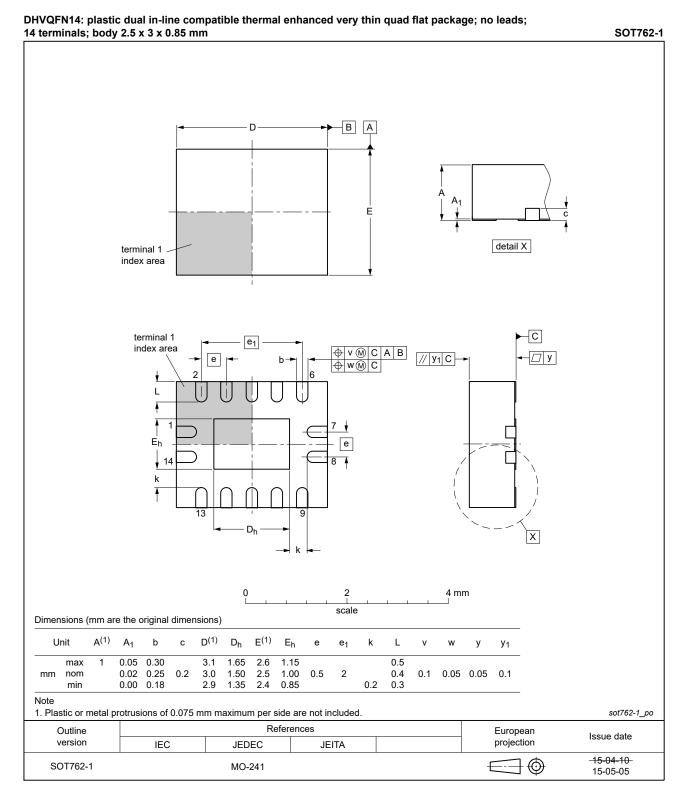


Fig. 10. Package outline SOT762-1 (DHVQFN14)

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12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC05 v.3	20200708	Product data sheet	-	74HC05 v.2	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 4: Derating values for Ptot total power dissipation have been updated. Table 6: Conditions for IOZ corrected. Package outline drawing of SOT762-1 (Fig. 10) updated. 				
74HC05 v.2	20090618	Product data sheet	-	74HC05 v.1	
Modifications:	Added type numbers 74HC05PW (TSSOP14 package) and 74HC05BQ (DHVQFN14 package)				
74HC05 v.1	20090427	Product data sheet	-	-	

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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