

74HC4052; 74HCT4052

Dual 4-channel analog multiplexer/demultiplexer

Rev. 12 — 10 October 2017

Product data sheet

1 General description

The 74HC4052; 74HCT4052 is a dual single-pole quad-throw analog switch (2x SP4T) suitable for use in analog or digital 4:1 multiplexer/demultiplexer applications. Each switch features four independent inputs/outputs (nY0, nY1, nY2 and nY3) and a common input/output (nZ). A digital enable input (\bar{E}) and two digital select inputs (S0 and S1) are common to both switches. When \bar{E} is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2 Features and benefits

- Wide analog input voltage range from -5 V to +5 V
- Low ON resistance:
 - 80 Ω (typical) at $V_{CC} - V_{EE} = 4.5$ V
 - 70 Ω (typical) at $V_{CC} - V_{EE} = 6.0$ V
 - 60 Ω (typical) at $V_{CC} - V_{EE} = 9.0$ V
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical 'break before make' built-in
- Complies with JEDEC standard no. 7A
- Input levels:
 - For 74HC4052: CMOS level
 - For 74HCT4052: TTL level
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3 Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4052D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4052D				
74HC4052DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4052DB				
74HC4052PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4052PW				
74HC4052BQ	-40 °C to +125 °C	DHVQFN16	plastic dual-in line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm	SOT763-1
74HCT4052BQ				

5 Functional diagram

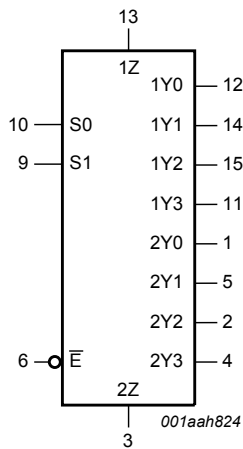


Figure 1. Logic symbol

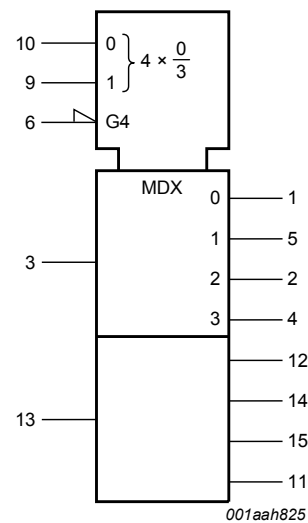


Figure 2. IEC logic symbol

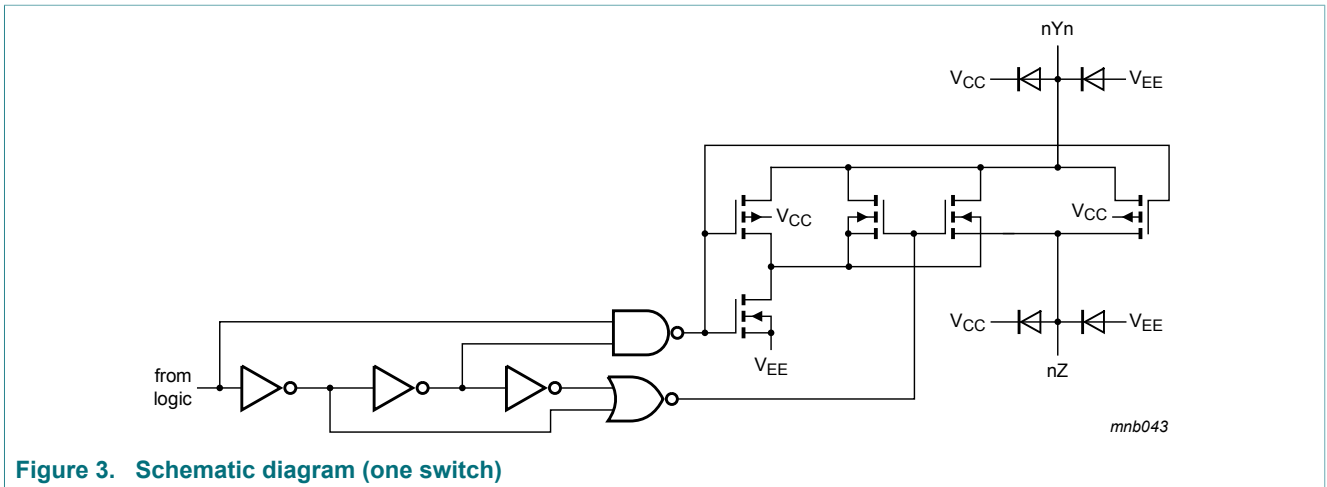


Figure 3. Schematic diagram (one switch)

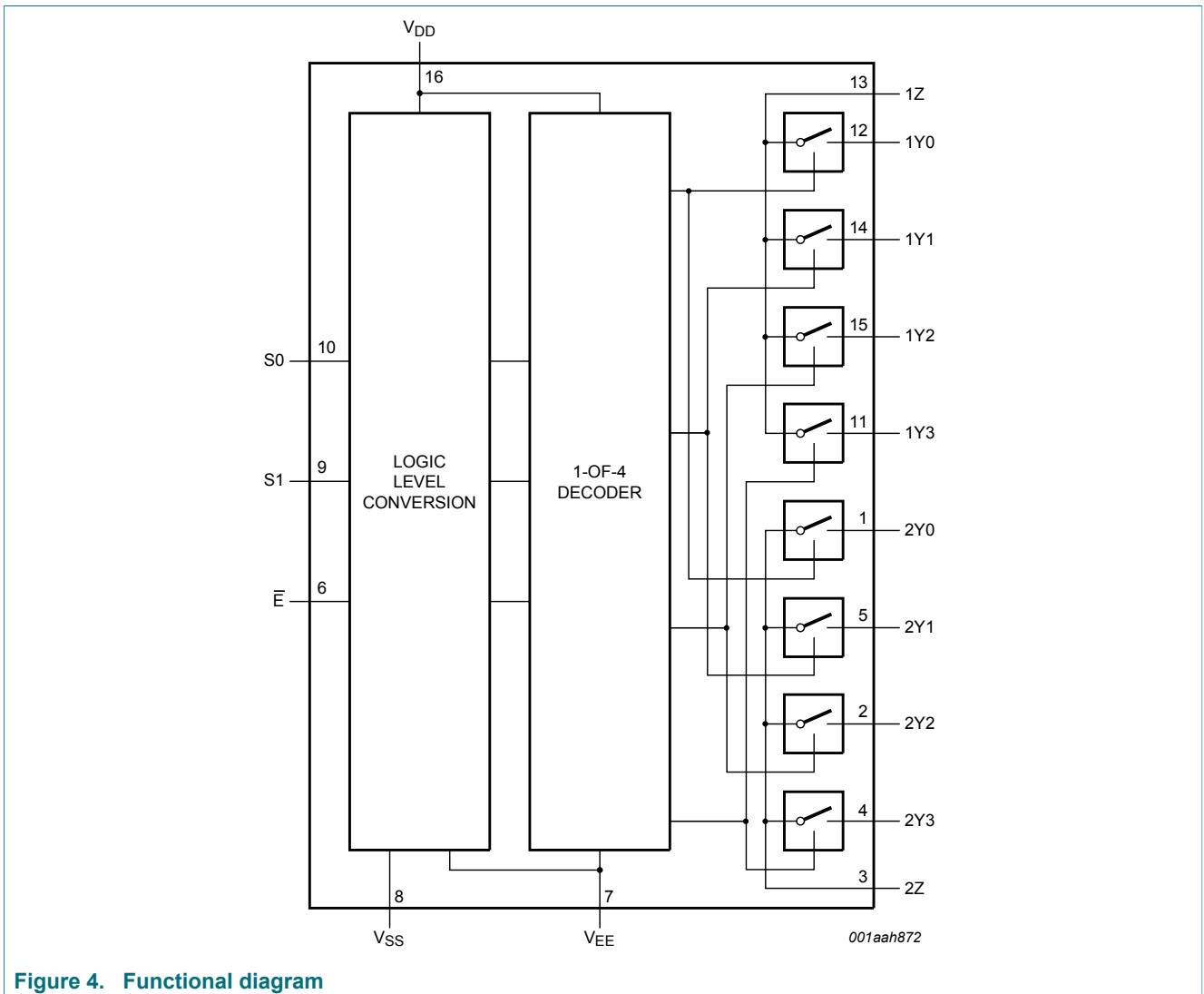


Figure 4. Functional diagram

6 Pinning information

6.1 Pinning

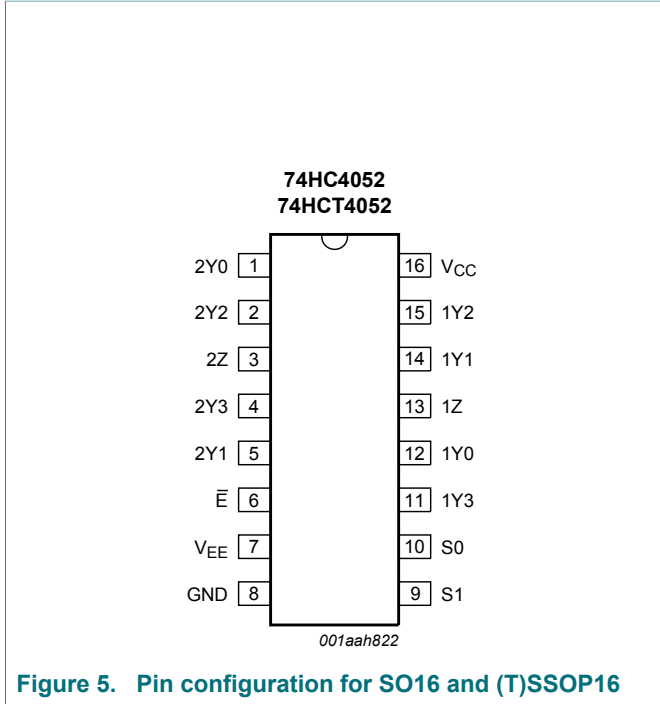
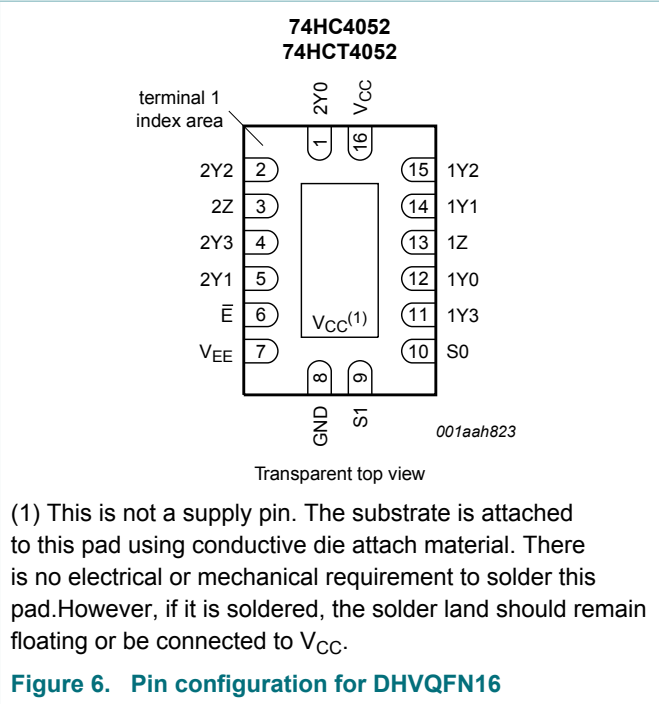


Figure 5. Pin configuration for SO16 and (T)SSOP16



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to V_{CC}.

Figure 6. Pin configuration for DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0, 2Y1, 2Y2, 2Y3	1, 5, 2, 4	independent input or output
1Z, 2Z	13, 3	common input or output
\bar{E}	6	enable input (active LOW)
V _{EE}	7	negative supply voltage
GND	8	ground (0 V)
S0, S1	10, 9	select logic input
1Y0, 1Y1, 1Y2, 1Y3	12, 14, 15, 11	independent input or output
V _{CC}	16	positive supply voltage

7 Functional description

Table 3. Function table ^[1]

Input			Channel on
\bar{E}	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Voltages are referenced to $V_{EE} = GND$ (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+11.0	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	±20	mA
I_{SK}	switch clamping current	$V_{SW} < -0.5 \text{ V}$ or $V_{SW} > V_{CC} + 0.5 \text{ V}$	-	±20	mA
I_{SW}	switch current	$-0.5 \text{ V} < V_{SW} < V_{CC} + 0.5 \text{ V}$	-	±25	mA
I_{EE}	supply current		-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-	-50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SO16, SSOP16, TSSOP16 and DHVQFN16 package	-	500	mW
P	power dissipation	per switch	-	100	mW

[1] To avoid drawing V_{CC} current out of pins nZ, when switch current flows in pins nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pins nZ, no V_{CC} current will flow out of pins nYn. In this case there is no limit for the voltage drop across the switch, but the voltages at pins nYn and nZ may not exceed V_{CC} or V_{EE} .

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For SSOP16 and TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

9 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4052			74HCT4052			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage	see Figure 7 and Figure 8							
		$V_{CC} - GND$	2.0	5.0	10.0	4.5	5.0	5.5	V
		$V_{CC} - V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V
V_I	input voltage		GND	-	V_{CC}	GND	-	V_{CC}	V
V_{SW}	switch voltage		V_{EE}	-	V_{CC}	V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V
		$V_{CC} = 10.0\text{ V}$	-	-	31	-	-	-	ns/V

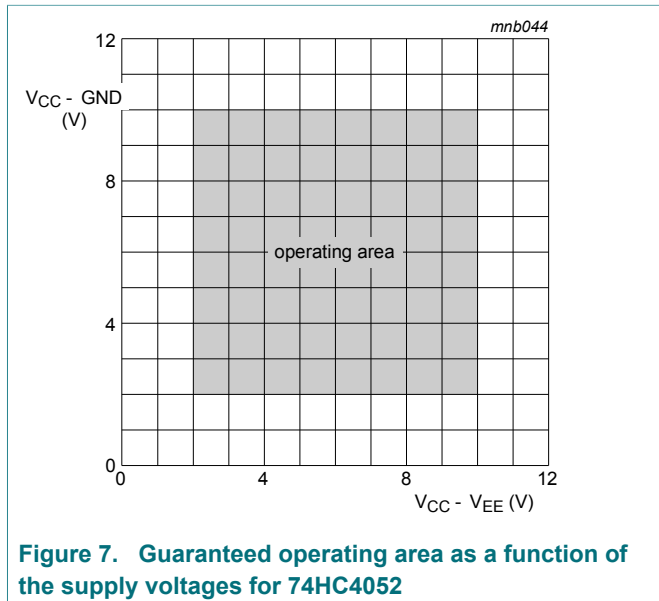


Figure 7. Guaranteed operating area as a function of the supply voltages for 74HC4052

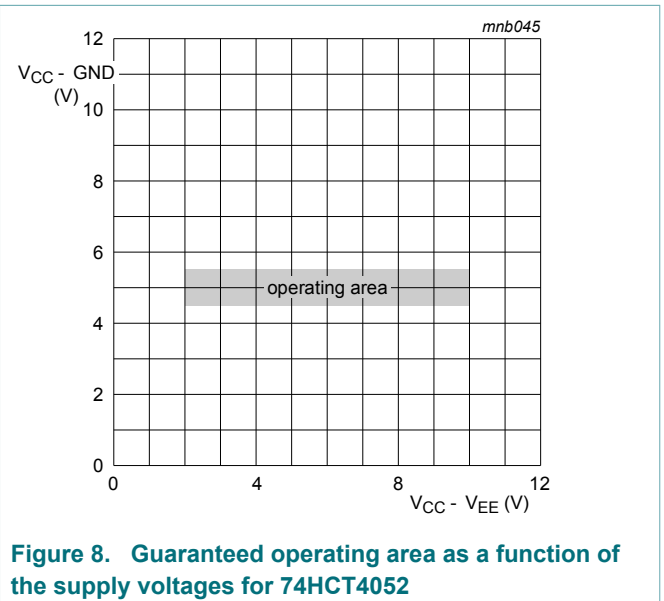


Figure 8. Guaranteed operating area as a function of the supply voltages for 74HCT4052

10 Static characteristics

Table 6. R_{ON} resistance per switch for 74HC4052 and 74HCT4052

V_I = V_{IH} or V_{IL}; for test circuit see Figure 9.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

For 74HC4052: V_{CC} - GND or V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

For 74HCT4052: V_{CC} - GND = 4.5 V and 5.5 V, V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit	
T_{amb} = -40 °C to +85 °C							
R _{ON(peak)}	ON resistance (peak)	V _{is} = V _{CC} to V _{EE}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA ^[2]	-	-	-	Ω	
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	100	225	Ω	
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	90	200	Ω	
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA	-	70	165	Ω	
R _{ON(rail)}	ON resistance (rail)	V _{is} = V _{EE}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA ^[2]	-	150	-	Ω	
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	80	175	Ω	
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	70	150	Ω	
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA	-	60	130	Ω	
		V _{is} = V _{CC}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA ^[2]	-	150	-	Ω	
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	90	200	Ω	
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	80	175	Ω	
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA	-	65	150	Ω	
ΔR _{ON}	ON resistance mismatch between channels	V _{is} = V _{CC} to V _{EE}					
		V _{CC} = 2.0 V; V _{EE} = 0 V ^[2]	-	-	-	Ω	
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	9	-	Ω	
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	8	-	Ω	
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	6	-	Ω	

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit	
T_{amb} = -40 °C to +125 °C							
R _{ON(peak)}	ON resistance (peak)	V _{is} = V _{CC} to V _{EE}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA [2]	-	-	-	Ω	
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	-	270	Ω	
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	-	240	Ω	
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA	-	-	195	Ω	
R _{ON(rail)}	ON resistance (rail)	V _{is} = V _{EE}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA [2]	-	-	-	Ω	
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	-	210	Ω	
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	-	180	Ω	
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA	-	-	160	Ω	
		V _{is} = V _{CC}					
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 μA [2]	-	-	-	Ω	
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	-	240	Ω	
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 μA	-	-	210	Ω	
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 μA	-	-	180	Ω	

[1] All typical values are measured at T_{amb} = 25 °C.

[2] When supply voltages (V_{CC} - V_{EE}) near 2.0 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.

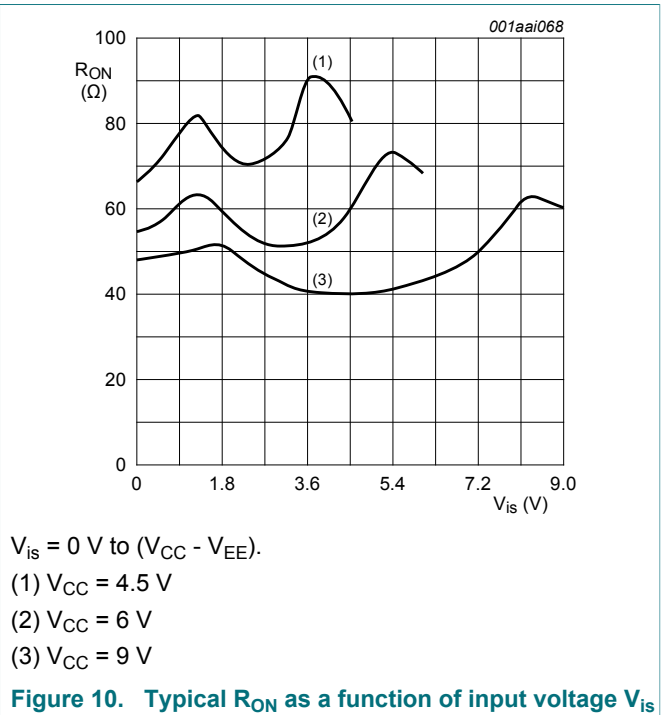
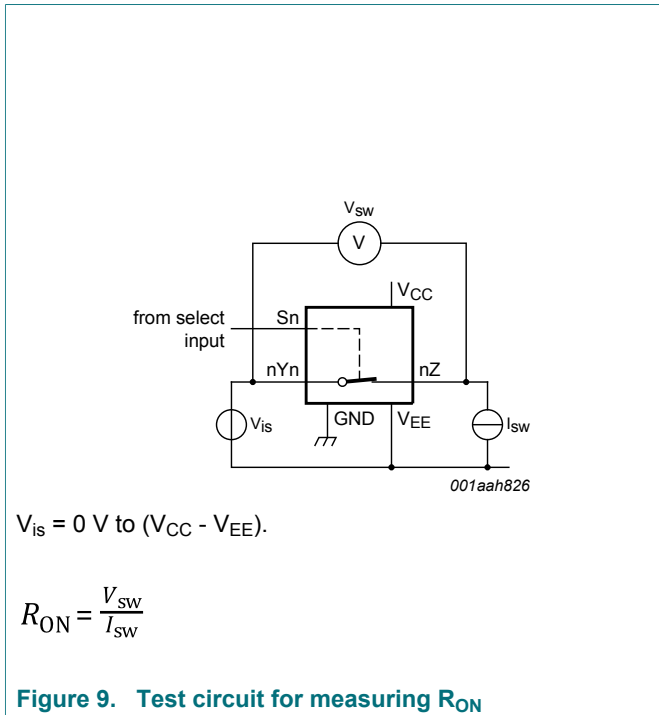


Table 7. Static characteristics for 74HC4052

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V
		V _{CC} = 9.0 V	6.3	4.7	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
		V _{CC} = 9.0 V	-	4.3	2.7	V
I _I	input leakage current	V _{EE} = 0 V; V _I = V _{CC} or GND				
		V _{CC} = 6.0 V	-	-	±1.0	μA
		V _{CC} = 10.0 V	-	-	±2.0	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Figure 11				
		per channel	-	-	±1.0	μA
		all channels	-	-	±2.0	μA
I _{S(ON)}	ON-state leakage current	V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; V _{CC} = 10.0 V; V _{EE} = 0 V; see Figure 12	-	-	±2.0	μA
I _{CC}	supply current	V _{EE} = 0 V; V _I = V _{CC} or GND; V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}				
		V _{CC} = 6.0 V	-	-	80.0	μA
		V _{CC} = 10.0 V	-	-	160.0	μA
C _I	input capacitance		-	3.5	-	pF
C _{sw}	switch capacitance	independent pins nYn	-	5	-	pF
		common pins nZ	-	12	-	pF

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
		V _{CC} = 9.0 V	6.3	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
		V _{CC} = 9.0 V	-	-	2.7	V
I _I	input leakage current	V _{EE} = 0 V; V _I = V _{CC} or GND				
		V _{CC} = 6.0 V	-	-	±1.0	µA
		V _{CC} = 10.0 V	-	-	±2.0	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Figure 11				
		per channel	-	-	±1.0	µA
		all channels	-	-	±2.0	µA
I _{S(ON)}	ON-state leakage current	V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; V _{CC} = 10.0 V; V _{EE} = 0 V; see Figure 12	-	-	±2.0	µA
I _{CC}	supply current	V _{EE} = 0 V; V _I = V _{CC} or GND; V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}				
		V _{CC} = 6.0 V	-	-	160.0	µA
		V _{CC} = 10.0 V	-	-	320.0	µA

[1] All typical values are measured at T_{amb} = 25 °C.

Table 8. Static characteristics for 74HCT4052

Voltages are referenced to GND (ground = 0 V).

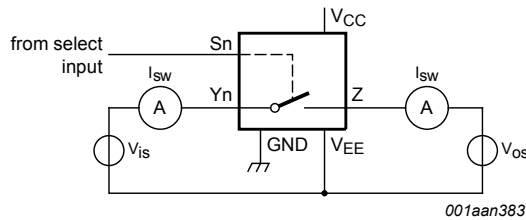
V_{is} is the input voltage at pins nYn or nZ, whichever is assigned as an input.

V_{os} is the output voltage at pins nZ or nYn, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	±1.0	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Figure 11				
		per channel	-	-	±1.0	µA
		all channels	-	-	±2.0	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Figure 12	-	-	±2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}				
		V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	80.0	µA
		V _{CC} = 5.0 V; V _{EE} = -5.0 V	-	-	160.0	µA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; V _{EE} = 0 V	-	45	202.5	µA
C _I	input capacitance		-	3.5	-	pF
C _{SW}	switch capacitance	independent pins nYn	-	5	-	pF
		common pins nZ	-	12	-	pF

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	±1.0	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Figure 11				
		per channel	-	-	±1.0	µA
		all channels	-	-	±2.0	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Figure 12	-	-	±2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}				
		V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	160.0	µA
		V _{CC} = 5.0 V; V _{EE} = -5.0 V	-	-	320.0	µA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; V _{EE} = 0 V	-	-	220.5	µA

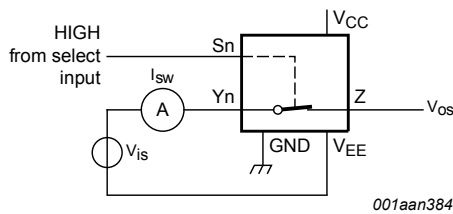
[1] All typical values are measured at T_{amb} = 25 °C.



V_{is} = V_{CC} and V_{os} = V_{EE}.

V_{is} = V_{EE} and V_{os} = V_{CC}.

Figure 11. Test circuit for measuring OFF-state current



V_{is} = V_{CC} and V_{os} = open-circuit.

V_{is} = V_{EE} and V_{os} = open-circuit.

Figure 12. Test circuit for measuring ON-state current

11 Dynamic characteristics

Table 9. Dynamic characteristics for 74HC4052

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see [Figure 15](#).

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
t_{pd}	propagation delay	V_{is} to V_{os} ; $R_L = \infty\ \Omega$; see Figure 13 ^[2]				
		$V_{CC} = 2.0\text{ V}$; $V_{EE} = 0\text{ V}$	-	14	75	ns
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	5	15	ns
		$V_{CC} = 6.0\text{ V}$; $V_{EE} = 0\text{ V}$	-	4	13	ns
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	4	10	ns
t_{on}	turn-on time	\bar{E} , Sn to V_{os} ; $R_L = \infty\ \Omega$; see Figure 14 ^[3]				
		$V_{CC} = 2.0\text{ V}$; $V_{EE} = 0\text{ V}$	-	105	405	ns
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	38	81	ns
		$V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$; $C_L = 15\text{ pF}$	-	28	-	ns
		$V_{CC} = 6.0\text{ V}$; $V_{EE} = 0\text{ V}$	-	30	69	ns
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	26	58	ns
t_{off}	turn-off time	\bar{E} , Sn to V_{os} ; $R_L = 1\text{ k}\Omega$; see Figure 14 ^[4]				
		$V_{CC} = 2.0\text{ V}$; $V_{EE} = 0\text{ V}$	-	74	315	ns
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	27	63	ns
		$V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$; $C_L = 15\text{ pF}$	-	21	-	ns
		$V_{CC} = 6.0\text{ V}$; $V_{EE} = 0\text{ V}$	-	22	54	ns
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	22	48	ns
C_{PD}	power dissipation capacitance	per switch; $V_I = GND$ to V_{CC} ^[5]	-	57	-	pF

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
t _{pd}	propagation delay	V _{is} to V _{os} ; R _L = ∞ Ω; see Figure 13 ^[2]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	90	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	18	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	15	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	12	ns
t _{on}	turn-on time	\bar{E} , Sn to V _{os} ; R _L = ∞ Ω; see Figure 14 ^[3]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	490	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	98	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	83	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	69	ns
t _{off}	turn-off time	\bar{E} , Sn to V _{os} ; R _L = 1 kΩ; see Figure 14 ^[4]				
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	-	375	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	75	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	64	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	57	ns

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{on} is the same as t_{PZH} and t_{PZL}.

[4] t_{off} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

N = number of inputs switching;

Σ{(C_L + C_{sw}) × V_{CC}² × f_o} = sum of outputs;

C_L = output load capacitance in pF;

C_{sw} = switch capacitance in pF;

V_{CC} = supply voltage in V.

Table 10. Dynamic characteristics for 74HCT4052

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see [Figure 15](#).

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
t _{pd}	propagation delay	V _{is} to V _{os} ; R _L = ∞ Ω; see Figure 13 ^[2]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	5	15	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	4	10	ns
t _{on}	turn-on time	\bar{E} , Sn to V _{os} ; R _L = 1 kΩ; see Figure 14 ^[3]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	41	88	ns
		V _{CC} = 5.0 V; V _{EE} = 0 V; C _L = 15 pF	-	18	-	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	28	60	ns
t _{off}	turn-off time	\bar{E} , Sn to V _{os} ; R _L = 1 kΩ; see Figure 14 ^[4]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	26	63	ns
		V _{CC} = 5.0 V; V _{EE} = 0 V; C _L = 15 pF	-	13	-	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	21	48	ns
C _{PD}	power dissipation capacitance	per switch; V _I = GND to V _{CC} - 1.5 V ^[5]	-	57	-	pF
T_{amb} = -40 °C to +125 °C						
t _{pd}	propagation delay	V _{is} to V _{os} ; R _L = ∞ Ω; see Figure 13 ^[2]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	18	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	12	ns
t _{on}	turn-on time	\bar{E} , Sn to V _{os} ; R _L = 1 kΩ; see Figure 14 ^[3]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	105	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	72	ns
t _{off}	turn-off time	\bar{E} , Sn to V _{os} ; R _L = 1 kΩ; see Figure 14 ^[4]				
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	75	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	57	ns

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{on} is the same as t_{PZH} and t_{PZL}.

[4] t_{off} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

N = number of inputs switching;

∑{(C_L + C_{sw}) × V_{CC}² × f_o} = sum of outputs;

C_L = output load capacitance in pF;

C_{sw} = switch capacitance in pF;

V_{CC} = supply voltage in V.

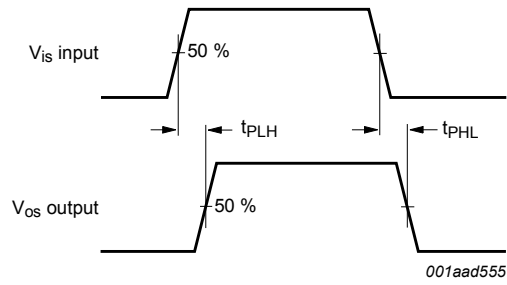
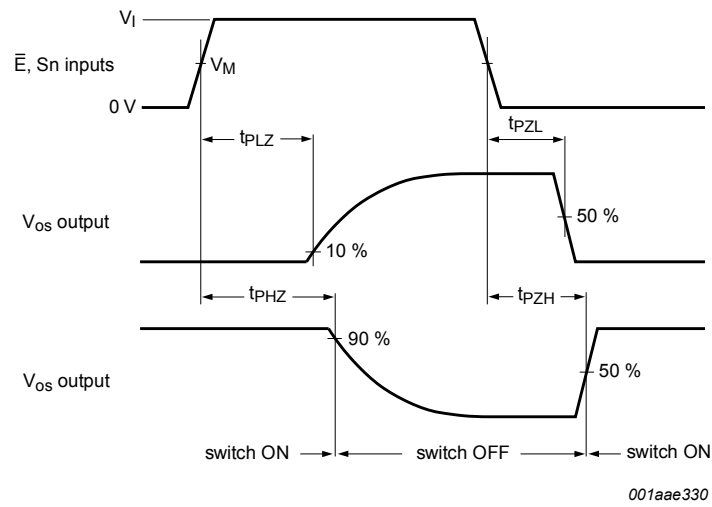


Figure 13. Input (V_{is}) to output (V_{os}) propagation delays



For 74HC4052: $V_M = 0.5 \times V_{CC}$.

For 74HCT4052: $V_M = 1.3 \text{ V}$.

Figure 14. Turn-on and turn-off times

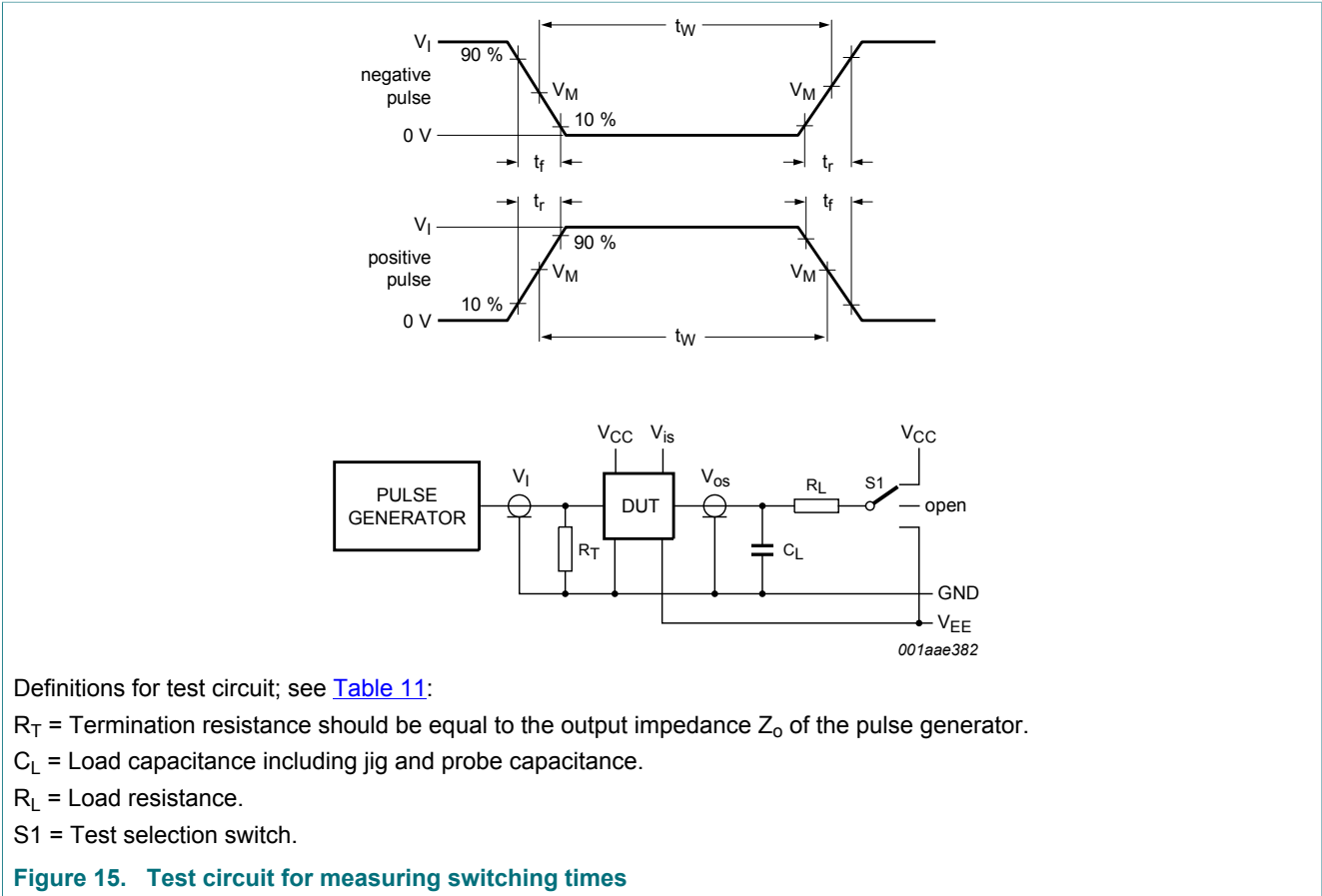


Table 11. Test data

Test	Input				Load		S1 position
	V_I	V_{is}	t_r, t_f		C_L	R_L	
			at f_{max}	other ^[1]			
t_{PHL}, t_{PLH}	[2]	pulse	< 2 ns	6 ns	50 pF	1 k Ω	open
t_{PZH}, t_{PHZ}	[2]	V_{CC}	< 2 ns	6 ns	50 pF	1 k Ω	V_{EE}
t_{PZL}, t_{PLZ}	[2]	V_{EE}	< 2 ns	6 ns	50 pF	1 k Ω	V_{CC}

[1] $t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint to t_r and t_f with 50 % duty factor.

[2] V_I values:

For 74HC4052: $V_I = V_{CC}$

For 74HCT4052: $V_I = 3$ V

12 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

Recommended conditions and typical values; $GND = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$.

V_{is} is the input voltage at pins nYn or nZ , whichever is assigned as an input.

V_{os} is the output voltage at pins nYn or nZ , whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
d_{sin}	sine-wave distortion	$f_i = 1\text{ kHz}$; $R_L = 10\text{ k}\Omega$; see Figure 16				
		$V_{is} = 4.0\text{ V (p-p)}$; $V_{CC} = 2.25\text{ V}$; $V_{EE} = -2.25\text{ V}$	-	0.04	-	%
		$V_{is} = 8.0\text{ V (p-p)}$; $V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	0.02	-	%
		$f_i = 10\text{ kHz}$; $R_L = 10\text{ k}\Omega$; see Figure 16				
		$V_{is} = 4.0\text{ V (p-p)}$; $V_{CC} = 2.25\text{ V}$; $V_{EE} = -2.25\text{ V}$	-	0.12	-	%
		$V_{is} = 8.0\text{ V (p-p)}$; $V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	0.06	-	%
α_{iso}	isolation (OFF-state)	$R_L = 600\ \Omega$; $f_i = 1\text{ MHz}$; see Figure 17				
		$V_{CC} = 2.25\text{ V}$; $V_{EE} = -2.25\text{ V}$ [1]	-	-50	-	dB
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$ [1]	-	-50	-	dB
Xtalk	crosstalk	between two switches/multiplexers; $R_L = 600\ \Omega$; $f_i = 1\text{ MHz}$; see Figure 18				
		$V_{CC} = 2.25\text{ V}$; $V_{EE} = -2.25\text{ V}$ [1]	-	-60	-	dB
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$ [1]	-	-60	-	dB
V_{ct}	crosstalk voltage	peak-to-peak value; between control and any switch; $R_L = 600\ \Omega$; $f_i = 1\text{ MHz}$; \bar{E} or S_n square wave between V_{CC} and GND ; $t_r = t_f = 6\text{ ns}$; see Figure 19				
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	110	-	mV
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	220	-	mV
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50\ \Omega$; see Figure 20				
		$V_{CC} = 2.25\text{ V}$; $V_{EE} = -2.25\text{ V}$ [2]	-	170	-	MHz
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$ [2]	-	180	-	MHz

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

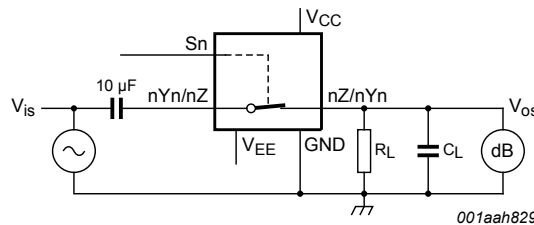
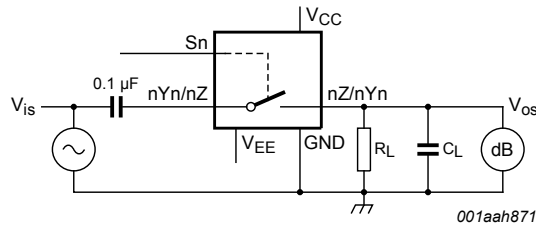
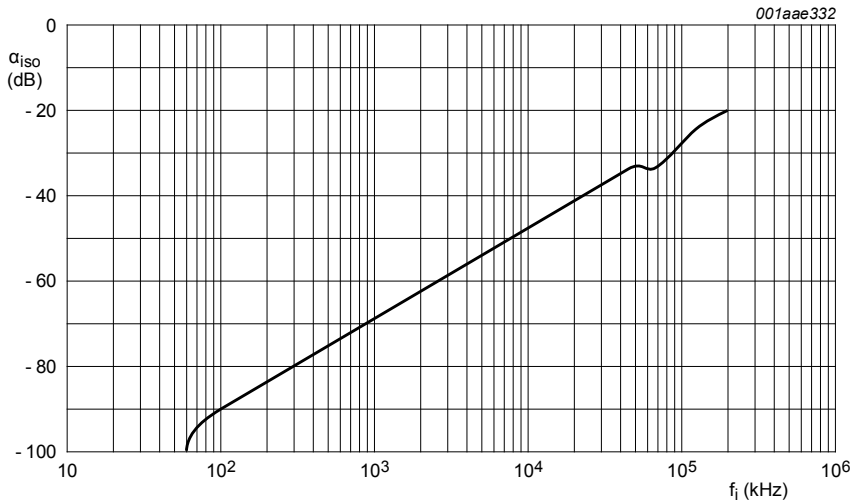


Figure 16. Test circuit for measuring sine-wave distortion



$V_{CC} = 4.5\text{ V}$; $GND = 0\text{ V}$; $V_{EE} = -4.5\text{ V}$; $R_L = 600\ \Omega$; $R_S = 1\text{ k}\Omega$.

a. Test circuit



b. Isolation (OFF-state) as a function of frequency

Figure 17. Test circuit for measuring isolation (OFF-state)

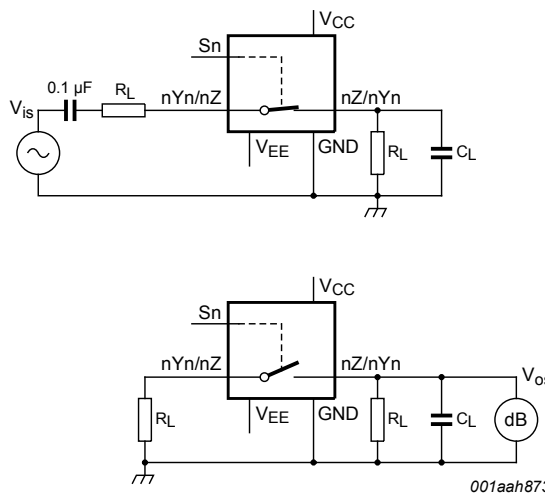


Figure 18. Test circuits for measuring crosstalk between any two switches/multiplexers

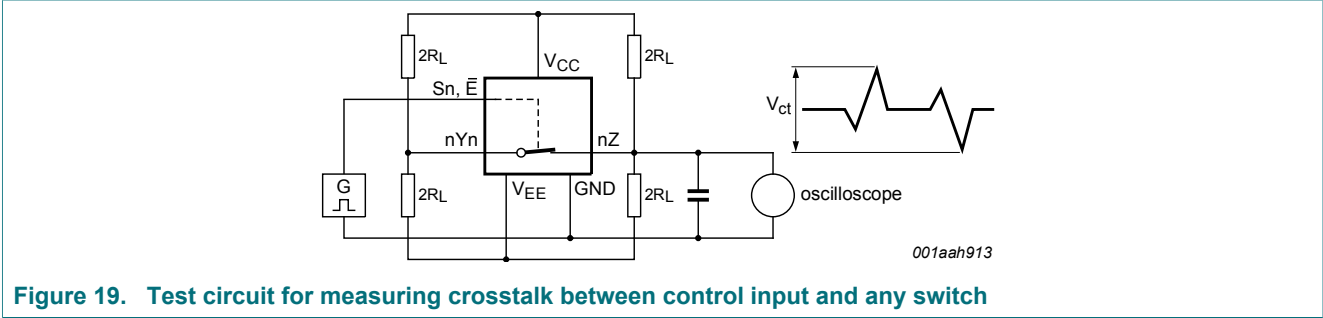


Figure 19. Test circuit for measuring crosstalk between control input and any switch

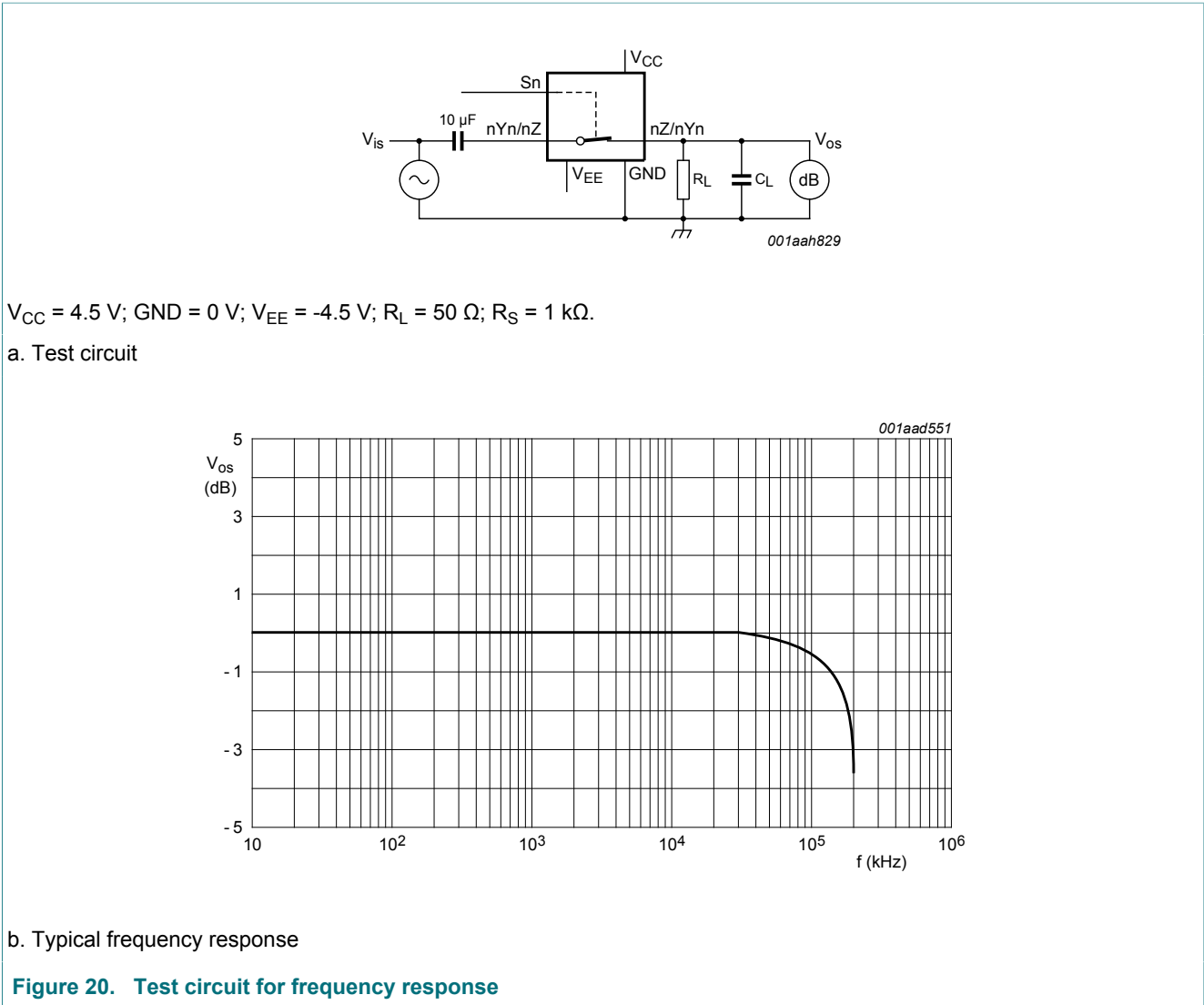
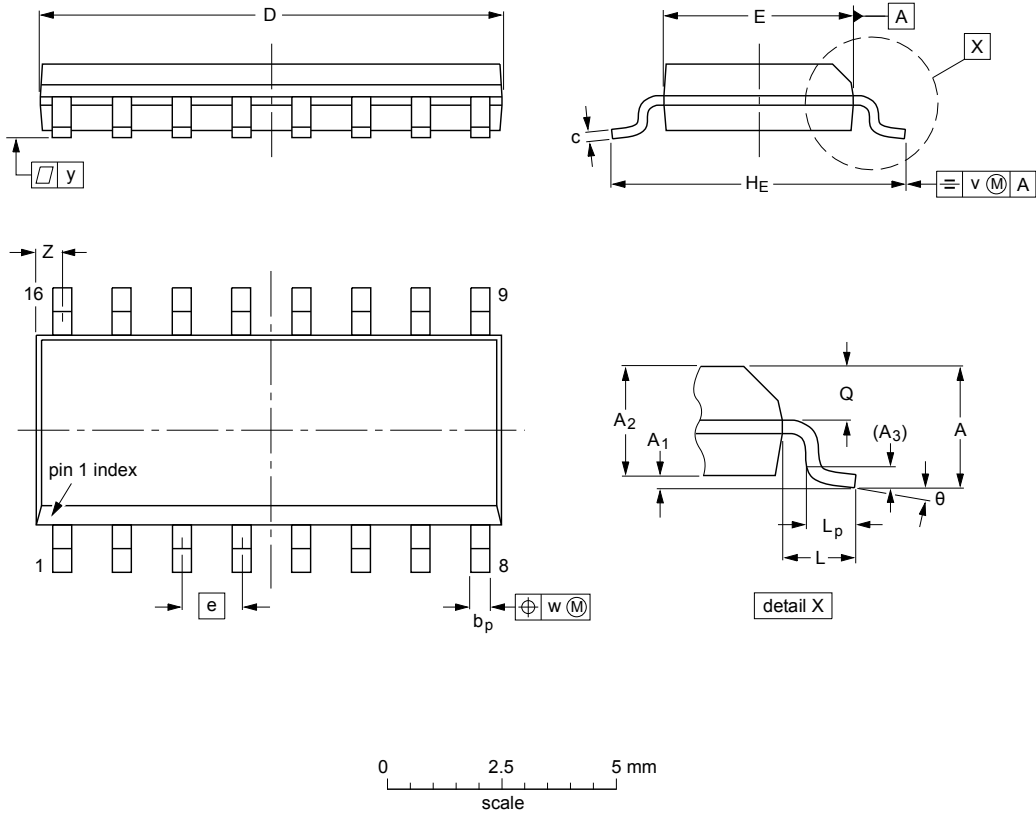


Figure 20. Test circuit for frequency response

13 Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

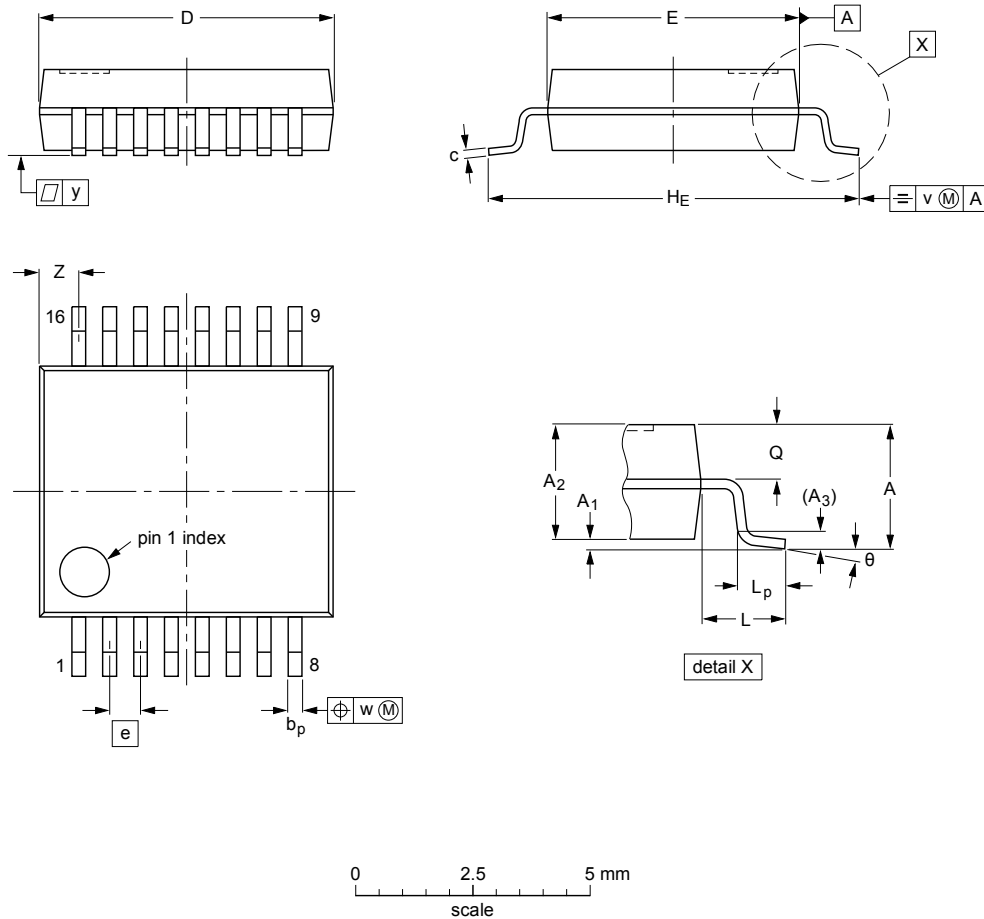
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT109-1	076E07	MS-012			99-12-27 03-02-19

Figure 21. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

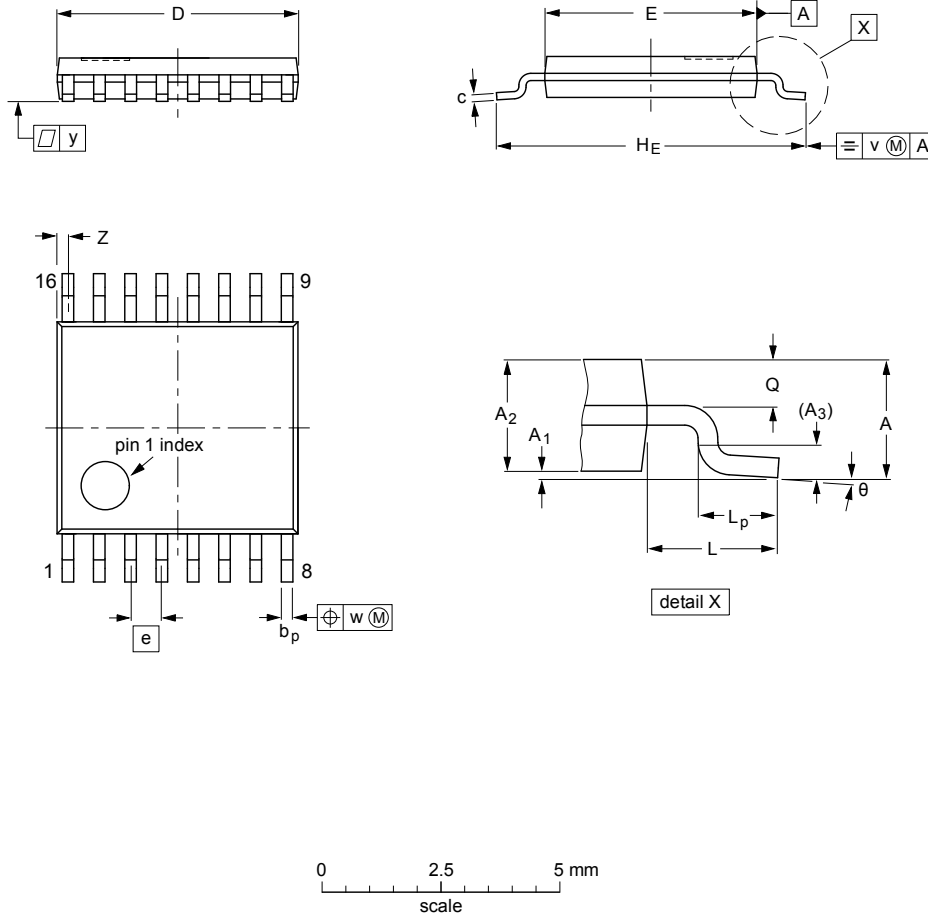
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				99-12-27 03-02-19

Figure 22. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18

Figure 23. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

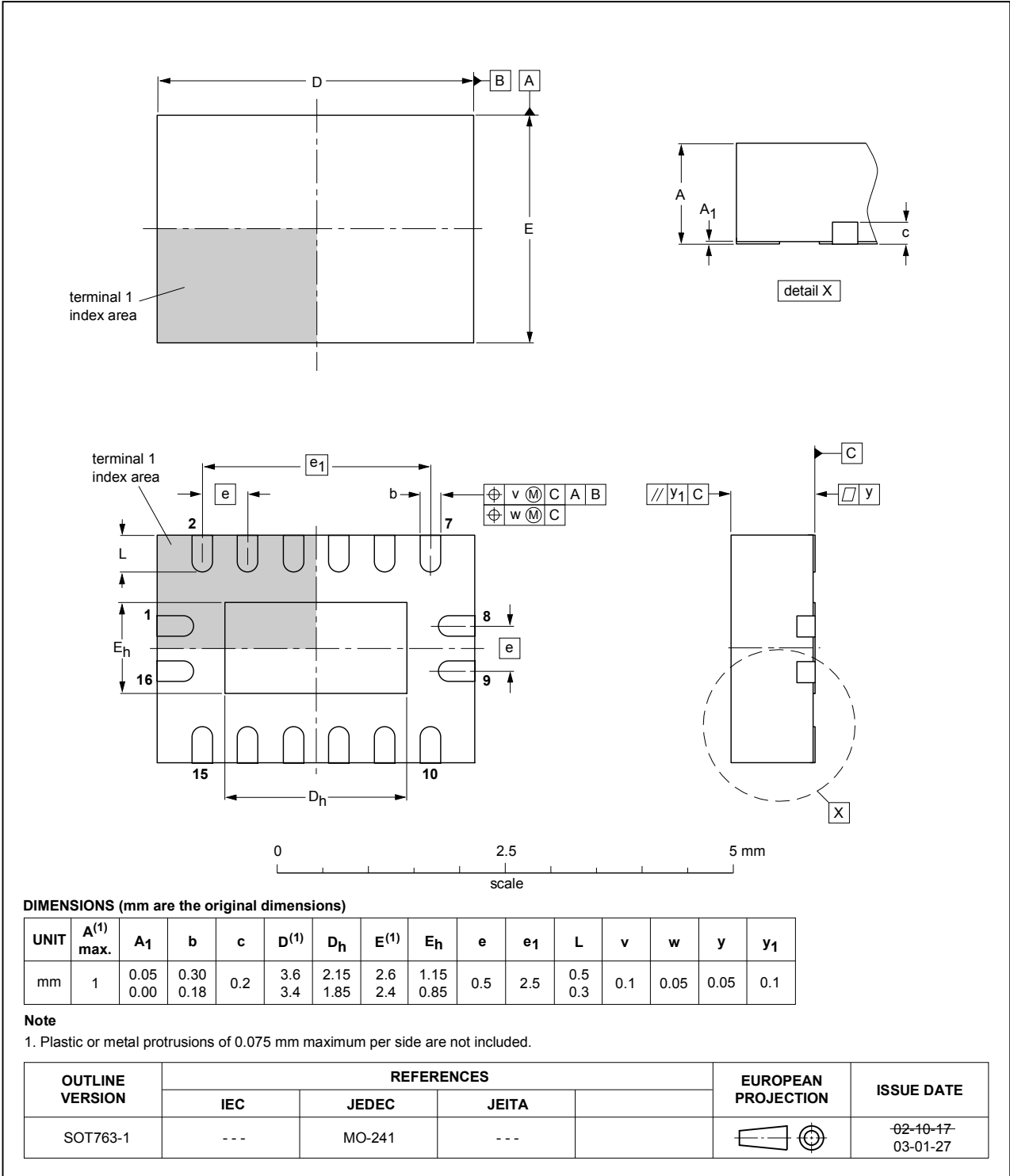


Figure 24. Package outline SOT763-1 (DHVQFN16)

14 Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15 Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4052 v.12	20171010	Product data sheet	-	74HC_HCT4052 v.11
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT4052 v.11	20160210	Product data sheet	-	74HC_HCT4052 v.10
Modifications:	<ul style="list-style-type: none"> Type numbers 74HC4052N and 74HCT4052N (SOT38-4) removed. 			
74HC_HCT4052 v.10	20120719	Product data sheet	-	74HC_HCT4052 v.9
Modifications:	<ul style="list-style-type: none"> CDM added to features. 			
74HC_HCT4052 v.9	20111213	Product data sheet	-	74HC_HCT4052 v.8
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74HC_HCT4052 v.8	20110511	Product data sheet	-	74HC_HCT4052 v.7
74HC_HCT4052 v.7	20110112	Product data sheet	-	74HC_HCT4052 v.6
74HC_HCT4052 v.6	20100111	Product data sheet	-	74HC_HCT4052 v.5
74HC_HCT4052 v.5	20080505	Product data sheet	-	74HC_HCT4052 v.4
74HC_HCT4052 v.4	20041111	Product specification	-	74HC_HCT4052 v.3
74HC_HCT4052 v.3	20030516	Product specification	-	74HC_HCT4052 v.2
74HC_HCT4052 v.2	19901201	-	-	-

16 Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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