74HC390; 74HCT390

Dual decade ripple counter

Rev. 5 — 18 October 2021 **Product data sheet**

1. General description

The 74HC390; 74HCT390 is a dual 4-bit decade ripple counter divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections share an asynchronous master reset input (nMR) and can be used in a BCD decade or bi-quinary configuration. If master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks (n$\overline{CP}$0 and n$\overline{CP}$1) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100. Each section is triggered by the HIGH-to-LOW transition of the clock inputs (n$\overline{CP}$0 and n$\overline{CP}$1). For BCD decade operation, the nQ0 output is connected to the n$\overline{CP}$1 input of the divide-by-5 section. For bi-quinary decade operation, the nQ3 output is connected to the n$\overline{CP}$0 input and nQ0 becomes the decade output. A HIGH on the nMR input overrides the clocks and sets the four outputs LOW. This device features reduced input threshold levels to allow interfacing to TTL logic levels. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC390: CMOS level
  - For 74HCT390: TTL level
- Two BCD decade or bi-quinary counters
- One device can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two master reset inputs to clear each decade counter individually
- Supply voltage range from 4.5 V to 5.5 V
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD7A (4.5 V to 5.5 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC390D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT390D				
74HC390PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT390PW				

nexperia

4. Functional diagram

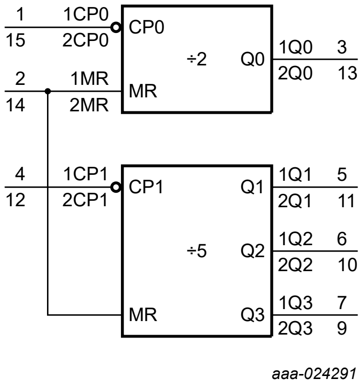


Fig. 1. Logic symbol

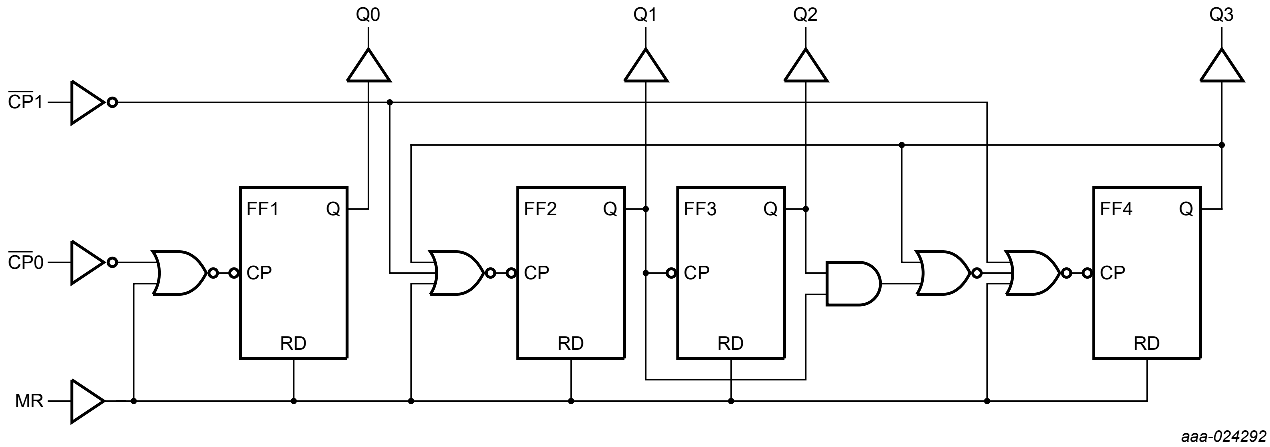


Fig. 2. Logic diagram (one counter)

5. Pinning information

5.1. Pinning

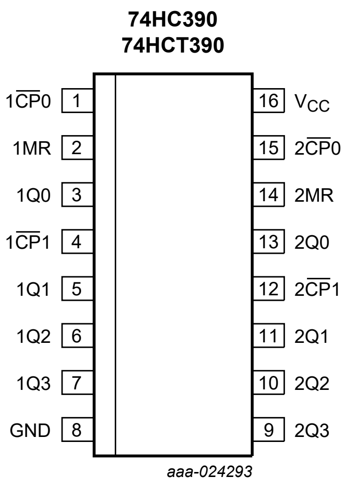


Fig. 3. Pin configuration for SOT109-1 (SO16)

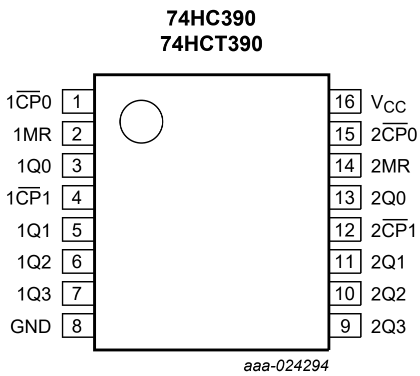


Fig. 4. Pin configuration for SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{CP}$0, 2$\overline{CP}$0	1, 15	clock input divide-by-2 section (HIGH-to-LOW; edge-triggered)
1MR, 2MR	2, 14	asynchronous master reset input (active HIGH)
1Q0, 1Q1, 1Q2, 1Q3	3, 5, 6, 7	flip-flop outputs
1$\overline{CP}$1, 2$\overline{CP}$1	4, 12	clock input divide-by-5 section (HIGH-to-LOW; edge-triggered)
GND	8	ground (0 V)
2Q0, 2Q1, 2Q2, 2Q3	13, 11, 10, 9	flip-flop outputs
V_{CC}	16	supply voltage

6. Functional description

Table 3. BCD count sequence

Output nQ0 connected to n$\overline{CP}$1; counter input on n$\overline{CP}$0;
H = HIGH voltage level; L = LOW voltage level

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Table 4. Bi-quinary count sequence

Output nQ3 connected to n$\overline{CP}$0; counter input on n$\overline{CP}$1;
H = HIGH voltage level; L = LOW voltage level

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC390			74HCT390			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC390										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT390										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		$n\overline{CP}0$ inputs	-	45	162	-	202.5	-	220.5	μA
		$n\overline{CP}1$, nMR inputs	-	60	216	-	270	-	294	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 7.

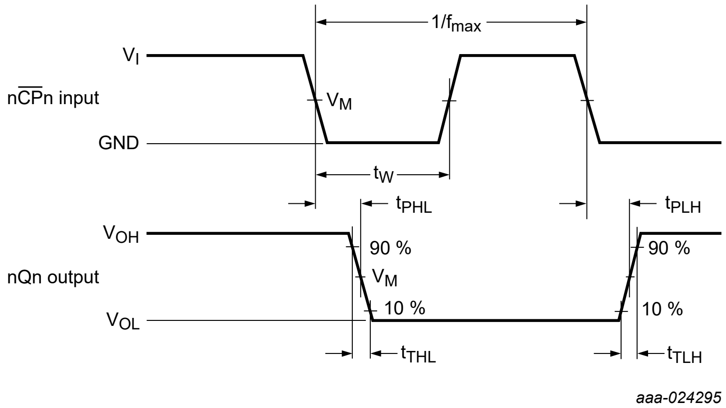
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74HC390										
t_{pd}	propagation delay	$n\overline{CP}0$ to nQ0; see Fig. 5 [2]								
		V_{CC} = 2.0 V	-	47	145	-	180	-	220	ns
		V_{CC} = 4.5 V	-	17	29	-	36	-	44	ns
		V_{CC} = 5 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	25	-	31	-	38	ns
		$n\overline{CP}1$ to nQ1; see Fig. 5								
		V_{CC} = 2.0 V	-	50	155	-	195	-	235	ns
		V_{CC} = 4.5 V	-	18	31	-	39	-	47	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	26	-	33	-	40	ns
		$n\overline{CP}1$ to nQ2; see Fig. 5								
		V_{CC} = 2.0 V	-	74	210	-	265	-	315	ns
		V_{CC} = 4.5 V	-	27	42	-	53	-	63	ns
		V_{CC} = 5 V; C_L = 15 pF	-	23	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	22	36	-	45	-	54	ns
		$n\overline{CP}1$ to nQ3; see Fig. 5								
		V_{CC} = 2.0 V	-	50	155	-	195	-	235	ns
		V_{CC} = 4.5 V	-	18	31	-	39	-	47	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	26	-	33	-	40	ns
t_{PHL}	HIGH to LOW propagation delay	nMR to nQn; see Fig. 6								
		V_{CC} = 2.0 V	-	52	165	-	205	-	250	ns
		V_{CC} = 4.5 V	-	19	33	-	41	-	50	ns
		V_{CC} = 5 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	28	-	35	-	43	ns
t_t	transition time	nQn; see Fig. 5 [3]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	Min	Max	
t_W	pulse width	$n\overline{CP}0$, $n\overline{CP}1$; HIGH or LOW; see Fig. 5									
		V_{CC} = 2.0 V		80	19	-	100	-	120	-	ns
		V_{CC} = 4.5 V		16	7	-	20	-	24	-	ns
		V_{CC} = 6.0 V		14	6	-	17	-	20	-	ns
		nMR HIGH; see Fig. 6									
		V_{CC} = 2.0 V		80	28	-	105	-	130	-	ns
		V_{CC} = 4.5 V		17	10	-	21	-	26	-	ns
		V_{CC} = 6.0 V		14	8	-	18	-	22	-	ns
t_{rec}	recovery time	nMR to $n\overline{CP}n$; see Fig. 6									
		V_{CC} = 2.0 V		75	22	-	95	-	110	-	ns
		V_{CC} = 4.5 V		15	8	-	19	-	22	-	ns
		V_{CC} = 6.0 V		13	6	-	16	-	19	-	ns
f_{max}	maximum frequency	$n\overline{CP}n$; see Fig. 5									
		V_{CC} = 2.0 V		6.0	20	-	4.8	-	4.0	-	MHz
		V_{CC} = 4.5 V		30	60	-	24	-	20	-	MHz
		V_{CC} = 5 V; C_L = 15 pF		-	66	-	-	-	-	-	MHz
		V_{CC} = 6.0 V		35	71	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC}	[4]	-	20	-	-	-	-	-	pF
74HCT390											
t_{pd}	propagation delay	$n\overline{CP}0$ to nQ0; see Fig. 5	[2]								
		V_{CC} = 4.5 V		-	21	34	-	43	-	51	ns
		V_{CC} = 5 V; C_L = 15 pF		-	18	-	-	-	-	-	ns
		$n\overline{CP}1$ to nQ1; see Fig. 5									
		V_{CC} = 4.5 V		-	22	38	-	48	-	57	ns
		V_{CC} = 5 V; C_L = 15 pF		-	19	-	-	-	-	-	ns
		$n\overline{CP}1$ to nQ2; see Fig. 5									
		V_{CC} = 4.5 V		-	30	51	-	64	-	77	ns
		V_{CC} = 5 V; C_L = 15 pF		-	26	-	-	-	-	-	ns
		$n\overline{CP}1$ to nQ3; see Fig. 5									
		V_{CC} = 4.5 V		-	22	38	-	48	-	57	ns
		V_{CC} = 5 V; C_L = 15 pF		-	19	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	nMR to nQn; see Fig. 6									
		V_{CC} = 4.5 V		-	21	36	-	45	-	54	ns
		V_{CC} = 5 V; C_L = 15 pF		-	18	-	-	-	-	-	ns
t_t	transition time	nQn; see Fig. 5	[3]								
		V_{CC} = 4.5 V		-	7	15	-	19	-	22	ns

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	Min	Max	
t_W	pulse width	$n\overline{CP}0$, $n\overline{CP}1$; HIGH or LOW; see Fig. 5									
		V_{CC} = 4.5 V		18	8	-	23	-	27	-	ns
		nMR HIGH; see Fig. 6									
		V_{CC} = 4.5 V		17	10	-	21	-	26	-	ns
t_{rec}	recovery time	nMR to $n\overline{CP}n$;see Fig. 6									
		V_{CC} = 4.5 V		15	8	-	19	-	22	-	ns
f_{max}	maximum frequency	$n\overline{CP}n$; see Fig. 5									
		V_{CC} = 4.5 V		27	55	-	22	-	18	-	MHz
		V_{CC} = 5 V; C_L = 15 pF		-	61	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; V_I = GND to V_{CC} - 1.5 V	[4]	-	21	-	-	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_t is the same as t_{THL} and t_{TLH}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum(C_L \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}{}^2 \times f_o)$ = sum of outputs.

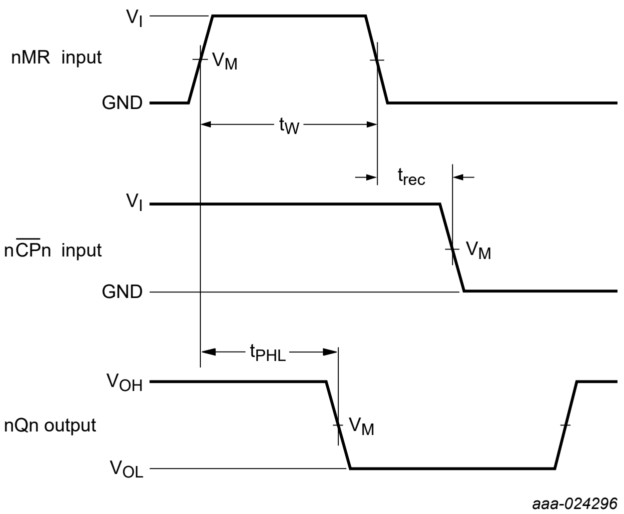
10.1. Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. The clock input (n$\overline{CP}$n) to output (nQn) propagation delays, output transition time, clock pulse width and maximum clock frequency



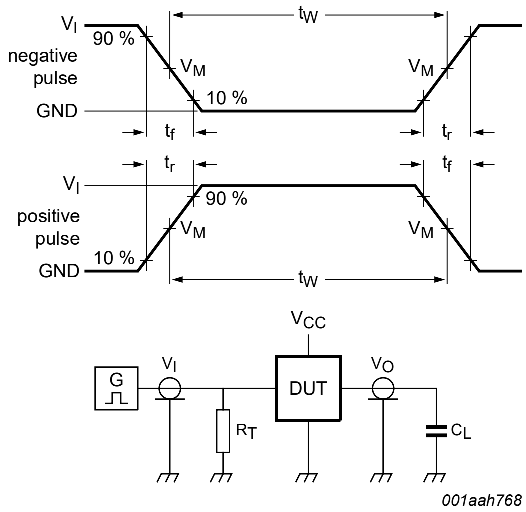
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. The master reset (nMR) pulse width, master reset to output (nQn) propagation delays and master reset to clock (n$\overline{CP}$n) recovery time

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74HC390	$0.5V_{CC}$	$0.5V_{CC}$
74HCT390	1.3 V	1.3 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

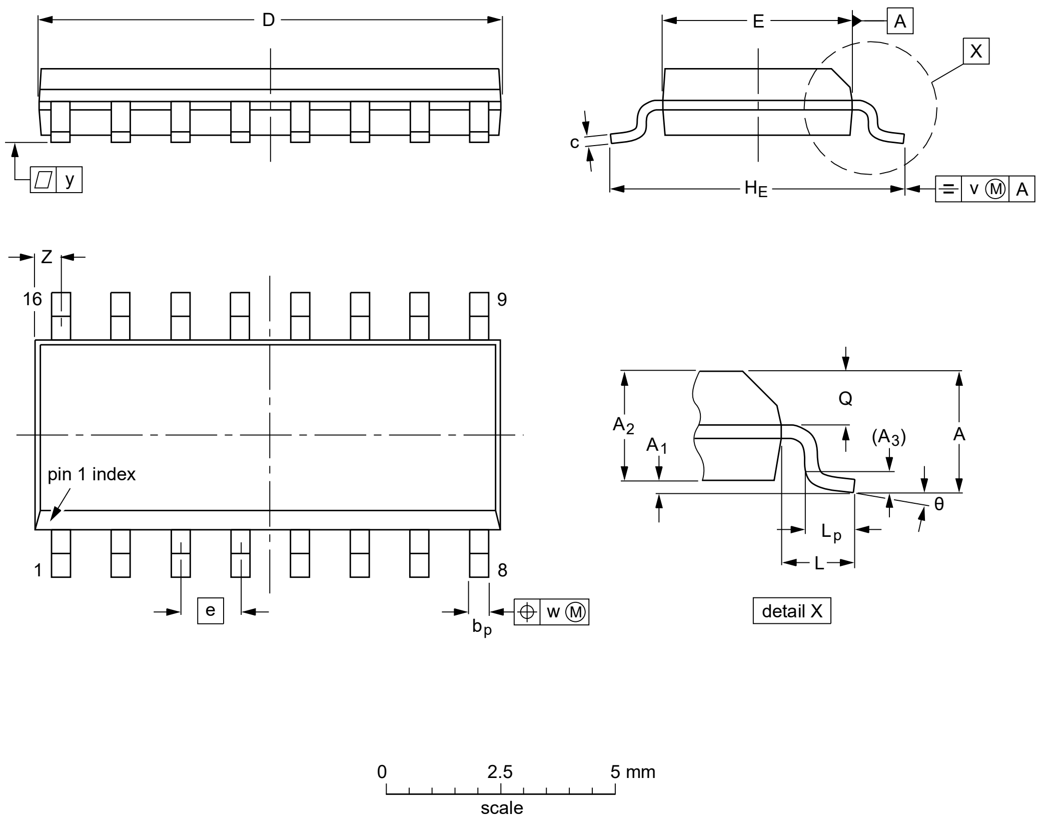
Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC390	V_{CC}	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT390	3 V	6 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

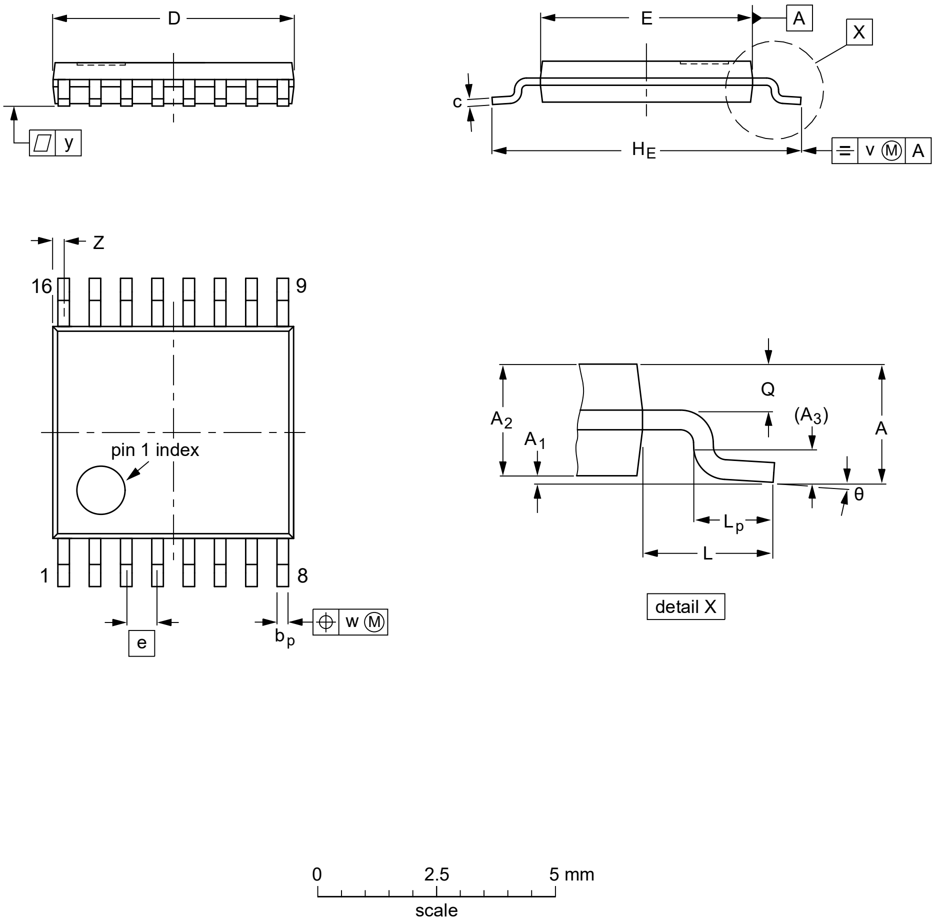
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 8. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 9. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT390 v.5	20211018	Product data sheet	-	74HC_HCT390 v.4
Modifications:	• Type number 74HCT390PW (SOT403-1 / TSSOP16) added.			
74HC_HCT390 v.4	20200821	Product data sheet	-	74HC_HCT390 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC390DB and 74HCT390DB (SOT338-1) removed. • Table 1: typo corrected. • Table 5: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT390 v.3	20160816	Product data sheet	-	74HC_HCT390_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC390N and 74HCT390N removed.			
74HC_HCT390_CNV v.2	19901201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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