

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT640

**Octal bus transceiver; 3-state;
inverting**

Product specification
File under Integrated Circuits, IC06

March 1988

Octal bus transceiver; 3-state; inverting

74HC/HCT640

FEATURES

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable (\overline{OE}) input for easy cascading and a send/receive (DIR) for direction control. \overline{OE} controls the outputs so that the buses are effectively isolated. The "640" is similar to the "245" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} /t _{PLH}	propagation delay A _n to B _n ; B _n to A _n	C _L = 15 pF; V _{CC} = 5 V	9	9	ns
C _I	input capacitance		3.5	3.5	pF
C _{I/O}	input/output capacitance		10	10	pF
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	35	35	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B ₀ to B ₇	data inputs/outputs
19	\overline{OE}	output enable input (active LOW)
20	V _{CC}	positive supply voltage

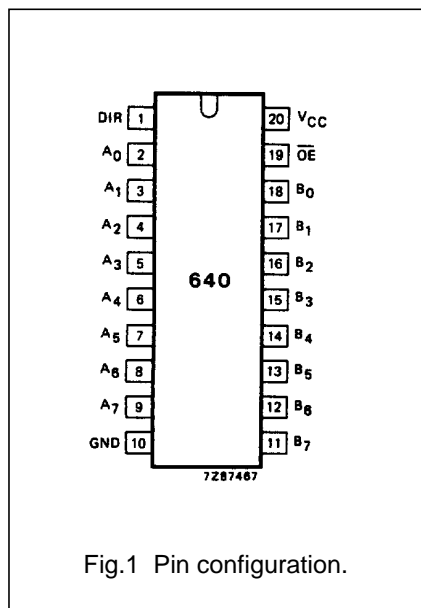


Fig.1 Pin configuration.

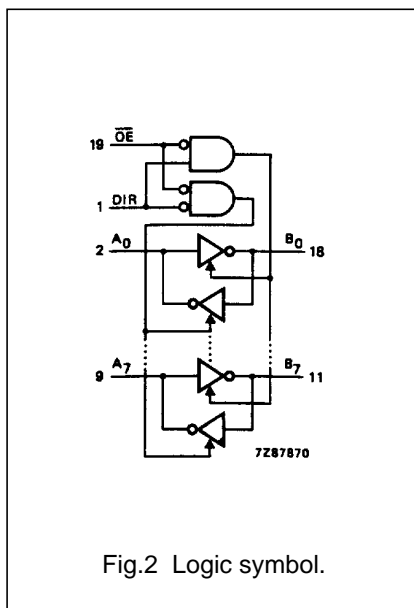


Fig.2 Logic symbol.

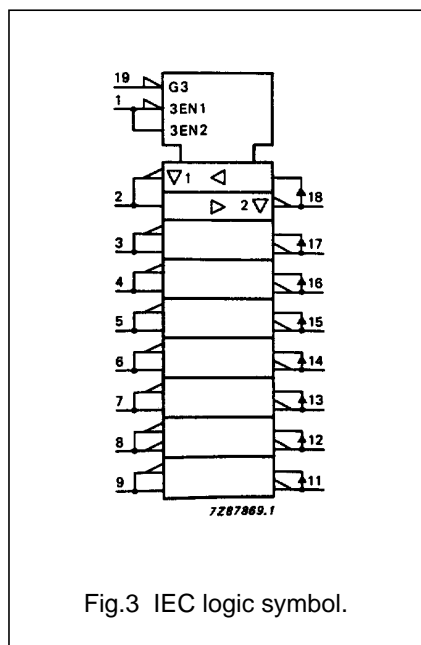


Fig.3 IEC logic symbol.

FUNCTION TABLE

inputs		inputs/outputs	
\overline{OE}	DIR	A _n	B _n
L	L	A= \overline{B}	inputs
L	H	inputs	B= \overline{A}
H	X	Z	Z

Note

- H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

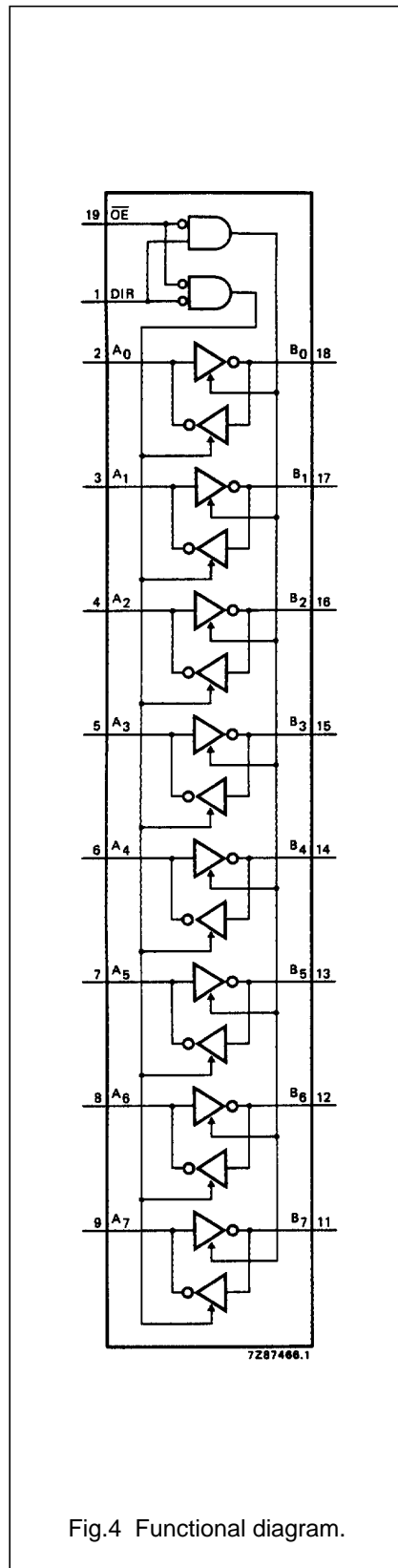


Fig.4 Functional diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		30 11 9	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.5
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE} , DIR to A _n ; \overline{OE} , DIR to B _n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE} , DIR to A _n ; \overline{OE} , DIR to B _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	1.50
B _n	1.50
\overline{OE}	1.50
DIR	0.90

AC CHARACTERISTICS FOR 74HCT

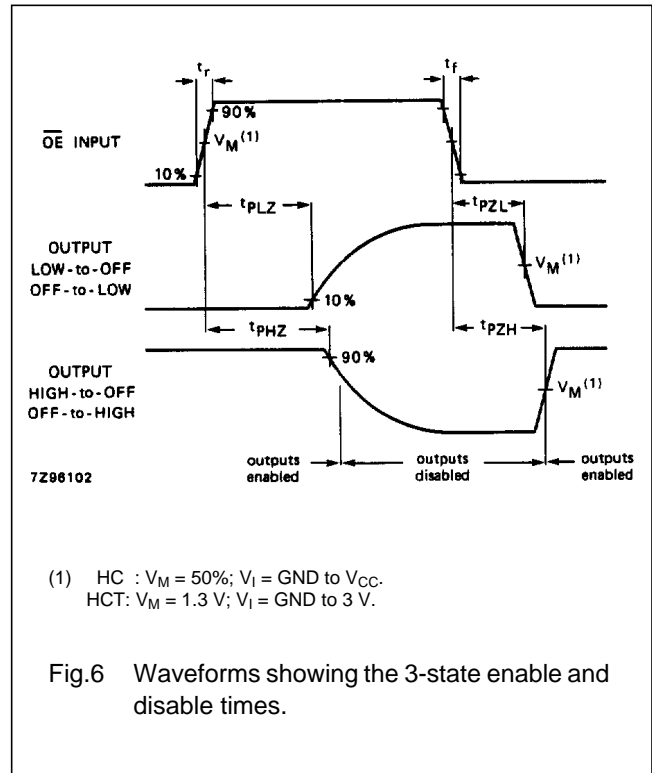
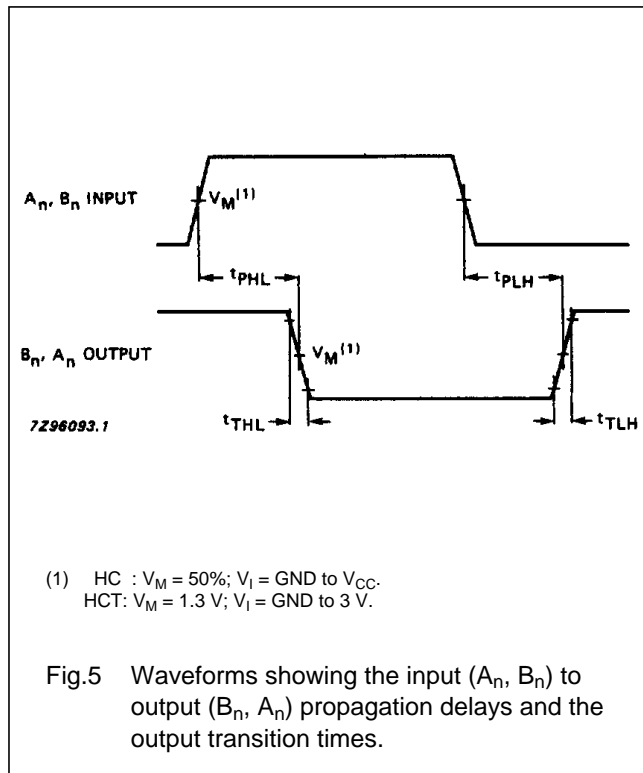
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		11	22		28		33	ns	4.5	Fig.5	
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE} , DIR to A _n ; \overline{OE} , DIR to B _n		18	30		38		45	ns	4.5	Fig.6	
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE} , DIR to A _n ; \overline{OE} , DIR to B _n		19	30		38		45	ns	4.5	Fig.6	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.5	

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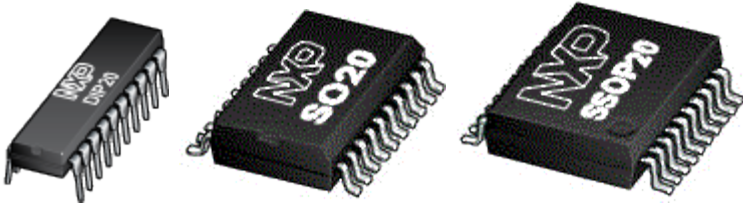
AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

74HC/HCT640 Packaging Information



Type Number	Orderable Part Number	Package Name
74HC640N	74HC640N	DIP20
74HC640D	74HC640D,652	SO20
74HC640DB	74HC640DB	SSOP20
74HCT640N	74HCT640N,652	DIP20
74HCT640D	74HCT640D,653	SO20
74HCT640D	74HCT640D,652	SO20
74HCT640DB	74HCT640DB,118	SSOP20
74HCT640DB	74HCT640DB,112	SSOP20

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