

# 74LV164

## 8-bit serial-in/parallel-out shift register

Rev. 4 — 9 December 2015

Product data sheet

### 1. General description

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The 74LV164 is a low-voltage, Si-gate CMOS device and is pin and function compatible with the 74HC164 and 74HCT164.

The 74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB) and either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock input (CP) and enters into Q0, which is the logical AND-function of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset input (MR) overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

### 2. Features and benefits

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- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low-voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce):  $< 0.8$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot):  $> 2$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Gated serial data inputs
- Asynchronous master reset
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from  $-40$  °C to  $+80$  °C and from  $-40$  °C to  $+125$  °C.

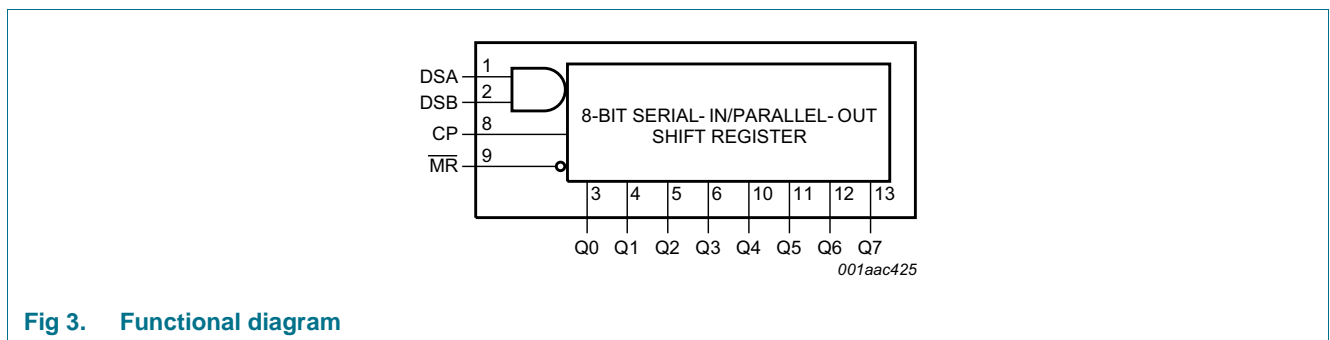
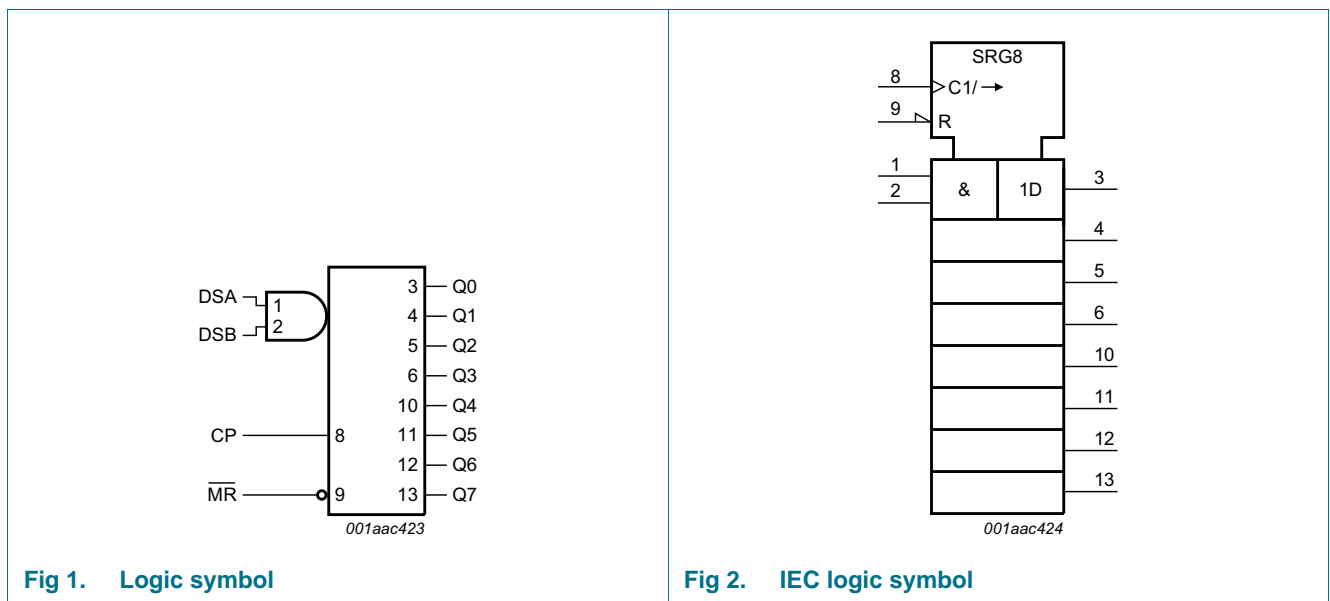


### 3. Ordering information

Table 1. Ordering information

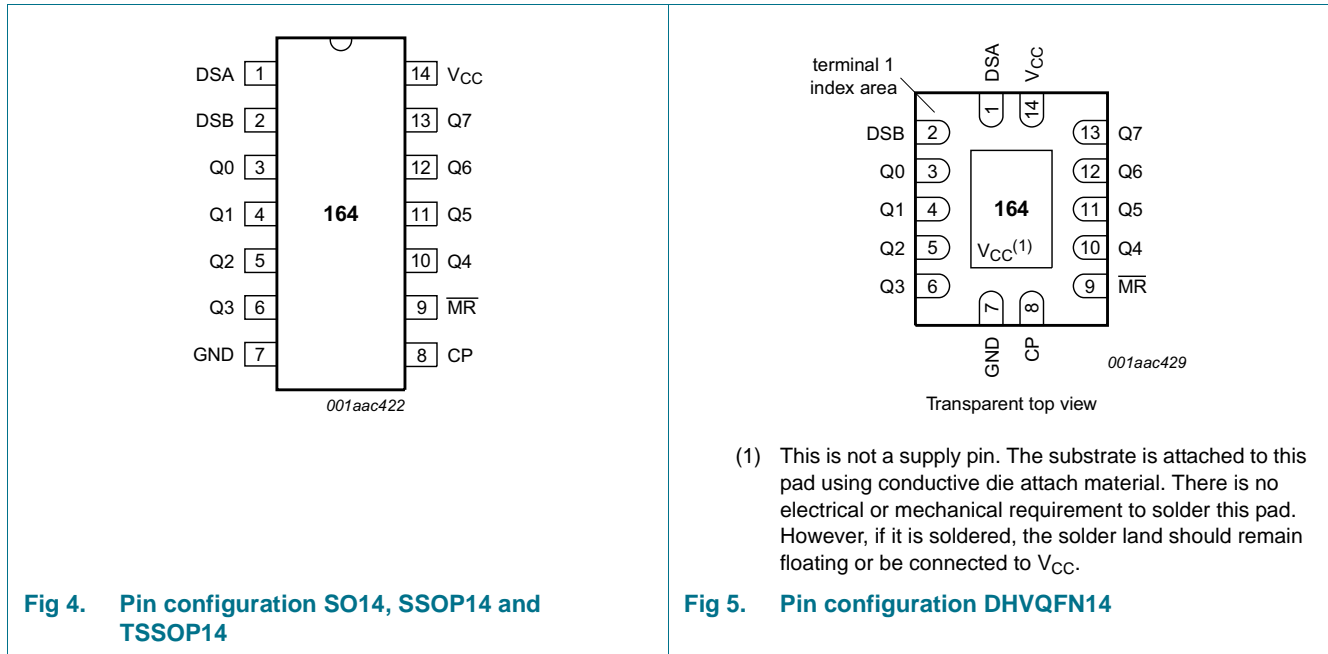
Type number	Package			Version
	Temperature range	Name	Description	
74LV164D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV164DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV164PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV164BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram



## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	data input SA
DSB	2	data input SB
Q0	3	output 0
Q1	4	output 1
Q2	5	output 2
Q3	6	output 3
GND	7	ground (0 V)
CP	8	clock input (edge triggered LOW-to-HIGH)
$\overline{\text{MR}}$	9	master reset input (active LOW)
Q4	10	output 4
Q5	11	output 5
Q6	12	output 6
Q7	13	output 7
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

### 6.1 Function table

Table 3. Function table<sup>[1]</sup>

Operating mode	Input				Output	
	MR	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 ↑ = LOW-to-HIGH clock transition;  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
 q = lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ <sup>[1]</sup>	-	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ <sup>[1]</sup>	-	±50	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	±25	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		SO14 package <sup>[2]</sup>	-	500	mW
		(T)SSOP14 package <sup>[3]</sup>	-	500	mW
		DHVQFN14 package <sup>[4]</sup>	-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2]  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 [3]  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
 [4]  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage	[1]	1.0	3.3	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.0 V to 2.0 V	-	-	500	ns/V
		V <sub>CC</sub> = 2.0 V to 2.7 V	-	-	200	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	100	ns/V
		V <sub>CC</sub> = 3.6 V to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 5.5 V, but LV devices are guaranteed to function down to V<sub>CC</sub> = 1.0 V (with input levels GND or V<sub>CC</sub>).

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	0.9	-	-	0.9	-	V
		V <sub>CC</sub> = 2.0 V	1.4	-	-	1.4	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.3	-	0.3	V
		V <sub>CC</sub> = 2.0 V	-	-	0.6	-	0.6	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	-	0.3V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.2 V	-	1.2	-	-	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V	2.5	2.7	-	2.5	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 3.0 V	2.8	3.0	-	2.8	-	V
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 4.5 V	4.3	4.5	-	4.3	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 3.0 V	2.4	2.82	-	2.2	-	V
I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 4.5 V	3.6	4.2	-	3.5	-	V		

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.2 V	-	0	-	-	-	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 3.0 V	-	0.25	0.40	-	0.50	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 4.5 V	-	0.35	0.55	-	0.65	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20.0	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 GND = 0 V; For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	CP to Qn; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	75	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	26	39	-	49	ns
		V <sub>CC</sub> = 2.7 V	-	19	29	-	36	ns
		V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF	-	12	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	14	23	-	29	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	-	12	19	-	24	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR to Qn; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.2 V	-	75	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	26	39	-	49	ns
		V <sub>CC</sub> = 2.7 V	-	19	29	-	36	ns
		V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF	-	12	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	14	23	-	29	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	-	12	19	-	24	ns

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V; For test circuit see [Figure 9](#).*

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>w</sub>	pulse width	CP; see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 2.0 V	34	9	-	41	-	ns
		V <sub>CC</sub> = 2.7 V	25	6	-	30	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	20	5	-	24	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	13	4	-	16	-	ns
		MR; <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 2.0 V	34	10	-	41	-	ns
		V <sub>CC</sub> = 2.7 V	25	8	-	30	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	20	6	-	24	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	13	5	-	16	-	ns
t <sub>rec</sub>	recovery time	MR to CP; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.2 V	-	30	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	19	10	-	24	-	ns
		V <sub>CC</sub> = 2.7 V	14	8	-	18	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	11	6	-	14	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	8	5	-	10	-	ns
t <sub>su</sub>	set-up time	Dn to CP; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 1.2 V	-	15	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	22	5	-	26	-	ns
		V <sub>CC</sub> = 2.7 V	16	4	-	19	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	13	3	-	15	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	9	2	-	10	-	ns
t <sub>h</sub>	hold time Dn to CP	see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 1.2 V	-	-10	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	5	-3	-	5	-	ns
		V <sub>CC</sub> = 2.7 V	5	-2	-	5	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	5	-2	-	5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	5	-1	-	5	-	ns
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 6</a>						
		V <sub>CC</sub> = 2.0 V	14	40	-	12	-	MHz
		V <sub>CC</sub> = 2.7 V	19	58	-	16	-	MHz
		V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF	-	78	-	-	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	24	70	-	20	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	36	100	-	30	-	MHz

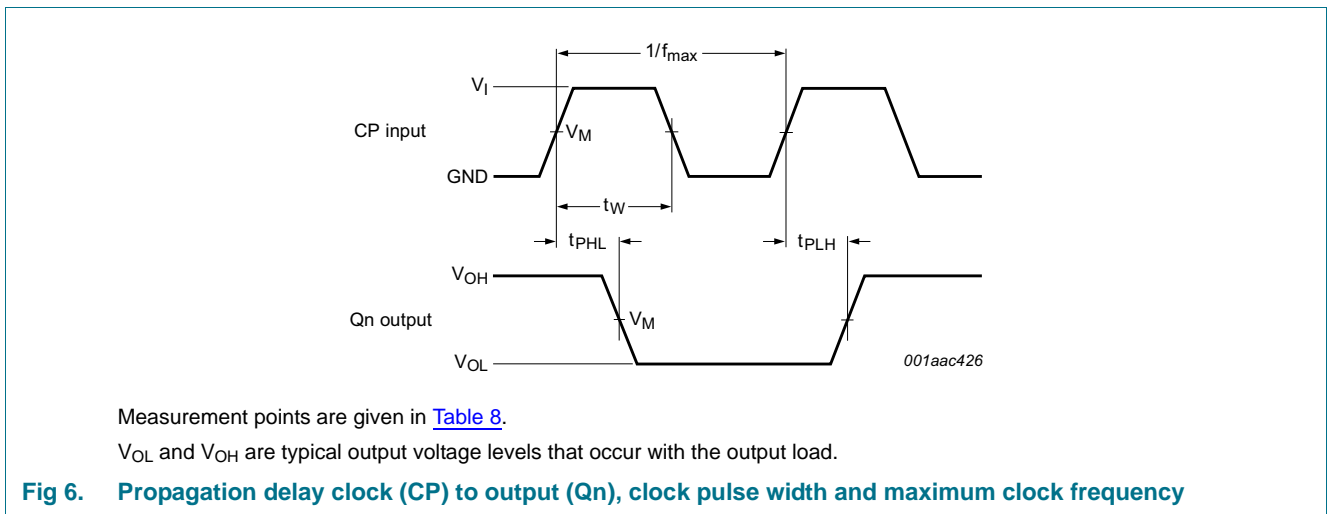
**Table 7. Dynamic characteristics ...continued**

$GND = 0\text{ V}$ ; For test circuit see [Figure 9](#).

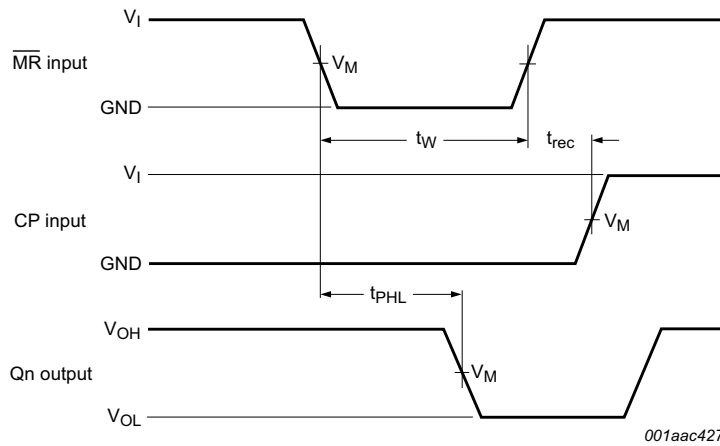
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$C_{PD}$	power dissipation capacitance	$V_{CC} = 3.3\text{ V}$ ; $C_L = 50\text{ pF}$ ; $f_i = 1\text{ MHz}$ ; $V_i = GND\text{ to }V_{CC}$ <sup>[4]</sup>	-	40	-	-	-	pF

- [1] All typical values are measured at  $T_{amb} = 25\text{ °C}$ .
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 5.0\text{ V}$ ).
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz,  $f_o$  = output frequency in MHz  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in V  
 $N$  = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## 11. Waveforms



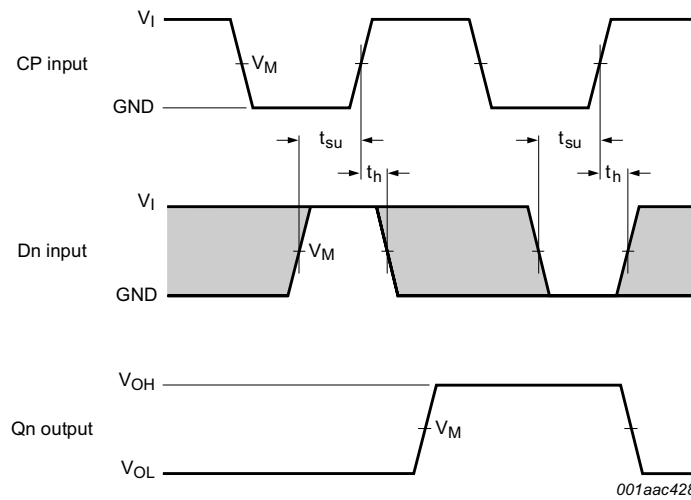




Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. Pulse width master reset ( $\overline{MR}$ ), propagation delay master reset ( $\overline{MR}$ ) to output ( $Q_n$ ) and the master reset ( $\overline{MR}$ ) to clock ( $CP$ ) recovery time**



Measurement points are given in [Table 8](#).

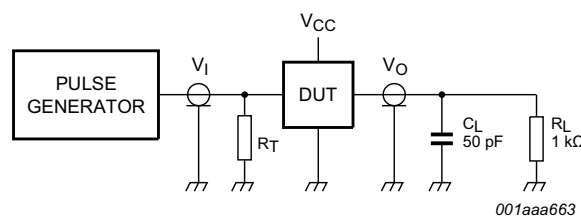
$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 8. Data set-up and hold times inputs ( $D_n$ ) to clock ( $CP$ )**

Table 8. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.0 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



001aaa663

Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 9. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		Test
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	
1.2 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$
2.0 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF, 15 pF	1 kΩ	$t_{PHL}, t_{PLH}$
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 kΩ	$t_{PHL}, t_{PLH}$

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

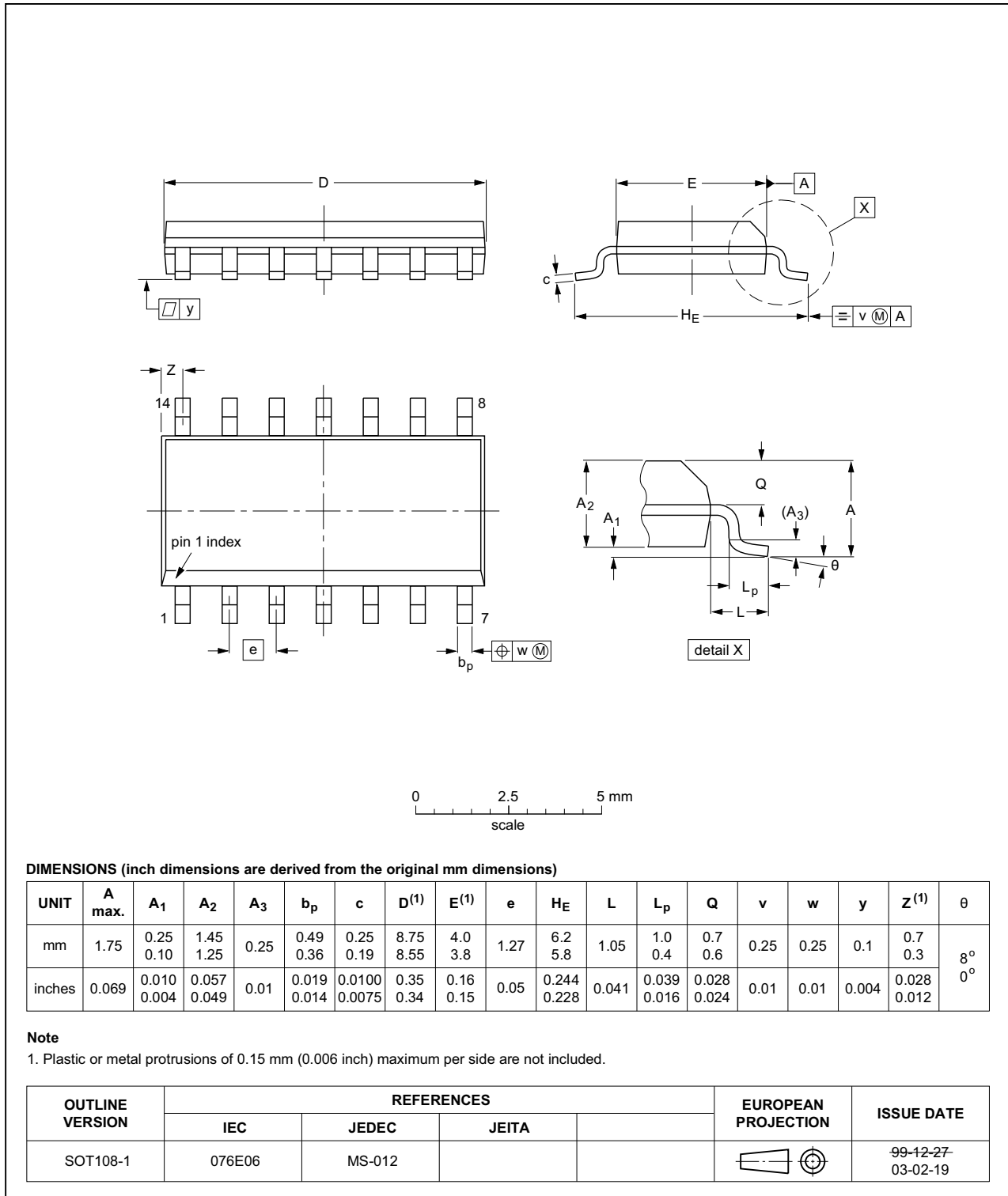


Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

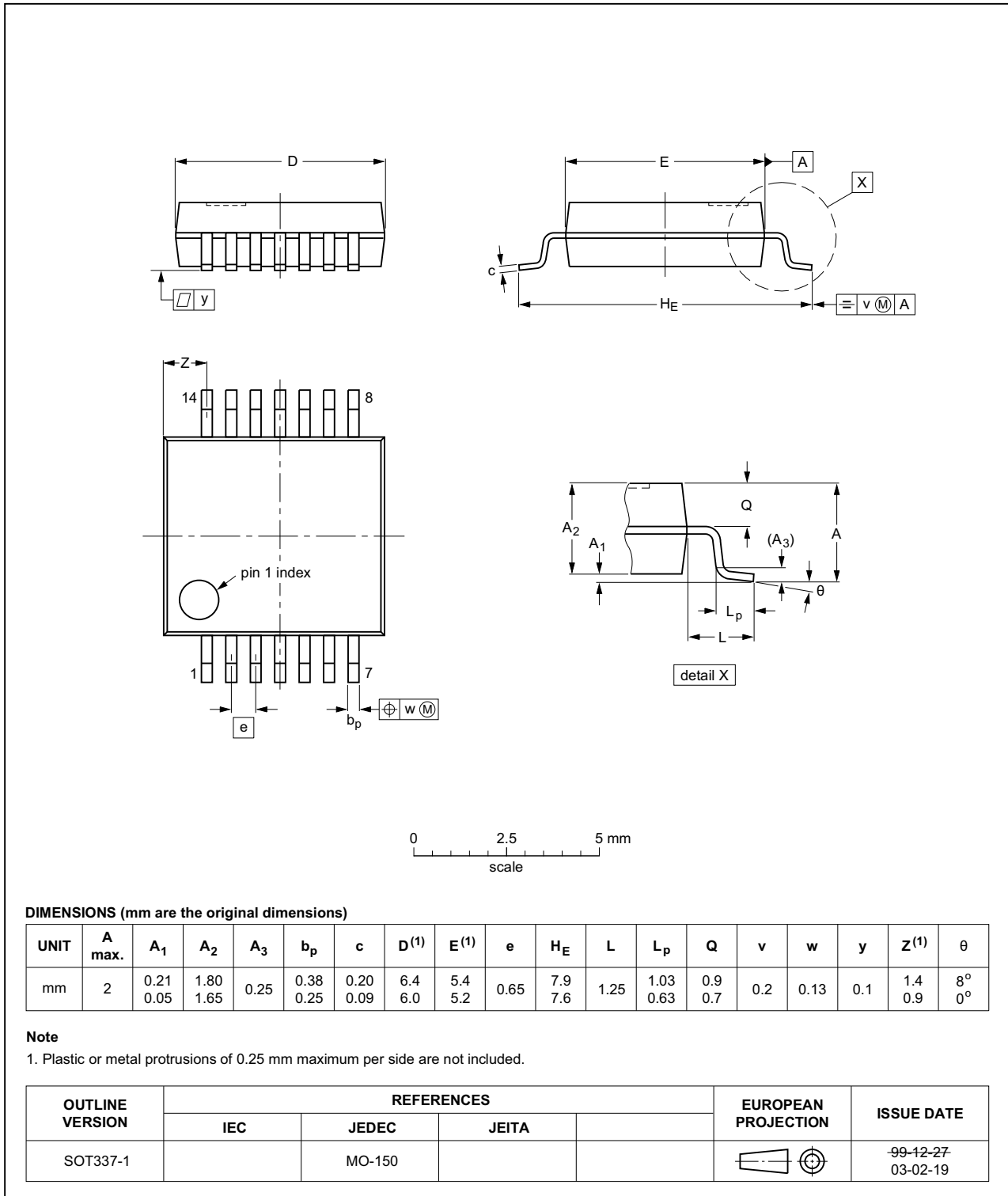


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

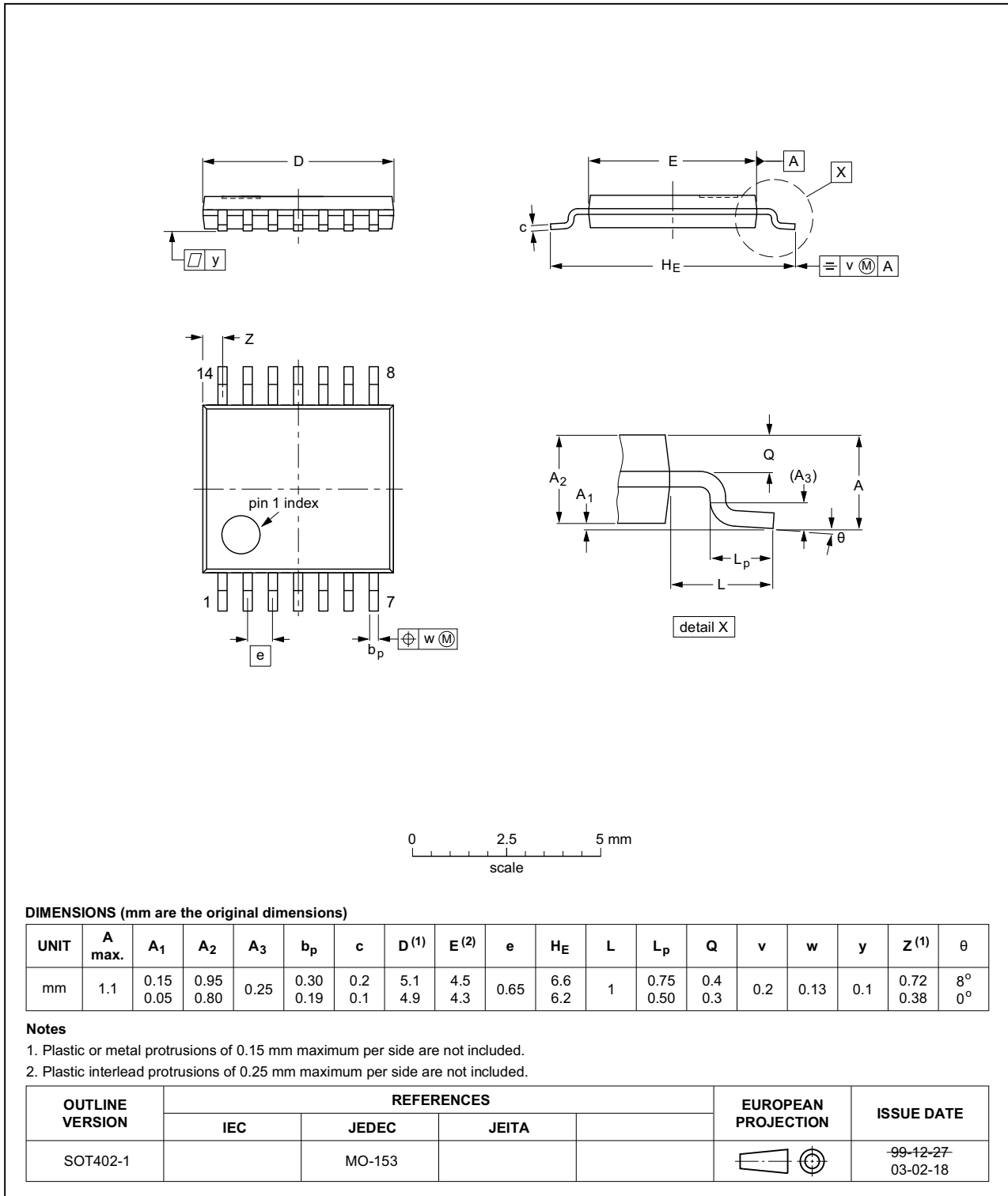


Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

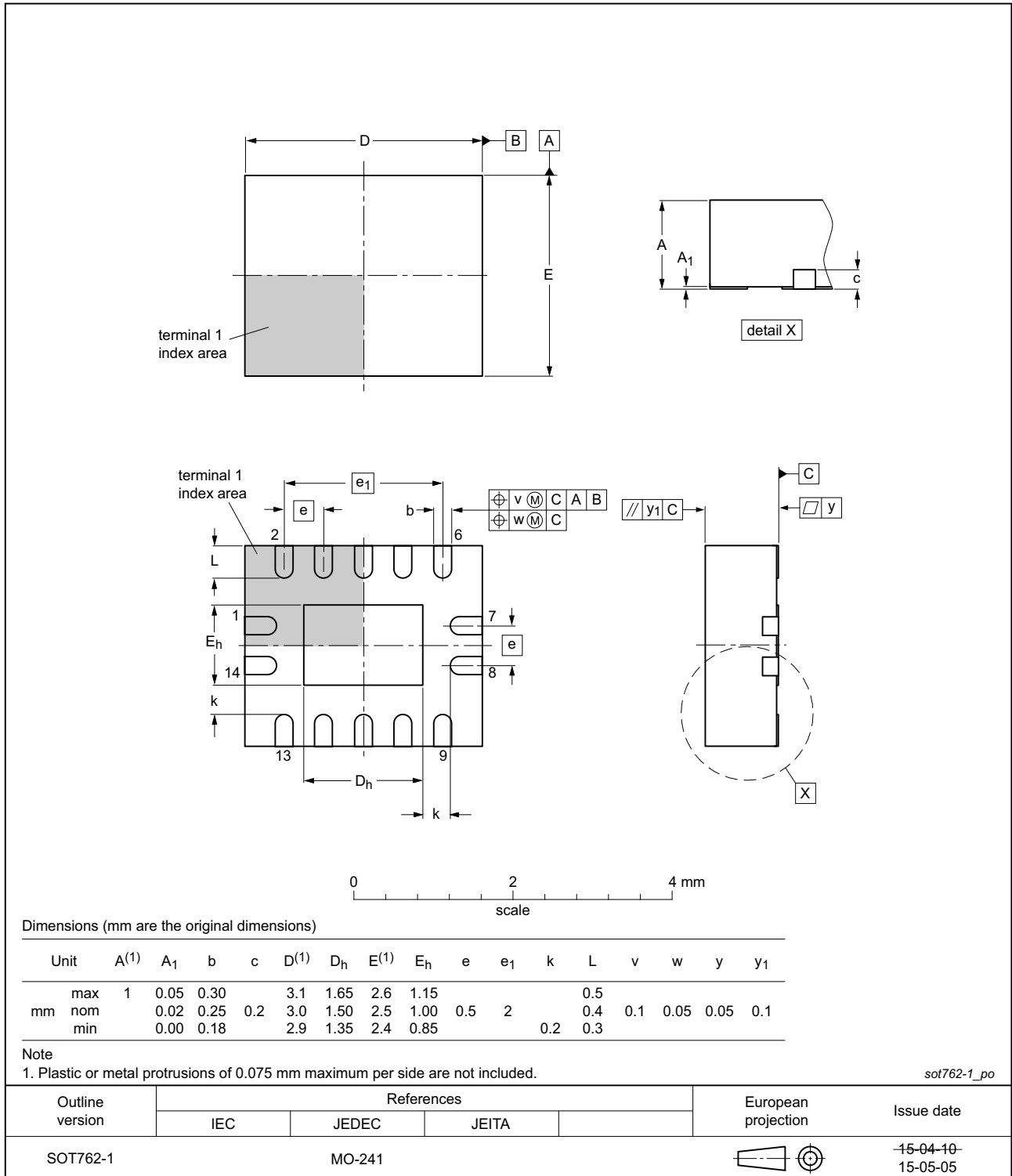


Fig 13. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV164 v.4	20151209	Product data sheet	-	74LV164 v.3
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LV164N (SOT27-1) removed.</li> </ul>			
74LV164 v.3	20050204	Product data sheet	-	74LV164 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors</li> <li>Added: type number 74LV164BQ (DHSVFN14 package).</li> </ul>			
74LV164 v.2	19980507	Product specification	-	74LV164 v.1
74LV164 v.1	19970328	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 17. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>3</b>
5.1	Pinning .....	3
5.2	Pin description .....	3
<b>6</b>	<b>Functional description</b> .....	<b>4</b>
6.1	Function table .....	4
<b>7</b>	<b>Limiting values</b> .....	<b>4</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>5</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>5</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>6</b>
<b>11</b>	<b>Waveforms</b> .....	<b>8</b>
<b>12</b>	<b>Package outline</b> .....	<b>11</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>15</b>
<b>14</b>	<b>Revision history</b> .....	<b>15</b>
<b>15</b>	<b>Legal information</b> .....	<b>16</b>
15.1	Data sheet status .....	16
15.2	Definitions .....	16
15.3	Disclaimers .....	16
15.4	Trademarks .....	17
<b>16</b>	<b>Contact information</b> .....	<b>17</b>
<b>17</b>	<b>Contents</b> .....	<b>18</b>

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Date of release: 9 December 2015

Document identifier: 74LV164

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