

74LVC163

Presettable synchronous 4-bit binary counter; synchronous reset

Rev. 6 — 20 November 2012

Product data sheet

1. General description

The 74LVC163 is a synchronous presettable binary counter which features an internal look-ahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (pin CP). The outputs (pins Q0 to Q3) of the counters may be preset to a HIGH-level or LOW-level. A LOW-level at the parallel enable input (pin PE) disables the counting action and causes the data at the data inputs (pins D0 to D3) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (pin CEP and CET). A LOW-level at the master reset input (pin MR) sets all four outputs of the flip-flops (pins Q0 to Q3) to LOW-level after the next positive-going transition on the clock input (pin CP) (provided that the set-up and hold time requirements for PE are met). This action occurs regardless of the levels at input pins \overline{PE} , CET and CEP. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (pin CEP and CET) must be HIGH in count. The CET input is fed forward to enable the terminal count output (pin TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH-level output of Q0. This pulse can be used to enable the next cascaded stage.

The maximum clock frequency for the cascaded counters is determined by t_{PHL} (propagation delay CP to TC) and t_{su} (set-up time CEP to CP) according to the formula:

$$f_{max} = \frac{1}{t_{PHL(max)} + t_{su}}$$

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Synchronous reset
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)



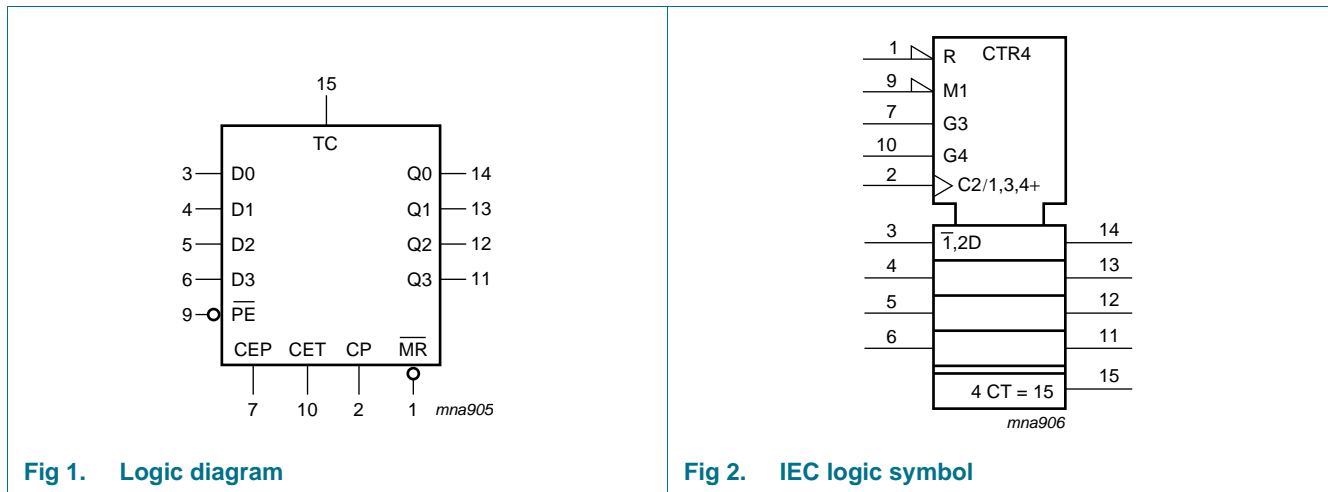
- ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to 125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC163D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC163DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LVC163PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC163BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram



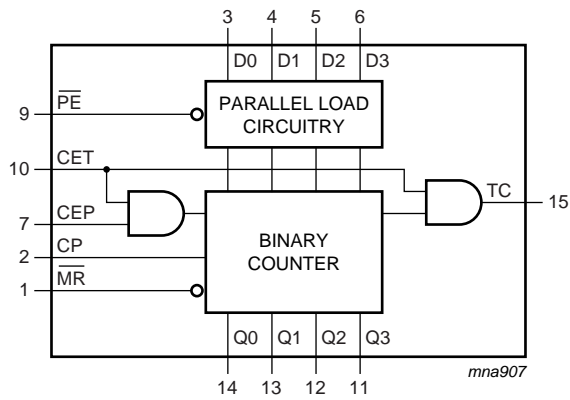


Fig 3. Functional diagram

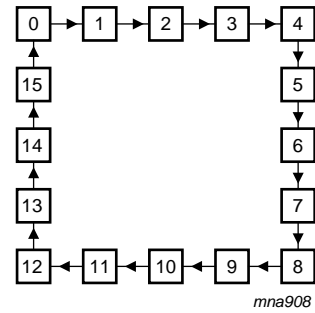
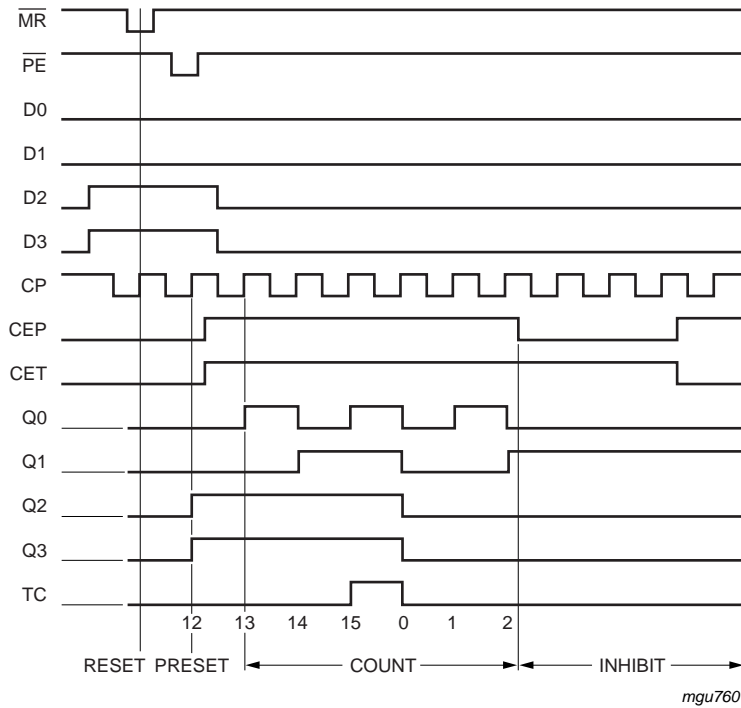


Fig 4. State diagram



Typical timing sequence: Reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

Fig 5. Timing sequence

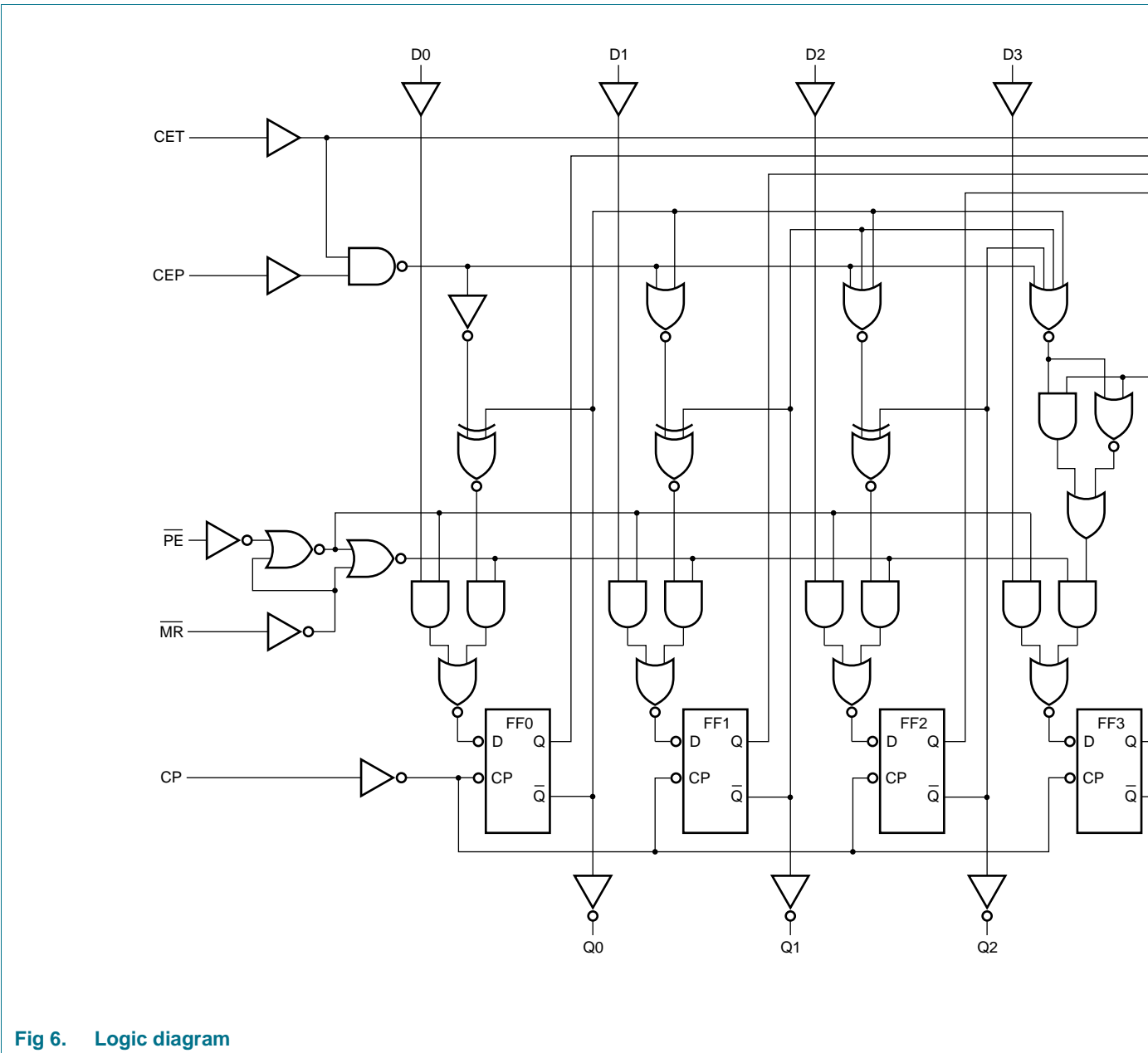
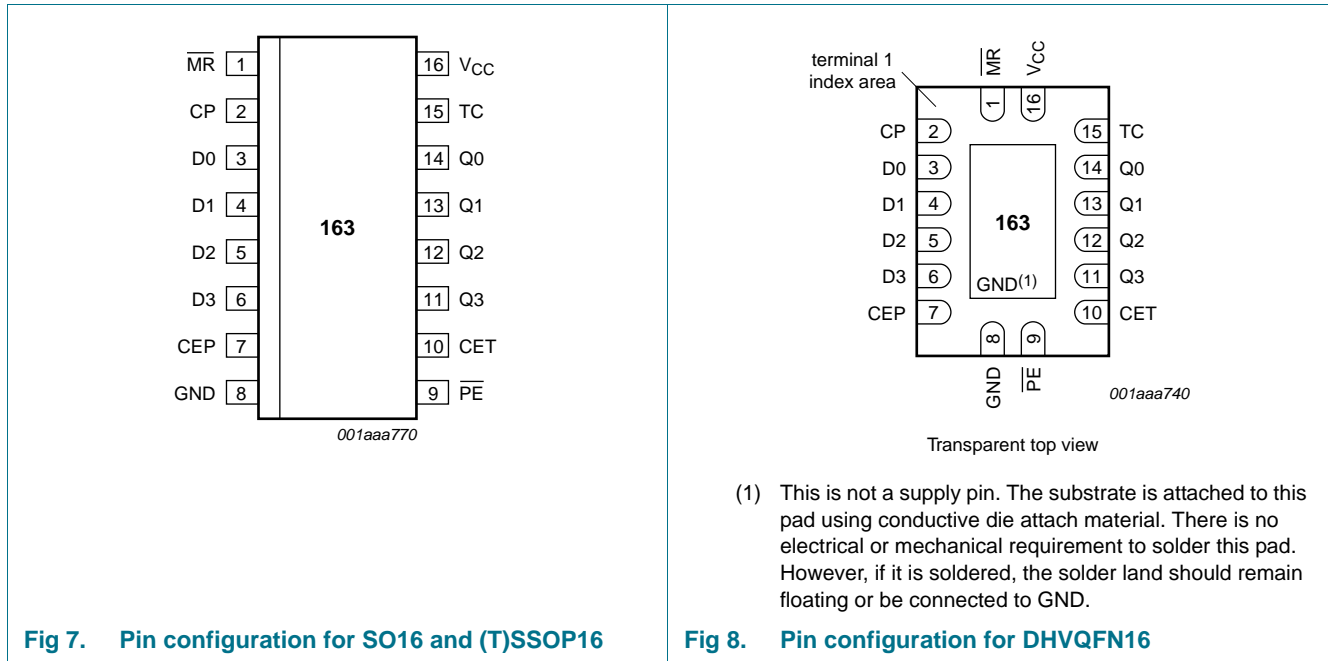


Fig 6. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	synchronous master reset (active LOW)
CP	2	clock input (LOW-to-HIGH, edge-triggered)
D[0:3]	3, 4, 5, 6	data input
CEP	7	count enable input
GND	8	ground (0)
PE	9	parallel enable input (active LOW)
CET	10	count enable carry input
Q[0:3]	14, 13, 12, 11	flip-flop output
TC	15	terminal count output
V _{CC}	16	supply voltage

6. Functional description

Table 3. Functional table^[1]

Operating modes	Input						Output	
	MR	CP	CEP	CET	\overline{PE}	Dn	Qn	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
Count	h	↑	h	h	h	X	count	*
Hold (do nothing)	h	X	l	X	h	X	q _n	*
	h	X	X	l	h	X	q _n	L

[1] * = the TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH)

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition

X = don't care

↑ = LOW-to-HIGH clock transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		^[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage		^[2] -0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	CP to Q _n ; see Figure 9 [2]						
		V _{CC} = 1.2 V	-	18	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	7.4	14.5	1.5	16.7	ns
		V _{CC} = 2.3 V to 2.7 V	2.6	4.2	8.1	2.6	9.4	ns
		V _{CC} = 2.7 V	1.5	4.0	7.3	1.5	9.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.8	7.3	1.5	9.5	ns
		CP to TC; see Figure 9 [2]						
		V _{CC} = 1.2 V	-	23	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	8.5	15.7	1.9	18.1	ns
		V _{CC} = 2.3 V to 2.7 V	3.0	4.8	8.8	3.0	10.2	ns
		V _{CC} = 2.7 V	1.5	4.6	8.1	1.5	10.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	4.3	7.9	1.5	10.0	ns
		CET to TC; see Figure 10 [2]						
		V _{CC} = 1.2 V	-	16	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.3	12.7	1.5	14.6	ns
V _{CC} = 2.3 V to 2.7 V	2.3	3.6	7.1	2.3	8.2	ns		
V _{CC} = 2.7 V	1.5	3.9	6.9	1.5	9.0	ns		
V _{CC} = 3.0 V to 3.6 V	1.5	3.3	6.4	1.5	8.0	ns		
t _w	pulse width	clock HIGH or LOW; see Figure 9						
		V _{CC} = 1.65 V to 1.95 V	6.0	-	-	6.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	5.0	-	-	5.0	-	ns
		V _{CC} = 2.7 V	5.0	-	-	5.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	4.0	1.2	-	4.0	-	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 14](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ ^[1]	Max	Min	Max		
t _{su}	set-up time	Dn to CP; see Figure 12							
		V _{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns	
		V _{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns	
		V _{CC} = 2.7 V	3.0	-	-	3.0	-	ns	
		V _{CC} = 3.0 V to 3.6 V	2.5	1.0	-	2.5	-	ns	
		MR, \overline{PE} to CP; see Figure 12							
		V _{CC} = 1.65 V to 1.95 V	4.5	-	-	4.5	-	ns	
		V _{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns	
		V _{CC} = 2.7 V	3.5	-	-	3.5	-	ns	
		V _{CC} = 3.0 V to 3.6 V	3.0	1.2	-	3.0	-	ns	
		CEP, CET to CP; see Figure 13							
		V _{CC} = 1.65 V to 1.95 V	8.5	-	-	8.5	-	ns	
		V _{CC} = 2.3 V to 2.7 V	6.5	-	-	6.5	-	ns	
		V _{CC} = 2.7 V	5.5	-	-	5.5	-	ns	
		V _{CC} = 3.0 V to 3.6 V	5.0	2.1	-	5.0	-	ns	
		t _h	hold time	Dn, \overline{PE} , CEP, CET to CP; see Figure 12 and 13					
V _{CC} = 1.65 V to 1.95 V	2.0			-	-	2.0	-	ns	
V _{CC} = 2.3 V to 2.7 V	2.0			-	-	2.0	-	ns	
V _{CC} = 2.7 V	0.0			-	-	0.0	-	ns	
V _{CC} = 3.0 V to 3.6 V	0.5			0.0	-	0.5	-	ns	
f _{max}	maximum frequency	see Figure 9							
		V _{CC} = 1.65 V to 1.95 V	100	-	-	80	-	ns	
		V _{CC} = 2.3 V to 2.7 V	125	-	-	100	-	ns	
		V _{CC} = 2.7 V	150	-	-	120	-	MHz	
		V _{CC} = 3.0 V to 3.6 V	150	200	-	120	-	MHz	
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per input; V _I = GND to V _{CC}	[4]						
		V _{CC} = 1.65 V to 1.95 V	-	9.8	-	-	-	pF	
		V _{CC} = 2.3 V to 2.7 V	-	13.4	-	-	-	pF	
		V _{CC} = 3.0 V to 3.6 V	-	16.6	-	-	-	pF	

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

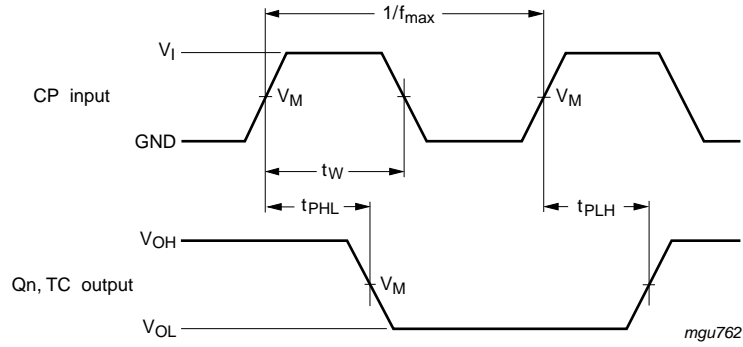
C_L = output load capacitance in pF

V_{CC} = supply voltage in V

N = number of inputs switching

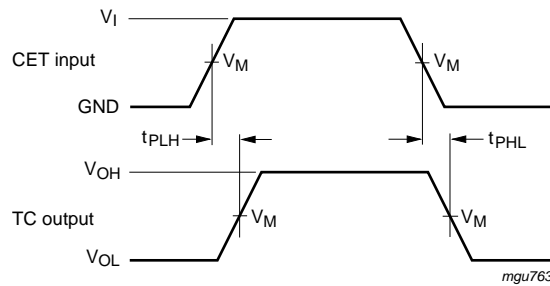
∑(C_L × V_{CC}² × f_o) = sum of outputs

11. AC waveforms



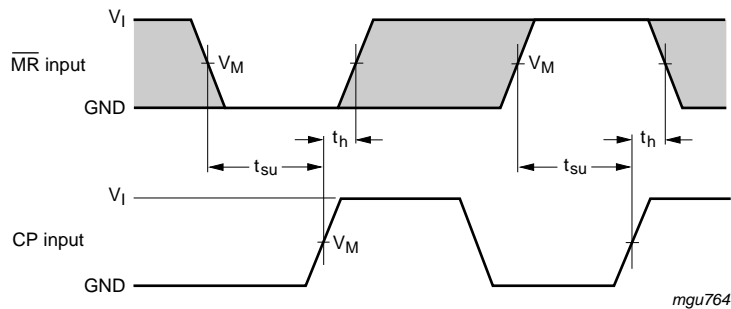
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Clock (CP) to outputs (Qn, TC) propagation delays, the clock pulse width, and the maximum frequency



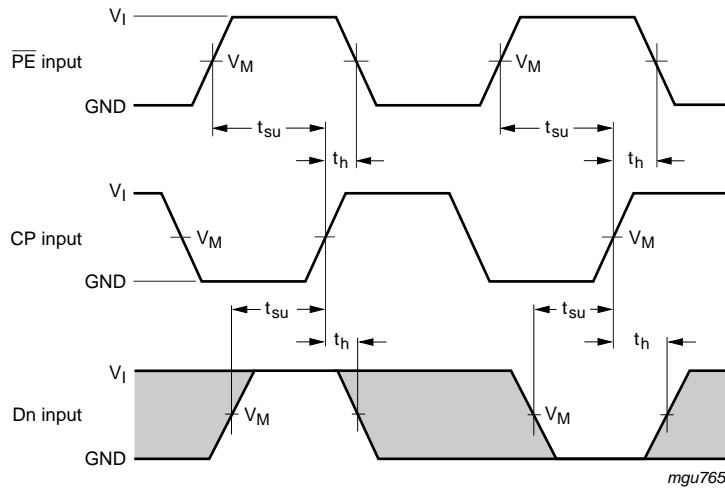
Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. Input (CET) to output (TC) propagation delays



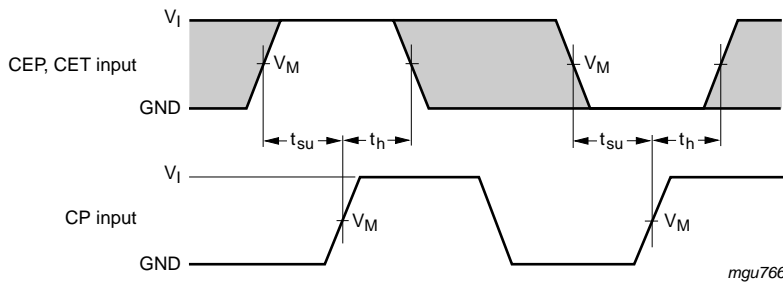
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 11. Master reset (MR) pulse width, the master reset to output (Qn, TC) propagation delays and the master reset to clock (CP) removal times



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 12. Set-up and hold times for the input (Dn) and parallel enable input (\overline{PE})

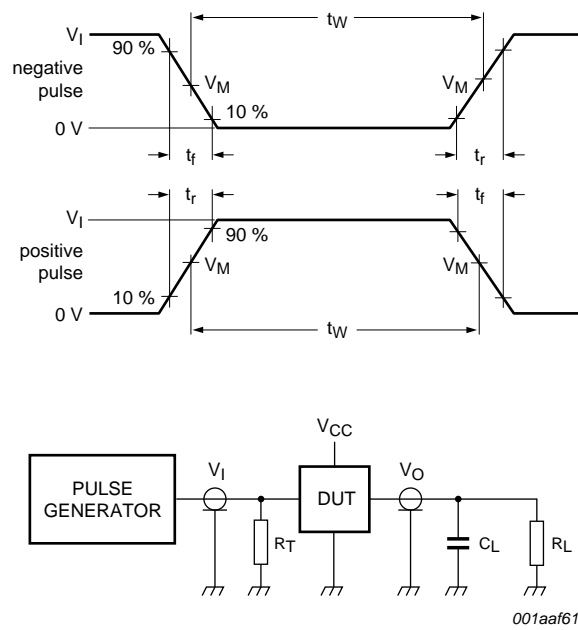


The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 13. CEP and CET set-up and hold times

Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_M
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V



001aa615

Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 14. Load circuitry for switching times

Table 9. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

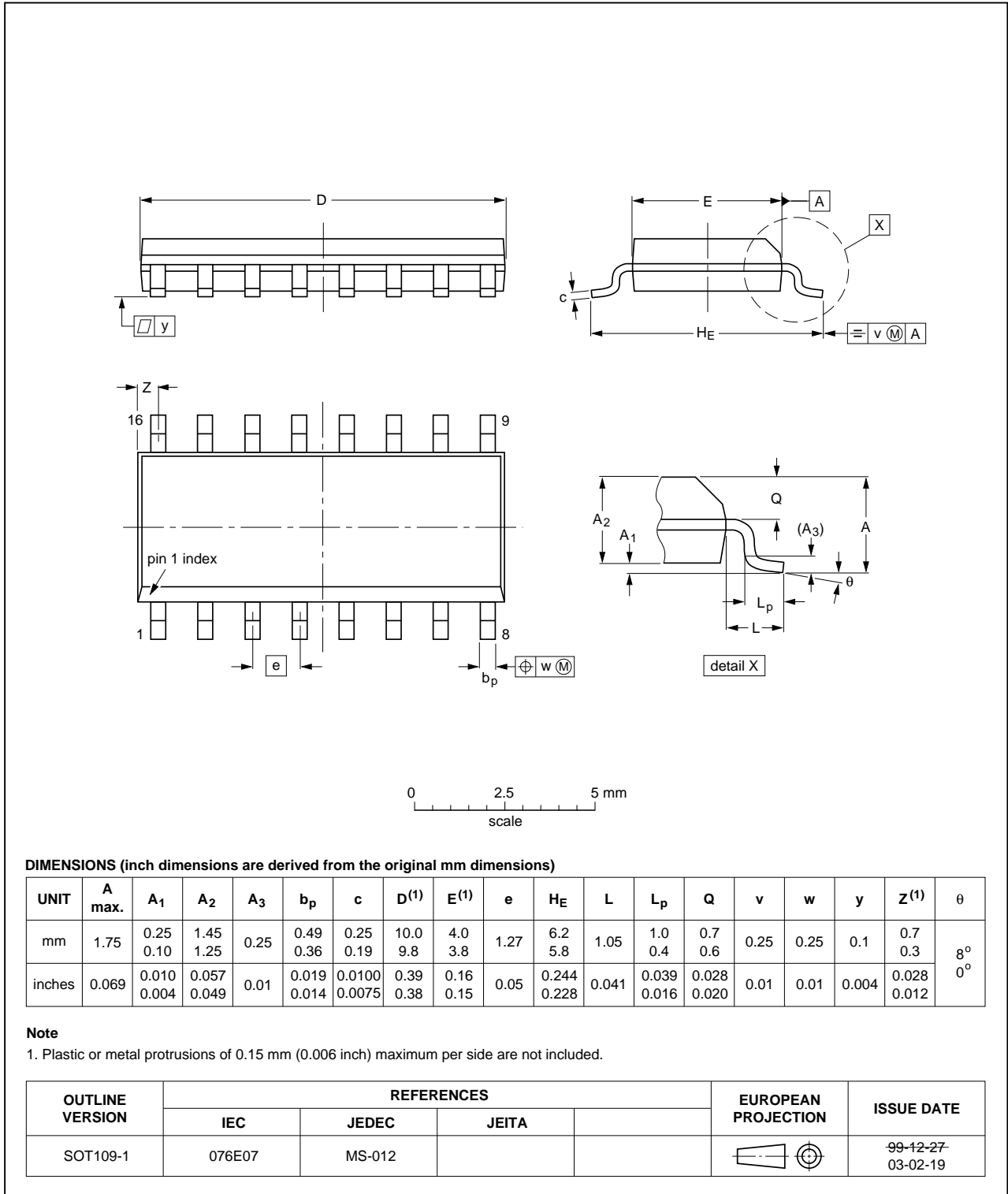


Fig 15. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

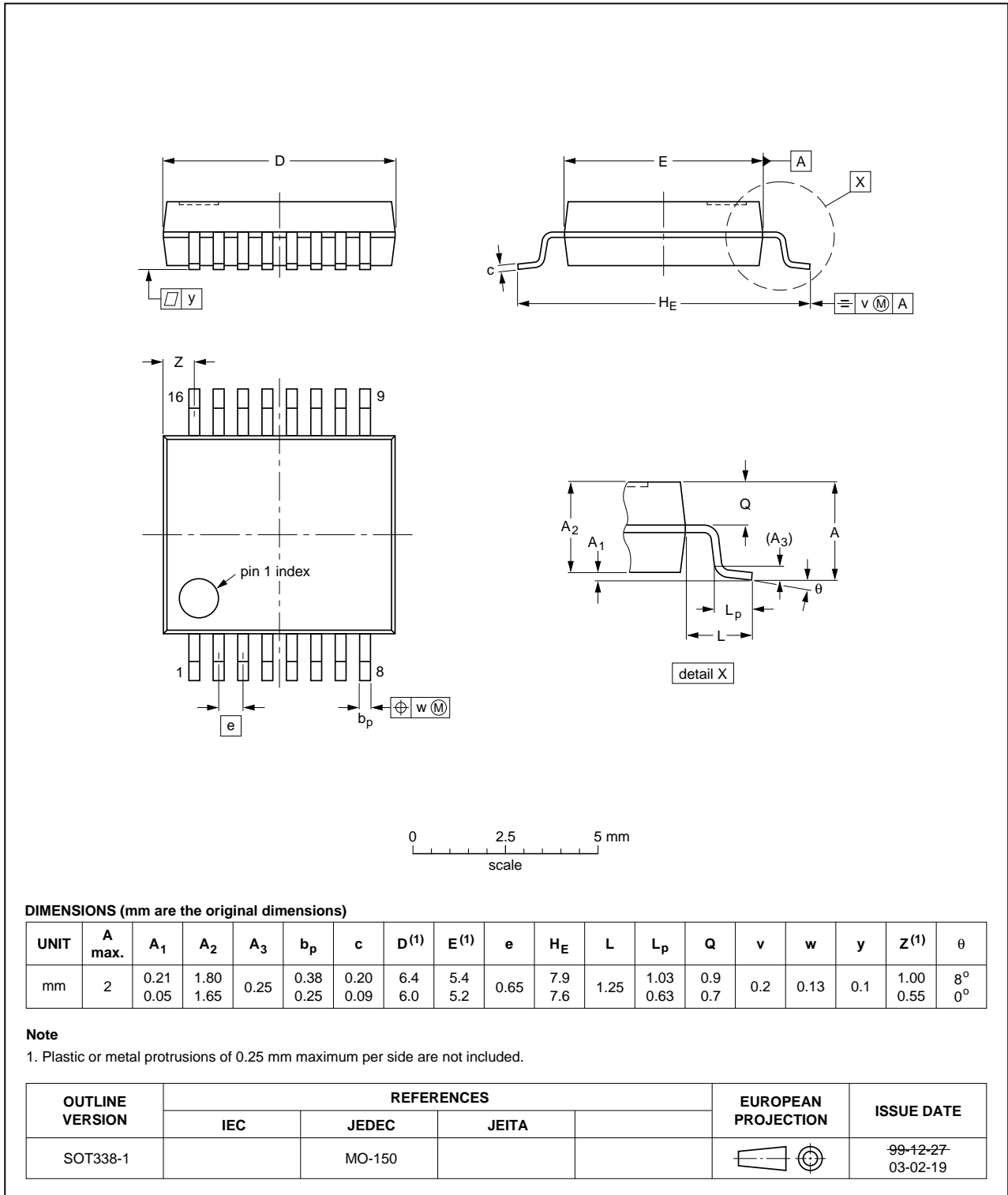


Fig 16. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

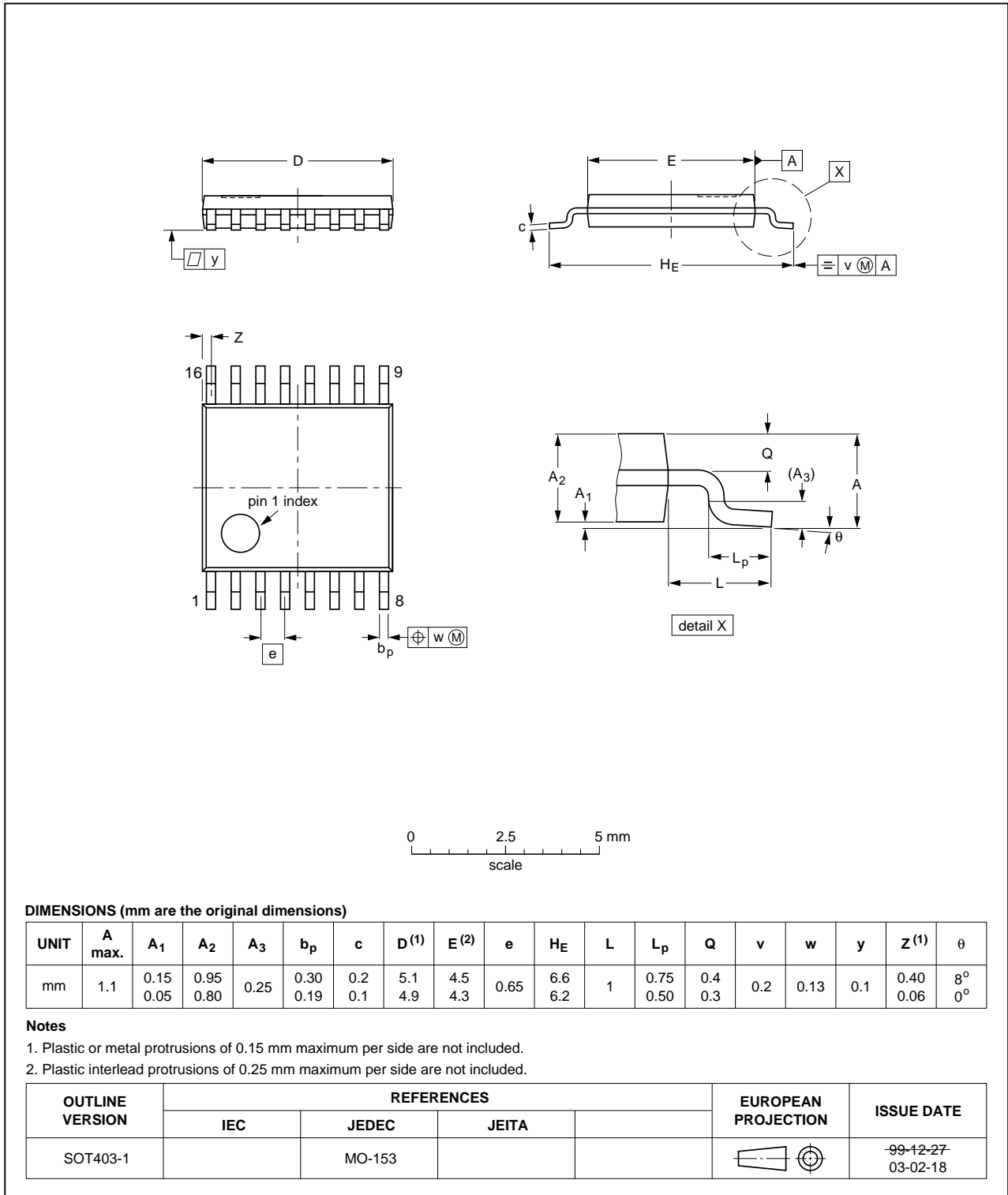


Fig 17. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

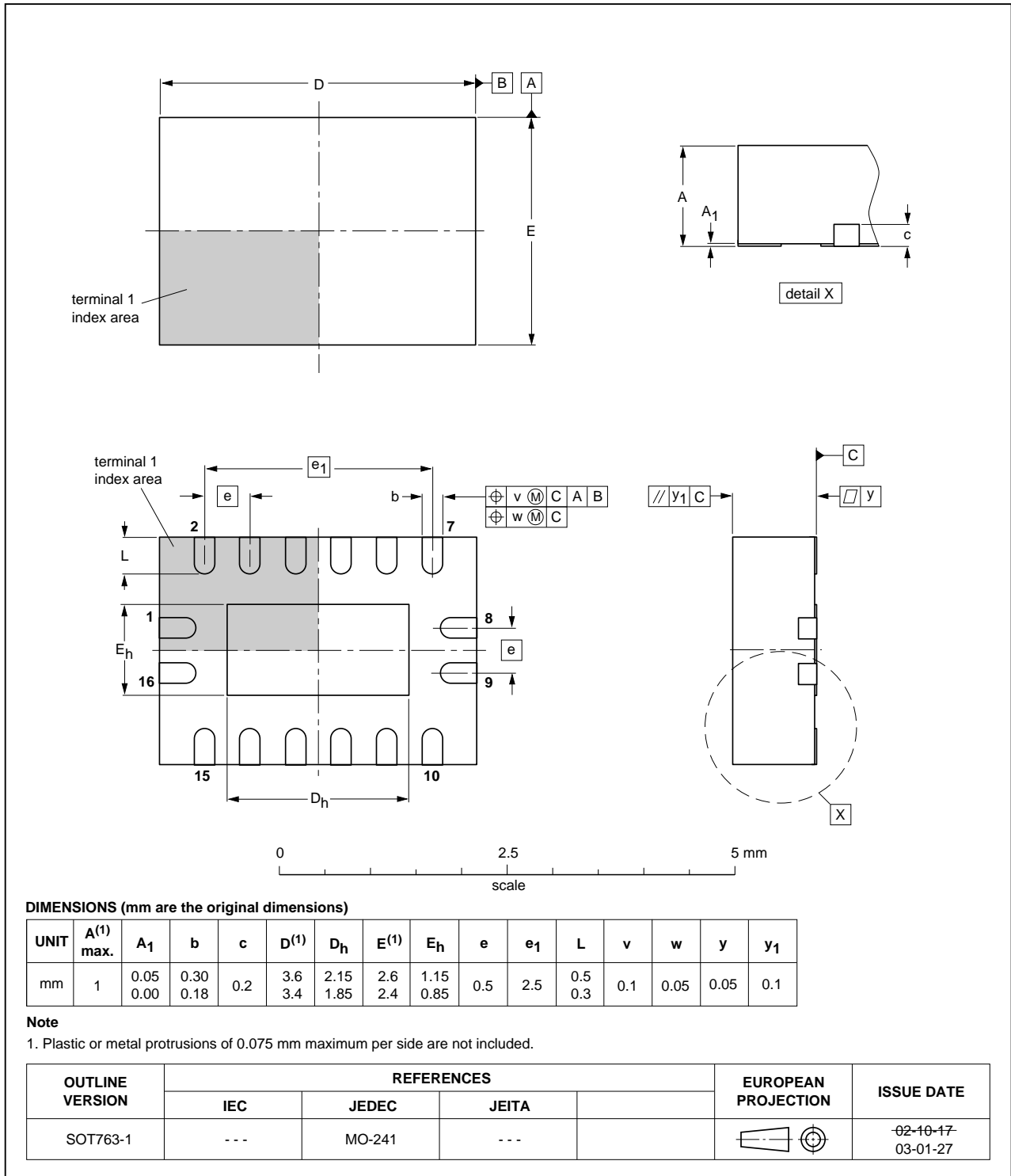


Fig 18. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC163 v.6	20121120	Product data sheet	-	74LVC163 v.5
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges. 			
74LVC163 v.5	20040505	Product specification	-	74LVC163 v.4
74LVC163 v.4	20030602	Product specification	-	74LVC163 v.3
74LVC163 v.3	20030509	Product specification	-	74LVC163 v.2
74LVC163 v.2	19980520	Product specification	-	74LVC163 v.1
74LVC163 v.1	19960823	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	5
5.1	Pinning	5
5.2	Pin description	5
6	Functional description	6
7	Limiting values	6
8	Recommended operating conditions	7
9	Static characteristics	7
10	Dynamic characteristics	8
11	AC waveforms	10
12	Package outline	13
13	Abbreviations	17
14	Revision history	17
15	Legal information	18
15.1	Data sheet status	18
15.2	Definitions	18
15.3	Disclaimers	18
15.4	Trademarks	19
16	Contact information	19
17	Contents	20

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