74LVC1G126

Bus buffer/line driver; 3-state

Rev. 14 — 15 March 2019

Product data sheet

1. General description

The 74LVC1G126 provides one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (OE). A LOW-level at pin OE causes the output to assume a high-impedance OFF-state.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- · High noise immunity
- · Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ±24 mA output drive (V_{CC} = 3.0 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- CMOS low power consumption
- Inputs accept voltages up to 5 V
- Latch-up performance exceeds 250 mA
- · Direct interface with TTL levels
- · Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



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3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G126GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G126GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
4LVC1G126GM -40 °C to +125 °C XSON6 plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm		SOT886		
74LVC1G126GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm	SOT891
74LVC1G126GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm	SOT1115
74LVC1G126GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm	SOT1202
74LVC1G126GX	-40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.35 mm	SOT1226

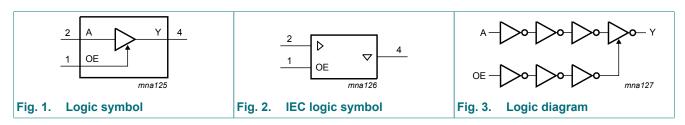
4. Marking

Table 2. Marking codes

Type number	Marking[1]
74LVC1G126GW	VN
74LVC1G126GV	V26
74LVC1G126GM	VN
74LVC1G126GF	VN
74LVC1G126GN	VN
74LVC1G126GS	VN
74LVC1G126GX	VN

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

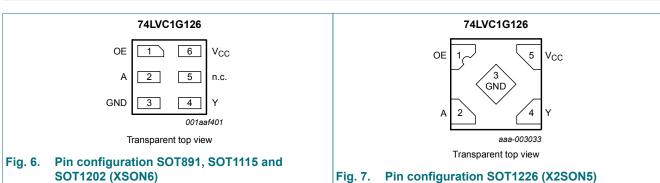


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6. Pinning information

6.1. Pinning





6.2. Pin description

Table 3. Pin description

Symbol	Pin	Pin			
	TSSOP5, SC-74A and X2SON5	XSON6			
OE	1	1	output enable input		
A	2	2	data input		
GND	3	3	ground (0 V)		
Υ	4	4	data output		
n.c.	-	5	not connected		
V _{CC}	5	6	supply voltage		

7. Functional description

Table 4. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care; \ Z = high-impedance \ OFF-state.$

Input	Output	
OE	A	Υ
Н	L	L
Н	Н	Н
L	X	Z

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
VI	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
Vo	output voltage	Active mode [1]	-0.5	V _{CC} + 0.5	V
		Power-down mode; V _{CC} = 0 V [1]	-0.5	+6.5	V
Io	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	250	mW
T _{stg}	storage temperature		-65	+150	°C

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.65	-	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	Active mode	0	-	V _{CC}	V
		V _{CC} = 0 V; Power-down mode	0	-	5.5	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

^[2] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K. For XSON6 and X2SON5 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

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10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T _{amb} = -2	10 °C to +85 °C					
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
	LOW-level input voltage LOW-level output voltage	V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_{O} = 100 μ A	-	-	0.1	V
		V _{CC} = 1.65 V; I _O = 4 mA	-	-	0.45	V
		V _{CC} = 2.3 V; I _O = 8 mA	-	-	0.3	V
		V _{CC} = 2.7 V; I _O = 12 mA	-	-	0.4	V
		V _{CC} = 3.0 V; I _O = 24 mA	-	-	0.55	V
		V _{CC} = 4.5 V; I _O = 32 mA	-	-	0.55	V
V _{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_{O} = -100 μA	V _{CC} - 0.1	-	-	V
		V _{CC} = 1.65 V; I _O = -4 mA	1.2	-	-	V
		V_{CC} = 2.3 V; I_{O} = -8 mA	1.9	-	-	V
		V _{CC} = 2.7 V; I _O = -12 mA	2.2	-	-	V
		V _{CC} = 3.0 V; I _O = -24 mA	2.3	-	-	V
		V _{CC} = 4.5 V; I _O = -32 mA	3.8	-	-	V
I _I	input leakage current	V _{CC} = 0 V to 5.5 V; V _I = 5.5 V or GND	-	±0.1	±1	μΑ
l _{OZ}	OFF-state output current	$V_{CC} = 3.6 \text{ V}; V_I = V_{IH} \text{ or } V_{IL};$ $V_O = 5.5 \text{ V or GND}$	-	±0.1	±2	μA
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 5.5 \text{ V}$	-	±0.1	±2	μA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	0.1	4	μA
ΔI _{CC}	additional supply current	per pin; V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	μΑ
Cı	input capacitance		-	5	-	pF

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T _{amb} = -4	0 °C to +125 °C					
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
Tamb = -40 ° VIH H VIL L° VOL H II in		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 2.3 V to 2.7 V V_{CC} = 2.7 V to 3.6 V V_{CC} = 4.5 V to 5.5 V V_{CC} = 1.65 V to 1.95 V V_{CC} = 2.3 V to 2.7 V V_{CC} = 2.7 V to 3.6 V V_{CC} = 4.5 V to 5.5 V V_{I} = V_{IH} or V_{IL} V_{CC} = 1.65 V to 5.5 V; I_{O} = 100 μA V_{CC} = 1.65 V; I_{O} = 4 mA V_{CC} = 2.3 V; I_{O} = 8 mA V_{CC} = 2.7 V; I_{O} = 12 mA V_{CC} = 3.0 V; I_{O} = 24 mA V_{CC} = 4.5 V; I_{O} = 32 mA V_{I} = V_{IH} or V_{IL} V_{CC} = 1.65 V to 5.5 V; I_{O} = 100 μA	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_{O} = 100 μ A	-	-	0.1	V
		V _{CC} = 1.65 V; I _O = 4 mA	-	-	0.70	V
		V _{CC} = 2.3 V; I _O = 8 mA	-	-	0.45	V
		V _{CC} = 2.7 V; I _O = 12 mA	-	-	0.60	V
		V _{CC} = 3.0 V; I _O = 24 mA	-	-	0.80	V
		V _{CC} = 4.5 V; I _O = 32 mA	-	-	0.80	V
V _{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_{O} = -100 μ A	V _{CC} - 0.1	-	-	V
		V _{CC} = 1.65 V; I _O = -4 mA	0.95	-	-	V
		V_{CC} = 2.3 V; I_{O} = -8 mA	1.7	-	-	V
		V _{CC} = 2.7 V; I _O = -12 mA	1.9	-	-	V
		V _{CC} = 3.0 V; I _O = -24 mA	2.0	-	-	V
		V_{CC} = 4.5 V; I_{O} = -32 mA	3.4	-	-	V
l _l	input leakage current	V _{CC} = 0 V to 5.5 V; V _I = 5.5 V or GND	-	-	±1	μΑ
I _{OZ}	OFF-state output current	$V_{CC} = 3.6 \text{ V}; V_{I} = V_{IH} \text{ or } V_{IL};$ $V_{O} = 5.5 \text{ V or GND}$	-	-	±2	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	-	±2	μΑ
I _{CC}	supply current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	-	4	μΑ
Δl _{CC}	additional supply current	per pin; V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	-	5 00	μΑ

^[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40	°C to +85	°C	-40 °C to	Unit	
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	A to Y; see Fig. 8 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3	8.0	1.0	10.5	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.1	5.5	0.5	7	ns
		V _{CC} = 2.7 V	0.5	2.3	5.5	0.5	7	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.0	4.5	0.5	6	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.7	4.0	0.5	5.5	ns
t _{en}	enable time	OE to Y; see Fig. 9 [3]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.2	9.4	1.0	12	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.2	6.6	0.5	8.5	ns
		V _{CC} = 2.7 V	0.5	2.4	6.6	0.5	8.5	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.1	5.3	0.5	7	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.6	5.0	0.5	6.5	ns
t _{dis}	disable time	OE to Y; see Fig. 9 [4]						
		V _{CC} = 1.65 V to 1.95 V	1.0	4.3	9.2	1.0	12	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.7	5.5	0.5	7	ns
		V _{CC} = 2.7 V	0.5	3.4	5.5	0.5	7	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	3.0	5.5	0.5	7	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	2.2	4.2	0.5	5.5	ns
C _{PD}	power dissipation	per buffer; $V_I = GND$ to V_{CC} [5]						
	capacitance	output enabled	-	25	-	-	-	pF
		output disabled	-	6	-	-	-	pF

^[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

 $P_D = C_{PD} x V_{CC}^2 x f_i x N + \sum (C_L x V_{CC}^2 x f_o)$ where:

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

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^[2] t_{pd} is the same as t_{PLH} and t_{PHL}

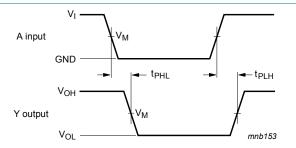
^[3] t_{en} is the same as t_{PZH} and t_{PZL}

^[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}

^[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

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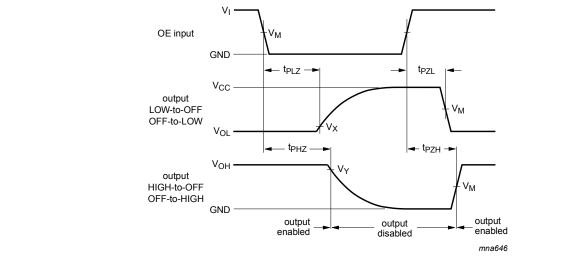
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Input A to output Y propagation delay times



Measurement points are given in <u>Table 9</u>.

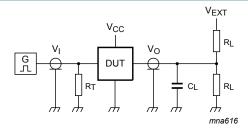
 $\ensuremath{V_{\text{OL}}}$ and $\ensuremath{V_{\text{OH}}}$ are typical output voltage levels that occur with the output load.

Fig. 9. 3-state enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output	Output						
V _{CC}	V _M	V _M	V _X	V _Y					
1.65 V to 1.95 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V					
2.3 V to 2.7 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V					
2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V					
3.0 V to 3.6 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V					
4.5 V to 5.5 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.3 V	V _{OH} - 0.3 V					

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Test data is given in Table 10.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig. 10. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	pply voltage Input		Load	Load		V _{EXT}		
V _{CC}	VI	t _r , t _f	CL	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2V _{CC}	
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	2V _{CC}	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V	
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	2V _{CC}	

Bus buffer/line driver; 3-state

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm SOT353-1 = v M A ⊕ w M detail X 3 mm scale **DIMENSIONS (mm are the original dimensions)** A_2 Α3 $D^{(1)}$ $E^{(1)}$ e₁ L $Z^{(1)}$ UNIT H_{E} θ Lp max 0.30 0.25 1.35 0.60 mm 1.1 0.15 0.65 1.3 0.425 0.3 0.1 0.1

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

	OUTLINE		REFERENCES			EUROPEAN	ISSUE DATE
	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT353-1		MO-203	SC-88A			-00-09-01 03-02-19

Fig. 11. Package outline SOT353-1 (TSSOP5)

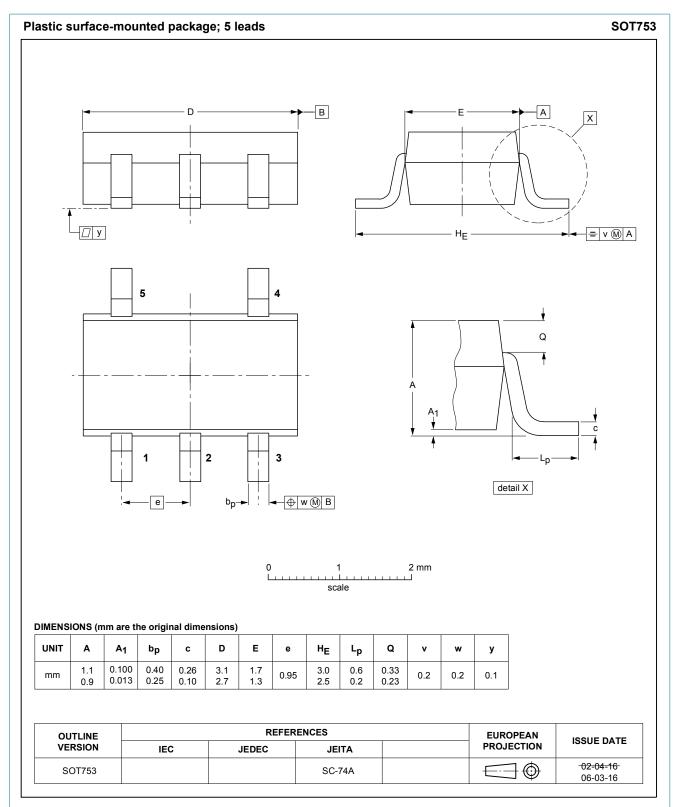


Fig. 12. Package outline SOT753 (SC-74A)

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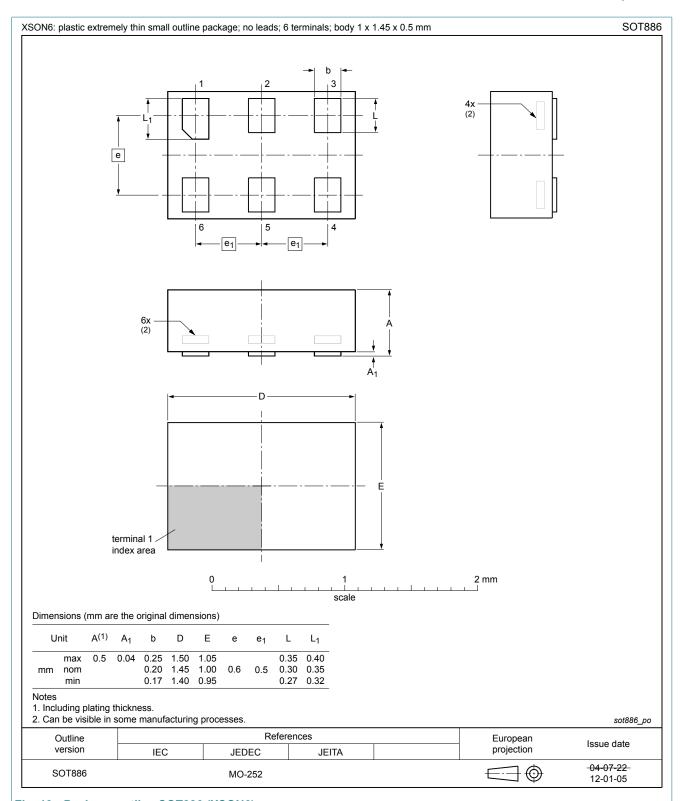


Fig. 13. Package outline SOT886 (XSON6)

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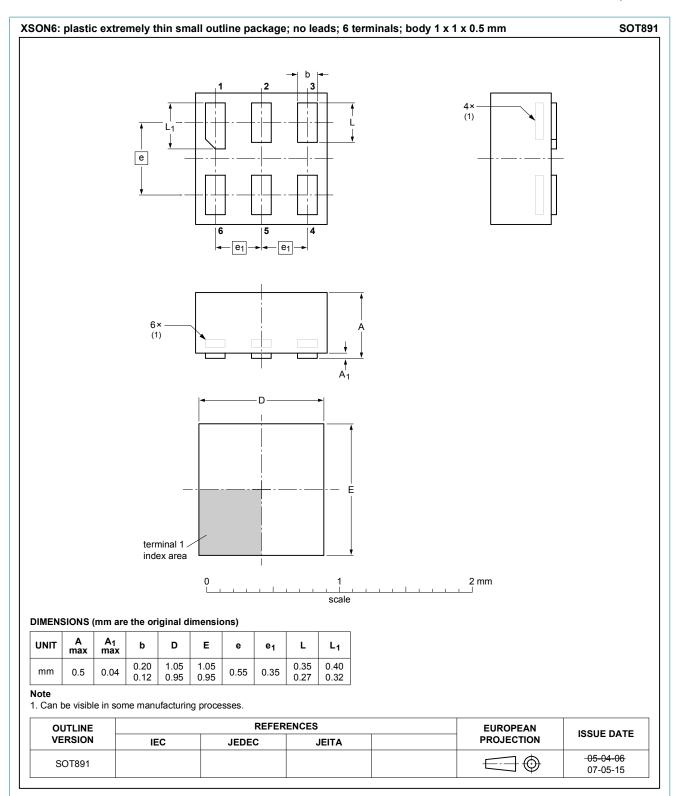


Fig. 14. Package outline SOT891 (XSON6)

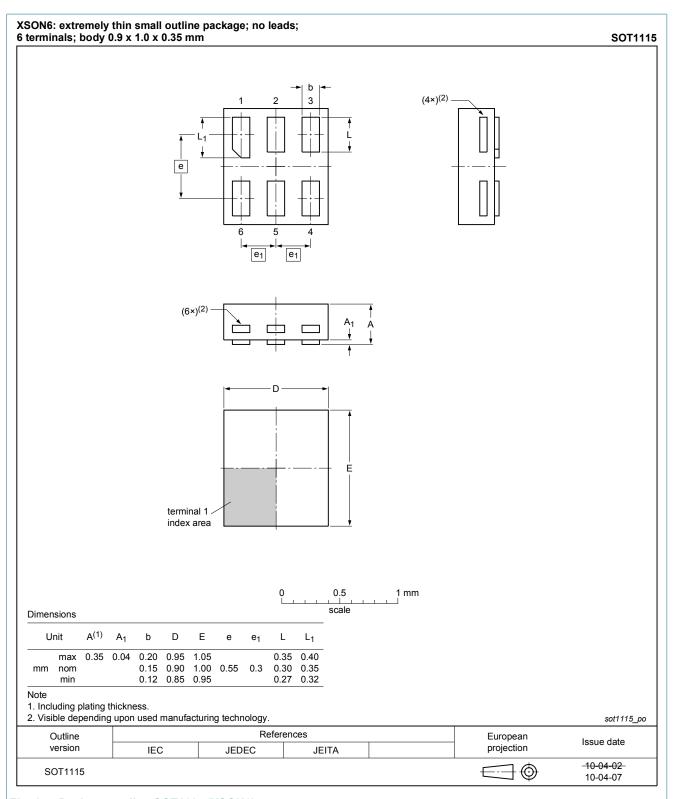


Fig. 15. Package outline SOT1115 (XSON6)

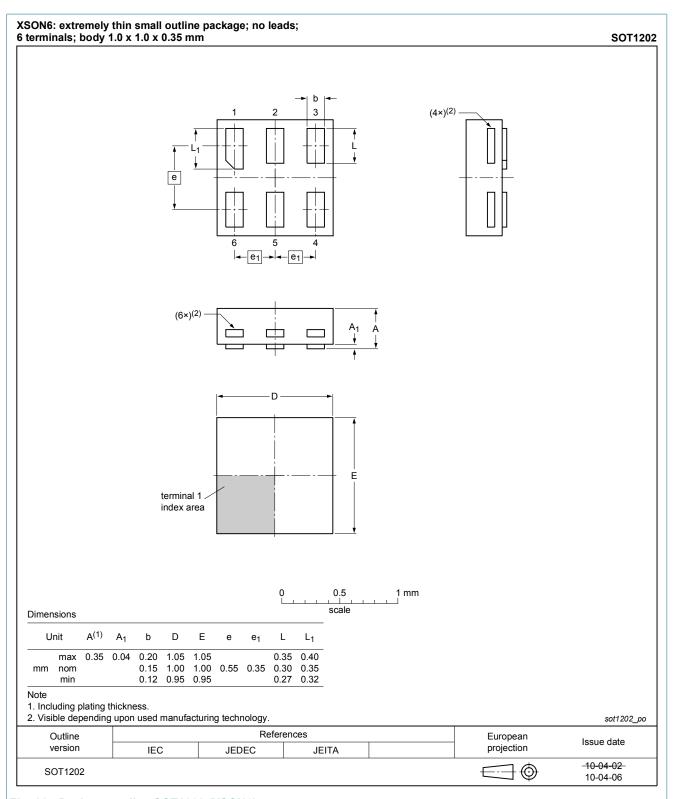


Fig. 16. Package outline SOT1202 (XSON6)

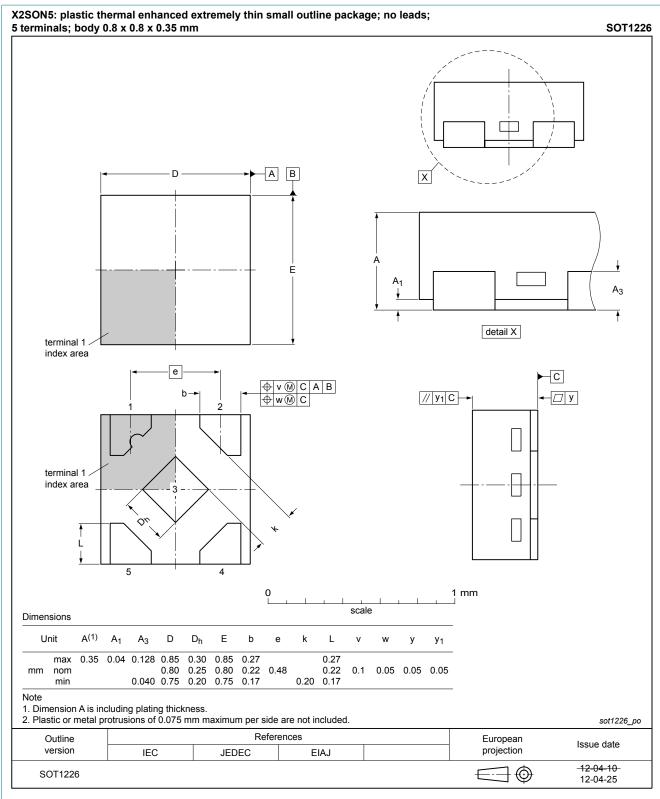


Fig. 17. Package outline SOT1226 (X2SON5)

Bus buffer/line driver; 3-state

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74LVC1G126 v.14	20190315	Product data sheet	-	74LVC1G126 v.13	
Modifications:	Nexperia.	f this data sheet has been rede ave been adapted to the new c			
74LVC1G126 v.13	20161202	Product data sheet	-	74LVC1G126 v.12	
Modifications:	<u>Table 7</u> : The maximum limits for leakage current and supply current have changed.				
74LVC1G126 v.12	20120702	Product data sheet	-	74LVC1G126 v.11	
Modifications:	 Added type number 74LVC1G126GX (SOT1226) Package outline drawing of SOT886 (Fig. 13) modified. 				
74LVC1G126 v.11	20111208	Product data sheet	-	74LVC1G126 v.10	
Modifications:	 Legal pages 	updated.			
74LVC1G126 v.10	20101229	Product data sheet	-	74LVC1G126 v.9	
74LVC1G126 v.9	20100825	Product data sheet	-	74LVC1G126 v.8	
74LVC1G126 v.8	20090409	Product data sheet	-	74LVC1G126 v.7	
74LVC1G126 v.7	20070830	Product data sheet	-	74LVC1G126 v.6	
74LVC1G126 v.6	20061009	Product data sheet	-	74LVC1G126 v.5	
74LVC1G126 v.5	20040921	Product specification	-	74LVC1G126 v.4	
74LVC1G126 v.4	20021002	Product specification	-	74LVC1G126 v.3	
74LVC1G126 v.3	20020528	Product specification	-	74LVC1G126 v.2	
74LVC1G126 v.2	20010406	Preliminary specification	-	74LVC1G126 v.1	
74LVC1G126 v.1	20001222	Preliminary specification	-	-	

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Bus buffer/line driver; 3-state

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