74LVT244A-Q100; 74LVTH244A-Q100

3.3 V octal buffer/line driver; 3-state

Rev. 2 — 24 August 2020

Product data sheet

1. General description

The 74LVT244A-Q100; 74LVTH244A-Q100 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables $(1\overline{OE}, 2\overline{OE})$, each controlling four of the 3-state outputs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
 - Specified from -40 °C to +85 °C
- · Octal bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
 - JESD78 Class II exceeds 500 mA
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

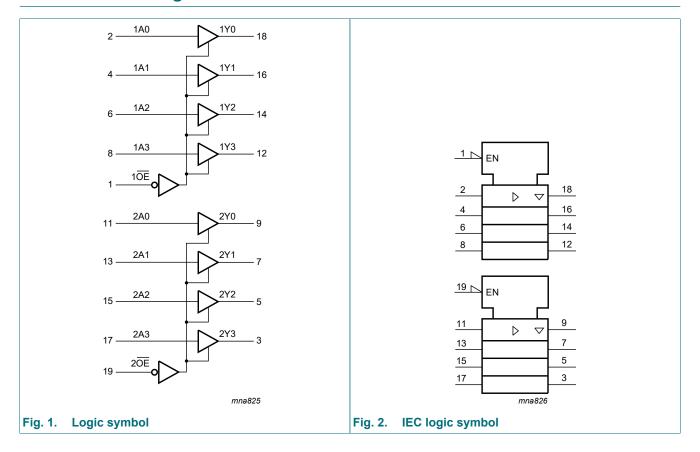
3. Ordering information

Table 1. Ordering information

Type number	Package				
	Temperature range	Name	Description	Version	
74LVT244AD-Q100	T244AD-Q100 -40 °C to +85 °C SO20		plastic small outline package; 20 leads;	SOT163-1	
74LVTH244AD-Q100			body width 7.5 mm		
74LVT244APW-Q100	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package;	SOT360-1	
74LVTH244APW-Q100			20 leads; body width 4.4 mm		
74LVT244ABQ-Q100	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal	SOT764-1	
74LVTH244ABQ-Q100			enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm		



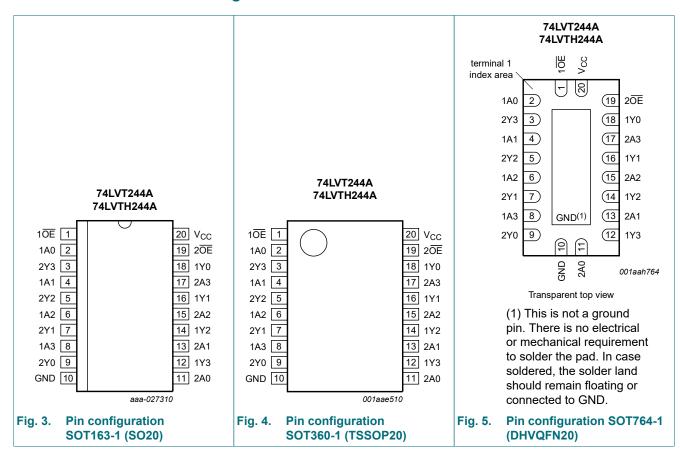
4. Functional diagram



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5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Table 2. Fill description		
Symbol	Pin	Description
1 OE , 2 OE	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table

 $H = HIGH \text{ voltage level}; L = LOW \text{ voltage level}; X = don't care; Z = high-impedance OFF-state.}$

	Input	Output		
nOE	nAn	nYn		
L	L	L		
L	Н	Н		
Н	X	Z		

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+4.6	V
VI	input voltage		[1]	-0.5	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
I _{OK}	output clamping current	V _O < 0 V		-50	-	mA
Io	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-64	-	mA
T _{stg}	storage temperature			-65	+150	°C
Tj	junction temperature		[2]	-	150	°C
P _{tot}	total power dissipation	T _{amb} = -40 to +85 °C	[3]	-	500	mW

^[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
VI	input voltage		0	-	5.5	V
I _{OH}	HIGH-level output current		-32	-	-	mA
I _{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f _i ≥ 1 kHz	-	-	64	mA
T _{amb}	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

^[3] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C. For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C. For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		T _{amb} = -40 °C to +85 °C				
				Min	Typ[1]	Max		
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA		-1.2	-0.9	-	V	
V _{IH}	HIGH-level input voltage			2.0	-	-	V	
V _{IL}	LOW-level input voltage			-	-	0.8	V	
V _{OH}	HIGH-level output	V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 μA		V _{CC} - 0.2	V _{CC} - 0.1	-	V	
	voltage	V _{CC} = 2.7 V to 3.6 V; I _{OH} = -8 mA		2.4	2.5	-	V	
		V _{CC} = 3.0 V; I _{OH} = -32 mA		2.0	2.2	-	V	
V _{OL}	LOW-level output	V _{CC} = 2.7 V; I _{OL} = 100 μA		-	0.1	0.2	V	
	voltage	V _{CC} = 2.7 V; I _{OL} = 24 mA		-	0.3	0.5	V	
		V _{CC} = 3.0 V; I _{OL} = 16 mA		-	0.25	0.4	V	
		V _{CC} = 3.0 V; I _{OL} = 32 mA		-	0.3	0.5	V	
		V _{CC} = 3.0 V; I _{OL} = 64 mA		-	0.4	0.55	V	
l _l	input leakage current	all input pins						
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V		-	0.1	10	μA	
		control pins						
		V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	±0.1	±1	μΑ	
		data pins	[2]					
		V _{CC} = 3.6 V; V _I = V _{CC}		-	0.1	1	μΑ	
		V _{CC} = 3.6 V; V _I = 0 V		-5	-1	-	μΑ	
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 0 \text{ V to } 4.5 \text{ V}$		-	1	±100	μΑ	
I _{BHL}	bus hold LOW current	V _{CC} = 3 V; V _I = 0.8 V		75	150	-	μA	
Івнн	bus hold HIGH current	V _{CC} = 3 V; V _I = 2.0 V		-	-150	-75	μΑ	
I _{BHLO}	bus hold LOW overdrive current	nAn input; $V_{CC} = 3.6 \text{ V}$; $V_{I} = 0 \text{ V}$ to 3.6 V	[3]	500	-	-	μΑ	
Івнно	bus hold HIGH overdrive current	nAn input; $V_{CC} = 3.6 \text{ V}$; $V_{I} = 0 \text{ V}$ to 3.6 V	[3]	-	-	-500	μΑ	
I _{EX}	external current	nYn output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5 \text{ V}$; $V_{CC} = 3.0 \text{ V}$		-	60	125	μΑ	
I _{O(pu/pd)}	power-up/power-down output current	$V_{CC} \le 1.2 \text{ V}; V_O = 0.5 \text{ V to } V_{CC};$ $V_I = \text{GND or } V_{CC}; \text{n} \overline{\text{OE}} = \text{don't care}$	[4]	-	±1	±100	μA	
loz	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL}						
		V _O = 3.0 V		-	1	5	μΑ	
		V _O = 0.5 V		-5	-1	-	μΑ	
lcc	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC} ; I_O = 0 A						
		output HIGH		-	0.13	0.19	mA	
		output LOW		-	3	12	mA	
		outputs disabled	[5]	-	0.13	0.19	mA	
ΔI _{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; one input at V_{CC} - 0.6 V and other inputs at V_{CC} or GND	[6]	-	0.1	0.2	mA	
Cı	input capacitance	V _I = 0 V or 3.0 V		-	4	-	pF	

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C				
			Min	Typ[1]	Max		
Co	output capacitance	outputs disabled; V _O = 0 V or 3.0 V	-	8	-	pF	

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] Unused pins at V_{CC} or GND.
- [3] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
 - From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.
- [5] I_{CC} is measured with outputs pulled to V_{CC} or GND.
- [6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	T _{am}	_b = -40 °C to +8	35 °C	Unit
			Min	Typ[1]	Max	
t _{PLH}	LOW to HIGH	nAn to nYn; see Fig. 6				
	propagation delay	V _{CC} = 2.7 V	-	-	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1	2.5	4.1	ns
t _{PHL}	HIGH to LOW	nAn to nYn; see Fig. 6				
	propagation delay	V _{CC} = 2.7 V	-	-	5.1	ns
		V _{CC} = 3.0 V to 3.6 V	1	2.6	4.1	ns
t _{PZH}	OFF-state to HIGH	nOE to nYn; see Fig. 7				
	propagation delay	V _{CC} = 2.7 V	-	-	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	1	3.2	5.2	ns
t _{PZL}	OFF-state to LOW	nOE to nYn; see Fig. 7				
	propagation delay	V _{CC} = 2.7 V	-	-	6.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.1	3.1	5.2	ns
t _{PHZ}	HIGH to OFF-state	nOE to nYn; see Fig. 7				
	propagation delay	V _{CC} = 2.7 V	-	-	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.9	3.3	5.6	ns
t _{PLZ}	LOW to OFF-state	nOE to nYn; see Fig. 7				
	propagation delay	V _{CC} = 2.7 V	-	-	5.6	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	3.3	5.1	ns

^[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

10.1. Waveforms and test circuit

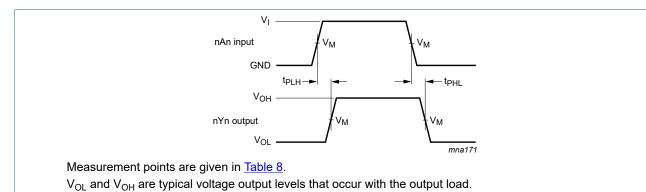


Fig. 6. Input (nAn) to output (nYn) propagation delays

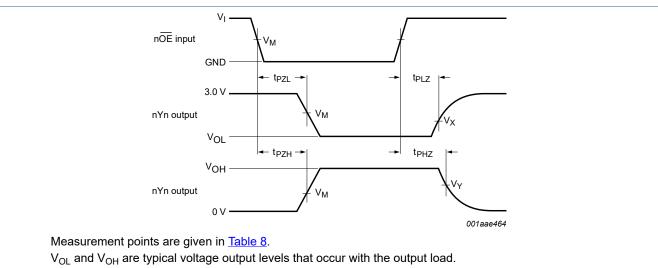
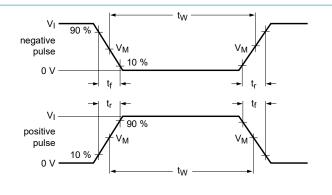


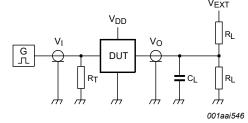
Fig. 7. 3-state output enable and disable times

Table 8. Measurement points

Input	Output	Putput							
V_{M}	V _M	V_{Y}							
1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V						

Product data sheet





Test data is given in Table 9.

Definitions test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 V_{EXT} = Test voltage for switching times.

Fig. 8. Test circuit for measuring switching times

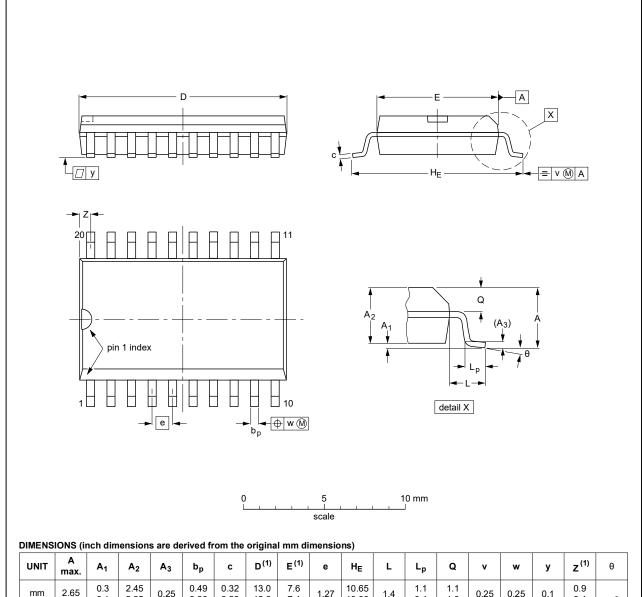
Table 9. Test data

Input				Load		V _{EXT}			
V _I f _i t		t _W	t _r , t _f	CL	R_L	t _{PHZ} , t _{PZH}	t _{PLZ} , t _{PZL}	t _{PLH} , t _{PHL}	
2.7 V ≤ 10 MHz 500 r		500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open	

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

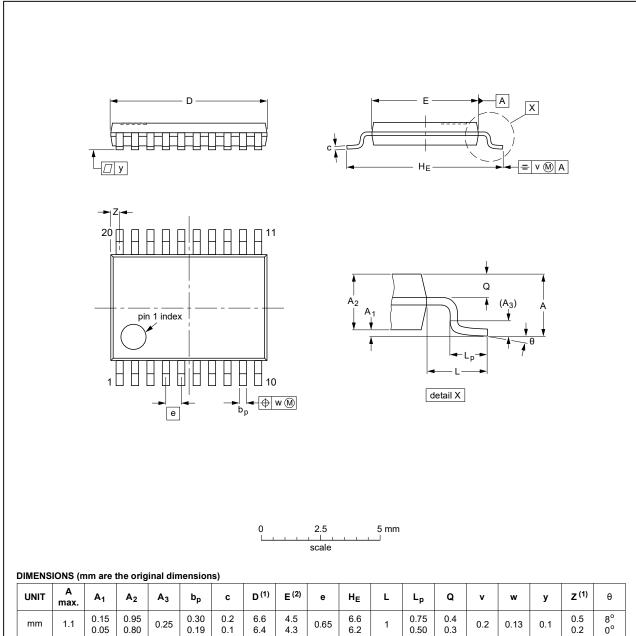
	OUTLINE		REFER	EUROPEAN	ISSUE DATE		
	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT163-1	075E04	MS-013				99-12-27 03-02-19

Fig. 9. Package outline SOT163-1 (SO20)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



UN	IIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
m	m	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE				
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE		
SOT360-1		MO-153				99-12-27 03-02-19		

Fig. 10. Package outline SOT360-1 (TSSOP20)

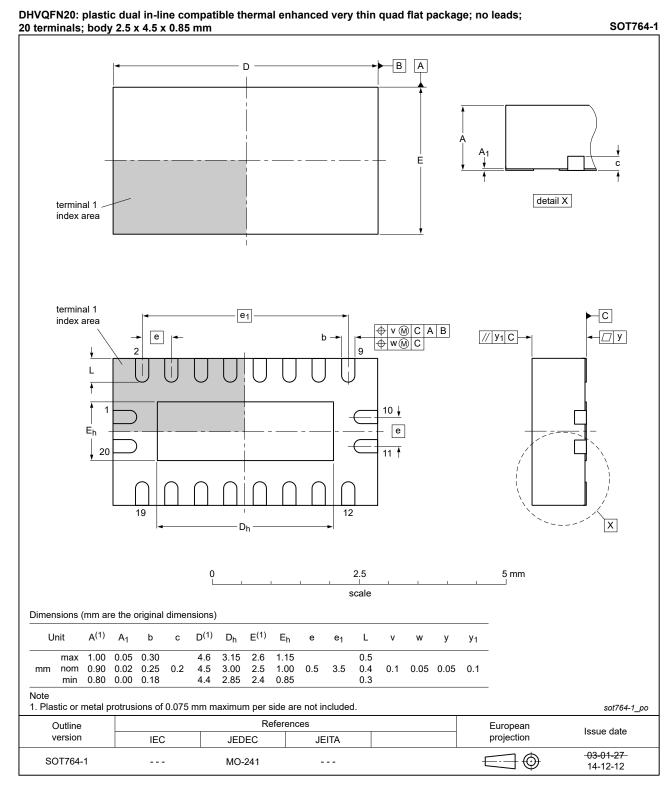


Fig. 11. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description						
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor						
DUT	Device Under Test						
ESD	ElectroStatic Discharge						
НВМ	Human Body Model						
MIL	Military						
MM	Machine Model						
TTL	Transistor-Transistor Logic						

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74LVT_LVTH244A_Q100 v.2	20200824	Product data sheet	-	74LVT_LVTH244A_Q100 v.1				
Modifications:	 Modifications: The format of this data sheet has been redesigned to comply with the identity guidel of Nexperia. 							
	 Legal texts have been adapted to the new company name where appropriate. 							
	• <u>Section 2</u> updated.							
	 <u>Table 4</u>: Derating values for P_{tot} total power dissipation have been updated 							
	<u>Table 6</u> : conditions for bushold overdrive current corrected.							
	(FN20) updated.							
74LVT_LVTH244A_Q100 v.1	20130422	Product specification	-	-				

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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