

74LVC8T245; 74LVCH8T245

8-bit dual supply translating transceiver; 3-state

Rev. 3 — 12 December 2011

Product data sheet

1. General description

The 74LVC8T245; 74LVCH8T245 are 8-bit dual supply translating transceivers with 3-state outputs that enable bidirectional level translation. They feature two data input-output ports (pins An and Bn), a direction control input (DIR), an output enable input (\overline{OE}) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2 V and 5.5 V making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An, \overline{OE} and DIR are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input (\overline{OE}) can be used to disable the outputs so the buses are effectively isolated.

The devices are fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A port and B port are in the high-impedance OFF-state.

Active bus hold circuitry in the 74LVCH8T245 holds unused or floating data inputs at a valid logic level.

2. Features and benefits

- Wide supply voltage range:
 - ◆ $V_{CC(A)}$: 1.2 V to 5.5 V
 - ◆ $V_{CC(B)}$: 1.2 V to 5.5 V
- High noise immunity
- Complies with JEDEC standards:
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8C (2.7 V to 3.6 V)
 - ◆ JESD36 (4.5 V to 5.5 V)
- ESD protection:
 - ◆ HBM JESD22-A114F Class 3A exceeds 4000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Maximum data rates:
 - ◆ 420 Mbps (3.3 V to 5.0 V translation)
 - ◆ 210 Mbps (translate to 3.3 V)
 - ◆ 140 Mbps (translate to 2.5 V)
 - ◆ 75 Mbps (translate to 1.8 V)



- ◆ 60 Mbps (translate to 1.5 V)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- ±24 mA output drive ($V_{CC} = 3.0\text{ V}$)
- Inputs accept voltages up to 5.5 V
- Low power consumption: 30 μA maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC8T245PW 74LVCH8T245PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74LVC8T245BQ 74LVCH8T245BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body $3.5 \times 5.5 \times 0.85\text{ mm}$	SOT815-1

4. Functional diagram

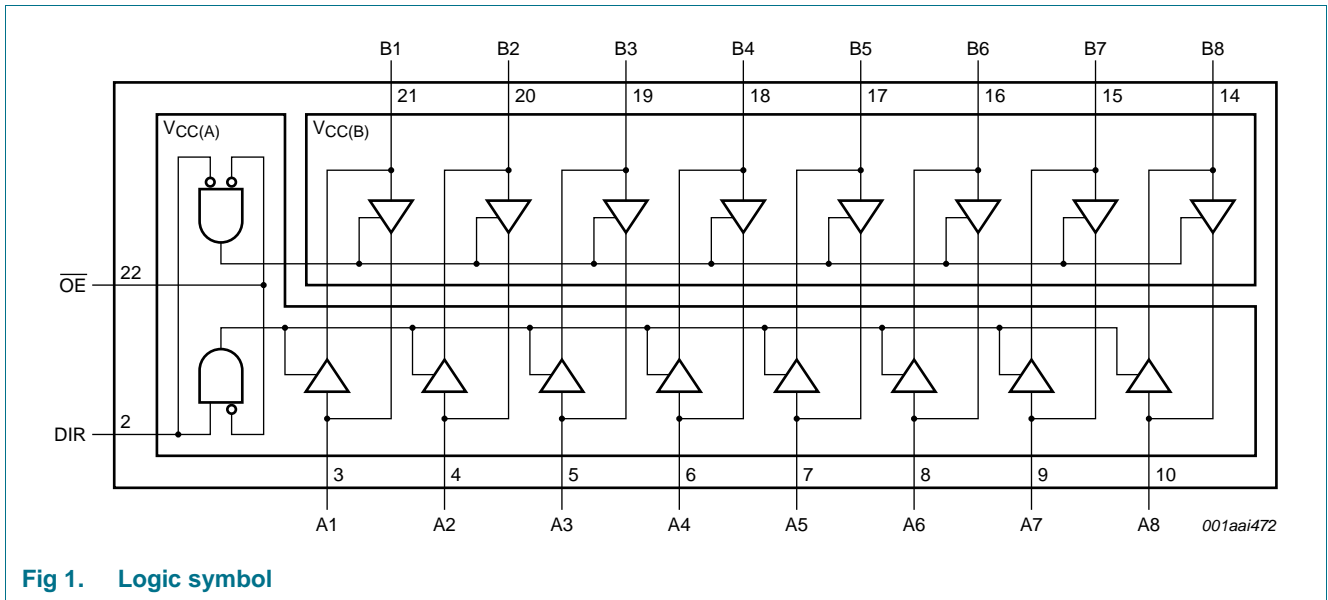


Fig 1. Logic symbol

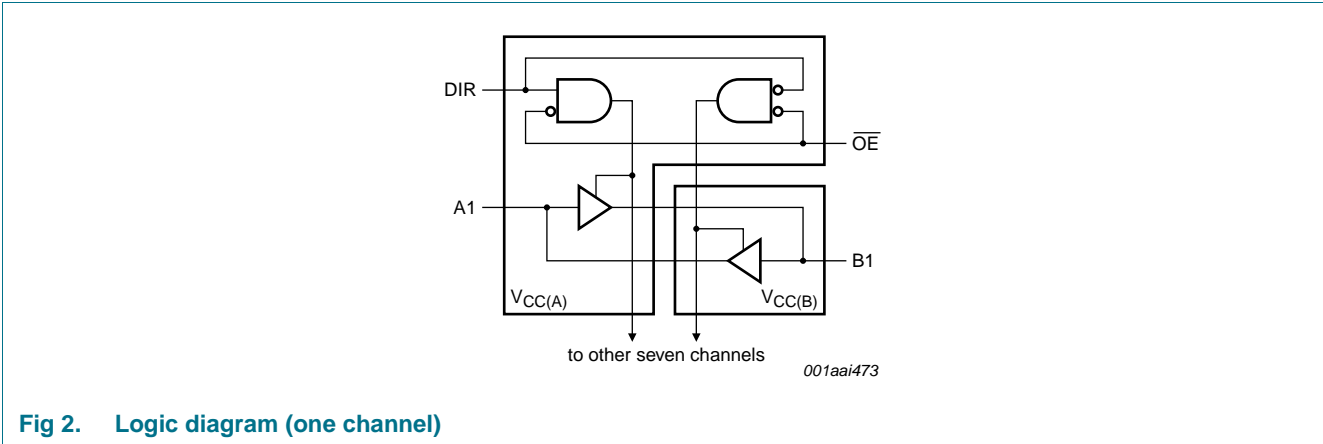


Fig 2. Logic diagram (one channel)

5. Pinning information

5.1 Pinning

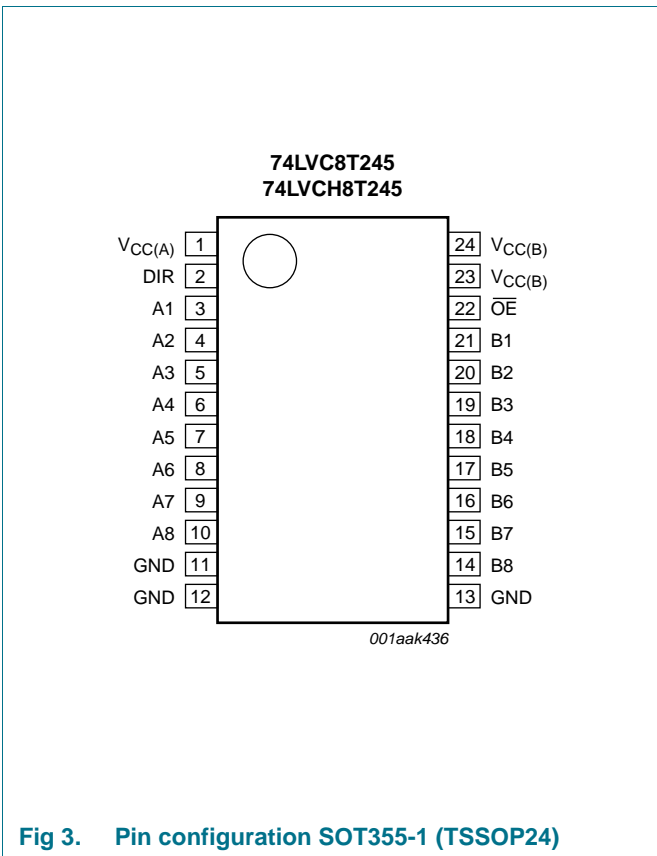


Fig 3. Pin configuration SOT355-1 (TSSOP24)

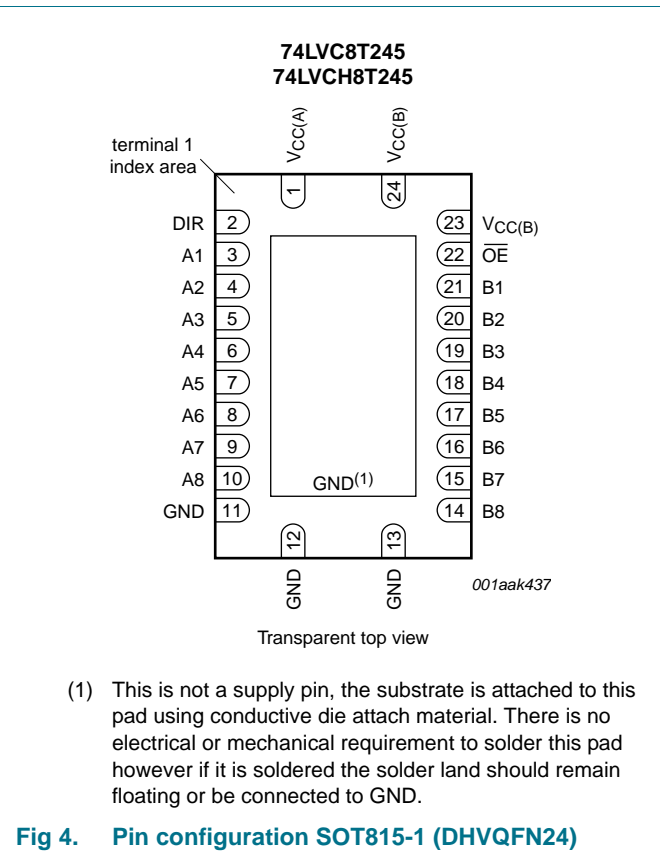


Fig 4. Pin configuration SOT815-1 (DHVQFN24)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A (An inputs/outputs, \overline{OE} and DIR inputs are referenced to $V_{CC(A)}$)
DIR	2	direction control
A1 to A8	3, 4, 5, 6, 7, 8, 9, 10	data input or output
GND ^[1]	11	ground (0 V)
GND ^[1]	12	ground (0 V)
GND ^[1]	13	ground (0 V)
B1 to B8	21, 20, 19, 18, 17, 16, 15, 14	data input or output
\overline{OE}	22	output enable input (active LOW)
$V_{CC(B)}$	23	supply voltage B (Bn inputs/outputs are referenced to $V_{CC(B)}$)
$V_{CC(B)}$	24	supply voltage B (Bn inputs/outputs are referenced to $V_{CC(B)}$)

[1] All GND pins must be connected to ground (0 V).

6. Functional description

Table 3. Function table^[1]

Supply voltage	Input		Input/output ^[3]	
	\overline{OE} ^[2]	DIR ^[2]	An ^[2]	Bn ^[2]
$V_{CC(A)}, V_{CC(B)}$				
1.2 V to 5.5 V	L	L	An = Bn	input
1.2 V to 5.5 V	L	H	input	Bn = An
1.2 V to 5.5 V	H	X	Z	Z
GND ^[3]	X	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The An inputs/outputs, DIR and \overline{OE} input circuit is referenced to $V_{CC(A)}$; The Bn inputs/outputs circuit is referenced to $V_{CC(B)}$.

[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		^[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode	^{[1][2][3]} -0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode	^[1] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CCO}	^[2] -	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin	-	100	mA

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
I_{GND}	ground current	per GND pin	-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$	[4] -	500	mW

- [1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] V_{CCO} is the supply voltage associated with the output port.
- [3] $V_{CCO} + 0.5\text{ V}$ should not exceed 6.5 V.
- [4] For TSSOP24 package: P_{tot} derates linearly at 5.5 mW/K above 60 °C.
For DHVQFN24 package: P_{tot} derates linearly at 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.2	5.5	V
$V_{CC(B)}$	supply voltage B		1.2	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	[1] 0	V_{CCO}	V
		Suspend or 3-state mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 1.2\text{ V}$	[2] -	20	ns/V
		$V_{CCI} = 1.4\text{ V to }1.95\text{ V}$	-	20	ns/V
		$V_{CCI} = 2.3\text{ V to }2.7\text{ V}$	-	20	ns/V
		$V_{CCI} = 3\text{ V to }3.6\text{ V}$	-	10	ns/V
		$V_{CCI} = 4.5\text{ V to }5.5\text{ V}$	-	5	ns/V

- [1] V_{CCO} is the supply voltage associated with the output port.
- [2] V_{CCI} is the supply voltage associated with the input port.

9. Static characteristics

Table 6. Typical static characteristics at $T_{amb} = 25\text{ °C}$

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}	[1]			
		$I_O = -3\text{ mA}; V_{CCO} = 1.2\text{ V}$	-	1.09	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 3\text{ mA}; V_{CCO} = 1.2\text{ V}$	[1] -	0.07	-	V
I_I	input leakage current	DIR, \overline{OE} input; $V_I = 0\text{ V to }5.5\text{ V}; V_{CCI} = 1.2\text{ V to }5.5\text{ V}$	[2] -	-	± 1	μA
I_{BHL}	bus hold LOW current	A or B port; $V_I = 0.42\text{ V}; V_{CCI} = 1.2\text{ V}$	[2] -	19	-	μA
I_{BHH}	bus hold HIGH current	A or B port; $V_I = 0.78\text{ V}; V_{CCI} = 1.2\text{ V}$	[2] -	-19	-	μA

Table 6. Typical static characteristics at $T_{amb} = 25\text{ }^{\circ}\text{C}$...continued
 At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BHLO}	bus hold LOW overdrive current	A or B port; $V_{CCI} = 1.2\text{ V}$	[2][3] -	19	-	μA
I_{BHHO}	bus hold HIGH overdrive current	A or B port; $V_{CCI} = 1.2\text{ V}$	[2][3] -	-19	-	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\text{ V}$ or V_{CCO} ; $V_{CCO} = 1.2\text{ V}$ to 5.5 V	[1] -	-	± 1	μA
		suspend mode A port; $V_O = 0\text{ V}$ or V_{CCO} ; $V_{CC(A)} = 5.5\text{ V}$; $V_{CC(B)} = 0\text{ V}$	[1] -	-	± 1	μA
		suspend mode B port; $V_O = 0\text{ V}$ or V_{CCO} ; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 5.5\text{ V}$	[1] -	-	± 1	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\text{ V}$ to 5.5 V ; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 1.2\text{ V}$ to 5.5 V	-	-	± 1	μA
		B port; V_I or $V_O = 0\text{ V}$ to 5.5 V ; $V_{CC(B)} = 0\text{ V}$; $V_{CC(A)} = 1.2\text{ V}$ to 5.5 V	-	-	± 1	μA
C_I	input capacitance	DIR, $\overline{\text{OE}}$ input; $V_I = 0\text{ V}$ or 3.3 V ; $V_{CC(A)} = 3.3\text{ V}$	-	3	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3\text{ V}$ or 0 V ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	6.5	-	pF

- [1] V_{CCO} is the supply voltage associated with the output port.
- [2] V_{CCI} is the supply voltage associated with the data input port.
- [3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO} / I_{BHHO} when the input is in the range V_{IL} to V_{IH} .

Table 7. Static characteristics
 At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input [1]					
		$V_{CCI} = 1.2\text{ V}$	$0.8V_{CCI}$	-	$0.8V_{CCI}$	-	V
		$V_{CCI} = 1.4\text{ V}$ to 1.95 V	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		$V_{CCI} = 2.3\text{ V}$ to 2.7 V	1.7	-	1.7	-	V
		$V_{CCI} = 3.0\text{ V}$ to 3.6 V	2.0	-	2.0	-	V
		$V_{CCI} = 4.5\text{ V}$ to 5.5 V	$0.7V_{CCI}$	-	$0.7V_{CCI}$	-	V
		DIR, $\overline{\text{OE}}$ input					
		$V_{CCI} = 1.2\text{ V}$	$0.8V_{CC(A)}$	-	$0.8V_{CC(A)}$	-	V
		$V_{CCI} = 1.4\text{ V}$ to 1.95 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CCI} = 2.3\text{ V}$ to 2.7 V	1.7	-	1.7	-	V
		$V_{CCI} = 3.0\text{ V}$ to 3.6 V	2.0	-	2.0	-	V
		$V_{CCI} = 4.5\text{ V}$ to 5.5 V	$0.7V_{CC(A)}$	-	$0.7V_{CC(A)}$	-	V

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{IL}	LOW-level input voltage	data input [1]					
		V _{CCI} = 1.2 V	-	0.2V _{CCI}	-	0.2V _{CCI}	V
		V _{CCI} = 1.4 V to 1.95 V	-	0.35V _{CCI}	-	0.35V _{CCI}	V
		V _{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		V _{CCI} = 4.5 V to 5.5 V	-	0.3V _{CCI}	-	0.3V _{CCI}	V
		DIR, $\overline{\text{OE}}$ input					
		V _{CCI} = 1.2 V	-	0.2V _{CC(A)}	-	0.2V _{CC(A)}	V
		V _{CCI} = 1.4 V to 1.95 V	-	0.35V _{CC(A)}	-	0.35V _{CC(A)}	V
		V _{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V _{CCI} = 4.5 V to 5.5 V	-	0.3V _{CC(A)}	-	0.3V _{CC(A)}	V		
V _{OH}	HIGH-level output voltage	V _I = V _{IH}					
		I _O = -100 μA; V _{CCO} = 1.2 V to 4.5 V [2]	V _{CCO} - 0.1	-	V _{CCO} - 0.1	-	V
		I _O = -6 mA; V _{CCO} = 1.4 V	1.0	-	1.0	-	V
		I _O = -8 mA; V _{CCO} = 1.65 V	1.2	-	1.2	-	V
		I _O = -12 mA; V _{CCO} = 2.3 V	1.9	-	1.9	-	V
		I _O = -24 mA; V _{CCO} = 3.0 V	2.4	-	2.4	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IL} [2]					
		I _O = 100 μA; V _{CCO} = 1.2 V to 4.5 V	-	0.1	-	0.1	V
		I _O = 6 mA; V _{CCO} = 1.4 V	-	0.3	-	0.3	V
		I _O = 8 mA; V _{CCO} = 1.65 V	-	0.45	-	0.45	V
		I _O = 12 mA; V _{CCO} = 2.3 V	-	0.3	-	0.3	V
		I _O = 24 mA; V _{CCO} = 3.0 V	-	0.55	-	0.55	V
I _I	input leakage current	DIR, $\overline{\text{OE}}$ input; V _I = 0 V to 5.5 V; V _{CCI} = 1.2 V to 5.5 V	-	±2	-	±10	μA
I _{BHL}	bus hold LOW current	A or B port [1]					
		V _I = 0.49 V; V _{CCI} = 1.4 V	15	-	10	-	μA
		V _I = 0.58 V; V _{CCI} = 1.65 V	25	-	20	-	μA
		V _I = 0.70 V; V _{CCI} = 2.3 V	45	-	45	-	μA
		V _I = 0.80 V; V _{CCI} = 3.0 V	100	-	80	-	μA
I _{BHL}	bus hold LOW current	V _I = 1.35 V; V _{CCI} = 4.5 V	100	-	100	-	μA

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I _{BHH}	bus hold HIGH current	A or B port [1]					
		V _I = 0.91 V; V _{CCI} = 1.4 V	-15	-	-10	-	μA
		V _I = 1.07 V; V _{CCI} = 1.65 V	-25	-	-20	-	μA
		V _I = 1.70 V; V _{CCI} = 2.3 V	-45	-	-45	-	μA
		V _I = 2.00 V; V _{CCI} = 3.0 V	-100	-	-80	-	μA
		V _I = 3.15 V; V _{CCI} = 4.5 V	-100	-	-100	-	μA
I _{BHLO}	bus hold LOW overdrive current	A or B port [1][3]					
		V _{CCI} = 1.6 V	125	-	125	-	μA
		V _{CCI} = 1.95 V	200	-	200	-	μA
		V _{CCI} = 2.7 V	300	-	300	-	μA
		V _{CCI} = 3.6 V	500	-	500	-	μA
		V _{CCI} = 5.5 V	900	-	900	-	μA
I _{BHHO}	bus hold HIGH overdrive current	A or B port [1][3]					
		V _{CCI} = 1.6 V	-125	-	-125	-	μA
		V _{CCI} = 1.95 V	-200	-	-200	-	μA
		V _{CCI} = 2.7 V	-300	-	-300	-	μA
		V _{CCI} = 3.6 V	-500	-	-500	-	μA
		V _{CCI} = 5.5 V	-900	-	-900	-	μA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CCO} = 1.2 V to 5.5 V [2]	-	±2	-	±10	μA
		suspend mode A port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 5.5 V; V _{CC(B)} = 0 V [2]	-	±2	-	±10	μA
		suspend mode B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 0 V; V _{CC(B)} = 5.5 V [2]	-	±2	-	±10	μA
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 5.5 V; V _{CC(A)} = 0 V; V _{CC(B)} = 1.2 V to 5.5 V	-	±2	-	±10	μA
		B port; V _I or V _O = 0 V to 5.5 V; V _{CC(B)} = 0 V; V _{CC(A)} = 1.2 V to 5.5 V	-	±2	-	±10	μA

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I _{CC}	supply current	A port; V _I = 0 V or V _{CCI} ; I _O = 0 A [1]					
		V _{CC(A)} , V _{CC(B)} = 1.2 V to 5.5 V	-	15	-	20	μA
		V _{CC(A)} = 5.5 V; V _{CC(B)} = 0 V	-	15	-	20	μA
		V _{CC(A)} = 0 V; V _{CC(B)} = 5.5 V	-2	-	-4	-	μA
		B port; V _I = 0 V or V _{CCI} ; I _O = 0 A					
		V _{CC(A)} , V _{CC(B)} = 1.2 V to 5.5 V	-	15	-	20	μA
		V _{CC(B)} = 0 V; V _{CC(A)} = 5.5 V	-2	-	-4	-	μA
		V _{CC(B)} = 5.5 V; V _{CC(A)} = 0 V	-	15	-	20	μA
		A plus B port (I _{CC(A)} + I _{CC(B)}); I _O = 0 A; V _I = 0 V or V _{CCI}					
V _{CC(A)} , V _{CC(B)} = 1.2 V to 5.5 V	-	25	-	30	μA		
ΔI _{CC}	additional supply current	per input; V _{CC(A)} , V _{CC(B)} = 3.0 V to 5.5 V					
		DIR and OE input; DIR or OE input at V _{CC(A)} - 0.6 V; A port at V _{CC(A)} or GND; B port = open	-	50	-	75	μA
		A port; A port at V _{CC(A)} - 0.6 V; DIR at V _{CC(A)} ; B port = open [4]	-	50	-	75	μA
		B port; B port at V _{CC(B)} - 0.6 V; DIR at GND; A port = open [4]	-	50	-	75	μA

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] To guarantee the node switches, an external driver must source/sink at least I_{BHLO} / I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

[4] For non bus hold parts only (74LVC8T245).

10. Dynamic characteristics

Table 8. Typical dynamic characteristics at $V_{CC(A)} = 1.2\text{ V}$ and $T_{amb} = 25\text{ °C}$ ^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for waveforms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{pd}	propagation delay	An to Bn	11.0	8.5	7.4	6.2	5.7	5.4	ns
		Bn to An	11.0	10.0	9.5	9.1	8.9	8.9	ns
t_{dis}	disable time	\overline{OE} to An	9.5	9.5	9.5	9.5	9.5	9.5	ns
		\overline{OE} to Bn	10.2	8.2	7.8	6.7	7.3	6.4	ns
t_{en}	enable time	\overline{OE} to An	13.5	13.5	13.5	13.5	13.5	13.5	ns
		\overline{OE} to Bn	13.6	10.3	8.9	7.5	7.1	7.0	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Table 9. Typical dynamic characteristics at $V_{CC(B)} = 1.2\text{ V}$ and $T_{amb} = 25\text{ °C}$ ^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for waveforms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
t_{pd}	propagation delay	An to Bn	11.0	10.0	9.5	9.1	8.9	8.8	ns
		Bn to An	11.0	8.5	7.3	6.2	5.7	5.4	ns
t_{dis}	disable time	\overline{OE} to An	9.5	6.8	5.4	3.8	4.1	3.1	ns
		\overline{OE} to Bn	10.2	9.1	8.6	8.1	7.8	7.8	ns
t_{en}	enable time	\overline{OE} to An	13.5	9.0	6.9	4.8	3.8	3.2	ns
		\overline{OE} to Bn	13.6	12.5	12.0	11.5	11.4	11.4	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Table 10. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\text{ °C}$ ^{[1][2]}

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$				Unit
			1.8 V	2.5 V	3.3 V	5.0 V	
C_{PD}	power dissipation capacitance	A port: (direction A to B); B port: (direction B to A)	1	1	1	2	pF
		A port: (direction B to A); B port: (direction A to B)	13	13	13	13	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] $f_i = 10\text{ MHz}$; $V_i = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\ \Omega$.

Table 11. Dynamic characteristics for temperature range –40 °C to +85 °C^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.5 V ± 0.1 V													
t _{pd}	propagation delay	An to Bn	1.7	27	1.7	23	1.3	18	1.0	15	0.8	13	ns
		Bn to An	0.9	27	0.9	25	0.8	23	0.7	23	0.7	22	ns
t _{dis}	disable time	\overline{OE} to An	1.5	30	1.5	30	1.5	30	1.5	30	1.4	30	ns
		\overline{OE} to Bn	2.4	34	2.4	33	1.9	15	1.7	14	1.3	12	ns
t _{en}	enable time	\overline{OE} to An	0.4	34	0.4	34	0.4	34	0.4	34	0.4	34	ns
		\overline{OE} to Bn	1.8	36	1.8	34	1.5	18	1.2	15	0.9	13	ns
V_{CC(A)} = 1.8 V ± 0.15 V													
t _{pd}	propagation delay	An to Bn	1.7	25	1.7	21.9	1.3	9.2	1.0	7.4	0.8	7.1	ns
		Bn to An	0.9	23	0.9	23.8	0.8	23.6	0.7	23.4	0.7	23.4	ns
t _{dis}	disable time	\overline{OE} to An	1.5	30	1.5	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
		\overline{OE} to Bn	2.4	33	2.4	32.2	1.9	13.1	1.7	12.0	1.3	10.3	ns
t _{en}	enable time	\overline{OE} to An	0.4	24	0.4	24.0	0.4	23.8	0.4	23.7	0.4	23.7	ns
		\overline{OE} to Bn	1.8	34	1.8	32.0	1.5	16.0	1.2	12.6	0.9	10.8	ns
V_{CC(A)} = 2.5 V ± 0.2 V													
t _{pd}	propagation delay	An to Bn	1.5	23	1.5	21.4	1.2	9.0	0.8	6.2	0.6	4.8	ns
		Bn to An	1.2	18	1.2	9.3	1.0	9.1	1.0	8.9	0.9	8.8	ns
t _{dis}	disable time	\overline{OE} to An	1.4	9.0	1.4	9.0	1.4	9.0	1.4	9.0	1.4	9.0	ns
		\overline{OE} to Bn	2.3	31	2.3	29.6	1.8	11.0	1.7	9.3	0.9	6.9	ns
t _{en}	enable time	\overline{OE} to An	1.0	10.9	1.0	10.9	1.0	10.9	1.0	10.9	1.0	10.9	ns
		\overline{OE} to Bn	1.7	32	1.7	28.2	1.5	12.9	1.2	9.4	1.0	6.9	ns
V_{CC(A)} = 3.3 V ± 0.3 V													
t _{pd}	propagation delay	An to Bn	1.5	23	1.5	21.2	1.1	8.8	0.8	6.3	0.5	4.4	ns
		Bn to An	0.8	15	0.8	7.2	0.8	6.2	0.7	6.1	0.6	6.0	ns
t _{dis}	disable time	\overline{OE} to An	1.6	8.2	1.6	8.2	1.6	8.2	1.6	8.2	1.6	8.2	ns
		\overline{OE} to Bn	2.1	30	2.1	29.0	1.7	10.3	1.5	8.6	0.8	6.3	ns
t _{en}	enable time	\overline{OE} to An	0.8	8.1	0.8	8.1	0.8	8.1	0.8	8.1	0.8	8.1	ns
		\overline{OE} to Bn	1.8	31	1.8	27.7	1.4	12.4	1.1	8.5	0.9	6.4	ns
V_{CC(A)} = 5.0 V ± 0.5 V													
t _{pd}	propagation delay	An to Bn	1.5	22	1.5	21.4	1.0	8.8	0.7	6.0	0.4	4.2	ns
		Bn to An	0.7	13	0.7	7.0	0.4	4.8	0.3	4.5	0.3	4.3	ns
t _{dis}	disable time	\overline{OE} to An	0.3	5.4	0.3	5.4	0.3	5.4	0.3	5.4	0.3	5.4	ns
		\overline{OE} to Bn	2.0	30	2.0	28.7	1.6	9.7	1.4	8.0	0.7	5.7	ns
t _{en}	enable time	\overline{OE} to An	0.7	6.4	0.7	6.4	0.7	6.4	0.7	6.4	0.7	6.4	ns
		\overline{OE} to Bn	1.5	31	1.5	27.6	1.3	11.4	1.0	8.1	0.9	6.0	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

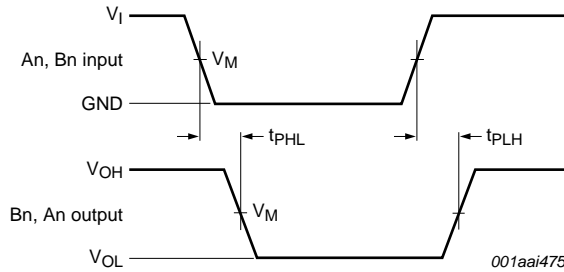
Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.5 V ± 0.1 V													
t _{pd}	propagation delay	An to Bn	1.7	32	1.7	27	1.3	21	1.0	18	0.8	16	ns
		Bn to An	0.9	32	0.9	30	0.8	28	0.7	28	0.7	26	ns
t _{dis}	disable time	\overline{OE} to An	1.5	34	1.5	34	1.5	34	1.5	34	1.4	34	ns
		\overline{OE} to Bn	2.4	41	2.4	40	1.9	18	1.7	17	1.3	15	ns
t _{en}	enable time	\overline{OE} to An	0.4	40	0.4	40	0.4	40	0.4	40	0.4	40	ns
		\overline{OE} to Bn	1.8	43	1.8	41	1.5	22	1.2	18	0.9	16	ns
V_{CC(A)} = 1.8 V ± 0.15 V													
t _{pd}	propagation delay	An to Bn	1.7	30	1.7	25.9	1.3	13.2	1.0	11.4	0.8	11.1	ns
		Bn to An	0.9	27	0.9	28.8	0.8	27.6	0.7	27.4	0.7	27.4	ns
t _{dis}	disable time	\overline{OE} to An	1.5	34	1.5	33.6	1.5	33.4	1.5	33.3	1.4	33.2	ns
		\overline{OE} to Bn	2.4	40	2.4	36.2	1.9	17.1	1.7	16.0	1.3	14.3	ns
t _{en}	enable time	\overline{OE} to An	0.4	28	0.4	28	0.4	27.8	0.4	27.7	0.4	27.7	ns
		\overline{OE} to Bn	1.8	41	1.8	40	1.5	20	1.2	16.6	0.9	14.8	ns
V_{CC(A)} = 2.5 V ± 0.2 V													
t _{pd}	propagation delay	An to Bn	1.5	28	1.5	25.4	1.2	13	0.8	10.2	0.6	8.8	ns
		Bn to An	1.2	23	1.2	13.3	1.0	13.1	1.0	12.9	0.9	12.8	ns
t _{dis}	disable time	\overline{OE} to An	1.4	13	1.4	13	1.4	13	1.4	13	1.4	13	ns
		\overline{OE} to Bn	2.3	37	2.3	33.6	1.8	15	1.7	14.3	0.9	10.9	ns
t _{en}	enable time	\overline{OE} to An	1.0	17.2	1.0	17.2	1.0	17.3	1.0	17.2	1.0	17.3	ns
		\overline{OE} to Bn	1.7	38	1.7	32.2	1.5	18.1	1.2	14.1	1.0	11.2	ns
V_{CC(A)} = 3.3 V ± 0.3 V													
t _{pd}	propagation delay	An to Bn	1.5	28	1.5	25.2	1.1	12.8	0.8	10.3	0.5	10.4	ns
		Bn to An	0.8	18	0.8	11.2	0.8	10.2	0.7	10.1	0.6	10	ns
t _{dis}	disable time	\overline{OE} to An	1.6	12.2	1.6	12.2	1.6	12.2	1.6	12.2	1.6	12.2	ns
		\overline{OE} to Bn	2.1	36	2.1	33	1.7	14.3	1.5	12.6	0.8	10.3	ns
t _{en}	enable time	\overline{OE} to An	0.8	14.1	0.8	14.1	0.8	13.6	0.8	13.2	0.8	13.6	ns
		\overline{OE} to Bn	1.8	37	1.8	31.7	1.4	18.4	1.1	12.9	0.9	10.9	ns
V_{CC(A)} = 5.0 V ± 0.5 V													
t _{pd}	propagation delay	An to Bn	1.5	26	1.5	25.4	1.0	12.8	0.7	10	0.4	8.2	ns
		Bn to An	0.7	16	0.7	11	0.4	8.8	0.3	8.5	0.3	8.3	ns
t _{dis}	disable time	\overline{OE} to An	0.3	9.4	0.3	9.4	0.3	9.4	0.3	9.4	0.3	9.4	ns
		\overline{OE} to Bn	2.0	36	2.0	32.7	1.6	13.7	1.4	12	0.7	9.7	ns
t _{en}	enable time	\overline{OE} to An	0.7	10.9	0.7	10.9	0.7	10.9	0.7	10.9	0.7	10.9	ns
		\overline{OE} to Bn	1.5	37	1.5	31.6	1.3	18.4	1.0	13.7	0.9	10.7	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

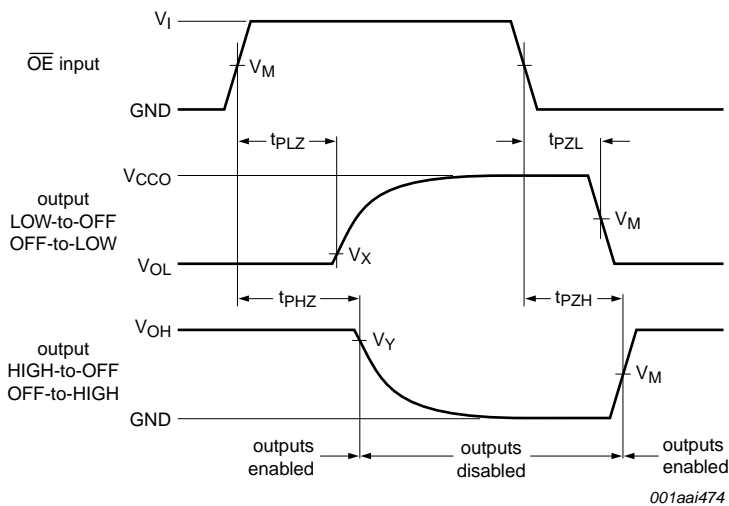
11. Waveforms



Measurement points are given in [Table 13](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. The data input (An, Bn) to output (Bn, An) propagation delay times



Measurement points are given in [Table 13](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

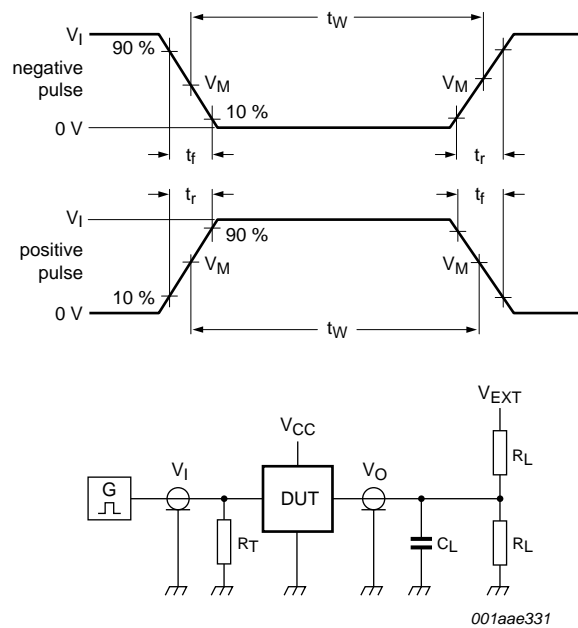
Fig 6. Enable and disable times

Table 13. Measurement points

Supply voltage	Input ^[1]	Output ^[2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
3.0 V to 5.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in [Table 14](#).
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance.
 V_{EXT} = External voltage for measuring switching times.

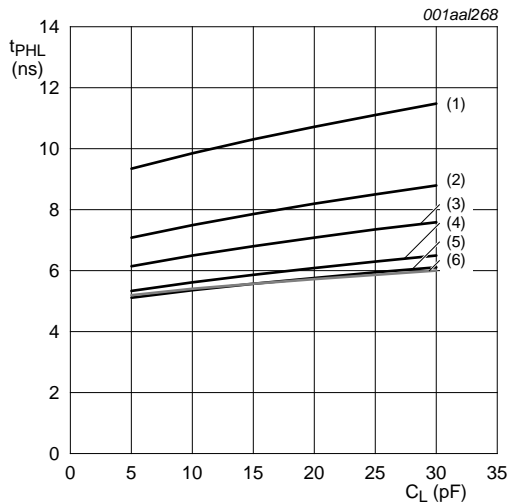
Fig 7. Load circuitry for switching times

Table 14. Test data

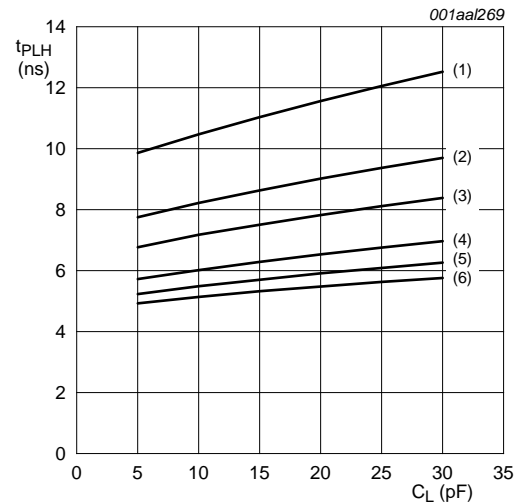
Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	V_I ^[1]	$\Delta t/\Delta V$ ^[2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} ^[3]
1.2 V to 5.5 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$

- [1] V_{CCI} is the supply voltage associated with the data input port.
- [2] $dV/dt \geq 1.0 \text{ V/ns}$.
- [3] V_{CCO} is the supply voltage associated with the output port.

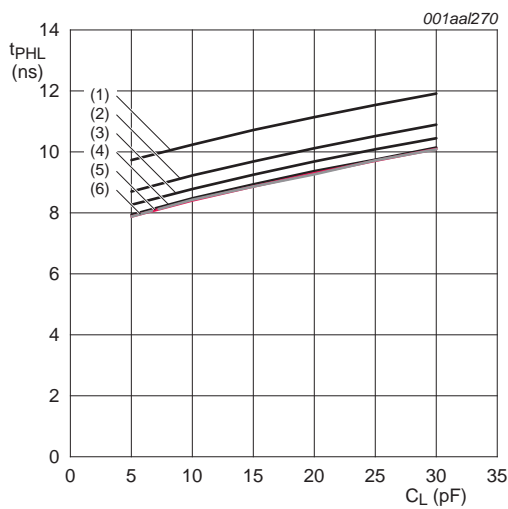
12. Typical propagation delay characteristics



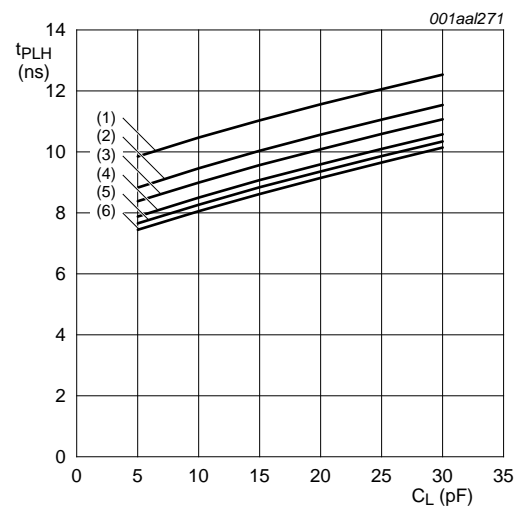
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



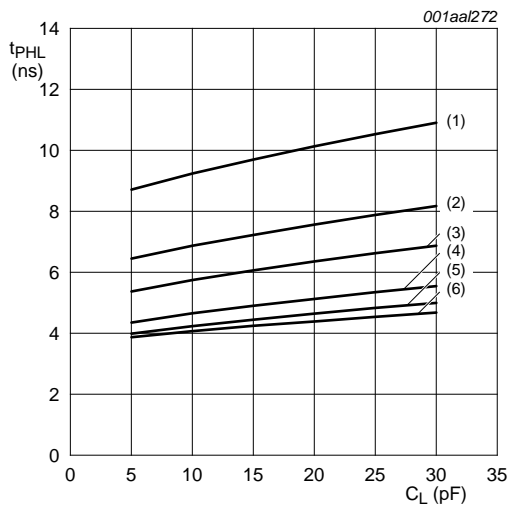
c. HIGH to LOW propagation delay (B to A)



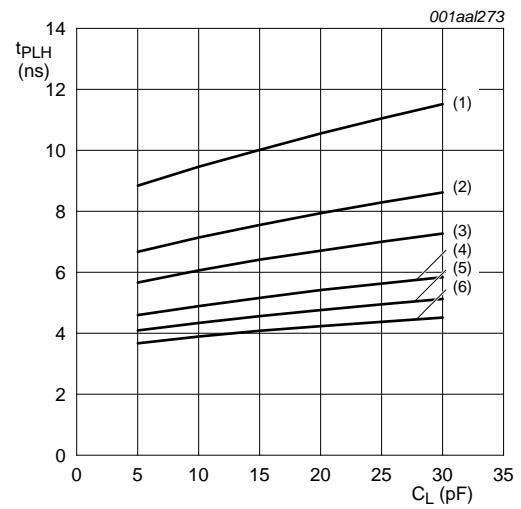
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2\text{ V}$.
- (2) $V_{CC(B)} = 1.5\text{ V}$.
- (3) $V_{CC(B)} = 1.8\text{ V}$.
- (4) $V_{CC(B)} = 2.5\text{ V}$.
- (5) $V_{CC(B)} = 3.3\text{ V}$.
- (6) $V_{CC(B)} = 5.0\text{ V}$.

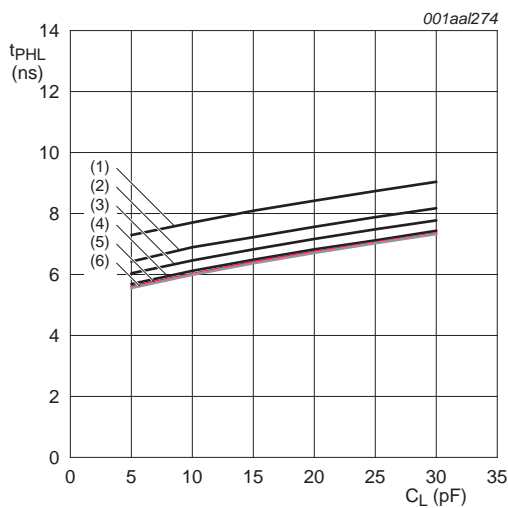
Fig 8. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CC(A)} = 1.2\text{ V}$



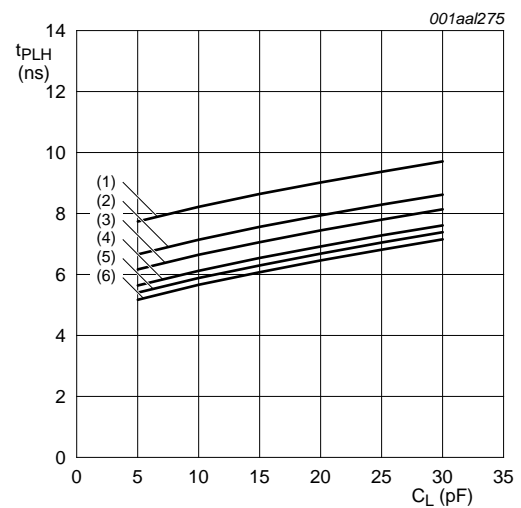
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



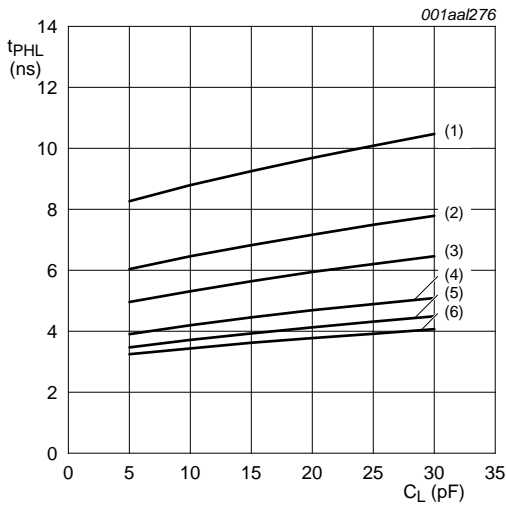
c. HIGH to LOW propagation delay (B to A)



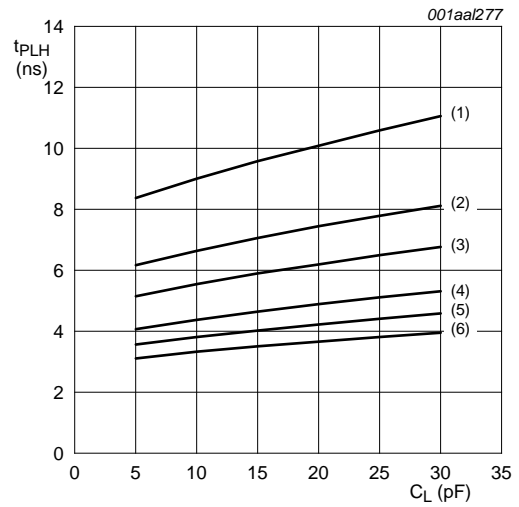
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2\text{ V}$.
- (2) $V_{CC(B)} = 1.5\text{ V}$.
- (3) $V_{CC(B)} = 1.8\text{ V}$.
- (4) $V_{CC(B)} = 2.5\text{ V}$.
- (5) $V_{CC(B)} = 3.3\text{ V}$.
- (6) $V_{CC(B)} = 5.0\text{ V}$.

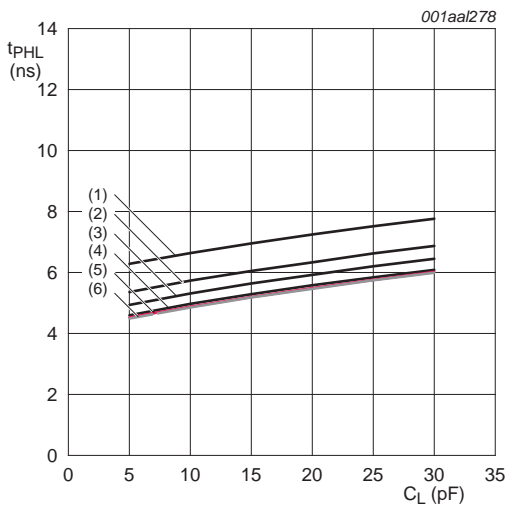
Fig 9. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{CC(A)} = 1.5\text{ V}$



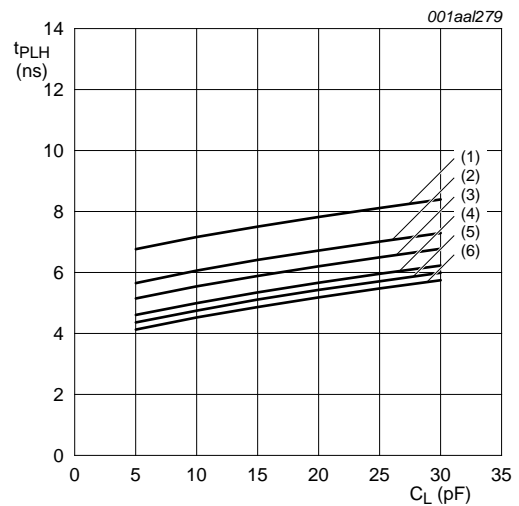
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



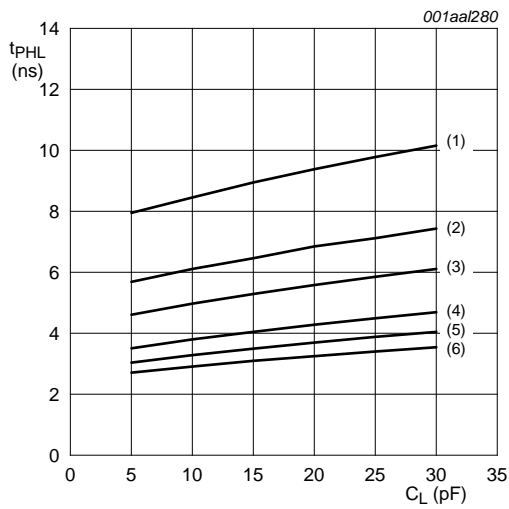
c. HIGH to LOW propagation delay (B to A)



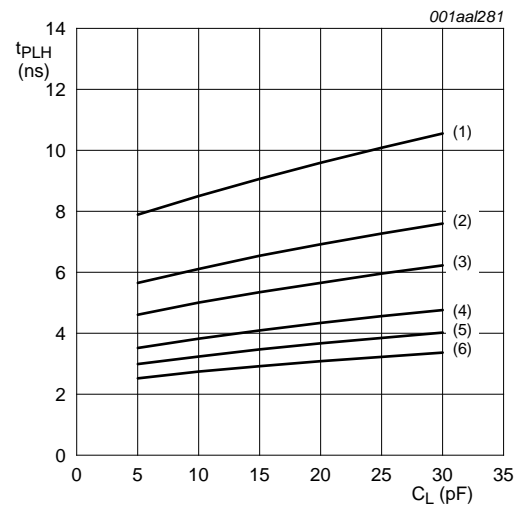
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2\text{ V}$.
- (2) $V_{CC(B)} = 1.5\text{ V}$.
- (3) $V_{CC(B)} = 1.8\text{ V}$.
- (4) $V_{CC(B)} = 2.5\text{ V}$.
- (5) $V_{CC(B)} = 3.3\text{ V}$.
- (6) $V_{CC(B)} = 5.0\text{ V}$.

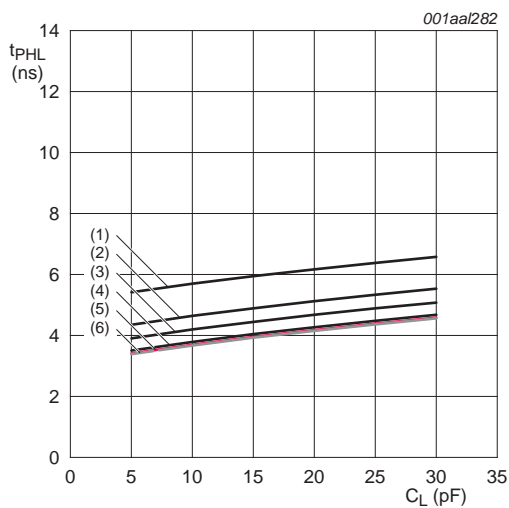
Fig 10. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{CC(A)} = 1.8\text{ V}$



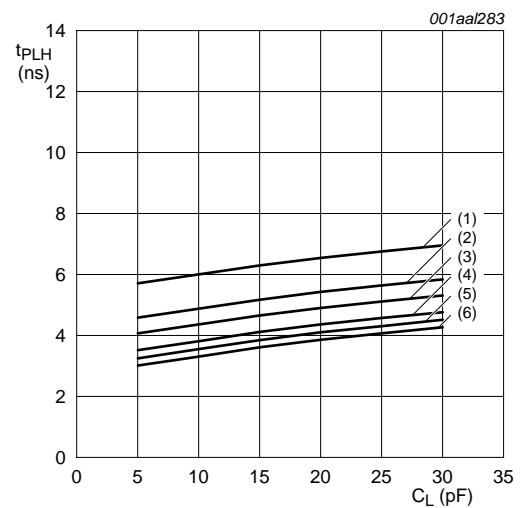
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



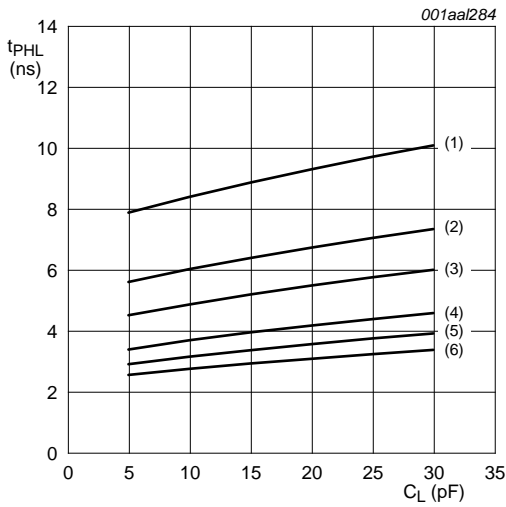
c. HIGH to LOW propagation delay (B to A)



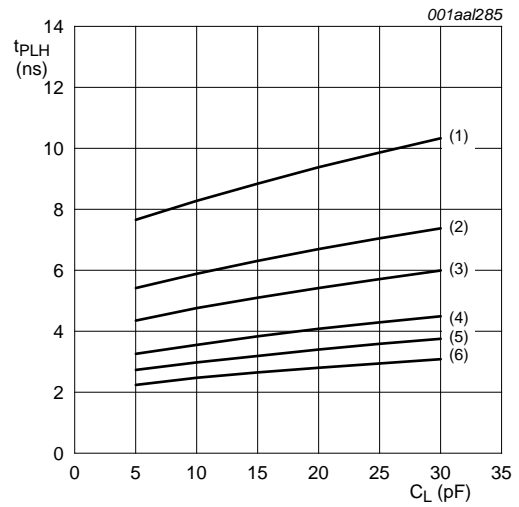
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2\text{ V}$.
- (2) $V_{CC(B)} = 1.5\text{ V}$.
- (3) $V_{CC(B)} = 1.8\text{ V}$.
- (4) $V_{CC(B)} = 2.5\text{ V}$.
- (5) $V_{CC(B)} = 3.3\text{ V}$.
- (6) $V_{CC(B)} = 5.0\text{ V}$.

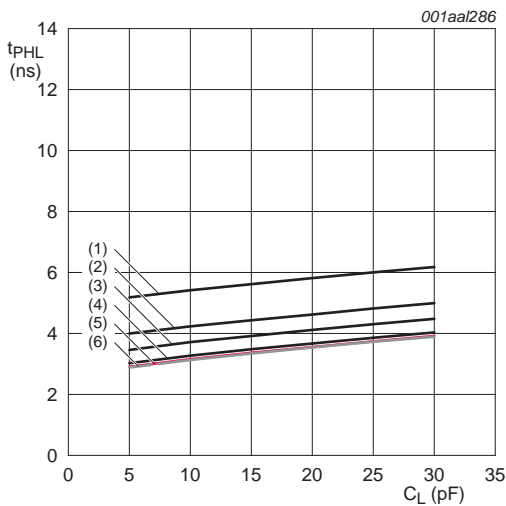
Fig 11. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{CC(A)} = 2.5\text{ V}$



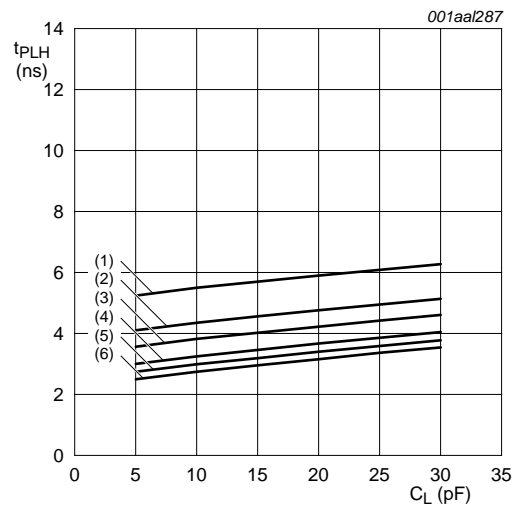
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



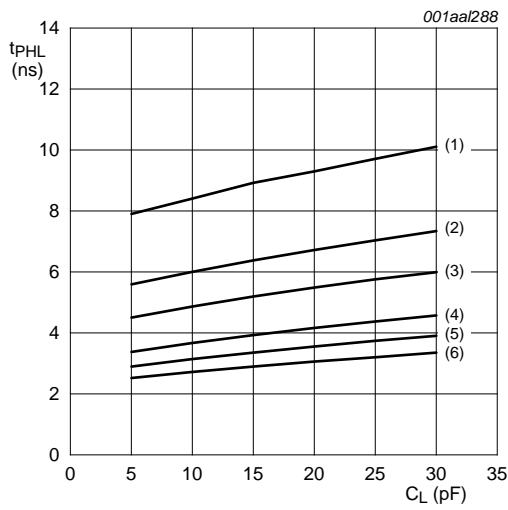
c. HIGH to LOW propagation delay (B to A)



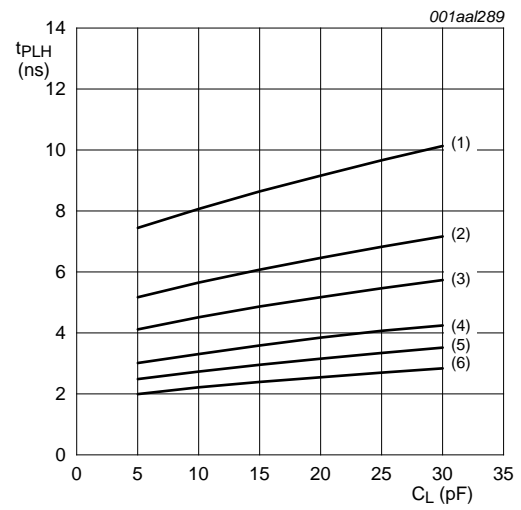
d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2\text{ V}$.
- (2) $V_{CC(B)} = 1.5\text{ V}$.
- (3) $V_{CC(B)} = 1.8\text{ V}$.
- (4) $V_{CC(B)} = 2.5\text{ V}$.
- (5) $V_{CC(B)} = 3.3\text{ V}$.
- (6) $V_{CC(B)} = 5.0\text{ V}$.

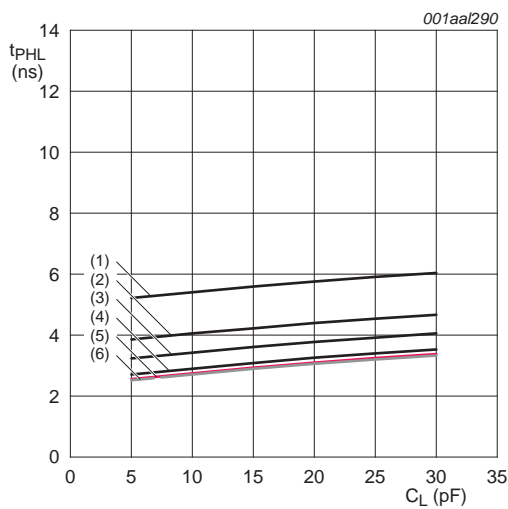
Fig 12. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{CC(A)} = 3.3\text{ V}$



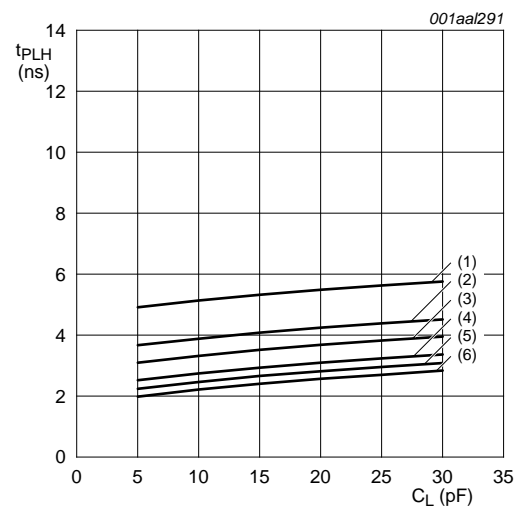
a. HIGH to LOW propagation delay (A to B)



b. LOW to HIGH propagation delay (A to B)



c. HIGH to LOW propagation delay (B to A)



d. LOW to HIGH propagation delay (B to A)

- (1) $V_{CC(B)} = 1.2\text{ V}$.
- (2) $V_{CC(B)} = 1.5\text{ V}$.
- (3) $V_{CC(B)} = 1.8\text{ V}$.
- (4) $V_{CC(B)} = 2.5\text{ V}$.
- (5) $V_{CC(B)} = 3.3\text{ V}$.
- (6) $V_{CC(B)} = 5.0\text{ V}$.

Fig 13. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{CC(A)} = 5\text{ V}$

13. Application information

13.1 Unidirectional logic level-shifting application

The circuit given in [Figure 14](#) is an example of the 74LVC8T245; 74LVCH8T245 being used in an unidirectional logic level-shifting application.

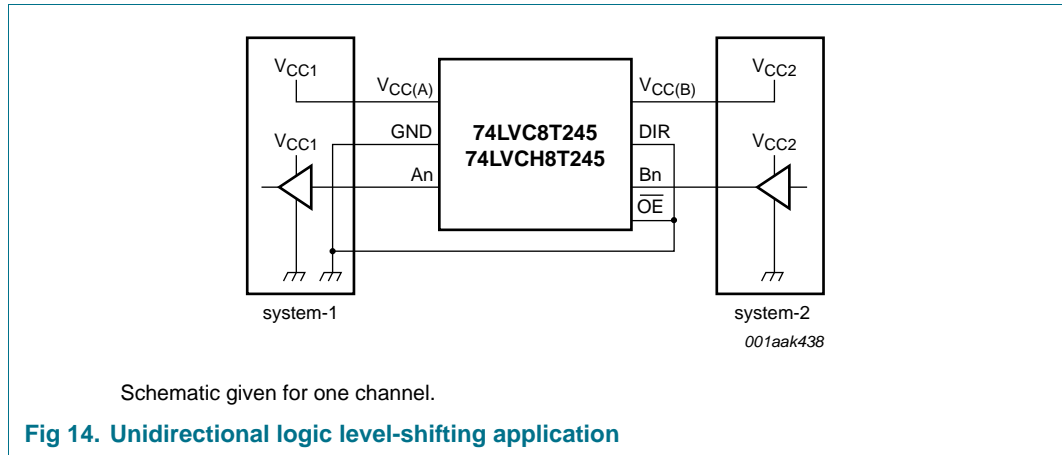


Table 15. Description unidirectional logic level-shifting application

Name	Function	Description
$V_{CC(A)}$	V_{CC1}	supply voltage of system-1 (1.2 V to 5.5 V)
GND	GND	device GND
A	OUT	output level depends on V_{CC1} voltage
B	IN	input threshold value depends on V_{CC2} voltage
DIR	DIR	the GND (LOW level) determines B port to A port direction
$V_{CC(B)}$	V_{CC2}	supply voltage of system-2 (1.2 V to 5.5 V)
\overline{OE}	\overline{OE}	The GND (LOW level) enables the output ports

13.2 Bidirectional logic level-shifting application

Figure 15 shows the 74LVC8T245; 74LVCH8T245 being used in a bidirectional logic level-shifting application.

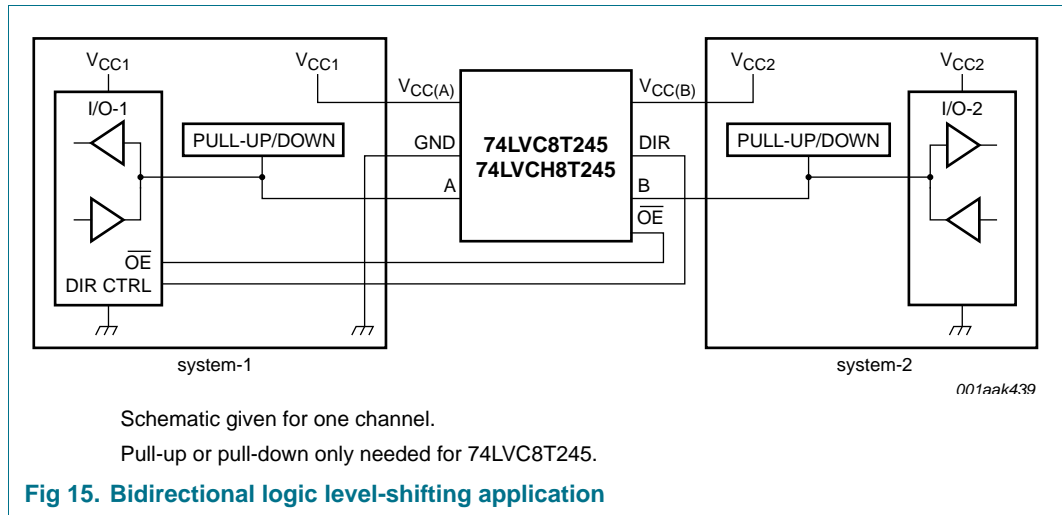


Fig 15. Bidirectional logic level-shifting application

Table 16 gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

Table 16. Description bidirectional logic level-shifting application

State	DIR CTRL	OE	I/O-1	I/O-2	Description
1	H	L	output	input	system-1 data to system-2
2	H	H	Z	Z	system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	H	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold.
4	L	L	input	output	system-2 data to system-1

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

13.3 Power-up considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

Table 17. Typical total supply current (I_{CC(A)} + I_{CC(B)})

V _{CC(A)}	V _{CC(B)}					Unit
	0 V	1.8 V	2.5 V	3.3 V	5.0 V	
0 V	0	< 1	< 1	< 1	< 1	μA
1.8 V	< 1	< 2	< 2	< 2	2	μA
2.5 V	< 1	< 2	< 2	< 2	< 2	μA
3.3 V	< 1	< 2	< 2	< 2	< 2	μA
5.0 V	< 1	2	< 2	< 2	< 2	μA

14. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

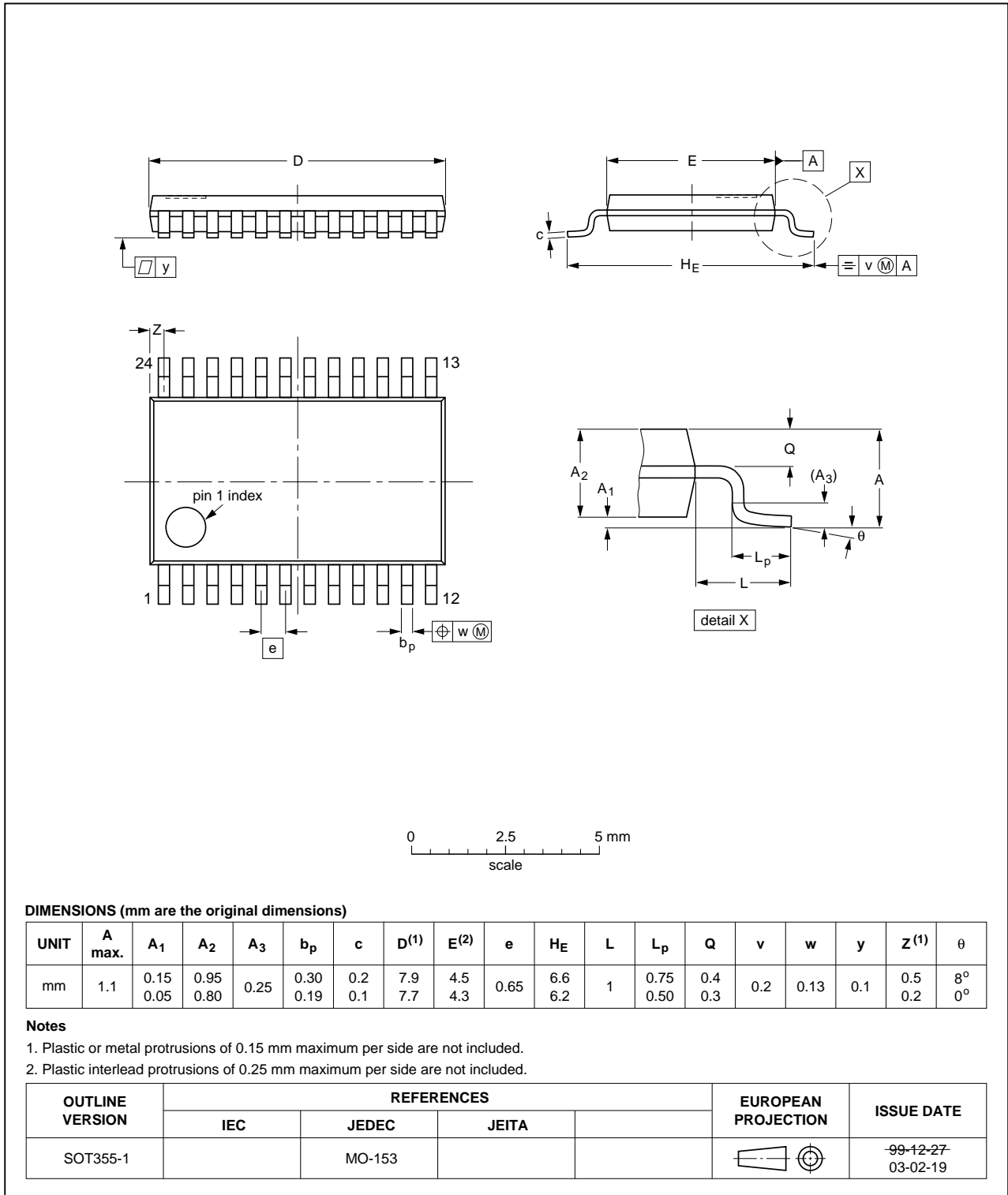


Fig 16. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

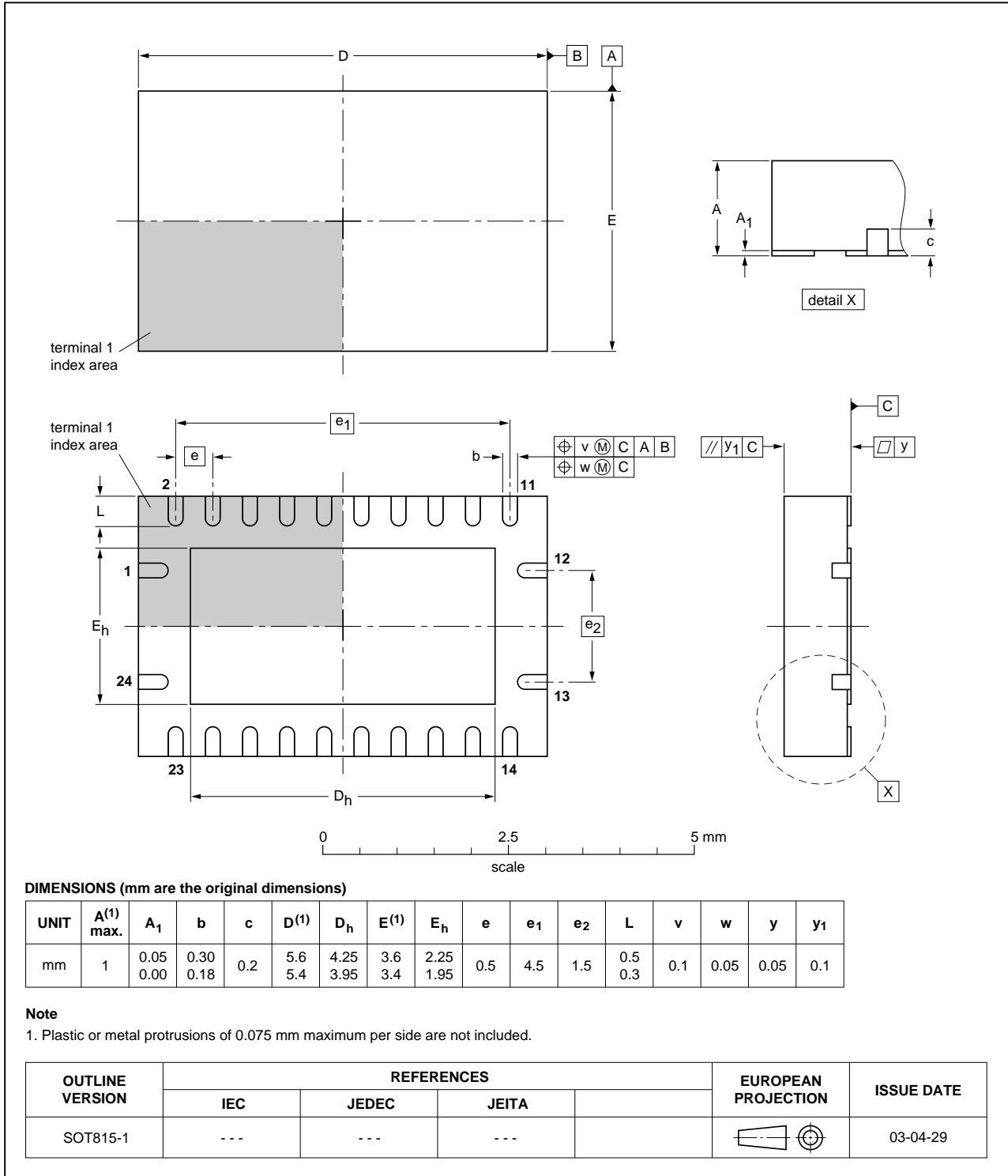


Fig 17. Package outline SOT815-1 (DHVQFN24)

15. Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
HBM	Human Body Model
MM	Machine Model

16. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH8T245 v.3	20111212	Product data sheet	-	74LVC_LVCH8T245 v.2
Modifications:	• Legal pages updated.			
74LVC_LVCH8T245 v.2	20110211	Product data sheet	-	74LVC_LVCH8T245 v.1
74LVC_LVCH8T245 v.1	20100111	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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