NXP Semiconductors
User Guide

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Eight-channel DMIC Board User Manual

Supports Board Revision B

Contents

Chapter 1
Overview

The eight-channel DMIC plug-in board (8CH-DMIC) provides a single, a double, a triple, a quad, a hexagonal, a hexagonal (with center mic), and an octal digital microphone (DMIC) solution. The plug-in board can be used with selected EVKs, such as MIMXRT685-EVK, MIMXRT685-AUD-EVK, and MIMXRT595-EVK (I2C LED control may not be supported on all boards).

This document provides the detail about the 11 DMICs and their configurations, jumpers, LEDs, switches, and other interfaces available on the board.

Example programs for use of the 8CH-DMIC board can be found in the MCUXpresso SDK software for the EVK being used (see https://mcuxpresso.nxp.com or download the SDK directly from within MCUXpresso IDE).

1.1 Acronyms

The following table describes the acronyms and abbreviations used in this document.

Table 1. Acronyms and Abbreviations

Term	Definition
ADC	Analog to digital converter
CPU	Central processing unit
DMIC	Digital microphone
GPIO	General-purpose input/output
LED	Light emitting diode
MCU	Microcontroller unit
PCB	Printed circuit board
RF	Radio frequency
SMA	Subminiature version a connector
SPI	Serial peripheral interface
UART	Universal asynchronous receiver transmitter

1.2 Related documentation

The table below lists and explains the additional documents and resources that you can refer to for more information on 8-CH DMIC board. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 2. Related documentation

Document	Description	Link/How to access
i.MX RT685 Evaluation Board User Manual	It describes the board layout and settings, and also different interfaces and peripherals available on the board.	UM11159
MIMXRT685-AUD-EVK Board User Manual	This document provides detailed information about the MIMXRT685-	Contact NXP FAE / sales representative

Table continues on the next page...

Table 2. Related documentation (continued)

Document	Description	Link/How to access
	AUD-EVK board interfaces, power supplies, clocks, push buttons, jumpers, and LEDs.	

1.3 Kit content

The table below describes the items included in the 8-CH DMIC board kit.

Table 3. Kit contents

Item	Quantity
Board hardware assembly	1

1.4 Block diagram

The figure below describes the 8-CH DMIC block diagram.

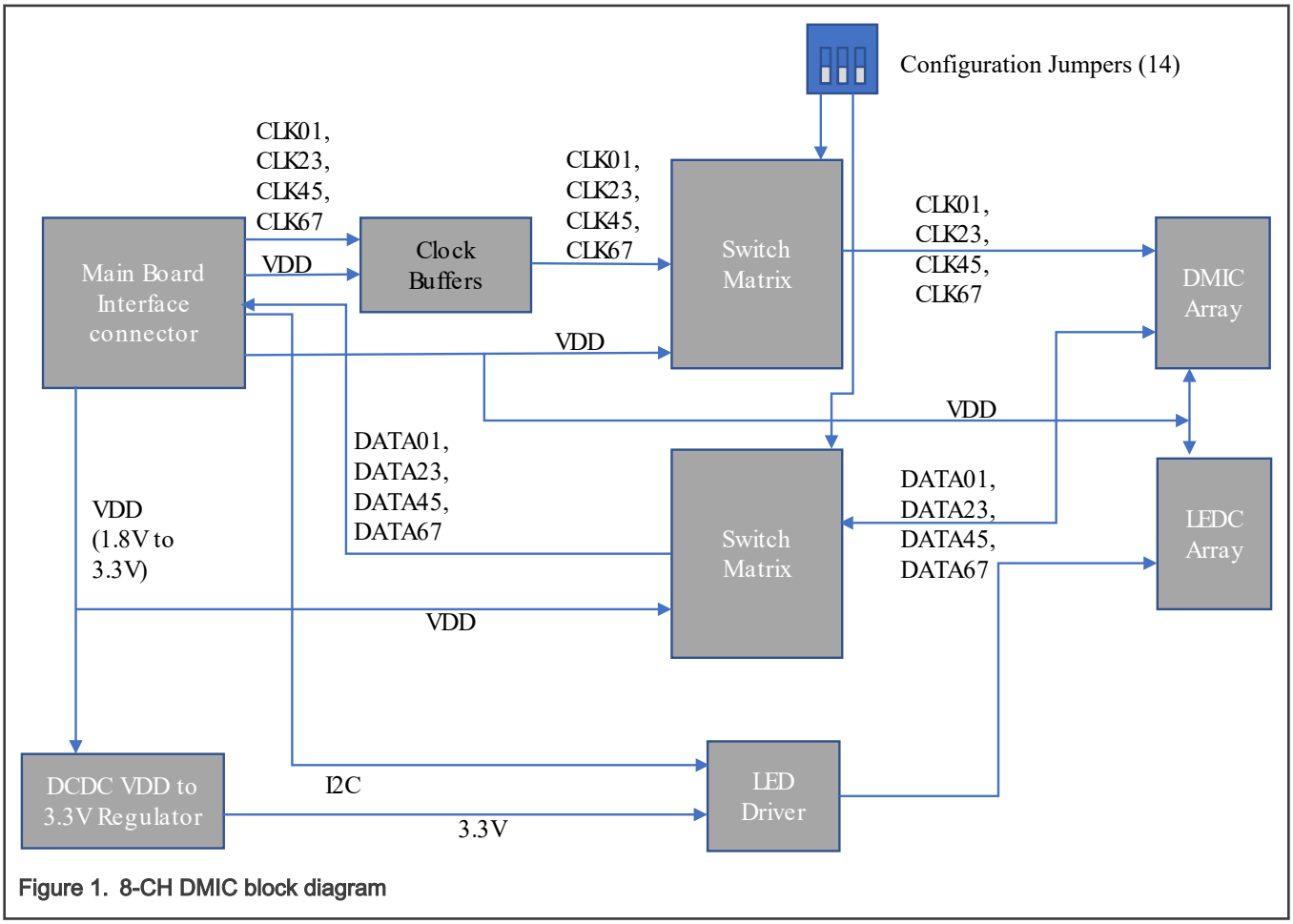

Figure 1. 8-CH DMIC block diagram

1.5 Board pictures

The figure below shows the top side of the board, and highlights the jumpers and LEDs available on the board.

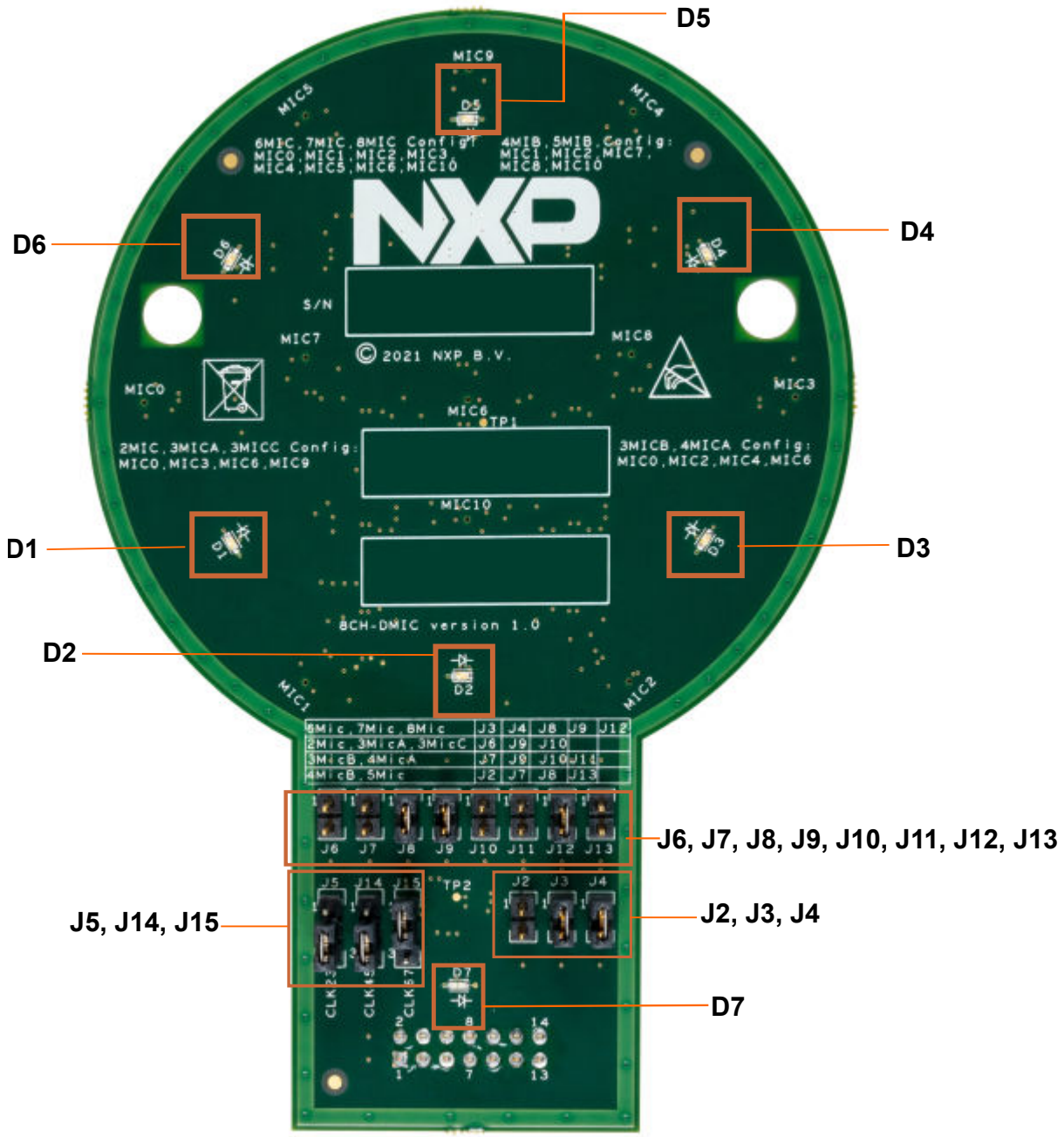

Figure 2. 8CH-DMIC board top side

The figure below shows the bottom side of the board, and highlights the interface connector.

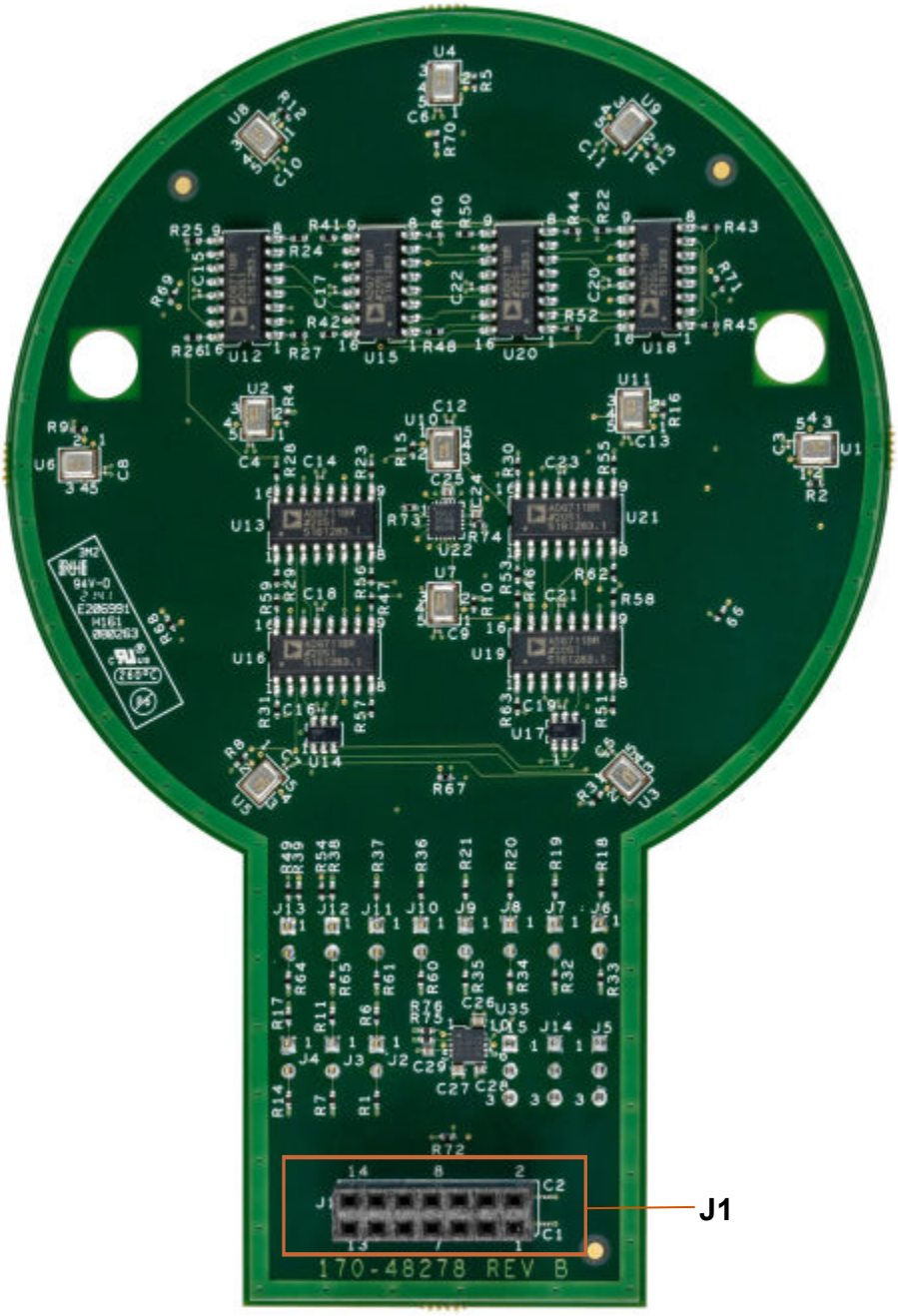

Figure 3. 8CH-DMIC board bottom side

1.6 Board features

The table below describes the DMIC board features.

Table 4. Main features

Board feature	Processor feature used	Description
Interfacing with Main board		14-pin connector used for DMIC board connection with the main board
Power	Input power ranges from 1.8 V to 3.3 V	Typically, 1.8 V power is used for DMICs, and other interfaces, however, 3.3 V power also works. **Note:** MCP1256T DC converter to convert 1.8 V input power supply to 3.3 V power supply for onboard LEDs.
Clock	Four clocks: CLK01, CLK23, CLK45, and CLK67	Clocks are used for 11 DMICs available on board. Clocks can be combined with jumpers J5, J14, and J15 for use with boards that do not have all the clocks available. Refer to Table 23 for settings.
DMIC array		11 DMICs; at most, eight DMICs are in use simultaneously. DMIC data signals: • DATA01 • DATA23 • DATA45 • DATA67

1.7 Connectors

Table 5. Connector detail

Part identifier	Connector type	Description
J1	2x7-pin connector	For 8-CH DMIC board connection with the main board

The table below describes the pin description of J1 connector.

Table 6. Interface connector pin detail

Pin	Signal	Direction
1	VDD	-
2	VDD	-
3	CLK01	I
4	DATA01	O
5	CLK23	I
6	DATA23	O
7	CLK45	I
8	DATA45	O
9	CLK67	I
10	DATA67	O

Table continues on the next page...

Table 6. Interface connector pin detail (continued)

Pin	Signal	Direction
11	GND	-
12	GND	-
13	I2C_SCL	I
14	I2C_SDA	I/O

1.8 Jumpers

The following table describes the jumpers available on the board.

Table 7. Jumpers

Part identifier	Jumper type	Description	Settings
J2	1x2 header	Jumper for SPH0641LM4H-1 MIC 1 (U3)	• Open: SELECT pin of SPH0641LM4H-1 MIC 1 (U3) is powered by 1.8 V and asserts data on CLK_MIC1 rising edge (default setting) • Shorted: SELECT pin of SPH0641LM4H-1 MIC 1 (U3) is grounded and asserts data on CLK_MIC1 falling edge
J3	1x2 header	Jumper for SPH0641LM4H-1 MIC 2 (U5)	• Open: SELECT pin of SPH0641LM4H-1 MIC2 (U5) is powered by 1.8 V and asserts data on CLK_MIC2 rising edge • Shorted: SELECT pin of SPH0641LM4H-1 MIC2 (U5) is grounded and asserts data on CLK_MIC2 falling edge (default setting)
J4	1x2 header	Jumper for SPH0641LM4H-1 MIC 6 (U10)	• Open: SELECT pin of SPH0641LM4H-1 MIC6 (U10) is powered by 1.8 V and asserts data on CLK_MIC6 rising edge • Shorted: SELECT pin of SPH0641LM4H-1 MIC6 (U10) is grounded and asserts data on CLK_MIC6 falling edge (default setting)
J5	1x3 header	Jumper for selection of CLK01 or CLK23 clock signal	• 1-2 shorted: CLK01 is connected and supplies the clock (option1) • 2-3 shorted: CLK23 is connected and supplies the clock (default setting) **NOTE** Combination of jumpers J5, J14, and J15 provide several clock selection options. For detail, see Table 23.
J6	1x2 header	Used to:	• Open: Data control and clock control signals for MIC 3 and MIC 9 are high, and MIC 3 and MIC 9 are not enabled (default setting)

Table continues on the next page...

Table 7. Jumpers (continued)

Part identifier	Jumper type	Description	Settings
		• control the data from ADG711 (U12) switch and clock from ADG711 (U16) switch for MIC 3 • control the data from ADG711 (U18) switch and clock from ADG711 (U21) switch for MIC 9	• Shorted: Data control and clock control signals for MIC 3 and MIC 9 are low, and MIC 3 and MIC 9 are enabled
J7	1x2 header	Used to control the data from ADG711 (U12) switch and clock from ADG711 (U13) switch for MIC 2	• Open: Data control and clock control signals for MIC 2 are high, and MIC 2 is not enabled (default setting) • Shorted: Data control and clock control signals for MIC 2 are low, and MIC 2 is enabled
J8	1x2 header	Used to control the data from ADG711 (U12) switch and clock from ADG711 (U13) switch for MIC 1	• Open: Data control and clock control signal for MIC 1 are high, and MIC 1 is not enabled • Shorted: Data control and clock control signal for MIC 1 are low, and MIC 1 is enabled (default setting)
J9	1x2 header	Used to control the data from ADG711 (U12) switch and clock from ADG711 (U13) switch for MIC 0	• Open: Data control and clock control signals for MIC 0 are high, and MIC 0 is not enabled • Shorted: Data control and clock control signals for MIC 0 are low, and MIC 0 is enabled (default setting)
J10	1x2 header	Used to control the data from ADG711 (U15) switch and clock from ADG711 (U19) switch for MIC 6	• Open: Data control and clock control signals for MIC 6 are high, and MIC 6 is not enabled (default setting) • Shorted: Data control and clock control signals for MIC 6 are low, and MIC 6 is enabled
J11	1x2 header	Used to control the data from ADG711 (U15) switch and clock from ADG711 (U16) switch for MIC 4	• Open: Data control and clock control signals for MIC 4 are high, and MIC 4 is not enabled (default setting) • Shorted: Data control and clock control signals for MIC 4 are low, and MIC 4 is enabled
J12	1x2 header	Used to: • control the data from ADG711 (U15) switch and clock from ADG711 (U16) switch for MIC 3 • control the data from ADG711 (U15) switch and clock from ADG711 (U13) switch for MIC 2	• Open: Data control and clock control signals for MIC 2, MIC 3, MIC 4, MIC 5, MIC 6, and MIC 10 are high, and MIC 2, MIC 3, MIC 4, MIC 5, MIC 6, and MIC 10 are not enabled • Shorted: Data control and clock control signals for MIC 2, MIC 3, MIC 4, MIC 5, MIC 6, and MIC 10 are high, and MIC 2, MIC 3, MIC 4, MIC 5, MIC 6, and MIC 10 are enabled (default setting)

Table continues on the next page...

Table 7. Jumpers (continued)

Part identifier	Jumper type	Description	Settings
		• control the data from ADG711 (U20) switch and clock from ADG711 (U19) switch for MIC 6 • control the data from ADG711 (U20) switch and clock from ADG711 (U21) switch for MIC 10 • control the data from ADG711 (U20) switch and clock from ADG711 (U19) switch for MIC 5 • control the data from ADG711 (U20) switch and clock from ADG711 (U16) switch for MIC 4	
J13	1x2 header	Used to: • control the data from ADG711 (U18) switch and clock from ADG711 (U19) switch for MIC 7 • control the data from ADG711 (U18) switch and clock from ADG711 (U21) switch for MIC 8 • control the data from ADG711 (U18) switch and clock from ADG711 (U21) switch for MIC 10	• Open: Data control and clock control signals for MIC 7, MIC 8, and MIC 10 are high, and MIC 7, MIC 8, and MIC 10 are not enabled (default setting) • Shorted: Data control and clock control signals for MIC 7, MIC 8, and MIC 10 are high, and MIC 7, MIC 8, and MIC 10 are enabled
J14	1x3 header	Jumper for selection of CLK01 or CLK45 clock signal	• 1-2 shorted: CLK01 is connected and supplies the clock (option1) • 2-3 shorted: CLK45 is connected and supplies the clock (default setting) **NOTE** Combination of jumpers J5, J14, and J15 provide several clock selection options. For detail, see Table 23.
J15	1x3 header	Jumper for selection of CLK45 or CLK67 clock signal	• 1-2 shorted: CLK45 is connected and supplies the clock (default setting) • 2-3 shorted: CLK67 is connected and supplies the clock (Option1)

Table continues on the next page...

Table 7. Jumpers (continued)

Part identifier	Jumper type	Description	Settings
			NOTE Combination of jumpers J5, J14, and J15 provide several clock selection options. For detail, see Table 23.

1.9 LEDs

Total of eight LEDs are available on the 8-CH DMIC board. The table below describes the DMIC board LEDs.

Table 8. LEDs

Part identifier	LED color	LED Placement	Description (When LED is ON)
D1	Blue	Available on top of the plug-in board	User Programmable LEDs
D2	Blue	Available on top of the plug-in board	
D3	Blue	Available on top of the plug-in board	
D4	Blue	Available on top of the plug-in board	
D5	Blue	Available on top of the plug-in board	
D6	Blue	Available on top of the plug-in board	
D7	Red	Available on top of the plug-in board next to the interface connector (J1)	

Chapter 2
Functional Description

This chapter describes the features and different interfaces of 8-CH DMIC board.

2.1 Power supply

This section describes the power supply on 8-CH DMIC board.

2.1.1 Main power supply

The 8-CH DMIC board can accept from 1.8 V up to 3.6 V for operation from the main board through J1 interface connector.

2.1.2 Secondary power supply

The MCP1256T device (U35) generates a 3.3 V output voltage from 1.8V input supply. The 3.3 V power supply is used for:

- Onboard LEDs [D1:D7]
- SX1502I087TRT GPIO expander used for LEDs

2.2 DMIC interface

A total of 11 DMICs are available on the DMIC board, however, at most, eight DMICs are in use simultaneously.

The below figure describes the different DMICs placement on the board.

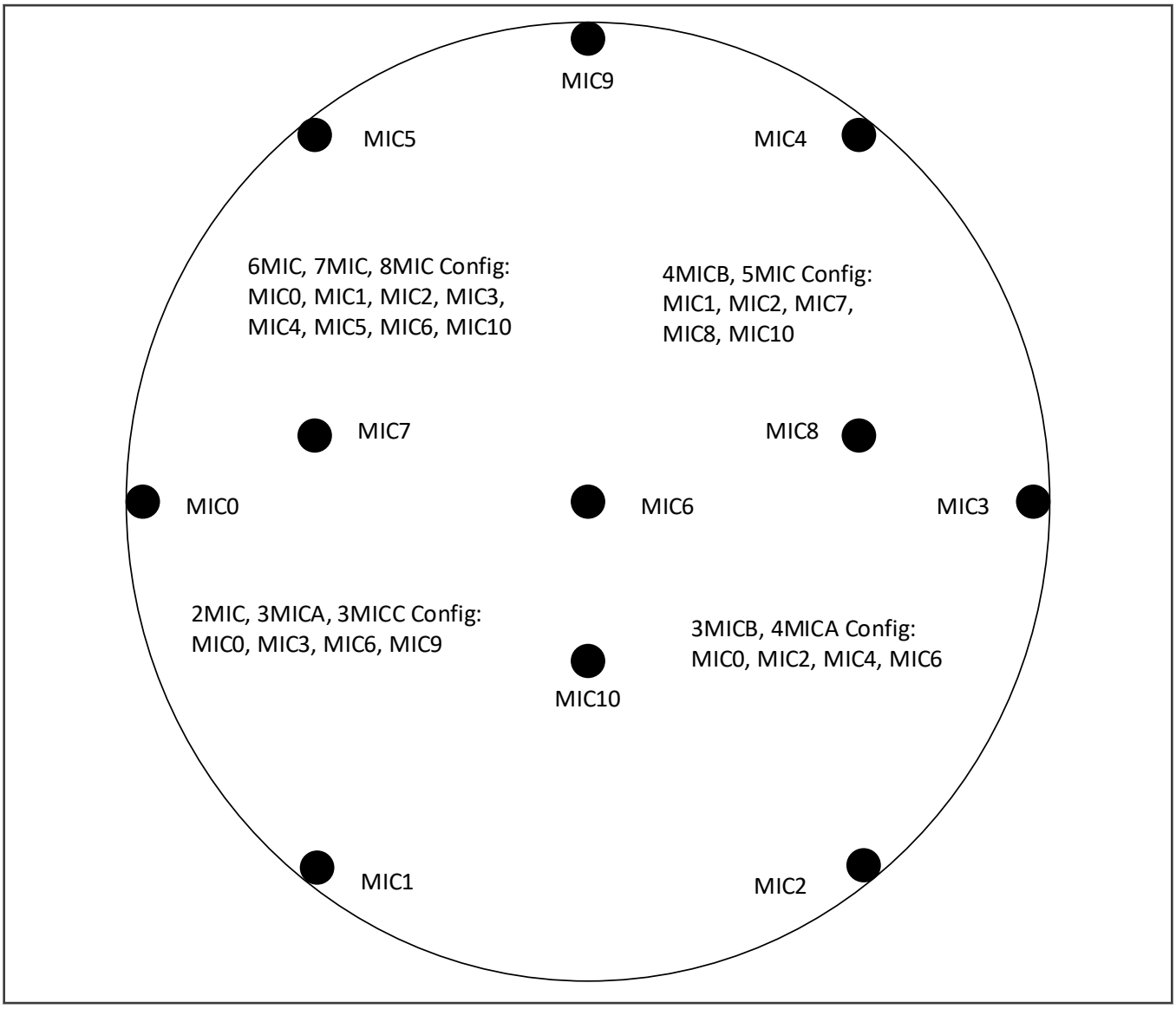

Table 9. DMIC Array

Part identifier	Device	Mic	Description
U1	SPH0641LM4H-1	MIC0	Asserts data on CLK_MIC0 falling edge
U3		MIC1	Asserts data on CLK_MIC1 rising and falling edge depending upon jumper J2 setting
U2		MIC8	Asserts data on CLK_MIC8 rising edge
U4		MIC9	Asserts data on CLK_MIC9 falling edge
U5		MIC2	Asserts data on CLK_MIC2 rising and falling edge depending upon jumper J3 setting
U6		MIC3	Asserts data on CLK_MIC3 rising edge
U7		MIC10	Asserts data on CLK_MIC10 rising edge

Table continues on the next page...

Table 9. DMIC Array (continued)

Part identifier	Device	Mic	Description
U8		MIC4	Asserts data on CLK_MIC4 falling edge
U9		MIC5	Asserts data on CLK_MIC5 rising edge
U10		MIC6	Asserts data on CLK_MIC6 rising and falling edge depending upon jumper J4 setting
U11		MIC7	Asserts data on CLK_MIC7 falling edge

2.2.1 DMIC configurations and signal connections

Ten different DMIC configurations are possible on the board as follows:

- 2DMIC
- 3DMIC[A]
- 3DMIC[B]
- 3DMIC[C]
- 4DMIC[A]
- 4DMIC[B]
- 5DMIC
- 6DMIC
- 7DMIC
- 8DMIC

The below tables describe the different DMIC configurations and respective data and clock signals that are active for these configurations.

2DMIC configuration

Table 10. 2DMIC configuration

Part identifier	DMIC	Active Data and Clock signal
U1	DMIC0	DATA01 and CLK01
U6	DMIC3	

The figure below shows the 2DDMIC configuration.

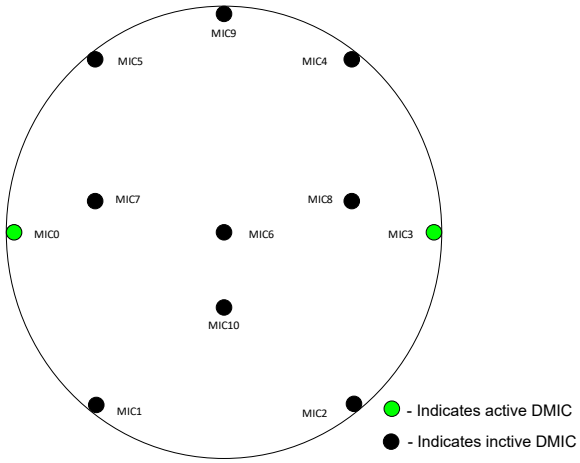

Figure 4. 2DMIC configuration

3DMIC[A] configuration

Table 11. 3DMIC[A] configuration

Part identifier	DMIC	Active Data and Clock signal
U1	DMIC0	DATA01 and CLK01
U6	DMIC3	
U4	DMIC9	DATA23 and CLK23

The figure below shows the 3DMIC[A] configuration.

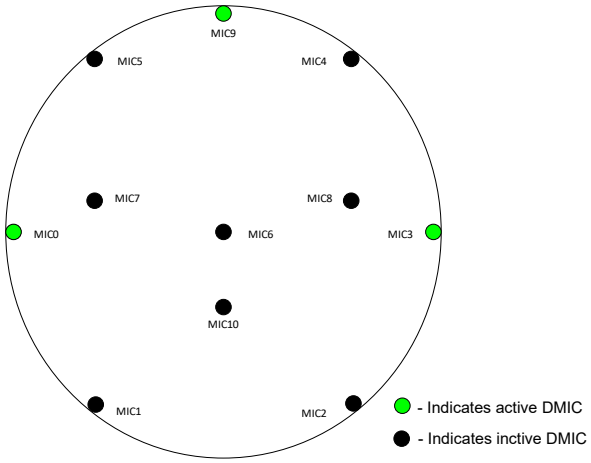

Figure 5. 3DMIC[A] configuration

3DMIC[B] configuration

Table 12. 3DMIC[B] configuration

Part identifier	DMIC	Active Data and Clock signal
U1	DMIC0	DATA01 and CLK01

Table continues on the next page...

Table 12. 3DMIC[B] configuration (continued)

Part identifier	DMIC	Active Data and Clock signal
U5	DMIC2	
U8	DMIC4	DATA23 and CLK23

The figure below shows the 3DMIC[B] configuration.

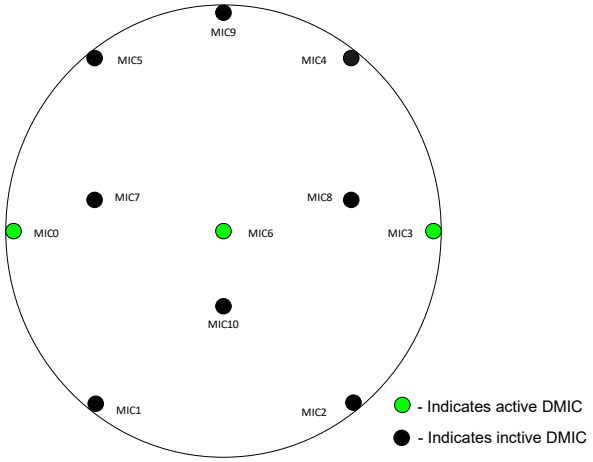

Figure 6. 3DMIC[B] configuration

3DMIC[C] configuration

Table 13. 3DMIC[C] configuration

Part identifier	DMIC	Active Data and Clock signal
U1	DMIC0	DATA01 and CLK01
U6	DMIC3	
U10	DMIC6	DATA23 and CLK23

The figure below shows the 3DMIC[C] configuration.

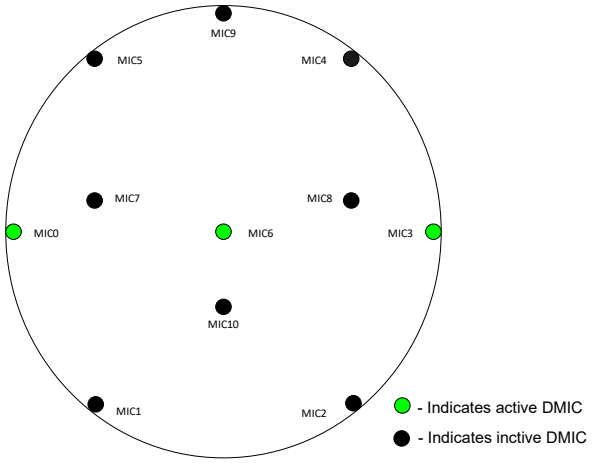

Figure 7. 3DMIC[C] configuration

4DMIC[A] configuration

Table 14. 4DMIC[A] configuration

Part identifier	DMIC	Active Data and Clock signal
U1	DMIC0	DATA01 and CLK01
U5	DMIC2	
U8	DMIC4	DATA23 and CLK23
U10	DMIC6	

The figure below shows the 4DMIC[A] configuration.

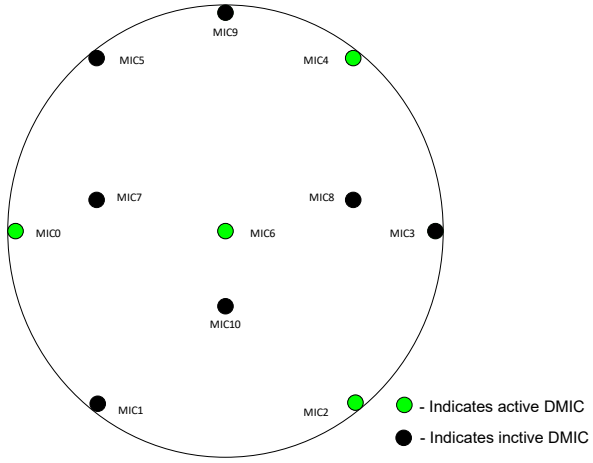

Figure 8. 4DMIC[A] configuration

4DMIC[B] configuration

Table 15. 4DMIC[B] configuration

Part identifier	DMIC	Active Data and Clock signal
U3	DMIC1	DATA01 and CLK01
U5	DMIC2	
U11	DMIC7	DATA23 and CLK23
U2	DMIC8	

The figure below shows the 4DMIC[B] configuration.

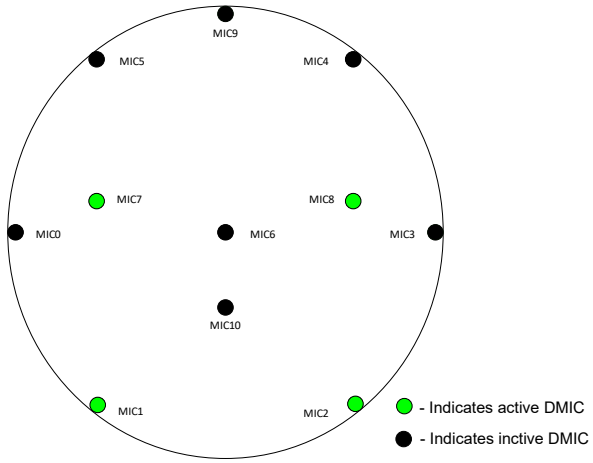

Figure 9. 4DMIC[B] configuration

5DMIC configuration

Table 16. 5DMIC configuration

Part identifier	DMIC	Active Data and Clock signal
U3	DMIC1	DATA01 and CLK01
U5	DMIC2	
U11	DMIC7	DATA23 and CLK23
U2	DMIC8	
U7	DMIC10	DATA45 and CLK45

The figure below shows the 5DMIC configuration.

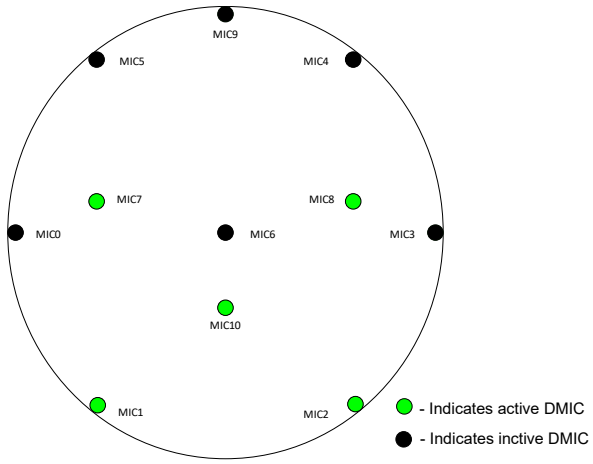

Figure 10. 5DMIC configuration

6DMIC configuration

Table 17. 6DMIC configuration

Part identifier	DMIC	Active Data and Clock signal
U1	DMIC0	DATA01 and CLK01
U3	DMIC1	
U5	DMIC2	DATA23 and CLK23
U6	DMIC3	
U8	DMIC4	DATA45 and CLK45
U9	DMIC5	

The figure below shows the 6DMIC configuration.

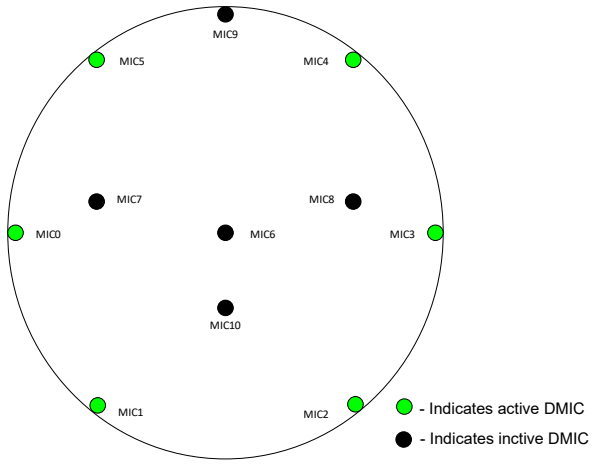

Figure 11. 6DMIC configuration

7DMIC configuration

Table 18. 7DMIC configuration

Part identifier	DMIC	Active Data and Clock signal
U1	DMIC0	DATA01 and CLK01
U3	DMIC1	
U5	DMIC2	DATA23 and CLK23
U6	DMIC3	
U8	DMIC4	DATA45 and CLK45
U9	DMIC5	
U10	DMIC6	DATA67 and CLK67

The figure below shows the 7DMIC configuration.

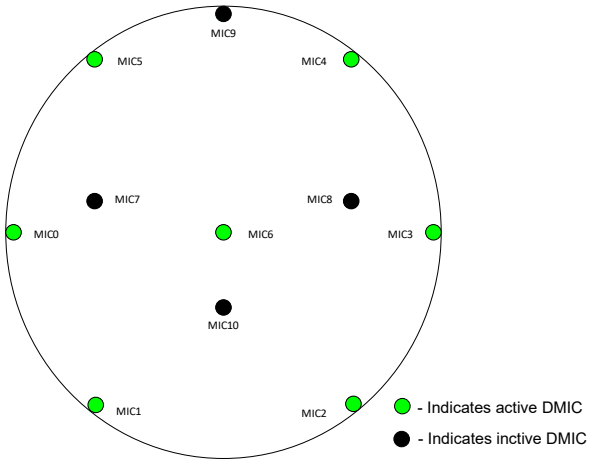

Figure 12. 7DMIC configuration

8DMIC configuration

Table 19. 8DMIC configuration

Part identifier	DMIC	Active Data and Clock signal
U1	DMIC0	DATA01 and CLK01
U3	DMIC1	
U5	DMIC2	DATA23 and CLK23
U6	DMIC3	
U8	DMIC4	DATA45 and CLK45
U9	DMIC5	
U10	DMIC6	DATA67 and CLK67
U7	DMIC10	

The figure below shows the 8DMIC configuration.

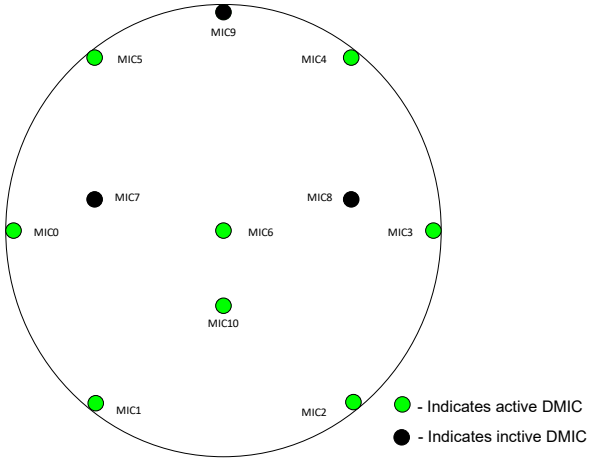

Figure 13. 8DMIC configuration

DMIC configuration and jumpers setting

The below table describes the jumpers configurations required for different DMIC configurations.

Table 20. DMIC configuration and jumpers setting

DMIC configuration	Jumpers (to be shorted)					Note
6 DMIC, 7 DMIC, 8 DMIC	J3	J4	J8	J9	J12	For Jumpers setting detail, see Jumpers.
2 DMIC, 3 DMIC[A], 3 DMIC[C]	J6	J9	J10		-	
3 DMIC[B], 4 DMIC[A]	J7	J9	J10	J11	-	
4 DMIC[B], 5 DMIC	J2	J7	J8	J13	-	

2.2.2 DMIC data switch

Four SPST switches(ADG711) are used on the board to switch DMICs data out as an input for the main board.

The following table describes the data switches.

Table 21. DMIC data switch matrix

Part identifier	Input Data	Output data	Jumpers used (see Jumpers)
U12	Input data from: • DMIC 0 • DMIC 1 • DMIC 2 • DMIC 3	DATA01	J6, J7, J8, J9
U15	Input data from: • DMIC 2 • DMIC 3 • DMIC 4 • DMIC 6	DATA23	J11, J12, J13
U18	Input data from: • DMIC 7 • DMIC 8 • DMIC 9 • DMIC 10	DATA 45	J6, J14
U20	Input data from: • DMIC 4 • DMIC 5 • DMIC 6 • DMIC 10	DATA67	J12

2.2.3 DMIC clock switch

Four SPST switches (ADG711) are used to switch clocks coming from the main board as an input to different DMICs on the 8CH-DMIC board.

The following table describes the clock switches.

Table 22. DMIC clock switch matrix

Part identifier	Input clock	Output clock	Jumpers used (see Jumpers)
U13	Four input clocks: • CLK01 • CLK01 • CLK01 • CLK01 or CLK23 [depending upon Jumper J5 setting]	Clock for: • DMIC0 • DMIC1 • DMIC2	J7, J8, J9, J12
U16	Four input clocks: • CLK01 • CLK01 or CLK23 [depending upon Jumper J5 setting] • CLK01 or CLK23 [depending upon Jumper J5 setting] • CLK45 [depending upon J14 jumper setting]	Clock for: • DMIC3 • DMIC4	J6, J11, J12
U19	Four input clocks: • CLK45 [depending upon J14 and J15 jumpers setting] • CLK23 [Or CLK01 depending upon J5 jumper setting] • CLK67 [depending upon J14 and J15 jumpers setting] • CLK23 [Or CLK01 depending upon J5 jumper setting]	Clock for: • DMIC5 • DMIC6 • DMIC7	J12, J10, J13, J12
U21	Four input clocks: • CLK23 [Or CLK01 depending upon J5 jumper setting] • CLK23 [Or CLK01 depending upon J5 jumper setting] • CLK45 [depending upon J14 and J15 jumpers setting] • CLK67 [depending upon J14 and J15 jumpers setting]	Clock for: • DMIC 8 • DMIC 9 • DMIC 10	J13, J6, J12

2.2.3.1 Clock configuration jumper settings

The following table describes the different clock configurations depending upon J5, J14, and J15 jumper settings.

Table 23. Clock configuration jumper settings

Clock In	000	001	010	011	100	101	110	111
	Config 1	Config 2	Config 3	Config 4	Config 5	Config 6	Config 7	Config 8
	J5:2-3	J5:2-3	J5:2-3	J5:2-3	J5:1-2	J5:1-2	J5:1-2	J5:1-2
	J14:2-3	J14:2-3	J14:1-2	J14:1-2	J14:2-3	J14:2-3	J14:1-2	J14:1-2
	J15:2-3	J15:1-2	J15:2-3	J15:1-2	J15:2-3	J15:1-2	J15:2-3	J15:1-2
CLK01	CLK01	CLK01	CLK01	CLK01	CLK01	CLK01	CLK01	CLK01
CLK23	CLK23	CLK23	CLK23	CLK23	CLK01	CLK01	CLK01	CLK01
CLK45	CLK45	CLK45	CLK01	CLK01	CLK45	CLK45	CLK01	CLK01
CLk67	CLk67	CLK45	CLk67	CLK01	CLk67	CLK45	CLk67	CLK01

NOTE

When using the 8CH-DMIC board with the i.MX RT600 EVK (MIMXRT685-AUD-EVK) board, the codec device on the MIMXRT685-AUD-EVK board must have the MCLK clock frequency reduced to 4.096 MHz and the Input Sample Rate (LRCK) must be reduced to 16 kHz. This change in clock frequency and LRCK maintains compliance of the MIMXRT685-AUD-EVK board with mandatory FCC and EU EMC limitations. Failure to do so will cause the MIMXRT685-AUD-EVK board to exceed FCC and EU EMC limits. It is the responsibility of the end user to comply with this requirement. The end user assumes all responsibility for not complying with this requirement.

Appendix A
Revision history

The table below summarizes the revisions to this document.

Table 24. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 2	15 March 2022	Clock configuration jumper settings	Added note.
Rev. 1	12 January 2022	-	Initial public release.

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