

Product data sheet

1. General description

An AC Thyristor power switch with very high noise immunity and over-voltage protection configured for negative gate triggering in a SOT96-1 (SO8) small surface-mountable plastic package

2. Features and benefits

- Exclusive negative gate triggering
- Full cycle AC conduction
- High noise immunity
- · Remote gate separates the gate driver from the effects of the load current
- Surface-mountable package
- Very sensitive gate for lowest gate trigger current
- · Safe clamping of low energy over-voltage transients
- · Self-protective turn-on during high energy voltage transients

3. Applications

- Fan motor circuits
- Pump motor circuits
- Lower-power highly inductive, resistive and safety loads

4. Quick reference data

Table 1. Qui	ck reference data					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DRM}	repetitive peak off- state voltage		-	-	600	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{amb} ≤ 100 °C; <u>Fig. 1;</u> <u>Fig. 2</u>	-	-	0.2	A
I _{TSM}	non-repetitive peak on- state current	full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms	-	-	8.8	A
		full sine wave; T _{j(init)} = 25 °C; t _p = 20 ms; <u>Fig. 3</u> ; <u>Fig. 4</u>	-	-	8	A
Tj	junction temperature		-	-	125	°C
V _{PP}	peak pulse voltage	T _j = 25 °C; non-repetitive, off-state; <u>Fig. 5</u>	-	-	2	kV
Static chara	acteristics	·	-			
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; <u>Fig. 7</u>	0.5	-	5	mA
		1				

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; <u>Fig. 7</u>	0.5	-	5	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	20	mA
V _T	on-state voltage	I _T = 0.3 A; T _j = 25 °C; <u>Fig. 10</u>	-	-	1.2	V
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 125 °C	650	-	-	V
Dynamic cha	rateristics	·				_
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 11	300	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	$\label{eq:VD} \begin{array}{l} V_D = 400 \; V; \; T_j = 125 \; ^\circ C; \; I_{T(RMS)} = 1 \; A; \\ dV_{com}/dt = 15 \; V/\mu s; \; gate \; open \; circuit; \\ \hline Fig. \; 12; \; Fig. \; 13 \end{array}$	0.15	-	-	A/ms

5. Pinning information

Table 2. Pinning information								
Pin	Symbol	Description	Simplified outline	Graphic symbol				
1	n.c.	not connected	8 <u>8 8 8 8 8</u> 5	LD				
2	LD	Load						
3	n.c.	not connected		G −0 ⊭↓				
4	n.c.	not connected		CM 001aaj924				
5	G	Gate	SO8 (SOT96-1)					
6	СМ	Common						
7	СМ	Common						
8	n.c.	not connected						

6. Ordering information

Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
ACT102H-600D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1			



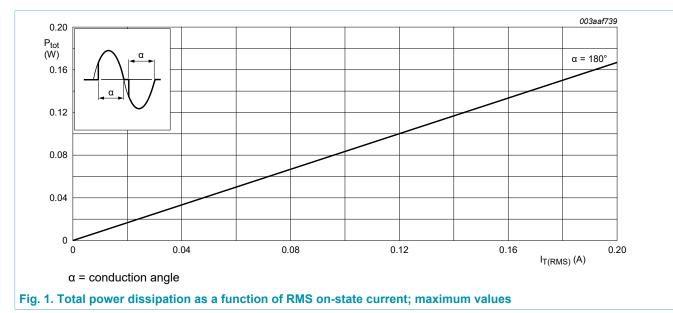
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7. Limiting values

Table 4. Limiting values

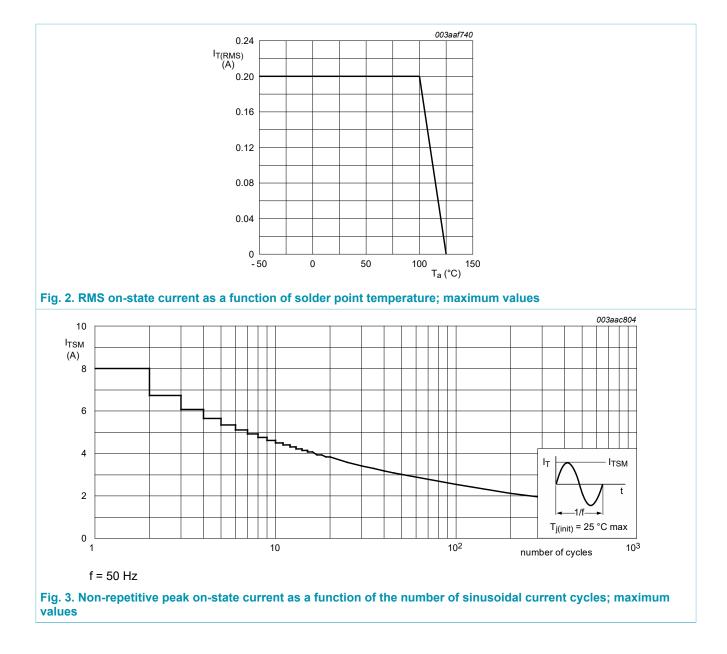
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		-	600	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{amb} ≤ 100 °C; <u>Fig. 1;</u> <u>Fig. 2</u>	-	0.2	A
I _{TSM}	non-repetitive peak on-	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms	-	8.8	А
state curr	state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 3; Fig. 4	-	8	A
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	0.31	A²s
dl _T /dt	rate of rise of on-state current	I _G = 10 mA	-	50	A/µs
I _{GM}	peak gate current	t = 20 μs	-	1	А
P _{GM}	peak gate power		-	2	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	150	°C
Tj	junction temperature		-	125	°C
V _{PP}	peak pulse voltage	T _j = 25 °C; non-repetitive, off-state; <u>Fig. 5</u>	-	2	kV



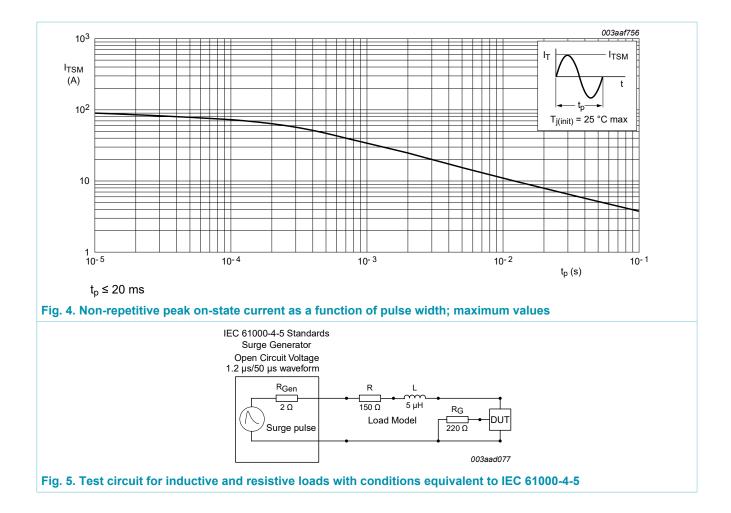
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8. Thermal characteristics

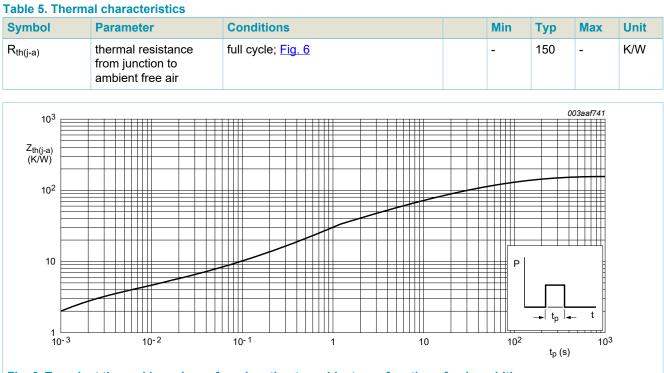
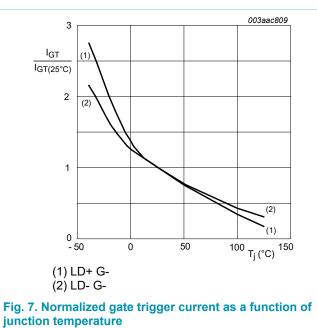


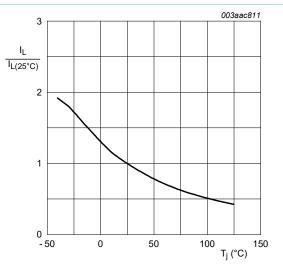
Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse width

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9. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; <u>Fig. 7</u>	0.5	-	5	mA
		V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; <u>Fig. 7</u>	0.5	-	5	mA
I _L lat	latching current	V _D = 12 V; I _G = 100 mA; LD+ G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	25	mA
		V _D = 12 V; I _G = 100 mA; LD- G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	25	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	20	mA
V _T	on-state voltage	I _T = 0.3 A; T _j = 25 °C; <u>Fig. 10</u>	-	-	1.2	V
V _{GT}	gate trigger voltage	V _D = 400 V; I _T = 100 mA; T _j = 125 °C	0.15	-	-	V
		V _D = 12 V; I _T = 100 mA; T _j = 25 °C	-	-	0.9	V
I _D	off-state current	V _D = 600 V; T _j = 25 °C	-	-	2	μA
		V _D = 600 V; T _j = 125 °C	-	-	0.2	mA
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 125 °C	650	-	-	V
Dynamic ch	narateristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 11	300	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	V_D = 400 V; T _j = 125 °C; I _{T(RMS)} = 1 A; dV _{com} /dt = 15 V/µs; gate open circuit; Fig. 12; Fig. 13	0.15	-	-	A/ms





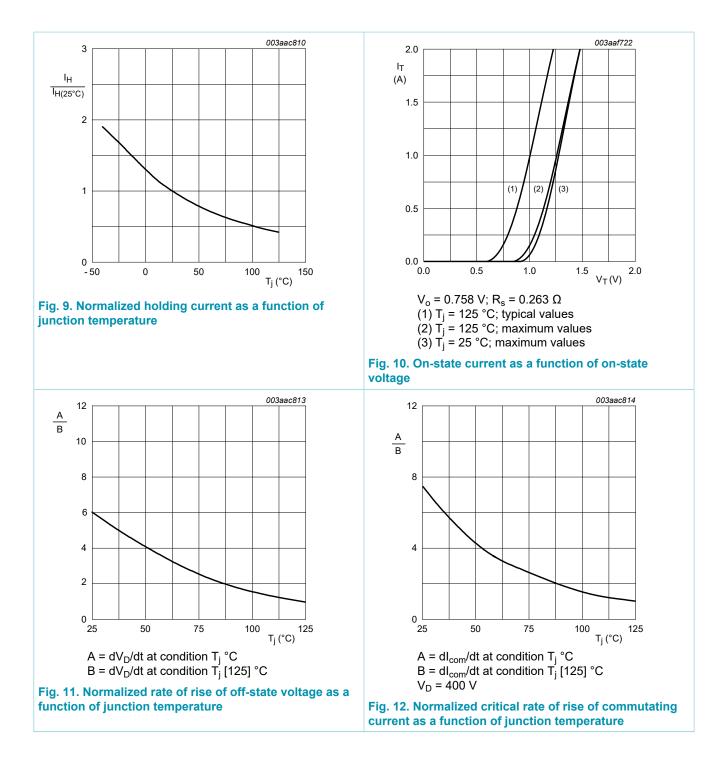


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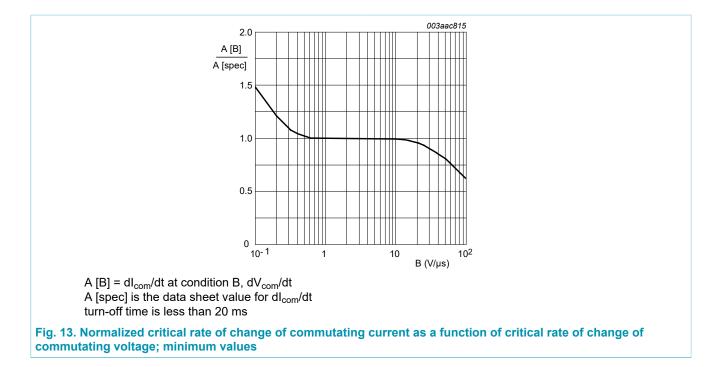
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10. Package outline

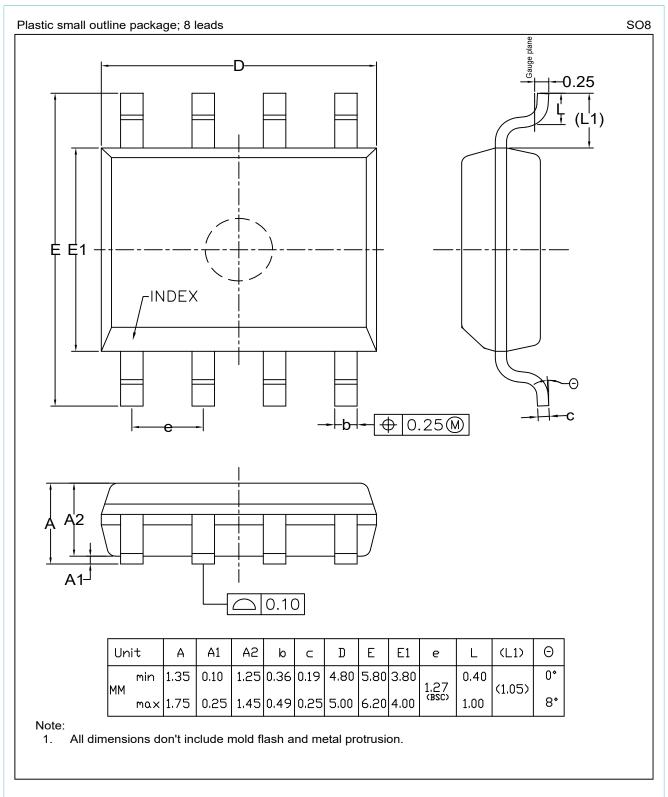


Fig. 14. Package outline SO8 (SOT96-1)

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11. Legal information

Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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