BAP64LX

Silicon PIN diode

Rev. 6 — 11 December 2018 Product data sheet

1 Product profile

1.1 General description

Planar PIN diode in a SOD882D leadless ultra small plastic SMD package.

1.2 Features and benefits

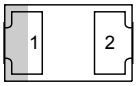
- High voltage, current controlled RF resistor for RF attenuators and switches
- Low diode capacitance
- Low forward resistance
- Very low series inductance
- For applications up to 3 GHz
- AEC-Q101 qualified

1.3 Applications

- RF attenuators and switches

2 Pinning information

Table 1. Discrete pinning

Pin	Description	Simplified outline	Symbol
1	cathode [1]	 Transparent top view	 sym006
2	anode		

[1] The marking bar indicates the cathode.

3 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BAP64LX	DFN1006D-2	leadless ultra small plastic package; 2 terminals; body 1 x 0.6 x 0.4 mm	SOD882D

4 Marking

Table 3. Marking codes

Type number	Marking code[1]
BAP64LX	1111 1111

[1] For SOD882D binary marking code description, see Figure 1.

4.1 Binary marking code description

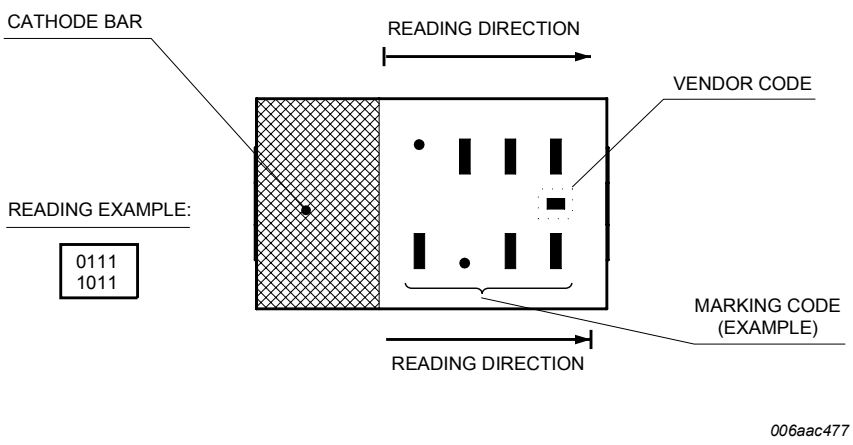


Figure 1. SOD882D binary marking code description example

5 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_R	reverse voltage		-	60	V
I_F	forward current		-	100	mA
P_{tot}	total power dissipation	$T_{sp} \leq 90$ °C	-	150	mW
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-65	+150	°C

6 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}sp)}$	thermal resistance from junction to solder point		56	K/W

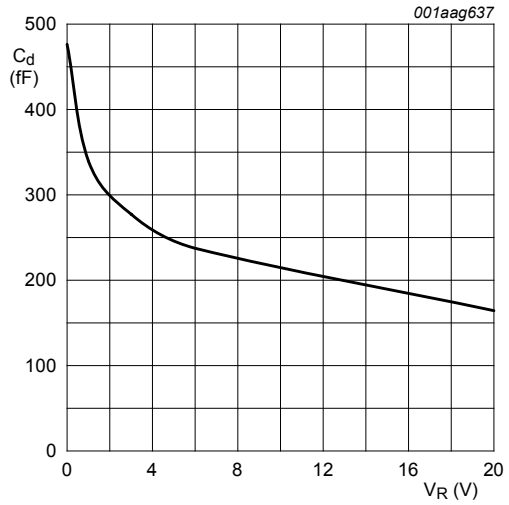
7 Characteristics

Table 6. Characteristics

T_{amb} = 25 °C unless otherwise specified.

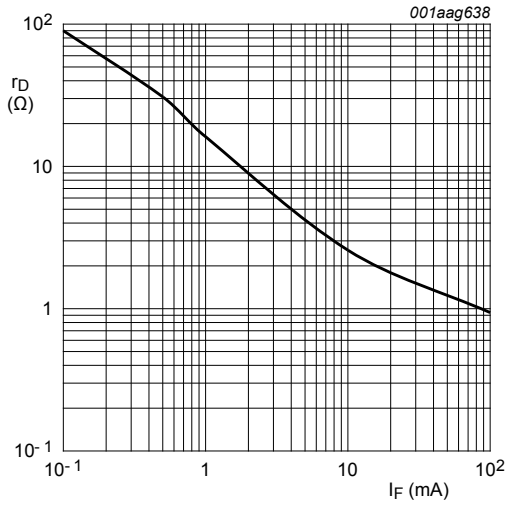
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_F	forward voltage	I_F = 100 mA	-	0.95	1.1	V
I_R	reverse current	V_R = 60 V	-	-	100	nA
C_d	diode capacitance	see Figure 2; f = 1 MHz;				
		V_R = 0 V	-	0.48	-	pF
		V_R = 1 V	-	0.34	-	pF
		V_R = 20 V	-	0.17	0.30	pF
r_D	diode forward resistance	see Figure 3; f = 100 MHz;				
		I_F = 0.5 mA	-	31	50	Ω
		I_F = 1 mA	-	16	26	Ω
		I_F = 10 mA	-	2.6	4.4	Ω
		I_F = 100 mA	-	0.9	1.5	Ω
ISL	isolation	see Figure 4; V_R = 0 V;				
		f = 900 MHz	-	22	-	dB
		f = 1800 MHz	-	16	-	dB
		f = 2450 MHz	-	14	-	dB
L_{ins}	insertion loss	see Figure 5; I_F = 0.5 mA;				
		f = 900 MHz	-	2.15	-	dB
		f = 1800 MHz	-	2.13	-	dB
		f = 2450 MHz	-	2.14	-	dB
L_{ins}	insertion loss	see Figure 5; I_F = 1 mA;				
		f = 900 MHz	-	1.21	-	dB
		f = 1800 MHz	-	1.21	-	dB
		f = 2450 MHz	-	1.22	-	dB
L_{ins}	insertion loss	see Figure 5; I_F = 10 mA;				
		f = 900 MHz	-	0.22	-	dB
		f = 1800 MHz	-	0.23	-	dB
		f = 2450 MHz	-	0.24	-	dB
L_{ins}	insertion loss	see Figure 5; I_F = 100 mA;				
		f = 900 MHz	-	0.09	-	dB
		f = 1800 MHz	-	0.1	-	dB
		f = 2450 MHz	-	0.11	-	dB
T_L	charge carrier life time	when switched from I_F = 10 mA to I_R = 6 mA; R_L = 100 Ω; measured at I_R = 3 mA	-	1.0	-	µs
L_S	series inductance	I_F = 100 mA; f = 100 MHz	-	0.4	-	nH

7.1 Graphics



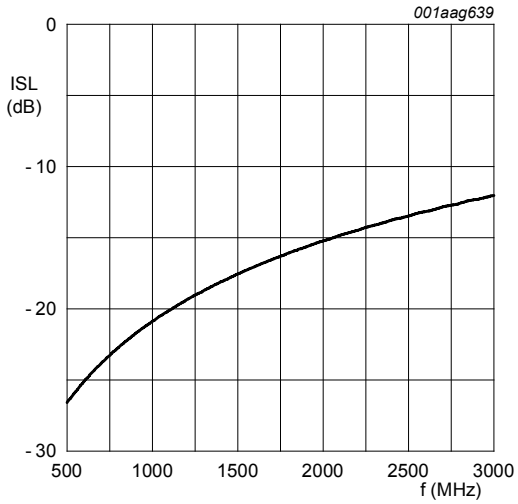
f = 1 MHz; T_j = 25 °C.

Figure 2. Diode capacitance as a function of reverse voltage; typical values



f = 100 MHz; T_j = 25 °C.

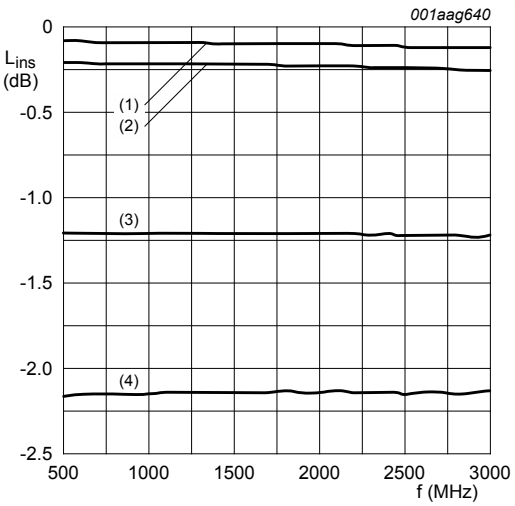
Figure 3. Forward resistance as a function of forward current; typical values



T_{amb} = 25 °C

Diode zero biased and inserted in series with a 50 Ω stripline circuit

Figure 4. Isolation of the diode as a function of frequency; typical values



T_{amb} = 25 °C

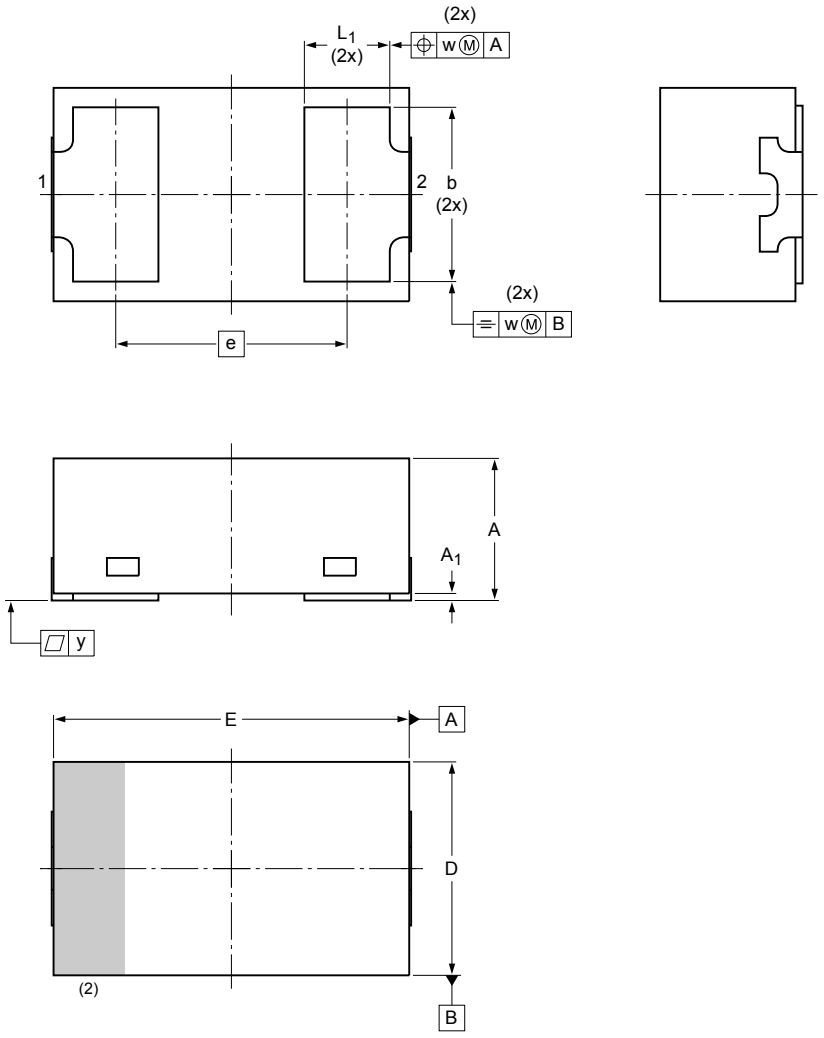
1. I_F = 100 mA
2. I_F = 10 mA
3. I_F = 1 mA
4. I_F = 0.5 mA

Diode inserted in series with a 50 Ω stripline circuit and biased via the analyzer Tee network

Figure 5. Insertion loss of the diode as a function of frequency; typical values

8 Package outline

DFN1006D-2: Leadless ultra small plastic package; 2 terminals; body 1 x 0.6 x 0.4 mm **SOD882D**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	L_1	w	y
mm	max	0.4	0.04	0.55	0.65	1.05		0.30	0.1	0.03
	nom			0.50	0.60	1.00	0.65	0.25		
	min			0.45	0.55	0.95		0.22		

0 0.5 1 mm
scale

Note
1. Dimension including plating thickness.
2. The marking bar indicates the cathode (if applicable).

sod882d_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD882D						~~10-09-27~~ 12-05-01

Figure 6. Package outline SOD882D (DFN1006D-2)

9 Abbreviations

Table 7. Abbreviations

Acronym	Description
AQL	acceptable quality level
PIN	P-type, intrinsic, N-type
SMD	surface mounted device
S4	special inspection level 4

10 Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BAP64LX v.6	20181211	Product data sheet	-	BAP64LX v.5
Modifications:	• changed max value off V_R at limiting values • changed $I_R$conditions at characteristics • adapted the layout of the data sheet			
BAP64LX v.5	20150512	Product data sheet	-	BAP64LX v.4
Modifications:	• AEC-Q101 qualified			
BAP64LX v.4	20140416	Product data sheet	-	BAP64LX v.3
BAP64LX v.3	20140211	Product data sheet	-	BAP64LX v.2
BAP64LX v.2	20130807	Product data sheet	-	BAP64LX v.1
BAP64LX v.1	20070629	Product data sheet	-	-

11 Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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