# DISCRETE SEMICONDUCTORS

# DATA SHEET

# **BFT46**N-channel silicon FET

**Product specification** 

December 1997



**BFT46** 

#### **DESCRIPTION**

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

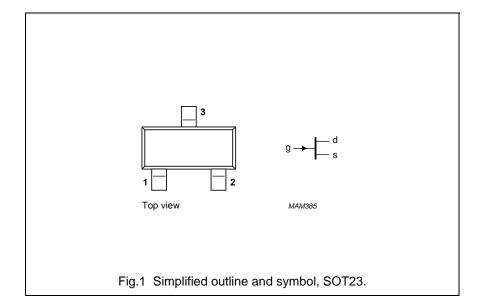
#### **PINNING**

1 = drain

2 = source

3 = gate

**Note :** Drain and source are interchangeable.



#### Marking code

BFT46 = M3p

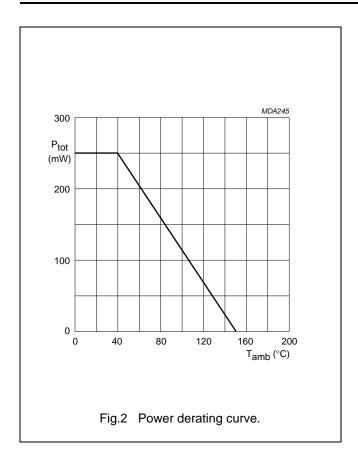
#### **QUICK REFERENCE DATA**

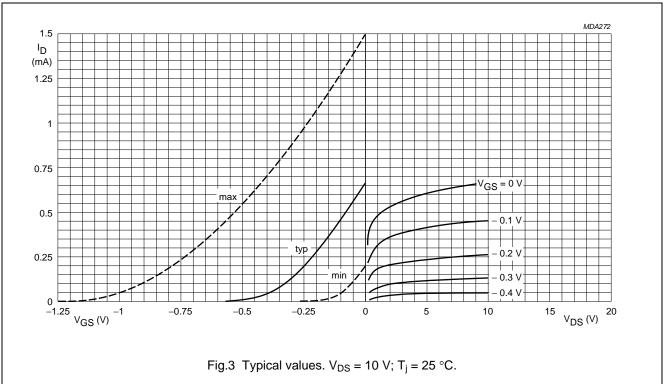
Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to T <sub>amb</sub> = 40 °C	$P_{tot}$	max.	250 mW
Drain current			
$V_{DS} = 10 \text{ V}; V_{GS} = 0$	1	>	0,2 mA
	I <sub>DSS</sub>		1,5 mA
Transfer admittance (common source)			
$I_D = 0.2 \text{ mA}$ ; $V_{DS} = 10 \text{ V}$ ; $f = 1 \text{ kHz}$	y <sub>fs</sub>	>	0,5 mS
Equivalent noise voltage			
$V_{DS}$ = 10 V; $I_{D}$ = 200 $\mu A$ ; B = 0,6 to 100 Hz	$V_n$	<	0,5 μV

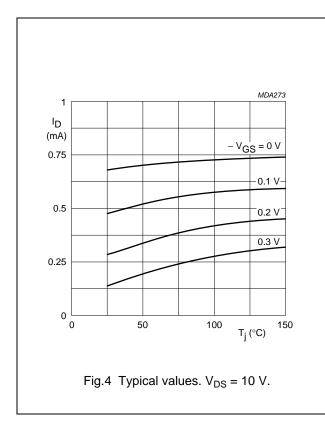
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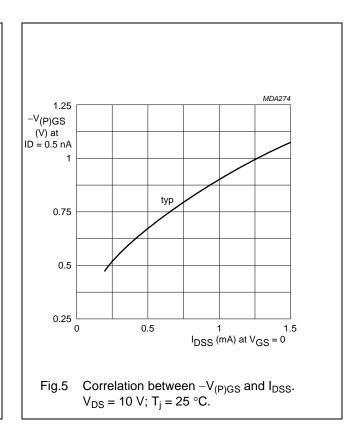
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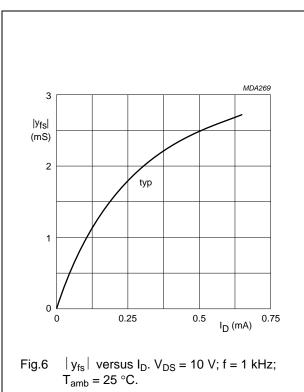
RATINGS			
Limiting values in accordance with the Absolute Maximum Sy	ystem (IEC 134)		
Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	$I_{D}$	max.	10 mA
Gate current	$I_{G}$	max.	5 mA
Total power dissipation up to $T_{amb} = 40  {}^{\circ}C^{(1)}$	$P_{tot}$	max.	250 mW
Storage temperature range	$T_{stg}$	−65 to	+150 °C
Junction temperature	$T_j$	max.	150 °C
THERMAL RESISTANCE			
From junction to ambient <sup>(1)</sup>	R <sub>th j-a</sub>	=	430 K/W
Note			
1. Mounted on a ceramic substrate of 8 mm $\times$ 10 mm $\times$ 0,7	mm.		
CHARACTERISTICS			
$T_j = 25$ °C unless otherwise specified			
Gate cut-off current			
$-V_{GS} = 10 \text{ V}; V_{DS} = 0$	-I <sub>GSS</sub>	<	0,2 nA
Drain current			
$V_{DS} = 10 \text{ V}; V_{GS} = 0$	ı	>	0,2 mA
	I <sub>DSS</sub>	<	1,5 mA
Gate-source voltage			
$I_D = 50 \mu A; V_{DS} = 10 V$	-V <sub>GS</sub>	>	0,1 V
	-v <sub>GS</sub>	<	1,0 V
Gate-source cut-off voltage			
$I_D = 0.5 \text{ nA}; V_{DS} = 10 \text{ V}$	$-V_{(P)GS}$	<	1,2 V
y-parameters at f = 1 kHz;			
$V_{DS} = 10 \text{ V}; V_{GS} = 0; T_{amb} = 25 ^{\circ}\text{C}$			
Transfer admittance	y <sub>fs</sub>	>	1,0 mS
Output admittance	y <sub>os</sub>	<	10 μS
$V_{DS}$ = 10 V; $I_D$ = 200 $\mu$ A; $T_{amb}$ = 25 °C			
Transfer admittance	y <sub>fs</sub>	>	0,5 mS
Output admittance	y <sub>os</sub>	<	5 μS
Input capacitance at f = 1 MHz;			
$V_{DS} = 10 \text{ V}; V_{GS} = 0; T_{amb} = 25 ^{\circ}\text{C}$	$C_{is}$	<	5 pF
Feedback capacitance at f = 1 MHz;			
$V_{DS} = 10 \text{ V}; V_{GS} = 0; T_{amb} = 25 ^{\circ}\text{C}$	$C_{rs}$	<	1,5 pF
Equivalent noise voltage			
$V_{DS}$ = 10 V; $I_D$ = 200 $\mu$ A; $T_{amb}$ = 25 °C			
B = 0.6 to 100 Hz	$V_n$	<	0,5 μV

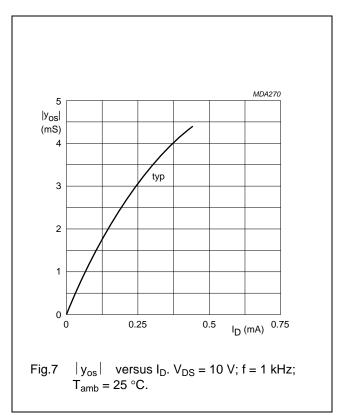


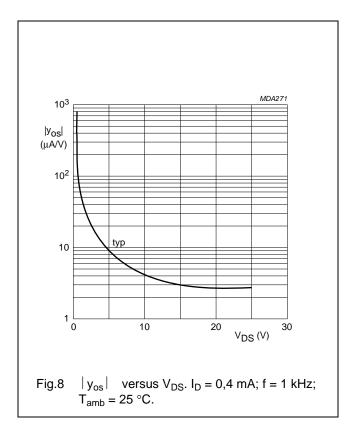


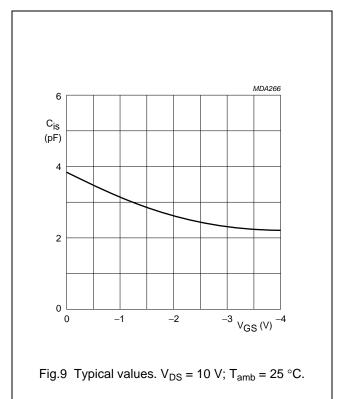


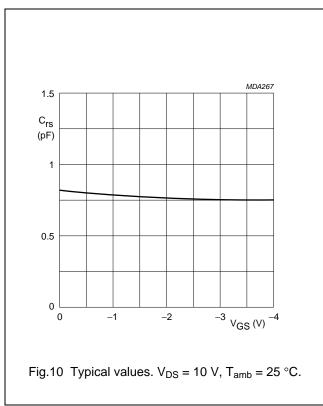


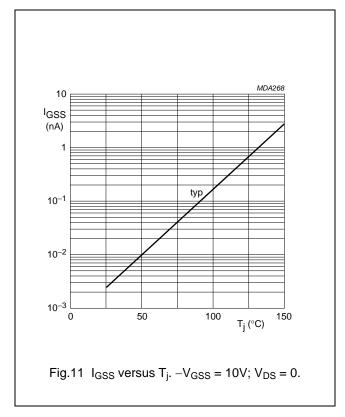


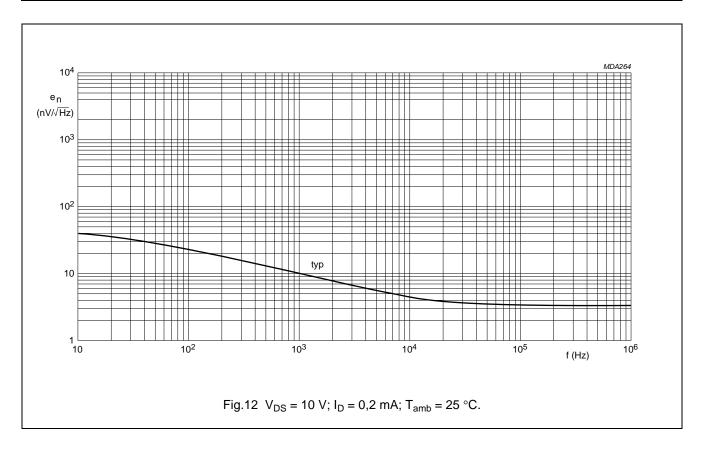


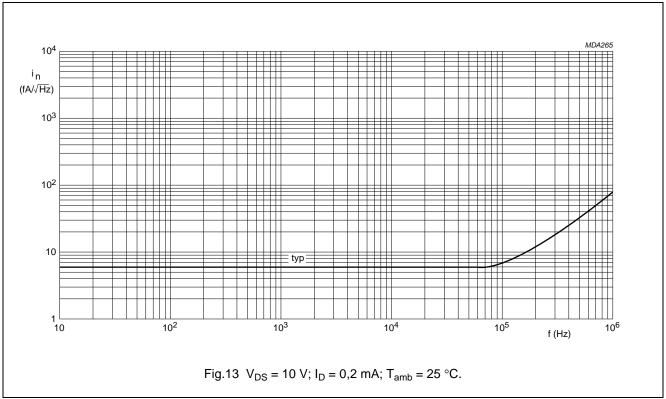










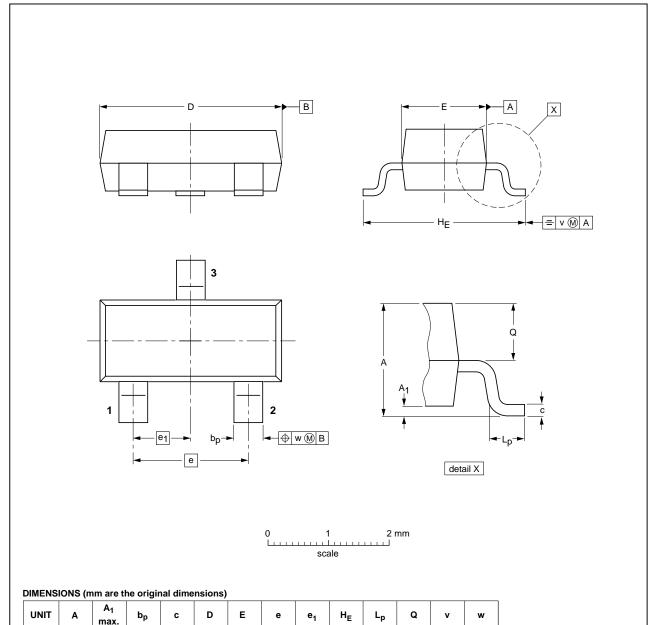


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#### **PACKAGE OUTLINE**

#### Plastic surface-mounted package; 3 leads

SOT23



OUTLINE	REFERENCES		EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	1330E DATE
SOT23		TO-236AB				<del>-04-11-04</del> 06-03-16

0.95

1.9

0.45

0.55

0.2

0.1

max.

0.1

0.48

0.38

0.15

1.1

0.9

mm

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#### **DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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December 1997

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#### **Contact information**

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