

## 1. General description

Planar passivated SCR with sensitive gate in a TO252 (DPAK) surface mountable plastic package. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

## 3. Applications

- General purpose switching
- Protection Circuits

## 4. Quick reference data

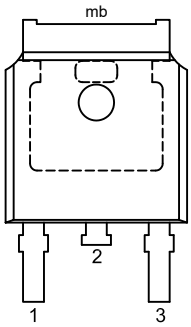

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		[1]	-	-	600 V
$V_{RRM}$	repetitive peak reverse voltage		-	-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	2.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	4	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	35	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 8.3\text{ ms}$	-	-	38	A
$T_j$	junction temperature		[2]	-	-	125 °C
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	15	200	$\mu\text{A}$
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 100\ \Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	-	50	-	$\text{V}/\mu\text{s}$

- [1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.
- [2] Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p style="text-align: center;">DPAK (TO252N)</p>	
2	A	anode[1]		
3	G	gate		
mb	A	mounting base; connected to anode		

[1] It is not possible to connect to pin 2 of the SOT428 package.

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT150S-600R	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	TO252N

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BT150S-600R	150S6

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		[1]	-	600	V
$V_{RRM}$	repetitive peak reverse voltage			-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; Fig. 1		-	2.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; Fig. 2; Fig. 3		-	4	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; Fig. 4; Fig. 5		-	35	A
		half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 8.3\text{ ms}$		-	38	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN		-	6.1	A <sup>2</sup> s
$di_T/dt$	rate of rise of on-state current	$I_G = 50\text{ mA}$		-	50	A/ $\mu$ s
$I_{GM}$	peak gate current			-	2	A
$V_{RGM}$	peak reverse gate voltage			-	5	V
$P_{GM}$	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
$T_{stg}$	storage temperature			-40	150	°C
$T_j$	junction temperature		[2]	-	125	°C

- [1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ $\mu$ s.
- [2] Operation above 110°C may require the use of a gate to cathode resistor of 1k $\Omega$  or less.

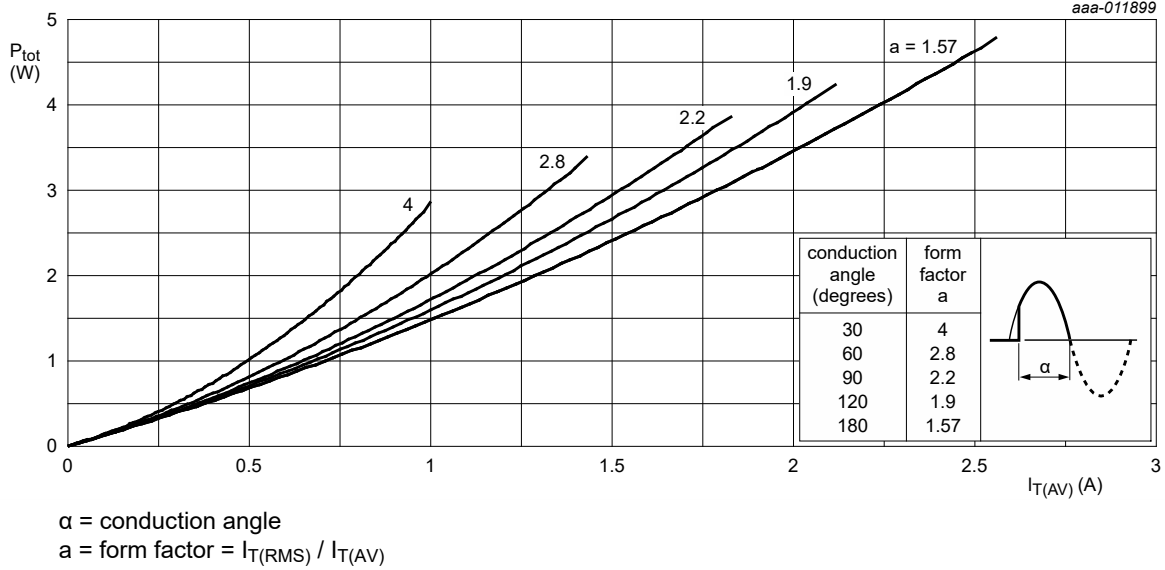


Fig. 1. Total power dissipation as a function of average on-state current; maximum values

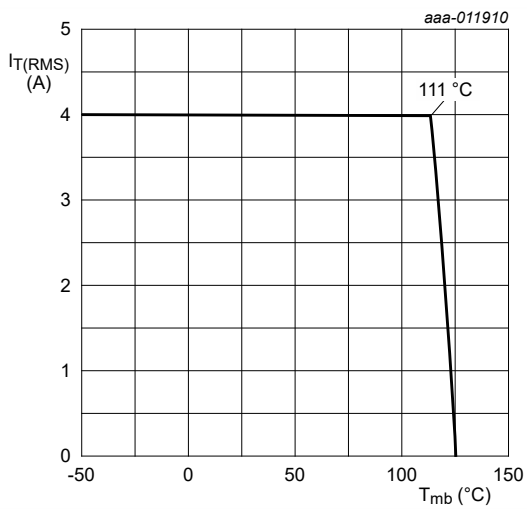


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values

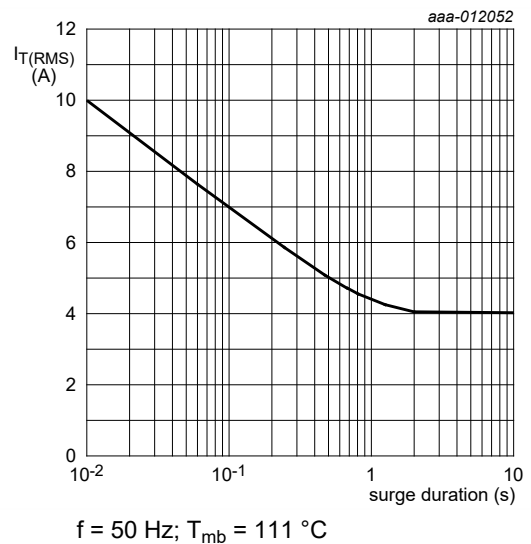


Fig. 3. RMS on-state current as a function of surge duration; maximum values

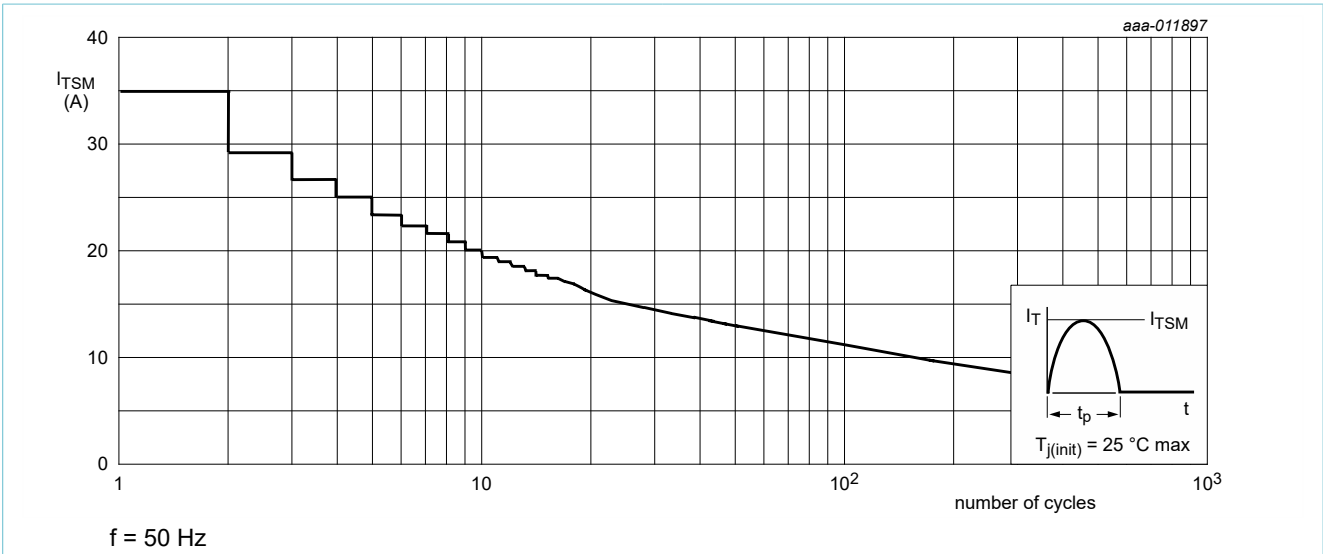


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

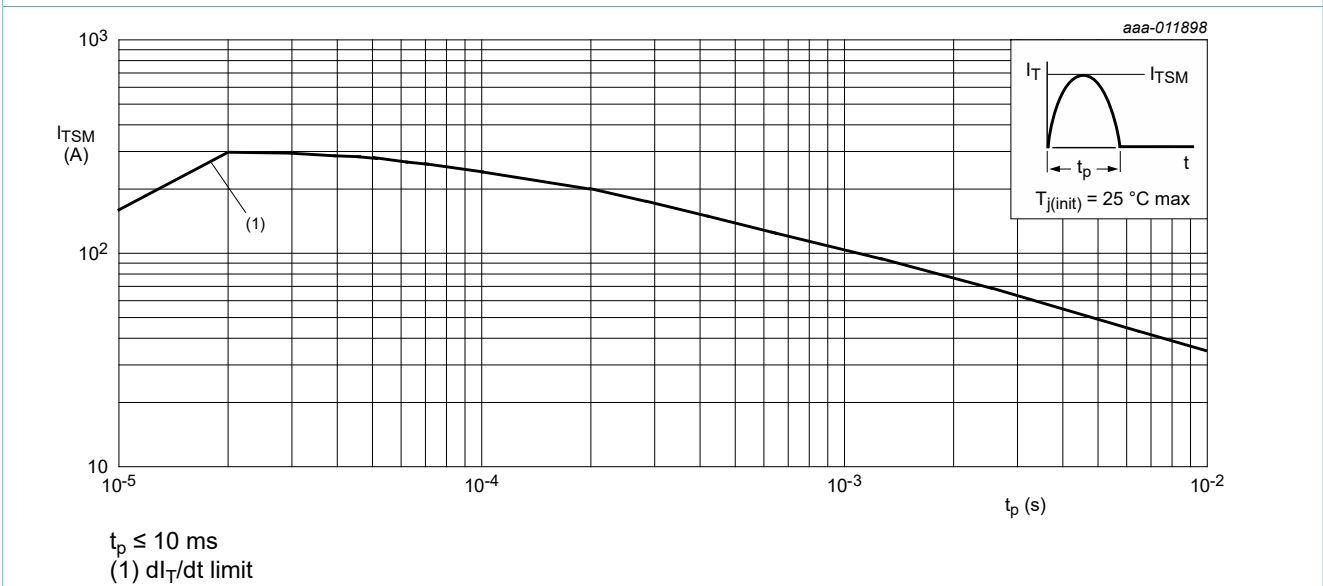


Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 6</a>	-	-	3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint	-	75	-	K/W

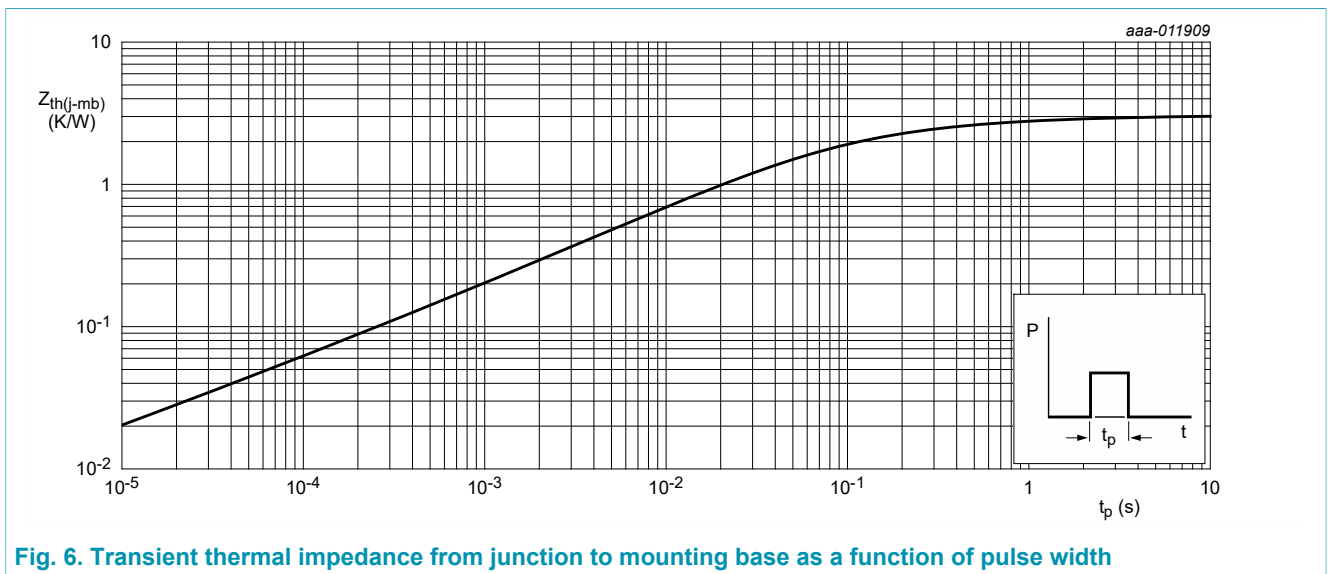
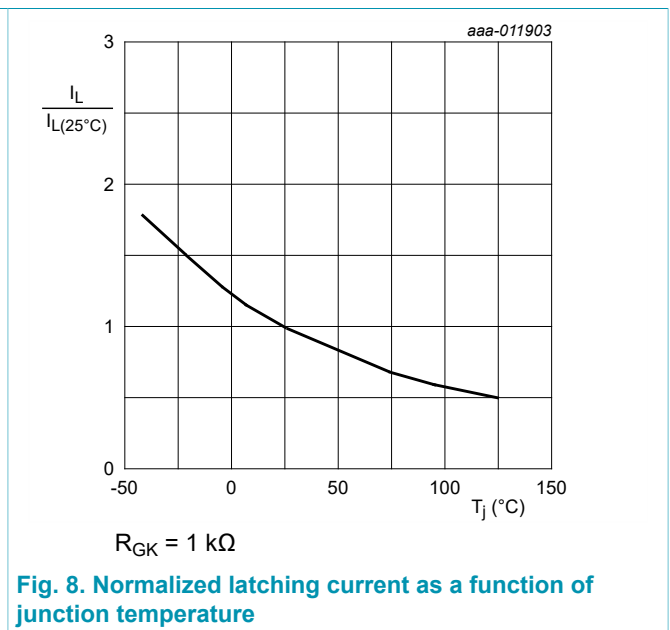
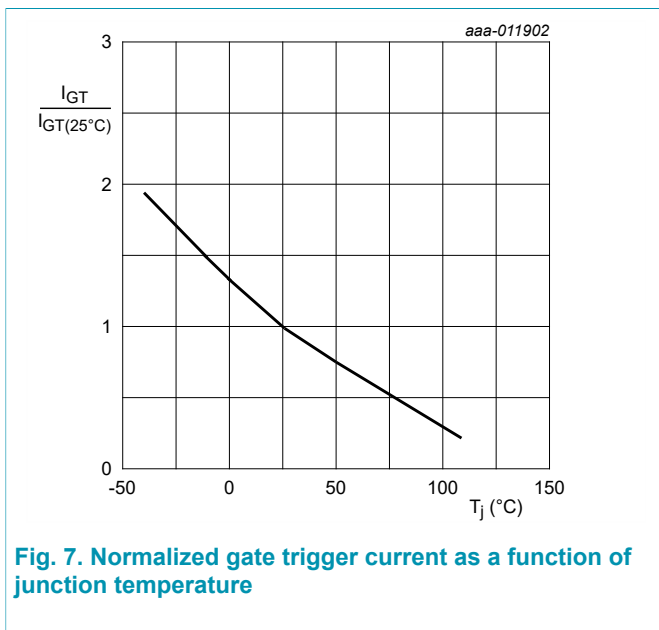


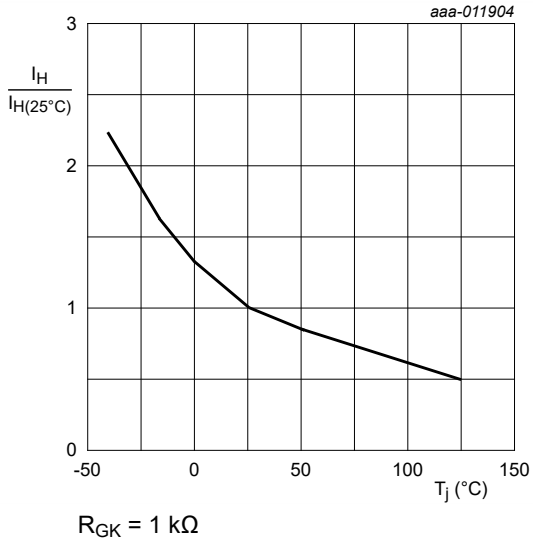
Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

## 10. Characteristics

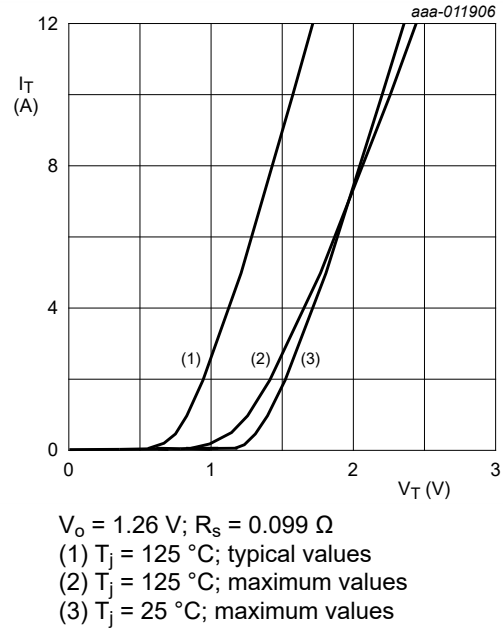
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 7</a>	-	15	200	$\mu\text{A}$
$I_L$	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 8</a>	-	0.17	10	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	0.1	6	mA
$V_T$	on-state voltage	$I_T = 5\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	1.23	1.8	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	0.4	1	V
		$V_D = 600\text{ V}; I_T = 0.1\text{ A}; T_j = 110\text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	0.1	0.2	-	V
$I_D$	off-state current	$V_D = 600\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
$I_R$	reverse current	$V_R = 600\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}; T_j = 125\text{ }^\circ\text{C}; R_{GK} = 100\text{ }\Omega;$ ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	-	50	-	$\text{V}/\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 10\text{ A}; V_D = 600\text{ V}; I_G = 5\text{ mA}; dI_G/dt = 0.2\text{ A}/\mu\text{s}; T_j = 25\text{ }^\circ\text{C}$	-	2	-	$\mu\text{s}$
$t_q$	commutated turn-off time	$V_{DM} = 402\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{TM} = 8\text{ A}; V_R = 10\text{ V}; (dI_T/dt)_M = 10\text{ A}/\mu\text{s}; dV_D/dt = 2\text{ V}/\mu\text{s}; R_{GK(ext)} = 1\text{ k}\Omega; (V_{DM} = 67\%$ of $V_{DRM})$	-	100	-	$\mu\text{s}$

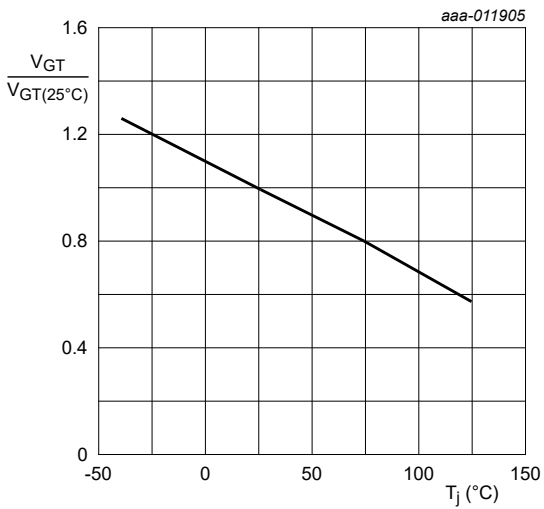




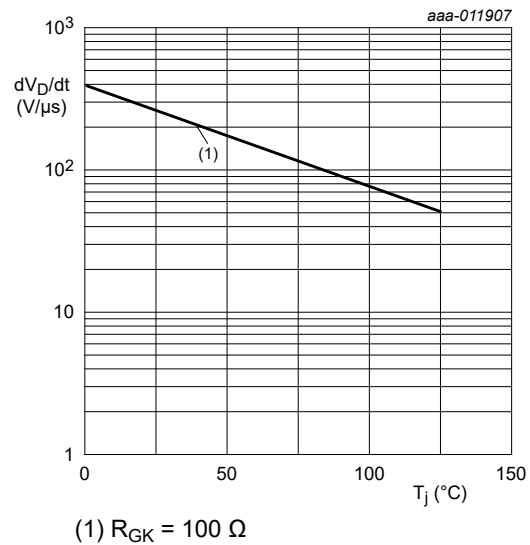
**Fig. 9. Normalized holding current as a function of junction temperature**



**Fig. 10. On-state current as a function of on-state voltage**



**Fig. 11. Normalized gate trigger voltage as a function of junction temperature**



**Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values**



### 11. Package outline

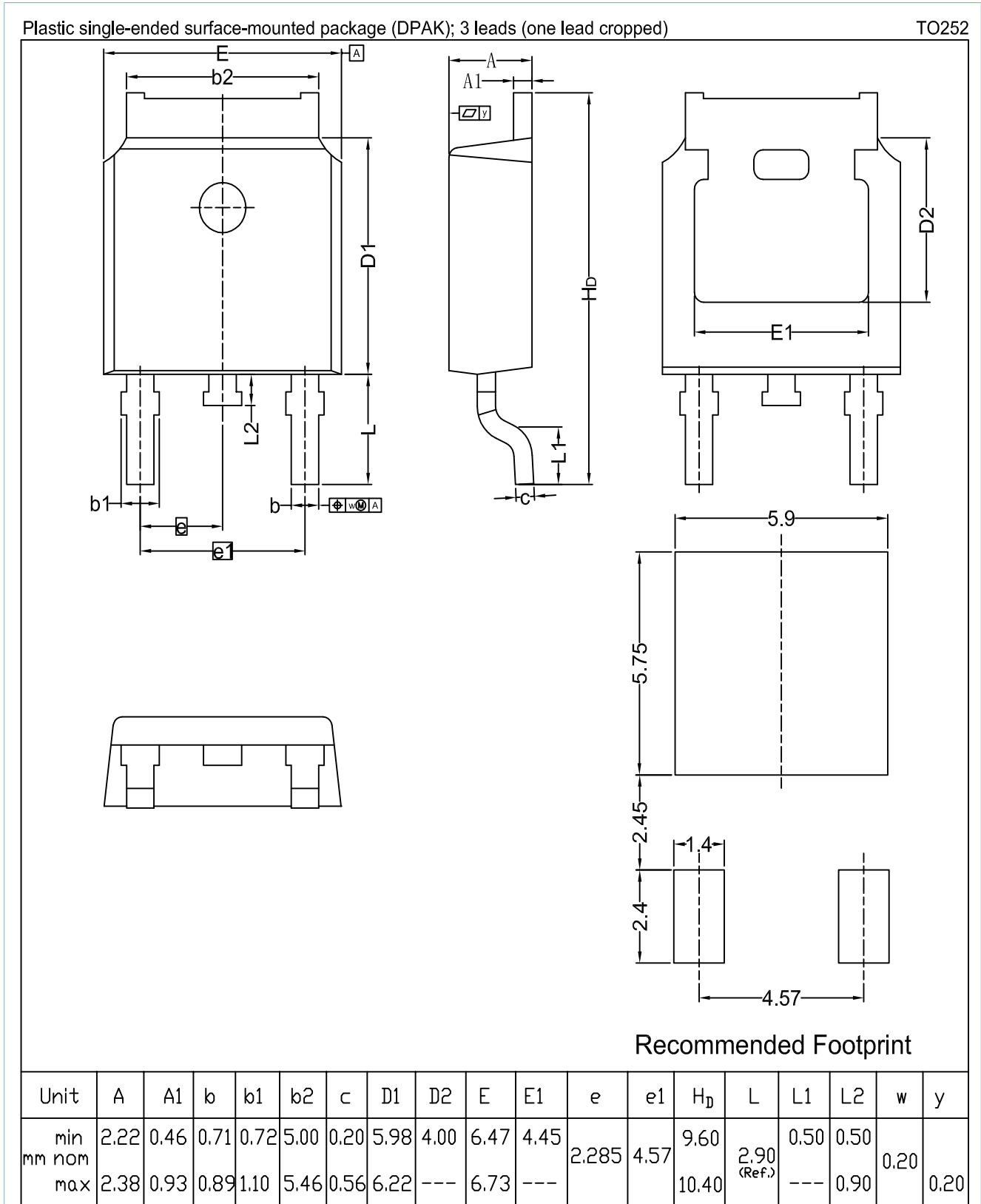


Fig. 13. Package outline DPAK (TO252N)

## 12. Legal information

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