## DISCRETE SEMICONDUCTORS

# DATA SHEET

# BTA216X series B Three quadrant triacs high commutation

**Product specification** 

September 2019



WeEn Semiconductors Product specification

## Three quadrant triacs high commutation

#### BTA216X series B

#### **GENERAL DESCRIPTION**

Planar passivated high commutation triacs in a full pack, plastic envelope intended for use in circuits where high static and dynamic dV/dt and high dl/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature, without the aid of a snubber.

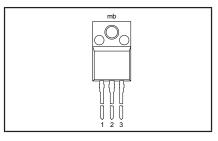
#### **QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
V <sub>DRM</sub>	BTA216X- Repetitive peak off-state voltages RMS on-state current	<b>500B</b> 500	<b>600B</b> 600	<b>800B</b> 800	V A
I <sub>TSM</sub>	Non-repetitive peak on-state current	140	140	140	А

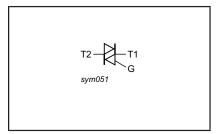
#### **PINNING - SOT186A**

PIN DESCRIPTION	
1	main terminal 1
2	main terminal 2
3	gate
case	isolated

#### PIN CONFIGURATION



#### **SYMBOL**



#### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
$V_{DRM}$	Repetitive peak off-state voltages		-	<b>-500</b> 500 <sup>1</sup>	<b>-600</b> 600 <sup>1</sup>	<b>-800</b> 800	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave;	-		16		Α
I <sub>TSM</sub>	Non-repetitive peak on-state current	$T_{hs} \le 38 ^{\circ}\text{C}$ full sine wave; $T_j = 25 ^{\circ}\text{C}$ prior to surge $t = 20 \text{ms}$	-		140		A
l <sup>2</sup> t	I <sup>2</sup> t for fusing	t = 16.7 ms t = 10 ms	-		150 98		A A <sup>2</sup> s
dl <sub>⊤</sub> /dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20 \text{ A}; I_G = 0.2 \text{ A}; $ $dI_G/dt = 0.2 \text{ A}/\mu\text{s}$			100		A/μs
I <sub>GM</sub>	Peak gate current Peak gate voltage		-		2 5 5		A V
P <sub>GM</sub>	Peak gate vollage Peak gate power		-				W
$P_{G(AV)}^{GM}$	Average gate power	over any 20 ms period	-		0.5		W
$T_{stg}^{stg}$	Storage temperature Operating junction temperature	poriod	-40 -		150 125		°C °C

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<sup>1</sup> Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/ $\mu$ s.

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#### **ISOLATION LIMITING VALUE & CHARACTERISTIC**

 $T_{hs}$  = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>isol</sub>	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C <sub>isol</sub>	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

#### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R <sub>th j-hs</sub>	Thermal resistance junction to heatsink	full or half cycle with heatsink compound without heatsink compound		-	4.0 5.5	K/W K/W
R <sub>th j-a</sub>	Thermal resistance junction to ambient	in free air	-	55	-	K/W

#### STATIC CHARACTERISTICS

 $T_i = 25$  °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>GT</sub>	Gate trigger current <sup>2</sup>	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}$				
·GI	and ingger content	T2+ G+	2	18	50	mA
		T2+ G-	2	21	50	mA
		T2- G-	2	34	50	mA
I <sub>L</sub>	Latching current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}$				
-		T2+ G+	-	31	60	mA
		T2+ G-	-	34	90	mA
		T2- G-	-	30	60	mA
l I <sub>H</sub>	Holding current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}$	-	31	60	mA
V <sub>T</sub>	On-state voltage	$I_{T} = 20 \text{ A}$	-	1.2	1.5	V
$egin{array}{c} I_{H} \\ V_{T} \\ V_{GT} \end{array}$	Gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}$	-	0.7	1.5	V
		$V_D = 400 \text{ V}; I_T = 0.1 \text{ A}; T_L = 125 ^{\circ}\text{C}$	0.25	0.4	<u>-</u> _	V
$  I_D  $	Off-state leakage current	$V_D = V_{DRM(max)}$ ; $T_j = 125 °C$	-	0.1	0.5	mA

#### **DYNAMIC CHARACTERISTICS**

T<sub>i</sub> = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV <sub>D</sub> /dt	Critical rate of rise of	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125 °C;$	1000	4000	-	V/μs
	off-state voltage Critical rate of change of commutating current	exponential waveform; gate open circuit $V_{DM} = 400 \text{ V}$ ; $T_j = 125 ^{\circ}\text{C}$ ; $I_{T(RMS)} = 16 \text{ A}$ ; without snubber; gate open circuit	-	28	-	A/ms
t <sub>gt</sub>	Gate controlled turn-on time	$I_{TM} = 20 \text{ A}$ ; $V_D = V_{DRM(max)}$ ; $I_G = 0.1 \text{ A}$ ; $dI_G/dt = 5 \text{ A}/\mu\text{s}$	-	2	-	μs

<sup>2</sup> Device does not trigger in the T2-, G+ quadrant.

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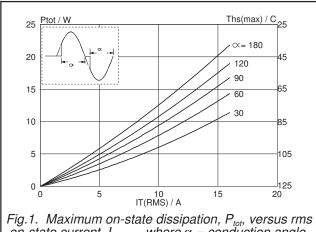


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus rms on-state current,  $I_{T(RMS)}$ , where  $\alpha$  = conduction angle.

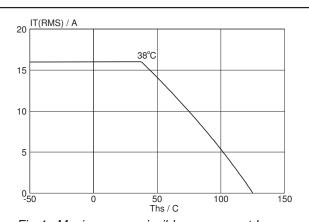


Fig.4. Maximum permissible rms current  $I_{T(RMS)}$ , versus heatsink temperature  $T_{hs}$ .

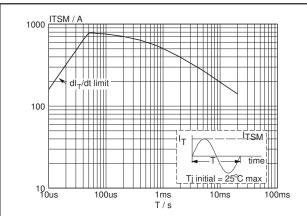


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \le 20$ ms.

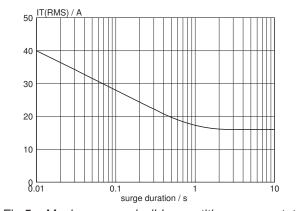


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents, f = 50 Hz;  $T_{hs} \le 38$  °C.

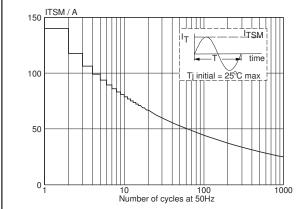


Fig.3. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents, f = 50 Hz.

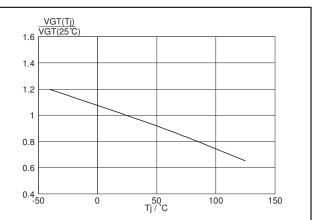
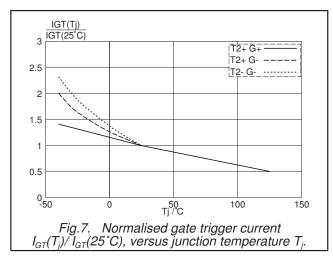


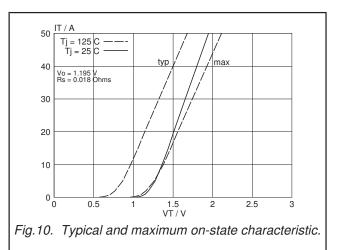
Fig.6. Normalised gate trigger voltage  $V_{GT}(T_i)/V_{GT}(25^{\circ}C)$ , versus junction temperature  $T_i$ 

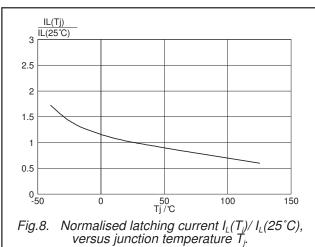
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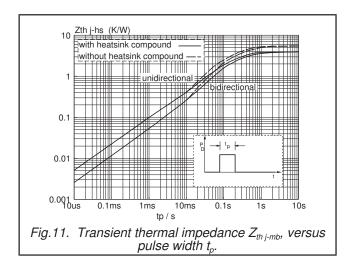
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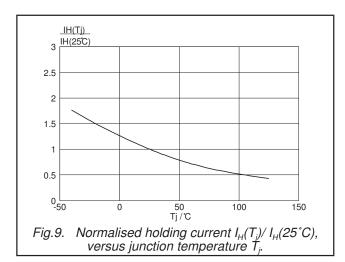
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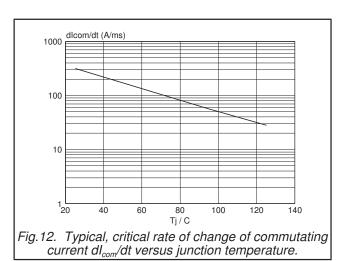








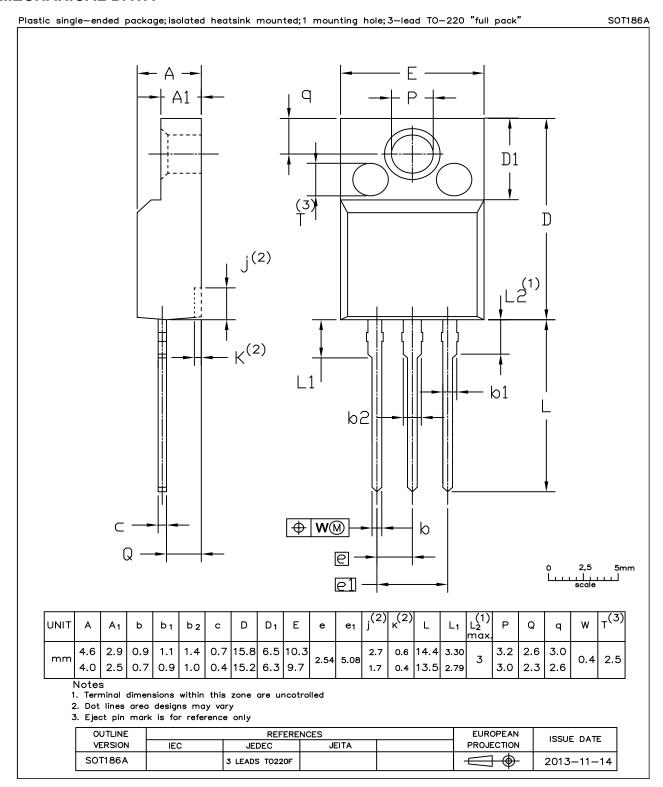




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#### Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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